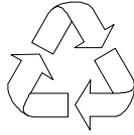


X3 System

Service Guide



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About this Manual

Purpose

This service guide aims to furnish technical information to the service engineers and advanced users when upgrading, configuring, or repairing the X3 system.

Manual Structure

This service guide contains technical information about the X3 system. It consists of three chapters and five appendices.

Chapter 1 System Introduction

This chapter describes the system features and major components. It contains the X3 system board layout, block diagrams, cache and memory configurations, power management and mechanical specifications, and operation theory.

Chapter 2 Major Chipsets

This chapter describes the features and functions of the major chipsets used in the system board, including the Pentium Pro processor. It also includes chipset block diagrams, pin diagrams, and pin descriptions.

Chapter 3 BIOS Setup Utility

This chapter describes the parameters in the BIOS Utility screens.

Appendix A Model Definition

This appendix shows the different configuration options for the X3 system.

Appendix B Spare Parts List

This appendix lists the spare parts for the X3 system with their part numbers and other information.

Appendix C Schematics

This appendix contains the schematic diagrams for the system board.

Appendix D Silk Screen

This appendix illustrates the system board silk screen.

Appendix E BIOS POST Check Points

This appendix lists and describes the BIOS POST check points.

Conventions

The following are the conventions used in this manual:

Text entered by user

Represents text input by the user.

Screen messages

Denotes actual messages that appear onscreen.

, , , etc.

Represent the actual keys that you have to press on the keyboard.



NOTE

Gives bits and pieces of additional information related to the current topic.



WARNING

Alerts you to any damage that might result from doing or not doing specific actions.



CAUTION

Gives precautionary measures to avoid possible hardware or software problems.



IMPORTANT

Reminds you to do specific actions relevant to the accomplishment of procedures.



TIP

Tells how to accomplish a procedure with minimum steps through little shortcuts.

Table of Contents

Chapter 1 System Introduction

1.1	Configuration Overview	1-1
1.1.1	Front Panel	1-1
1.1.2	Rear Panel.....	1-6
1.2	Features	1-7
1.2.1	Intel Pentium Pro Microprocessor.....	1-7
1.2.2	System Architecture	1-8
1.2.3	SCSI Disk Array	1-9
1.2.4	Server Management.....	1-10
1.2.5	Redundant Power Supply Subsystem.....	1-10
1.2.6	Security.....	1-10
1.2.7	Memory Board	1-10
1.2.8	Major Components.....	1-11
1.3	Board Layouts.....	1-12
1.3.1	System Board	1-12
1.3.2	Memory Board	1-13
1.3.3	SCSI Disk Array Backplane Board.....	1-13
1.3.4	RDM Module.....	1-14
1.4	Jumpers and Connectors	1-15
1.4.1	Jumper Settings	1-16
1.4.2	Connector List.....	1-18
1.5	System Board Specifications	1-20
1.6	Hardware Configurations.....	1-21
1.6.1	Memory Configurations	1-21
1.6.2	Video Memory Specification.....	1-23
1.6.3	Video Display Modes and Refresh Rates.....	1-23
1.6.4	Parallel Port Configurations.....	1-24
1.6.5	Serial Port Configurations	1-24
1.6.6	Memory Address Map	1-24
1.6.7	Interrupt Channels Map	1-25
1.6.8	I/O Address Map	1-26
1.7	Block Diagrams.....	1-27

1.7.1	System Block Diagram.....	1-27
1.7.2	Memory Controller Block Diagram.....	1-28
1.7.3	Memory Interleaving Block Diagram	1-29
1.7.4	System Clock Diagram.....	1-30
1.7.5	Interrupt Distribution Logic Diagram	1-31
1.7.6	Dual-processor Operation Diagram	1-32
1.8	Power Requirements.....	1-33
1.8.1	400W Power Supply for IDX-2.....	1-33
1.9	Mechanical Specifications.....	1-35
1.9.1	IDX-2 Housing.....	1-35
1.10	Shipping Configuration.....	1-37
1.11	Cable Connections.....	1-38

Chapter 2 Major Chipsets

2.1	Pentium Pro processor (P6).....	2-1
2.1.1	Features.....	2-1
2.1.2	Pin Diagram.....	2-4
2.1.3	CPU ID	2-5
2.1.4	Signal Types	2-6
2.1.5	Signal Descriptions	2-8
2.2	Memory Interface Component (S82451GX)	2-33
2.2.1	Features.....	2-33
2.2.2	S82451GX Pin Diagram.....	2-34
2.2.3	S82451GX Signal Descriptions	2-35
2.3	Data Path Chipset (S82452GX)	2-36
2.3.1	Features.....	2-36
2.3.2	S82452GX Pin Diagram.....	2-38
2.3.3	S82452GX Signal Descriptions	2-39
2.4	DRAM Control Chipset (S82453GX)	2-41
2.4.1	S82453GX Pin Diagram.....	2-41
2.4.2	S82453GX Signal Descriptions	2-42
2.5	PCI Bridge (S82454GX).....	2-44
2.5.1	Features.....	2-44
2.5.2	S82454GX Block Diagram	2-46

2.5.3	S82454GX Pin Diagram	2-47
2.5.4	S82454GX Signal Descriptions.....	2-48
2.6	SIO (82379AB)	2-51
2.6.1	Features.....	2-51
2.6.2	82379AB Block Diagram	2-53
2.6.3	82379AB Pin Diagram.....	2-54
2.6.4	82379AB Signal Descriptions	2-55
2.7	EISA System Component (82374SB).....	2-64
2.7.1	Features.....	2-64
2.7.2	Block Diagram	2-66
2.7.3	Pin Diagram	2-67
2.7.4	Signal Descriptions	2-68
2.8	PCI-EISA Bridge (82375SB)	2-92
2.8.1	Features.....	2-92
2.8.2	Block Diagram	2-94
2.8.3	Pin Diagram	2-95
2.8.4	Signal Descriptions	2-96
2.9	SCSI Controller (AIC 7880).....	2-111
2.9.1	Features.....	2-111
2.9.2	Block Diagram	2-114
2.9.3	Pin Diagram	2-115
2.9.4	Signal Descriptions	2-116
2.10	ATI 264VT	2-127
2.10.1	Features.....	2-127
2.10.2	Block Diagram	2-128
2.10.3	Pin Diagram	2-129
2.10.4	Signal Descriptions	2-130
2.10.5	Display Modes.....	2-135
2.11	Super I/O Controller (SMC 37C935).....	2-136
2.11.1	Features.....	2-136
2.11.2	Block Diagram	2-138
2.11.3	Pin Diagram	2-139
2.11.4	Signal Descriptions	2-140

Chapter 3 BIOS Setup Utility

3.1	Entering Setup.....	3-1
3.2	System Information.....	3-2
3.2.1	Processor.....	3-3
3.2.2	Processor Speed.....	3-3
3.2.3	Bus Frequency.....	3-3
3.2.4	Internal Cache.....	3-3
3.2.5	External Cache	3-3
3.2.6	Floppy Drive A.....	3-3
3.2.7	Floppy Drive B.....	3-3
3.2.8	IDE Primary Channel Master.....	3-4
3.2.9	IDE Primary Channel Slave	3-4
3.2.10	Total Memory.....	3-4
3.2.11	Serial Port 1.....	3-4
3.2.12	Serial Port 2.....	3-4
3.2.13	Parallel Port.....	3-4
3.2.14	Pointing Device.....	3-4
3.3	Product Information	3-5
3.3.1	Product Name.....	3-5
3.3.2	Main Board ID.....	3-5
3.3.3	Main Board S/N.....	3-5
3.3.4	System BIOS Version	3-5
3.3.5	System BIOS ID.....	3-6
3.3.6	BIOS Release Date.....	3-6
3.4	Disk Drives	3-6
3.4.1	Floppy Drives.....	3-7
3.4.2	IDE Drives	3-8
3.5	Startup Configuration.....	3-10
3.5.1	System POST Mode	3-10
3.5.2	Silent Boot	3-10
3.5.3	Num Lock After Boot.....	3-11
3.5.4	Memory Test.....	3-11
3.5.5	Initialize SCSI Before IDE	3-11
3.5.6	Boot from IDE CD-ROM.....	3-11

3.5.7	System Boot Drive	3-11
3.5.8	MP Compliant Revision.....	3-11
3.6	Advanced Configuration.....	3-12
3.6.1	Onboard Devices Configuration	3-13
3.6.2	PnP/PCI System Configuration	3-17
3.6.3	Memory/Cache Configuration.....	3-19
3.6.4	Non-PnP ISA Device Configuration.....	3-20
3.6.5	Chipset Configuration.....	3-23
3.7	System Security Setup.....	3-25
3.7.1	IDE Disk Drive Control	3-25
3.7.2	Setup Password	3-26
3.7.3	Power-on Password.....	3-28
3.8	Date and Time	3-29
3.8.1	Date	3-29
3.8.2	Time	3-29
3.9	Remote Diagnostic Configuration.....	3-29
3.10	Load Default Settings.....	3-30
3.11	Abort Settings Change	3-30
3.12	Reset Non-PnP ISA Device Setting.....	3-31
3.13	Leaving Setup.....	3-31

Appendices

Appendix A Model Definition

Appendix B Spare Parts List

Appendix C Schematics

Appendix D Silk Screens

Appendix E BIOS POST Check Points

List of Figures

1- 1	Front Panel.....	1-1
1- 2	Front Panel Features	1-2
1- 3	RDM LED	1-5
1- 4	Rear Panel.....	1-6
1- 5	Pentium Pro CPU Architecture.....	1-8
1- 6	System Architecture.....	1-8
1- 7	Memory Board Layout.....	1-13
1- 8	SCSI Disk Array Backplane Board	1-13
1- 9	RDM Module Layout	1-14
1- 10	System Board Jumper and Connector Locations.....	1-15
1- 11	System Block Diagram	1-27
1- 12	Memory Controller Block Diagram	1-28
1- 13	Memory Interleaving Block Diagram	1-29
1- 14	System Clock Diagram	1-30
1- 15	Interrupt Distribution Logic Diagram.....	1-31
1- 16	Dual-processor Operation Logic Diagram.....	1-32
1- 17	IDX-2 Housing	1-36
1- 18	Basic Model Configuration	1-37
1- 19	System Board Power Cable Connections.....	1-38
1- 20	System Boards and Power Subsystem Interconnections	1-39
1- 21	Door Switches Circuit.....	1-39
1- 22	Cable 1 Definition for Power Subsystem J11.....	1-40
1- 23	Cable 2 Definition for Power Subsystem J2	1-40
1- 24	Cable 3 Definition for Power Subsystem J3	1-41
1- 25	Cable 4 Definition for Power Subsystem J4	1-41
1- 26	Cable 5 Definition for Power Subsystem J5	1-42
1- 27	Cable 6 Definition for Power Subsystem J6	1-42
1- 28	Cable 7 Definition for Power Subsystem J7	1-43
1- 29	Cable 9 Definition for Power Subsystem J10.....	1-43
1- 30	Cable 10 Definition for Power Subsystem J14.....	1-44
1- 31	Cable 11 Definition for the Front Panel Board.....	1-44
1- 32	Cable 12 Definition for the Wide SCSI Connectors	1-45
1- 33	Cables 14 and 15 Definition for the SCSI Backplane Board	1-45
1- 34	Cables 16 and 17 Definition for Diskette and IDE Drives.....	1-46

1- 35	Cable 18 Definition for Power Subsystem J7.....	1-46
1- 36	Cable 19 Definition for the Narrow SCSI Connector	1-47
2- 1	P6 Processor Pin Diagram	2-4
2- 2	Pentium Pro CPU Identification Markings	2-5
2- 3	GTL+ Bus Topology	2-7
2- 4	S82451GX Pin Diagram.....	2-34
2- 5	S82452GX Pin Diagram.....	2-38
2- 6	S82453GX Pin Diagram.....	2-41
2- 7	S82454GX Block Diagram	2-46
2- 8	S82454GX Pin Diagram.....	2-47
2- 9	82379AB Block Diagram	2-53
2- 10	82379AB Pin Diagram	2-54
2- 11	ESC (82374SB) Block Diagram	2-66
2- 12	ESC (82374SB) Pin Diagram	2-67
2- 13	PCEB (82375SB) Block Diagram	2-94
2- 14	PCEB (82375SB) Pin Diagram.....	2-95
2- 15	AIC 7880 Block Diagram.....	2-114
2- 16	AIC 7880 Pin Diagram	2-115
2- 17	ATI 264VT Block Diagram	2-128
2- 18	ATI 264VT Pin Diagram	2-129
2- 19	37C935 Block Diagram	2-138
2- 20	37C935 Pin Diagram.....	2-139

List of Tables

1- 1	LED Indicator Description	1-3
1- 2	LCD Messages	1-4
1- 3	System Board Specifications	1-20
1- 4	Memory Configurations.....	1-21
1- 5	Video memory Specification	1-23
1- 6	Display Modes and Refresh Rates for EDO DRAM	1-23
1- 7	Parallel Port Operation Mode Settings	1-24
1- 8	Memory Address Map.....	1-24
1- 9	Interrupt Channels Map.....	1-25
1- 10	I/O Address Map.....	1-26
1- 11	400W SPS Output Rating	1-33
1- 12	IDX-2 Housing Specifications.....	1-35
2- 1	GTL+ Bus Termination Voltage Specifications.....	2-6
2- 2	P6 Processor Signal Descriptions	2-8
2- 3	S82451GX Signal Descriptions	2-35
2- 4	S82452GX Signal Descriptions	2-39
2- 5	S82453GX Signal Descriptions	2-42
2- 6	S82454GX Signal Descriptions	2-48
2- 7	82379AB Signal Descriptions.....	2-55
2- 8	ESC (82374SB) Signal Abbreviations	2-68
2- 9	ESC (82374SB) Signal Descriptions	2-69
2- 10	PCEB (82375SB) Signal Descriptions	2-96
2- 11	AIC 7880 I/O Type Descriptions.....	2-116
2- 12	AIC 7880 Signal Descriptions.....	2-116
2- 13	ATI 264VT Signal Descriptions	2-130
2- 14	Display Modes for DRAM (45ns) or EDO DRAM (60ns)	2-135
2- 15	Display Modes for Synchronous DRAM or EDO DRAM with Burst CAS	2-135
2- 16	37C935 Buffer Type Descriptions.....	2-140
2- 17	37C935 Signal Descriptions	2-140
3- 1	Parallel Port Operation Mode Settings	3-15
3- 2	Drive Control Settings.....	3-25

System Introduction

1.1 Configuration Overview

1.1.1 Front Panel

The system front panel is divided into two sections. The upper front panel consists of the diskette/CD-ROM/tape drive bays, keylock, power switch, LED indicators, LCD display screen, and an embedded reset switch.

The lower part contains the externally accessible hard disk drive bays with 14 drive trays for narrow or wide SCSI drives.

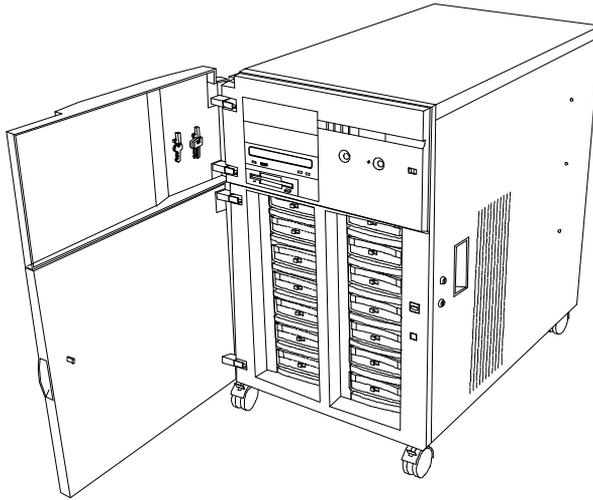


Figure 1- 1 Front Panel



One pair of system keys and one pair of power switch keylock are hung inside the upper front door. Additional duplicate keys can be found at the back of the system.

1.1.1.1 Front Panel Features

Figure 1-2 gives a closer look of the upper front panel features.

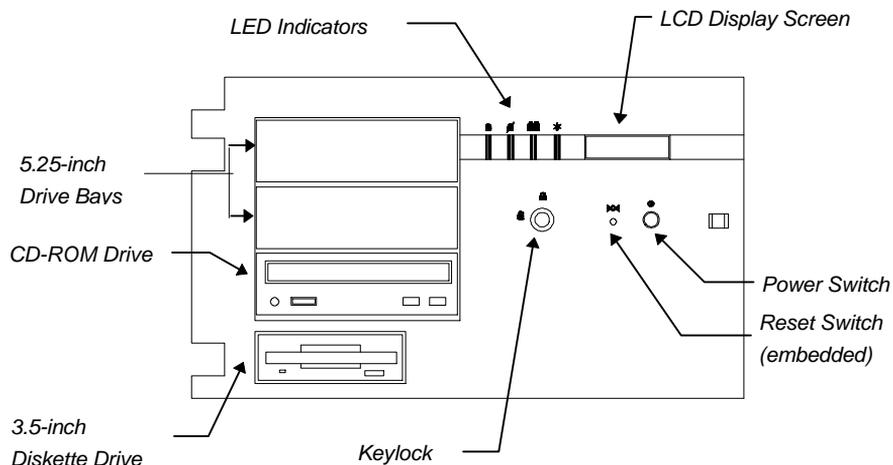


Figure 1-2 Front Panel Features

1.1.1.2 CD-ROM Drive

The basic system comes with a SCSI CD-ROM drive already installed.

1.1.1.3 3.5-inch Diskette Drive

A 3.5-inch diskette drive also comes with the basic system.

1.1.1.4 5.25-inch Drive Bays

Two empty 5.25-inch drive bays allow installation of additional devices.

1.1.1.5 Power Switch

The power switch allows you to turn the system power on or off.

1.1.1.6 Reset Switch

Pressing the reset switch generates a hardware reset pulse that restarts the system initializing all the registers, buffers, and memory subsystems.

1.1.1.7 Keylock

The keylock gives security to the system against unauthorized users. Turning the keylock to the unlocked position enables the power and reset switches. Turning the keylock to the locked position disables both switches whether the system is on or off. Supposing the system is on and you intend to reset or turn it off, make sure that the keylock is unlocked. Otherwise, the switches do not respond.

1.1.1.8 LED Indicators

Table 1- 1 LED Indicator Description

LED Icons	Description
Power Status 	Green Indicates that power is on. This color also denotes that the system is running on a good supply of AC power. Red Indicates that power is on. The AC power supply fails and the system is running on battery power.
Battery Status 	Green Indicates that a battery is present and in good condition. The battery LED shows this color during normal system operation, during which the battery automatically charges. When the power status LED is red, a green battery LED also indicates that the system is running on battery power. When this happens, shutdown the system immediately because the battery keeps a fully-configured system running only for about eight minutes. Red Normally, this color indicates that the battery is bad. However, there are times when the battery LED turns red for a few seconds due to other factors and NOT because the battery is bad. See below.
Hard Disk Busy 	Green Indicates that at least one of the hard disks is currently accessing.
Hard Disk Failure 	Green Indicates that all the hard disks installed on the backplane board are in good condition. Red Indicates that one of the hard disks installed on the backplane board is bad.

In these instances, the battery LED may turn red for a few seconds but DOES NOT necessarily indicate that the battery is bad.

- System Startup

At system power on, the battery LED shows red light when the system performs initialization and self-tests. The red light should remain for only a few seconds and eventually turn to green.

- Resumption of AC power supply while the system is running on battery power.

When AC power is cut-off, the battery automatically supplies the system power. The sudden return of AC power at this time when the system is running on battery may cause the battery LED to change to red. Simultaneously, the message "Battery Fails !" may appear on the LCD screen. When this happens, allow the battery to recover for a while. Wait for the battery LED to return to green and the LCD message to disappear.



If the battery LED remains red for several seconds and the message "Battery Fails !" still shows on the LCD screen, change the battery or call your dealer or a technician for assistance.

1.1.1.9 LCD Display Screen

The LCD display is a two-line by 16-character screen that indicates the boot status as well as any BIOS check point errors encountered upon system initialization. Normally, the system BIOS and the microcontroller firmware send the LCD display messages that appear on the screen. However, if you hooked up a special purpose driver to control the LCD module, this driver define the messages. See the driver manual for more information.

Table 1-2 lists the LCD messages from the system BIOS and the microcontroller at power on.

Table 1-2 LCD Messages

Message	Description
Hello! Welcome !	This is the first message that appears on the LCD screen. This message indicates that the microcontroller works fine.
POST Checkpoints	During the system power-on self-tests (POST), the LCD screen shows which POST check-point is currently being tested.
Power #1 Fails !	After POST, the microcontroller checks the power subsystem status. If it detects that power supply module 1 is bad, this message appears on the LCD screen.
Power #2 Fails !	If the microcontroller detects that power supply module 2 is bad, this message appears on the LCD screen.
Power #3 Fails !	If the microcontroller detects that power supply module 3 is bad, this message appears on the LCD screen.
Battery Fails !	Normally, this message indicates that the battery is bad and must be replaced with a new one. There are times when this message appears for a few seconds but do not necessarily mean that the battery is bad. Refer to the previous page for these instances.
Power Fan Fails !	This message indicates that one or more fans on the power subsystem failed.
AC Power Fails !	This message indicates that there is no power coming from the AC line and the system is currently running only on battery power.
The system is running well !	This message appears after POST and other tests. It shows that the system has passed all the tests and is running fine.

1.1.1.10 RDM LED

The RDM LED located on the lower right panel enables the remote diagnostic management feature. Refer to the RDM User's Guide for information on the RDM feature.

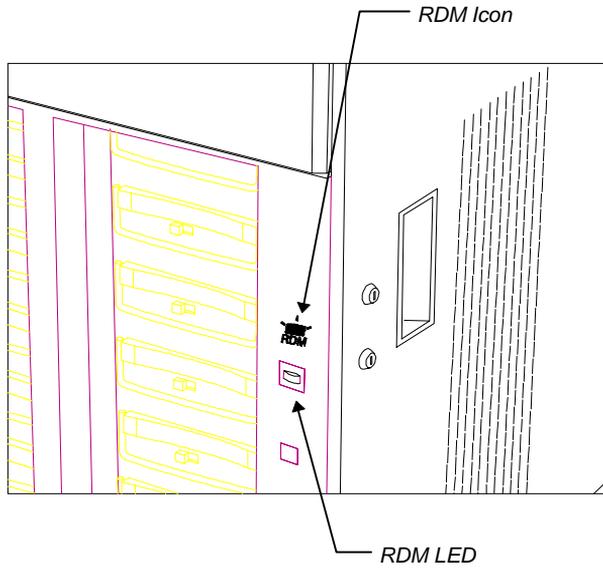


Figure 1-3 RDM LED

1.1.2 Rear Panel

The rear panel includes the connectors for the keyboard, mouse, VGA monitor, printer, and serial devices. Below the connectors are the slot openings for expansion boards. On the lower left is the socket for the system power cable. A standby current adapter socket is located on the lower right corner.

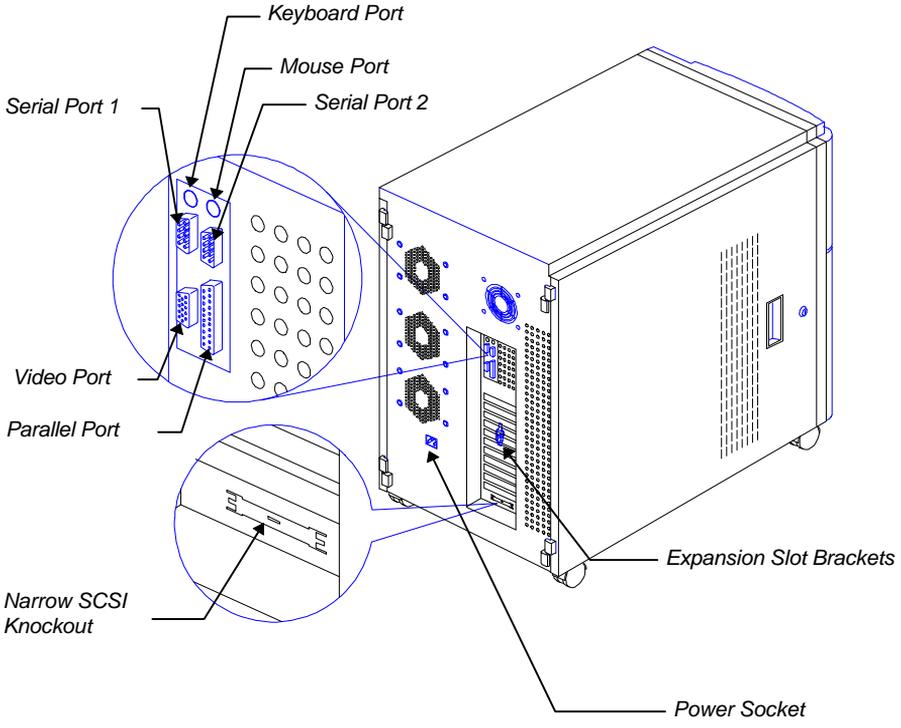


Figure 1-4 Rear Panel

1.2 Features

The AcerAltos 19000Pro4 is a powerful 64-bit quad-processor system loaded with a host of new and innovative features. The system offers a new standard for flexible productivity ideal for local area networks and multiuser server environments.

1.2.1 Intel Pentium Pro Microprocessor

The Intel Pentium Pro CPU is the heart of the AcerAltos 19000Pro4 system. Designed to work with the Orion chipset composed of a PCI bridge and memory controller, the Pentium Pro running at 200 MHz carries a new generation of power not present in its predecessors.

The system board has four CPU sockets to accommodate up to four Intel Pentium Pro CPUs for a multiprocessor configuration. This configuration doubles efficiency and reliability thereby upgrading overall system performance. The Pentium Pro supports a wide range of applications running under SMP network operating systems such as WindowsNT, UNIX, NetWare, etc.

The CPU also incorporates the first-level (L1) and second-level (L2) caches, the advanced peripheral interrupt controller (APIC), and the system bus controller. Figure 1-5 shows the CPU architecture.

1.2.1.1 First-level and Second-level Cache

The Pentium Pro has a 16-KB first-level and 256/512/1024-KB second-level cache. These caches produce a high hit rate that reduces the processor's external memory bandwidth requirements.

1.2.1.2 Advanced Peripheral Interrupt Controller (APIC)

The APIC unit inside the CPU along with the I/O APIC unit facilitate multiprocessor interrupt management. The APIC works with multiple I/O subsystems where each subsystem have its own interrupts that help minimize centralized system overhead.

1.2.1.3 Bus Controller

The bus controller integrated in the Pentium Pro CPU controls the system bus to make it perform its functions efficiently. It ensures that the bus serves as a reliable interconnection between one or two CPUs, I/O bridge, and memory controllers.

1.2.1.4 Pentium Pro CPU Architecture

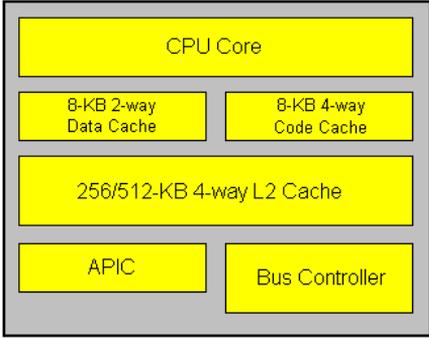


Figure 1-5 Pentium Pro CPU Architecture

1.2.2 System Architecture

The system bus, PCI buses, EISA bus, Orion PCI bridge (OPB), Orion memory controller (OMC), PCI/EISA Bridge (PCEB), and EISA system controller (ESC) comprise the basic system architecture.

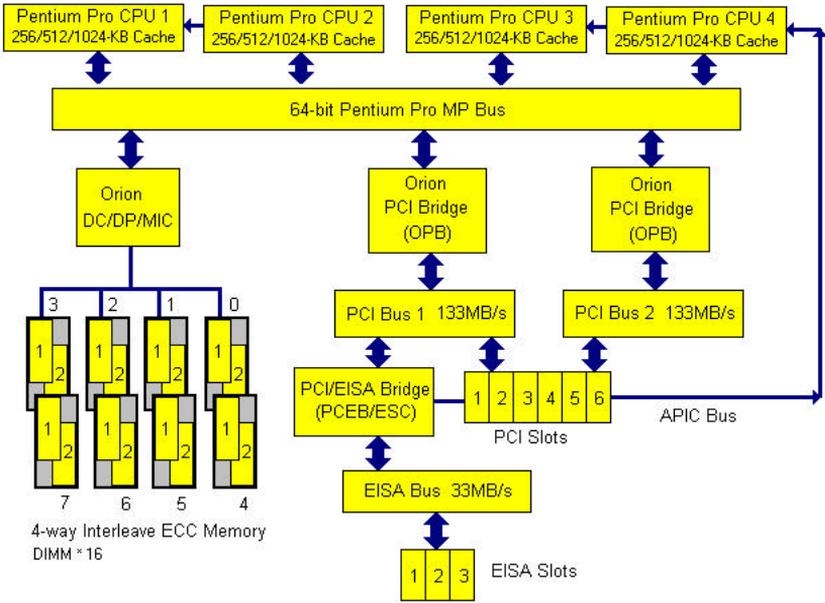


Figure 1-6 System Architecture

1.2.2.1 System Bus

The system bus is the CPU's major connection to all the system devices, primarily the PCI and EISA bridges, and the memory controllers. It can handle as many as eight outstanding transactions at a time through the transaction pipelining feature in which consecutive tasks from the CPU are queued in and transported to the designated devices on a first-in first-out basis. Pipelining allows for transaction overlapping in different phases as the CPU does not have to wait for each transaction to complete before it issues the next transaction. This produces significant improvement on overall system performance.

The bus architecture supports a number of features that ensure high reliability. It has an 8-bit error correction code (ECC) that protects the data lines and a 2-bit parity code that protects the address lines.

The bus uses the gunning transceiver logic (GTL+), a synchronous latched bus protocol that simplifies timing constraints. This protocol supports higher frequency system designs but requires a low voltage that reduces electromagnetic interference (EMI) resulting to a lower power consumption.

1.2.2.2 PCI and EISA Buses

The system supports two PCI buses created by the two PCI bridge chipsets (OPB). The PCI buses serve as the links between the PCI bridges and the PCI devices onboard. The presence of two buses instead of one reduces the I/O bottleneck and matches the higher bandwidth of the CPU for faster data transfers.

The EISA bus connects the EISA devices to the other system devices through the PCI/EISA bridge (PCEB) and the EISA system controller (ESC). The use of the PCEB and ESC maintains compatibility with the EISA environment.

1.2.2.3 Orion PCI Bridge

The Orion PCI bridge (OPB) is a low-cost I/O subsystem solution for high-performance systems. The OPB translates transactions between the system bus and the PCI buses using 32-byte buffers for inbound and outbound postings. The use of two OPBs in the system creates an architecture that allows faster data transfers.

1.2.2.4 Orion Memory Controller

The Orion memory controller (OMC) acts as an interface between the system bus and the system memory. It consists of the DRAM control (DC) chip and the data path (DP) chip. The OMC relates to the DRAM array through four memory interface controller (MIC) chips. The OMC supports 256-bit 4-way memory interleaving resulting to a more efficient memory traffic management.

1.2.3 SCSI Disk Array

The system supports an array of 14 hot-swappable disk drive trays through two 7-slot SCSI backplane boards (Acer BP-W7). The trays accommodate wide and narrow SCSI hard disks. With the AIC-7880 SCSI controller onboard, the transfer rate reaches up to 40 MB per second for ultra-wide SCSI.

1.2.4 Server Management

The system comes with the ASM Pro feature that allows voltage stability and CPU thermal monitoring, prevents data loss by prompt ECC memory error reporting, maximizes system resources by indicating the PCI bus utilization, and promotes efficiency by minimizing system downtime.

A related feature of ASM is the remote diagnostic management (RDM) that permits system diagnosis from a remote site through a modem. The RDM facilitate the fixing of detected problems, changing system configurations or rebooting in the event of system failure.

1.2.5 Redundant Power Supply Subsystem

The system comes with a power backplane that holds up to three 400-watt power supply modules. The power subsystem supports a redundant configuration such that even if one power supply fails, the remaining two continues to work together to supply the 800-watt requirement for a fully-configured system.

Two important segments of the power subsystem configuration are the charger board and battery box. Together, these two components function like an uninterruptible power supply (UPS). Providing an additional support to the three 400-watt power supply modules, the battery automatically charges whenever the system is on. The battery gives a fully-configured system the ability to run continuously through short interruptions in wall power or for a maximum of six minutes in the event of total AC power shutdown.

1.2.6 Security

The system housing comes with mechanical security locks on both the front panel and the side panel preventing unauthorized access to the internal components and system use.

The system BIOS secures the CMOS data and other system software with power-on password, keyboard password, setup control, disk drive control, and monitor control.

1.2.7 Memory Board

The memory board comes already installed with the basic system. A total of 16 168-pin DIMM sockets reside on the board. The sockets accept 32-MB, 64-MB, and 128-MB DIMMs for a maximum of 2 GB memory configuration.

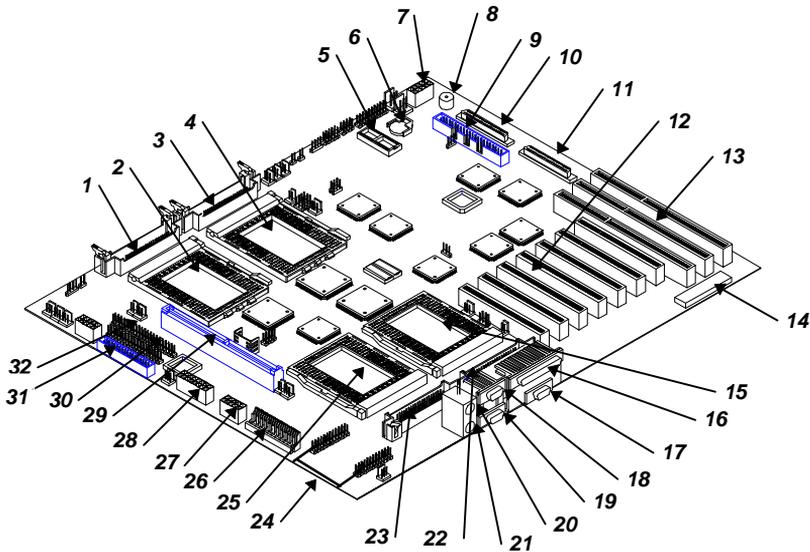
1.2.8 Major Components

The main board contains the following features:

- Four ZIF-type socket 8 for Intel Pentium Pro CPU
- Four VRM8 sockets for voltage regulator modules
- Seven PCI, three EISA expansion slots
- Intel Orion chip set and Intel EISA bridge
- Two Adaptec 7880 PCI fast/wide SCSI controller
- ATI 264VT/GT PCI VGA chip plus 1M/2M byte DRAM
- SMC FDC37C935 super IO chip
- Acer server management hardware module
- Remote diagnostic module
- 128-byte CMOS NVRAM as system clock/calendar storage plus 8K-byte extended NVRAM for EISA configuration storage
- 256K-byte Flash ROM containing system, onboard SCSI, and on-board VGA BIOS
- PS/2 keyboard and mouse interface
- Front panel interface including power and hard disk LEDs

1.3 Board Layouts

1.3.1 System Board



- | | |
|---------------------------------------|-------------------------------|
| 1. VRM connector 1 | 17. Video port |
| 2. Pentium Pro CPU socket 1 | 18. Serial port 1 |
| 3. VRM connector 3 | 19. Serial port 2 |
| 4. Pentium Pro CPU socket 3 | 20. Mouse port |
| 5. BIOS | 21. Keyboard port |
| 6. Battery | 22. VRM connector 4 |
| 7. +12V, +5V downside power connector | 23. VRM connector 2 |
| 8. Buzzer | 24. RDM connectors |
| 9. Narrow SCSI interface | 25. Pentium Pro CPU socket 2 |
| 10. Wide SCSI interface 1 | 26. ±12V, ±5V power connector |
| 11. Wide SCSI interface 2 | 27. +12V, +5V power connector |
| 12. PCI slots | 28. VCC3 power connector |
| 13. EISA slots | 29. Memory board slot |
| 14. Keyboard controller | 30. IDE connector |
| 15. Pentium Pro CPU socket 4 | 31. Front Panel Connector |
| 16. Parallel port | 32. Diskette drive connector |

1.3.2 Memory Board

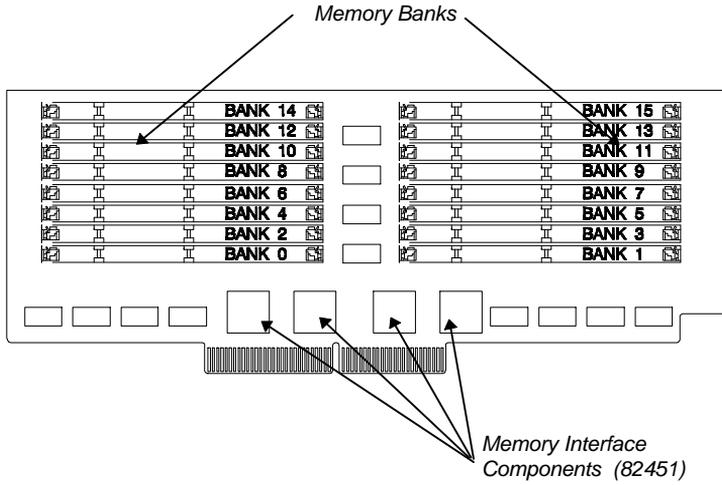


Figure 1-7 Memory Board Layout

1.3.3 SCSI Disk Array Backplane Board

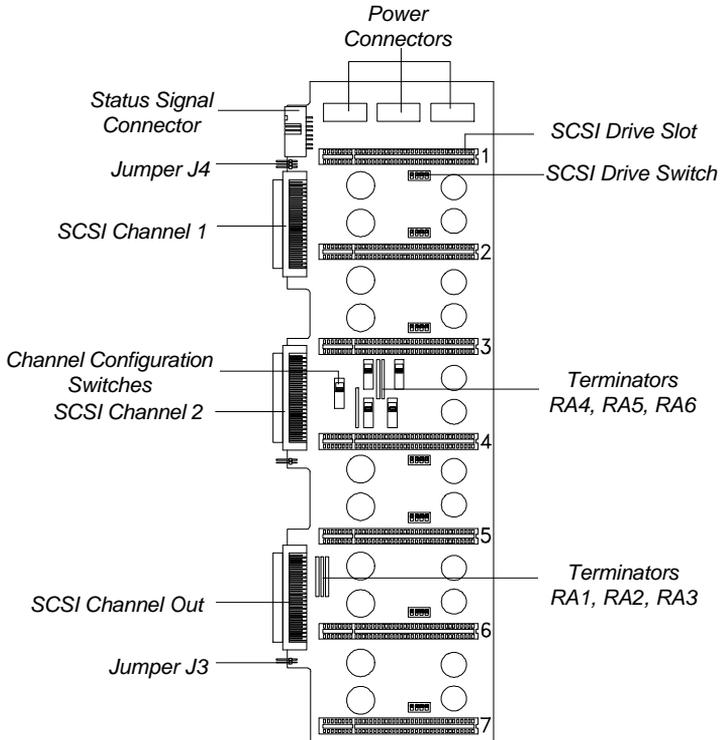
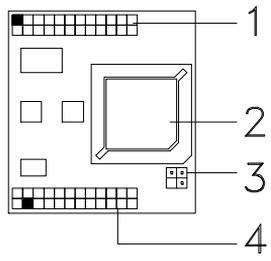


Figure 1-8 SCSI Disk Array Backplane Board

1.3.4 RDM Module



- 1 23-pin connector
- 2 RDM controller
- 3 RDM LED connector
- 4 23-pin connector

Figure 1- 9 RDM Module Layout

1.4 Jumpers and Connectors

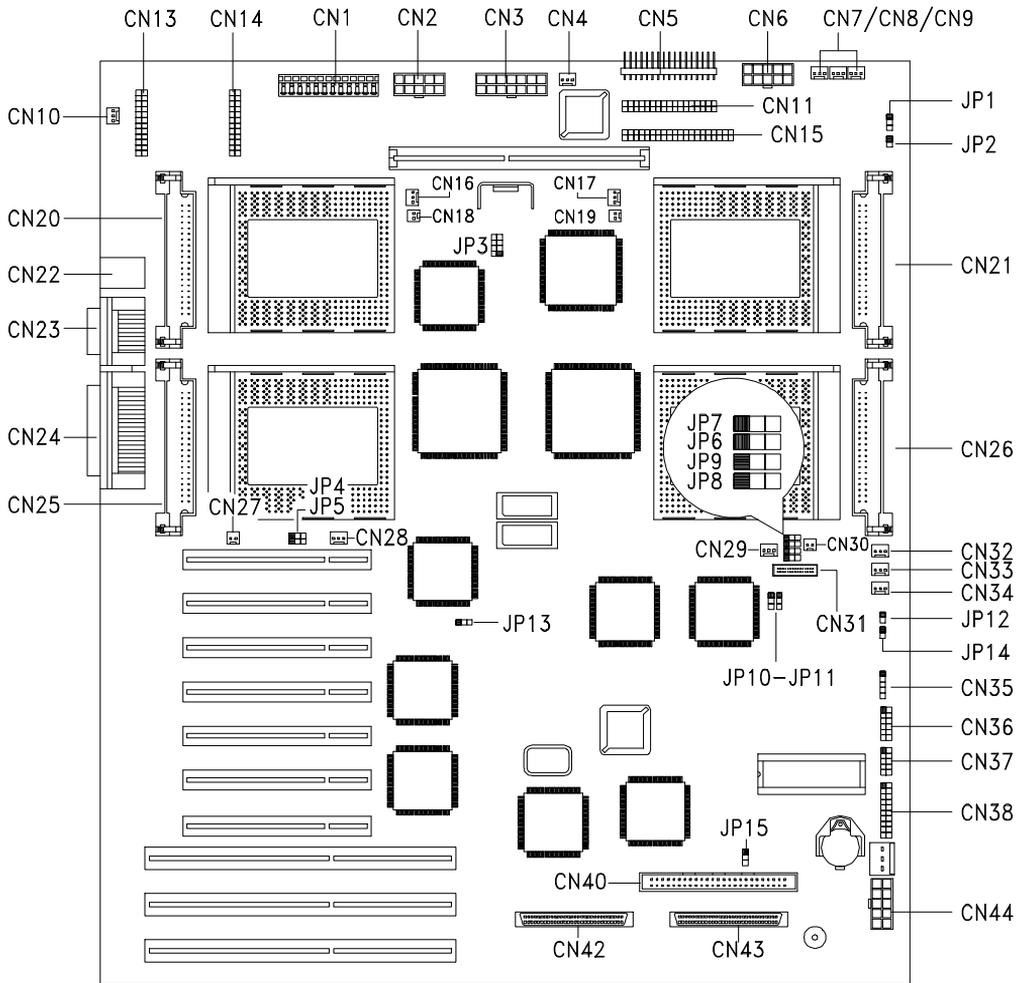


Figure 1- 10 System Board Jumper and Connector Locations



The blackened pin of a jumper or connector represents pin 1.

1.4.1 Jumper Settings

Table 3-2 Jumper Settings

Jumper	Setting	Function
JP1		Reserved
JP2		Reserved
JP10		Reserved
JP11	1-2 2-3*	Password Security Check password Bypass password
JP12		Reserved
JP13	1-2* 2-3	Onboard VGA Enabled Disabled
JP14		Reserved
JP15	1-2 2-3* Open	CPU Bus Frequency 60 MHz 66 MHz 50 MHz
JPX1		Reserved
JPX2		Reserved
JPX3		Reserved

The following sections describe and illustrate the jumpers that are not listed in the above table.

* Default setting

1.4.1.1 CPU Activation Jumpers

Jumpers JP4, JP5, JP6, JP7, JP8, and JP9 allow you to select the CPU to activate at a time. Table 3-3 lists the settings and the corresponding functions of these jumpers.

Table 3-3 CPU Activation Jumpers

Group 1 CPUs (CPU1 and CPU3)		
JP6	JP7	Function
2-3	Open	CPU1 only
1-2	1-2	CPU3 only
1-2	2-3	CPU1 and CPU3
Group 2 CPUs (CPU2 and CPU4)		
JP4	JP5	Function
2-3	Open	CPU2 only
1-2	1-2	CPU4 only
1-2	2-3	CPU2 and CPU4
Groups 1 and 2 CPUs		
JP8	JP9	Function
2-3	1-2	Group 1 only
1-2	2-3	Group 2 only
2-3	2-3	Group 1 and Group 2

1.4.1.2 CPU Frequency Jumper

Table 3-4 lists the CPU frequency ratios depending on JP3 settings.

Table 3-4 CPU Frequency Ratios (JP3)

JP3 Settings				Core/Bus
1-2	3-4	5-6	7-8	
C	C	C	C	2
C	C	O	C	3
C	C	C	O	4
C	C	O	O	5
O	C	C	C	2.5
O	C	O	C	3.5

C = Closed (Processor pin connected to Vss)

O = Open



DO NOT change jp3 settings unless you are qualified to do so. Ask a technician if you need help when configuring the jumper.

1.4.2 Connector List

Table 3-5 Connector Functions

Connector	Function
CN1	Power connector for $\pm 12V$, $\pm 5V$
CN2	Power connector for $\pm 12V$, $\pm 5V$
CN3	Power connector for VCC3
CN4	Power switch connector
CN5	Front panel connector
CN6	Power connector for $\pm 12V$, $\pm 5V$
CN7	System fan connector
CN8	System fan connector
CN9	System fan connector
CN10	System fan connector
CN11	Diskette drive connector
CN12	RDM LED connector
CN13	RDM connector (to FP11 on the front panel board)
CN14	RDM connector (to FP11 on the front panel board)
CN15	IDE connector
CN16	CPU2 fan connector
CN17	CPU1 fan connector
CN18	CPU2 temp. connector
CN19	CPU1 temp. connector
CN20	Voltage regulator module 2 (VRM2)
CN21	Voltage regulator module 1 (VRM1)
CN22	Keyboard/mouse connector
CN23	Serial ports 1 and 2
CN24	Video port/Parallel port
CN25	Voltage regulator module 4 (VRM4)
CN26	Voltage regulator module 3 (VRM3)
CN27	CPU4 temp. connector
CN28	CPU4 fan connector
CN29	CPU3 fan connector
CN30	CPU3 temp. connector
CN31	ITP connector
CN32	System fan connector
CN33	System fan connector
CN34	System fan connector

Table 3-5 Connector Functions (continued)

Connector	Function
CN35	HDD LED connector
CN36	Extended controller connector
CN37	Redundant power signal connector
CN38	Intel feature connector
CN40	Narrow SCSI connector
CN42	Wide SCSI connector 2
CN43	Wide SCSI connector 1
CN44	Down-side power connector for +12V, +5V

1.5 System Board Specifications

Table 1-3 System Board Specifications

Item	Description
PCB Size	410mm x 360mm
Processor I/O Integrated	Quad PPro CPUs & VRM on-board; (200MHz/512KB, 200MHz/1MB)
Memory	ECC Memory card- 16 DIMM slots, up to 2GB (4GB in the future) 1/2/4-way interleaving access
Slots	6 PCI, 2 EISA, plus one PCI/EISA shared slot
RDM Module	Remote Diagnostic Module H/W & F/W built in
Server Management	ASM Pro Server Management H/W & S/W included
VGA and DRAM	PCI VGA, 1MB DRAM on-board, expandable to 2MB
PCI-SCSI	Two Adaptec 7880 Ultra/Fast, Wide/Narrow SCSI on-board
I/O Integrated	Super I/O SMC935- FDC, AT-IDE, ECP/EPP, 16550 * 2

1.6 Hardware Configurations

1.6.1 Memory Configurations

The memory board comes already installed with the basic system. A total of 16 168-pin DIMM sockets reside on the board. The sockets accept 32-MB, 64-MB, and 128-MB DIMMs for a maximum of 2 GB memory configuration.

1.6.1.1 Important points to configure memory

- The above table must be followed when upgrading memory
- All DIMMs in each of slot0-3, 4-7, 8-11, 12-15 must be populated with identical ones
- Banks should be populated in the order from Bank 0 to Bank 15
- Install DIMMs in slot0-3, (and 4-7, and 8-11, and 12-15) makes 4-way interleaving

Table 1- 4 Memory Configurations

Bank 0	Bank 1	Bank 2-3	Bank 4-7	Bank 8-11	Bank 12-15	Total Memory
32MB * 1						32MB
32MB * 1	32MB * 1					64MB
32MB * 1	32MB * 1	32MB * 2				128MB
32MB * 1	32MB * 1	32MB * 2	32MB * 4			256MB
32MB * 1	32MB * 1	32MB * 2	32MB * 4	32MB * 4		384MB
32MB * 1	32MB * 1	32MB * 2	32MB * 4	32MB * 4	32MB * 4	512MB
32MB * 1	32MB * 1	32MB * 2	32MB * 4	64MB * 4		512MB
32MB * 1	32MB * 1	32MB * 2	32MB * 4	64MB * 4	64MB * 4	768MB
32MB * 1	32MB * 1	32MB * 2	32MB * 4	128MB * 4		768MB
32MB * 1	32MB * 1	32MB * 2	32MB * 4	128MB * 4	128MB * 4	1280MB
32MB * 1	32MB * 1	32MB * 2	32MB * 4	256MB * 4		1280MB
32MB * 1	32MB * 1	32MB * 2	32MB * 4	256MB * 4	256MB * 4	2304MB
64MB * 1						64MB
64MB * 1	64MB * 1					128MB
64MB * 1	64MB * 1	64MB * 2				256MB
64MB * 1	64MB * 1	64MB * 2	64MB * 4			512MB
64MB * 1	64MB * 1	64MB * 2	64MB * 4	32MB * 4		640MB
64MB * 1	64MB * 1	64MB * 2	64MB * 4	32MB * 4	32MB * 4	768MB
64MB * 1	64MB * 1	64MB * 2	64MB * 4	64MB * 4		768MB

Table 3-6 Memory Configurations (continued)

Bank 0	Bank 1	Bank 2-3	Bank 4-7	Bank 8-11	Bank 12-15	Total Memory
64MB * 1	64MB * 1	64MB * 2	64MB * 4	64MB * 4	64MB * 4	1024MB
64MB * 1	64MB * 1	64MB * 2	64MB * 4	128MB * 4		1024MB
64MB * 1	64MB * 1	64MB * 2	64MB * 4	128MB * 4	128MB * 4	1536MB
64MB * 1	64MB * 1	64MB * 2	64MB * 4	256MB * 4		1536MB
64MB * 1	64MB * 1	64MB * 2	64MB * 4	256MB * 4	256MB * 4	2560MB
128MB * 1						128MB
128MB * 1	128MB * 1					256MB
128MB * 1	128MB * 1	128MB * 2				512MB
128MB * 1	128MB * 1	128MB * 2	128MB * 4			1024MB
128MB * 1	128MB * 1	128MB * 2	128MB * 4	32MB * 4		1152MB
128MB * 1	128MB * 1	128MB * 2	128MB * 4	32MB * 4	32MB * 4	1280MB
128MB * 1	128MB * 1	128MB * 2	128MB * 4	64MB * 4		1280MB
128MB * 1	128MB * 1	128MB * 2	128MB * 4	64MB * 4	64MB * 4	1536MB
128MB * 1	128MB * 1	128MB * 2	128MB * 4	128MB * 4		1536MB
128MB * 1	128MB * 1	128MB * 2	128MB * 4	128MB * 4	128MB * 4	2048MB
128MB * 1	128MB * 1	128MB * 2	128MB * 4	256MB * 4		2048MB
128MB * 1	128MB * 1	128MB * 2	128MB * 4	256MB * 4	256MB * 4	3072MB
256MB * 1						256MB
256MB * 1	256MB * 1					512MB
256MB * 1	256MB * 1	256MB * 2				1024MB
256MB * 1	256MB * 1	256MB * 2	256MB * 4			2048MB
256MB * 1	256MB * 1	256MB * 2	256MB * 4	32MB * 4		2176MB
256MB * 1	256MB * 1	256MB * 2	256MB * 4	32MB * 4	32MB * 4	2304MB
256MB * 1	256MB * 1	256MB * 2	256MB * 4	64MB * 4		2304MB
256MB * 1	256MB * 1	256MB * 2	256MB * 4	64MB * 4	64MB * 4	2560MB
256MB * 1	256MB * 1	256MB * 2	256MB * 4	128MB * 4		2560MB
256MB * 1	256MB * 1	256MB * 2	256MB * 4	128MB * 4	128MB * 4	3072MB
256MB * 1	256MB * 1	256MB * 2	256MB * 4	256MB * 4		3072MB
256MB * 1	256MB * 1	256MB * 2	256MB * 4	256MB * 4	256MB * 4	4096MB

1.6.2 Video Memory Specification

Table 1- 5 Video memory Specification

Item	Specification	
Memory size	1MB	2MB
Memory type	EDO RAM	
Memory configuration	256K*16 x 2	256K*16 x 4
Fixed or upgradeable	1 st MB is fixed onboard, 2 nd MB is upgradeable	
Memory speed	60ns	
Memory voltage	5V	
Memory package	SOJ 40-pin	

1.6.3 Video Display Modes and Refresh Rates

Table 1- 6 Display Modes and Refresh Rates for EDO DRAM

Resolution	256 colors		64K colors		16.7M colors	
	1 MB	2 MB	1 MB	2 MB	1 MB	2 MB
640 x 480	100	100	100	100	90	100
800 x 600	100	100	90	100	—	100
1024 x 768	100	100	—	100	—	—
1152 x 864	80	80	—	80	—	—
1280 x 1024	*	75	—	—	—	—

* - 1280 x 1024 @ 16 colors is available at 75 Hz.

1.6.4 Parallel Port Configurations

The onboard parallel port interface supports a 25-pin D-type connector. The port functions in different operation modes and is adjustable to select LPT1, LPT2, and LPT3 by changing the CMOS settings in the BIOS Utility.

Table 1-7 lists the operation mode settings and their corresponding functions.

Table 1-7 Parallel Port Operation Mode Settings

Setting	Function
Standard Parallel Port (SPP)	Allows normal speed operation but in one direction only
Enhanced Parallel Port (EPP 1.7/1.9)	Allows bidirectional parallel port operation at maximum speed
Extended Capabilities Port (ECP)	Allows parallel port to operate in bidirectional mode and at a speed higher than the maximum data transfer rate
Standard and Bidirectional	Allows normal speed operation in a two-way mode

1.6.5 Serial Port Configurations

The system board has two high-speed 9-pin D-type serial ports. These ports are NS16C550-compatible UARTs with 16-byte FIFO send/receive capability. The port functions are software adjustable to select COM1, COM2, COM3, and COM4.

1.6.6 Memory Address Map

Table 1-8 Memory Address Map

Address	Name	Function
00000000 ~ 0009FFFF	640 KB system memory	Main Memory
000A0000 ~ 000BFFFF	128 KB video RAM	Graphics display buffer
000C0000 ~ 000C7FFF	32 KB I/O expansion ROM	Video BIOS
000C8000 ~ 000CFFFF	32 KB I/O expansion ROM	Reserved for ROM on I/O adapters
000D0000 ~ 000DFFFF	64 KB I/O expansion ROM	Reserved for ROM on I/O adapters
000E0000 ~ 000E7FFF	32 KB	System extended BIOS (SCSI BIOS)
000E8000 ~ 000EFFFF	32 KB	Reserved for system extended BIOS
000F0000 ~ 000FFFFFFF	64 KB	System BIOS
00100000 ~ FFFFFFFF	System memory	System Memory

1.6.7 Interrupt Channels Map

Table 1-9 *Interrupt Channels Map*

IRQ	System Device
IRQ0	Timer output 0
IRQ1	Keyboard
IRQ2	Reserved
IRQ3	Serial port 2
IRQ4	Serial port 1
IRQ5	Reserved
IRQ6	Diskette drive
IRQ7	Parallel port
IRQ8	Real-time clock
IRQ9	Reserved
IRQ10	Reserved
IRQ11	Reserved
IRQ12	PS/2 mouse
IRQ13	Numeric processor
IRQ14	IDE primary channel
IRQ15	IDE secondary channel

1.6.8 I/O Address Map

Table 1- 10 I/O Address Map

Hex Range	Device
000 ~ 00F	DMA controller-1
020 ~ 021	Interrupt controller-1
022 ~ 023	ESC (82374) configuration
040 ~ 043	System timer-1
048 ~ 04B	System timer-2
061	NMI status and control
070	NMI mask
080 ~ 08F	DMA page register
092	System control port
0A0 ~ 0A1	Interrupt controller-2
0B2 ~ 0B3	Advanced power management
0C0 ~ 0DE	DMA controller-2
0F0	Reset IRQ 13
1F0 ~ 1F7	Hard disk
278 ~ 27F	Parallel port 2
2F8 ~ 2FF	Serial port 2
378 ~ 37F	Parallel port 1
3B0 ~ 3BF	Monochrome display
3C0 ~ 3CF	EGA, VGA, SVGA
3D0 ~ 3DF	CGA, VGA, SVGA
3F0 ~ 3F7	Diskette drive controller
3F8 ~ 3FF	Serial port 1
*4A0	On board peripherals control
*4A1-4A3	ASM control and status(1)
*4A4	Redundant power supply status
*4A5	ASM control and status(2)
*4A6	RDM control and status
*4A7	Backplane board status
*4A8-4AF	ASM control and status(3)
CF8	PCI configuration address regulation
CFC	PCI configuration data regulation

1.7 Block Diagrams

1.7.1 System Block Diagram

X3 Block Diagram

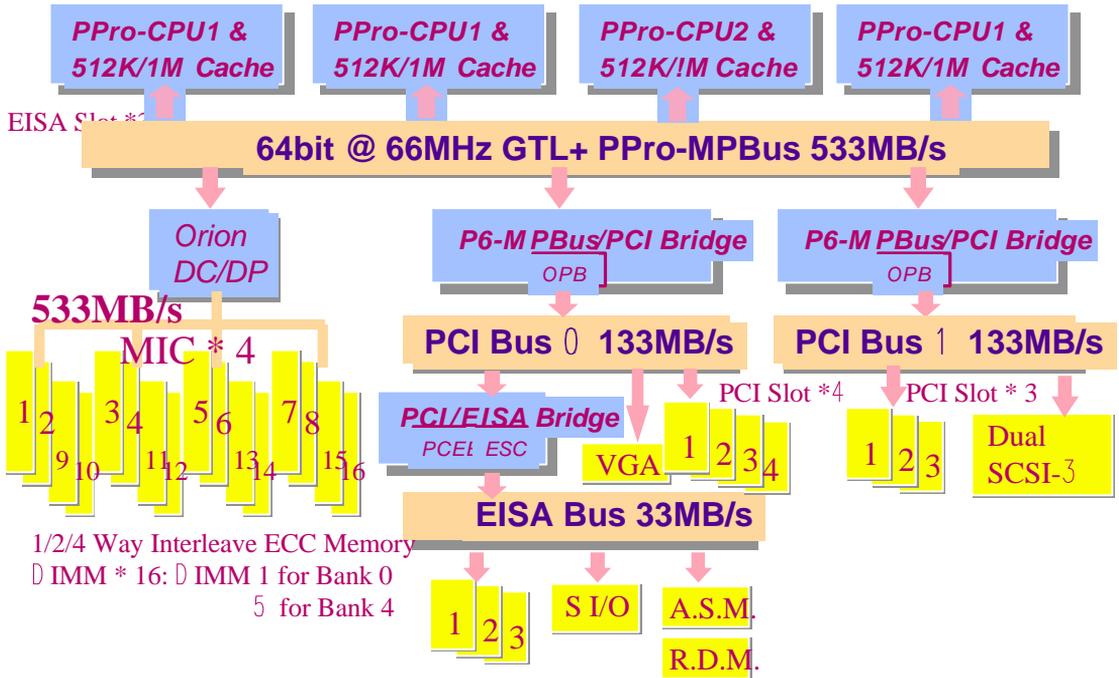


Figure 1- 11 System Block Diagram

1.7.2 Memory Controller Block Diagram

Two-bank, N : 1 - way Interleaved Memory Data Connections

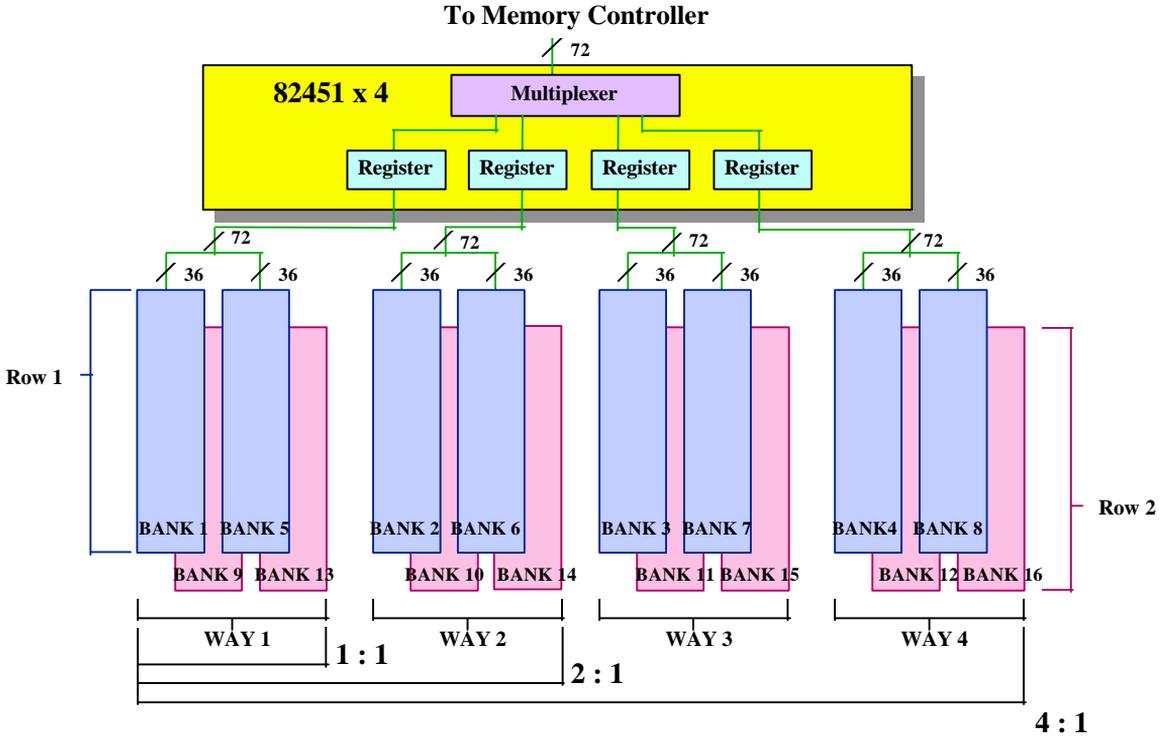
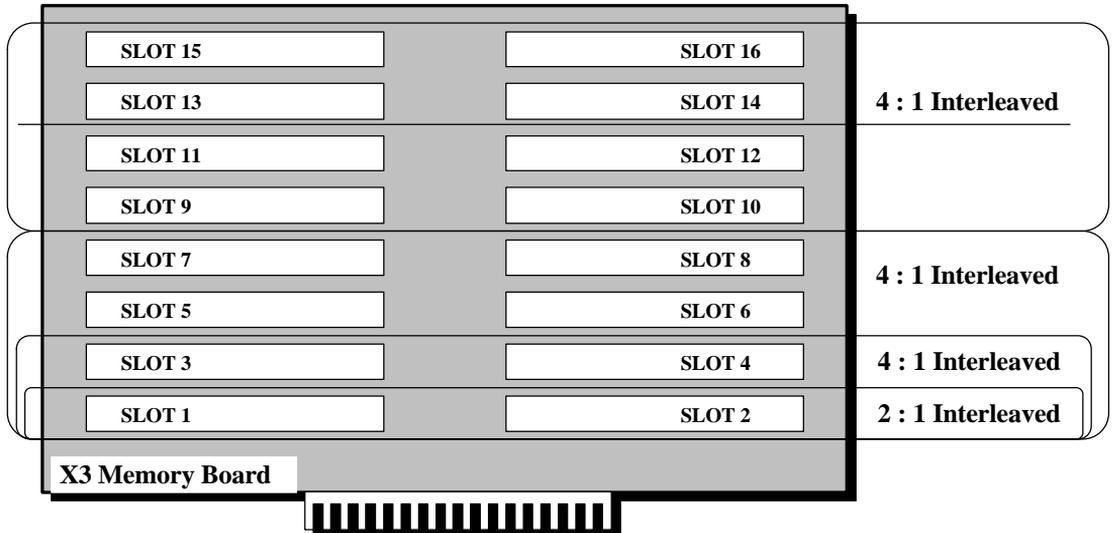


Figure 1- 12 Memory Controller Block Diagram

1.7.3 Memory Interleaving Block Diagram



DIMMs Population Rules of X3 Memory Board

Figure 1- 13 Memory Interleaving Block Diagram

Remark

1. Please follow Table 1-4(page 1-21 and 1-22) for the memory configurations.
2. Every 4 consecutive DIMMs are set as a group.(e.g. Group 1 means slot 1~4, Group 2 means slot 5~8, Group 3 means slot 9~12, Group 4 means slot 13~16)
3. Except for group 1, memory upgrade should be performed at least one group(4 DIMMs) at a time.
4. All DIMMs in a group should be of the same DIMM size.
5. Adding 1 DIMM, 2 DIMMs or 4 DIMMs is allowed in group 1, but not in group 2, 3 and 4.
6. Please follow the DIMM QVL of this product when you select DIMM for upgrade. Using DIMM out of the QVL is not quality assured.

1.7.4 System Clock Diagram

System Clock Diagram

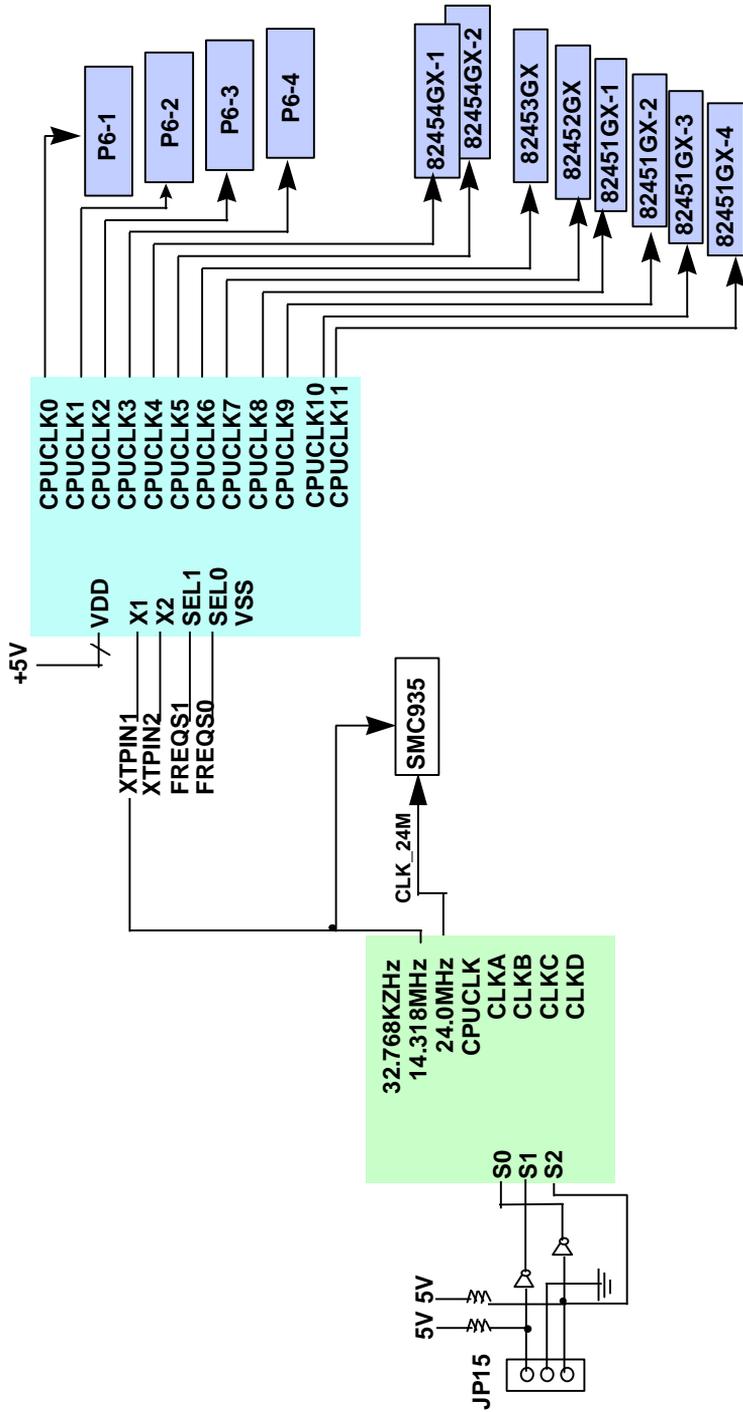


Figure 1- 14 System Clock Diagram

1.7.5 Interrupt Distribution Logic Diagram

Interrupt Distribution Logic

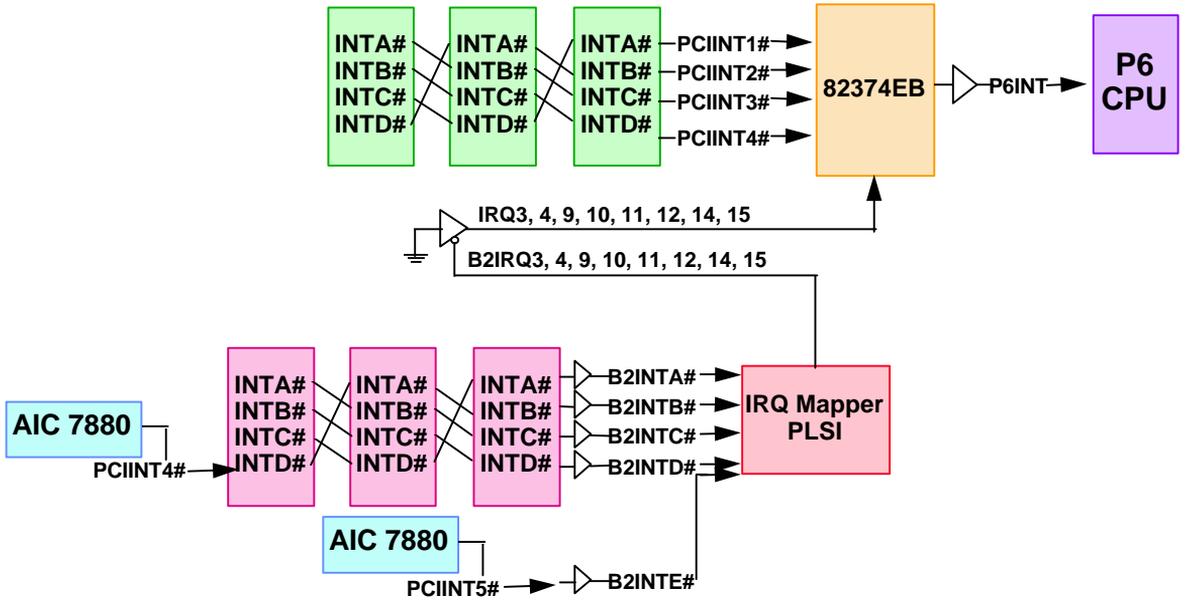


Figure 1- 15 Interrupt Distribution Logic Diagram

1.7.6 Quad-processor Operation Diagram

Quad-processor Operation Logic

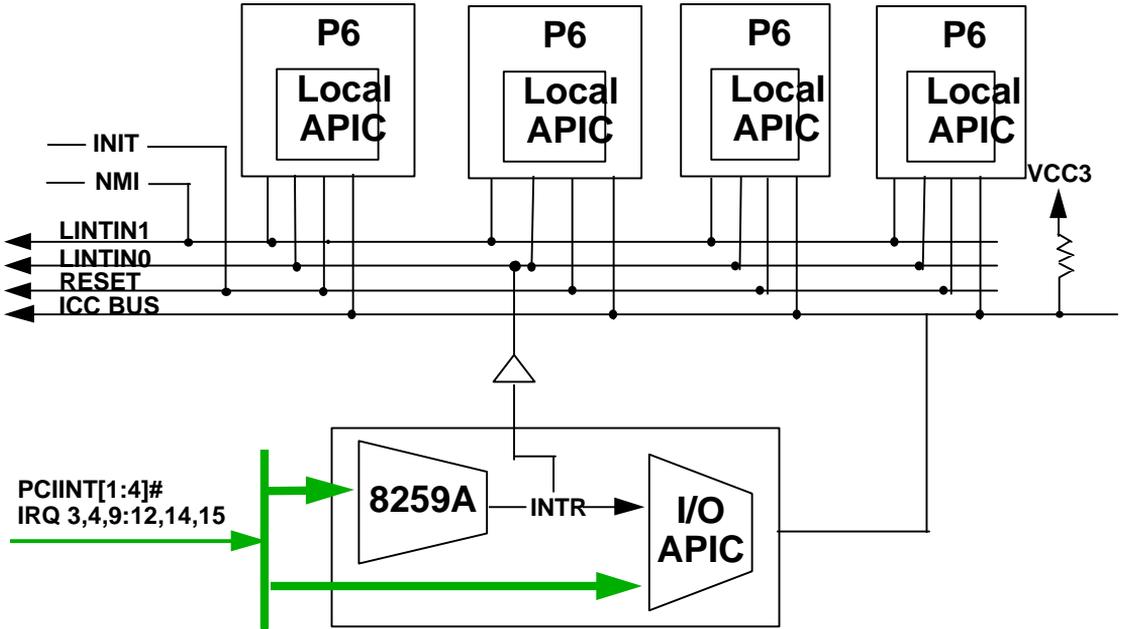


Figure 1- 16 Dual-processor Operation Logic Diagram

1.8 Power Requirements

The specific housing configuration of the X3 system determines the total power consumption required by the system.

1.8.1 400W Power Supply for IDX-2

X3 systems with IDX-2 housing require two to three units of 400-watt power supply modules. The following specifications are for a single 400-watt module.

1.8.1.1 Output Requirements

Table 1- 11 400W SPS Output Rating

Output	Nominal	Output Power	Ripple and Noise	Minimum	Maximum
1	+5.1V	204 W	50 mV	5A	40A
2	5V	5 W	50 mV	0	1A
3	3.3V	89 W	33 mV	0	27A
4	+12V	168 W	120 mV	1A	14A
5	-12V	36 W	120 mV	0	3A
6	5V	0.5 W	50 mV	0	0.1A
7	56.5V	56.5 W	800 mV	0	1A



Ripple and noise bandwidth from 10 Hz to 20 MHz.

*When AC power is on, +12V should provide 10A surge current.
This regulation should be within -6% and +7%.*

Regulation: The total voltage regulation for each level is calculated in terms of the band of voltage defined by the maximum positive and negative excursions (from nominal) that occur.

1.8.1.2 Installation Requirements

Installing or removing power supply modules, battery, or charger while the AC power cord is plugged-in may damage the whole power subsystem. Adhere to the standard procedure when installing or removing power supply modules, battery, or charger.



Failure to follow the standard safety procedure when installing or removing power modules may result to a fatal system damage.

Follow these steps to install or remove power supply modules, battery, or charger:

1. If the system is on, press the power switch to turn off the power.
2. Unplug the AC power cord from the power outlet.
3. Open the right panel of the system housing.
4. Remove or install power modules.
5. Close the housing then apply AC power.

1.9 Mechanical Specifications

1.9.1 IDX-2 Housing

Table 1- 12 *IDX-2 Housing Specifications*

Item	Description
Dimensions	740 mm (d) x 435 mm (w) x 700 mm (h)
Spacing between adapter cards	0.8 inch
Weight Basic Model Full-load	58 kg 82 kg (maximum)
Opening for expansion slots	12
Drive Bays	One 3.5-inch external bays Three 5.25-inch external bays 14 SCSI disk array drive bays
Major subassembly support	Major subassemblies are rigidly held in place by frame components. Adequate clearances are provided so that cards can be installed and removed without bending or forcing. All other components such as SPS and FDD can be assembled easily.
Circuit card support	Circuit cards plugged into the system board are supported by a card edge connector, the card end bracket, and by a card edge guide supporting the card edge from the farthest end bracket (if the card conforms to the full length).
Metal finish	All metal surfaces are plated or equivalent treatment Lower case: metal Left cover: metal Frame: metal Right cover: metal
Color/Paint	Units delivered in specified MCS colors. Paint samples supplied to the vendor as required.
Case finish	All surfaces are textured or equivalent treatment

Figure 1-17 shows the IDX-2 housing.

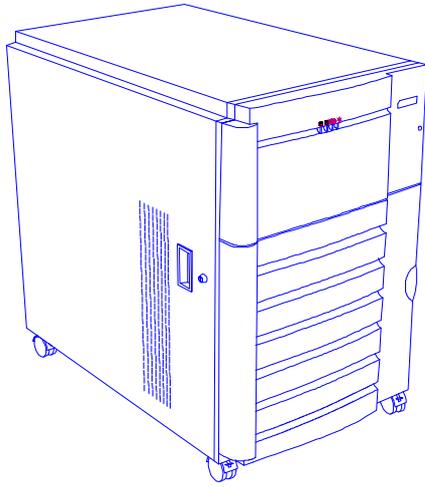


Figure 1- 17 *IDX-2 Housing*

1.10 Shipping Configuration

Figure 1-18 shows the basic model configuration for an X3 system with IDX-2 housing (AcerAltos 19000Pro4).

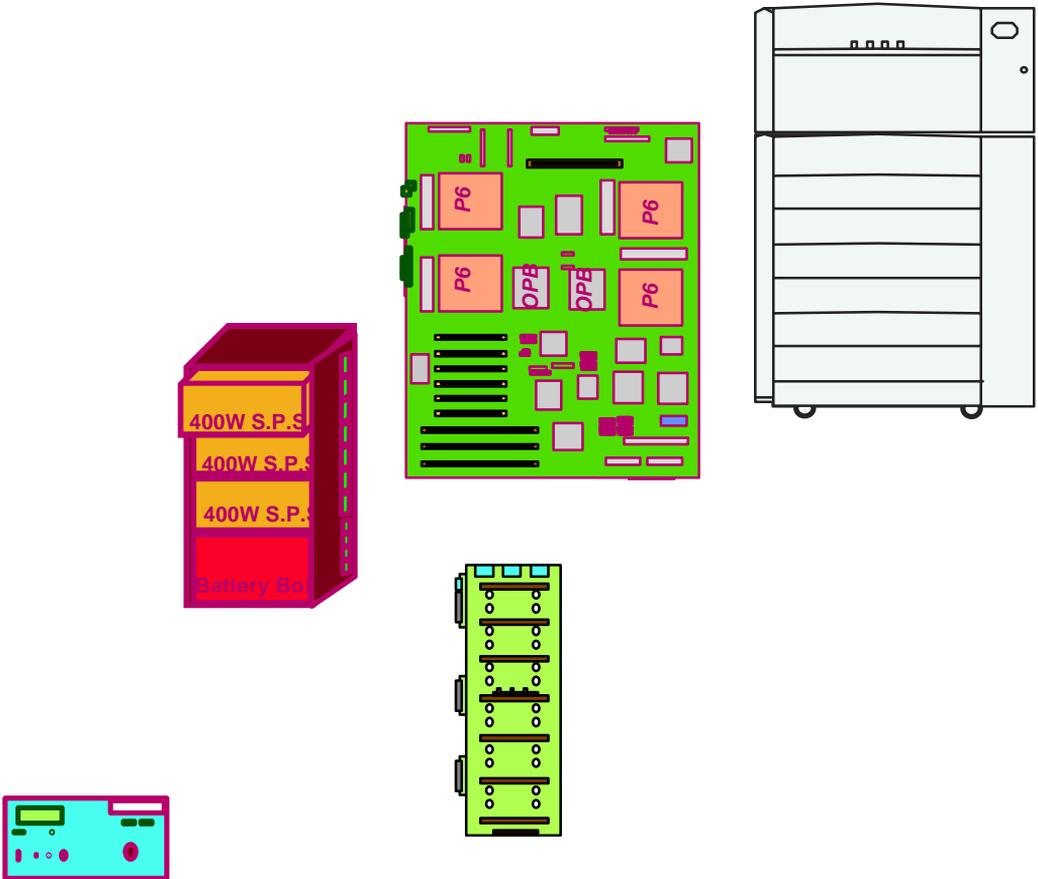


Figure 1- 18 Basic Model Configuration

1.11 Cable Connections

The following figures illustrate the cable connections for the different system components.

System Board Power Connections

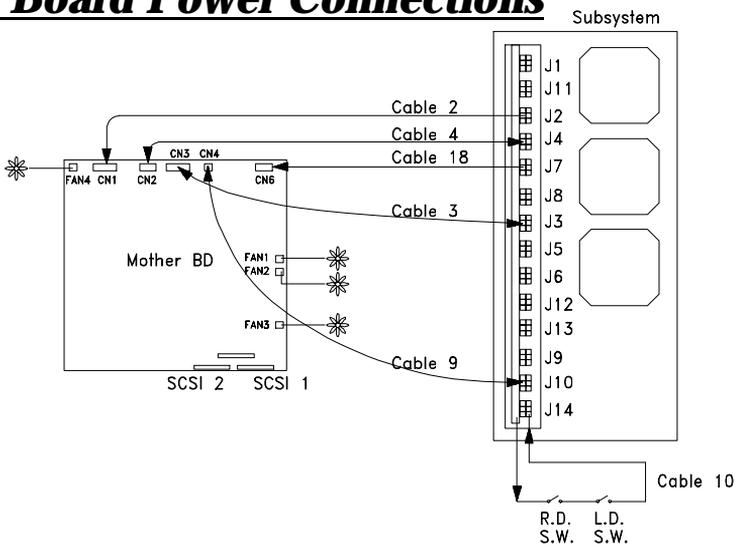


Figure 1- 19 System Board Power Cable Connections

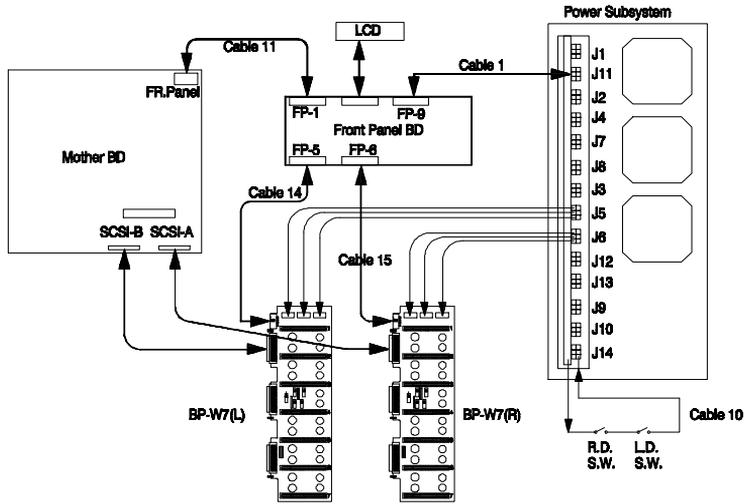


Figure 1-20 System Boards and Power Subsystem Interconnections

Door Switches Circuit

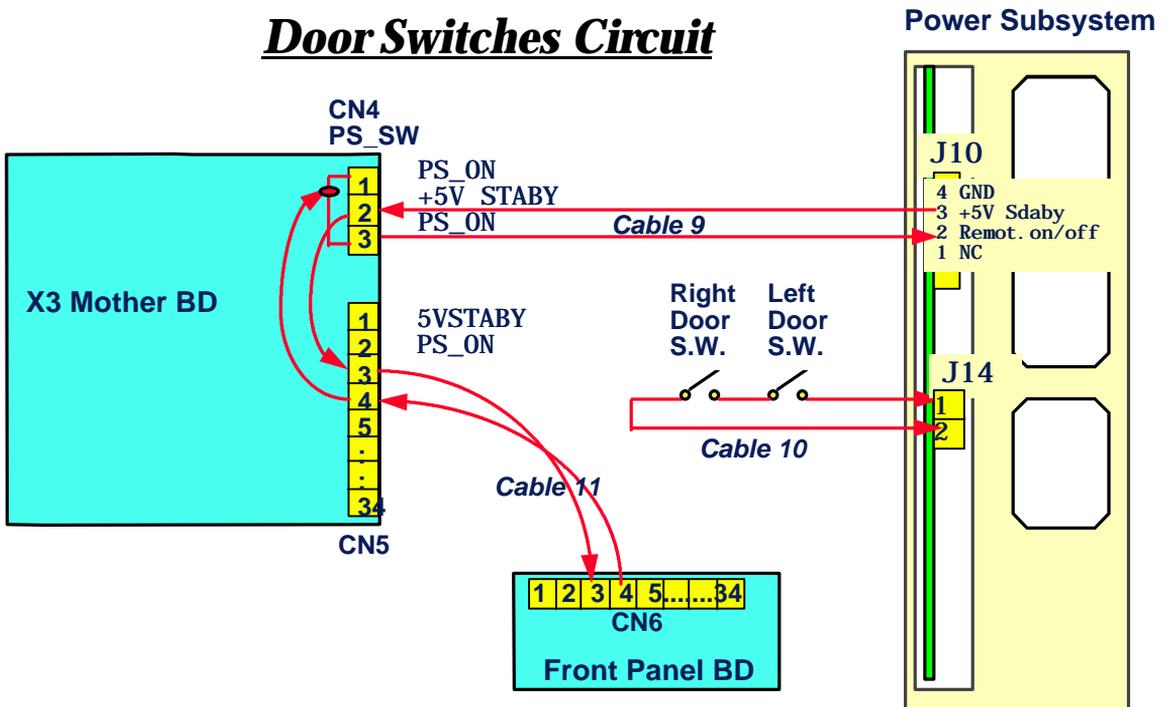


Figure 1-21 Door Switches Circuit

Cable 1 - Power Subsystem J11

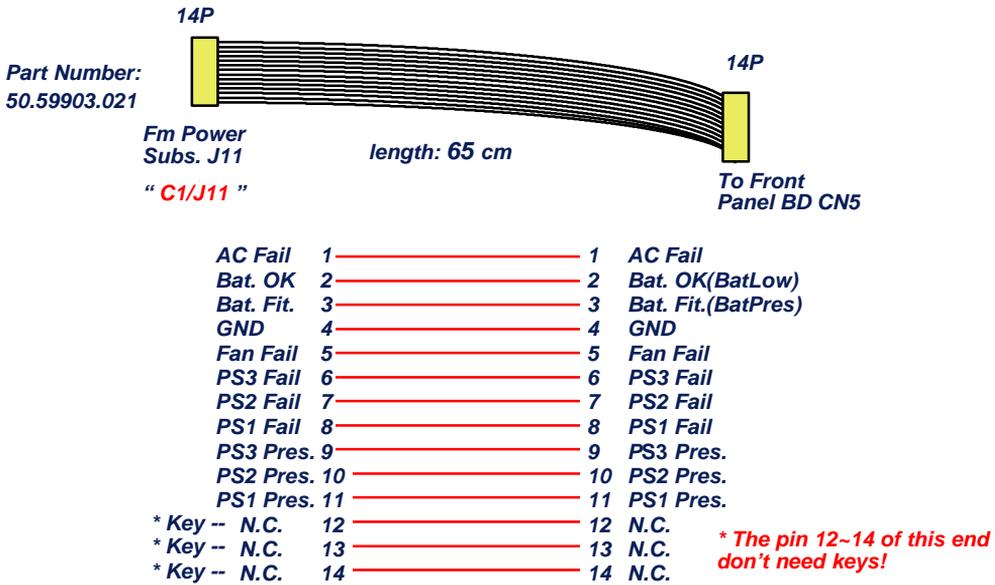


Figure 1- 22 Cable 1 Definition for Power Subsystem J11

Cable 2 - Power Subsystem J2

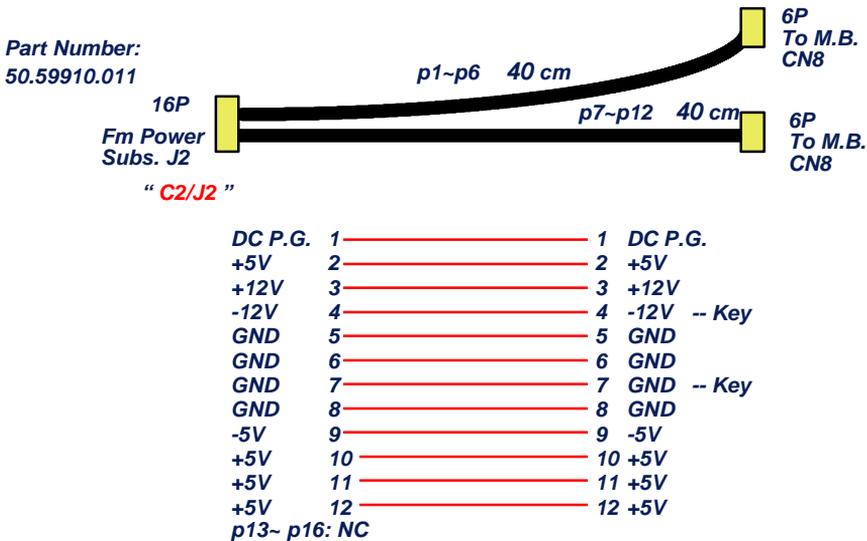


Figure 1- 23 Cable 2 Definition for Power Subsystem J2

Cable 3 - Power Subsystem J3

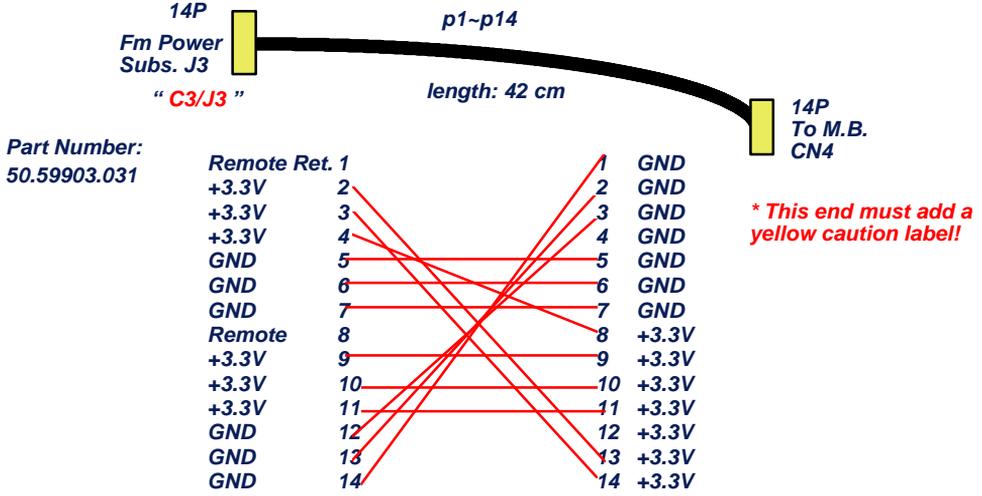


Figure 1-24 Cable 3 Definition for Power Subsystem J3

Cable 4 - Power Subsystem J4

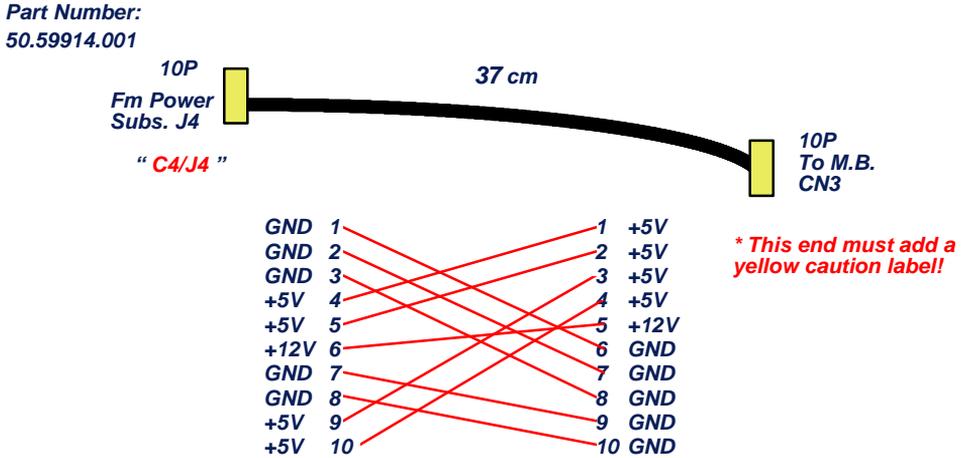


Figure 1-25 Cable 4 Definition for Power Subsystem J4

Cable 5 - Power Subsystem J5

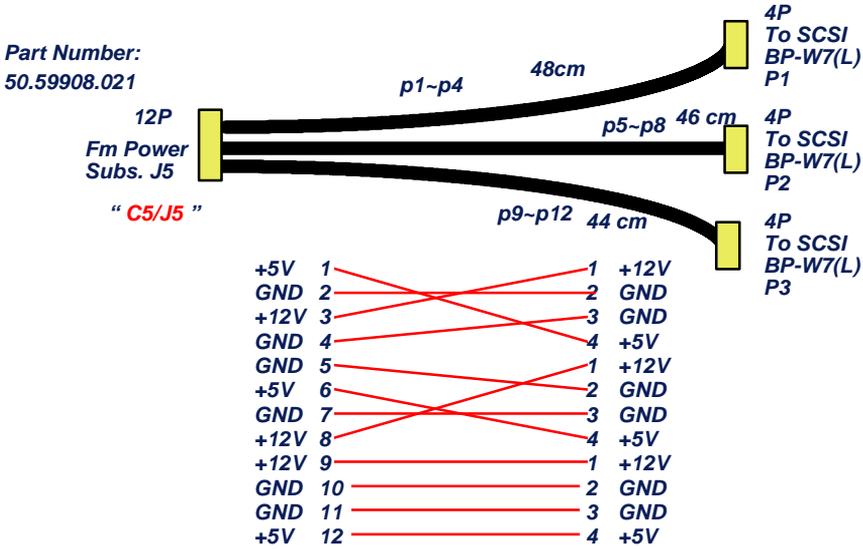


Figure 1- 26 Cable 5 Definition for Power Subsystem J5

Cable 6 - Power Subsystem J6

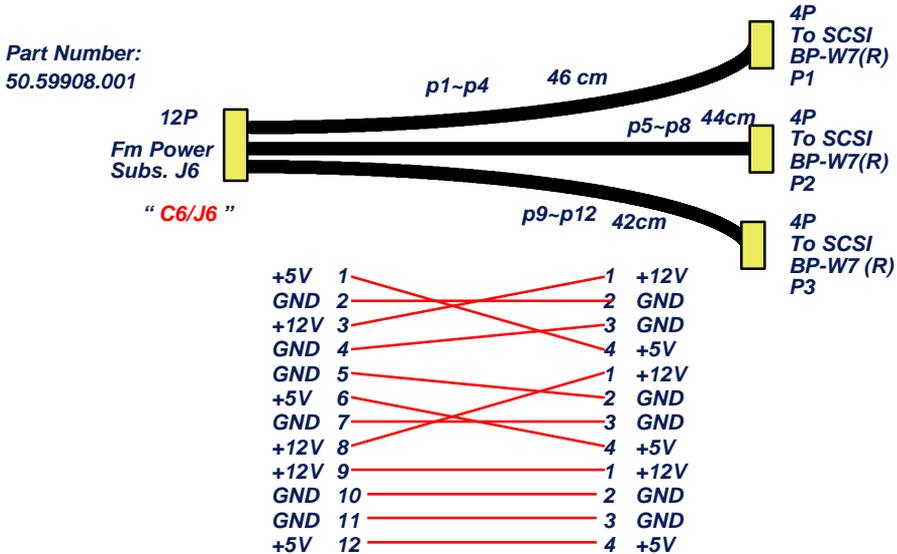


Figure 1- 27 Cable 6 Definition for Power Subsystem J6

Cable 7 - J12 for FDD/HDD/...

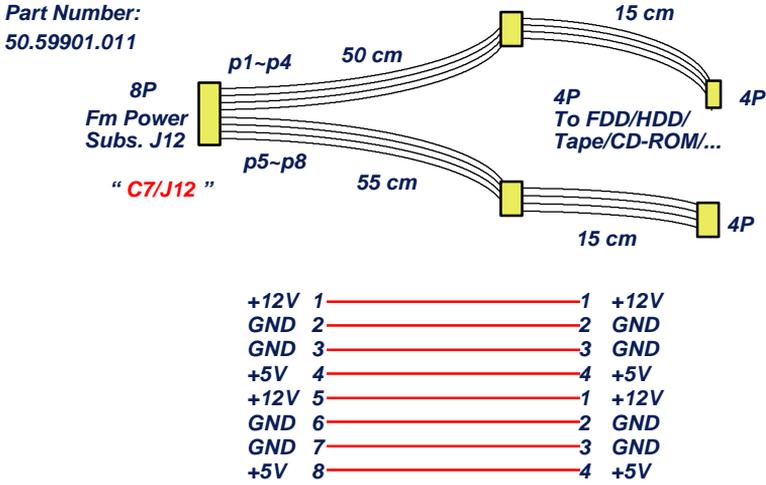


Figure 1- 28 Cable 7 Definition for Power Subsystem J7

Cable 9 - Power Subsystem J10

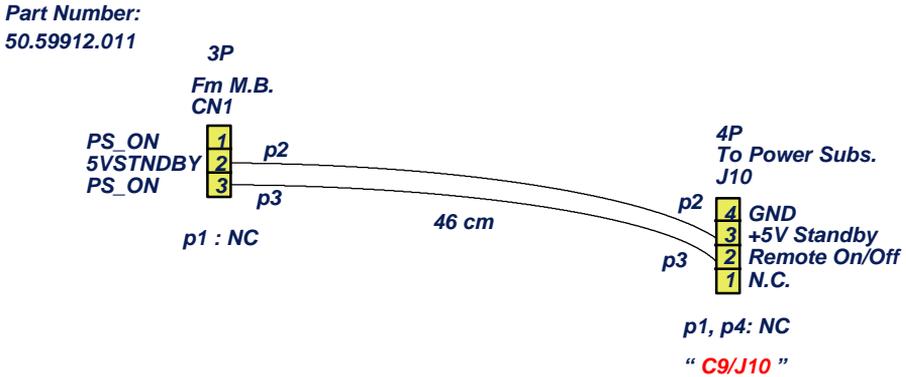
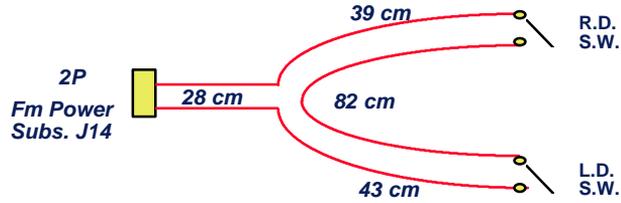


Figure 1- 29 Cable 9 Definition for Power Subsystem J10

Cable 10 - Power Subsystem J14

Part Number:
50.59911.021



* Cable: 22 AWG, Black

Figure 1- 30 Cable 10 Definition for Power Subsystem J14

Cable 11 - Front Panel BD

Part Number:
50.59904.021

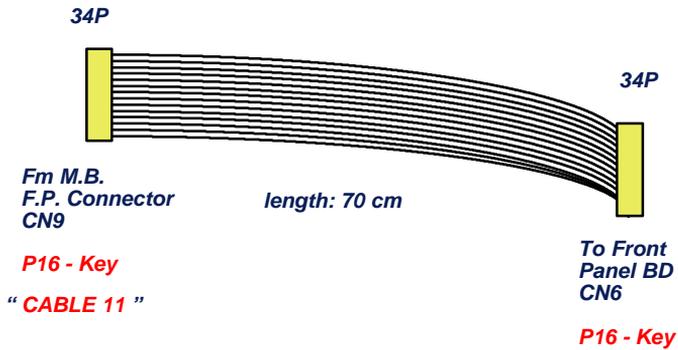


Figure 1- 31 Cable 11 Definition for the Front Panel Board

Cable 12 - Wide SCSI Cables

Part Number:
50.59906.001

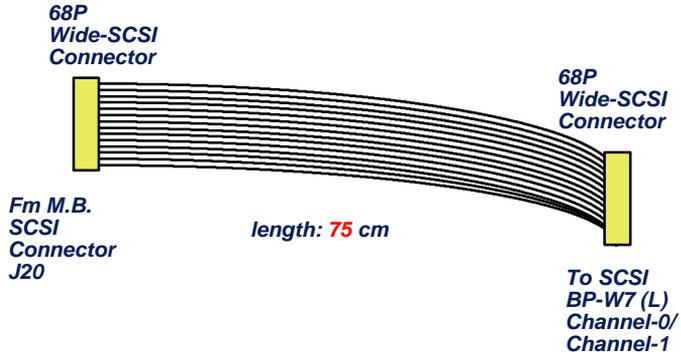
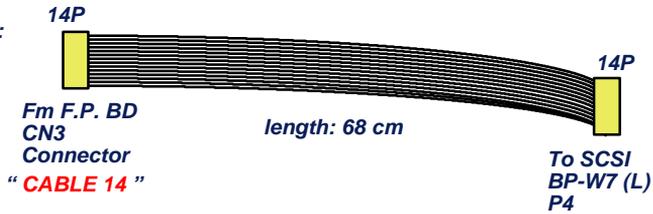


Figure 1- 32 Cable 12 Definition for the Wide SCSI Connectors

Cable 14 & 15 - SCSI B.P. BD

Part Number:
50.59903.041



Part Number:
50.59903.001

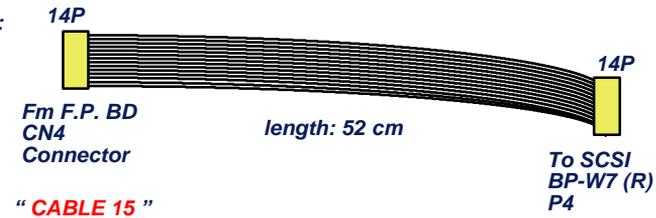


Figure 1- 33 Cables 14 and 15 Definition for the SCSI Backplane Board

Cable 16 & 17 - Floppy & IDE

Part Number:
50.59904.031

34P
Fm M.B.
Floppy
Connector
CN10

length: 47cm

34P
To FDD



Pin-5 : Key
" CABLE 16 "

* Note: Pin10 ~ Pin 16 must
be inverted for 3.25" FDD.

Part Number:
50.59905.011

40P
Fm M.B.
IDE
Connector
CN12

length: 47 cm

40P
To HDD

40P
To HDD

" CABLE 17 "

Figure 1- 34 Cables 16 and 17 Definition for Diskette and IDE Drives

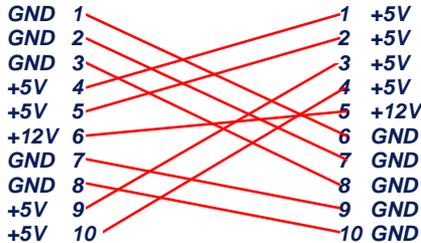
Cable 18 - Power Subsystem J7

Part Number:
50.59914.011

10P
Fm Power
Subs. J7
" C18/J7 "

28 cm

10P
To M.B.
CN2



* This end must add a
yellow caution label!

Figure 1- 35 Cable 18 Definition for Power Subsystem J7

Cable 19 - Narrow SCSI Cable

Part Number:
50.58607.001

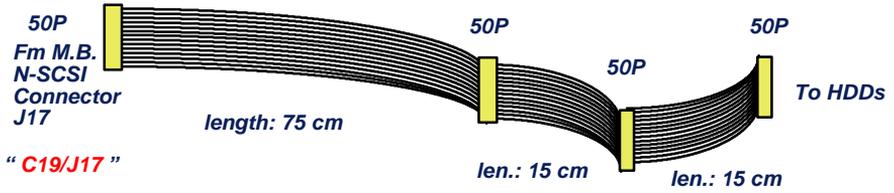


Figure 1- 36 Cable 19 Definition for the Narrow SCSI Connector

Major Chipsets

This chapter describes the major chipsets used in the X3 system board and memory board. It includes the chipset features, block diagram, and signal descriptions.

2.1 Pentium Pro processor (P6)

2.1.1 Features

The Pentium™ Pro (P6) CPU is the next generation in the Intel386™/Intel486™ family of microprocessors. The P6 processor maintains binary compatibility with the 8086/88, 80286, Intel386, Intel486, and Pentium processors. It integrates the second-level cache, APIC, and memory bus controller found in previous Intel processors as a single component.

The P6 processor provides significant performance improvements using the following internal architectural improvements:

- Super-scalar model
- Super-pipelined model
- Register renaming
- Out-of-order execution
- Speculative execution

The expected P6 processor performance gains, over a Pentium processor using the same process technology, are 1.5X (Integer Specmark), 2.0X (Floating-point Specmark), and 1.75X (Aggregate Specmark).

Increasing clock frequencies and processor performance can complicate system designs. To counter this trend, a primary design goal of the P6 processor bus is to simplify system design as much as possible while still providing advanced features and high performance. The P6 processor provides all of the debug hooks on previous generation processors, and has increased the debug information available directly from the bus. In addition, the P6 processor integrates several system components and has a configurable bus frequency.

The external P6 bus design enables it to be multiprocessor ready. It integrates bus arbitration and control, cache coherency circuitry, an MP interrupt controller, and other system-level functions into the bus interface.

To relax timing constraints, the P6 implements a synchronous latched bus protocol to enable a full clock cycle for signal transmission and a full-clock cycle for signal interpretation and generation. This latched protocol simplifies interconnect timing requirements and supports higher frequency system designs using inexpensive ASIC interconnect technology. The P6 bus uses low-voltage swing gunning transceiver logic (GTL) I/O buffers, making high-frequency signal communication easier.

The P6 processor component contains a processor core and a large second-level (L2) cache. The high internal cache hit rate satisfies most of the CPU core's bandwidth and latency requirements. The L2 cache reduces the P6 processor's external memory bandwidth requirement and makes the processor's performance less sensitive to bus access latency. Eliminating external caches removes some complexities in P6 processor system design.

The processor handles most of the P6 processor cache protocol complexity. A non-caching I/O bridge on the P6 bus does not need to comprehend the cache protocol and does not need snoop logic. The I/O bridge can issue standard memory accesses on the P6 bus, which are transparently snooped by all P6 bus agents. If data is modified in a P6 processor cache, the processor transparently provides data on the bus, instead of the memory controller. This functionality eliminates the need for a back-off capability that existing I/O bridges require to enable cache write-back cycles. The memory controller must observe snoop response signals driven by the P6 bus agents, absorb write-back data on a modified hit, and merge any write data.

The P6 processor integrates memory type range registers (MTRRs) that can replace the external address decode logic used to decode cacheability attributes.

The P6 bus protocol enables a near linear increase in system performance with an increase in the number of processors. The P6 processor interfaces to a multiprocessor system without any support logic. This "glueless" interface enables a desktop P6 processor system to be built with an upgrade socket for another P6 processor. The key design challenge in a P6 processor chipset is to take advantage of the P6 bus protocol and adapt to the higher bandwidth requirements of multiple processors.

The external P6 bus and P6 processor use a ratio clock design that provides modularity and upgradability. The processor's internal clock frequency is a multiple of the bus clock frequency, where the multiple is 2, 3, or 4. Only certain bus and processor frequency combinations are supported. This specification reserves additional combinations to provide future upgrade paths.

The ratio clock approach reduces the tight coupling between the processor clock and the external bus clock. For a fixed system-bus clock frequency, P6 processors introduced later with higher processor clock frequencies can use the same support chipset at the same bus frequency. Faster and slower P6 processors can co-exist in the same system. A customer's investment in a P6 processor chipset is protected for a longer time and for a greater range of processor frequencies. The ratio clock approach also preserves system modularity, allowing a system's electrical topology to determine the system bus clock frequency while process technology can determine the processor clock frequency.

The P6 bus architecture provides a number of features to support high reliability and high availability designs. Most of these additional features can be disabled, if necessary. For example, the bus architecture allows the data bus to be unprotected with parity, or protected with an error correcting code (ECC). Error detection and limited recovery are built into the bus protocol.

A P6 processor-based cluster can contain up to four P6 processors, and a combination of four other loads consisting primarily of memory controllers, I/O bridges, and custom attachments.

In a four-processor system, the data bus is the most critical resource. To account for this situation the P6 bus implements several features to maximize available bus bandwidth. These features allow for pipelined transactions in which bus transactions in different phases overlap an increase in transaction pipeline depth over previous generations, and support for deferring a transaction for later completion.

A P6 processor system for the high-end server market can contain four-processor clusters, each behind a level 2 (L2) cache controller. The P6 processor cache protocol provides flexibility in the L2 cache design, enabling high-end servers to use their L2 cache design for a key difference in performance. Non-latency L2 misses can be supported in a deferred reply mode without preventing further transactions from being issued and completed.

The P6 bus architecture is therefore adaptable to various classes of systems. In desktop multiprocessor systems, a subset of the bus features can be used. In the low-end server market, the P6 bus provides an easier entry into low-end multiprocessing with linear increases in performance as CPUs are added. Finally, the P6 bus meets the demands of the high-end server marketplace, allowing P6 processor systems to be considered for applications currently being downsized.

2.1.2 Pin Diagram

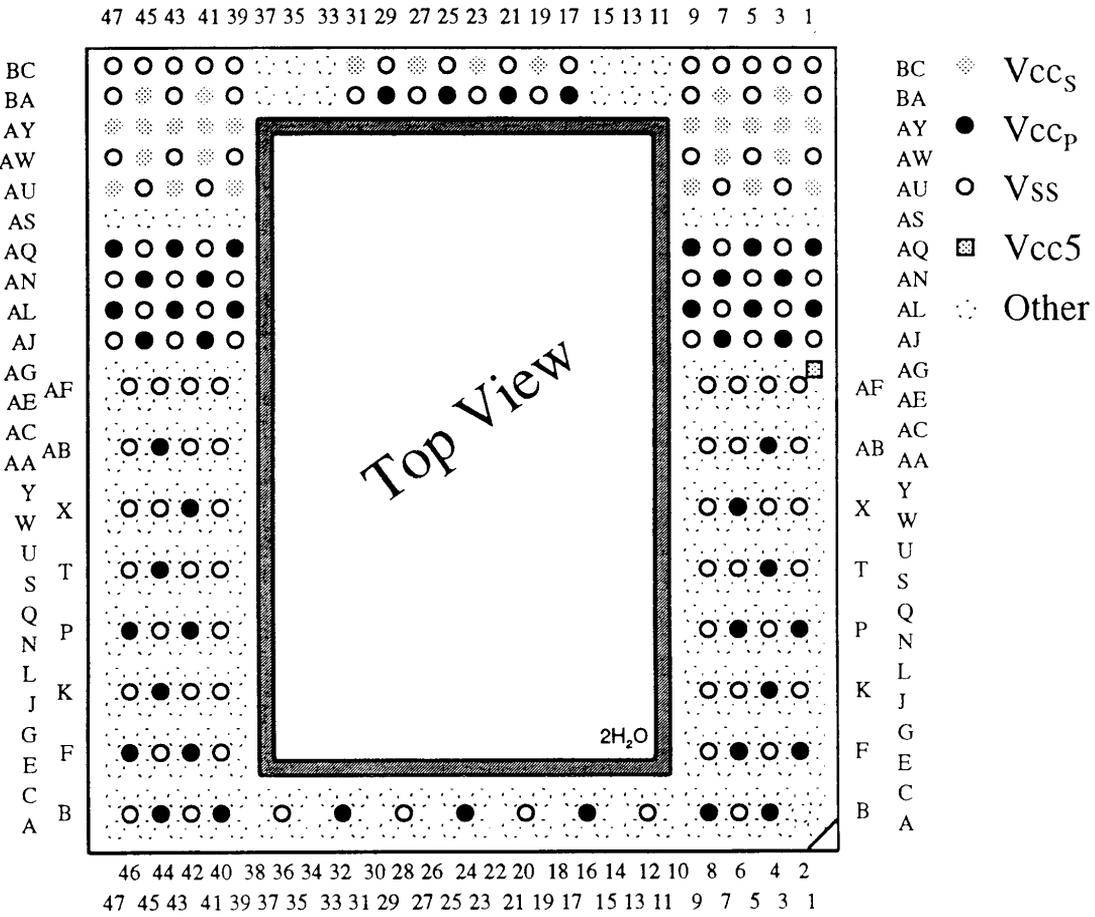


Figure 2- 1 P6 Processor Pin Diagram

2.1.3 CPU ID

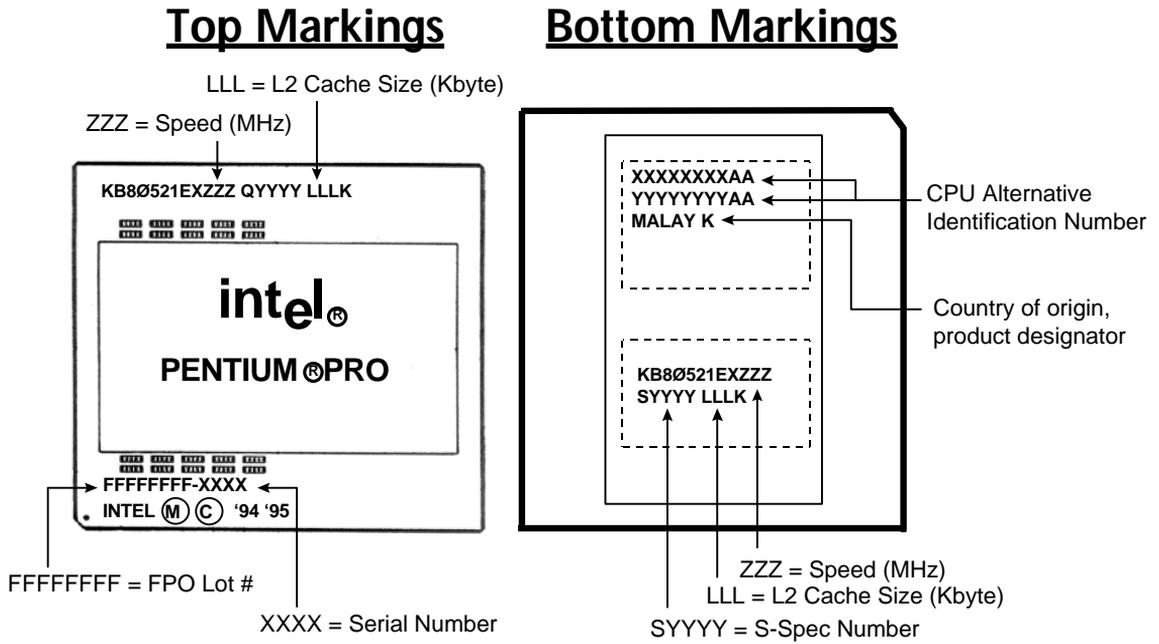


Figure 2-2 Pentium Pro CPU Identification Markings

Source: Intel Pentium Pro Processor Specification Update released on May 15, 1996.

2.1.4 Signal Types

The P6 processor has following signal types.

- 3.3V Tolerant Type (TTL-compatible)
- 5V Tolerant Type (TTL-compatible)
- GTL+ Type
- JTAG Type

2.1.4.1 GTL+ Type

Most of the P6 processor signals use a variation of the low-voltage Gunning Transceiver Logic (GTL) signaling technology. The P6 processor bus specification is similar to the GTL specification plus enhancements to provide larger noise margins and reduced ringing. This is accomplished by increasing the termination voltage level and controlling the edge rates. Since this specification is different from the standard GTL specification, it is referred to as GTL+ in this document.

The GTL+ signals are open-drain and require external termination to a supply that provides the high-signal level. The GTL+ inputs use differential receivers that require a reference signal (V_{REF}). Termination, usually a resistor on each end of the signal trace, is used to pull the bus up to the high-voltage level and to control reflections on the stub-free transmission line. The receivers use V_{REF} to determine if a signal is a logical 0 or a logical 1.

Table 2-1 lists the bus termination voltage specifications for GTL+.

Table 2- 1 GTL+ Bus Termination Voltage Specifications

Symbol	Parameter	Voltage (V)
V_{TT}	Bus Termination Voltage	$1.5 \pm 10\%$
V_{REF}	Input Reference Voltage	$2/3 V_{TT} \pm 2\%$



V_{REF} should be created from V_{TT} by a voltage divider of 1% resistors.

There are eight V_{REF} pins on the P6 processor to ensure that internal noise does not affect the performance of the I/O buffers. Pins A1, C7, S7 and Y7 (V_{REF} [3:0]) must be tied together while pins A47, U41, AE47 and AG45 (V_{REF} [7:4]) must be tied together. The two groups may also be tied to each other if desired.

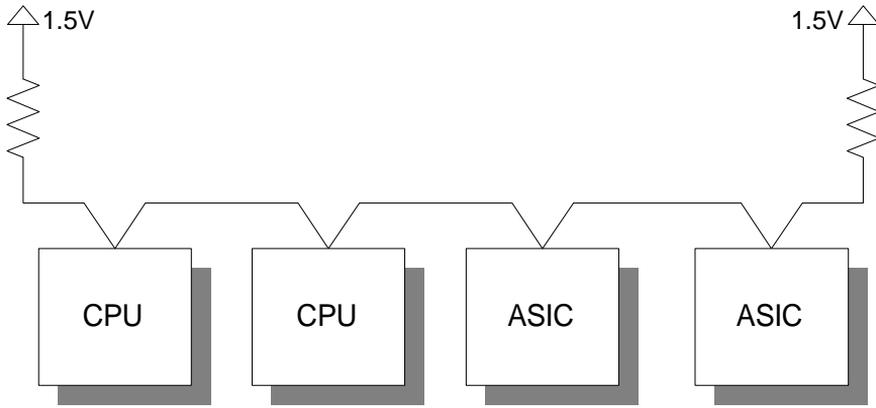


Figure 2- 3 GTL+ Bus Topology

2.1.4.2 JTAG

JTAG stands for Joint Test Action Group. This signal type is tolerant to 3.3V and especially used for testing and debugging.

2.1.5 Signal Descriptions

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
A[35:32]# A[31:28]# A[27:24]# A[23:20]# A[19:16]# A[15:12]# A[11:08]# A[07:03]#	C1, E9, E7, E5 G9, E3, E1, J9 G5, G7, L9, G3 J7, G1, J3, J5 J1, L7, N9, L3 L5, N3, N7, N1 N5, Q9, Q1, Q7 Q3, S1, Q5, S3 S5	I/O, GTL+	<p>The A[35:3]# signals are the address signals. They are driven during the two-clock request phase by the request initiator. The signals in the two clocks are referenced Aa[35:3]# and Ab[35:3]#. During both clocks, A[35:24]# signals are protected with the AP1# parity signal, and A[23:3]# signals are protected with the APO# parity signal.</p> <p>The Aa[35:3]# signals are interpreted based on information carried during the first request phase clock on the REQa[4:0]# signals.</p> <p>For memory transactions as defined by REQa[4:0]# = {XX01X,XX10X,XX11X}, the Aa[35:3]# signals define a 236-byte physical memory address space. The cacheable agents in the system observe the Aa[35:3]# signals and begin an internal snoop. The memory agents in the system observe the Aa[35:3]# signals and begin address decode to determine if they are responsible for the transaction completion. Aa[4:3]# signals define the critical word, the first data chunk to be transferred on the data bus.</p> <p>For P6.0 DX IO transactions as defined by REQa[4:0]# = 1000X, the signals Aa[16:3]# define a 64K+3 byte physical IO space. The IO agents in the system observe the signals and begin address decode to determine if they are responsible for the transaction completion. Aa[35:17]# are always zero. Aa[16:3]# is zero unless the IO space being accessed is the first three bytes of a 64KB address range.</p> <p>For deferred reply transactions as defined by REQa[4:0]# = 00000, Aa[23:16]# carry the deferred ID. This signal is the same deferred ID supplied by the request initiator of the original transaction on Ab[23:16]#/DID[7:0]# signals. P6 bus agents that support deferred replies sample the deferred ID and perform an internal match against any outstanding transactions waiting for deferred replies. During a deferred reply, Aa[35:24]# and Aa[15:3]# are reserved.</p> <p>For the branch-trace message transaction as defined by REQa[4:0]# = 01001 and for special and interrupt acknowledge transactions, as defined by REQa[4:0]# = 01000, the Aa[35:3]# signals are reserved and undefined.</p>

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
A[35:32]# A[31:28]# A[27:24]# A[23:20]# A[19:16]# A[15:12]# A[11:08]# A[07:03]# (continued)	C1, E9, E7, E5 G9, E3, E1, J9 G5, G7, L9, G3 J7, G1, J3, J5 J1, L7, N9, L3 L5, N3, N7, N1 N5, Q9, Q1, Q7 Q3, S1, Q5, S3 S5	I/O, GTL+	<p>During the second clock of the request phase, Ab[35:3]# signals perform identical signal functions for all transactions. For ease of description, these functions are described using new signal names. Ab[31:24]# are renamed the attribute signals ATTR[7:0]#. Ab[23:16]# are renamed the Deferred ID signals DID[7:0]#. Ab[15: 8]# are renamed the eight-byte enable signals BE[7:0]. Ab[7:3]# are renamed the extended function signals EXF[4:0].</p> <p>On the active-to-inactive transition of RESET#, each P6 bus agent samples A[35:3]# signals to determine its power-on configuration. Two clocks after RESET# is sampled deasserted, these signals begin normal operation.</p>
A20M#	A11	I, 3.3V	<p>The A20M# signal is the address-20 mask signal in the PC Compatibility group. If the A20M# input signal is asserted, the P6 processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wraparound at the one MB boundary. Only assert A20M# when the processor is in real mode. The effect of asserting A20M# in protected mode is undefined and may be implemented differently in future processors.</p> <p>Snoop requests and cache-line write-back transactions are unaffected by A20M# input. Address 20 is not masked when the processor samples external addresses to perform internal snooping.</p> <p>A20M# is an asynchronous input. However, to guarantee recognition of this signal that follows an I/O write instruction, A20M# must be valid with active RS[2:0]# signals of the corresponding I/O write bus transaction. In FRC mode, A20M# must be synchronous to BCLK.</p> <p>During active RESET#, the P6 processor begins sampling the A20M# and IGNNE# values to determine the ratio of core-clock frequency to bus-clock frequency.</p>

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description																																													
A20M# continued	A11	I, 3.3V	<p>The following table shows the bus frequency to core frequency ratio configuration:</p> <table border="1"> <thead> <tr> <th>Ratio of Core Clock to Bus Clock</th> <th>LINT[1]</th> <th>LINT[0]#</th> <th>IGNNE#S</th> <th>A20M#</th> </tr> </thead> <tbody> <tr> <td>2</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>3</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>4</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>5</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>5/2</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>7/2</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>9/2</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>11/2</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>(All other combinations are reserved.)</p>	Ratio of Core Clock to Bus Clock	LINT[1]	LINT[0]#	IGNNE#S	A20M#	2	0	0	0	0	3	0	0	1	0	4	0	0	0	1	5	0	0	1	1	5/2	0	1	0	0	7/2	0	1	1	0	9/2	0	1	0	1	11/2	0	1	1	1
Ratio of Core Clock to Bus Clock	LINT[1]	LINT[0]#	IGNNE#S	A20M#																																												
2	0	0	0	0																																												
3	0	0	1	0																																												
4	0	0	0	1																																												
5	0	0	1	1																																												
5/2	0	1	0	0																																												
7/2	0	1	1	0																																												
9/2	0	1	0	1																																												
11/2	0	1	1	1																																												
ADS#	AE3	I/O, GTL+	<p>The ADS# signal is the address strobe signal. It is asserted by the current bus owner for one clock to indicate a new request phase. A new request phase can only begin if the in-order queue has less than the maximum number of entries defined by the power-on configuration (1 or 8), the request phase is not being stalled by an active BNR# sequence and the ADS# associated with the previous request phase is sampled inactive. Along with the ADS#, the request initiator drives A[35:3]#, REQ[4:0]#, AP[1:0]#, and RP# signals for two clocks. During the second request phase clock, ADS# must be inactive. RP# provides parity protection for REQ[4:0]# and ADS# signals during both clocks. If the transaction is part of a bus locked operation, LOCK# must be active with ADS#.</p> <p>If the request initiator continues to own the bus after the first request phase, it can issue a new request every three clocks. If the request initiator needs to release the bus ownership after the request phase, it can deactivate its BREQn#/BPRI# arbitration signal as early as with the activation of ADS#.</p> <p>All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. On sampling the asserted ADS#, all agents load the new transaction in the in-order queue and update internal counters. The error, snoop, response, and data phase of the transaction are defined with respect to ADS# assertion.</p>																																													

Table 2-2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
AERR#	AE9	I/O, GTL+	<p>The AERR# signal is the address parity error signal. Assuming the AERR# driver is enabled during the power-on configuration, a bus agent can drive AERR# active for exactly one clock during the error phase of a transaction. AERR# must be inactive for a minimum of two clocks. The error phase is always three clocks from the beginning of the request phase.</p> <p>On observing active ADS#, all agents begin parity and protocol checks for the signals valid in the two request phase clocks. Parity is checked on AP[1:0]# and RP# signals. AP1# protects A[35:24]#, AP0# protects A[23:3]# and RP# protects REQ[4:0]#. A parity error without a protocol violation is signaled by AERR# assertion.</p> <p>If AERR# observation is enabled during a power-on configuration, AERR# assertion in a valid error phase aborts the transaction. All bus agents remove the transaction from the in-order queue and update internal counters. The snoop phase, response phase, and data phase of the transaction are aborted. Specifically if the snoop phase associated with the aborted transaction is driven in the next clock, the snoop results, including a STALL condition (HIT# and HITM# asserted for one clock), are ignored. All bus agents must also begin an arbitration reset sequence and deassert BREQn#/BPRI# arbitration signals on sampling AERR# active. A current bus owner in the middle of a bus lock operation must keep LOCK# asserted and assert its arbitration request BPRI#/BREQn# after keeping it inactive for two clocks to retain its bus ownership and guarantee lock atomicity. All other agents, including the current bus owner not in the middle of a bus lock operation, must wait at least 4 clocks before asserting BPRI#/BREQn# and beginning a new arbitration.</p> <p>If AERR# observation is enabled, the request initiator can retry the transaction up to n times until it reaches the retry limit defined by its implementation. After n retries, the request initiator treats the error as a hard error. The request initiator asserts BERR# or enters the machine check exception handler, as defined by the system configuration.</p> <p>If AERR# observation is disabled during a power-on configuration, AERR# assertion is ignored by all bus agents except a central agent. Based on the system machine check architecture, the central agent can ignore AERR#, assert NMI to execute NMI handler, or assert BINIT# to reset</p>

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
			the bus units of all agents and execute an MCE handler.
AP[1:0]#	S9, U1	I/O, GTL+	<p>The AP[1:0]# signals are the address parity signals. They are driven by the request initiator during the two request phase clocks along with ADS#, A[35:3]#, REQ[4:0]#, and RP#. AP1# covers A[35:24]#. AP0# covers A[23:3]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This rule allows parity to be high when all the covered signals are high.</p> <p>Provided "AERR# drive" is enabled during the power-on configuration, all bus agents begin parity checking on observing active ADS# and determine if there is a parity error. On observing a parity error on any one of the two request phase clocks, the bus agent asserts AEPR# during the error phase of the transaction.</p>
BCLK	A19	I, 3.3V	<p>The BCLK (clock) signal is the execution control group input signal. It determines the bus frequency. All agents drive their outputs and latch their inputs on the BCLK rising edge.</p> <p>The BCLK signal indirectly determines the P6 processor's internal clock frequency. Each P6 processor derives its internal clock from BCLK by multiplying the BCLK frequency by 2, 3, or 4 as defined and allowed by the power-on configuration.</p> <p>All external timing parameters are specified with respect to the BCLK signal.</p>
BERR#	C5	I/O, GTL+	<p>The BERR# signal is the error group bus error signal. It indicates an unrecoverable error without a bus protocol violation if asserted.</p> <p>The BERR# protocol is as follows: If an agent detects an unrecoverable error for which BERR# is a valid error response and BERR# is sampled inactive, it asserts BERR# for three clocks. An agent can assert BERR# only after observing that the signal is inactive. An agent asserting BERR# must deassert the signal in two clocks if it observes that another agent began asserting BERR# in the previous clock.</p> <p>BERR# assertion conditions are defined by the system configuration. Configuration options enable the BERR# driver as follows:</p> <ul style="list-style-type: none"> • enabled or disabled asserted optionally for internal errors along with IERR# optionally asserted by the request initiator of a bus transaction after it observed an error • asserted by any bus agent when it observes an error

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
			in a bus transaction
BERR# continued	C5	I/O, GTL+	BERR# sampling conditions are also defined by the system configuration. Configuration options enable the BERR# receiver to be enabled or disabled. When the bus agent samples an active BERR# signal and if MCE is enabled, the P6 processor enters the machine check handler. If MCE is disabled, typically the central agent forwards BERR# as an NMI to one of the processors.
BINIT#	AC43	I/O, GTL+	<p>The BINIT# signal is the bus initialization signal. If the BINIT# driver is enabled during the power on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information.</p> <p>The BINIT# protocol is as follows: If an agent detects an error for which BINIT# is a valid error response, and BINIT# is sampled inactive, it asserts BINIT# for three clocks. An agent can assert BINIT# only after observing that the signal is inactive. An agent asserting BINIT# must deassert the signal in two clocks if it observes that another agent began asserting BINIT# in the previous clock.</p> <p>If BINIT# observation is enabled during a power-on configuration, and BINIT# is sampled asserted, all bus state machines are reset. All agents reset their rotating ID for bus arbitration to the state after reset, and internal count information is lost. The L1 and L2 caches are not affected.</p> <p>If BINIT# observation is disabled during power-on configuration, BINIT# is ignored by all bus agents except a central agent that must handle the error in a manner appropriate to the system architecture.</p>
BNR#	U7	I/O, GTL+	<p>The BNR# signal is the block next request signal in the arbitration group. The BNR# signal is used to assert a bus stall by any bus agent who is unable to accept new bus transactions to avoid an internal transaction queue overflow. During a bus stall, the current bus owner cannot issue any new transactions.</p> <p>Since multiple agents might need to request a bus stall at the same time, BNR# is a wire-OR signal. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.</p>

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
BNR# continued	U7	I/O, GTL+	<p>A valid bus stall involves assertion of BNR# for one clock on a well-defined clock edge (T1), followed by de-assertion of BNR# for one clock on the next clock edge (T1+1). BNR# can first be sampled on the second clock edge (T1+1) and must always be ignored on the third clock edge (T1+2). An extension of a bus stall requires one clock active (T1+2), one clock inactive (T1+3) BNR# sequence with BNR# sampling points every two clocks (T1+1, T1+3,...).</p> <p>After the RESET# active-to-inactive transition, bus agents might need to perform hardware initialization of their bus unit logic. Bus agents intending to create a request stall must assert BNR# in the clock after RESET# is sampled inactive.</p> <p>After BINIT# assertion, all bus agents go through a similar hardware initialization and can create a request stall by asserting BNR# four clocks after BINIT# assertion is sampled.</p> <p>On the first BNR# sampling clock that BNR# is sampled inactive, the current bus owner is allowed to issue one new request. Any bus agent can immediately reassert BNR# (four clocks from the previous assertion or two clocks from the previous de-assertion) to create a new bus stall. This throttling mechanism enables independent control on every new request generation.</p> <p>If BNR# is deasserted on two consecutive sampling points, new requests can be freely generated on the bus. After receiving a new transaction, a bus agent can require an address stall due to an anticipated transaction-queue overflow condition. In response, the bus agent can assert BNR#, three clocks from active ADS# assertion and create a bus stall. Once a bus stall is created, the bus remains stalled until BNR# is sampled asserted on subsequent sampling points.</p>
BP[3:2]#	AC39, AE43	I/O, GTL+	<p>The BP[3:2]# signals are the system support group breakpoint signals. They are outputs from the PE processor that indicates the status of breakpoints.</p>
BPM[1:0]#	AA39, AC41	I/O, GTL+	<p>The BPM[1:0]# signals are more system support group breakpoint and performance monitor signals. They are outputs from the P6 processor that indicates the status of breakpoints and programmable counters used for monitoring P6 performance.</p>

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
BPRI#	U5	I, GTL+	<p>The BPRI# is the priority-agent bus request signal. The priority agent arbitrates for the bus by asserting BPRI#. The priority agent is always the next bus owner. Observing BPRI# active causes the current symmetric owner to stop issuing new requests unless the requests are part of an ongoing locked operation.</p> <p>If LOCK# is sampled inactive two clocks from BPRI# driven asserted, the priority agent can issue a new request within four clocks of asserting BPRI#. The priority agent can further reduce its arbitration latency to two clocks if it samples active ADS# and inactive LOCK# on the clock in which BPRI# was driven active. It can reduce its arbitration latency to three clocks if it samples active ADS# and inactive LOCK# on the clock in which BPRI# was sampled active. If LOCK# is sampled active, the priority agent must wait for LOCK# to be sampled deasserted to gain bus ownership in two clocks. The priority agent can keep BPRI# asserted until all of its requests are completed and can release the bus by deasserting BPRI# at the same clock edge on which it issued the last request.</p> <p>On observation of active AERR#, RESET#, or BINIT#. BPRI# must be deasserted in the next clock. BPRI# can be reasserted in the clock after sampling the RESET# active-to-inactive transition or three clocks after sampling BINIT# active and RESET# inactive. On AERR# assertion, if the priority agent is in the middle of a bus-locked operation, BPRI# must be reasserted after two clocks, otherwise BPRI# must stay inactive for at least 4 clocks.</p> <p>After the RESET# inactive transition, P6 bus agents begin BPRI# and BNR# sampling on BNR# sample points. If both BNR# and BPRI# are observed inactive on BNR# sampling points, the P6 APIC units on a common APIC bus are synchronized. In a system with multiple P6 bus clusters sharing a common APIC bus, BPRI# signals of all clusters must be asserted after RESET# until BNR# is observed inactive on a BNR# sampling point. The BPRI# signal on all P6 buses must then be deasserted within 100ns of each other to accomplish APIC bus synchronization across all processors.</p>
CPUPRES#	B2	Other	<p>CPUPRES# is a ground pin that allows a designer to detect the presence of a processor in a socket.</p>

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description																																							
BR0# BR[3:1]#	AC5 U9, AA1, W3	I/O, GTL+ I, GTL+	<p>The BR[3:0]# pins are the physical bus request pins that drive the BREQ[3:0]# signals in the system. The BREQ[3:0]# signals are interconnected in a rotating manner to individual processor pins. Below are the rotating interconnections between the processor and bus signals.</p> <table border="1"> <thead> <tr> <th rowspan="2">Bus Signal</th> <th colspan="4">Pins</th> </tr> <tr> <th>Agent 0</th> <th>Agent 1</th> <th>Agent 2</th> <th>Agent 3</th> </tr> </thead> <tbody> <tr> <td>BREQ0#</td> <td>BR0#</td> <td>BR3#</td> <td>BR2#</td> <td>BR1#</td> </tr> <tr> <td>BREQ1#</td> <td>BR1#</td> <td>BR0#</td> <td>BR3#</td> <td>BR2#</td> </tr> <tr> <td>BREQ2#</td> <td>BR1#</td> <td>BR0#</td> <td>BR3#</td> <td>BR3#</td> </tr> <tr> <td>BREQ3#</td> <td>BRS#</td> <td>BR2#</td> <td>BR1#</td> <td>BR0#</td> </tr> </tbody> </table> <p>During a power-up configuration, the central agent must assert the BR0# bus signal. All symmetric agents sample their BR[3:0]# pins on active-to-inactive transition of RESET#. The pin on which the agent samples an active level determines its agent ID. All agents then configure their pins to match the appropriate bus signal protocol, as shown in below:</p> <table border="1"> <thead> <tr> <th>Pin sampled active on RESET#</th> <th>Agent ID</th> </tr> </thead> <tbody> <tr> <td>BR0#</td> <td>0</td> </tr> <tr> <td>BR3#</td> <td>1</td> </tr> <tr> <td>BR2#</td> <td>2</td> </tr> <tr> <td>BR1#</td> <td>3</td> </tr> </tbody> </table>	Bus Signal	Pins				Agent 0	Agent 1	Agent 2	Agent 3	BREQ0#	BR0#	BR3#	BR2#	BR1#	BREQ1#	BR1#	BR0#	BR3#	BR2#	BREQ2#	BR1#	BR0#	BR3#	BR3#	BREQ3#	BRS#	BR2#	BR1#	BR0#	Pin sampled active on RESET#	Agent ID	BR0#	0	BR3#	1	BR2#	2	BR1#	3
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D[63:60]# D[59:56]# D[55:52]# D[51:48]# D[47:44]# D[43:40]# D[39:36]# D[35:32]# D[31:28]# D[27:24]# D[23:20]# D[19:16]# D[15:12]# D[11:08]# D[07:04]# D[03:00]#	W43, Y47, W45, U43 S39, W47, S41, U45 U47, S43, S45, Q41 Q39, S47, Q43, Q45 N43, Q47, N41, N39 L43, N45, N47, L41 L47, J43, L39, L45 J41, J47, J45, J39 G47, G43, G41, G45 G39, E47, E43, E45 E41, E39, C47, C41 C45, C43, C39, A45 C37, A37, A43, C35 A41, A39, A35, A33 C33, C31, A31, C29 A29, C27, A27, C25	I/O, GTL+	<p>The D[63:0]# signals are the data signals. They are driven during the data phase by the agent responsible for driving the data. These signals provide a 64-bit data path between various P6 bus agents. The 32-byte line transfers require four data transfer clocks with valid data on all eight bytes. Partial transfers require one data transfer clock with valid data on the byte(s) indicated by active byte enables BE[7:0]#. Data signals not valid for a particular transfer must still have correct ECC (if data bus ECC is selected). If BE0# is asserted, D[7:03]# transfers the least significant byte. If BE7# is asserted, D[63:56]# transfers the most significant byte.</p> <p>The data driver asserts DRDY# to indicate a valid data transfer. If the data phase involves more than one clock the data driver also asserts DBSY# at the beginning of the data phase and deasserts DBSY# on the same clock that it performs the last data transfer.</p>																																							

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
DBSY#	AA5	I/O, GTL+	<p>The DBSY# signal is the data-bus busy signal. It indicates that the data bus is busy. It is asserted by the agent responsible for driving the data during the data phase, provided the data phase involves more than one clock. DBSY# is asserted at the beginning of the data phase and is deasserted on the same clock on which the last data is driven.</p> <p>When normal read data is being returned, the data phase begins with the response phase. Thus the agent returning read data can assert DBSY# when the transaction reaches the top of the in-order queue and it is ready to return response on RS[2:0]# signals. In response to a write request, the agent driving the write data must drive DBSY# active after the write transaction reaches the top of the in-order queue and it sees active TRDY# with inactive DBSY# indicating that the target is ready to receive data. For an implicit write-back response, the snoop agent must assert DBSY# active after the target memory agent of the implicit write-back asserts TRDY#. Implicit write-back TRDY# assertion begins after the transaction reaches the top of the in-order queue, and TRDY# de-assertion associated with the write portion of the transaction, if any, is completed. In this case, the memory agent guarantees assertion of implicit write-back response in the same clock in which the snooping agent asserts DBSY#.</p>
DEFER#	Y5	I, GTL+	<p>The DEFER# signal is the defer signal. It is asserted by an agent during the snoop phase to indicate that the transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory: agent or I/O agent. For systems that involve resources on a system bus other than the P6 bus, a bridge agent can accept the DEFER# assertion responsibility on behalf of the addressed agent.</p> <p>DEFER# can only be asserted if DEN# is active during the request phase. When HITM# and DEFER# are both active during the snoop phase, HITM# is given priority and the transaction must be completed with implicit write-back response. If HITM# is inactive, and DEFER# active, the agent asserting DEFER# must complete the transaction with a deferred or retry response.</p>

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
DEFER#	Y5	I, GTL+	<p>If DEFER# is inactive, or HITM# is active, then the transaction is committed for in-order completion and snoop ownership is transferred normally between the requesting agent, the snooping agents, and the response agent.</p> <p>If DEFER# is active with HITM# inactive, the transaction commitment is deferred. If the defer agent completes the transaction with a retry response, the requesting agent must retry the transaction. If the defer agent returns a deferred response, the requesting agent must freeze snoop state transitions associated with the deferred transaction and issues of new order-dependent transactions until the corresponding deferred reply transaction. In the meantime, the ownership of the deferred address is transferred to the defer agent and it must guarantee management of conflicting transactions issued to the same address.</p> <p>If DEFER# is active in response to a newly issued bus-lock transaction, the entire bus-locked operation is re-initiated regardless of HITM#. This feature is useful for a bridge agent in response to a split bus-locked operation. It is recommended that the bridge agent extend the snoop phase of the first transaction in a split locked operation until it can either guarantee ownership of all system resources to enable successful completion of the split sequence or assert DEFER# followed by a retry response to abort the split sequence.</p>
DEP[7:0]#	U39, Y45, AA47, W41, A47, W39, Y43, AC45	I/O, GTL+	<p>The DEP[7:0]# signals are the data bus ECC/parity signals. They are driven during the data phase by the agent responsible for driving D[63:0]#. The DEP[7:0]# signals provide optional ECC protection for the data bus. During power-on configuration, DEP[7:0]# signals can be enabled for either ECC checking or no checking.</p> <p>The ECC error correcting code can detect and correct single-bit errors and detect double-bit or nibble errors.</p> <p>DEP[7:0]# provide valid ECC for the entire data bus on each data clock, regardless of which bytes are valid. If checking is enabled, receiving agents check the ECC signals for all 64 data signals.</p>

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
DRDY#	AA3	I/O, GTL+	The DRDY# signal is the data phase data-ready signal. The data driver asserts DRDY# on each data transfer, indicating valid data on the data bus. In a multi-cycle data transfer, DRDY# can be deasserted to insert idle clocks in the data phase. During a line transfer, DRDY# is active for four clocks. During a partial 1-to-8 byte transfer, DRDY# is active for one clock. Except for the last data clock during a data phase, DRDY# and DBSY# must both be active together. If a data transfer is exactly one clock, then the entire data phase consists of one clock active DRDY# and inactive DBSY#.
FERR#	C17	O, 3.3V	The FERR# signal is the PC compatibility group floating-point error signal. The P6 processor asserts FERR# when it detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel387 coprocessor. FERR# is included for compatibility with systems using DOS-type floating-point error reporting.
FLUSH#	A15	I, 3.3V	<p>When the FLUSH# input signal is asserted, the P6 bus agent writes back all internal cache lines in the modified state and invalidates all internal cache lines. At the completion of a flush operation, the P6 processor issues a flush acknowledge transaction to indicate that the cache flush operation is complete. The P6 processor stops caching any new data while the FLUSH# signal remains asserted.</p> <p>FLUSH# is an asynchronous input. However, to guarantee recognition of this signal following an I/O write instruction, FLUSH# must be valid along with RS[2:0]# in the response phase of the corresponding I/O Write bus transaction. In FRC mode, FLUSH# must be synchronous to BCLK.</p> <p>On active-to-inactive transition of RESET#, each P6 bus agent samples FLUSH# signals to determine its power-on configuration. Two clocks after RESET# is sampled deasserted, these signals begin normal operation.</p>

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
FRCERR	C9	I/O, GTL+	<p>The FRCERR signal is the error group 7 functional-redundancy-check error signal. If two P6 processors are configured in an FRC pair, as a single "logical" processor, then the checker processor asserts FRCERR if it detects a mismatch between its internally sampled outputs and the master processor's outputs. The checker's FRCERR output pin is connected to the master's FRCERR input pin.</p> <p>For point-to-point connections, the checker always compares against the master's outputs. For bussed single-driver signals, the checker compares against the signal when the master is the only allowed driver. For bussed multiple-driver wire-OR signals, the checker compares against the signal only if the master is expected to drive the signal low.</p> <p>FRCERR is also toggled during the P6 processor's reset action. A P6 processor asserts FRCERR for approximately 1 second after RESET's active-to-inactive transition if it executes its built-in self-test (BIST). When BIST execution completes, the P6 processor de-asserts FRCERR if BIST completed successfully and continues to assert FRCERR if BIST fails. If the P6 processor does not execute the BIST action, then it keeps FRCERR asserted for approximately 20 clocks and then deasserts it.</p>
HIT# HITM#	AC3 AA7	I/O, GTL+ I/O, GTL+	<p>The HIT# and HITM# signals are snoop-hit and hit-modified signals. They are snoop results asserted by any P6 bus agent in the snoop phase.</p> <p>Any bus agent can assert both HIT# and HITM# together for one clock in the snoop phase to indicate that it requires a snoop stall. When a stall condition is sampled, all bus agents extend the snoop phase by two clocks. The stall can be continued by reasserting HIT# and HITM# together every other clock for one clock.</p> <p>A caching agent must assert HITM# for one clock in the snoop phase if the transaction hits a modified line, and the snooping agent must perform an implicit write-back to update main memory. The snooping agent with the modified line makes a transition to shared state if the original transaction is read line or read partial, otherwise it transitions to invalid state. A deferred reply transaction may have HITM# asserted to indicate the return of unexpected data.</p>

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
HIT# HITM# continued	AC3 AA7	I/O, GTL+ I/O, GTL+	<p>A snooping agent must assert HIT# for one clock during the snoop phase if the line does not hit a modified line in its write-back cache and if at the end of the transaction its plans to keep the line in shared state. Multiple caching agents can assert HIT# in the same snoop phase. If the requesting agent observes HIT# active during the snoop phase it can not cache the line in exclusive or modified state.</p> <p>On observing a snoop stall, the agents asserting HIT# and HITM# independently reassert the signal after one inactive clock so that the correct snoop result is available, in case the snoop phase terminates after the two clock extension.</p>
IERR#	C3	O, 3.3V	<p>The IERR# is the error group internal error signal. A P6 processor asserts IERR# when it observes an internal error. It keeps IERR# asserted until it is turned off as part of the machine check error or the NMI handler in software, or with RESET#, BINIT#, and INIT# assertion.</p> <p>An internal error can be handled in several ways inside the processor based on its power-on configuration. If MCE is enabled, IERR# causes an MCE entry. IERR# can also be directed on the BERR# pin to indicate an error. Usually BERR# is sampled back by all processors to enter MCE or it can be redirected as an NMI by the central agent.</p>
IGNNE#	A9	I, 3.3V	<p>The IGNNE# signal is the PC Compatibility group Ignore numeric error signal. If IGNNE# is asserted, the P6 processor ignores a numeric error and continues to execute non-control floating-point instructions. If IGNNE# is deasserted, the P6 processor freezes on a non-control floating-point instruction if previous instruction caused an error.</p> <p>IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is an asynchronous input. However, to guarantee recognition of this signal following an I/O write instruction, IGNNE# must be valid along with RS[2:0]# in the response phase of the corresponding I/O Write bus transaction. In FRC mode, IGNNE# must be synchronous to BCLK. During active RESET#, the P6 processor begins sampling the A20M# and IGNNE# values to determine the ratio of core-clock frequency to bus-clock frequency. (See A20M# signal description for details).</p> <p>After the PLL-lock time, the core clock is stabilized and locked to the external bus clock. On the active-to-inactive transition of RESET#, the P6 processor latches A20M# and IGNNE# and freezes the frequency ratio internally. Normal operation on the two signals continues two clocks</p>

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
			after sampling RESET# inactive.
INIT#	C11	I, 3.3V	<p>The INIT# signal is the execution control group initialization signal. Active INIT# input resets integer registers inside all P6 processors without affecting their internal (L1 or L2) caches or their floating-point registers. Each P6 processor begins execution at the power-on reset vector configured during power-on configuration regardless of whether INIT# has gone inactive. The processor continues to handle snoop requests during INIT# assertion.</p> <p>INIT# can be used to help performance of DOS extenders written for the Intel 80286 processor. INIT# provides a method to switch from protected mode to real mode while maintaining the contents of the internal caches and floating-point state. INIT# can not be used in lieu of RESET# after power-up.</p> <p>On active-to-inactive transition of RESET#, each P6 bus agent samples INIT# signals to determine its power-on configuration. Two clocks after RESET# is sampled deasserted these signals begin normal operation.</p> <p>INIT# is an asynchronous input. In FRC mode, INIT# must be synchronous to BCLK.</p>
INTR	AG43	I, 3.3V	<p>The INTR signal is the interrupt request signal. It is the power-on default state of the LINT0 signal in the APIC group. The INTR input indicates that an external interrupt has been generated. The interrupt is maskable using the IF bit in the EFLAGS register. If the IF bit is set, the P6 processor vectors to the interrupt handler after the current instruction execution is completed. Upon recognizing the interrupt request, the P6 processor issues a single interrupt acknowledge (INTA) bus transaction. INTR must remain active until the INTA bus transaction to guarantee its recognition.</p> <p>INTR is sampled on every rising BCLK edge. INTR is an asynchronous input but recognition of INTR is guaranteed in a specific clock if it is asserted synchronously and meets the setup and hold times. INTR must also be deasserted for a minimum of two clocks to guarantee its inactive recognition. In FRC mode, INTR must be synchronous to BCLK.</p>

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
LINT[1:0]	AG41, AG43	I, 3.3V	<p>The LINT[1:0] signals are the execution control group local interrupt signals. When APIC is disabled, LINT0 signal defaults to the maskable interrupt request signal INTR and LINT1 to a non-maskable interrupt (NMI). INTR and NMI are backward compatible with the same signals in the Pentium processor. Both signals are asynchronous inputs. In FRC mode, LINT[1:0] must be synchronous to BCLK. LINT[1:0] signals need to be programmed when APIC is enabled.</p> <p>During active RESET#, P6 begins sampling the A20M# and IGNNE# values to determine the ratio of core-clock frequency to bus-clock frequency. After the PLL-lock time, the core clock is stabilized and locked to the external bus clock. On the active-to-inactive transition of RESET#, P6 latches A20M# and IGNNE#, and internally freezes the frequency ratio. Normal operation on the two signals continues two clocks after sampling RESET# inactive.</p> <p>LINT[1:0]# is used for core-to-bus frequency ratio extensions of future processors. Use the pins in the power-on configuration logic similar to the A20M# and IGNNE# pins.</p>
LOCK#	AA9	I/O, GTL+	<p>The LOCK# signal is the arbitration group bus lock signal. For a locked transaction sequence, LOCK# is asserted from the first transaction's request phase through the last transaction's response phase. A locked operation can be prematurely aborted (and LOCK# deasserted) if AERR# or DEFER# is asserted during the first bus transaction of the sequence. The sequence can also be prematurely aborted if a hard error (such as a hard failure response or AERR# assertion beyond the retry limit) occurs on any one of the transactions during the locked operation.</p> <p>When the priority agent asserts BPRI# to arbitrate for bus ownership, it waits until it observes LOCK# deasserted. This enables symmetric agents to retain bus ownership throughout the bus locked operation and guarantee the atomicity of lock. If AERR# is asserted up to the retry limit during an ongoing locked operation, the arbitration protocol ensures that the lock owner receives the bus ownership after arbitration logic is reset. This is accomplished by requiring the lock owner to reactivate its arbitration request one clock ahead of other agents' arbitration request. LOCK# is kept asserted throughout the arbitration reset sequence.</p>

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
NMI	AG41	I, 3.3V	<p>The NMI signal is the non-maskable interrupt signal. It is the default state of the LINT1 signal. Asserting NMI causes an interrupt with an internally supplied vector value of 2. An external interrupt-acknowledge transaction is not generated. If NMI is asserted during the execution of an NMI service routine, it remains pending and is recognized after the IREI is executed by the NMI service routine. At most, one assertion of NMI is held pending.</p> <p>NMI is rising-edge sensitive. Recognition of NMI is guaranteed in a specific clock if it is asserted synchronously and meets the setup and hold times. If asserted asynchronously, active and inactive pulse widths must be a minimum of two clocks. In FRC mode, NMI must be synchronous to BCLK.</p>
PICCLK	AA43	I, 5V	The PICCLK signal is the execution control group APIC Clock signal. It is an input clock to the P6 processor for synchronous operation of the APIC bus. PICCLK must be synchronous to BCLK in FR7 mode.
PICD[1:0]	AE21, AA41	I/O, 5V	The PICD[1:0] signals are the execution control group APIC Data signals. They are used for bidirectional serial message passing on the APIC bus.
PLL[2:1]	C23, C19	Others	Isolated analog decoupling is required for the internal phase lock loop (PLL). This should be equivalent to 0.1uF of ceramic capacitance across the PLL1 and PLLw pins.
PRDY#	Y39	O, GTL+	The PRDY# signal is the system support group probe ready signal. A P6 processor asserts PRDY to indicate that it has entered probe mode and that its test access port (TAP) is ready to accept a boundary scan or probe mode command.
PREQ#	AA45	I, 3.3V	The PREQ# signal is the system support group probe request signal. Asserting PREQ# stops normal P6 processor execution and places the P6 processor in probe mode, where it is capable of executing probe instructions. Probe mode is similar to ICE mode (in-circuit emulator mode) on other Intel processors.
PWRGOOD	AG7	I, 3.3V	PWRGOOD is a 3.3V tolerant input. This signal is a clean indication that clocks and the system 3.3V, 5V and V _{CCP} supplies are stable and within their specifications. PWRGOOD can be driven inactive at any time but power and clocks must be stable before the rising edge of PWRGOOD.

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description																																																												
REQ[4:0]#	W5, Y1, Y3, W7, W9	I/O, GTL+	<p>The REQ[4:0]# signals are request command signals. They are asserted by the current bus owner in both clocks of the request phase. In the first clock, the REQa[4:0]# signals define the transaction type to a level sufficient to begin a snoop request. In the second clock, REQb[4:0]# signals carry additional information to define the complete transaction type. REQb[4:2]# is reserved. REQb[1:0]# signals transmit LEN[1:0]# (the data transfer length information). In both clocks, REQ[4:0]# and ADS# are protected by parity RP#.</p> <p>All receiving agents observe the REQ[4:0]# signals to determine the transaction type and participate in the transaction as necessary, as shown in below:</p> <table border="1"> <thead> <tr> <th>Transaction</th> <th>REQa[4:0]#</th> <th>REQb[4:0]#</th> </tr> </thead> <tbody> <tr> <td>Deferred Reply</td> <td>00000</td> <td>XXXXX</td> </tr> <tr> <td>Rsvd (Ignore)</td> <td>00001</td> <td>XXXXX</td> </tr> <tr> <td>Interrupt</td> <td></td> <td></td> </tr> <tr> <td>Acknowledge</td> <td>01000</td> <td>DSZ[1:0]#,000</td> </tr> <tr> <td>Special Transactions</td> <td>01000</td> <td>DSZ[1:0]#,001</td> </tr> <tr> <td>Rsvd (Central agent response)</td> <td>01000</td> <td>DSZ[1:0]#,01X</td> </tr> <tr> <td>Rsvd (Central agent response)</td> <td>01000</td> <td>DSZ[1:0]#,1XX</td> </tr> <tr> <td>Branch Trace</td> <td></td> <td></td> </tr> <tr> <td>Message</td> <td>01001</td> <td>DSZ[1:0]#,000</td> </tr> <tr> <td>Rsvd (Central agent response)</td> <td>01001</td> <td>DSZ[1:0]#,001</td> </tr> <tr> <td>Rsvd (Central agent response)</td> <td>01001</td> <td>DSZ[1:0]#,01X</td> </tr> <tr> <td>Rsvd (Central agent response)</td> <td>01001</td> <td>DSZ[1:0]#,1XX</td> </tr> <tr> <td>I/O Read</td> <td>10000</td> <td>DSZ[1:0]#, rsvd, LEN[1:0]#</td> </tr> <tr> <td>I/O Write</td> <td>10001</td> <td>DSZ[1:0]#, rsvd, LEN[1:0]#</td> </tr> <tr> <td>Rsvd (Ignore)</td> <td>1100X</td> <td>DSZ[1:0]#,XXX</td> </tr> <tr> <td>Memory Read & Invalidate</td> <td>ASZ[1:0]#, 010</td> <td>DSZ[1:0]#, rsvd, LEN[1:0]#</td> </tr> <tr> <td>Rsvd (Memory Write)</td> <td>ASZ[1:0]#, 011</td> <td>DSZ[1:0]#, rsvd, LEN[1:0]#</td> </tr> <tr> <td>Memory Read</td> <td>ASZ[1:0]#, 1, D/C#, 0</td> <td>DSZ[1:0]#, rsvd, LEN[1:0]#</td> </tr> <tr> <td>Memory Write</td> <td>ASZ[1:0]#, 1, W/WB#, 0</td> <td>DSZ[1:0]#, rsvd, LEN[1:0]#</td> </tr> </tbody> </table>	Transaction	REQa[4:0]#	REQb[4:0]#	Deferred Reply	00000	XXXXX	Rsvd (Ignore)	00001	XXXXX	Interrupt			Acknowledge	01000	DSZ[1:0]#,000	Special Transactions	01000	DSZ[1:0]#,001	Rsvd (Central agent response)	01000	DSZ[1:0]#,01X	Rsvd (Central agent response)	01000	DSZ[1:0]#,1XX	Branch Trace			Message	01001	DSZ[1:0]#,000	Rsvd (Central agent response)	01001	DSZ[1:0]#,001	Rsvd (Central agent response)	01001	DSZ[1:0]#,01X	Rsvd (Central agent response)	01001	DSZ[1:0]#,1XX	I/O Read	10000	DSZ[1:0]#, rsvd, LEN[1:0]#	I/O Write	10001	DSZ[1:0]#, rsvd, LEN[1:0]#	Rsvd (Ignore)	1100X	DSZ[1:0]#,XXX	Memory Read & Invalidate	ASZ[1:0]#, 010	DSZ[1:0]#, rsvd, LEN[1:0]#	Rsvd (Memory Write)	ASZ[1:0]#, 011	DSZ[1:0]#, rsvd, LEN[1:0]#	Memory Read	ASZ[1:0]#, 1, D/C#, 0	DSZ[1:0]#, rsvd, LEN[1:0]#	Memory Write	ASZ[1:0]#, 1, W/WB#, 0	DSZ[1:0]#, rsvd, LEN[1:0]#
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RESET#	Y41	I, GTL+	<p>The RESET# signal is the execution control group reset signal. Asserting RESET# resets all P6 processors to known states and invalidates their L1 and L2 caches without writing back modified (M state) lines. RESET# must remain active for one microsecond for a "warm" reset. For a power-on type reset, RESET# must stay active for at least one millisecond after VCC and CLK have reached their proper DC and AC specifications. On observing active RESET#, all bus agents must deassert their outputs within two clocks.</p>																																																												

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description																																				
RESET# continued	Y41	I, GTL+	<p>A number of bus signals are sampled at the active-to-inactive transition of RESET# for the power-on configuration.</p> <p>Unless its outputs are tristated during power-on configuration, after active-to-inactive transition of RESET#, the P6 processor optionally executes its built-in self-test (BIST) and begins program execution at reset-vector 00_000F_FFF0H or 00_FFFF_FFF0H.</p>																																				
RP#	AC7	I/O, GTL+	<p>The RP# signal is the request parity signal. The request initiator drives it in both clocks of the request phase. RP# provides parity protection on ADS# and REQ[4:0]#. When a P6 bus agent observes an RP# parity error on any one of the two request phase clocks, it must assert AERR# in the error phase, provided "AERR# drive" is enabled during the power-on configuration. A correct parity signal is high if an even number of covered signals are low. It is low if an odd number of covered signals are low. Parity are high when all covered signals are high.</p>																																				
RS[2:0]#	AE7,AE5,AC9	I, GTL+	<p>The RS[2:0]# signals are the response status signals. They are driven by the response agent (the agent responsible for completion of the transaction at the top of the in-order queue). Assertion of RS[2:0]# to a non-zero value for one clock completes the response phase for a transaction. The response encodings are shown in below. Only certain response combinations are valid, based on the snoop result signaled during the transaction's snoop phase.</p> <table border="1"> <thead> <tr> <th>RS[2:0]#</th> <th>HITM#</th> <th>DEFER#</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>NA</td> <td>NA</td> <td>Idle state.</td> </tr> <tr> <td>001</td> <td>0</td> <td>0</td> <td>Retry Response. The transaction is canceled and must be retried by the initiator.</td> </tr> <tr> <td>010</td> <td>0</td> <td>1</td> <td>Defer Response. The transaction is suspended. The defer agent completes it with a defer reply</td> </tr> <tr> <td>011</td> <td>0</td> <td>1</td> <td>Reserved</td> </tr> <tr> <td>100</td> <td>X</td> <td>X</td> <td>Hard Failure. The transaction received a hard error. Exception handling is required.</td> </tr> <tr> <td>101</td> <td>0</td> <td>0</td> <td>Normal without data</td> </tr> <tr> <td>110</td> <td>1</td> <td>X</td> <td>Implicit write-back response. Snooping agent transfers the modified cache line on be data bus.</td> </tr> <tr> <td>111</td> <td>0</td> <td>0</td> <td>Normal with data.</td> </tr> </tbody> </table>	RS[2:0]#	HITM#	DEFER#	Description	000	NA	NA	Idle state.	001	0	0	Retry Response. The transaction is canceled and must be retried by the initiator.	010	0	1	Defer Response. The transaction is suspended. The defer agent completes it with a defer reply	011	0	1	Reserved	100	X	X	Hard Failure. The transaction received a hard error. Exception handling is required.	101	0	0	Normal without data	110	1	X	Implicit write-back response. Snooping agent transfers the modified cache line on be data bus.	111	0	0	Normal with data.
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Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
RS[2:0]# continued	AE7, AE5, AC9	I, GTL+	<p>The RS[2:0]# assertion for a transaction is initiated when all of the following conditions are met:</p> <ul style="list-style-type: none"> • All bus agents have observed the snoop phase completion of the transaction. • The transaction is at the top of in-order queue. • RS[2:0]# are sampled in the idle state <p>The response driven depends on the following transactions:</p> <ul style="list-style-type: none"> • The response agent returns a hard-failure response for any transaction in which the response agent observes a hard error. • The response agent returns a normal with data response for a read; transaction with HITM# and DEFER# deasserted in the snoop phase, when the addressed agent is ready to return data and samples inactive DBSY#. • The response agent returns a normal without data response for a write transaction with HITM# and DEFER# deasserted in the snoop phase, when the addressed agent samples TRDY# active and DBSY# inactive, and it is ready to complete the transaction. • The response agent must return an implicit write-back response in the next clock for a read transaction with HITM# asserted in the snoop phase, when the addressed agent samples TRDY# active and DBSY# inactive. <p>The addressed agent must return an implicit write-back response in the clock after the following sequence is sampled for a write transaction with HITM# asserted:</p> <ul style="list-style-type: none"> • TRDY# active and DBSY# inactive • followed by TRDY# inactive • followed by TRDY# active and DBSY# inactive <p>The defer agent can return a deferred, retry, or split response anytime for a read transaction with STM# deasserted and DEFER# asserted.</p> <p>The defer agent returns deferred, retry, or split response when it samples TRDY# active and DBSY# inactive for a write transaction with HITM# deasserted and DEFER# asserted.</p>

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
SMI#	W1	I, 3.3V	The SMI# is the response system management interrupt (SMI) signal. It is asserted by the response agent in the response phase. The addressed I/O agent asserts SMI# to signal a synchronous I/O restart SMI in response to an I/O transaction initiated by the processor to a powered-down I/O device. In observing an active RSMI# during the response phase, the P6 processor saves the current state and enters SMM mode. It issues an SMI acknowledge bus transaction then begins program execution from the SMM handler. It is not protected under parity and is an optional signal if the system does not support any synchronous I/O restart capability.
RSP#	U3	I, GTL+	The RSP# is the response parity signal. It is driven by the response agent during the assertion of RS[2:0]#. RSP# provides parity protection for RS[2:0]#. <p>A correct parity signal is high if an even number of covered signals are low. It is if an odd number of covered signals are low. During idle state of RS[2:0]# (RS[2:0]#=000), RSP# is also high since it is not driven by any agent guaranteeing correct parity.</p> <p>P6 bus agents check RSP# at all times and if a parity error is observed, treat it as a protocol violation error. If the BINIT# driver is enabled during configuration, the agent observing RSP# parity error asserts BTNIT#.</p>
STPCLK#	A3	I, 3.3V	The STPCLK# is the stop clock signal. When asserted, P6 enters a low power stop-clock state. The processor issues a stop clock acknowledge special transaction and stops sending internal clock signals to all units except the bus unit and the APIC unit. P6 continues to snoop bus transactions and service interrupts in the stop clock state. When STPCLK# is deasserted, P6 restarts its internal lock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock. STPCLK# is an asynchronous input. In FRC mode, STPCLK# must be synchronous to BCLK.
TCK	A5	I, JTAG	The TCK is the system support group test clock signal. TCK provides the clock input for the test bus (also known as the test access port). TCK must be connected to a clock to ensure initialization of the JTAG support.
TDI	A13	I, JTAG	The TDI is the system support group test-data-in signal. TDI transfers serial test data into the P6 processor. TDI provides the serial input needed for JTAG support.

Table 2-2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
TDO	C13	O, JTAG	The TDO is the system support group test-data-out signal. TDO transfers serial test data out from the P6 processor. TDO provides the serial output needed for JTAG support.
TESTHI	A23, A25, AE39	Other	TESTHI pins should be tied to V_{CCP} . A 10K pull-up resistor may be used.
TESTLO	C21, AS39, AS41, AS43, AS45, BA13, BA15, BA33, BA37, BC13, BC15, BC33, BC37	Other	TESTLO pins should be tied to V_{SS} . A 1K pull-down resistor may be used.
THERMTRIP#	A17	O, 3.3V	The P6 processor protects itself from catastrophic overheating through an internal thermal sensor. This sensor is set way above the normal operating temperature to ensure that there are no false trips. The P6 stops all executions when the junction temperature exceeds 135°C. This is signaled to the system by the THERMTRIP# pin. Once activated, the signal remains latched and P6 stopped, until RESET# goes active. There is no hysteresis built into the thermal sensor itself. As long as the temperature drops below the trip level, a RESET# pulse resets P6 and the execution continues. If the temperature has not dropped beyond the trip level, P6 continues to drive THERMTRIP# and remain in inactivity.
TMS	C15	I, JTAG	The TMS is an additional system support group JTAG-support signal.
TRDY#	Y9	I, GTL+	The TRDY# is the target ready signal. It is asserted by the target in the response phase to indicate that the target is ready to receive write or implicit write-back data transfer. This enables the request initiator or the snooping agent to begin the appropriate data transfer. There is no data transfer after a TRDY# assertion if a write has zero length in the request phase. The data transfer is optional if an implicit write-back occurs for a transaction that writes a full cache line (P6.0 DX performs the implicit write-back). For a write transaction, TRDY# is driven by the addressed agent when: <ul style="list-style-type: none"> the transaction has a write or write-back data transfer it has a free buffer available to receive the write data there is a minimum of 3 clocks after ADS# for the transaction the transaction reaches the top of the in-order queue there is a minimum of 1 clock after RS[2:0]# active assertion for transaction "n-1" (after the transaction reaches the top of in-order queue).
TRDY# continued	Y9	I, GTL+	For an implicit write-back, TRDY# is driven by the addressed agent when:

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
			<ul style="list-style-type: none"> transaction has an implicit write-back data transfer indicated in the Snoop Result Phase. it has a free cache line buffer to receive the cache line write-back if the transaction also has a request initiated transfer, that the request initiated TRDY# was asserted and then deasserted (EDY# must be deasserted for at least one clock between the TRDY# for the write and the TRDY# for the implicit write-back), a minimum of 1 clock after RS[2:0]# active assertion for transaction "n-1". (After the transaction reaches the top of in-order queue). <p>TRDY# for a write or an implicit write-back may be deasserted when:</p> <ul style="list-style-type: none"> inactive DBSY# and active TRDY# are observed DBSY# is observed inactive on the clock TRDY# is asserted. a minimum of 3 clocks are guaranteed between two TRDY# active-to-inactive transitions the response is driven on RS[2:0]# inactive DBSY# and active TRDY# are observed for a write, and TRDY# is required for an implicit write-back
TRST#	A7	I, JTAG	The TRST# is an additional system support group JTAG-support signal.
UP#	AG3	Other	The upgrade present signal is an open in the P6 processor and tied to V _{SS} in the OverDrive processor. This prevents the operation of voltage regulators that cause a potentially harmful voltage to the OverDrive processor. It also prevents a contention between onboard regulator and OverDrive processor VRM.
V _{CC5}		Power	V _{CC5} is used by the OverDrive processor for fan/heatsink power.
V _{CCP}	B4, B8, B16, B24, B32, B40, B44, F2, F6, F42, F46, K4, K44, P2, P6, P42, P46, T4, T44, X6, X42, AB4, AB44, AJ3, AJ7, AJ41, AJ45, AL1, AL5, AL39, AL43, AL47, AN3, AN7, AN41, AN45, AQ1, AQ5, AQ9, AQ39, AQ43, AQ47, BA17, BA21, BA25, BA29	Power	V _{CCP} the primary power supply.

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description																																				
V _{CCS}	AU1, AU5, AU9, AU39, AU43, AU47, AW3, AW7, AW41, AW45, AY1, AY3, AY5, AY7, AY9, AY39, AY41, AY43, AY45, AY47, BA3, BA7, BA41, BA45, BC19, BC23, BC27, BC31	Power	V _{CCS} is the secondary power supply used by some second level cache versions.																																				
VID[3:0]	AS1, AS3, AS5, AS7		<p>VID[3:0] are 4-voltage identification pins on the P6. These pins support automatic selection of power supply voltage. These pins are not signals but are either an open circuit in the processor or a short circuit to V_{SS}.</p> <p>The open and short circuits define the voltage required by P6. This has been added to cleanly support voltage specification variations on future P6 processors. The following are the voltage definition of these pins:</p> <table border="1"> <thead> <tr> <th>VID[3:0]</th> <th>Voltage Setting</th> <th>VID[3:0]</th> <th>Voltage Setting</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>3.5</td> <td>1000</td> <td>2.7</td> </tr> <tr> <td>0001</td> <td>3.4</td> <td>1001</td> <td>2.6</td> </tr> <tr> <td>0010</td> <td>3.3</td> <td>1010</td> <td>2.5</td> </tr> <tr> <td>0011</td> <td>3.2</td> <td>1011</td> <td>2.4</td> </tr> <tr> <td>0100</td> <td>3.1</td> <td>1100</td> <td>2.3</td> </tr> <tr> <td>0101</td> <td>3.0</td> <td>1101</td> <td>2.2</td> </tr> <tr> <td>0110</td> <td>2.9</td> <td>1110</td> <td>2.1</td> </tr> <tr> <td>0111</td> <td>2.8</td> <td>1111</td> <td>No CPU</td> </tr> </tbody> </table>	VID[3:0]	Voltage Setting	VID[3:0]	Voltage Setting	0000	3.5	1000	2.7	0001	3.4	1001	2.6	0010	3.3	1010	2.5	0011	3.2	1011	2.4	0100	3.1	1100	2.3	0101	3.0	1101	2.2	0110	2.9	1110	2.1	0111	2.8	1111	No CPU
VID[3:0]	Voltage Setting	VID[3:0]	Voltage Setting																																				
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0011	3.2	1011	2.4																																				
0100	3.1	1100	2.3																																				
0101	3.0	1101	2.2																																				
0110	2.9	1110	2.1																																				
0111	2.8	1111	No CPU																																				
V _{REF} [7:0]	AG45, U41, AE47, A47, Y7, S7, C7, A1	Power	V _{REF} [7:0] are the reference voltage pins for the GTL+ buffers.																																				

Table 2- 2 P6 Processor Signal Descriptions

Signal	Pin	Type	Description
V _{SS}	B6, B12, B20, B28, B36, B42, B46, F4, F8, F40, F44, K2, K6, K8, K40, K42, K46, P4, P8, P40, P44, T2, T6, T8, T40, T42, T46, X3, X4, X8, X40, X44, X46, AB2, AB6, AB8, AB40, AB42, AB46, AF2, AF4, AF6, AF8, AF40, AF42, AF44, AF46, AJ1, AJ5, AJ9, AJ39, AJ43, AJ47, AL3, AL7, AL41, AL45, AN1, AN5, AN9, AN39, AN43, AN47, AQ3, AQ7, AQ41, AQ45, AU3, AU7, AU41, AU45, AW1, AW5, AW9, AW39, AW43, AW47, BA1, BA5, BA9, BA19, BA23, BA27, BA31, BA39, BA43, BA47, BC1, BC3, BC5, BC7, BC9, BC17, BC21, BC25, BC29, BC39, BC41, BC43, BC45, BC47	Power	Ground

2.2 Memory Interface Component (S82451GX)

The Memory Interface Component (MIC) provides part of a high-performance, low-cost memory subsystem solution for P6.0 based systems by combining high-integration, high-performance technology with an architecture that is capable of low-latency response and high throughput.

The MIC can connect directly to a Memory Controller with no external glue components. A typical P6.0 system may be composed of one to four P6.0 processors and a PCI bridge. The system bus is designed to support eight physical loads at 66.67 MHz so it may need an additional bridge, memory controller, or other custom attachments. These may be connected to the system bus. Additional loads may be supported at a lower bus frequency.

The four Memory Interface Component are used to interface the Memory Controller data path with the Memory sub-system. Four MIC's handle one quad-word of data between the Memory Controller and Memory. Three basic types of memory system are supported: a 4 way interleaved DRAM system, a two-way interleaved DRAM system, and a one-way non-interleaved DRAM system.

A rich set of features are provided by the MIC to meet the requirements of "state-of-the-art" high-integration desktop and server systems. In addition to the memory configurations described above, the MIC handles data that includes ECC, two back-to-back cache line writes are supported for slow DIMMs, and 3V/5V DIMMs are supported. Some power management features are included that allow some I/O drivers to be put in standby when not in use.

2.2.1 Features

- Memory support
 - Support for 4-way interleaved conventional DRAM
 - Support for 2-way inlerleaved conventional DRAM
 - Support for 1-way non-interleaved conventional DRAM
 - Support for partial reads and partial writes
 - Support for part line read and writes
 - Any one of 4 interleaves can be populated
 - Read rate programmable
 - Volt and 5 Volt DIMMs are supported
 - Standard 36 bit DIMMs are supported
- Device features
 - 144-pin PQFP
 - 0.5 um, 3.3 V CMOS gate array
 - Maximum power dissipation of tbd (< 1.5 W)
 - On-chip PLL
 - JTAG support

2.2.2 S82451GX Pin Diagram

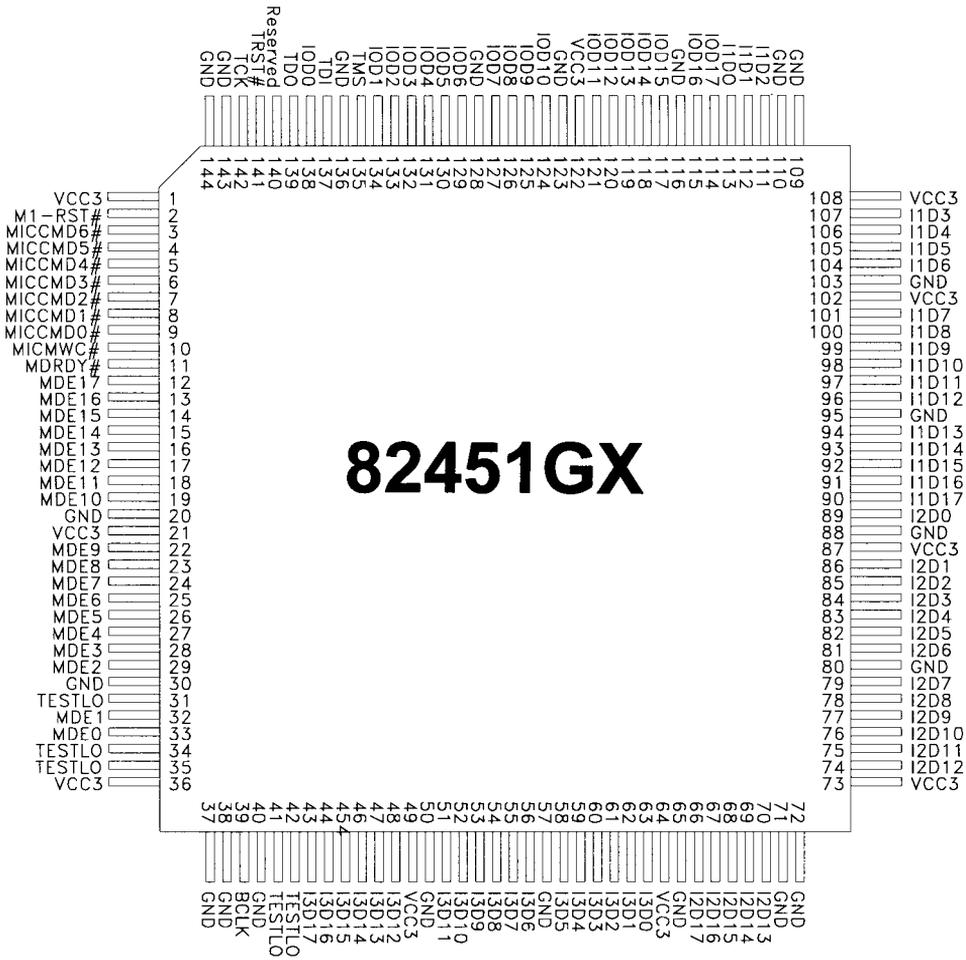


Figure 2- 4 S82451GX Pin Diagram

2.2.3 S82451GX Signal Descriptions

Table 2- 3 S82451GX Signal Descriptions

Signal	Pin	Type	Description
MIC Control Interface Signals			
MICCMD#[6:0]	03-09	I	MIC Command. Used to receive a command from the 82453GX to read data or write data, or to write MIC configuration data.
MICMWC#	10	I	MIC Write Command. Command from the 82453GX to write data held in the MIC to memory.
MIC Data Path Interface Signals			
MDE[17:10] MDE[09-02] MDE[01:00]	12-19 22-29 32-33	I/O	Memory Data and ECC. ECC is computer over 64-bit data words. MDE[17:0] is one fourth of a Quad-Word.
MD_RDY#	11	I	Memory Data Ready. Asserted when input data on the memory data bus is valid.
Memory Interface Signals			
I0_D[17:16] I0_D[15-11] I0_D[10-07] I0_D[06-01]	114,115 117-121 124-127 129-134	I/O	Memory Data ECC. ECC is computed over 64-bit data words. I0_D[17:0] is one fourth of a Quad-Word that is connected to interleave zero of the memory.
I1_D[17:13] I1_D[12-07] I1_D[06-03] I1_D[02-00]	90-94 96-101 104-107 111-113	I/O	Memory Data and ECC. ECC is computed over 64-bit data words. I1_D[17:0] is one fourth of a Quad-Word that is connected to interleave one of the memory.
I2_D[17:13] I2_D[12-07] I2_D[06-01] I2_D[00]	66-70 74-79 81-86 89	I/O	Memory Data and ECC. ECC is computed over 64-bit data words. I2_D[17:0] is one fourth of a Quad-Word that is connected to interleave two of the memory.
I3_D[17:12] I3_D[11-06] I3_D[05-00]	43-48 51-56 58-63	I/O	Memory Data and ECC. ECC is computed over 64-bit data words. I3_D[17:0] is one fourth of a Quad-Word that is connected to interleave three of the memory.
Clock Support Signals			
BCLK	39	I	PLL Reference Clock. This is the input to the device.
System Support Signals			
MI_RST#	2	I	System Reset Control.
Test Interface			
TCLK	142	I	JTAG Test Clock.
TDI	137	I	JTAG Test Data In.
TDO	139	O	JTAG Test Data Out.
TMS	135	I	JTAG Test Mode Select.
TRST#	141	I	JTAG Test Reset.

2.3 Data Path Chipset (S82452GX)

The S82452GX, together with S82453GX, provides a high-performance, low-cost memory subsystem solution for P6.0-based systems by combining high-integration, high-performance technology with an architecture that is capable of low-latency response and high throughput.

The S82452GX can connect directly to a P6.0 system bus with no external glue components. A typical P6.0 system may be composed of one to four P6.0 processors and a PCI bridge. The system bus is designed to support eight physical loads at 66.67 MHz so the system bus may need an additional bridge, memory controller, or other custom attachments. Additional loads may be supported at lower bus frequencies.

The S82452GX and S82453GX act as interface between the P6.0 bus and the system memory. The system supports three basic types of memory: a 4:1 interleaved DRAM system, a 2:1 interleaved DRAM system, and a non-interleaved DRAM system. The 4:1 interleaved DRAM system supports a maximum memory size of 4 MB using 64-Mbit technology. For the 2:1 interleaved and non-interleaved DRAM system, the maximum memory sizes are 2 GB and 1 Byte, respectively.

The S82452GX and S82453GX also have data integrity features that include ECC in the memory array, support for memory scrubbing, and parity (control) and ECC (data) on the system bus. These features, as well as a set of error reporting mechanisms, can be selected by configuring the S82452GX and S82453GX.

2.3.1 Features

- Processor support
 - Full support for the 64 bit P6.0 bus operating at 50.0 to 66.67 MHz (15ns).
 - ECC protection for the P6.0 data bus.
 - Parity protection for the P6.0 control bus.
 - Support for 36 bit addresses.
 - 8 or 1 deep in-order queue; 4 deep request queue.
 - Four cache line read buffer, 4 cache line write buffer.
 - Multiprocessor support (snarfing).
 - Support for third party defer of transactions.
 - GTL+ bus driver technology.
- Memory support
 - Support for up to 4 GB of 4-way interleaved conventional DRAM, per controller, using 64 Mbit technology DRAMs.
 - Support for 2-way interleaved and non-interleaved conventional DRAM.
 - Support for 4 Mbit, 16 Mbit, and 64 Mbit devices.
 - Supports permuting memory address bits to obtain alternate row selection bits.
 - Mixed memory sizes allowed (when address bit permuting is not used).
 - Staggered CAS-before-RAS Refresh

-
- Single error correction, double and nibble error detection.
 - Support for memory scrubbing.
 - Power management of the memory array.
 - Support for shadowing in the 640K to 1 MB address range.
 - Remapping of addresses above 1 MB to recover memory ranges mapped to other P6.0 devices.
 - Expandable to four memory controllers.
 - LVTTTL interface to memory interface components (MICs).
- Device features
 - Two packages: a 208 pin PQFP controller and a 240 pin PQFP or 256 pin BGA data path.
 - 0.5 um, 3.3 V CMOS gate array.
 - On-chip Digital PLL.
 - JTAG Boundary Scan support.

2.3.3 S82452GX Signal Descriptions

Table 2- 4 S82452GX Signal Descriptions

Signal	Pin	Type	Description
P6.0 Bus Interface			
D#[63:60] D#[59:56] D#[55:52] D#[51:48] D#[47:44] D#[43:40] D#[39:36] D#[35:32] D#[31:28] D#[27:24] D#[23:20] D#[19:16] D#[15:12] D#[11:08] D#[07:04] D#[03:00]	105, 109, 106, 99, 92, 108, 93, 102, 103, 95, 96, 86, 84, 98, 87, 89, 79, 90, 77, 76, 71, 82, 83, 70, 74, 64, 68, 73, 63, 67, 65, 58, 57, 54, 53, 56, 51, 50, 47, 48, 45, 44, 42, 37, 39, 38, 35, 34, 29, 26, 32, 23, 31, 28, 25, 22, 19, 16, 18, 13, 15, 10, 12, 09	I/O	Data.
DEP#[7:0]	227, 233, 235, 230, 237, 229, 232, 236	I/O	Data ECC/Parity. ECC computed over the 64 data bits. Parity is not generated or checked.
DRDY#	226	I/O	Data Ready. Asserted for each cycle that data is transferred.
Data Path Reset Signal			
MI-RST#	238	I	Reset. This signal is driven by MI_RST# signal from the S82452GX.
S82451GX Data Path Interface			
MDE[71:64] MDE[63:56] MDE[55:48] MDE[47:40] MDE[39:31] MDE[30:23] MDE[22:16] MDE[15:08] MDE[07:00]	198-191, 189-182, 178-171, 169-162, 59-151, 148-141, 138-132, 130-123, 119-112	I/O	Memory Data and ECC. ECC is computed over 64-bit data words. Parity is computed as byte-parity over a 64-bit word.
MDRDY0# MDRDY1#	111, 150	O	Memory Data Ready. Asserted when write data on the memory data bus is valid. Two copies are provided to support external loading.
S82453GX / S82452GX Interchip			
MEMCMD#[7:0]	213-206	I/O	Memory side command.
MEMERR#[1:0]	215,214	DP→DC	Indicates memory error conditions detected in the S82452GX.
SYSCMD#[4:0]	223, 222, 219, 218, 217	DC→DP	System side command.
SYSERR#	216	DP→DC	Indicates system error conditions detected in the S82452GX.
SYSDEN#	224	DC→DP	System side data enable.

Table 2- 4 S82452GX Signal Descriptions

Signal	Pin	Type	Description
Support Signals			
GTL_REFV	239	I	GTL Reference Voltage.
BCLK	204	I	PLL Reference Clock.
Test			
TCK	3	I	Test Clock.
TDI	6	I	Test Data In.
TDO	7	O	Test Data Out.
TMS	5	I	Test Mode Select.
TRST#	8	I	Test Reset. For normal operation, TRST# must be asserted low after PWR_GD is asserted.

2.4 DRAM Control Chipset (S82453GX)

2.4.1 S82453GX Pin Diagram

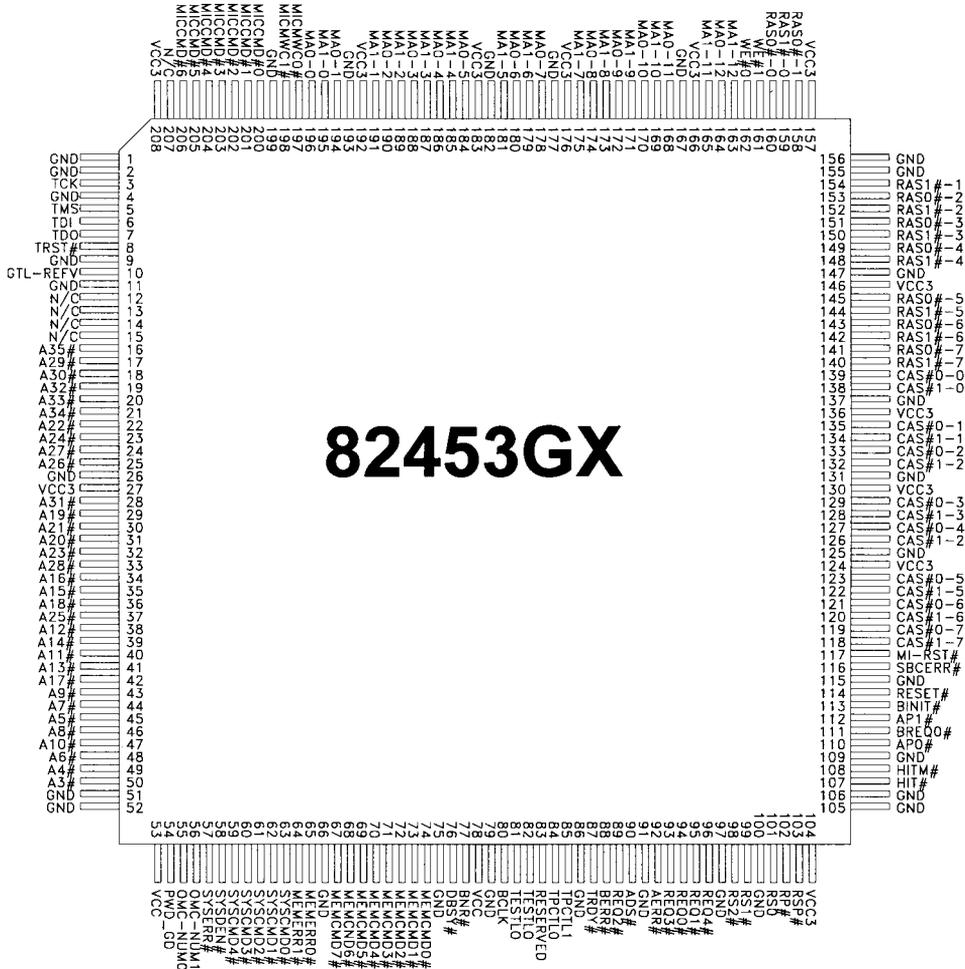


Figure 2- 6 S82453GX Pin Diagram

2.4.2 S82453GX Signal Descriptions

Table 2- 5 S82453GX Signal Descriptions

Signal	Pin	Type	Description
Bus Address/Control Interface			
ADS#	90	I	Address Strobe. Indicates that the current cycle is the first of two cycles of request.
REQ#[4:0]	96, 93, 89, 95, 94	I	Request. In the first cycle of a request these signals carry the request type. In the second, they carry the data size and transfer length.
RP#	102	I	Request Parity. Parity computed over ADS# and REQ#[3:0].
A#[35:32] A#[31:28] A#[27:24] A#[23:20] A#[19:16] A#[15:12] A#[11:08] A#[07:04] A#03	16, 21, 20, 19, 28, 18, 17, 33, 24, 25, 37, 23, 32, 22, 30, 31, 29, 36, 42, 34, 35, 39, 41, 38, 40, 47, 43, 46, 44, 48, 45, 49, 50	I	Address. Upper address bits issued with the current request.
AP#[1:0]	112, 110	I	Address Parity. Parity computed over the address, AP#[1] covers A#[35:24], and AP#[0] cover A#[23:3].
BREQ#[0]	111	O	Bus Request 0. Asserted at reset to set agent lds in all processors.
AERR#	92	I/O	Address Parity Check. Asserted when either an address or request parity error occurs.
BNR#	77	I/O	Block Next Request. Used to block the current request bus owner from issuing new requests.
HITM#	108	I/O	Hit Modified. Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HIT# to extend the snoop windows.
HIT#	107	I/O	Hit. Indicates that a caching agent holds a modified version of the requested line. Also, driven in conjunction with HiTM# to extend the snoop window.
TRDY#	87	I/O	Target Ready. Indicates a valid response cycle.
RS#[2:0]	98, 99, 101	I/O	Response. Indicates type of response.
RSP#	103	I/O	Response Parity. Parity computed over RS#.
DBSY#	76	I/O	Data Bus Busy. Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
Bus Address/Control Interface			
BERR#	88	I/O	Bus Error. Indicates an unrecoverable bus error.
BINIT#	113	I/O	Bus Initialization.
RESET#	114	I	Reset.

Table 2- 5 S82453GX Signal Descriptions

Signal	Pin	Type	Description
Memory Address/Control Interface			
MA0[12:10] MA0[09:07] MA0[06:04] MA0[03:00] MA1[12:10] MA1[09:07] MA1[06:04] MA1[03:00]	164, 168, 170, 172, 174, 178, 180, 184, 186, 188, 190, 194, 196, 163, 165, 169, 171, 173, 175, 179, 181, 185, 187, 189, 191, 195	O	Memory Address. Multiplexed row and column memory address. Two copies are provided to support external loading.
RAS0#[07:05] RAS0#[04:02] RAS0#[01:00] RAS1#[07:05] RAS1#[04:02] RAS1#[01:00]	141, 143, 145, 149, 151, 153, 158, 160, 140, 142, 144, 148, 150, 152, 154, 159	O	Row Address Strobe. Indicates that the address on MA[12:0] is the row address. There is one RAS# per logical row of memory. Two copies are provided to support external loading.
CAS0#[07:05] CAS0#[04:02] CAS0#[01:00] CAS1#[07:05] CAS1#[04:02] CAS1#[01:00]	119, 121, 123, 127, 129, 133, 135, 139, 118, 120, 122, 126, 128, 132, 134, 138	O	Column Address Strobe. Indicates that the address on MA[12:0] is the column address. There is one CAS# per logical row of memory. Two copies are provided to support external loading.
WE0#, WE1#	162, 161	O	Write Enable. Indicates that the current memory request is a write. Two copies are provided to support external loading.
S82451GX Control Interface			
MICCMD#[6:0]	206-200	O	MIC Command. Used to send a command to the S82451GX to read or write data, or to write configuration data.
MICMWC0# MICMWC1#	197, 198	O	Memory Write Command. Used to command the S82451GX to write data held in its internal buffers to memory. Two copies are provided to support external loading.
S82453GX Memory Reset and Error			
SBCERR#	116	O	Single Bit Corrected Memory Error. Indicates that a single bit error was detected and corrected in the memory array.
MI_RST#	117	O	Memory Interface Reset. Used to reset the S82452GX and the S82451GX.
S82453GX Controller Number			
OMC_NUM[1:0]	56, 55	I	Memory Controller Number.
S82453GX Third Party Control			
TPCTL[1:0]	85, 84	I	Third party control inputs.
Support Signals			
PWR_GD	54	I	Power good.

2.5 PCI Bridge (S82454GX)

The S82454GX PCI Bridge provides a high-performance, low-cost I/O subsystem solution for P6.0 based systems by combining high integration, high-performance technology with an architecture that is capable of low latency response and high throughput.

The goal of the S82454GX is to bring PCI performance to the P6.0 market while meeting the P6.0 product goals of ease of system design with resultant reduction in time to market and reduced cost of system integration. Chipset features and performance issues were evaluated with the above goal in mind.

The S82454GX is a single-chip PCI bridge that can connect directly to a P6.0 system bus with no external glue components. The system bus is designed to support eight physical loads at 66.66 MHz, so an additional bridge, memory controller, or other custom attachment may be connected to the system bus. Additional loads can be supported at lower bus frequencies.

The PCI bridge takes advantage of the P6.0 ratio clocking scheme in order to assure modularity now and upgradability in the future. The bridge has a synchronous interface to the P6.0 bus and supports either a free-running or a derived clock for the synchronous PCI interface. In derived clock mode the 82454GX derives either a 25.0 or 33.33 MHz PCI clock output from the P6.0 bus clock. No internal synchronizers are needed in this mode. In free-running clock mode the PCI clock is an input and the 82454GX uses internal synchronizers to support any legal PCI bus clock speed.

Support for multiple I/O bridges provides a modular approach to I/O performance improvements by adding additional I/O bridges or other high-priority bus agents. Compatibility versus speed issues are addressed with an optional compatibility operating mode in order to guarantee standard bus compatible operation when needed, but allow bus concurrency when possible.

2.5.1 Features

Processor support

- Synchronous P6.0 bus interface supports either 50.0 Hz or 66.66 MHz P6.0 bus speeds.
- Full support for the P6.0 bus protocol.
- Parity protection on P6.0 control signals.
- ECC protection on P6.0 data signals.
- Up to eight deep In-Order Queue; IOQ = 1, four deep outbound request queue (holds P6.0 initiated requests directed to the PCI bus).
- Non-caching bridge.
- Multiprocessor support
- GTL+ bus driver technology.
- Gated GTL+ Receivers for reduced power.
- 36-bit address decode. 36-bit address drive.

PCI Support

- Synchronous PCI interface supports either a free-running or a P6.0 clock derived PCI clock.
- Derived clock mode provides a 66.66 MHz (15 ns) P6.0 to 33.33 MHz (30 ns) PCI or a 50.0 MHz (20 ns) P6.0 to 25.0 MHz (40 ns) PCI interface that requires no internal synchronizers.
- 32 bit Address/Data PCI bus (64 bit dual cycle address support) using TTL bus driver technology.
- Parity protection on all PCI bus signals.
- Full support for the PCI Configuration Space Enable (CSE) protocol.
- Four deep inbound request queue (holds PCI initiated requests directed to the P6.0 bus).
- Four cache line size outbound data buffers (holds data going to PCI - from P6.0 writes or PCI reads). Four cache line size inbound data buffers (holds data going to P6.0 - from PCI writes or P6.0 reads).
- Data collection / write assembly of line bursts.
- Support for multiple I/O bridges through either internal or external I/O bridge arbitration. The internal arbitration unit can support up to two I/O bridges.

Device features

- Single chip: combined controller and data path.
- 0.5 um, 3.3 V CMOS gate array.
- GTL+ P6.0 bus interface
- PCI bus interface uses 5V tolerant PCI drivers.
- Maximum power dissipation of 2.4 Watts.
- On-chip digital PLL (DPLL).
- Component and in-system connectivity test support (JTAG).

2.5.2 S82454GX Block Diagram

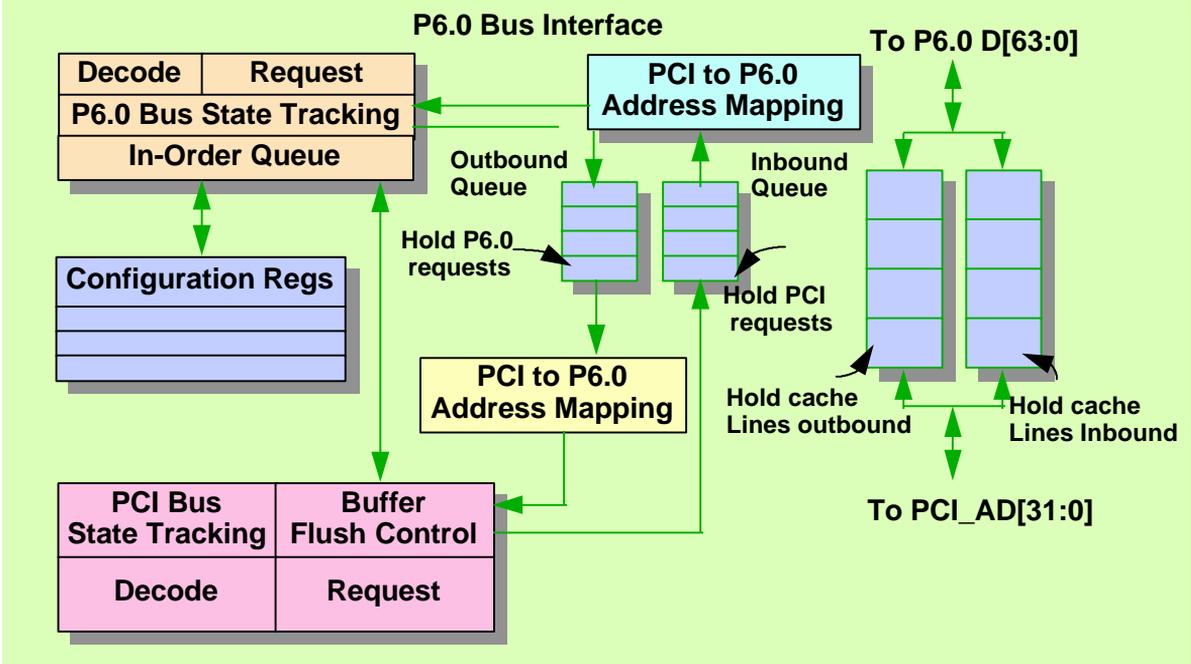


Figure 2- 7 S82454GX Block Diagram

2.5.3 S82454GX Pin Diagram

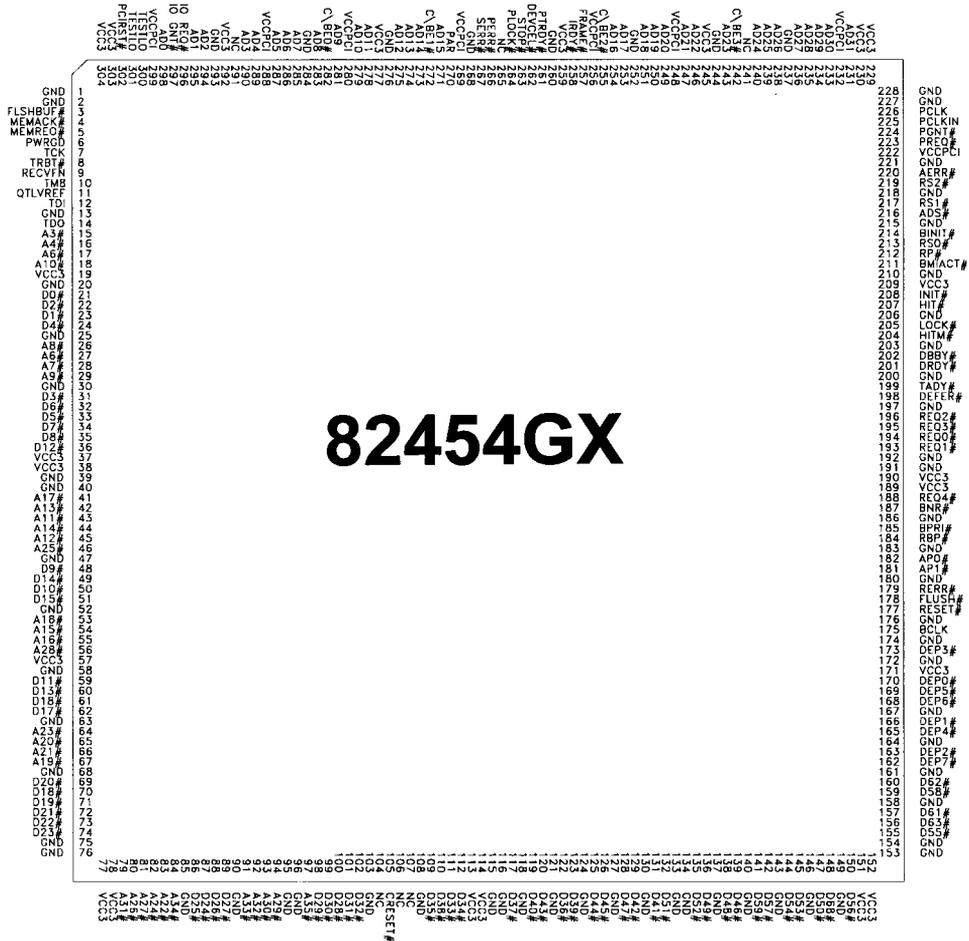


Figure 2-8 S82454GX Pin Diagram

2.5.4 S82454GX Signal Descriptions

Table 2- 6 S82454GX Signal Descriptions

Signal	Pin	Type	Description
P6 System Bus Interface Signals			
BPRI#	185	I/O, GTL+	Address Strobe.
ADS#	216	I/O, GTL+	Priority Agent Bus Request
A#[35:32] A#[31:28] A#[27:24] A#[23:20] A#[19:16] A#[15:12] A#[11:8] A#[7:4], A#[3]	97, 84, 91, 92, 79, 93, 94, 56, 81, 80, 46, 82, 64, 83, 66, 65, 67, 53, 41, 55, 54, 44, 42, 45, 43, 18, 29, 26, 28, 17, 7, 16, 15	I/O, GTL+	Request Address on cycle where ADS# is asserted. Alternate functions on second cycle.
REQ[4:2]# REQ[1:0]#	188,195,196, 193,194	I/O, GTL+	Command and address space when ADS# is valid Data size and length on second cycle.
LOCK#	205	I/O, GTL#	Bus Lock.
RP#	212	I/O, GTL+	Request Parity
AP#[1:0]	181, 182	I/O, GTL+	Address Parity
AERR#	220	I/O, GTL+	Address Error
BNR#	187	I/O, GTL+	Block Next Request
HIT#	207	I/O, GTL+	Cache Hit
HITM#	204	I/O, GTL+	Hit Modified
DEFER#	198	I/O, GTL+	Defer
TRDY#	199	I/O, GTL+	Target Ready
DRDY#	201	I/O, GTL+	Data Ready
DBSY#	202	I/O, GTL+	Data Bus Busy
RS[2:0]	219, 217, 213	I/O, GTL+	Response Status
RSP#	184	I/O, GTL+	Response Parity
D#[63:61] D#[60:58] D#[57:55] D#[54:52] D#[51:49] D#[48:46] D#[45:43] D#[42:40] D#[39:37] D#[36:34] D#[33:31] D#[30:27] D#[26:23] D#[22:19] D#[18:15] D#[14:11] D#[10:7] D#[6:3], D#[2:0]	156, 160, 157, 148, 155, 141, 159, 42, 150, 144, 145, 135, 132, 147, 136, 138, 128, 139, 126, 125, 120, 129, 131, 119, 123, 110, 117, 122, 109, 112, 111, 102, 101, 99, 98, 100, 89, 88, 86, 87, 74, 73, 72, 69, 71, 70, 62, 61, 51, 49, 60, 36, 59, 50, 48, 35, 34, 32, 33, 24, 31, 22, 23, 21	I/O	Data

Table 2- 6 S82454GX Signal Descriptions

Signal	Pin	Type	Description
P6 System Bus Interface Signals			
DEP#[7:5] DEP#[4:2] DEP#[1:0]	162, 168, 169, 165, 173, 163, 166, 170	I/O	Data Even Parity
CLK	175	I, CMOS	P6 System Bus Clock
RESET#	177	I/O, GTL+	P6 System Reset
CRESET#	105	I/O, CMOS	CMOS System Reset
INIT#	208	O, GTL+	Initialize (soft reset)
BINIT#	214	I/O, GTL+	Bus Initialize
BERR#	179	I/O, GTL+	Bus Error
FLUSH#	178	O, CMOS	Write back modified lines and disable further caching.
SMIACT#	211	O, CMOS	SMI Active
PCI Bus Interface Signals			
AD[31:29] AD[28:26] AD[25:23] AD[22:20] AD[19:17] AD[16:14] AD[13:11] AD[10:8] AD[7:5] AD[4:2] AD[1:0]	231, 233, 234, 235, 236, 238, 239, 240, 243, 246, 247, 249, 250, 251, 253, 254, 271, 273, 274, 275, 278, 279, 281, 283, 285, 286, 287, 289, 290, 294, 295, 298	I/O, PCI	Address and Data signals
C/BE[2:0]#	255, 272, 282	I/O, PCI	Command/Byte Enable
PCLK	226	I/O, CMOS	PCI Clock Mode Detect/Derived clock Out
PCLKIN	225	I, CMOS	PCI Bus Clock Input.
P_TRDY#	261	I/O, PCI	Target Ready.
STOP#	263	I/O, PCI	Stop
P_LOCK#	264	I/O, PCI	Lock
DEVSEL#	262	I/O, PCI	Device Select
PAR	270	I/O, PCI	Parity
IRDY#	258	I/O, PCI	Initiator Ready
FRAME#	257	I/O, PCI	Frame
PERR#	266	I/O, PCI	Parity Error
SERR#	267	I/O, PCI	System Error
P_REQ#	223	O, CMOS	Request
P_GNT#	224	I, CMOS	Grant
Standard Bus Bridge Interface Signals			
FLSBF#	3	I, CMOS	Flush Buffers outbound buffers.
MEMACK#	4	O, CMOS	Memory Acknowledge

Table 2- 6 S82454GX Signal Descriptions

Signal	Pin	Type	Description
MEMREQ#	5	I, CMOS	Memory Request
Multi- Bridge Sideband Signals			
IO_GNT# (BDEVNUM[1])	297	I, CMOS	I/O Grant (provides Device Number - DEVNUM[1] during reset).
IO_REQ# (BDEVNUM[0])	296	O, CMOS	I/O Request (provides Device Number - DEVNUM[0] during reset).
Support Signals			
GTL_REFV	11	I, Analog	GTL+ Reference Voltage.
PLL_TMD1	300		PLL Test input 1. (Must be grounded)
PLL_TMD0	301		PLL Test input 0. (Must be grounded)
PWR_GD	6	I, CMOS	Power Good
PCIRST#	302	O, CMOS	PCIRReset
RECV_EN	9	I, CMOS	Enable GTLs receivers.
JTAG Test Signals			
TMS	10	I, CMOS	Test Mode Select
TDI	12	I, CMOS	Test Data In
TDO	14	O, CMOS	Test Data Out.
TCK	7	I, CMOS	Test Clock.
TRST#	8	I, CMOS	Test Reset.
Power and Miscellaneous Signals			
GND	1, 2, 13, 20, 25, 30, 39, 40, 47, 52, 58, 63, 68, 75, 76, 85, 90, 95, 96, 103, 108, 115, 116, 118, 121, 124, 127, 133, 130, 134, 137, 140, 143, 146, 149, 153, 154, 158, 161, 164, 167, 172, 174, 176, 180, 183, 186, 191, 192, 197, 200, 203, 206, 210, 215, 218, 221, 227, 228, 237, 224, 252, 260, 268, 276, 284, 93		
VCC3	19, 37, 38, 57, 77, 78, 113, 114, 151, 152, 171, 189, 190, 209, 229, 230, 259, 277, 292, 303, 304		
VCC_PCI	232, 248, 256, 269, 280, 288, 299		
N.C.	104, 106, 107, 241, 265, 291		

2.6 SIO (82379AB)

The 82379AB also integrates many of the common I/O functions found in today's ISA-based PC systems. The 82379AB incorporates the logic for a PCI interface (master and slave), ISA interface (master and slave), enhanced seven channel DMA controller that supports data buffers to isolate the PCI bus from the ISA bus and to enhance performance, PCI and ISA arbitration, 14 level interrupt controller, a 16-bit BIOS timer, three programmable timer/counters, and non-maskable interrupt (NMI) control logic. The 82379AB also provides decode for peripheral devices such as the Flash BIOS, real-time clock, keyboard/mouse controller, diskette drive controller, two serial ports, one parallel port, and IDE hard disk drive. The 82379AB supports several advanced power management features such as SMI# Interrupt. The 82379AB also supports a total of six PCI masters, and up to four PCI interrupts. The 82379AB incorporates an advanced programmable interrupt controller (APIC) that communicates with the processor via a dedicated two data bit bus.

2.6.1 Features

- Provides the Bridge Between the PCI Bus and ISA Bus.
- 100% PCI and ISA Compatible
 - PCI and ISA Master/Slave Interface
 - Directly Drives 10 PCI Loads and 6 ISA Slots
 - Supports PCI at 25 MHz and 33 MHz
 - Supports ISA from 6 MHz to 8.33 MHz
- Enhanced DMA Functions
 - Compatible DMA Transfers
 - 27-bit addressing
 - Seven Independently Programmable Channels
 - Functionality of Two 82C37A DMA controllers
- Integrated Data Buffers to Improve Performance
 - 8-byte DMA/ISA Master Line Buffer
 - 32-bit Posted Memory Write Buffer to ISA
- Integrated 16-bit BIOS Timer
- Non-Maskable Interrupts(NMI)
 - PCI System Errors
 - ISA Parity Errors
- Four Dedicated PCI Interrupts
 - Level Sensitive
 - Can be Mapped to Any Unused Interrupt

-
- Arbitration for PCI Devices
 - Four PCI Masters are Supported
 - Fixed, Rotating, or a Combination of the Two
 - Arbitration for ISA Devices
 - ISA Masters
 - DMA and Refresh
 - Utility Bus (X-Bus) Peripheral Support
 - Provides Chip Select Decode
 - Controls Lower X-Bus Data Byte Transceiver
 - Integrates Port 92, Mouse Interrupt, Coprocessor Error Reporting
 - Integrates the Functionality of one 82C54 Timer
 - System Timer
 - Refresh Request
 - Speaker Tone Output
 - Integrates the Functionality of two 82C59 Interrupt Controllers
 - 14 Interrupts Supported
 - Edge/Level Selectable Interrupts: Each Interrupt Individually Programmable
 - Complete Support for SL Enhanced Intel486™ CPU's
 - SMI# Generation Based on System Hardware Events
 - STPCLK# Generation to Power Down the CPU
 - Integrated I/O Advanced
 - Programmable Interrupt Controller (APIC)

2.6.2 82379AB Block Diagram

82379AB : SIO

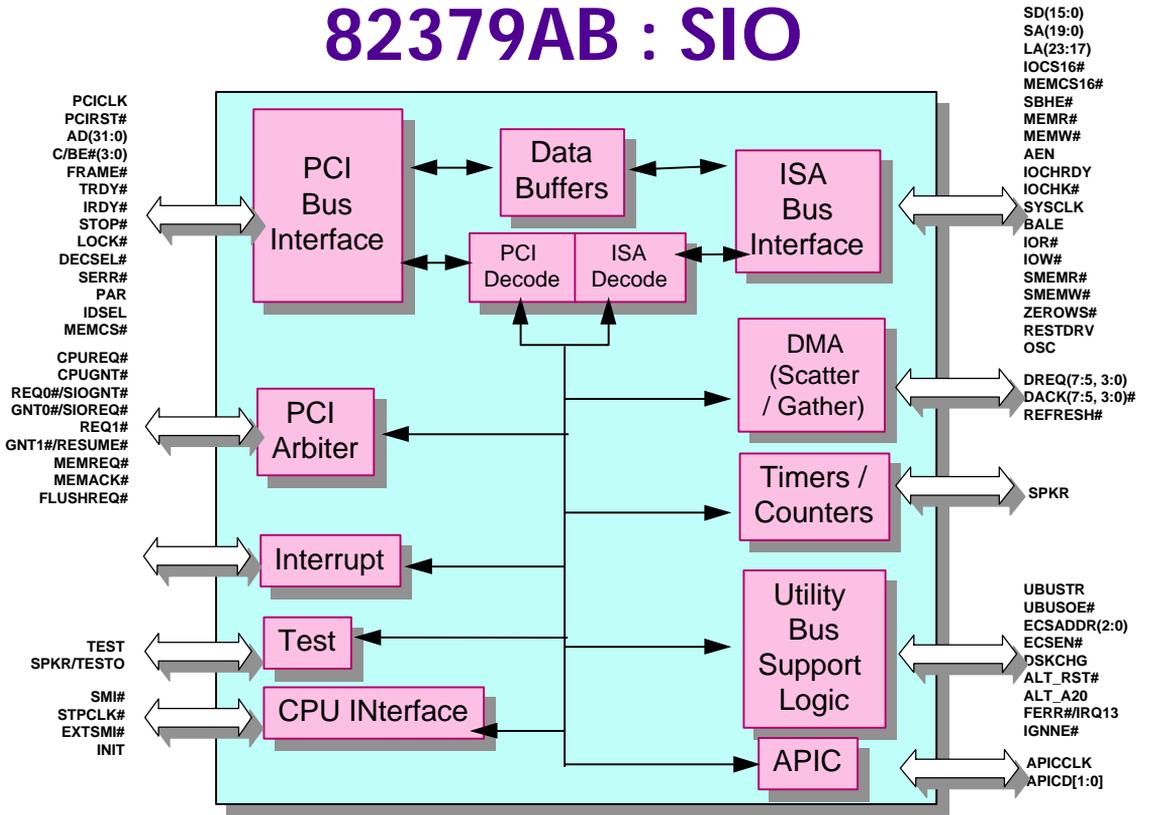


Figure 2- 9 82379AB Block Diagram

2.6.3 82379AB Pin Diagram

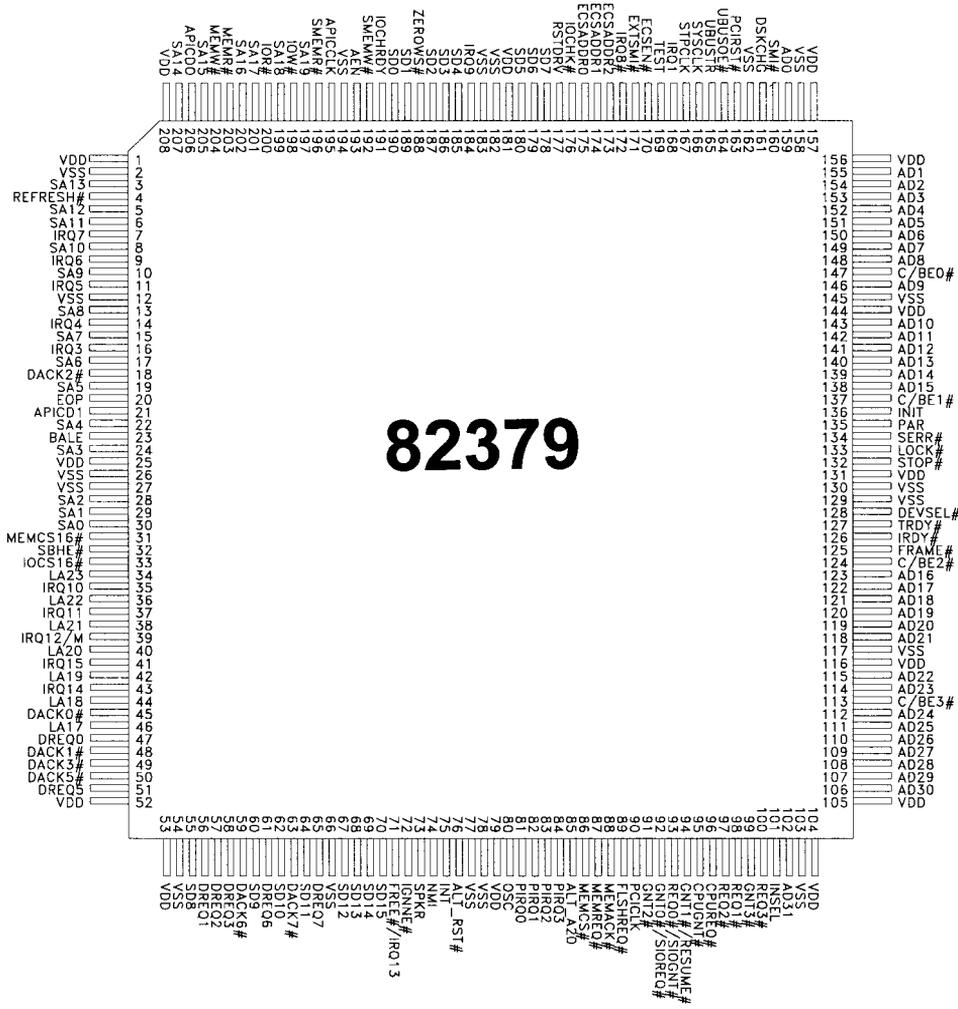


Figure 2- 10 82379AB Pin Diagram

2.6.4 82379AB Signal Descriptions

Table 2- 7 82379AB Signal Descriptions

Signal	Pin	Type	Description
PCI Bus Interface			
PCICLK	90	I	PCI Clock: PCICLK provides timing for all transactions on the PCI Bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge.
PCIRST#	163	I	PCI Reset: PCIRST# forces the SIO to a known state. AD[31:0], C/BE[3:0]#, and PAR are always driven low by the SIO synchronously from the leading edge of PCIRST#. The SIO always tristates these signals from the trailing edge of PCIRST#. If the internal arbiter is enabled (CPUREQ# sampled high on the trailing edge of PCIRST#), the SIO drives these signals low again (synchronously 2-5 PCICLKs later) until the bus is given to another master. If the internal arbiter is disabled (CPUREQ# sampled low on the trailing edge of PCIRST#), these signals remain tristated until the SIO is required to drive them valid as a master or slave.
AD[31:0]	102,106-112, 114, 115, 118-123, 138-143, 146, 148-155, 159	I/O	PCI Address / Data: AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contains a physical byte address (32 bits). During subsequent clocks, AD[31:0] contains data.
C/BE[3:0]#	113, 124, 137, 147	I/O	Bus Command and Byte Enables: The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase, C/BE[3:0]# are used as Byte Enables. The Byte Enables determine which byte lanes carry meaningful data.
FRAME#	125	I/O s/t/s	Cycle Frame: FRAME# is driven by the current master to indicate the beginning and duration of an access.
TRDY#	127	I/O s/t/s	Target Ready: TRDY# indicates the SIO's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#.
IRDY#	126	I/O s/t/s	Initiator Ready: IRDY# indicates the SIO's ability, as an initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#.

Table 2- 7 82379AB Signal Descriptions

Signal	Pin	Type	Description
PCI Bus Interface			
STOP#	132	I/O s/t/s	Stop: STOP# indicates that the SIO, as a target, is requesting a master to stop the current transaction. As a master, STOP# causes the SIO to stop the current transaction. STOP# is an output when the SIO is a target and an input when the SIO is an initiator.
LOCK#	133	I	Lock: LOCK# indicates an atomic operation that may require multiple transactions to complete. When other masters attempt accesses while the SIO is locked, the SIO responds with a retry termination.
IDSEL	101	I	Initialization Device Select: IDSEL is used as a chip select during configuration read and write transactions.
DEVSEL	128	I/O s/t/s	Device Select: The SIO asserts DEVSEL# to claim a PCI transaction through positive or subtractive decoding.
PAR	135	O	Calculated Parity Signal: PAR is "even" parity and is calculated on 36 bits - AD[31:0] plus C/BE[3:0]#.
SERR#	134	I	System Error: SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the SIO generates a non-maskable interrupt (NMI) to the CPU.
PCI Arbiter Interface			
CPUREQ#	96	I	CPU Request: This signal provides the following functions: <ol style="list-style-type: none"> 1) If CPUREQ# is sampled high on the trailing edge of PCIRST#, the internal arbiter is enabled. If CPUREQ# is sampled low on the trailing edge of PCIRST#, the internal arbiter is disabled. 2) If the SIO's internal arbiter is enabled, this pin is configured as CPUREQ#. An active low assertion indicates that the CPU initiator wants to use the PCI Bus. If the internal arbiter is disabled, this pin is meaningless after reset.
REQ0# / SIOGNT#	93	I	Request 0 / SIO Grant: If the SIO's internal arbiter is enabled, this pin is configured as REQ0#. An active low assertion indicates that initiator desires the use of the PCI Bus. If the internal arbiter is disabled, this pin is configured as SIOGNT#. When asserted, SIOGNT# indicates that the external PCI arbiter has granted use of the bus to the SIO.

Table 2- 7 82379AB Signal Descriptions

Signal	Pin	Type	Description
PCI Arbiter Interface			
REQ[3:1]#	100, 97, 98	I	Request [3:1]: If the SIO's internal arbiter is enabled through the Arbiter Configuration Register, then this signal is configured as REQ1#. An active low assertion indicates that Initiator desires the use of the PCI Bus. If the internal arbiter is disabled, the SIO ignores REQ1# after reset.
CPUGNT#	95	t/s/o	CPU Grant: If the SIO's internal arbiter is enabled, this pin is configured as CPUGNT#. The SIO's internal arbiter asserts CPUGNT# to indicate that the CPU initiator has been granted the PCI Bus. If the internal arbiter is disabled, this signal is meaningless.
GNT0# / SIOREQ#	92	t/s/o	Grant 0 / SIO Request: If the SIO's internal arbiter is enabled, this pin is configured as GNT0#. The SIO's internal arbiter asserts GNT0# to indicate that Initiator0 has been granted the PCI Bus. If the internal arbiter is disabled, this pin is configured as SIOREQ#. The SIO asserts SIOREQ# to request the PCI Bus.
GNT[3:1]# / RESUME#	99, 91, 94	t/s/o	Grant [3:1] / Resume: If the SIO's internal arbiter is enabled, this pin is configured as GNT#. The SIO's internal arbiter asserts GNT# to indicate that Initiator has been granted the PCI Bus. If the internal arbiter is disabled, this pin is configured as RESUME#. The SIO asserts RESUME# to indicate that the conditions causing the SIO to retry the cycle has passed.
MEMREQ#	87	t/s/o	Memory Request: If the SIO is configured in Guaranteed Access Time (GAT) Mode, MEMREQ# will be asserted when an ISA master or DMA is requesting the ISA Bus (along w/ FLSHREQ#) to indicate that SIO requires ownership of main memory. If this pin is asserted alone (FLSHREQ# not asserted), with either GAT (Guaranteed Access Time) mode being enabled or disabled, it indicates that buffers pointing to the main memory must be flushed and temporary disabled for the duration of assertion. This is used to control buffer coherency in the systems which use APIC as a system interrupt controller.
FLSHREQ#	89	t/s/o	Flush Request: FLSHREQ# is generated by the SIO to command all of the system's posted write buffers pointing towards the PCI Bus to be flushed. This is required before granting the ISA Bus to an ISA master or the DMA. For the APIC related buffer flush

Table 2- 7 82379AB Signal Descriptions

Signal	Pin	Type	Description
			requests this pin is deasserted.
PCI Arbiter Interface			
MEMACK#	88	I	Memory Acknowledge: MEMACK# is the response handshake that indicates to the SIO that the function requested over the MEMREQ# and/or FLSHREQ# signals has been completed. If this pin is asserted in response to assertion of MEMREQ# (with GAT mode being either enabled or disabled) it indicates that buffers pointing towards main-memory are flushed and temporary disabled so that APIC can proceed with interrupt message sequence.
ISA Interface			
AEN	193	O	Address Enable: AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMA cycles as valid I/O cycles.
BALE	23	O	Bus Address Latch Enable: BALE is an active high signal asserted by the SIO to indicate that the address (SA[19:0], LA[23:17]), AEN and SBHE# signal lines are valid.
SYSCLK	166	O	System Clock: SYSCLK is an output of the SIO component. The frequencies supported are 6 to 8.33 MHz.
IOCHRDY	191	I/O	I/O Channel Ready: Resources on the ISA Bus assert IOCHRDY to indicate that additional time (wait state) is required to complete the cycle.
Address Decoder			
MEMCS#	86	O	Memory Chip Select: MEMCS# is a programmable address decode signal provided to a Host CPU bridge. A CPU bridge can use MEMCS# to forward a PCI cycle to main memory behind the bridge.
IOCS16#	33	I	16-Bit I/O Chip Select: This signal is driven by I/O devices on the ISA Bus to indicate that they support 16-bit I/O bus cycles.
IOCHK#	176	I	I/O Channel Check: IOCHK# can be driven by any resource on the ISA Bus. When asserted, it indicates that a parity or an uncorrectable error has occurred for a device or memory on the ISA Bus.
IOR#	200	I/O	I/O Read: IOR# is the command to an ISA I/O slave device that the slave may drive data onto the ISA data bus (SD[15:0]).
IOW#	198	I/O	I/O Write IOW# is the command to an ISA I/O slave device that the slave may latch data

Table 2- 7 82379AB Signal Descriptions

Signal	Pin	Type	Description
			from the ISA data bus (SD[15:0]).
Address Decoder			
LA[23:17]	34, 36, 38, 40, 42, 44, 46	I/O	Unlatched Address: The LA[23:17] address lines are bidirectional. These address lines allow accesses to physical memory on the ISA Bus up to 16 MB.
SA[19:0]	197, 199, 201-202, 205, 207, 3, 5, 6, 8, 10, 13, 15, 17, 19, 22, 2428, 29, 30	I/O	System Address Bus: These bidirectional address lines define the selection with the granularity of one byte within the one MB section of memory.
SBHE#	32	I/O	System Byte High Enable: SBHE# indicates, when asserted, that a byte is being transferred on the upper byte (SD[15:8]) of the data bus.
MEMCS16#	31	OD	Memory Chip Select 16: MEMCS16# is a decode of LA[23:17] without any qualification of the command signal lines.
MEMR#	203	I/O	Memory Read: MEMR# is the command to a memory slave that it may drive data onto the ISA data bus.
MEMW#	204	I/O	Memory Write: MEMW# is the command to a memory slave that it may latch data from the ISA data bus.
SMEMW#	192	O	System Memory Write: The SIO asserts SMEMW# to request a memory slave to accept data from the data lines.
SMEMR#	196	O	System Memory Read: The SIO asserts SMEMR# to request a memory slave to accept data from the data lines.
ZEROWS#	188	I	Zero Wait States: An ISA slave asserts ZEROWS# after its address and command signals have been decoded to indicate that the current cycle can be shortened.
OSC	80	I	Oscillator: OSC is the 14.3818 MHz ISA clock signal. It is used by the internal 8254 Timer, counters 0, 1, and 2.
RSTDRV	177	O	Reset Drive: The SIO asserts RSTDRV to reset devices that reside on the ISA Bus.
SD[15:0]	70-67, 64, 62, 60, 55, 178-180, 185-187, 189-190	I/O	System Data: SD[15:0] provide the 16-bit data path for devices residing on the ISA Bus.
DMA			
DREQ [3:0, 7:5]	65, 61, 51, 58-56, 47	I	DMA Request: The DREQ lines are used to request DMA service from the SIO's DMA controller or for a 16-bit master to gain control of the ISA expansion bus.
DACK# [3:0, 7:5]	49, 18, 48, 45, 63, 59, 50	I	DMA Acknowledge: The DACK output lines indicate that a request for DMA service has

Table 2- 7 82379AB Signal Descriptions

Signal	Pin	Type	Description
			been granted by the SIO or that a 16-bit master has been granted the bus.
DMA			
EOP	20	I/O	End of Process: EOP is bidirectional, and is directly connected to the TC line of the ISA Bus. DMA slaves assert EOP to the SIO to terminate DMA cycles. The SIO asserts EOP to DMA slaves as a terminal count indicator.
REFRESH#	4	I/O	Refresh: As an output, REFRESH# is used by the SIO to indicate when a refresh cycle is in progress. It should be used to enable the SA[15:0] address to the row address inputs of all banks of dynamic memory on the ISA Bus.
SPKR	73	O	Speaker Drive: This signal drives an external speaker driver device. The previous function of the TESTO pin in the SIO.G is multiplexed on the SPKR signal. The TESTO function is selected when the appropriate test mode is invoked.
Interrupt Controller			
IRQ[15, 14, 11:9, 7:3, 1]	41, 43, 37, 35, 184, 7, 9, 11, 14, 16, 168	I	Interrupt Request: The IRQ signals provide both system board components and ISA Bus I/O devices with a mechanism for synchronously interrupting the CPU. TTL Schmitt trigger input buffers are used on all of the XIRQx signals. This helps prevent spurious interrupts.
IRQ8#	172	I	Interrupt Request Eight Signal: IRQ8# is an active low interrupt input. TTL Schmitt trigger input buffers are used on all of the XIRQx signals. This helps prevent spurious interrupts.
INT	75	O	CPU Interrupt: INT is driven by the SIO to signal the CPU that an interrupt request is pending and needs to be serviced.
NMI	74	O	Non-Maskable Interrupt: NMI is used to force a non-maskable interrupt to the CPU. The SIO generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed.

Table 2- 7 82379AB Signal Descriptions

Signal	Pin	Type	Description
Utility Bus			
UBUSTR	165	O	Utility Data Bus Transmit/Receive. UBUSTR is tied directly to the direction control of a 74F245 that buffers the utility data bus UD[7:0].
UBUSOE#	164	O	Utility Data Bus Output Enable. UBUSOE# is tied directly to the output enable of a 74F245 that buffers the utility data bus UD[7:0] from the system data bus SD[7:0].
ECSADDR[2:0]	173-174	O	Encoded Chip Selects. ECSADDR[2:0] are the encoded chip selects and/or control signals for the Utility Bus peripherals supported by the SIO. The binary code formed by the three signals indicates which Utility Bus device is selected. These signals tie to the address inputs of two external 74F138 decoder chips and are driven valid/invalid from the SA[16:0] and LA[23:17] address lines.
ECSSEN#	170	O	Encoded Chip Select Enable. ECSSEN# is used to determine which of the two external 74F138 decoders is to be selected.
ALT_RST#	76	O	Alternate Reset. ALT_RST# is used to reset the CPU under program control. This signal is AND'ed together externally with the reset signal (KBDRST#) from the keyboard controller to provide a software means of resetting the CPU. This provides a faster means of reset than is provided by the keyboard controller.
ALT_A20	85	O	Alternate A20. ALT_A20 is used to force A20M# to the CPU low for support of real mode compatible software.
DSKCHG	161	I	Disk Change. DSKCHG is tied directly to the DSKCHG signal of the floppy controller.
FERR# / IRQ13	71	I	Numeric Coprocessor Error / IRQ13. If programmed to support coprocessor error reporting, this signal is tied to the coprocessor error signal on the CPU. If the coprocessor error reporting is disabled, FERR# can be used by the system as IRQ13. TTL Schmitt trigger input buffers are used on all of the XIRQx signals. This helps prevent spurious interrupts.
IGNNE#	72	O	Ignore Error. This signal is connected to the ignore error pin of the CPU.

Table 2- 7 82379AB Signal Descriptions

Signal	Pin	Type	Description
Utility Bus			
IRQ12/M	39	I	Interrupt Request/Mouse Interrupt. In addition to providing the standard interrupt function as described in the pin description for IRQ[15,14,11:9,7:3,1], this pin also provides a mouse interrupt function. TTL Schmitt trigger input buffers are used on all of the XIRQx signals. This helps prevent spurious interrupts.
Energy Efficient Desktop Support			
SMI#	160	O	System Management Interrupt. SMI# is an active low output that is asserted by the SIO in response to one of many hardware or software events. SMI# connects directly to the CPU. The SMI# signal is an asynchronous input to the CPU. The CPU recognizes the falling edge responds by entering SMM (System Management Mode). SMI# is deasserted during and following reset.
STPCLK#	167	O	Stop Clock. STPCLK# is an active low output that is asserted by the SIO in response to one of many hardware or software events. STPCLK# connects directly to the CPU. The STPCLK# signal is an asynchronous input to the CPU. When the CPU samples STPCLK# asserted it responds by stopping its internal clock. STPCLK# is deasserted during and following reset.
EXTSMI#	171	I	External System Management Interrupt. EXTSMI# is a falling edge triggered input to the SIO indicating that an external device is requesting the system to enter SMM mode. When enabled a falling edge on EXTSMI# will result in the assertion of the SMI# signal to the CPU. EXTSMI# is an asynchronous input to the SIO. However when the setup and hold times are met it is only required to be asserted for one PCICLK. Once deasserted it must remain deasserted for at least four PCICLKs in order to allow the edge detect logic to reset.
INIT	136	I	INIT. INIT is an input to the SIO indicating that the CPU is actually being soft reset. It is connected to the INIT pin of the CPU. The SIO monitors this pin so that when necessary it can regenerate an SMI# edge after INIT is deasserted. INIT is an asynchronous input.

Table 2- 7 82379AB Signal Descriptions

Signal	Pin	Type	Description
PCI Interrupts			
PIRQ[3:0]#	84-81	I	PCI Interrupt Request. PIRQ#s are used to generate asynchronous interrupts to the CPU via the Programmable Interrupt Controllers (82C59s) integrated in the SIO. These signals are defined as level sensitive and are asserted low. The PIRQx# can be steered into any unused IRQ interrupt. The PIRQx# Route Control Register determines which IRQ interrupt each PCI interrupt is steered into. TTL Schmitt trigger input buffers are used on all of the XIRQx signals. This helps prevent spurious interrupts.
APIC			
APICD1	21		This signal functions as bidirectional open drain APICD1. This is APIC Data Bit 0 of the serial APIC data bus. APICD1 should be tristated during PCIRST#. APICD1 also has a weak internal pull-down resistor since this pin may be a "no comment" on an old board.
APICD0	206		This signal functions as bidirectional open drain APICD0. This is APIC Data Bit 0 of the serial APIC data bus. APICD0 should be tristated during PCIRST#.
APICCLK	195		This signal functions as input APICCLK. SIO.A supports a maximum frequency on APICCLK of 33MHz.

2.7 EISA System Component (82374SB)

The 82374EB/SB EISA System Component (ESC) provides all the EISA system compatible functions. The ESC with the PCEB provide all the functions to implement an EISA-to-PCI bridge and EISA I/O subsystem. The ESC integrates the common I/O functions found in today's EISA-based PC systems. The ESC incorporates the logic for an EISA (master and slave) interface, EISA bus controller, enhanced seven channel DMA controller with scatter-gather support, EISA arbitration, 14 channel interrupt controller, Advanced Programmable Interrupt Controller (APIC), five programmable timer/counters, and non-maskable-interrupt (NMI) control logic. The ESC also integrates support logic to decode peripheral devices such as the Flash BIOS, real time clock, keyboard/mouse controller, floppy controller, two serial ports, one parallel port, and IDE hard disk drive.

2.7.1 Features

- Integrates EISA Compatible bus Controller
 - Translates Cycles Between EISA and ISA bus
 - Supports EISA Burst and Standard Cycles
 - Supports ISA Zero Wait-State Cycles
 - Supports Byte Assembly/ Disassembly for 8-, 16- and 32-Bit Transfers
 - Supports EISA bus Frequency of up to 8.33 MHz
- Supports Eight EISA Slots
 - Directly Drives Address, Data and Control Signals for Eight Slots
 - Decodes Address for Eight Slot Specific AENs
- Provides Enhanced DMA Controller
 - Provides Scatter-Gather Function
 - Supports Type A, Type B, Type C (Burst), and Compatible DMA Transfer
 - Provides Seven Independently Programmable Channels
 - Integrates Two 82C37A Compatible DMA Controllers
- Integrates the Functionality of two 82C59 Interrupt Controllers and two 82C54 Timers
 - Provides 14 Programmable Channels for Edge or Level Interrupts
 - Provides 4 PCI Interrupts Routable to any of 11 Interrupt Channels
 - Supports Timer Function for Refresh Request, System Timer, Speaker Tone, Fail Safe Timer, and CPU Speed Control
- Advanced Programmable Interrupt Controller (APIC)
 - Multiprocessor Interrupt Management
 - Separate bus For Interrupt Messages
- 5 V CMOS Technology

-
- Provides High Performance Arbitration
 - Supports Eight EISA Masters and PCEB
 - Supports ISA Masters, DMA Channels, and Refresh
 - Provides Programmable Arbitration Scheme for Fixed, Rotating, or Combination Priority
 - Integrates Support Logic for X-bus Peripherals
 - Generates Chip Selects/Encoded Chip Selects for Floppy and Keyboard Controller, IDE, Parallel/Serial Ports, and General Purpose Peripherals
 - Provides Interface for Real Time Clock
 - Generates Control Signals for X-bus Data Transceiver
 - Integrates Port 92, Mouse Interrupt, and Coprocessor Error Reporting
 - Generates Non-Maskable Interrupts (NMI)
 - PCI System Errors
 - PCI Parity Errors
 - EISA bus Parity Errors
 - Fail Safe Timer
 - bus time-out
 - Via Software Control
 - Provides BIOS Interface
 - Supports 512K Bytes of Flash or EPROM BIOS on the X-bus
 - Allows BIOS on PCI
 - Supports Integrated VGA BIOS
 - 208-Pin QFP Package

2.7.2 Block Diagram

82374SB : ESC

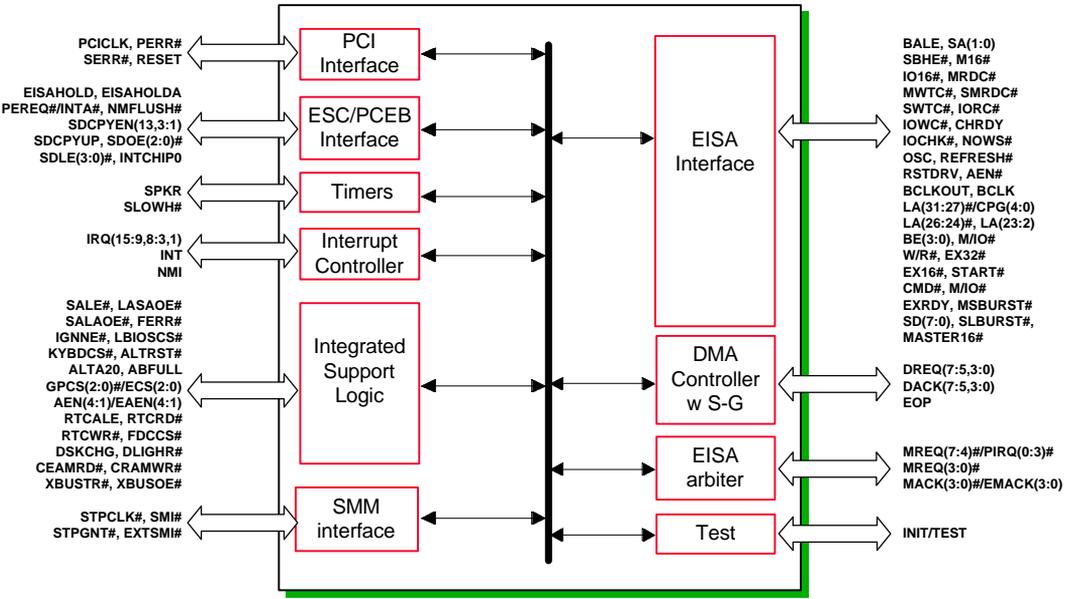


Figure 2- 11 ESC (82374SB) Block Diagram

2.7.3 Pin Diagram

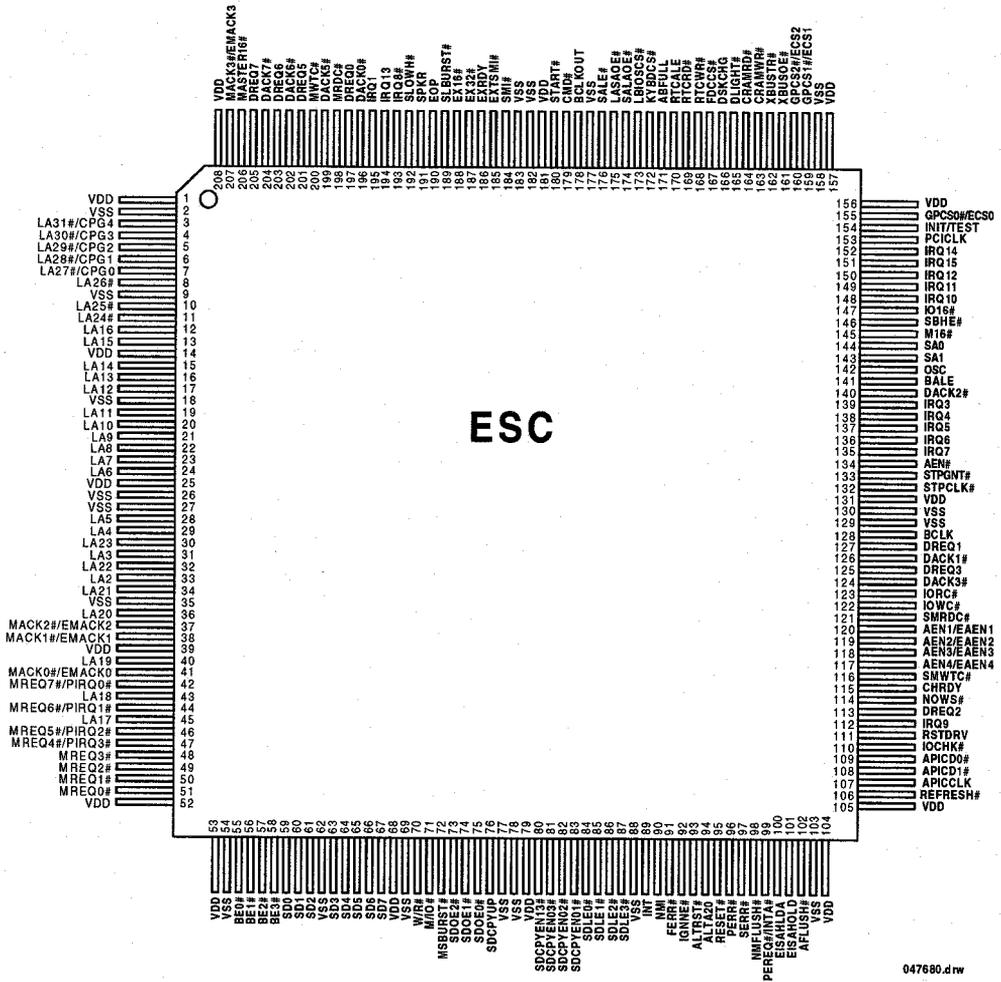


Figure 2- 12 ESC (82374SB) Pin Diagram

2.7.4 Signal Descriptions

The following notations describe the signal types.

Table 2- 8 ESC (82374SB) Signal Abbreviations

Signal	Description
in	Input is a standard input-only signal.
out	Totem Pole Output is a standard active driver.
O/d	Open Drain Input/Output.
Vs	Tristate is a bidirectional, tristate input/output pin.
s/Vs	Sustained Tristate is an active low tristate signal owned and driven by one and only one agent at a time. The agent that drives a s/Vs pin low must drive it high for at least one clock before letting it float. A new agent can not start driving a s/Vs signal any sooner than one clock after the previous owner tristates it. A pull-up sustains the inactive state until another agent drives it and is provided by the central resource.

During a hard reset, INTR, NMI, IGNNE#, SMI# (on 82374SB), ALTRST#, STPCLK# (on 82374SB) and ALTA20 are driven low to prevent problems associated with 5V/3.3V power sequencing. Any outputs of the ESC that are directed to a 3.3V CPU must be driven through a 5V to 3.3V translator.

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
PCI Local Bus Interface			
PCICLK	153	in	PCI CLOCK: PCICLK provides timing for all transactions on the PCI bus. The ESC uses the PCI Clock (PCICLK) to generate EISA bus Clock (BCLK). The PCICLK is divided by 3 or 4 to generate the BCLK. The EISA Bridge supports PCI Clock frequencies of 25 MHz through 33 MHz.
PERR#	96	in	PARITY ERROR: PERR# indicates a data parity error. PERR# may be pulsed active by any agent that detects an error condition. Upon sampling PERR# active, the ESC generates an NMI interrupt to the CPU.
SERR#	97	in	SYSTEM ERROR: SERR# may be pulsed active by any agent that detects an error condition. Upon sampling SERR# active, the ESC generates an NMI interrupt to the CPU.
PCI Local Bus Interface			
RESET#	95	in	SYSTEM RESET: RESET# forces the entire ESC chip into a known state. All internal ESC state machines are reset and all registers are set to their default values. RESET# may be asynchronous to PCICLK when asserted or negated. Although asynchronous, negation must be a clean, bounce-free edge. The ESC uses RESET# to generate RSTDRV signal.
EISA Bus Interface			
BCLKOUT	178	out	EISA BUS CLOCK OUTPUT: BCLKOUT is typically buffered to create EISA bus Clock (BCLK). The BCLK is the system clock used to synchronize events on the EISA/ISA bus. The BCLKOUT is generated by dividing the PCICLK. The ESC uses a divide by 3 or divide by 4 to generate the BCLKOUT.
BCLK	128	in	EISA BUS CLOCK: The ESC uses BCLK to synchronize events on the EISA bus. The ESC generates or samples all the EISA/ISA bus signals on either the rising or the falling edge of BCLK.

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
EISA Bus Interface			
LA[31:27]# / CPG[4:0]	3, 4, 5, 6, 7	t/s	<p>EISA ADDRESS BUS/CONFIGURATION RAM PAGE ADDRESS: These are multiplexed signals. These signals behave as the EISA address bus under all conditions except during access cycle to the Configuration RAM.</p> <p>EISA Address bus: LA[31:27]# are directly connected to the EISA address bus. The ESC uses the address bus in conjunction with the BE[3:0]# signals as inputs to decode accesses to its internal resources except in DMA and Refresh modes. During DMA and Refresh modes, these are outputs, and the ESC uses these signals in conjunction with BE[3:0]# to drive Memory address.</p> <p>Configuration Ram Page Address: CPG[4:0] are connected to Configuration SRAM address lines. During I/O access to 0800h-08FFh, the ESC drives these signals with the configuration page address (the value contained in register 0C00h). The Configuration RAM Page Address function can be disabled by setting Mode Select register bit 5 = 0.</p>
LA[26:24]#, LA[23:2]	8, 10, 11, 30, 32, 34, 36, 40, 43, 45, 12:13, 15:17, 19, 20:24, 28:29, 31, 33	t/s	<p>EISA ADDRESS BUS: These signals are directly connected to the EISA address bus. The ESC uses the address bus in conjunction with the BE[3:0]# signals as inputs to decode accesses to its internal resources except in DMA and Refresh modes. During DMA and Refresh modes, these are outputs, and the ESC uses these signals in conjunction with BE[3:0]# to drive Memory address.</p>
BE[3:01#	58, 57, 56, 55	t/s	<p>BYTE ENABLES: BE[3:0]# signals are directly connected to the EISA address bus. These signals indicate which byte on the 32-bit EISA data bus are involved in the current cycle. BE[3:0]# are inputs during EISA master cycles which do not require assembly/disassembly operation. For EISA master assembly/disassembly cycles, ISA master cycles, DMA, and Refresh cycles BEf3:01# are outputs.</p> <p>BE0#: Corresponds to byte lane 0-SD[7:0] BE1# BE1#: Corresponds to byte lane 0-SD[15:8] BE2# BE2#: Corresponds to byte lane 0-SD[23:16] BE3# BE3#: Corresponds to byte lane 0-SD[31:24]</p>

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
EISA Bus Interface			
M/IO#	71	t/s	MEMORY OR I/O CYCLE: M/IO# signal is used to differentiate between memory cycles and I/O cycles on the EISA bus. A High value on this signal indicates a memory cycle, and a Low value indicates an I/O cycle. M/IO# is an input to the ESC during EISA master cycles, and M/IO# is an output during ISA, DMA, and ESC initiated Refresh cycles. M/IO# is floated during ISA master initiated Refresh cycles.
W/R#	70	t/s	WRITE OR READ CYCLE: W/R# signal is used to differentiate between write and read cycles on the EISA bus. A High value on this signal indicates a Write cycle, and a Low value indicates a Read cycle. W/R# is an input to the ESC during EISA master cycles, and W/R# is an output during ISA, DMA, and Refresh cycles.
EX32#	187	o/d	EISA 32 BIT DEVICE DECODE: EX32# signal is asserted by a 32-bit EISA slave device. EX32# assertion indicates that an EISA device has been selected as a slave, and the device has a 32-bit data bus size. The ESC uses this signal as an input as part of its slave decode to determine if data size translation and/or cycle translation is required. EX32# is an output of the ESC during the last portion of the mismatched cycle. This is an indication to the backed-off EISA master that the data translation has been completed. The backed-off EISA master uses this signal to start driving the EISA bus again.
EX16#	188	o/d	EISA 16-BIT DEVICE DECODE: EX16# signal is asserted by a 16-bit EISA slave device. EX16# assertion indicates that an EISA device has been selected as a slave, and the device has a 16 bit data bus size. The ESC uses this signal as an input as part of its slave decode to determine if data size translation and/or cycle translation is required. EX16# is an output of the ESC during the last portion of the mismatched cycle. This is an indication to the backed-off EISA master that the data translation has been completed. The backed-off EISA master uses this signal to start driving the EISA bus again.
START#	180	t/s	START CYCLE: START# signal provides timing control at the start of an EISA cycle. START# is asserted for one BCLK. START# is an input to the ESC during EISA master cycles except portions of the EISA master to mismatched slave cycles where it becomes an output. During ISA, DMA, and Refresh cycles

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
			START# is an output.
EISA Bus Interface			
CMD#	179	out	COMMAND: CMD# signal provides timing control within an EISA cycle. The ESC is a central resource of the CMD# signal, and the ESC generates CMD# during all EISA cycles. CMD# is asserted from the rising edge of BCLK simultaneously with the negation of START#, and remains asserted until the end of the cycle.
EXRDY	186	o/d	EISA READY: EXRDY signal is deasserted by EISA slave devices to add wait states to a cycle. EXRDY is an input to the ESC for EISA master cycles, ISA master cycles, and DMA cycles where an EISA slave has responded with EX32# or EX16# asserted. The ESC samples EXRDY on the falling edge of BCLK after CMD# is asserted (except during DMA compatible cycles). During DMA compatible cycles, EXRDY is sampled on the second falling edge of BCLK after CMD# is driven active. For all types of cycles if EXRDY is sampled inactive, the ESC keeps sampling it on every falling edge of BCLK#. EXRDY is an output for EISA master cycles decoded as accesses to the ESC internal registers. ESC forces EXRDY low for one BCLK at the start of a potential DMA burst write cycle to insure that the initial write data is held long enough to be sampled by the memory slave.
SLBURST#	189	in	SLAVE BURST: SLBURST# signal is asserted by an EISA slave to indicate that the device is capable of accepting EISA burst cycles. The ESC samples SLBURST# on the rising edge of BCLK at the end of START# for all EISA cycles. During DMA cycles, the ESC samples SLBURST# twice; once on the rising edge of BCLK at the beginning of START# and again on the rising edge of BCLK at the end of START#.
MSBURST#	72	t/s	MASTER BURST: MSBURST# signal is asserted by an EISA master to indicate EISA burst cycles. MSBURST# is asserted by an EISA master in response to an asserted SLBURST# signal. The ESC samples SLBURST# on the rising edge of BCLK that CMD# is asserted. If asserted, the ESC samples SLBURST# on all subsequent rising edges of BCLK until sampled negated. The ESC keeps CMD# asserted during Burst cycles. MSBURST# is an output during DMA burst cycles. The ESC drives MSBURST# active on the falling edge of BCLK, one half

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
			BCLK after SLBURST# is sampled after at the end of START#.
EISA Bus Interface			
MASTER16#	206	in	MASTER 16-BIT: MASTER16# is asserted by a 16-bit EISA bus master or an ISA bus master device to indicate that it has control of the EISA bus or ISA bus. The ESC samples MASTER16# on the rising edge of BCLK that START# is asserted. If MASTER16# is sampled asserted, the ESC determines that a 1 6-bit EISA bus master or an ISA bus master owns the bus. If MASTER16# is sampled negated at the first sampling point, the ESC will sample MASTER16# a second time on the rising edge of BCLK at the end of START#. If MASTER16# is sampled asserted here, the ESC determines that a 32-bit EISA bus master has downshifted to a 1 6-bit bus master. and thus. the ESC will disable the data size translation function
SD[7:0]	67:63, 61:59	t/s	SYSTEM DATA: SD[7:0] signals are directly connected to the System Data bus. The SD[7:0] pins are outputs during I/O reads when the ESC internal registers are being accessed and during interrupt acknowledge cycles. The SD[7:0] pins are input during I/O writes cycles when the ESC internal registers are being accessed.
BALE	141	out	BUS ADDRESS LATCH ENABLE: BALE signal is asserted by the ESC to indicate that a address (SA[19:0], LA[23:17]), AEN and SBHE# signal lines are valid. The LA[23:17] address lines are latched on the trailing edge of BALE. BALE remains active throughout DMA and ISA Master cycles and Refresh cycles.
SA[1:0]	143:144	t/s	ISA ADDRESS BITS 0&1 : SA[1:0] are the least significant bits of the ISA address bus. SA[1:0] are inputs to the ESC during ISA master cycles except during ISA master initiated Refresh cycles. The ESC uses the SA[1:0] in conjunction with SBHE# to generate BE[3:0]# on the EISA bus. The SA[1:0] are outputs of the ESC during EISA master cycles and DMA cycles. The ESC generates these from BE[3:0]#.
SBHE#	146	t/s	ISA BYTE HIGH ENABLE: SBHE# signal indicates that the high byte on the ISA data bus (SD[15:8]) is valid. SBHE# is an input to the ESC during ISA master cycles, except during ISA master initiated Refresh cycles. The ESC uses the SBHE# in conjunction with

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
			SA[1:0] to generate BE[3:0]# on the EISA bus. SBHE# is an output during EISA master and DMA cycles.
EISA Bus Interface			
M16#	145	o/d	MEMORY CHIP SELECT 16: M16# is an input when the ESC component owns the ISA bus. M16# is an output when an external ISA bus Master owns the ISA bus. The ISA slave memory drives this signal Low if it is a 16-bit memory device. For ISA to EISA translation cycles, the ESC asserts M16# if either EX32# or EX16# are asserted. This signal has an external pull-up resistor.
IO16#	147	o/d	16-BIT I/O CHIP SELECT: IO16# signal is used to indicate a 16-bit I/O bus cycle. This signal is asserted by the I/O devices to indicate that they support 16-bit I/O bus cycles. All I/O accesses to the ESC registers are run as 8-bit I/O bus cycles. This signal has an external pull-up resistor.
MRDC#	198	t/s	MEMORY READ: MRDC# signal indicates a read cycle to the ISA memory devices. MRDC# is the command to a memory slave that it may drive data onto the ISA data bus. MRDC# is an output when the ESC owns the ISA bus. MRDC# is an input when an external ISA bus master owns the ISA bus. This signal is driven by the ESC during refresh cycles.
MWTC#	200	t/s	MEMORY WRITE: MWTC# signal indicates a write cycle to the ISA memory devices. MWTC# is the command to a memory slave that it may latch data from the ISA data bus. MWTC# is an output when the ESC owns the ISA bus. MWTC# is an input when an ISA bus master owns the ISA bus.
SMRDC#	121	out	SYSTEM MEMORY READ: SMRDC# signal is asserted by the ESC to request a memory slave to drive data onto the data lines. SMRDC# indicates that the memory read cycle is for an address below the 1 MB range on the ISA bus. This signal is also asserted during refresh cycles.
SMWTC#	116	out	SYSTEM MEMORY WRITE: SMWTC# signal is asserted by the ESC to request a memory slave to accept data from the data lines. SMWTC# indicates that the memory write cycle is for an address below the 1 MB range.
IORC#	123	t/s	I/O READ: IORC# is the command to an ISA I/O slave device that it may drive data on to the data bus (SD[15:0]). The device must hold the data valid until after IORC# is negated.

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
			IORC# is an output when the ESC component owns the ISA bus. IORC# is an input when an ISA bus master owns the ISA bus.
ISA Bus Interface			
IOWC#	122	t/s	I/O WRITE: IOWC# is the command to an ISA I/O slave device that it may latch data from the ISA data bus (SD[15:0]). IOWC# is an output when the ESC component owns the ISA bus. IOWC# is an input when an ISA bus master owns the ISA bus.
CHRDY	115	o/d	I/O CHANNEL READY: CHRDY when asserted allows ISA bus resources request additional time (wait-states) to complete the cycle. CHRDY is an input when the ESC owns the ISA bus. CHRDY is an input to the ESC during compatible DMA cycles. CHRDY is an output during ISA bus master cycles to PCI slave or ESC internal register. The ESC will ignore CHRDY for ISA bus master accessing an ISA-bus slave.
IOCHK#	110	in	I/O CHANNEL CHECK: IOCHK# can be asserted by any resource on the ISA bus. When asserted, it indicates that a parity or an uncorrectable error has occurred for a device or memory on the ISA bus. A NMI will be generated to the CPU if enabled.
NOWS#	114	o/d	ZERO WAIT STATES: NOWS# indicates that a peripheral device wishes to execute a zero wait-state bus cycle (the normal default 16-bit ISA bus memory or I/O cycle is 3 BCLKS). When NOWS# is asserted, a 16-bit memory cycle occurs in two BCLKs and a 16-bit I/O cycle occurs in three BCLKs. When NOWS# is asserted by an 8-bit device the default 6 BCLKs cycle is shortened to 4 or 5 BCLKs. NOWS# is an input when the ESC performing bus translation cycles. NOWS# is an output when the ESC internal registers are accessed. If CHRDY and NOWS# are both asserted during the same clock then NOWS# will be ignored and wait-states will be added as a function of CHRDY (CHRDY has precedence over NOWS#).
OSC	142	in	OSCILLATOR: OSC is the 14.31818 MHz signal with 50% duty cycle. OSC is used by the ESC timers
RSTDRV	111	out	RESET DRIVE: RSTDRV is asserted by the ESC. An asserted RSTDRV causes a hardware reset of the devices on the ISA bus. RSTDRV is asserted whenever the RESET# input to the ESC is asserted.

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
ISA Bus Interface			
REFRESH#	106	t/s	REFRESH: REFRESH# is used by the ESC as an output to indicate when a refresh cycle is in progress. It should be used to enable the SA[t5:0] address to the row address inputs of all banks of dynamic memory on the ISA bus so that when MRDC# goes active, the entire expansion bus dynamic memory is refreshed. Memory slaves must not drive any data onto the bus during refresh and should not add wait states since this affects the entire system throughput. As an output, this signal is driven directly onto the ISA bus. This signal is an output only when the ESC DMA Refresh is a master on the bus responding to an internally generated request for Refresh. Upon RESET this pin tristates. Note that address lines [15:8] are driven during refresh, but the value is meaningless and is not used to refresh ISA bus memory. REFRESH# may asserted by an expansion bus adapter acting as a 1 6-bit ISA bus master.
AEN#	134	out	ADDRESS ENABLE: AEN# is driven high for bus master cycles. AEN# is driven low for DMA cycles. and Refresh cycles. AEN# is used to disable I/O devices from responding to DMA and Refresh cycles. System designs which do not used the slots specific AENs (AEN[4:1]/EAEN[4:1]) provided by the ESC can use the AEN# signal to generate their own slot specific AENs.
AEN[4: 1] / EAEN[4: 1]	117, 118, 119, 120	out	SLOT SPECIFIC ADDRESS ENABLE/ENCODED SLOT SPECIFIC ADDRESS ENABLE: These pins have a slightly different function depending on the ESC configuration (Mode Select register bit 1 and bit 0). Slot Specific Address Enable: If the ESC is programmed to support 4 EISA slots, these signals function as Slot Specific Address Enables (AEN[4:1]). Encoded Slot Specific Address Enable: If the ESC has been programmed to support more than 4 EISA slots, then these signals behave as Encoded Address Enables (EAEN[4:1]). A discrete decoder is required to generate slot specific AENs.

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
DMA Signals			
DREQ[7:5,3:0]	205, 203, 201, 125, 113, 127, 197	in	DMA REQUEST: DREQ signals are either used to request DMA service from the ESC or used to gain control of the ISA bus by a ISA bus master. The active level (high or low) is programmed in the Command registers. When the Command register bit 6 is programmed to 0, DREQ are asserted high, otherwise the DREQ are asserted low. All inactive to active edges of DREQ are assumed to be asynchronous. The request must remain asserted until the appropriate DACK is negated. At power-up and after RESET, these lines should be low (negated).
DACK# [7:5,3:0]	204, 202, 199, 124, 140, 126, 196	out	DMA ACKNOWLEDGE: DACK# indicate that a request for DMA service from the DMA subsystem has been recognized or that an ISA bus master has been granted the bus. The level of the DACK lines when asserted may be programmed to be either high or low. This is accomplished by programming the DMA Command register. These lines should be used to decode the DMA slave device with the IORC# or IOWC# line to indicate selection. If used to signal acceptance of a bus master request, this signal indicates when it is legal to assert MASTER16#. If the DMA controller has been programmed for a timing mode other than compatible mode, and another device has requested the bus, and a 4 us time has elapsed, DACK# will be negated and the transfer stopped before the transfer is complete. In this case, the transfer will be restarted at the next arbitration period in which the channel wins the bus. Upon reset these lines are negated.
EOP	190	t/s	END OF PROCESS: EOP pin acts in one of two modes, and it is directly connected to the TC line of the ISA bus. In the first mode, EOP-In, the pin is an input and can be used by a DMA slave to stop a DMA transfer. In the second mode, TC-Out, it is used as a terminal count output by DMA slaves. An active pulse is generated when the byte counter reaches its last value. EOP-In Mode: During DMA, for all transfer types, the EOP pin is sampled by the ESC. If it is sampled asserted, the address bus is tristated and the transfer is terminated

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
DMA Signals			
EOP continued	190	t/s	<p>TC-Out Mode: The EOP output is asserted after a new address has been output if the byte count expires with that transfer. The EOP (TC) stays asserted until AEN# is negated unless AEN is negated during an auto-initialization. EOP (TC) is negated before AEN is negated during an auto-initialization.</p> <p>Input Mode: In this mode the EOP signal has the same behavior as the Chaining Interrupt or the Scatter-Gather interrupt to the host processor (IRQ13). If a scatter-gather or chaining buffer is expired, EOP goes active on the falling edge of BCLK. Only the currently active channel's interrupt is reflected on this pin. Other channel's with active interrupts pending will not affect the EOP pin.</p> <p>Whenever all the DMA channels are not in use the EOP pin is kept in output mode and negated. After reset, the EOI pin is kept in output mode and negated.</p>
EISA Arbitration Signals			
MREQ[3:0]#	48:51	in	<p>MASTER REQUEST: MREQ[3:0]# are slot specific signals used by EISA bus masters to request bus access. MREQ# once asserted, must remain asserted until the corresponding MACK# is asserted. The MREQ# is negated on the falling edge of BCLK slightly before the end of a master transfer. The LA[], BE[]#, M/IO#, and W/R# lines should be floated on or before the rising edge of BCLK after MREQ# is negated. The end of the last bus cycle is derived from CMD# in this case. The MREQ# signals are asserted on the falling edge of BCLK. MREQ# is always sampled on the rising edge of BCLK. MREQ# is synchronous with respect to BCLK. After asserting MREQ#, the corresponding master must not assert MREQ# until 1.5 BCLKs after CMD# is negated.</p>
MREQ[7:4]#/ PIRQ[0:3]#	52, 44, 46, 47,	in	<p>MASTER REQUEST/PCI INTERRUPT REQUEST: These pins behave in one of two modes depending on the state of the Mode Select Register bit 1 and bit 0.</p> <p>Master Request: MREQ# lines are slot specific signals used by EISA bus masters to request bus access. This signal behave in the same manner as MREQ[3:0]# signals.</p>

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
EISA Arbitration Signals			
MREQ[7:4]#/PIRQ[0:3]# continued	52, 44, 46, 47,	in	PCI Interrupt Request: PIRQ# are used to generate asynchronous interrupts to the CPU via the Programmable Interrupt Controller (82C59) integrated in the ESC. These signals are defined as level sensitive and are asserted low. The PIRQx# can be shared with PC compatible interrupts IRQ3:IRQ7, IRQ9:IRQ15. The PIRQx# Route Control Register determines which PCI interrupt is shared with which PC compatible interrupt.
MACK[3:0]#/EMACK[3:0]	207, 37:38, 41	out	<p>MASTER ACKNOWLEDGE:/ENCODED MASTER ACKNOWLEDGE: These pins behave in one of two modes depending on the state of the Mode Select register bit 1 and bit 0. If the ESC is programmed to support 4 EISA slots, these pins are used as MACK#. If the ESC is programmed to support more than 4 EISA slots, these pins are used as EMACK#.</p> <p>Master Acknowledge: The MACK[3:0]# signals are asserted from the rising edge of BCLK at which time the bus master may begin driving the LA[], BE[]#, M/IO#, and W/R# lines on the next falling edge of BCLK. MACK# will stay asserted until the rising edge of BCLK when MREQ# is sampled negated. MACK# is sampled by EISA bus masters on the falling edge of BCLK. If another device has requested the bus, MACK# is negated before MREQ# is negated. When MACK# is negated, the granted device has a maximum of 8 μs to negate MREQ# and begin a final bus cycle. The ESC may negate the MACK# signal a minimum of one BCLK after asserting it if another device (or refresh) is requesting the bus. Upon reset MACK# is negated.</p> <p>Encoded Master Acknowledge: EMACK# behaves like MACK#. The difference is that a discrete decoder is required to generate MACK# for the EISA bus masters.</p>

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
Timer Unit Signals			
SPKR	191	out	SPEAKER DRIVE: SPKR is the output of Timer 1, Counter 2 and is "ANDed" with Port 061 h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the ISA system speaker. SPKR has a 24 mA drive capability. Upon reset, its output state is low.
SLOWH#	192	out	<p>SLOW DOWN CPU: SLOWH# is the output of Timer 2, Counter 2. This counter is used to slow down the main CPU of its execution via the CPU's HOLD pin by pulse width modulation. The first read of I/O register in the 048h-04Bh range enables SLOWH# signal to follow the output of the Timer 2, Counter 2. Upon reset, SLOWH# is negated.</p> <p>Hardware Reset (Strapping Option) During hardware reset this signal is an input and the level on the pin at the end of the reset sequence determines where BIOS resides. A high level indicates that BIOS resides on the X-bus and a low level indicates that BIOS resides on the ISA bus. The status is used by the ESC, to control the X-bus transceivers during BIOS access.</p> <p>Note: For the 82374EB, this pin has an internal weak pull-up of approximately 8 Kn. For proper configuration of the BIOS location during reset, a weak external pull-down resistor (approx. 500S2) must be connected to this pin. An external pull-down resistor is not needed for the 82374SB.</p>
Interrupt Controller Signals			
IRQ[15:9], IRQ8#, IRQ[7:3,1]	151:152, 194, 150, 149:148, 112, 193, 135:137, 195	in	INTERRUPT REQUEST: IRQ These signals provide both system board components and EISA bus I/O devices with a mechanism for asynchronously interrupting the CPU. The assertion mode of each interrupt can be programmed to be edge or level triggered. An asserted IRQ input must remain asserted until after the falling edge of INTA#. If the input is negated before this time, a DEFAULT IRQ7 occurs when the CPU acknowledges the interrupt. IRQ8# requires an external pull-up resistor (8-10 KΩ).

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
Interrupt Controller Signals			
INTR	89	out	CPU INTERRUPT: INTR is driven by the ESC to signal the CPU that an Interrupt request is pending and needs to be serviced. It is asynchronous with respect to BCLK or PCICLK and it is always an output. The interrupt controllers must be programmed following a reset to ensure that this pin takes on a known state. Upon reset the state of this pin is undefined.
NMI	90	out	NON-MASKABLE INTERRUPT: NMI is used to force a non-maskable interrupt to the CPU. The CPU registers an NMI when it detects A rising edge on NMI. NMI remains active until a read from the CPU to the NMI register at port 061 h is detected by the ESC. This signal is set to low upon reset.
APIC Bus Signals			
APICCLK	107	in	APIC BUS CLOCK: APICCLK provides the timing reference for the APIC bus. Changes on APICD[1:0]# are synchronous to the rising edge of APICCLK.
APICD[1:0]#	108, 109	od	APIC DATA: APICD1 and APICD0 are the APIC data bus signals. Interrupt messages are sent/received over this bus. APIC arbitration uses APICD1.
System Power Management Signals			
STPCLK	132	out	STOP CLOCK: ESC asserts STPCLK# in response to one of many maskable hardware or software events. For 3.3V processors that are not 5V tolerant, STPCLK# is driven to the CPU STPCLK# pin through a 5V to 3.3V translator. When the CPU samples STPCLK# asserted it responds by stopping its internal clock. This signal is negated after a hard reset.
SMI#	184	out	SYSTEM MANAGEMENT INTERRUPT: SMI# is asserted by the ESC in response to one of many maskable hardware or software events. For 3.3V processors that are not 5V tolerant, SMO# is driven to the CPU SMI# pin through a 5V to 3.3V translator. The CPU recognizes the falling edge of SMI# as the highest priority interrupt in the system. The CPU responds by entering SMM (system Management Mode). SMI# is negated during and following reset. After a hard reset, this signal is negated.

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
System Power Management Signals			
EXTSMI#	185	in	EXTERNAL SYSTEM MANAGEMENT INTERRUPT: EXTSMI# is a falling edge input to the ESC indicating that an external device is requesting the system to enter SMM mode. When enabled via the SMI Enable Register, a falling edge on EXTSMI# results in the assertion of the SMI# signal to the CPU. EXTSMI# is an asynchronous input to ESC.
INIT/TEST	154	in	INITIALIZE/TEST: On the 82374SB, the function of this pin is selected by the value on the GPCS0# pin at reset. If GPCS0# is low, INIT is selected and if GPCD0# is high, TEST is selected. On the 82374EB, this pin only functions as the TEST pin. INIT is connected to the INIT pin on the CPU and indicates to the ESC that a CPU soft reset is occurring. When asserted, the ESC ensures that STPCLK# is negated when the CPU comes out of the soft reset. The ESC also blocks SMI# generation when INIT is asserted.
ESC/PCEB Interface			
Arbitration and Interrupt Acknowledge Control			
EISAHOLD	101	out	EISA Hold. EISAHOLD is used to request the EISA bus control from its default owner, the PCEB. This signal is synchronous to PCICLK and is asserted when RESET# is asserted.
EISAhLDA	100	in	EISA HOLD ACKNOWLEDGE: EISAhLDA is used by the PCEB to inform the ESC that it has been granted ownership of EISA bus. This signal is synchronous to PCICLK.
PEREQ# / INTA#	99	in	PCI to EISA Request or Interrupt Acknowledge. PEREQ#/INTA# is a dual function signal. The EISAhLDA signal state determines the context of this signal. When EISAhLDA is deasserted, this signal has the context of Interrupt Acknowledge, such that if PEREQ#/INTA# is asserted, it indicates to the ESC that current EISA cycle is an interrupt acknowledge. When EISAhLDA is asserted this signal has the context of PCI-to-EISA Request, i.e. if PEREQ#/INTA# is asserted, it indicates to the ESC that PCEB has to own the EISA bus on behalf of a PCI agent. This signal is synchronous to the PCICLK and driven inactive when RESET# is asserted.

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
ESC/PCEB Interface			
PCEB Buffer Coherency Control			
NMFLUSH#	98	T/S	<p>NEW MASTERFLUSH: NMFLUSH# is a bidirectional signal which is used to provide handshake between PCEB and ESC to control flushing of system buffers on behalf of EISA masters.</p> <p>During an EISA bus ownership change, before ESC can grant the bus to the EISA master (or DMA) it must ensure that system buffers are flushed and buffers pointing (potentially) towards EISA subsystem are disabled. The ESC asserts NMFLUSH# signal for one PCI clock indicating the request for system buffer flushing. (After driving NMFLUSH# asserted for 1 PCI clock the ESC tristates NMFLUSH# signal.) When PCEB samples NMFLUSH# asserted it starts immediately to drive NMFLUSH# asserted and initiates internal and external requests for buffer flushing. After all buffers have been flushed (indicated by the proper handshake signals), the PCEB negates NMFLUSH# for 1 PCI clock and stops driving it.</p> <p>When the ESC samples the deasserted signal that indicates that all system buffers are flushed, it grants EISA bus to an EISA master (or DMA). The ESC resumes responsibility of default NMFLUSH# driver and starts driving NMFLUSH# deasserted until the next time a new EISA master (or DMA) wins arbitration.</p> <p>This signal is synchronous with PCICLK and is negated by the ESC at reset.</p>
AFLUSH#	102	T/S	<p>APICFLUSH: AFLUSH# is bidirectional signal between the PCEB and ESC that controls system buffer flushing on behalf of the APIC. After a reset the ESC negates AFLUSH# until the APIC is initialized and the first interrupt request is recognized.</p>
SDCPYUP	76	out	<p>SYSTEM (DATA) COPY UP: SDCPYUP is used to control the direction of the byte copy operation. A high on the signal indicates a COPY UP operation where the lower byte lower word of the SD data bus is copied on to the higher byte or higher word of the bus. A Low on the signal indicates a COPY DOWN operation where the higher byte(s) of the data bus are copied on to the lower byte(s) of the bus. The PCEB uses the signal to perform the actual data byte copy operation during mismatched cycles.</p>

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
ESC/PCEB Interface			
PCEB Buffer Coherency Control			
SDOE[2:0]#	73:75	out	<p>SYSTEM DATA OUTPUT ENABLES: SDOE# enable the SD data output of the PCEB Data Swap buffers on to EISA bus. The ESC activates these signals only during mismatched cycles. The PCEB uses these signal to enable the SD data buffers as follows:</p> <p>SDOE0#: Enables byte lane 0 SD[7:0] SDOE1#: Enables byte lane 1 SD[15:8] SDOE2#: Enables byte lane 2 SD[23:16] and byte lane 3 SD[31 :24]</p>
SDLE[3:0]#	87:84	out	<p>SYSTEM DATA LATCH ENABLES: SDLE[3:0]# enable the latching of EISA data bus. These signals are activated only during mismatched cycles except PCEB initiated write cycle. The PCEB uses these signals to latch the SD data bus as follows:</p> <p>SDLE0#: Latch byte lane 0 SD[7:0] SDLE1#: Latch byte lane 0 SD[15:8] SDLE2#: Latch byte lane 0 SD[23:16] SDLE3#: Latch byte lane 0 SDF31:24</p>
Integrated Logic Signals			
EISA Address Buffer Control			
SALE#	176	out	<p>SA LATCH ENABLE: SALE# is directly connected to F543s which buffer the LA addresses from the SA addresses. The rising edge of SALE# latches the LA address bit LA[19:2] to the SA address bit SA[19:2].</p>
LASAOE#	175	out	<p>LA TO SA ADDRESS OUTPUT ENABLE: LASAOE# is directly connected to the SA output buffer enables of the F543s. The ESC asserts LASAOE# during EISA master cycles. When LASAOE# is asserted, the LA to SA output buffers of the F543s are enabled.</p>
SALAOE#	174	out	<p>SA TO LA ADDRESS OUTPUT ENABLE: SALAOE# is connected to the LA output buffer enables of the F543s. This signal functionally is the exact opposite of LASAOE# signals. The ESC asserts SALAOE# during ISA master cycles. When LASAOE# is asserted, the SA to LA output buffers of the F543s are enabled.</p>

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
Integrated Logic Signals			
Coprocessor Interface			
FERR#	91	in	NUMERIC COPROCESSOR ERROR: FERR# signal is tied to the coprocessor error signal of the CPU. If FERR# is asserted (coprocessor error detected by the CPU), an internal IRQ13 is generated and the INTR from the ESC will be asserted.
IGNNE#	92	out	IGNORE NUMERIC ERROR: IGNNE# is tied to the ignore numeric error pin of the CPU. IGNNE# is asserted and internal IRQ13 is negated from the falling edge of IOWC# during an I/O write to location 00FOh. IGNNE# will remain asserted until FERR# is negated. During reset, this signal is driven low.
BIOS Interface			
LBIOSCS#	173	out	LATCHED BIOS CHIP-SELECT: LBIOSCS# indicates that the current address is for the system BIOS. The ESC generates this signal by decoding the EISA LA addresses. The ESC uses a transparent latch to latch the decoded signal. The LBIOSCS# is latched on the falling edge of BALE and qualified with REFRESH#.
Keyboard Controller Interface			
KYBDCS#	172	out	KEYBOARD CHIP SELECT: KYBDCS# connects to the 80C42 chip select. This signal is active for I/O addresses 0060h and 0064h.
ALTRST#	93	out	ALTERNATE RESET: ALTRST# is used to reset the CPU under program control. This signal is AND'ed together externally with the reset signal (RSTAR#) from the keyboard controller to provide a software means of resetting the CPU. This provides a faster means of reset than is provided by the Keyboard controller. Writing a 1 to bit 0 in the Port 92 register will cause this signal to pulse active (low) for approximately 4 BCLK's. Before another ALTRST# pulse can be generated, bit 0 must be written back to a 0. During reset, this signal is driven low.

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
Integrated Logic Signals			
Keyboard Controller Interface			
ALTA20	94	out	ALTERNATE A20: ALTA20 is used to force A20M# to the CPU low for support of real mode compatible software. This signal is externally OR'ed with the ALTA20 signal from the Keyboard controller and CPURST to control the A20M# input of the CPU. Writing a "0" to bit 1 of Port 92h Register forces ALTA20 inactive (low). This in turn drives A20M# to the CPU low, if A20GATE from the keyboard controller is also low. Writing a "1 " to bit 1 of the Port 92h Register forces ALTA20 active (high), which in turn drives A20M# to the CPU high, regardless of the state of ALTA20 from the keyboard controller. Upon reset, this signal is driven low.
ABFULL	171	in	AUXILIARY BUFFER FULL: ABFULL is tied directly to the ABFULL signal on the keyboard controller on the system board. This signal indicates that the keyboard controller auxiliary buffer for the mouse interface is full. See the CLKDIV Register description for programming the ABFULL function. If this function is not used, ABFULL should be tied low through a 1 K resistor.
Real-time Clock Interface			
RTCALE	170	out	Real-time Clock Address Latch Enable: RTCALE is directly connected to the system Real Time Clock. The RTC uses this signal to latch the appropriate memory address. A write to port 070h with the appropriate Real Time Clock memory address that will be written to or read from will cause RTCALE to go active.
RTCRD# / PIRQ3#	169	out	Real-time Clock Read Command/PCI Interrupt Request 3: This signal pin has two functions selected via the Mode Select Register. When functioning as RTCRD#, this signal is asserted for I/O reads from address 0071h. If the Power On Password protection is enabled (I/O Port 92h bit 3=1), then for accesses to RTC addresses 36h-3Fh (Port 70h), RTCRD# is not asserted. For details on PIRQ3#, see the Mode Select Register description. For the PIRQ3# function, an external pull-up resistor (10-20 K Ω) must be added to this signal.

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
Integrated Logic Signals			
Real-time Clock Interface			
RTCWR# / PIRQ2#	168	out	Real-time Clock Write Command/PCI Interrupt Request 2: This signal pin has two functions selected via the Mode Select Register. When functioning as RTCWR#, this signal is asserted for I/O writes to address 0071h. If the Power On Password protection is enabled (I/O Port 92h bit 3=1) accesses to RTC addresses 36h-3Fh (Port 70h) RTCWR# are not generated. See the Mode Select Register description for details on PIRQ2#. For the PIRQ2# function, add an external pull-up resistor (10-20 K Ω) to this signal.
Diskette Drive Controller Interface			
FDCCS#/ PIRQ1#	167	out	Diskette Drive Controller Chip Select/PCI Interrupt Request PIRQ1 #1: This signal has two functions selected via the Mode Select Register. As FDCCS# is asserted for I/O cycles to the floppy drive controller. When functioning as FDCCS#, this signal is also asserted when IDECS1# is decoded. See the Mode Select Register description for details on the PIRQ1 # function of this signal. For the PIRQ1 # function, an external pull-up resistor (10-20 K Ω) must be added to this signal.

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description																								
Integrated Logic Signals																											
Diskette Drive Controller Interface																											
DSKCHG	166	in	<p>Disk Change: DSKCHG signal is tied directly to the DSKCHG signal of the floppy controller. This signal is inverted and driven onto system data line 7 (SD7) during I/O read cycles to floppy address locations 3F7h (primary) or 377h (secondary) as indicated by the table below. Note that the primary and secondary locations are programmed in the X-bus Address Decode Enable/Disable Register "A".</p> <table border="1"> <thead> <tr> <th>FDCCS# Decode</th> <th>IDECSx# Decode</th> <th>State of SD7 (output)</th> <th>State of XBUSOE#</th> </tr> </thead> <tbody> <tr> <td>Enabled</td> <td>Enabled</td> <td>Tristated</td> <td>Enabled</td> </tr> <tr> <td>Enabled</td> <td>Disabled</td> <td>Driven</td> <td>Disabled</td> </tr> <tr> <td></td> <td colspan="3" style="text-align: center;">via DSKCHG</td> </tr> <tr> <td>Disabled</td> <td>Enabled</td> <td>Tristated</td> <td>Disabled (note)</td> </tr> <tr> <td>Disabled</td> <td>Disabled</td> <td>Tristated</td> <td>Disabled</td> </tr> </tbody> </table> <p>Note: This mode is not supported because of potential contention between the X-bus buffer and a diskette on the ISA bus driving the system bus at the same time during shared I/O accesses.</p> <p>This signal is also used to determine if the floppy controller is present on the X-bus. It is sampled on the trailing edge of RESET, and if high, the floppy is present. For systems that do not support a floppy via the ESC, this pin should be strapped low. If sampled low, the SD7 function and XBUSOE# are not enabled for accesses to the floppy disk controller.</p>	FDCCS# Decode	IDECSx# Decode	State of SD7 (output)	State of XBUSOE#	Enabled	Enabled	Tristated	Enabled	Enabled	Disabled	Driven	Disabled		via DSKCHG			Disabled	Enabled	Tristated	Disabled (note)	Disabled	Disabled	Tristated	Disabled
FDCCS# Decode	IDECSx# Decode	State of SD7 (output)	State of XBUSOE#																								
Enabled	Enabled	Tristated	Enabled																								
Enabled	Disabled	Driven	Disabled																								
	via DSKCHG																										
Disabled	Enabled	Tristated	Disabled (note)																								
Disabled	Disabled	Tristated	Disabled																								
DLIGHT#/ PIRQ0#			<p>DLIGHT#/ PIRQ0# out Hard Disk Activity Light/PCI Interrupt Request 0: This signal has two functions depending on the programming of the Mode Select Register. As DLIGHT#, this signal controls the hard disk X light. When low, the light is on. When high, the light is off. If either bit 6 or bit 7 of the Port 92 register is set to a 1 (bit 6 and 7 are internally NOR'ed together), DLIGHT# is driven active (low). Setting both bits 6 and 7 low causes DLIGHT# to be driven high. For the PIRQ0# function, see the Mode Select Register description. For the PIRQ0# function, an external pull-up resistor (10-20 KΩ) must be added to this signal.</p>																								

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
Integrated Logic Signals			
Configuration RAM Interface			
CRAMRD#	164	out	Configuration RAM Read Command: CRAMRD# connects directly to the system Configuration RAM. The ESC asserts CRAMRD# for I/O reads from the address range programmed into the low and high bytes of the configuration RAM command registers.
CRAMWR#	163	out	Configuration RAM Write Command: This is an active Low output. CRAMWR# is connected directly to the system Configuration RAM. The ESC activates CRAMWR# for I/O writes to the address range programmed into the low and high bytes of the configuration RAM command registers.
X-bus Control and General Purpose Decode			
XBUST/R#	162	out	X-Bus Data Transmit/Receive: XBUST/R# is tied directly to the direction control of a 74F245 that buffers the X-bus data XD(7:0) from the system data bus SD(7:0). XBUST/R# is driven high (transmit) during I/O and memory reads for EISA and ISA masters. For DMA cycles (channel 2 only), XBUST/R# is driven high for the following cases: <ul style="list-style-type: none"> 1. Memory read, I/O write cycles where LBIOSCS# is asserted. 2. I/O read, memory write cycles where Digital Output Register bit 3 is set to 1. XBUST/R# is driven low (receive) under all other conditions.
DLIGHT# / PIRQ0#	165	out	Hard Disk Activity Light/PCI Interrupt Request 0: This signal has two functions, depending on the programming of the Mode Select Register. As DLIGHT#, this signal controls the hard disk X light. When low, the light is on. When high, the light is off. If either bit 6 or bit 7 of the Port 92 register is set to 1 (bit 6 and 7 are internally NOR'ed together), DLIGHT# is driven active (low). Setting both bits 6 and 7 low causes DLIGHT# to be driven high. For the PIRQ0# function, see the Mode Select Register description. For the PIRQ0# function, an external pull-up resistor (10-20 K Ω) must be added to this signal.

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
Integrated Logic Signals			
X-bus Control and General Purpose Decode			
XBUSOE#	161	out	<p>X-Bus Data Output Enable: XBUSOE# is tied directly to the output enable of a 74F245 that buffers the X-bus data XD(7:0) from the data bus SD(7:0). For EISA and ISA master memory read or write cycles, XBUSOE# is asserted when LBIOSCS# is asserted. Otherwise, XBUSOE# is not asserted. For EISA and ISA master I/O read or write cycles, SBUSOE# is asserted if an ISC-supported X-bus device has been decoded and the decoding for that device was enabled via the proper configuration registers. An exception to this is during an I/O read access to floppy location 3F7h (primary) or 377h (secondary) if the IDE decode space is disabled (i.e., IDE is not present on the X-bus).</p> <p>In this case, XBUSOE# is not asserted. XBUSOE# is also not asserted during an I/O access to the floppy controller if DSKCHG is sampled low at reset. XBUSOE# is not asserted during DMA cycles, except for channel 2 DMA. For channel 2 DMA, XBUSOE# is asserted.</p>
GPCS[2:0]# / ECS[2:0]	160:159, 155	out	<p>General Purpose Chip Select/Encoded Chip Select: These are dual-function signals. The function of these pins is selected through the Mode Select Register bit 4.</p> <p>General Purpose Chip Select: GPCS[2:0]# are chip selections for peripheral devices. These devices can be mapped to the I/O range by programming the General Purpose Chip Select Base Address registers and General Purpose Mask registers (offset 64h-6Eh).</p> <p>Encoded Chip Select: ECS[2:0] provide encoded chip select decoding for serial ports, parallel port, IDE and general purpose devices. The device chip selection for the peripheral devices are generated by using a F138 with ECSS2:01 as inputs.</p> <p>Hardware Reset (Test Mode, 82374SB only). During reset, GPCS0/ECS0 is an input signal. The level of this signal is sampled at the end of the reset sequence to determine whether the test pin is used as the current test function (sampled 1) or as the INIT signal (sampled 0). After reset, the existing GPCS/ECS functionality on this pin is determined. Make sure that the INIT mode on the TEST pin is selected and an external pull-down</p>

Table 2- 9 ESC (82374SB) Signal Descriptions

Signal	Pin	Type	Description
			(approximately 500Ω) is connected to the pin.
Test Signal			
INIT/TEST	154	in	Initialization Test: On the 82374SB, the DPCS0# pin value at reset selects the function of this pin. If GPCS0# is low, INIT is selected and if GPCS0# is high, TEST is selected. On the 82374EB, this pin only functions as a TEST pin. TEST is used to tristate all of the outputs. This signal should be tied to Vcc in normal operations and to ground in test mode.

2.8 PCI-EISA Bridge (82375SB)

The 82375EB/SB PCI-EISA Bridge (PCEB) provides the master/slave functions on both the PCI Local bus and the EISA bus. Functioning as a bridge between the PCI and EISA buses, the PCEB provides the address and data paths, bus controls, and bus protocol translation for PCI-to-EISA and EISA-to-PCI transfers. Extensive data buffering in both directions increases system performance by maximizing PCI and EISA bus efficiency and allowing concurrency on the two buses. The PCEB's buffer management mechanism ensures data coherency. The PCEB integrates central bus control functions including a programmable bus arbiter for the PCI bus and EISA data swap buffers for the EISA bus. Integrated system functions include PCI parity generation, system error reporting, and programmable PCI and EISA memory and I/O address space mapping and decoding. The PCEB also contains a BIOS Timer that can be used to implement timing loops. The PCEB is intended to be used with the EISA System Component (ESC) to provide an EISA I/O subsystem interface.

2.8.1 Features

- Provides the Bridge Between the PCI Local bus and EISA bus
- 100% PCI and EISA Compatible
 - PCI and EISA Master/Slave Interface
 - Directly Drives 10 PCI Loads and 8
 - EISA Slots
 - Supports PCI from 25 to 33 MHz
- Data Buffers Improve Performance
 - Four 32-bit PCI-to-EISA Posted Write Buffers
 - Four 16-byte EISA-to-PCI Read/Write Line Buffers
 - EISA-to-PCI Read Prefetch
 - EISA-to-PCI and PCI-to-EISA Write Posting
- Data Buffer Management Ensures Data Coherency
 - Flush Posted Write Buffers
 - Flush or Invalidate Line Buffers
 - System-Wide Data Buffer Coherency Control
- Burst Transfers on both the PCI and EISA buses
- 32-Bit Data Paths
- Integrated EISA Data Swap Buffers
- Arbitration for PCI Devices
 - Supports Six PCI Masters
 - Fixed, Rotating, or a Combination of the Two
 - Supports External PCI Arbiter and Arbiter Cascading

-
- PCI and EISA Address Decoding and Mapping
 - Positive Decode of Main Memory Areas (MEMCS# Generation)
 - Four Programmable PCI Memory Space Regions
 - Four Programmable PCI I/O Space Regions
 - Programmable Main Memory Address Decoding
 - Main Memory Sizes up to 512 MB
 - Access Attributes for 15 Memory Segments in First 1 MB of Main Memory
 - Programmable Main Memory Hole
 - Integrated 16-bit BIOS Timer

2.8.2 Block Diagram

82375SB : PCEB

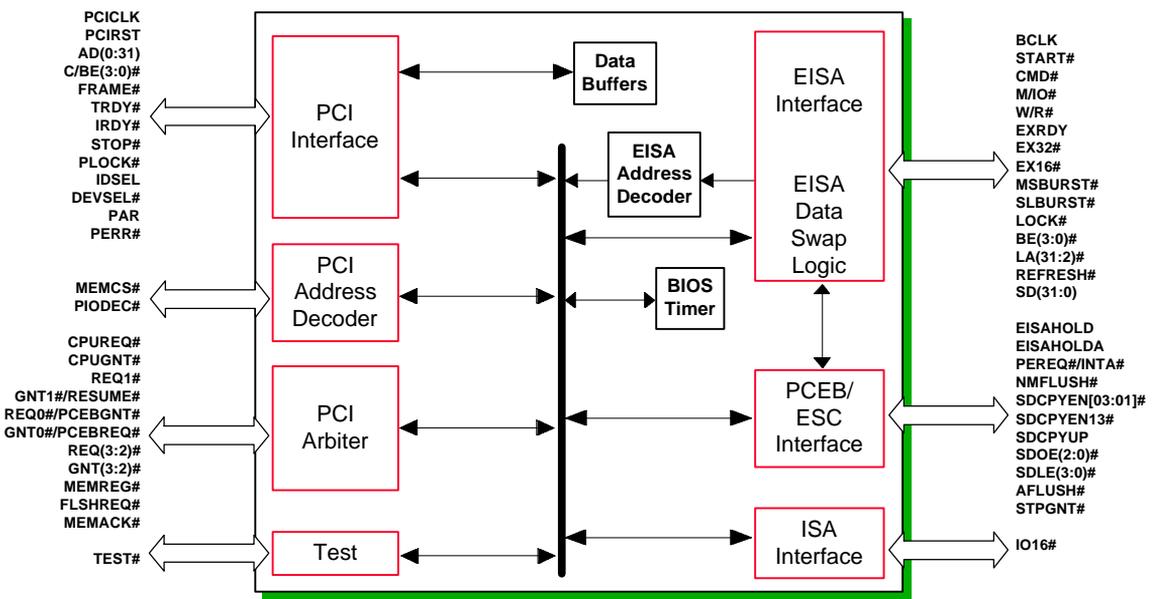


Figure 2- 13 PCEB (82375SB) Block Diagram

2.8.3 Pin Diagram

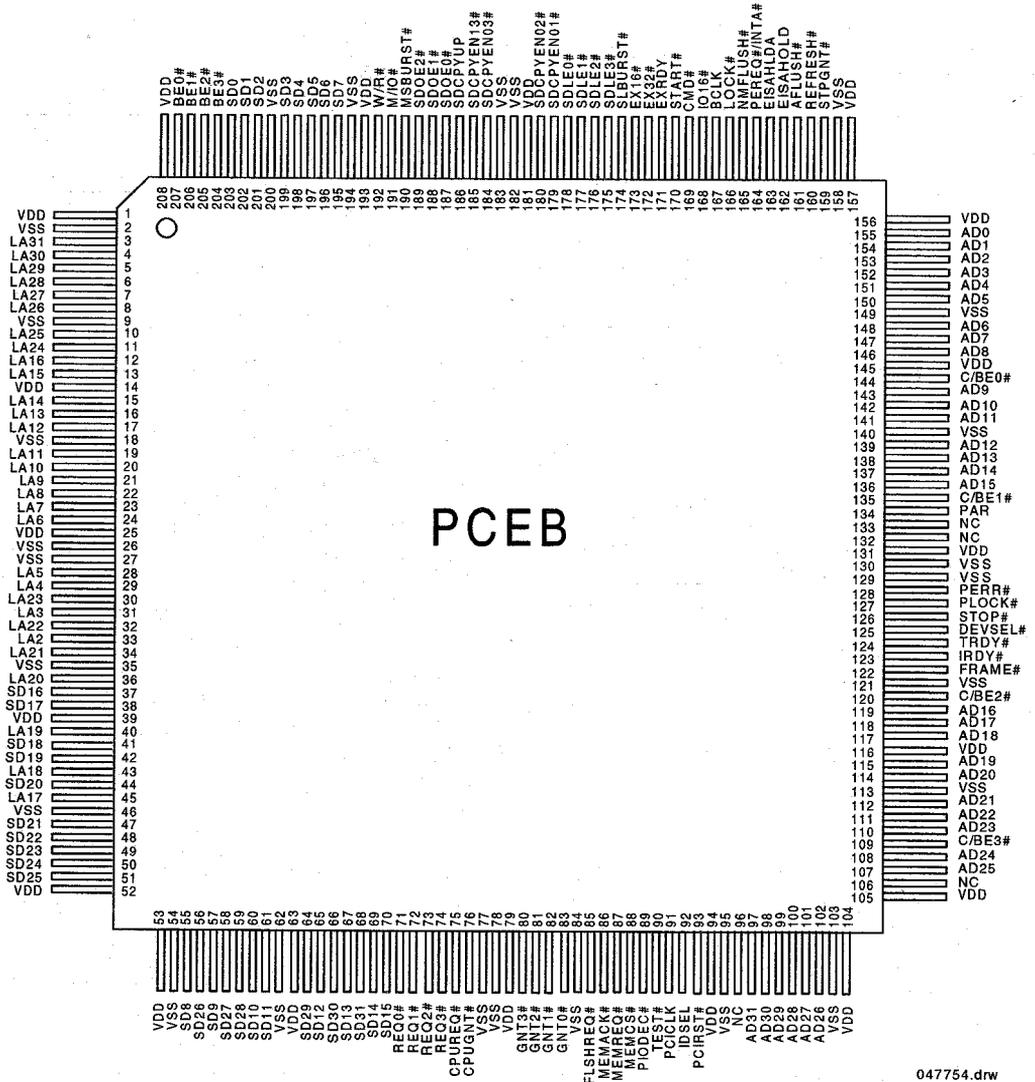


Figure 2- 14 PCEB (82375SB) Pin Diagram

2.8.4 Signal Descriptions

Table 2- 10 PCEB (82375SB) Signal Descriptions

Signal	Pin	Type	Description
PCI Bus Interface			
PCICLK	91	in	PCI Clock. PCICLK provides timing for all transactions on the PCI bus. All other PCI signals are sampled on the rising edge of PCICLK and all timing parameters are defined based on this edge. Frequencies supported by the PCEB range from 25 to 33 MHz.
PCI RST#	93	in	PCI Reset. PCIRST# forces the PCEB into a known state. All Vs and s/t/s signals are forced to a high impedance state, and the s/o/d signals are allowed to float high. The PCEB negates all GNT# lines to the PCI bus and the PCEB negates its internal request. The PCEB drives AD[31:0], C/BE[3:0]#, and PAR during reset to keep these signals from floating (depends on CPUREQ# and REQ1# state). As long as PCIRST# is asserted, the PCEB drives the AD[31:0] signals to keep them from floating. Note that CPUREQ# must be sampled high when PCIRST# is asserted. All PCEB registers are set to their default values. PCIRST# may be asynchronous to PCICLK when asserted or negated. Although asynchronous, the negation of PCIRST# must be a clean, bounce-free edge. PCIRST# must be asserted for a minimum 1 μ s, and the PCICLK must be active during the last 100 μ s of the PCIRST# pulse.
AD[31 :0]	97:102, 107, 108, 110:112, 114, 115, 117:119, 136:139, 141:143, 146:148, 150:155	t/s	Address and Data. AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address. During subsequent clocks, AD[31:01] contain data. A PCEB bus transaction consists of an address phase followed by one or more data phases. Little-end and byte ordering is used. AD[7:0] define the least significant byte (LSB) and AD[31:24] the most significant byte (MSB). The information in the two low order address bits varies by address space. In the I/O address space, AD[1:0] provide full-byte address. In the memory and configuration address space, AD[1:0] are driven 00 during the address phase. The other three encodings are reserved.

Table 2- 10 PCEB (82375SB) Signal Descriptions

Signal	Pin	Type	Description
PCI Bus Interface			
AD[31 :0] continued	97:102, 107, 108, 110:112, 114, 115, 117:119, 136:139, 141:143, 146:148, 150:155	t/s	<p>When the PCEB is a target, AD[31:0] are inputs during the address phase of a transaction. During the following data phase(s), the PCEB may be asked to supply data on AD[31:0] as for a PCI read, or accept data as for a PCI write. As an Initiator, the PCEB drives a valid address on AD[31:0] (with exceptions related to AD[1:0]) during the address phase, and drives write or latches read data on ADf31:01 during the data phase.</p> <p>When PCIRST# is asserted, the PCEB drives the AD[31:0] signals to keep them from floating. In addition, the PCEB acts as the central resource responsible for driving the AD[31:0] signals when no device owns the PCI bus and the bus is idle.</p>
C/BE13:01#	109, 120, 135, 144	t/s	<p>Bus Command and Byte Enables. The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command for bus command definitions. During the data phase, C/BE[3:0]# are used as Byte Enables. The Byte Enables determine which byte lanes carry meaningful data. C/BE[0]# applies to byte 0 and C/BE[3]# to byte 3. C/BE[3:0]# are not used for address decoding. The PCEB drives C/BE[3:0]# as an initiator of a PCI bus cycle and monitors C/BE[3:0]# as a target.</p> <p>When PCIRST# is asserted, the PCEB drives C/BE[3:0]# to keep them from floating. In addition, the PCEB acts as the central resource responsible for driving the C/BE[3:0]# signals when no device owns the PCI bus and the bus is idle.</p>
FRAME#	122	s/t/s	<p>Frame. FRAME# is driven by the current initiator to indicate the beginning and duration of an access. FRAME# is asserted to indicate that a bus transaction is beginning. During a transaction, data transfers continue while FRAME# is asserted. When FRAME# is negated, the transaction is in the final data phase. FRAME# is an input when the PCEB is the target. FRAME# is an output when the PCEB is the initiator. During reset, this signal is tristated.</p>

Table 2- 10 PCEB (82375SB) Signal Descriptions

Signal	Pin	Type	Description
PCI Bus Interface			
TRDY#	124	s/t/s	Target Ready. TRDY#, as an output, indicates the target's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock that both TRDY# and IRDY# are sampled asserted. When PCEB is the target during a read cycle, TRDY# indicates that the PCEB has valid data present on AD[31:0]. During a write, it indicates that the PCEB, as a target, is prepared to latch data. TRDY # is an input to the PCEB when the PCEB is the initiator. This signal is tristated during reset.
IRDY#	123	s/t/s	Initiator Ready. IRDY#, as an output, indicates the initiator's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock that both IRDY# and TRDY# are sampled asserted. When PCEB is the initiator of a write cycle, IRDY# indicates that the PCEB has valid data present on AD[31:0]. During a read, it indicates the PCEB is prepared to latch data. IRDY# is an input to the PCEB when the PCEB is the target. This signal is tristated during reset.
STOP#	126	s/t/s	Stop. As a target, the PCEB asserts STOP# to request that the master stop the current transaction. When the PCEB is an initiator, STOP# is an input. As an initiator, the PCEB stops the current transaction when STOP# is asserted. Different semantics of the STOP# signal are defined in the context of other handshake signals (TRDY# and DEVSEL#). This signal is tristated during reset.
PLOCK#	127	s/t/s	PCI Lock. PLOCK# indicates an atomic operation that may require multiple transactions to complete. PLOCK# is an input when PCEB is the target and output when PCEB is the initiator. When PLOCK# is sampled negated during the address phase of a transaction, a PCI agent acting as a target considers itself a locked resource until it samples PLOCK# and FRAME# negated. When other masters attempt accesses to the PCEB (particularly to the EISA subsystem) while the PCEB is locked, the PCEB responds with a retry termination. This signal is tristated during reset.

Table 2- 10 PCEB (82375SB) Signal Descriptions

Signal	Pin	Type	Description
PCI Bus Interface			
IDSEL	92	in	Initialization Device Select. IDSEL is used as a chip select during configuration read and write transactions. The PCEB samples IDSEL during the address phase of a transaction. If the PCEB samples IDSEL asserted during a configuration read or write, the PCEB responds by asserting DEVSEL# in the next cycle.
DEVSEL#	125	s/t/s	Device Select. The PCEB asserts DEVSEL# to claim a PCI transaction as a result of positive or subtractive decode. As an output, the PCEB asserts DEVSEL# when it samples IDSEL asserted during configuration cycles to PCEB configuration registers. As an input, DEVSEL# indicates the response to a PCEB-initiated transaction. When PCE1N is not a master, it samples this signal for all PCI transactions to decide whether to subtractively decode the cycle (except for configuration and special cycles). This signal is tristated during reset.
PAR	134	t/s	Parity. PAR is even parity across AD[31:0] and C/BE[3:0]#. When acting as a master, the PCEB drives PAR during the address and write data phases. As a target, the PCEB drives PAR during read data phases. When PCIRST# is asserted, the PCEB drives the PAR signal to keep it from floating. The PCEB acts as the central resource responsible for driving the PAR signal when no other device is granted the PCI bus and is idle. The driving and tristating of the PAR signal is always one clock delayed from the corresponding driving and tristating of the AD[31:0] and C/BE[3:0]# signals.
PERR#	128	s/t/s	Parity Error. PERR# reports data parity errors on all transactions, except special cycles. This signal can only be asserted (by the agent receiving data) two clocks following the data (which is one clock following the PAR signal that covered the data). The duration of PERR# is one clock for each data phase that a data parity error is detected. If multiple data errors occur during a single transaction the PERR# signal is asserted for more than a single clock. PERR# must be driven high for one clock before being tristated. This signal is tristated during reset.

Table 2- 10 PCEB (82375SB) Signal Descriptions

Signal	Pin	Type	Description															
PCI Arbiter Signals																		
CPUREQ#	75	in	CPU Request. CPUREQ# asserted indicates that the Host CPU requests use of the PCI bus. During PCIRST#, this signal must be sampled high by the PCEB. When PCIRST# is asserted (and CPUREQ# is sampled high), the PCEB drives the AD, C/BE#, and PAR signals to keep them from floating.															
REQ[3:0]#	74:71	in	Request. A bus master asserts the corresponding request signal to request the PCI bus.															
CPUGNT#	76	out	CPU Grant. The PCEB asserts CPUGNT# to indicate that the CPU master (Host Bridge) has been granted the PCI bus. During PCI reset, CPUGNT# is tristated.															
GNT[3:0]#	80:83	out	Grant. The PCEB asserts one of the GNT[3:0] signals to indicate that the corresponding PCI master has been granted the PCI bus. During PCI reset, these signals are tristated.															
MEMREQ#	87	out	Memory Request. If the PCEB is configured in Guaranteed Access Time (GAT) Mode, MEMREQ# is asserted when an EISA device or DMA requests the EISA bus. The PCEB asserts this signal (along with FLSHREQ#) to indicate that the PCEB requires ownership of main memory. The PCEB asserts FLSHREQ# concurrently with asserting MEMREQ#. This signal is synchronous to the PCI clock. During reset, this signal is driven.															
MEMREQ# continued	87	out	<table border="1"> <thead> <tr> <th>FLSHREQ#</th> <th>MEMREQ#</th> <th>Meaning</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>Idle</td> </tr> <tr> <td>0</td> <td>1</td> <td>Flush buffers pointing towards PCI to avoid ISA deadlock</td> </tr> <tr> <td>1</td> <td>0</td> <td>GAT enabled or disabled: For buffer coherency in APIC systems, the buffers pointing to main memory must be flushed and disabled for the duration of assertion.</td> </tr> <tr> <td>0</td> <td>0</td> <td>GAT mode: Guarantee PCI bus immediate access to main memory (this may or may not require the PCI-to-main memory buffers to be flushed first, depending on the number of buffers).</td> </tr> </tbody> </table>	FLSHREQ#	MEMREQ#	Meaning	1	1	Idle	0	1	Flush buffers pointing towards PCI to avoid ISA deadlock	1	0	GAT enabled or disabled: For buffer coherency in APIC systems, the buffers pointing to main memory must be flushed and disabled for the duration of assertion.	0	0	GAT mode: Guarantee PCI bus immediate access to main memory (this may or may not require the PCI-to-main memory buffers to be flushed first, depending on the number of buffers).
FLSHREQ#	MEMREQ#	Meaning																
1	1	Idle																
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0	0	GAT mode: Guarantee PCI bus immediate access to main memory (this may or may not require the PCI-to-main memory buffers to be flushed first, depending on the number of buffers).																

Table 2- 10 PCEB (82375SB) Signal Descriptions

Signal	Pin	Type	Description
PCI Arbiter Signals			
FLSHREQ#	85	out	<p>Flush Request. FLSHREQ# is asserted by the PCEB to command all of the system's posted write buffers pointing towards PCI to be flushed. This is required before granting the EISA bus to an EISA master or the DMA. Note that, for APIC related buffer flush requests, this signal is negated. This signal is synchronous to the PCI clock. During reset, this signal is driven high.</p>
MEMACK#	86	in	<p>Memory Acknowledge. MEMACK# is the response handshake that indicates to the PCEB that the function requested over the MEMREQ# and/or FLSHREQ# signals has been completed.</p> <p>If the PCEB is configured for Guaranteed Access Time Mode through the Arbiter Control Register, and both MEMREQ# and FLSHREQ# are asserted, the assertion of MEMACK# indicates to the PCEB that ownership of main memory has been granted and that all system buffers have been flushed and temporarily disabled.</p> <p>If MEMACK# is asserted in response to assertion of MEMREQ# (GAT either enabled or disabled), it indicates that the system's buffers pointing toward the main memory are flushed and temporarily disabled so that APIC can proceed with the interrupt message sequence.</p> <p>If FLSHREQ# is asserted and MEMREQ# is not asserted (with GAT mode being either enabled or disabled), the assertion of MEMACK# indicates that the system's posted write buffers pointing towards PCI are flushed and temporarily disabled, and the EISA bus can be granted to an EISA master or DMA. This signal is synchronous to the PCI clock.</p>

Table 2- 10 PCEB (82375SB) Signal Descriptions

Signal	Pin	Type	Description
Address Decoder Signals			
MEMCS#	88	out	Memory Chip Select. MEMCS# is a programmable address decode signal provided to a Host CPU bridge. A Host bridge can use MEMCS# to forward a PCI cycle to the main memory behind the bridge. MEMCS# is asserted one PCI clock after FRAME# is sampled asserted (address phase) and is valid for one clock cycle before being negated. MEMCS# is driven high during reset.
PIODEC#	89	in	PCI I/O Space Decoder. PIODEC# can be used to provide arbitrarily complex EISA-to-PCI I/O address space mapping. This signal can be connected to the decode select output of an external I/O address decoder. When PIODEC# is asserted during an EISA I/O cycle, that cycle is forwarded to the PCI bus. An external pull-up resistor is required if this input signal is not used (i.e., not driven by the external logic).
EISA Interface			
BCLK	167	in	Bus Clock. BCLK is the system clock used to synchronize events on the EISA bus. The ESC device generates BCLK (BCLKOUT), which is a divided down clock from a PCICLK. BCLK runs at a frequency that is dependent on PCICLK and a selected division factor (within the ESC). For example, a 25 MHz PCICLK and a division factor of 3 results in an 8.33 MHz BCLK.
START#	170	t/s	Start. START# provides timing control at the start of the cycle and remains asserted for one BCLK period. When the PCEB is an EISA master, START# is an output signal. START# is asserted after LA[31:24]#, LA[23:2] and M/IO# become valid. START# is negated on the rising edge of the BCLK, one BCLK after it was asserted. The trailing edge of START# is always delayed from the rising edge of BCLK. When the PCEB is an EISA master, for cycles to a mismatched slave (see note at the end of this section), START# becomes an input signal at the end of the first START# phase and remains an input until the negation of the last CMD#. The ESC gains the control of the transfer and generates START#. When the PCEB is an EISA slave, START# is an input signal. It is sampled on the rising edge of BCLK. Upon PCIRST#, this signal is tristated and

Table 2- 10 PCEB (82375SB) Signal Descriptions

Signal	Pin	Type	Description
			placed in output mode.
EISA Interface			
CMD#	169	in	Command. CMD# provides timing control within the cycle. In all cases, CMD# is an input to the PCEB from the ESC. CMD# is asserted from the rising edge of BCLK, simultaneously with the negation of START#, and remains asserted until the end of the cycle.
M/IO#	191	t/s	Memory or I/O. M/IO# identifies the current cycle as a memory or an I/O cycle. M/IO# is pipelined from one cycle to the next and must be latched by the slave. M/IO# = 1 indicates a memory cycle and M/IO# = 0 indicates an I/O cycle. When the PCEB is an EISA master, the M/IO# is an output signal. When the PCEB is an EISA slave, M/IO# is an input signal. The PCEB responds as an EISA slave for both memory and I/O cycles. Upon PCIRST#, this signal is tristated and is placed in output mode.
W/R#	192	t/s	Write or Read. W/R# identifies the cycle as a write or a read cycle. The W/R# signal is pipelined from one cycle to the next and must be latched by the slave. W/R# = 1 indicates a write cycle and W/R# = 0 indicates a read cycle. When the PCEB is an EISA master, W/R# is an output signal. When the PCEB is an EISA slave, W/R# is an input signal. Upon PCIRST#, this signal is tristated and placed in output mode.
EXRDY	171	od	EISA Ready. EXRDY is used by EISA I/O and memory slaves to request wait states during a cycle. Each wait state is a BCLK period. The PCEB, as an EISA master or slave, samples EXRDY. As an input, the EXRDY is sampled on the falling edge of BCLK after the CMD# has been asserted, and if inactive, each falling edge thereafter. When PCEB is an EISA slave, it may drive EXRDY low to introduce wait states. During reset, this signal is not driven.

Table 2- 10 PCEB (82375SB) Signal Descriptions

Signal	Pin	Type	Description
EISA Interface			
EX32#	172	od	<p>EISA 32-bit. EX32# is used by the EISA slaves to indicate support of 32 bit transfers. When the PCEB is an EISA master, it samples EX32# on the same rising edge of BCLK that START# is negated.</p> <p>During mismatched cycles (see note at the end of this section), EX32# (and EX16#) is used to transfer the control back to the PCEB. EX32# (along with EX16#) is asserted by the ESC on the falling edge of BCLK before the rising edge of the BCLK when the last CMD# is negated. This indicates that the cycle control is transferred back to the PCEB.</p> <p>As an EISA slave, the PCEB always drives EX32# to indicate 32-bit support for EISA cycles. During reset, this signal is not driven.</p>
EX16#	173	in	<p>EISA 16-bit. EX16# is used by the EISA slaves to indicate their support of 16-bit transfers. As an EISA master, the PCEB samples EX16# on the same rising edge of BCLK that START# is negated.</p> <p>During mismatched cycles (see note at the end of this section), EX16# (and EX32#) is used to transfer the control back to the PCEB. EX16# (along with EX32#) is asserted by the ESC on the falling edge of the BCLK before the rising edge of the BCLK when the last CMD# is negated. This indicates that the cycle control is transferred back to the PCEB.</p> <p>As an EISA slave, the PCEB never asserts EX16#.</p>
MSBURST#	190	t/s	<p>Master Burst. MSBURST# is an output when the PCEB is an EISA master and an input when the PCEB is a slave.</p> <p>As a master, the PCEB asserts MSBURST# to indicate to the slave that the next cycle is a burst cycle. If the PCEB samples SLBURST# asserted on the rising edge of BCLK after START# is asserted, the PCEB asserts MSBURST# on the next BCLK edge and proceeds with the burst cycle.</p> <p>As a slave, the PCEB monitors this signal in response to the PCEB asserting SLBURST#. The EISA master asserts MSBURST# to the PCEB to indicate that the next cycle is a burst cycle. As a slave, the PCEB samples MSBURST# on the rising edge of BCLK after the rising edge of BCLK that CMD# is asserted by the ESC. MSBURST# is sampled on all subsequent rising edges of BCLK until</p>

Table 2- 10 PCEB (82375SB) Signal Descriptions

Signal	Pin	Type	Description
			the signal is sampled negated.
EISA Interface			
MSBURST# continued	190	t/s	The burst cycle is terminated on the rising edge of BCLK when MSBURST# is sampled negated, unless EXRDY is sampled negated on the previous falling edge of BCLK. During reset, this signal is tristated.
SLBURST#	174	t/s	<p>Slave Burst. SLBURST# is an input when the PCEB is an EISA master and an output when the PCEB is a slave.</p> <p>When the PCEB is a master, the slave indicates that it supports burst cycles by asserting SLBURST# to the PCEB. The PCEB samples SLBURST# on the rising edge of BCLK at the end of START# for EISA master cycles.</p> <p>When the PCEB is an EISA slave, this signal is an output. As a slave, the PCEB asserts this signal to the master indicating that the PCEB supports EISA burst cycles. During reset, this signal is tristated.</p>
LOCK#	166	t/s	<p>Lock. When asserted, LOCK# guarantees exclusive memory access. This signal is asserted by the PCEB when the PCI master is running locked cycles to EISA slaves., When asserted, this signal locks the EISA subsystem.</p> <p>LOCK# can also be activated by a device on the EISA bus. This condition is propagated to the PCI bus via the PLOCK# signal. During reset, this signal is tristated</p>
BE[3:0]#	204:207	t/s	<p>Byte Enables. BE[3:0]# identify the specific bytes that are valid during the current EISA bus cycles. When the PCEB is an EISA master and the cycles are directed to a matched slave (slave supports 32-bit transfers), the BE[3:0]# are outputs from the PCEB.</p> <p>When the cycles are directed to a mismatched slave (slave does not support 32-bit transfers), the BE[3:0]# are floated one and half BCLKs after START# is asserted. These signals become inputs (driven by the ESC) for the rest of the cycle.</p> <p>BE[3:0]# are pipelined signals and must be latched by the addressed slave. When the PCEB is an EISA/ISA/DMA slave, BE[3:0]# are inputs to the PCEB.</p> <p>Upon PCIRST#, these signals are tristated and placed in output mode.</p>

Table 2- 10 PCEB (82375SB) Signal Descriptions

Signal	Pin	Type	Description
EISA Interface			
LA[31 :24]#, LA[23:2]	3:8, 10, 11, 30, 32, 34, 36, 40, 43, 45, 12, 13, 15:17, 19:24, 28, 29, 31, 33	t/s	<p>Latchable Address. LA[31:24]# and LA[23:2] are the EISA address signals. When the PCEB is an EISA master, these signals are outputs from the PCEB. These addresses are pipelined and must be latched by the EISA slave. LA[31:24]# and LA[23:2] are valid on the falling edge of START#. The upper address bits are inverted before being driven on LA[31:24]#. The timing for LA[31:24] and LA[23:2] are the same. When the PCEB is an EISA slave, these signals are inputs and are latched by the PCEB.</p> <p>For I/O cycles, the PCEB, as an EISA master, floats LA[31:24]# to allow for ESC address multiplexing (during I/O cycle to configuration RAM). LA[23:2] are actively driven by the PCEB. For memory cycles, the PCEB as an EISA master, drives the LA address lines. These signals are tristated during reset.</p>
SD[31:0]	68, 66, 64, 59, 58, 56, 51, 50:47, 44, 42, 41, 38, 37, 70, 69, 67, 65, 61, 60, 57, 55, 195:199, 201:203	t/s	<p>System data. SD[31:0] are bidirectional data lines that transfer data between the PCEB and other EISA devices. Data transfer between EISA and PCI devices use these signals. The data swapping logic in the PCEB ensures that the data is available on the correct byte lanes for any given transfer. These signals are tristated during reset.</p>
REFRESH#	160	in	<p>Refresh. When asserted, REFRESH# indicates to the PCEB that the current cycle on the EISA bus is a refresh cycle. It is used by the PCEB decoder to distinguish between EISA memory read cycles and refresh cycles.</p> <p>Note:</p> <p>Mismatched Cycles. When the PCEB is an EISA master, cycles to the slaves other than 32-bit transfers are considered a mismatched cycle. For mismatched cycles, the PCEB backs off the EISA bus one and half BCLKs after it asserted START# by releasing (floating) START#, BE[3:0]# and the SD[31:0] lines. The ESC device then takes control of the transfer until the last transfer. At the end of the last transfer, the ESC returns the control to the PCEB by asserting EX32# and EX16# on the falling edge of BCLK before the rising edge of BCLK when the last CMD# is negated.</p>

Table 2- 10 PCEB (82375SB) Signal Descriptions

Signal	Pin	Type	Description
ISA Interface			
IO16#	168	o/d	<p>16-bit I/O Chip Select. As an EISA slave, the PCEB asserts IO16# when PNODEC# is asserted or an I/O cycle to PCI is detected.</p> <p>As an EISA master, the PCEB uses IO16# as an input to determine the correct amount of I/O recovery time from the I/O Recovery Time (IORT) Register. This register contains bit-fields that are used to program recovery times for 8-bit and 16-bit I/O. When IO16# is asserted, the recovery time programmed into the 16-bit I/O field (bits [1:0]), if enabled, is used. When IO16# is negated, the recovery time programmed into the 8-bit I/O field (bits [5:3]), if enabled, is used. This signal must have an external pull-up resistor. This signal is not driven during reset.</p> <p>Note: An ISA interface signal is included to improve the PCEB's handling of I/O cycles on the EISA side of the bridge. This signal permits ISA masters to address PCI I/O slaves using the full 16-bit bus size. The signal also allows the PCEB to identify 8-bit I/O slaves for purposes of generating the correct amount of I/O recovery.</p>
PCEB/ESC Interface			
Arbitration and Interrupt Acknowledge Control			
EISAHOLD	163	in	<p>EISA Hold. ESC uses EISAHOLD to request control of the EISA bus from the PCEB. This signal is synchronous to PCICLK and is driven inactive when PCIRST# is asserted.</p>
EISAH LDA	162	out	<p>EISA Hold Acknowledge. The PCEB asserts EISAH LDA to inform the ESC that it has been granted ownership of the EISA bus. This signal is synchronous to the PCICLK.</p>
PEREQ#/ INTA#	164	out	<p>PCI-to-EISA Request or Interrupt Acknowledge: PEREQ#/INTA# is a dual-function signal. The signal function is determined by the state of EISAH LDA signal.</p> <p>When EISAH LDA is negated, this signal is an interrupt acknowledge (i.e. PEREQ#/INTA# asserted indicates to the ESC that the current EISA cycle is an interrupt acknowledge).</p>
PEREQ#/ INTA# continued	164	out	<p>When EISAH LDA is asserted, this-signal is a PCI-to-EISA request (i.e. PEREQ#ANTA# asserted indicates to the ESC that the PCEB needs to obtain the ownership of the EISA bus on behalf of a PCI agent).</p> <p>This signal is synchronous to the PCICLK and it is driven inactive when PCIRST# is</p>

Table 2- 10 PCEB (82375SB) Signal Descriptions

Signal	Pin	Type	Description
			asserted.
PCEB/ESC Interface			
Arbitration and Interrupt Acknowledge Control			
STPGNT#	159	out	Stop Grant Acknowledge. STPGNT# is asserted when the PCEB receives a STOP GRANT PCI special cycle for one PCICLK period. This signal is only asserted when the PCI AD[31:0] signals equal 00120002h during the first data phase of the PCI special cycle. Data of 0012000sh on AC[31:0] in subsequent data phases during a PCI special cycle does not result in the assertion of STPGNT#.
PCEB Buffer Coherency Control			
NMFLUSH#	165	t/s	<p>New Master Flush. The bidirectional NMFLUSH# signal provides handshake between the PCEB and ESC to control flushing of PCI system buffers on behalf of EISA masters.</p> <p>During an EISA bus ownership change, before the ESC can grant the bus to the EISA master (or DMA), the ESC must ensure that system buffers are flushed and the buffers pointing towards the EISA subsystem are disabled. The ESC asserts NMFLUSH# for one PCI clock to request system buffer flushing. (After asserting NMFLUSH# for 1 PCI clock, the ESC tristates NMFLUSH#.) When the PCEB samples NMFLUSH# asserted, it starts immediately to assert NMFLUSH# and begins flushing its internal buffers, if necessary. The PCEB also requests PCI system buffer flushing via the MEMREQ#. FLSHREQ#. and MEMACK# signals.</p> <p>When the PCEB completes its internal buffer flushing and MEMACK# is asserted (indicating that the PCI system buffer flushing is complete), the PCEB negates NMFLUSH# for 1 PCI clock and stops driving it. When the ESC samples NMFLUSH# negated, it grants the EISA bus to an EISA master (or DMA). The ESC resumes responsibility of the default NMFLUSH# driver and starts driving NMFLUSH# negated until the next time a new EISA master (or DMA) wins arbitration.</p> <p>This signal is synchronous with PCICLK and is negated by the ESC at rs3S.</p>
AFLUSH#	161	t/s	APIC Flush. AFLUSH# is bidirectional signal between the PCEB and ESC that controls system buffer flushing on behalf of the APIC. After a reset the ESC negates AFLUSH# until the APIC is initialized and the first interrupt

Table 2- 10 PCEB (82375SB) Signal Descriptions

Signal	Pin	Type	Description
			request is recognized.
PCEB/ESC Interface			
Data Swap Buffer Control			
SDCPYEN01# SDCPYEN02# SDCPYEN03# SDCPYEN13#	185, 184, 180, 179	in	<p>Copy Enable. These active Low signals perform byte copy operation on the EISA data bus (SD[31:0]). The copy enable signals are asserted during mismatched cycles and are used by the PCEB to enable byte copy operations between the SD data byte lanes 0, 1, 2, and 3 as follows:</p> <p>SDCPYEN01#: Copy between Byte Lane 0 SD[7:0] and Byte Lane 1 SD[15:8]</p> <p>SDCPYEN02#: Copy between Byte Lane 0 SD[7:0] and Byte Lane 2 SD[23:16]</p> <p>SDCPYEN03#: Copy between Byte Lane 0 SD[7:0] and Byte Lane 3 SD[31:24]</p> <p>SDCPYEN13#: Copy between Byte Lane 1 SD[15:8] and Byte Lane 3 SD[31:24]</p> <p>Note that SDCPYUP controls the direction of the copy.</p>
SDCPYUP	186	in	<p>System Data Copy Up. SDCPYUP controls the direction of the byte copy operation. A high on SDCPYUP indicates a COPY UP operation where the lower byte(s) of the SD data bus are copied onto the higher byte(s) of the bus. A low on the signal indicates a COPY DOWN operation where the higher byte(s) of the data bus are copied on to the lower byte(s) of the bus. The PCEB uses this signal to perform the actual data byte copy operation during mismatched cycles.</p>
SDOE[2:0]#	189:187	in	<p>System Data Output Enable. These active Low signals enable the SD data output onto the EISA bus. The ESC only activates these signals during mismatched cycles. The PCEB uses these signal to enable the SD data buffers as follows:</p> <p>SDOE0# Enables byte lane 0 SD[7:0]</p> <p>SDOE1# Enables byte lane 1 SD[15:8]</p> <p>SDOE2# Enables byte lane 3 SD[31:24] and byte lane 2 SD[23 16]</p>

Table 2- 10 PCEB (82375SB) Signal Descriptions

Signal	Pin	Type	Description
PCEB/ESC Interface			
Data Swap Buffer Control			
SDLE[3:0]#	175:178	in	<p>System Data Latch Enable. SDLE[3:0]# enable the latching of data on the EISA bus. These signals are activated only during mismatched cycles, except PCEB-initiated write cycles. The PCEB uses these signals to latch the SD data bus as follows:</p> <p>SDLE0# Latch byte lane 0 SD[7:0] SDLE1# Latch byte lane 1 SD[15:8] SDLE2# Latch byte lane 2 SD[23:16] SDLE3# Latch byte lane 3 SD[31:24]</p>
Test			
TEST#	90	in	<p>TEST: This pin is used to tristate all PCEB outputs. During normal operations, this pin must be tied high.</p>

2.9 SCSI Controller (AIC 7880)

The AIC-7880 provides advanced host adapter features in a single chip with a SCSI-2 bus controller and a full featured PCI 32-bit bus master with zero wait state transfer capability including PCI enhanced data transfer commands. The AIC-7880 chip incorporates a dedicated processor, the SCSI PhaseEngine™ (RISC Sequencer), which executes a SCSI command described by a Sequencer Control Block (SCB). Sixteen SCBs may be stored in the internal SCB Array and with the addition of an external SRAM, a maximum of 256 SCBs may be stored for execution. These SCBs are executed independently of the SCSI target ID in the order that they are received. The SCB is a data structure which contains all information necessary for the execution of the command. The sequencer in the chip handles all phases of the SCSI bus, including the Disconnect/ Reconnect and Command Complete message. On the PCI host side, bus master transfers are made in a 64-bit address space at up to the maximum burst rate of 133 MB/ sec with data buffering of 256 bytes.

The AIC-7880 also provides a memory port for external access, an 8-bit ROM/EEPROM (for add-in card local BIOS support), a serial 1-bit EEPROM (for nonvolatile SCSI bus device and parameter storage, and/or adapter board assembly/serial/revision information), an 8/9-bit SRAM (for SCB expansion), and external board logic control.

2.9.1 Features

- Automatic data threshold selection
- Power-down modes
- Scatter/Gather operations supported
- Extremely low SCSI command overhead
- Data residue reported on underruns
- One interrupt per command completion, multiple command completion may be queued on a single interrupt
- Queued commands per Target/LUN
- Overlapped command execution
- Modify Data Pointers message handled
- Tagged Queuing supported
- SCSI Configured AutoMagically (SCAM level 1 support)
- Data path from PCI bus to SCSI bus internally byte parity protected
- Hardware address breakpoint capability for software debug
- External BIOS ROM option with in-place BIOS update (EEPROM) capability
- Device ID option for exchanging internal default value with an external value
- External Board Control option for controlling host adapter logic external to the AIC-7880 from the PCI bus

SCSI Features

- Fast (10 MHz) data transfers
- Wide data transfers
- Differential controls
- Flexible configuration
 - One 8-bit Single-ended, Fast
 - One 8-bit Differential, Fast
 - One 16-bit Single-ended, Fast
 - One 16-bit Differential, Fast
- Auto SCSI bus PIO
- Wide data connector indicator
- LED indicator control (SCSI busy, diagnostics, external ID clock) or general purpose control
- Selectable SCSI output active negation
- SCSI termination power down control or general purpose control
- SCAM level 1 support
- Digital filtering for incoming REQ and ACK signals

PCI 32-bit Interface

- Direct pin out connection to PCI 32-bit bus interface
- PCI bus master with zero wait state 32-bit memory data transfers at 133 MB/sec, capable of leading and trailing 32-bit boundary offset bytes, with a 32-bit address range within a selected 64-bit address page
- Supports both PCI single and dual address cycles
- PCI bus master/slave timing referenced to PCI signal PCLK (33.3 MHz max.)
- Buffered PCI signal PCLK output for adapter card logic usage
- PCI bus master programmable Latency Timer, Cache Size, and Interrupt Line Select registers
- PCI bus access of AIC-7880 device registers from both PCI I/O and memory address spaces
- Supports exchange of internal device ID default value with an external value
- Supports medium PCI target device-select response time
- Supports enhanced PCI system memory data Read and Write commands
- Cache line streaming capability
- Supports PCI bus address and data parity generation and checking

-
- Supports PCI PERR and SERR requirements
 - Supports 32-bit external ROM read access
 - Data transfers may be selected to be initiated by CACHESIZE or data level thresholds
 - Data FIFO data flush for transfers to system memory
 - IRQA# interrupt generation .from hardware, firmware and software controlled sources
 - Supports reduced power requirements when not performing master data transfers

Data Buffer

- Data FIFO provides 256 bytes of storage, dual-ported RAM, with parity per byte
- Programmable data and cache size threshold levels to initiate PCI bus master requests
- Early FIFO full status
- Multi byte-width data ports: 8 (PCI), 2 (SCSI), 1 (sequencer or driver) byte with byte parity
- Byte write parity generation and byte read parity checking
- Read/write capable address counters
- Partial quad-word detection and adjustment
- Starting address byte offset capable

Scratch RAM

- 64 bytes of dual-ported SRAM, accessible by sequencer and host drivers
- Byte parity protected

Sequencer (SCSI PhaseEngine)

- RISC instruction per clock design
- Clock rate selectable for 8 or 10 MHz operation
- SRAM microcode storage, 512 29-bit words plus byte parity
- Sixteen instruction group types
- Operation may be paused by maskable interrupt condition or software driver
- Diagnostic single-step and address breakpoint
- SLEEP mode for chip power reduction

2.9.2 Block Diagram

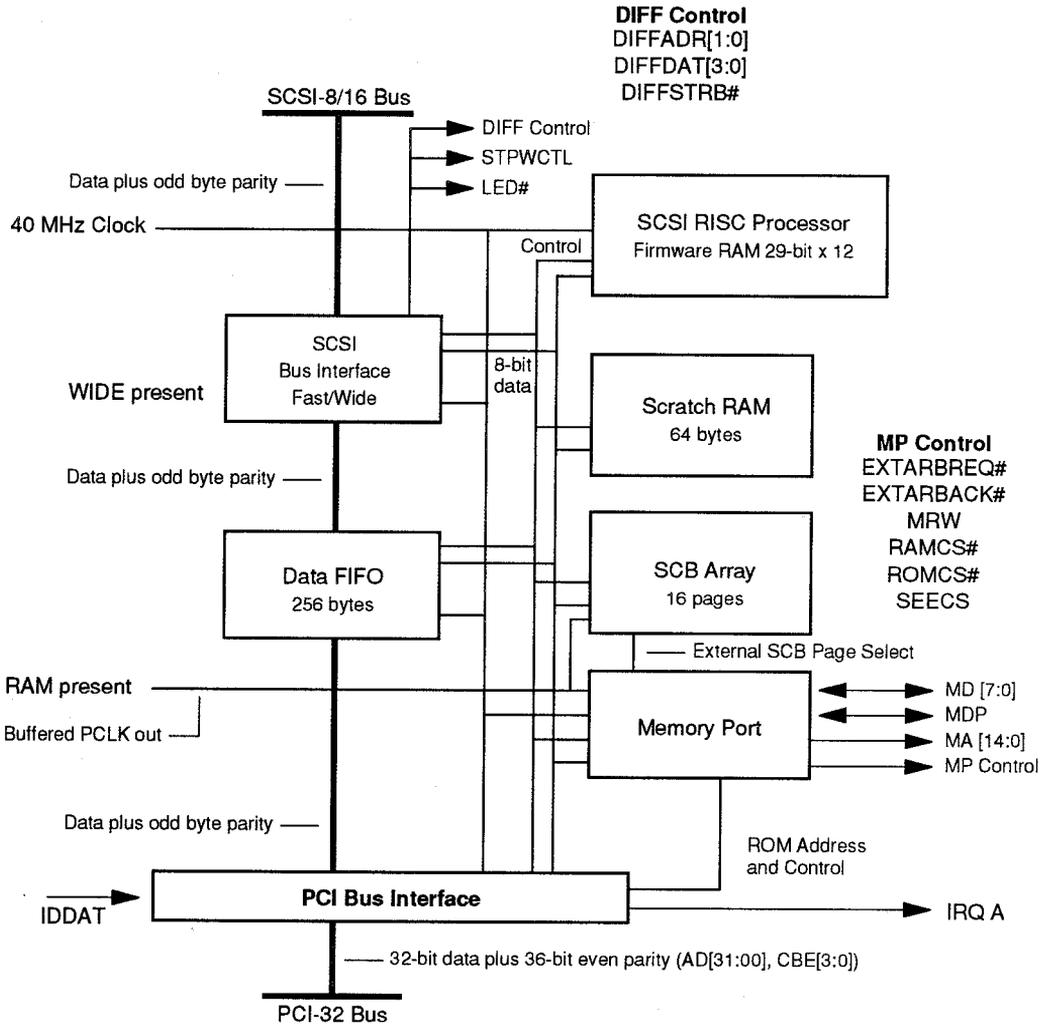


Figure 2- 15 AIC 7880 Block Diagram

2.9.3 Pin Diagram

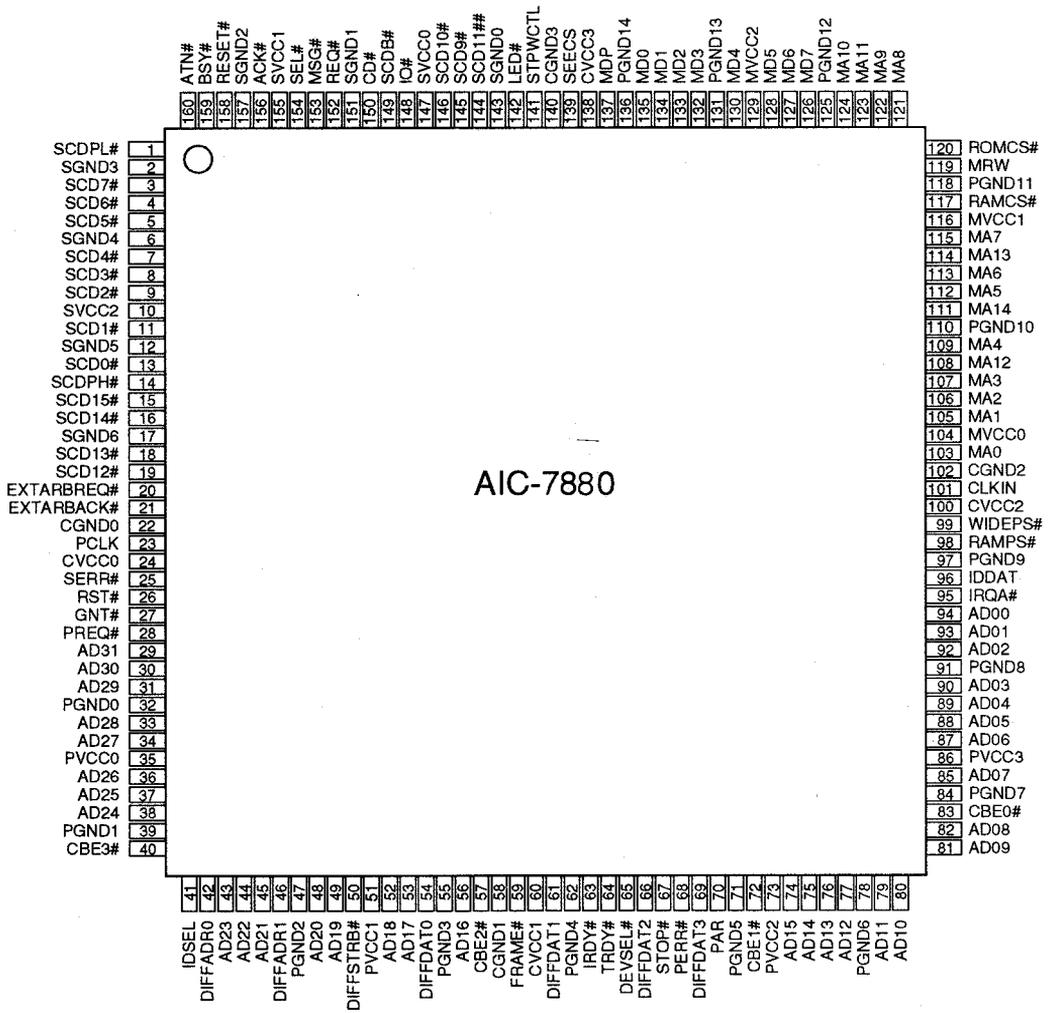


Figure 2- 16 AIC 7880 Pin Diagram

2.9.4 Signal Descriptions

Table 2- 11 AIC 7880 I/O Type Descriptions

Type	Description
I	Input
3ST/#	Tristate output/minute drive current in mA
OD/#	Open drain output/minute drive current in mA
NOD/#	Negation capable open drain output/minute sink current in mA

Table 2- 12 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
Host Interface			
AD[31:00]	29-31, 33, 34, 36-38, 43-45, 48, 49, 52, 53, 56, 74-77, 79-82, 85, 87-90, 92-94	I, 3ST/6	Address and Data. These are multiplexed on the same PCI bus pin. During the first clock of a transaction, AD[31:00] signals contain 32-bit physical byte address called low address (31:00) for Single Address Cycles (SAC). During subsequent clocks, AD[31:00] contain 32-bit data called low data 31:00 except for Dual Address Cycle (DAC) where both the first and the second (high address 63:32) clocks of a transaction contain address and the remaining clocks contain data (low data 31:00). The turn-around PCLK period for AD[31:00] is the idle cycle between transactions.
CBE[3:0]#	40, 57, 72, 83	3ST/6; I	Bus Command and Byte Enables. These signals are multiplexed on the same PCI pins. During the address phase of a transaction, CBE[3:0]# may assert concurrently and indicate a command to PCI.
DEVSEL#	65	I; 3ST/6	Device Select. When this signal is asserted, it indicates that the driving device has decoded its address as the selected target of the current bus transaction. DEVSEL# cannot be de-asserted once it is asserted unless FRAME# is sampled de-asserted except for the target abort case. Also, DEVSEL# must be asserted for one or more PCLKs before a target-abort condition may be signaled.

¹ Host interface signals separated by semi-colon (;) are for I/O PCI master and I/O PCI target, respectively.

Table 2- 12 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
Host Interface ¹			
FRAME#	59	3ST/6; I	Frame. The FRAME# signal is asserted by the current master to indicate the duration of a bus transaction. The assertion of FRAME# identifies an address phase of a transaction. De-assertion of this signal identifies the final data phase of the transaction.
GNT#	27	I; NA	Grant. An asserted GRANT# signal indicates to master that a bus transaction may be performed. This is a point-to-point signal with every master having its own GNT# signal. Only one GNT# may be asserted by the PCI System Board Central Source Arbitrator at a time.
IDSEL	41	NA; I	Initialization Device Select. The signal is used in lieu of the upper 24 ADn address signals and is valid only during configuration read and write transactions. This signal is validated with FRAME# assertion and valid CBE# values. IDSEL is a point-to-point signal with each agent having its own IDSEL. PCI convention is to connect a different AD[31:11] line to IDSEL input of each device on the bus. Dagger respond to all accesses in its configuration address range.
IRDY#	63	3ST/6; I	Initiator Ready#. This signal is asserted to indicate the current master's ability to complete the current data phase of a transaction. During a write, IRDY# indicates that the master is prepared to accept data on AD[31:00]. It is used in conjunction with TRDY#. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. A data phase is completed on any PCLK when IRDY# and TRDY# are both sampled asserted. An idle cycle (PCI bus free) occurs when both FRAME# and IRDY# are de-asserted. The turn-around PCLK period for IRDY# is the address phase of a transaction.
PAR	70	I, 3ST/6	Parity. This is an even-parity bit that protects both AD[31:00] and CBE[3:0]# signals. PAR is generated by the agent that is sourcing the 32-bit address of the transaction and/or the data of the transaction, including the CBE[3:0] values.

¹ Host interface signals separated by semi-colon (;) are for I/O PCI master and I/O PCI target, respectively.

Table 2- 12 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
Host Interface¹			
PCLK	23	I	PCI Bus Clock Input. This input supports timing for all transactions on the PCI bus. All other PCI signals are sampled on the rising edge of PCLK and all other parameters are defined with respect to this edge. PCLK is a controlled skew, point-to-point signal to each agent and is only driven by the PCI System Board Central Resource. The PCLK signal for the Dagger is a maximum rate of 33.3 MHz.
PERR#	68	I, 3ST/6	Parity Error#. This signal may be asserted (Pulsed for one PCLK period for each detected error, provided that the Parity Error Response bit, PERRESPEN, is active in the Configuration Command register) only by the agent receiving the data. Also, a target cannot assert PERR# until it has claimed the access by asserting DEVSEL# and completing the data transfer. The turn-around PCLK for PERR# is the third PCLK period after the last address PAR period for an agent. PERR# is asserted for detected errors after two PCLK periods.
PREQ#	28	3ST/6; NA	PCI Request. Once asserted, this pin indicates to the PCI System Board Arbitrator that a master desires use of the bus. This is a point-to-point signal with every master having its own PREQ#. Arbitration for the PCI bus is performed either when the bus is idle or in parallel with the transaction in process.
RST#	26	I	Reset#. When this signal is asserted, it forces agents to a known initialization state. RST# may be synchronous to PCLK when asserted or de-asserted.
SERR#	25	NA; OD/6	System Error#. This signal may be asserted by a PCI agent that detects an address parity error (provided that PERRESPEN and SERRESPEN are active) during the address phase of a transaction or for data parity errors on special cycles and for any other system error where the result is a catastrophic error. The transaction master is solely responsible for reporting master or target aborts. Targets do not assert SERR# when using target-abort termination.

¹ Host interface signals separated by semi-colon (;) are for I/O PCI master and I/O PCI target, respectively.

Table 2- 12 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
Host Interface ¹			
STOP#	67	I; 3SR/6	Stop. An asserted STOP# signal indicates that the current target is requesting the master to stop the current data phase of a transaction in process. STOP#, once asserted, must remain asserted until FRAME# is de-asserted and data may or may not be transferred in the final data phase of the transaction. The turn-around PCLK period for STOP# is the address phase of a transaction.
TRDY#	64	I; 3ST/6	Target Ready#. When this signal is asserted, this indicates that the current slave's ability to complete the current data phase of a transaction. During a read, TRDY# indicates that the slave is asserting valid data on AD[31:00]. During a write, it indicates that the slave is prepared to accept data. It is used in conjunction with IRDY#. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. Wait cycles should be minimized when more than eight are expected. Except for the first transfer, the transaction should be disconnected by the target and retried by the master. A data phase is completed on any PCLK when IRDY# and TRDY# are both sampled asserted. The turn-around PCLK period for TRDY# is the address phase of a transaction.
IRQA#	95	3ST/4	Interrupt Request A. IRQA# assertion state changes are synchronized to PCLK for PCI type errors and parity errors. Dagger interrupt conditions cannot assert IRQA when the INTEN bit is not active or the POWRDN bit is active in the HCNTL register. For IRQA# assertion conditions, see INSTAT register. Note that IRQA output is floated when RST# is asserted.
SCSI Interface			
SCD(15:0)#	15, 16, 18, 19, 144, 145, 146, 149, 3-5, 7-9, 11, 13	I, NOD/48	SCSI Data [15:0]#. The SCSI data lines drive the ID during arbitration and selection, command and data information, as well as status and messages.
SCDPH#	14	I, NOD/48	SCSI High Byte Parity. This bit supports odd parity for SCD[15:8]#.
SCDPL#	1	I, NOD/48	SCSI Low Byte Parity. This bit supports odd parity for SCD[7:0].

¹ Host interface signals separated by semi-colon (;) are for I/O PCI master and I/O PCI target, respectively.

Table 2- 12 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
SCSI Interface			
CD#	150	I, NOD/48	Command Data. This control line is received when in Initiator mode or driven when in Target mode. It indicates Command or Message phase when asserted, and Data phase when de-asserted. This control signal is used for 8 or 16 bit transfers.
IO#	148	I, NOD/48	In/Out. This control line is received when in Initiator mode or driven when in Target mode. It indicates the In direction when asserted, and the Out direction when de-asserted. This control signal is used for 8 or 26 bit transfers.
MSG#	153	I, NOD/48	Message#. This control line is received when in Initiator mode or driven when in Target mode. It indicates a Message phase when asserted, and a Command or Data phase when de-asserted. This control signal is used for 8 or 16 bit transfers.
REQ#	152	I, NOD/48	Request#. This control line is received by the device when in Initiator mode and driven when in Target mode. A Target asserts REQ# to indicate that a byte is ready or is needed by the Target. This control signal is used for 8 or 16 bit transfers.
ACK#	156	I, NOD/48	Acknowledge#. This control line is received by the device when in Target mode, and driven when in Initiator mode. An Initiator asserts ACK# to indicate that a byte is ready for or is received from the target. This control signal is used for 8 or 16 bit transfers.
RESET#	158	I, NOD/48	Reset#. This line is received and/or driven. It is interpreted as a hard reset and clears all commands pending on the SCSI bus. This control signal is used for 8 or 16 bit transfers.
SEL#	154	I, NOD/48	Select#. This line is driven after a successful arbitration to select as an Initiator or re-select as a Target, and otherwise it is received. This control signal is used for 8 or 16 bit transfers.
BSY#	159	I, NOD/48	Busy#. This line is driven by the Initiator as a handshake during arbitration and received for the rest of the transfer. As a target, it is driven also as a handshake during arbitration and then is driven for the rest of the transfer.
ATN#	160	I, NOD/48	Attention#. This line is driven as an Initiator when a special condition occurs. It is received by the target. This control signal is also used for 16 bit transfers.

Table 2- 12 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
DIFFADR[1:0]	43, 42	3ST/4	Differential Control Address. This line determines the meaning of DIFFDAT[3:0]. This control signal is used for 8- or 16-bit data transfers.
SCSI Interface			
DIFFDAT[3:0]	69, 66, 61, 54	3ST/4	Differential Control Data. These lines contain information latched by outside circuitry to control differential drivers. The definition of these bits depends on the value of DIFFADR[1:0]. This control signal is used for 8- or 16-bit data transfers.
DIFFSTRB#	50	3ST/4	Differential Control Strobe. This signals clocks the data from DIFFDAT into the addressed latch specified by DIFFADR on the rising edge. Both DIFFDAT and DIFFADR are stable for the duration of DIFFSTRB#. This control signal is used for 8- or 16-bit transfers.
LED#	142	3ST/4	LED#. The LED# output has three functions: <ol style="list-style-type: none"> 1. To indicate that AIC-7880 is actively connected to the SCSI bus. LED asserted state is latched with the ORrf result of active bits SELINGO, SELDI, and SELDO in the SSTAT0 register and de-asserted by the following SCSI bus free condition. LED# may be used to supply the system status of AIC-7880 SCSI bus activity and may directly drive an indicator (LED) provided that the current is limited to a maximum of 20 Ma. 2. As a clock to shift in an external device ID value from input IDDAT, to replace the internal default device ID value. This use of LED# is triggered as a result of RST# assertion. 3. For diagnostic support or general purpose output control bit. Note that LED# output is floated when RST# is asserted.

Table 2- 12 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
STPWCTL	141	3ST/4	SCSI Termination Power Down Control. This supports the capability to enable or disable the external SCSI bus termination power source. The enable/disable polarity of STPWCTL may be selected with the STPWLEVEL bit in the Configuration DEVCONFIG register and the actual enable/disable state is selected with the STPWEN bit in the device SXFRCTL1 register. CHIPRST forces STPWCTL to the selected disabled state and STPWEN to the inactive state. RST# assertion forces STPWCL to be floated and both STPWLEVEL and STPWEN to be inactive. STPWCL may also be used for a general purpose output control bit.
SCSI Interface			
WIDEPS#	99	I	Wide Present#. When asserted (=0), this signal indicates that a wide (16-bit) cable connector is present. WIDEPS# input contains an internal pull-up and only needs to be connected for 16-bit operations.
Memory Port Interface			
EXTARBACK#	21	I	External Arbitration Acknowledge is a status input to AIC-7880 with an internal pull-up. When EXTARBACK# is asserted low in response to AIC-7880's asserted EXTARBREQ# output, it indicates to the AIC-7880 that it may drive its memory port outputs and access external memory devices. EXTARBACK# remains asserted until some other user needs access to the memory port external shared memory devices which is detected by the external memory port arbitrator.
EXTARBREQ#	20	3ST/8	External Arbitrator Request. When asserted, this status output indicates an external arbitrator that AIC-7880 requires access to the memory port external devices such as SRAM (SCB), ROM/EEPROM, SEEPROM, and other board control devices. All requests for the memory port access is delayed until access is initially granted with EXTARBACK# assertion. EXTARBREQ# remains asserted until EXTARBACK# is de-asserted and AIC-7880 is not performing an access before being de-asserted. When EXTREQLCK is active, it will not affect the assertion of EXTARBREQ#, but once EXTARBREQ# is asserted, it extends its assertion until EXTREQLCK is inactive. EXTARBREQ# output has high impedance during assertion of RST#.

Table 2- 12 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
MA[14:0]	111, 114, 108, 123, 124, 122, 121, 115, 113, 112, 109, 107, 106, 105, 103	3ST/8	Memory Address [14:0] are address bus outputs to the external memory devices. They are in a float condition and become driven only after EXTARBACK# is asserted due to AIC-7880 EXTARBREQ# being asserted or when MPORTMODE is active. They are driven continuously until EXTARBREQ# is de-asserted. MA[14:0] outputs have high impedance during assertion of RST#.
Memory Port Interface			
MD[7:0]	126-128, 130, 132-135	I, 3ST/8	Memory Data [7:0] is the memory port data bus. It is used to read or write external ROM/EEPROM byte data when AIC-7880 is a target, to read or write external SRAM SCB page byte data by the sequencer or by the driver when AIC-7880 is a target, to read or write external SEEPROM bit data or board control device data by the sequencer or by the driver when AIC-7880 is a target. The are in a float condition and become driven only after EXTARBACK# is asserted or when MPORTMODE is active due to AIC-7880 EXTARBREQ# being asserted and a write process is to be performed. MD[7:0] outputs have high impedance during assertion of RST#.
MDP	137	I, 3ST/8	Memory Data Parity is optionally used for parity protection of SCB data stored in the external SRAM 99-bit device). Odd parity data are always generated and parity checking is enabled when EXTSCBPEN is active in the configuration DEVCONFIG register. MDP is in a float condition and become driven only after EXTARBACK# is asserted due to AIC-7880 EXTARBREQ# being asserted or when MPORTMODE is active. It is driven when a write access is to be performed. MDP output is floated during and following assertion of RST#. When the external SRAM is an 8-bit device,EXTSCBPEN must be inactive.

Table 2- 12 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
MRW	119	3ST/24	<p>Memory Port Read Write is driven when AIC-7880 has been granted the arbitration for an access to the external SRAM/ROM/EEPROM memory devices. A read cycle results when output MRW is at a high level (=1), while RAMCS# or RMCS# is asserted. A write cycle results when output MRW is at a low level (=0), while RAMCS#/ROMCS# is asserted. A read cycle, a write cycle, or a read-modify-write cycle may be performed by the sequencer with memory port timed control of MRW and RAMCS# in a single sequencer instruction cycle access of the memory port.</p> <p>AIC-7880 as a target may only perform a read or a write cycle access through the memory port with timing following the source of the access time. MRW is in a float condition and is driven only after EXTARBACK# is asserted due to AIC-7880 EXTARBREQ# being asserted or when MPORTMODE is active. MRW is floated during and following assertion of RST# or a write to CHIPRESET=1.</p>
Memory Port Interface			
RAMCS#	117	3ST/24	<p>RAM Chip Select# is driven when AIC-7880 has been granted the arbitration for an access to the external memory SRAM device and is asserted (=0) for an access to the external SRAM. RAMCS# is in a float condition and is driven only after EXTARBACK# is asserted due to AIC-7880 EXTARBREQ# being asserted or when MPORTMODE is active. RAMCS# is floated during and following assertion of RST# or a write to CHIPRESET=1. The SRAM cycle access time is 20 nanoseconds.</p>
ROMCS#	120	3ST/4	<p>ROM Chip Select# is driven when AIC-7880 has been granted the arbitration for an access to the external ROM/EEPROM and is asserted (=0) for access of the external memory ROM/EEPROM device. ROMCS# is in a float condition and is driven only after EXTARBACK# is asserted due to AIC-7880 EXTARBREQ# being asserted or when MPORTMODE is active. ROMCS# is floated during and following assertion of RST# or a write to CHIPRESET=1. The cycle access time is hardware controlled for a 150-ns device. The external ROM control interface should be such that when MRW is low (write access) and ROMCS# is asserted, ROM data outputs are not enabled, then the cycle becomes a NOP with no contention with AIC-7880 driven MD[7:0] outputs.</p>

Table 2- 12 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
SEECs	139	3ST/4	Serial EEPROM Chip Select output is asserted (=1) if SEEMS is active and AIC-7880 has been granted arbitration for an access to the external memory SEEPROM device. SEECs output may now be controlled by the state stored in bit SEECs in the SEECTL register. SEECs is in a float condition and is driven only after EXTARBACK# is asserted due to AIC-7880 EXTARBREQ# being asserted or when MPORTMODE is active. SEECs is floated while RST# is asserted or POR is active.
Memory Port Interface			
RAMPS#	98	I, 3ST/4	RAM Present# is asserted (=0) to enable access of an external SRAM for expanded SCB array data storage. When RAMPS# is de-asserted the internal AIC-7880 SCB array RAM is used for SCB storage of 16 SCBs (0-15), the SCBPTR register maximum stored value is restricted to 1Fh, and the QINFIFO/QINCNT/ QOUTFIFO/QOUTCNT storage and count (0=empty, 16=full) supports only 16 SCBs. When RAMPS# is asserted, an external SRAM is required. The size of the SRAM is 4 KB for 128 SCBs and 8 KB for 256 SCBs. The software driver must scan to determine the actual installed SRAM size.
Miscellaneous			
IDDAT	96	I	Identification Data. This input signal performs the shifting-in of an external device ID value to replace the internal default device ID value readable from the DEVICEID1 configuration register or the DSDEVID1 device register. The external IDDAT data source should be initialized with the desired identification data to be shifted-in when RST# is asserted. The loaded data will be shifted with the rising edge of 8 IDDAT shift clocks supplied on LED# commencing (2 to 3 CLKINs) after sampling RST# is de-asserted. LED# transitions after the 8 IDDAT shift clocks are ignored by the IDDAT data load logic.
CLKIN	101	I	Input Clock Frequency. Standard input (Dagger) - 40 MHz nominal input frequency. This is used internally by the SCSI, SEQUENCER, DFIFO, memory port, and the PCI host blocks for timing.
Power Distribution			
Core Logic Power Pins			
Only pin 23 is connected to and utilizes power supplied by the Core Logic pins.			

Table 2- 12 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
CVCC[3:0]	138, 100, 60, 24	PWR	Core Logic Positive Voltage Supply
CGND[3:0]	140, 102, 58, 22	PWR	Core Logic Ground
SCSI Interface Power Pins			
The following external pins are connected to and utilize power supplied by these power pins: SCD[15:0]#, SCDPH#, SCDPL#, CD#, IO#, MSG#, REQ#, ACK#, RESET#, SEL#, BSY#, ATN#, LED#, STPWCTL.			
SVCC [2:0]	10, 155, 147	PWR	SCSI Bus Driver Positive Voltage Supply
SGND [5:1]	17, 12, 6, 2, 157, 151, 143	PWR	SCSI Bus Driver Ground
PCI Interface Power Pins			
The following external pins are connected to and utilize power supplied by the PVCC power pins: AD[31:00], CBE[3:0]#, CLKIN, DEVSEL#, FRAME#, GNT#, IDSEL#, IRDY#, PAR#, PCLK, PERR#, PREQ#, RST#, SERR#, STOP#, TRDY#, IRQA#, DIFFDAT[3:0], DIFFADR[1:0], DIFFSTRB#, EXTARBREQ#, EXTARBACK#.			
PVCC[3:0]	86, 73, 51, 35	PWR	PCI Bus Driver Positive Voltage Supply
The following external pins are connected to and utilize power supplied by the PGND power pins: AD[31:00], CBE[3:0]#, CLKIN, DEVSEL#, FRAME#, GNT#, IDSEL#, IRDY#, PAR#, PCLK, PERR#, PREQ#, RST#, SERR#, STOP#, TRDY#, IRQA#, DIFFDAT[3:0], DIFFADR[1:0], DIFFSTRB#, WIDEPS#, MD[7:0], MDP, MA[14:0], ROMCS#, RAMCS#, MRW, RAMPS#, SEECS, IDDAT, EXTARBREQ#, EXTARBACK#.			
PGND [14:0]	136, 131, 125, 118, 110, 97, 91, 84, 78, 71, 62, 55, 47, 39, 32	PWR	PCI Bus Driver Ground
Memory Port Interface Power Pins			
The following external pins are connected to and utilize power supplied by this power pin: IRQA#, WIDEPS#, MD[7:0], MDP, MA[14:0], ROMCS#, RAMCS#, MRW, RAMPS#, SEECS, IDDAT.			
MVCC[2:0]	129, 116, 104	PWR	Memory Port Bus Driver Positive Voltage Supply

2.10 ATI 264VT

The ATI 264VT is a highly integrated multimedia graphics and video controller for both multiplexed VESA Local Bus (VLB) and PCI Bus systems. The VT achieves unprecedented performance with an "all-in-one" design that integrates a video scaler, a color space converter, a true-color palette DAC, and a triple-clock synthesizer with ATI's proven mach64 graphics engine.

Active power management techniques are used to monitor activity levels within these graphics controllers and to perform real-time power reductions such as dynamic clock control and graphics engine shutdown. Because full-speed operation can be restored without delay, these techniques do not have impact on performance.

The VT is register-compatible with ATI's *mach64* accelerator series and provides immediate compatibility with a wide range of application drivers.

The VT is backward compatible with ATI's family of integrated controllers, providing OEM with a low-cost path to additional features and performance.

2.10.1 Features

- High integration results in a low cost and small footprint graphics subsystem ideal for motherboard implementations.
- PCI revision 2.0 bus for Plug-and-Play ease of use.
- True-color palette DAC supporting pixel clock rates up to 135 MHz for 1280 x 1024 resolution at 75 Hz.
- YUV to RGB conversion with support for both packed-pixel and planar YUV formats
- DDC1 and DDC2B Plug-and-Play monitor support.
- Support for 26-pin VESA compatible feature connector that supports up to 1024 x 768 resolution
- Flexible memory configurations: 1 MB to 4 MB DRAM, 256K x 4, 256K x 8, or 256K x 16 with support for either dual CAS or dual write.

2.10.2 Block Diagram

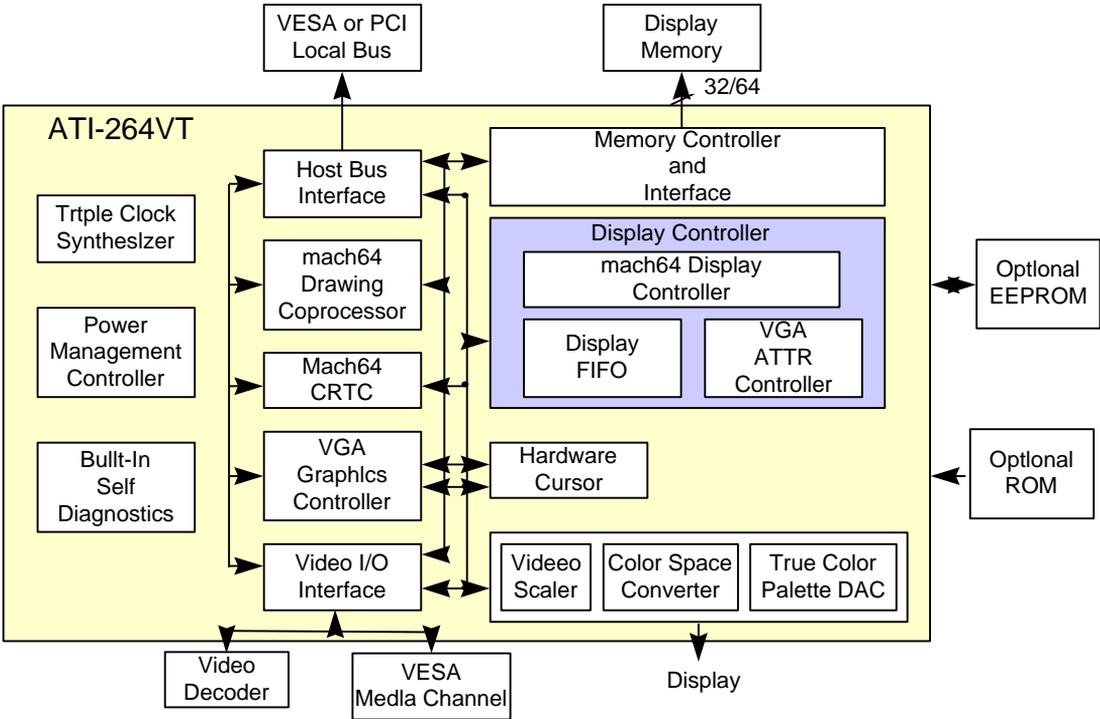


Figure 2- 17 ATI 264VT Block Diagram

2.10.3 Pin Diagram

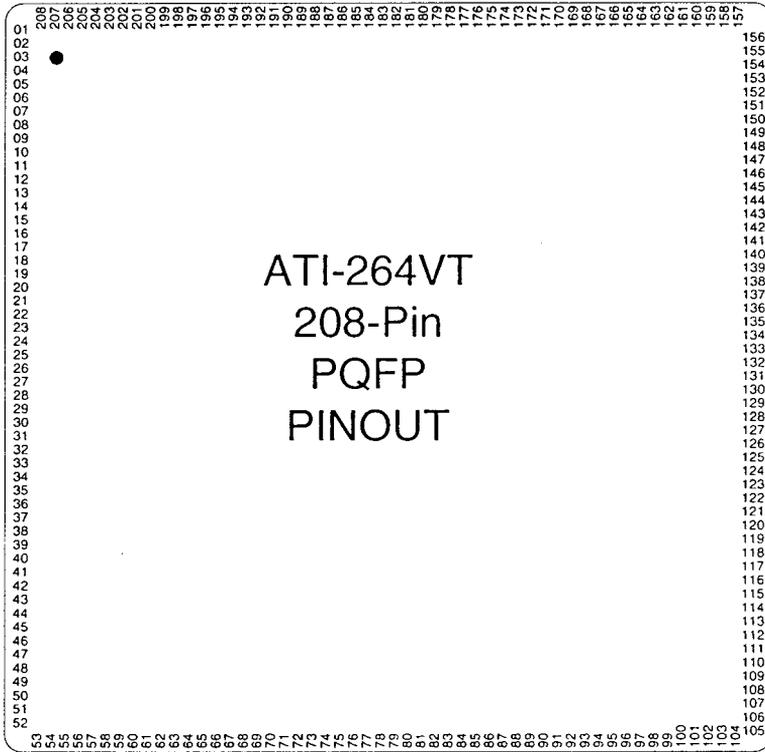


Figure 2- 18 ATI 264VT Pin Diagram

2.10.4 Signal Descriptions

Table 2- 13 ATI 264VT Signal Descriptions

Signal	Pin	Type	Description
Bus Interface			
PCI Local Bus Implementation			
AD[31:0]	143: 150, 153: 154 158: 163, 174: 181 185: 192	I/O	Multiplexed: System Address or Data bits (31:0)
C/BE#[3:0]	151, 164, 173, 184	I	Multiplexed: Bus Command or Byte Enable bits 3:0. BE# signals are active low.
CPUCLK	142	I	Bus Clock
DEVSEL#	169	O	Device Select. When actively driven, it indicates that the controller has decoded its address.
FRAME#	165	I	Frame is driven by the current bus master to indicate the beginning and duration of an access.
IDSEL	152	I	Initialization Device Select. Used as a chip select during configuration read and write transactions.
INTR#	140	O	Interrupt Request. Level triggered, active low by default
IRDY#	166	I	Initiator Ready. Indicates the bus master is able to complete the current data phase of transaction.
PAR	172	O	Parity. Even parity used
RESET#	141	I	Bus Reset
STOP#	171	O	Stop. Indicates the current target us requesting the master to stop the current transaction.
TRDY#	167	O	Target Ready. Indicates the target agent is able to complete the current data phase of the transaction.
VLB Multiplexed Local Bus Implementation			
AD[31:0]	143:150, 153:154. 158:163, 174:181, 185:192	I/O	Multiplexed: System Address or Data bits [31:0]
BE#3 [IDSEL]	152	I	BE#[3]
BE#0 [TRDY#]	167	I	BE#[0]
BE#1 [DEVSEL#]	169	I	BE#[1]
BE#2 [STOP#]	171	I	BE#[2]
RESET	141	I	Reset
LCLK [CPUCLK]	142	I	CPUCLK

Table 2- 13 ATI 264VT Signal Descriptions

Signal	Pin	Type	Description
Bus Interface			
VLB Multiplexed Local Bus Implementation			
RDYRTN [IRDY]	166	O	RDYRTN#
LRDY# [FRAME#]	165	I	LRDY#
ADS# [PAR]	172	O	ADS#
DIR [C/BE3]	151	O	DIR
DEN3	164	O	DEN#
AEN# [C/BE1]	173	O	AEN#
LDEV# [C/BE0]	184	O	LDEV#
INTR	140	I	INTR
Memory Interface			
Dual-write Memory 256x4, 256x8, 256x16			
CAS0#/WE#0	29	O	Column Address Strobe for first and second MB of memory
CAS1#/WE#1	28	O	Column Address Strobe for third and fourth MB of memory
MA[9:0]	204, 198, 196, 194:193	O	Memory Address bits 9:0
MD[31:0]	55:54, 50:40, 38, 36:30, 24:14	I/O	Data bits 31:0 for first and third MB of memory
MD[63:32]	92:90, 88:80 77:65, 63, 61:56	I/O	Data bits 63 and 32 of second and fourth MB of memory
OE#0	205	O	Output Enable for first and second MB of memory
OE#1	207	O	Output Enable for third and fourth MB of memory
RAS#0	3	O	Row Address Strobe for first and second MB of memory
RAS#1	206	O	Row Address Strobe for third and fourth MB of memory
WE#/CAS# [7:0]	4:9, 11, 13	I/O	Write Enable bits 7:0
WE#/CAS# [7:0]	4:9, 11, 13	I/O	Column Address Strobe
MA[9:0]	204, 198 196 194: 193	O	Memory Address bits 9:0
MD[31:0]	55:54, 50: 40, 38, 36:30, 24:14	I/O	Data bits 63 and 32 of second and fourth MB of memory

Table 2- 13 ATI 264VT Signal Descriptions

Signal	Pin	Type	Description
Memory Interface			
Dual-CAS Memory 256x4, 256x8, 256x16			
MD[63:32]	92:90, 88:80, 77:65, 63, 61:56	I/O	Data bits 63 and 32 of second and fourth MB of memory
RAS#0	3	O	Row Address Strobe for first and second MB of memory
RAS#1	206	O	Row Address Strobe for the third and fourth MB of memory
CAS#/WE#0	29	O	Write Strobe for first and second MB of memory
CAS#/WE#1	28	O	Write Strobe for the third and fourth MB of memory
OE#0	205	O	Output enable for the first and second MB of memory
OE#1	207	O	Output enable for third and fourth MB of memory
SDRAM Memory 128x16x2			
CAS# [1:0]	28, 29	O	CAS[1:0]
RAS# [1:0]	3,206	O	RAS[1:0]
WE# [7:0]	4, 9, 11, 13	O	DQM[7:0]
OE#1	205	O	WE#
OE#0	207	O	CLK
MA[9:0]	204:198, 196, 194, 193	O	MA[9:0]
MD[63:0]	55, 54, 50:40, 38, 36:30, 24:14, 92:90, 88:80, 77:65, 63, 61:56	I/O	AD[63:0]
DAC and Monitor Interface			
R	120	O	Red analog pixel data output to monitor
G	121	O	Green analog pixel data output to monitor
B	122	O	Blue analog pixel data output to monitor
COMP	124	A	Compensation pin for the DAC
RSET	123	A	Current setting resistor for the DAC
VREF	125	A	DAC reference voltage
HSYNC	129	O	Horizontal sync
VSYNC	128	O	Vertical sync

Table 2- 13 ATI 264VT Signal Descriptions

Signal	Pin	Type	Description
Frequency Synthesizer Interface			
MLOOP	111	A	Memory clock loop filter
PLOOP	114	A	Pixel clock loop filter
XTALIN ¹	102	A	14.31818 MHz crystal or TTL oscillator connection
XTALOUT ¹	103	A	14.31818 MHz crystal connection
Feature Connector Interface			
EDCLK	107	I	Auxiliary Pixel Clock Select
ESYNC	133	I	Auxiliary Pixel Clock Select
EVIDEO	132	I	Auxiliary Pixel Data Select
BLANK#	135	O	Blank Signal
DCLK	134	O	Pixel Clock Output
PIXEL[7:0]	93:100	O	Pixel Data Output
EEPROM Interface			
GIO2	135	I/O	EEPROM Data I/O
GIO3	136	O	EEPROM Chip Select
GIO1	109	I/O	EEPROM Clock
EPROM Interface			
ROMCS#	113	O	ROM Chip Select
MD [46:32]	72:56	I/O	EPROM Address Bus
MD [63:56]	92:84	I/O	EPROM Data Bus
Monitor ID Interface			
GIO0	108	I/O	DDC Serial Data
GIO4	138	I/O	DDC Serial Clock
VMC Interface			
SA#	117		Serial I/O Interrupt Request
SB# [EDCLK]	107		Serial I/O Interrupt Request
BS#0 [BLANK#]	135		Bus Size
BS#1 [EVIDEO#]	133		Bus Size
VMCCTRL [ESYNC]	133		VMC Control Cycle Flag
VMCMASK	25		Pixel Mask

¹ For designs using an external clock source (instead of a crystal), the input XTALIN is CMOS inverter C_{in}=0.5pF, and XTALOUT is not connected.

Table 2- 13 ATI 264VT Signal Descriptions

Signal	Pin	Type	Description
VMC Interface			
VMCCLK [DCLK]	134		VMC Clock
SNRDY#	137		Slave Not Ready
DATA [7:0]	100:93		Data Bits
Power and Ground Pins			
VCC	10, 27, 37, 53, 62, 78, 89, 104, 127, 130, 170, 195, 208	Pwr	3.3V Power
VSS	1, 2, 12, 26, 39, 51, 52, 64, 79, 101, 105, 118, 131, 155, 156, 168, 182, 197	Gnd	Ground
PVDD	110, 115	PWR	PLL Power
PVSS	112	GND	PLL Ground
QVSS	106	GND	PLL Ground
AVDD	126	PWR	DAC Analog Power
AVSS	119	GND	DAC Analog Ground
VEE	139, 157, 183	PWR	5.0V Power

2.10.5 Display Modes

Table 2- 14 Display Modes for DRAM (45ns) or EDO DRAM (60ns)

Resolution	256 colors		65K colors			16.7M colors		
	1 MB	2 MB	1 MB	2 MB	4 MB	1 MB	2 MB	4 MB
640 x 480	100	100	100	100	100	90	100	100
800 x 600	100	100	90	100	100	—	100	100
1024 x 768	100	100	—	100	100	—	—	75
1152 x 864	80	80	—	80	80	—	—	60
1280 x 1024	*	75	—	—	60	—	—	—

* - 1280 x 1024 @ 16 colors is available at 75 Hz.

Table 2- 15 Display Modes for Synchronous DRAM or EDO DRAM with Burst CAS

Resolution	256 colors		65K colors			16.7M colors		
	1 MB	2 MB	1 MB	2 MB	4 MB	1 MB	2 MB	4 MB
640 x 480	100	100	100	100	100	100	100	100
800 x 600	100	100	100	100	100	—	100	100
1024 x 768	100	100	—	100	100	—	—	100
1152 x 864	80	80	—	80	80	—	—	80
1280 x 1024	*	75	—	—	75	—	—	75

* - 1280 x 1024 @ 16 colors is available at 75 Hz.

2.11 Super I/O Controller (SMC 37C935)

The SMC 37C935 is an advanced high-performance multi-mode parallel port super I/O diskette drive controller.

2.11.1 Features

- Compatible with ISA Plug-and-Play standard (Version 1.0a)
- 8042 Keyboard Controller
 - 2K Program ROM
 - 256 Bytes Data RAM
 - Asynchronous Access to Two Data Registers and One Status Register
 - Supports Interrupt and Polling Access
 - 8 Bit Timer Counter
- Real Time Clock
 - MC146818 and DS1287 Compatible
 - 256 Bytes of Battery Backed CMOS in Two Banks of 128 Bytes
 - 128 Bytes of CMOS RAM Lockable in 4x32 Byte Blocks
 - 12 and 24 Hour Time Format
 - Binary and BCD Format
 - <1ua Standby Current (typ)
- Intelligent Auto Power Management
- 2.88MB Super I/O Floppy Disk Controller
 - Relocatable to 480 Different Addresses
 - 13 IRQ Options
 - 3 DMA Options
 - Licensed CMOS 765B Floppy Disk Controller
 - Advanced Digital Data Separator
 - Software and Register Compatible with SMC's Proprietary 82077AA Compatible Core
 - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
 - Game Port Select Logic
 - Supports Two Floppy Drives Directly
 - 24 mA AT Bus Drivers
 - Low Power CMOS Design

-
- Licensed CMOS 765B Floppy Disk Controller Core
 - Supports Vertical Recording Format
 - 16 Byte Data FIFO
 - 100% IBM Compatibility
 - Detects All Overrun and Underrun Conditions
 - 48 mA Drivers and Schmitt Trigger Inputs
 - DMA Enable Logic
 - Data Rate and Drive Control Registers
 - Enhanced Digital Data Separator
 - Low Cost Implementation
 - No Filter Components Required
 - 2 Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
 - Programmable Precompensation Modes
 - Serial Ports
 - Relocatable to 480 Different Addresses
 - 13 IRQ Options
 - Two High Speed NS16C550 Compatible UARTs with Send/Receive 16 Byte FIFOs
 - Programmable Baud Rate Generator
 - Modem Control Circuitry Including 230K and 460K Baud
 - IrDA, HP-SIR, ASK-IR Support
 - IDE Interface
 - Relocatable to 480 Different Addresses
 - 13 IRQ Options
 - 6 DMA Options
 - Two Channel/Four Drive Support
 - On-Chip Decode and Select Logic Compatible with IBM PC/Xr and PC/A? Embedded Hard Disk Drives
 - Multi-Modem Parallel Port with ChiProtect
 - Relocatable to 480 Different Addresses

2.11.2 Block Diagram

37C935 Control Block Diagram

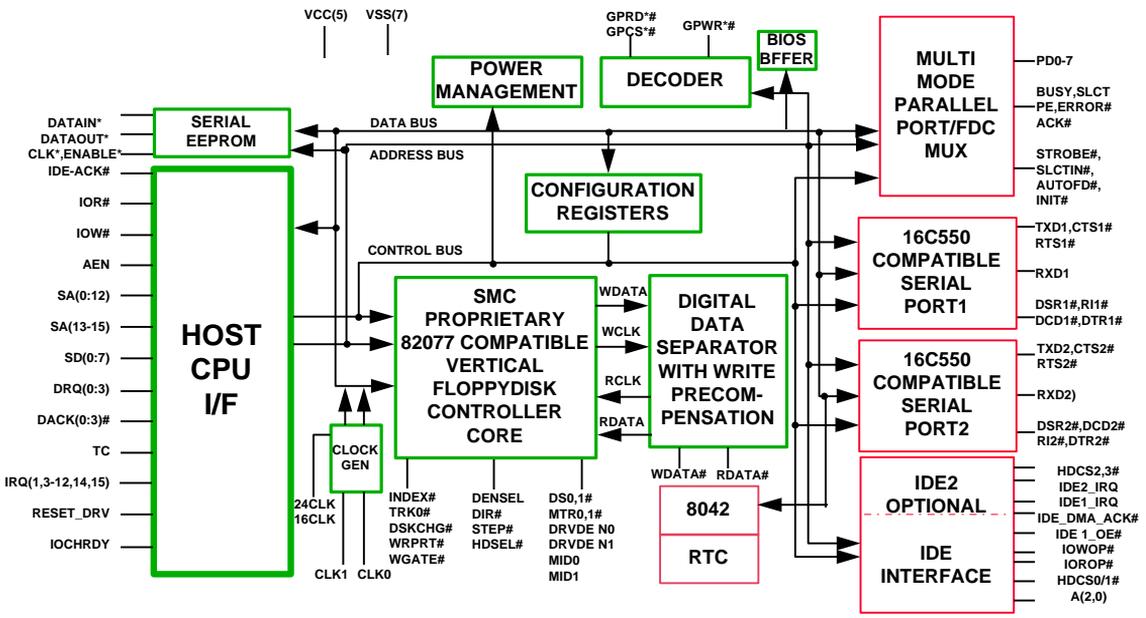


Figure 2- 19 37C935 Block Diagram

2.11.3 Pin Diagram

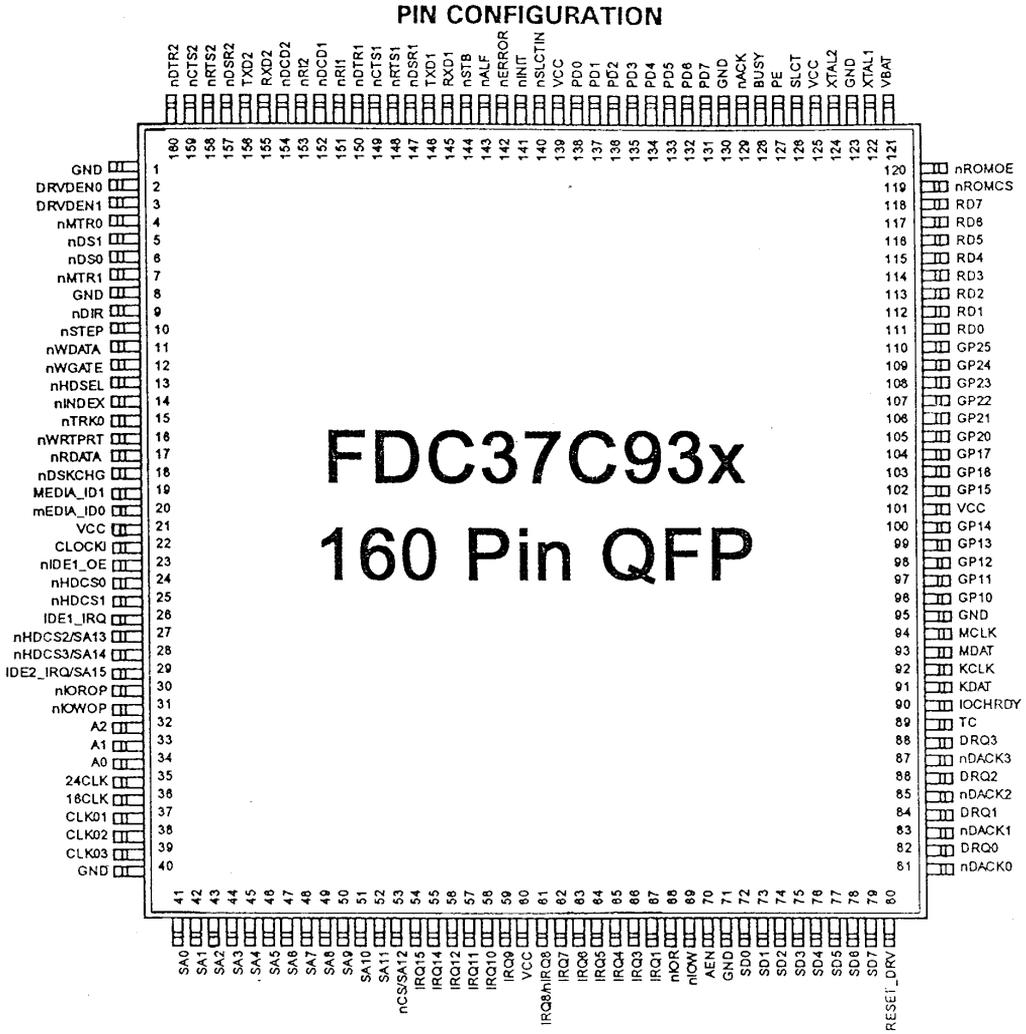


Figure 2- 20 37C935 Pin Diagram

2.11.4 Signal Descriptions

Table 2-16 lists and describes the buffer types for the 37C935 signals.

Table 2- 16 37C935 Buffer Type Descriptions

Buffer Type	Description
I	Input TTL compatible
IS	Input with Schmitt Trigger
I/OD16P	Input/output, 19mA sink, 90mA pull-up
I/O24	Input/output pin. 24mA sink; 12mA source
O4	Output, 4mA sink; 2.0mA source
O8SR	Output, 8mA sink; 4.0mA source with Slow Rate Limiting
O24	Output, 24mA sink; 12mA source
OD24	Output, open drain; 24mA sink
OD48	Output, open drain; 48mA sink
OD24P	Output, open drain; 24mA sink, 4mA source pull-up
OP24	Output; 24mA sink, 12mA source
OCLK	Clock output
ICLK	Clock input

Table 2- 17 37C935 Signal Descriptions

Signal	Pin	Type	Description
Host Processor Interface			
SD0 - SD7	72:79	I/O24	System Data Bus
SA0 - SA11	41:52	I	System Address Bus
CS#	53	I	Chip Select / SA12
AEN	70	I	Address Enable
IOCHRDY	90	OD24	I/O Channel Ready
RESET_DRV	80	IS	Reset Drive
IRQ[1, 3:12, 14, 15]	67:61, 59:54	OD24	Interrupt Requests
DRQ[0:3]	82,84,86,88	O24	DMA Request
DACK[0:3]#	81, 83, 85, 87	I	DMA Acknowledge
TC	89	I	Terminal Count
IOR#	68	I	I/O Read
IOW#	69	I	I/O Write
24CLK	35	O8SR	Serial Clock Out (24MHz)
16CLK	36	O8SR	16MHz Out

Table 2- 17 37C935 Signal Descriptions

Signal	Pin	Type	Description
Host Processor Interface			
CLOCKI	22	ICLK	14.318MHz Clock Input
CLOCK1	37	O8SR	14.318MHz Clock Output 1
CLOCK2	38	O8SR	14.318MHz Clock Output 2
CLOCK3	39	O8SR	14.318MHz Clock Output 3
Diskette Drive Interface			
RDATA#	17	IS	Read Disk Data
WGATE#	12	OD48	Write Gate
WDATA#	11	OD48	Write Data
HDSEL#	13	OD48	Head Select (1 = side 0)
DIR#	9	OD48	Direction Control (1 = out)
STEP#	10	OD48	Step Pulse
DSKCHG#	18	IS	Disk Change
DS[0:1]#	5,6	OD48	Drive Select 0, 1
MTR[0:1]#	7,4	OD48	Motor On Lines
WPROT#	16	IS	Write Protected
TR0#	15	IS	Track 00
INDEX#	14	IS	Index Pulse Input
DRV DEN[1:0]	3,2	OD48	Drive Density Select [1:0]
MID[1:0]	19,20	IS	Media ID Inputs
Serial Port Interface			
RXD1, RXD2	145, 155	I	Receive Data
TXD1, TXD2	146, 156	O4	Transmit Data
RTS1#, RTS2#	148, 158	O4	Request to Send
CTS1#, CTS2#	149, 159	I	Clear to Send
DTR1#, DTR2#	150, 160	O4	Data Terminal Ready
DSR1#, DSR2#	147, 157	I	Data Set Ready
DCD1#, DCD2#	152, 154	I	Data Carrier Select
RI1#, RI2#	151, 153	I	Ring Indicator
Parallel Port Interface			
PD0-PD7	138:131	I/OP24	Port Data
SLCTIN#	140	OD24/OP24	Printer Select
INIT#	141	OD24/OP24	Initiate Output
AUTOFD#	143	OD24/OP24	Autofeed Signal
STROBE#	144	OD24/OP24	Strobe Signal
BUSY	128	I	Busy Signal
ACK#	129	I	Acknowledge Handshake

Table 2- 17 37C935 Signal Descriptions

Signal	Pin	Type	Description
Parallel Port Interface			
PE	127	I	Paper End
SLCT	126	I	Printer Selected
ERR#	142	I	Error at Printer
IDE			
IDE1_OE#	23	O4	IDE1 Enable
HDCS0#	24	O24	IDE 1 Chip Select0
HDCS1#	25	O24	IDE 1 Chip Select1
IOROP#	30	O24	IOR Output
IOWOP#	31	O24	IOW Output
A[2:0]	32:34	O24	Address [2:0] Output
IDE1_IRQ	26	I	IDE Interrupt Request
HDCS2	27	O24	IDE2 Chip Select 2 / SA13
HDCS3	28	O24	IDE2 Chip Select 3 / SA14
IDE2_IRQ	29	I	IDE2 Interrupt Request / SA15
Real Time Clock			
XTAL1	122	ICLK	32KHz Crystal Input
XTAL2	124	OCLK	32KHz Crystal Output
Vbat	121		Battery Voltage
Keyboard / Mouse			
KDAT	91	I/OD16P	Keyboard Data
KCLK	92	I/OD16P	Keyboard Clock
MDAT	93	I/OD16P	Mouse Data
MCLK	94	I/OD16P	Mouse Clock
General Purpose I/O			
GP10	96	I/O4	IRQ in
GP11	97	I/O4	IRQ in
GP12	98	I/O4	WD Timer Output / IRRX
GP13	99	I/O24	Power LED Output / IRTX
GP14	100	I/O4	General Purpose Read Strobe
GP15	102	I/O4	General Purpose Write Strobe
GP16	103	I/O4	Joy Stick Read Strobe / JOYCS
GP17	104	I/O4	Joy Stick Write Strobe
GP20	105	I/O4	IDE2 Output Enable
GP21	106	I/O4	Serial EEPROM Data In
GP22	107	I/O4	Serial EEPROM Data Out
GP23	108	I/O4	Serial EEPROM Clock
GP24	109	I/O4	Serial EEPROM Enable
GP25	110	I/O4	8042 P21

Table 2- 17 37C935 Signal Descriptions

Signal	Pin	Type	Description
BIOS Buffers			
RD[0:7]	111:118	I/O4	ROM Bus (I/O to the SD bus)
DOMCS#	119	I	ROM Chip Select (for ROM) only
ROMOE#	120	I	ROM Output Enable (DIR) (for ROM only)
Power			
VCC	21, 60, 101, 125, 139		+ 5V Supply Voltage
GND↔	1, 8, 40, 71, 95, 123, 130		Ground

BIOS Utility

Most systems are already configured by the manufacturer or the dealer. There is no need to run Setup when starting the computer unless you get a Run Setup message. If you repeatedly receive Run Setup messages, the battery may be bad. In this case, the system cannot retain configuration values in CMOS. Ask a qualified technician for assistance.

Before you run Setup, make sure that you have saved all open files. The system reboots immediately after you exit Setup.

3.1 Entering Setup

To enter Setup, press the key combination **CTRL** + **ALT** + **ESC** .



*You must press **CTRL** + **ALT** + **ESC** while the system is booting. This key combination does not work during any other time.*

The BIOS Utility main menu then appears:

BIOS Utility
System Information Product Information Disk Drives Startup Configuration Advanced Configuration System Security Date and Time Remote Diagnostic Configuration Load Default Settings Abort Settings Change Reset Non-PnP ISA Device Setting
↑↓ = Move Highlight Bar, ← = Select, Esc = Exit

3.2 System Information

The following screen appears if you select System Information from the main menu.

```
System Information                               Page 1/1

Processor .....Pentium Pro
Processor Speed .....200 MHz
Bus Frequency .....66 MHz
Internal Cache .....16 KB, Enabled
External Cache .....512 KB, Enabled

Floppy Drive A .....1.44 MB, 3.5-inch
Floppy Drive B .....None

IDE Primary Channel Master..Hard Disk, xxx MB
IDE Primary Channel Slave...None

Total Memory .....64 MB
Serial Port 1 .....3F8h, IRQ 4
Serial Port 2 .....2E8h, IRQ 3
Parallel Port .....378h, IRQ 7
Pointing Device .....Installed

Note: This screen will display any parameter setting
      changes only after rebooting the system.

PgUp PgDn = Move Screen, Esc = Back to Main Menu
```

The System Information menu shows the current basic configuration of your system.

The command line at the bottom of the menu tells you how to move from one screen to another and return to the main menu.

Press **PGDN** to move to the next page or **PGUP** to return to the previous page.

Press **ESC** to return to the main menu.

The following sections explain the parameters.



The parameters on the screens show default values. These values may not be the same as those in your system.

The items on the screens have fixed settings and are not user-configurable.

3.2.1 Processor

The Processor parameter specifies the type of processor currently installed in your system. The system is designed to support the Intel Pentium Pro CPU.

3.2.2 Processor Speed

The Processor Speed parameter specifies the speed of the CPU currently installed in your system. The system supports Intel Pentium Pro CPU running at 200 MHz.

3.2.3 Bus Frequency

The Bus Frequency parameter specifies the system external clock. The bus frequency can be either 50, 60 or 66 MHz.

3.2.4 Internal Cache

This parameter specifies the first-level or the internal memory size (i.e., the memory integrated into the CPU), and whether it is enabled or disabled. For information on how to configure the system memory, see section 3.3.3.

3.2.5 External Cache

This parameter specifies the second-level cache memory size currently supported by the system, and whether it is enabled or disabled. For information on how to configure the system memory, see Chapter 1.

3.2.6 Floppy Drive A

This parameter specifies the type of drive designated as Floppy Drive A. For information on how to configure the floppy drives, see section 3.4.1.

3.2.7 Floppy Drive B

This parameter specifies the system's current floppy drive B settings. For information on how to configure the floppy drives, see section 3.4.1.

3.2.8 IDE Primary Channel Master

This parameter specifies the current configuration of the IDE device connected to the master port of the primary IDE channel. For information on how to configure IDE devices, see section 3.4.2.

3.2.9 IDE Primary Channel Slave

This parameter specifies the current configuration of the IDE device connected to the slave port of the primary IDE channel. For information on how to configure IDE devices, see section 4.4.2.

3.2.10 Total Memory

This parameter specifies the total system memory. The memory size is automatically detected by BIOS during the POST. If you install additional memory, the system automatically adjusts this parameter to display the new memory size.

3.2.11 Serial Port 1

This parameter indicates the serial port 1 address and IRQ setting.

3.2.12 Serial Port 2

This parameter indicates the serial port 2 address and IRQ setting.

3.2.13 Parallel Port

This parameter indicates the parallel port address and IRQ setting.

3.2.14 Pointing Device

The BIOS utility automatically detects if there is a mouse connected to the system. If there is, this parameter displays the **Installed** setting. Otherwise, this is set to **None**.

3.3 Product Information

The Product Information contains general data about the system. It includes the product name, serial number, BIOS version, etc. These information are necessary for troubleshooting and may be required when asking for technical support.

The following screen shows the Product Information items.

```
Product Information                               Page 1/1

Product Name ..... Quad Pentium
Main Board ID ..... X3
Main Board P/N ..... 55.59901.001
System BIOS Version ..... V3.0
System BIOS ID ..... R01-A0           EN
BIOS Release Date ..... xxx. xx, '97

Esc = Back to Main Menu
```

3.3.1 Product Name

This parameter specifies the product name of the system.

3.3.2 Main Board ID

This parameter specifies the system board's identification number.

3.3.3 Main Board S/N

This parameter specifies the system board's serial number.

3.3.4 System BIOS Version

This parameter specifies the version of the BIOS utility.

3.3.5 System BIOS ID

This parameter specifies the identification number of the BIOS utility.

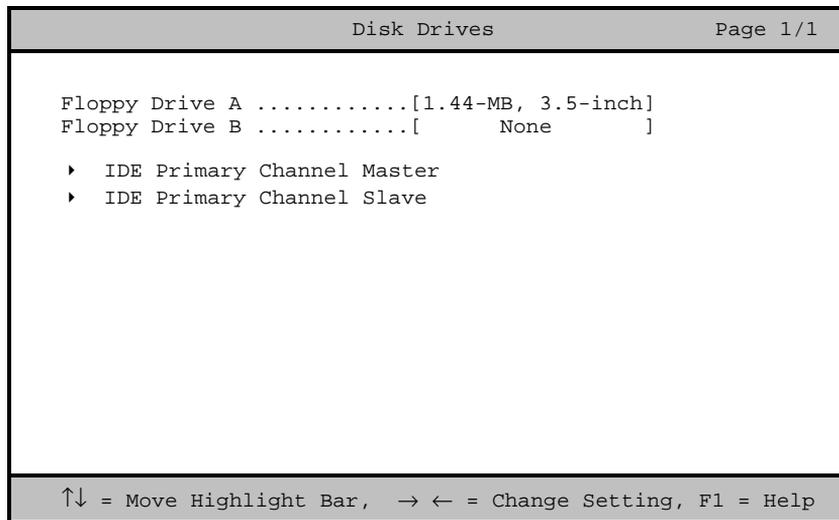
3.3.6 BIOS Release Date

This parameter specifies the official date the BIOS version is released.

3.4 Disk Drives

The Disk Drives menu lets you configure the IDE hard disk and disk drive settings.

The following screen shows the Disk Drives parameters and their default settings:



The triangle mark that precede an item within a menu indicates that there is a detailed menu for that particular item. Select the item to display the menu.

From the Disk Drives screen, select the IDE Primary Channel Master and IDE Primary Channel Slave items to display their respective menus. The screen on the next page shows the menu.

```
IDE Primary Channel Master                               Page 1/1

Type..... [Auto]
Cylinder ..... [  ]
Head ..... [  ]
Sector ..... [  ]
Size ..... [  ] MB

Hard Disk Block Mode ..... [Auto]
Hard Disk Size > 504MB ..... [Auto]

↑↓ = Move Highlight Bar, ← → = Change Setting, F1 = Help
```

The parameters for the IDE Primary Channel Slave menu are the same as in the above screen.

3.4.1 Floppy Drives

To configure the first floppy drive (drive A), highlight the Floppy Drive A parameter. Press  or  key to view the options, then select the appropriate value.

Possible settings for the Floppy Drive parameters:

- [**None**]
- [**360 KB, 5.25-inch**]
- [**1.2 MB, 5.25-inch**]
- [**720 KB, 3.5-inch**]
- [**1.44 MB, 3.5-inch**]
- [**2.88 MB, 3.5-inch**]

Follow the same procedure to configure floppy drive B. Choose **None** if you do not have a second floppy drive.

3.4.2 IDE Drives

There are two IDE drive option items under the Disk Drives menu. Select the IDE Primary Channel Master if you want to configure an IDE device set as master. Select the IDE Primary Channel Slave if you want to configure an IDE device set as slave.

To configure an IDE device designated as master:

1. Select the IDE Primary Channel Master option to display its menu.
2. Highlight the parameter Type, then press  or  to display the IDE drive types with their respective values for cylinder, head, sector, and size.

You may do any of the following:

- Select the type that corresponds to your IDE hard disk drive.
- If you do not know the exact type of your IDE device, select the **Auto** option to let the BIOS utility automatically detect the installed IDE drive type.
- You may save the values under the option **User**. The next time you boot the system, the BIOS utility does not have to auto-configure your IDE drive as it detects the saved disk information during POST.



Copy the IDE disk drive values and keep them in a safe place in case you have to reconfigure the disk in the future.

- If you have installed an IDE hard disk that was previously formatted but does not use the disk native parameters or structure, i.e., the disk may be formatted according to the user-specified number of cylinders, heads, and sectors, select the **User** option. Then enter the appropriate drive information.
- If there is no device connected, choose **None**.

To configure an IDE device designated as slave:

1. Select the IDE Primary Channel Slave option to display its menu.
2. Follow step 2 of the procedure when configuring a master device.

3.4.2.1 Hard Disk Block Mode

This function enhances disk performance depending on the hard disk in use. If you set this parameter to **Auto**, the BIOS utility automatically detects if the installed hard disk drive supports the Block Mode function. If supported, it allows data transfer in blocks (multiple sectors) at a rate of 256 bytes per cycle. To disregard the feature, change the setting to **Disabled**.

3.4.2.2 Hard Disk Size > 504 MB

When set to **Auto**, the BIOS utility automatically detects if the installed hard disk supports the function. If supported, it allows you to use a hard disk with a capacity of more than 504 MB. This is made possible through the Logical Block Address (LBA) mode translation. However, enhanced IDE feature works only under DOS and Windows 3.x, 95 environment. Other operating systems require this parameter to be set to **Disabled**.

3.5 Startup Configuration

The Startup Configuration allows you to specify your preferred setting for bootup.

The following screen appears if you select the Startup Configuration option from the main menu:

Startup Configuration		Page 1/1
System POST Mode	[Diagnostic]	
Silent Boot	[Disabled]	
Num Lock After Boot	[Enabled]	
Memory Test	[Disabled]	
Initialize SCSI Before IDE	[Disabled]	
Boot from IDE CD-ROM	[Disabled]	
System Boot Drive	[Drive A Then C]	
MP Compliant Revision	[V1.4]	

↑↓ = Move Highlight Bar, ← → = Change Setting, F1 = Help

3.5.1 System POST Mode

This parameter allows the system to perform the POST routines in **Diagnostic** and **Normal** modes. The **Diagnostic** mode shows the current status on the front panel LCD display. The default setting is **Diagnostic**.

3.5.2 Silent Boot

This parameter enables or disables the Silent Boot function. When set to **Enabled**, BIOS is in graphical mode and displays only an identification logo during POST and while booting. After which the screen displays the operating system prompt (such as DOS) or logo (such as Windows 95). If any error occurred while booting, the system automatically switches to the text mode.

Even if your setting is **Enabled**, you may also switch to the text mode while booting by pressing **F8** after you hear a beep that indicates the activation of the keyboard.

When set to **Disabled**, BIOS is in the conventional text mode where you see the system initialization details on the screen.

3.5.3 Num Lock After Boot

This parameter allows you to activate the Num Lock function upon booting. The default setting is **Enabled**.

3.5.4 Memory Test

When set to **Enabled**, this parameter allows the system to perform a RAM test during the POST routine. When set to **Disabled**, the system detects only the memory size and bypasses the test routine. The default setting is **Disabled**.

3.5.5 Initialize SCSI Before IDE

When enabled, this parameter allows initialization of installed SCSI drives first before initializing any IDE drives. When this parameter is disabled, IDE drives are initialized first.

3.5.6 Boot from IDE CD-ROM

When set to **Enabled**, the system checks for a bootable CD in the CD-ROM drive. If a CD is present, the system boots from the CD-ROM; otherwise, it boots from the drive specified in the System Boot Drive parameter.

When set to **Disabled**, the system boots from the drive specified in the System Boot Drive parameter.

3.5.7 System Boot Drive

This parameter allows you to specify the system search sequence. The selections are:

- **Drive A then C:** The system checks drive A first. If there is a diskette in the drive, the system boots from drive A. Otherwise, it boots from drive C.
- **Drive C then A:** The system checks drive C first. If there is a hard disk (drive C) installed, the system boots from drive C. Otherwise, it boots from drive A.
- **C:** The system always boots from drive C.
- **A:** The system always boots from drive A.

3.5.8 MP Compliant Revision

This parameter shows the multiprocessor specification compliance version. The default setting is **v1.4**. If you install an older operating system, particularly SCO UNIX v3.2.x.x or earlier, set this parameter to **v1.1**.

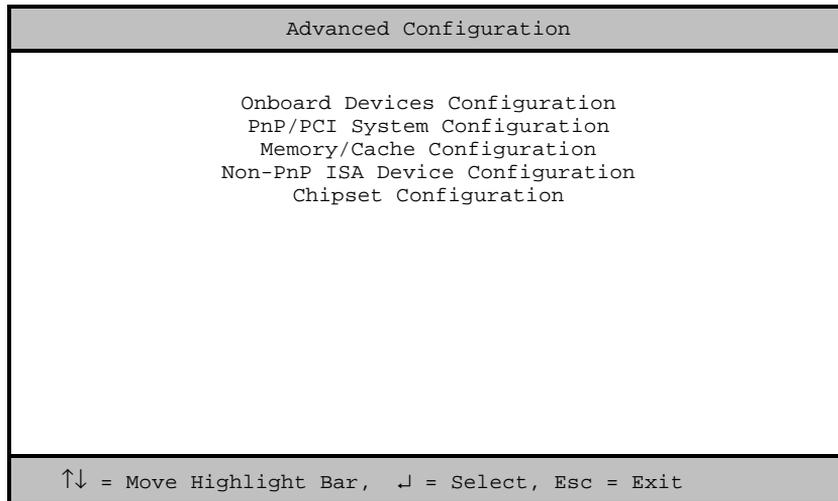
3.6 Advanced Configuration

The Advanced Configuration option allows you to configure the advanced system memory functions.



Do not change any settings in the Advanced Configuration if you are not a qualified technician to avoid damaging the system.

The following screen shows the Advanced Configuration parameters.



3.6.1 Onboard Devices Configuration

The Onboard Devices Configuration allows you to configure the onboard communication ports and the onboard devices. Selecting this option from the Advanced Configuration menu displays the following screen:

```
Onboard Devices Configuration                               Page 1/2

Serial Port 1 ..... [Enabled ]
  Base Address ..... [3F8h]
  IRQ ..... [4 ]
Serial Port 2 ..... [Enabled ]
  Base Address ..... [2F8h]
  IRQ ..... [3 ]
Parallel Port ..... [Enabled ]
  Base Address ..... [378h]
  IRQ ..... [7 ]
  Operation Mode ..... [ Standard ]
  ECP DMA Channel ..... [ - ]

↑↓ = Move Highlight Bar, ← → = Change Setting, F1 = Help
PgUp/PgDn = Move Screen
```

The following screen shows page 2 of the Onboard Devices Configuration menu.

```
Onboard Devices Configuration                               Page 2/2

Onboard Floppy Disk Controller ..... [Enabled ]
Onboard IDE Primary Channel ..... [Enabled ]

Onboard PS/2 Mouse (IRQ 12) ..... [Enabled ]

Onboard SCSI1 ..... [Enabled ]
  Boot from SCSI1 Device ..... [Enabled ]
Onboard SCSI2 ..... [Enabled ]
  Boot from SCSI2 Device ..... [Enabled ]

↑↓ = Move Highlight Bar, ← → = Change Setting, F1 = Help
PgUp/PgDn = Move Screen
```

3.6.1.1 Serial Port 1

This parameter allows you to enable or disable the serial port 1.

BASE ADDRESS

This function lets you set a logical base address for serial port 1. The options are:

- 3F8h
- 2F8h
- 3E8h
- 2E8h

IRQ

This function lets you assign an interrupt for serial port 1. The options are IRQ 3 and 4.

Note that the Base Address and IRQ parameters are configurable only if Serial Port 1 is enabled.

3.6.1.2 Serial Port 2

This parameter allows you to enable or disable the serial port 2.

BASE ADDRESS

This function lets you set a logical base address for serial port 2. The options are:

- 3F8h
- 2F8h
- 3E8h
- 2E8h

IRQ

This function lets you assign an interrupt for serial port 2. The options are IRQ 3 and 4.

Note that the Base Address and IRQ parameters are configurable only if Serial Port 2 is enabled.



If you assign 3F8h to serial port 1, you may only assign 2F8h or 2E8h to serial port 2.

If you assign 2F8h to serial port 1, you may only assign 3F8h or 3E8h to serial port 2.

3.6.1.3 Parallel Port

This parameter allows you to enable or disable the parallel port.

BASE ADDRESS

This function lets you set a logical base address for the parallel port. The options are:

- 3BCh
- 378h
- 278h

IRQ

This function lets you assign an interrupt for the parallel port. The options are IRQ 5 and 7.



The Base Address and IRQ parameters are configurable only if Parallel Port is enabled.

If you install an add-on card that has a parallel port whose address conflicts with the parallel port onboard, the system automatically disables the onboard functions.

Check the parallel port address on the add-on card and change the address to one that does not conflict.

OPERATION MODE

This item allows you to set the operation mode of the parallel port. Table 3-1 lists the different operation modes.

Table 3-1 Parallel Port Operation Mode Settings

Setting	Function
Standard Parallel Port (SPP)	Allows normal speed one-way operation
Standard and Bidirectional	Allows normal speed operation in a two-way mode
Enhanced Parallel Port (EPP)	Allows bidirectional parallel port operation at maximum speed
Extended Capabilities Port (ECP)	Allows parallel port to operate in bidirectional mode and at a speed higher than the maximum data transfer rate

ECP DMA CHANNEL

This item becomes active only if you select **Extended Capabilities Port (ECP)** as the operation mode. It allows you to assign DMA channel 1 or DMA channel 3 for the ECP parallel port function.

3.6.1.4 Onboard Floppy Disk Controller

This parameter lets you enable or disable the onboard floppy disk controller.

3.6.1.5 Onboard IDE Primary Channel

This parameter lets you enable or disable the primary IDE channel. When enabled, it allows access to the devices connected to the primary channel. When disabled, it deactivates the devices.

3.6.1.6 Onboard PS/2 Mouse (IRQ 12)

This parameter enables or disables the onboard PS/2 mouse. When enabled, it allows you to use the onboard PS/2 mouse assigned with IRQ12. When disabled, it deactivates the mouse and makes IRQ12 available for use of other devices.

3.6.1.7 Onboard SCSI1

This parameter enables or disables the onboard SCSI1 device controller. The default setting is **Enabled**.

BOOT FROM SCSI1 DEVICE

When enabled, this parameter allows the system to boot from the SCSI1 device. The default setting is **Enabled**. This item is grayed and non-configurable when the Onboard SCSI1 parameter is disabled.

3.6.1.8 Onboard SCSI2

This parameter enables or disables the onboard SCSI2 device controller. The default setting is **Enabled**.

BOOT FROM SCSI2 DEVICE

When enabled, this parameter allows the system to boot from the SCSI2 device. The default setting is **Enabled**. This item is grayed and non-configurable when the Onboard SCSI2 parameter is disabled.

3.6.2 PnP/PCI System Configuration

The PnP/PCI System Configuration allows you to specify the settings for your PCI devices. Selecting this option displays the following screen.

PnP/PCI System Configuration		Page 1/1		
PCI IRQ Setting [Auto]				
	INTA	INTB	INTC	INTD
PCI Slot 1	[--]	[--]	[--]	[--]
PCI Slot 2	[--]	[--]	[--]	[--]
PCI Slot 3	[--]	[--]	[--]	[--]
PCI Slot 4	[--]	[--]	[--]	[--]
PCI Slot 5	[--]	[--]	[--]	[--]
PCI Slot 6	[--]	[--]	[--]	[--]
PCI Slot 7	[--]	[--]	[--]	[--]
PCI OB SCSI1	[--]			
PCI OB SCSI2	[--]			
PCI IRQ Sharing [No]				
VGA Palette Snoop [Disabled]				
↑↓ = Move Highlight Bar, ← → = Change Setting, F1 = Help				

3.6.2.1 PCI IRQ Setting

This function is fixed at **Auto** setting and is nonconfigurable. It automatically configures the plug-and-play (PnP) devices installed in your system.

Refer to your manual for technical information about the PCI card.

PCI SLOTS

These parameters specify the auto-assigned interrupt for each of the PCI devices. Like the PCI IRQ Setting parameter, these are also non-configurable.

3.6.2.2 PCI IRQ Sharing

Setting this parameter to **Yes** allows you to assign the same IRQ to two different devices. To disable the feature, select **No**.



If there are no IRQs available to assign for the remaining device function, we recommend that you enable this parameter.

3.6.2.3 VGA Palette Snoop

This parameter permits you to use the palette snooping feature if you installed more than one VGA card in the system.

The VGA palette snoop function allows the control palette register (CPR) to manage and update the VGA RAM DAC (Digital Analog Converter, a color data storage) of each VGA card installed in the system. The snooping process lets the CPR send a signal to all the VGA cards so that they can update their individual RAM DACs. The signal goes through the cards continuously until all RAM DAC data have been updated. This allows display of multiple images on the screen.



Some VGA cards have required settings for this feature. Check your VGA card manual before setting this parameter.

3.6.3 Memory/Cache Configuration

The Memory/Cache Configuration allows you to specify the appropriate settings for your system memory. Selecting the option displays the following screen.

Memory/Cache Configuration	Page 1/1
Internal Cache (CPU Cache) [Enabled] Cache Scheme [Write Back] Memory at 15MB-16MB Reserved for [System]	
↑↓ = Move Highlight Bar, ← → = Change Setting, F1 = Help	

3.6.3.1 Internal Cache (CPU Cache)

This parameter enables or disables the first-level or internal memory. The default setting is **Enabled**.

3.6.3.2 Cache Scheme

This parameter allows you to select **Write back** or **Write through** for the cache mode. **Write back** updates the cache but not the memory when there is a write instruction. It updates the memory only when there is an inconsistency between the cache and the memory. **Write through** updates both the cache and the memory whenever there is a write instruction.

3.6.3.3 Memory at 15MB-16MB Reserved for

To prevent memory address conflicts between the system and expansion boards, reserve this memory range for the use of either the system or an expansion board.

3.6.4 Non-PnP ISA Device Configuration

The Non-PnP ISA Device Configuration parameters allow you to specify the settings for cards without the plug-and-play (PnP) feature.

Non-PnP ISA Device Configuration		Page 1/4
System Resources Used by Non-PnP ISA Cards		
IRQ		
IRQ 00 --- [---]	IRQ 08 --- [---]	
IRQ 01 --- [---]	IRQ 09 --- [No]	
IRQ 02 --- [---]	IRQ 10 --- [No]	
IRQ 03 --- [No]	IRQ 11 --- [No]	
IRQ 04 --- [No]	IRQ 12 --- [No]	
IRQ 05 --- [No]	IRQ 13 --- [---]	
IRQ 06 --- [---]	IRQ 14 --- [No]	
IRQ 07 --- [No]	IRQ 15 --- [No]	
↑↓ = Move Highlight Bar, ← →= Change Setting F1 = Help PgUp/PgDn = Move Screen		

Non-PnP ISA Device Configuration		Page 2/4
DMA		
DMA 0 ---- [No]	DMA 4----- [---]	
DMA 1 ---- [No]	DMA 5----- [No]	
DMA 2 ---- [---]	DMA 6----- [No]	
DMA 3 ---- [No]	DMA 7----- [No]	
Expansion ROM Region		
C8000h - CBFFFh -----	[No]	
CC000h - CFFFFh -----	[No]	
D0000h - D3FFFh -----	[No]	
D4000h - D7FFFh -----	[No]	
D8000h - DBFFFh -----	[No]	
DC000h - DFFFFh -----	[No]	
↑↓ = Move Highlight Bar, ← →= Change Setting F1 = Help PgUp/PgDn = Move Screen		

I/O Region

100h-10Fh----	[No]	1E0h-1EFh ---	[No]
110h-11Fh----	[No]	1F0h-1FFh ---	[---]
120h-12Fh----	[No]	200h-20Fh ---	[No]
130h-13Fh----	[No]	210h-21Fh ---	[No]
140h-14Fh----	[No]	220h-22Fh ---	[No]
150h-15Fh----	[No]	230h-23Fh ---	[No]
160h-16Fh----	[No]	240h-24Fh ---	[No]
170h-17Fh----	[---]	250h-25Fh ---	[No]
180h-18Fh----	[No]	260h-26Fh ---	[No]
190h-19Fh----	[No]	270h-27Fh ---	[No]
1A0h-1AFh----	[No]	280h-28Fh ---	[No]
1B0h-1BFh----	[No]	290h-29Fh ---	[No]
1C0h-1CFh----	[No]	2A0h-2AFh ---	[No]
1D0h-1DFh----	[No]	2B0h-2BFh ---	[No]

↑↓ = Move Highlight Bar, ← → = Change Setting F1 = Help
PgUp/PgDn = Move Screen

I/O Region

2C0h-2CFh-----	[No]	3A0h-3AFh ---	[No]
2D0h-2DFh-----	[No]	3B0h-3BFh ---	[No]
2E0h-2EFh-----	[No]	3C0h-3CFh ---	[No]
2F0h-2FFh-----	[No]	3D0h-3DFh ---	[No]
300h-30Fh-----	[No]	3E0h-3EFh ---	[No]
310h-31Fh-----	[No]	3F0h-3FFh ---	[No]
320h-32Fh-----	[No]		
330h-33Fh-----	[No]		
340h-34Fh-----	[No]		
350h-35Fh-----	[No]		
360h-36Fh-----	[No]		
370h-37Fh-----	[No]		
380h-38Fh-----	[No]		
390h-39Fh-----	[No]		

↑↓ = Move Highlight Bar, ← → = Change Setting F1 = Help
PgUp/PgDn = Move Screen



Refer to your non-PnP ISA device manual when setting the following parameters.

3.6.4.1 IRQ/DMA

These items allow you to assign specific IRQ and DMA channels to non-PnP ISA devices. The system will not use such IRQ and DMA channels when it automatically assigns channels to PnP devices.

3.6.4.2 Expansion ROM Region

These items specify the memory regions available for add-on card use. It allows you to manually assign specific regions to non-PnP devices so that the system will not use those regions anymore when it automatically configures PnP devices.

3.6.4.3 I/O Region

The items under this parameter allow you to reserve 16-byte memory address ranges for non-PnP devices. When the system configures PnP devices, the address ranges that you marked will not be used anymore.

You can assign memory addresses to non-PnP devices at random as long as you cover the address range required by the device. For example, for a card that requires 178h-188h address, you have to set regions 170h-17Fh and 180h-18Fh to **yes**.

3.6.5 Chipset Configuration

The Chipset Configuration option normally does not appear under the Advanced Configuration screen. To display the Chipset Configuration menus, press F4.

The Chipset Configuration parameters allow changes to the system controller chipset. For details on the parameters, refer to the Intel data sheet.

Chipset Configuration		Page 1/3
P6 CPU Bus Configuration		
BINIT# Signal	[Ignore]	
BERR# Signal	[Enabled]	
AERR# Signal	[Ignore]	
In-order Queue Depth	[8]	
PCI Mode	[Disabled]	
MP Compliant Revision	[V1.4]	
↑↓ = Move Highlight Bar, ← → = Change Setting, F1 = Help PgUp/PgDn = Move Screen		

Chipset Configuration		Page 2/3
OPB(s) Setting		
ECC/Parity Mode Selection	[Enabled]	
PCI to P6 Bus Write Posting	[Enabled]	
P6 Bus to PCI Write Posting	[Enabled]	
P6 Bus to PCI Write Burst	[Enabled]	
PCI Line Read		
PCI Memory Read Cmd	[Enabled]	
Pre-fetch PCI Memory Read Cmd	[Enabled]	
PCI Memory Read Multi-Cmd	[Enabled]	
Pre-fetch PCI Memory Read Multi-Cmd	[Enabled]	
PCI Memory Read Line Cmd	[Enabled]	
Pre-fetch PCI Memory Read Line Cmd	[Enabled]	
Defer Reply	[Disabled]	
↑↓ = Move Highlight Bar, ← → = Change Setting, F1 = Help PgUp/PgDn = Move Screen		

OMC Setting

Page Open Policy[Enabled]
Read-Around-Write (OMC level)[Enabled]
Ext-Read-Around-Write (MIC level)[Enabled]
Memory Single-Bit Error Correcting[Enabled]
Refresh Stagger[7]

PCEB Setting

Guaranteed Access Time[Enabled]
PCI Highest Priority Setting[Rotate]
EISA-to-PCI Line Buffer[Enabled]

PCI Latency Timer Initial Value (in 8 system clk)

Slot 1, 2, 3, 4[60h]
Slot 5, 6, 7[60h]

↑↓ = Move Highlight Bar, ← → = Change Setting, F1 = Help
PgUp/PgDn = Move Screen

3.7 System Security Setup

The Setup program has a number of security features to prevent unauthorized access to the system and its data.

The following screen appears if select System Security from the main menu.

System Security		Page 1/1
IDE Disk Drive Control		
Floppy Drive	[Normal]	
IDE Hard Disk Drive ...	[Normal]	
Setup Password.....	[None]	
Power On Password.....	[None]	
Operation Mode.....	[Normal]	
↑↓ = Move Highlight Bar, ← → = Change Setting, F1 = Help		

3.7.1 IDE Disk Drive Control

The disk drive control features allow you to control the floppy drive or the hard disk drive boot function to prevent loading operating systems or other programs from a certain drive while the other drives are operational.

Table 3-2 lists the drive control settings and their corresponding functions.

Table 3-2 Drive Control Settings

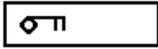
Setting	Description
Floppy Drive	
Normal	Diskette drive functions normally
Write Protect All Sectors	Disables the write function on all sectors
Write Protect Boot Sector	Disables the write function only on the boot sector
Disabled	Disables all diskette functions
IDE Hard Disk Drive	
Normal	Hard disk drive functions normally
Write Protect All Sectors	Disables the write function on all sectors
Write Protect Boot Sector	Disables the write function only on the boot sector
Disabled	Disables all hard disk functions

3.7.2 Setup Password

The Setup Password prevents unauthorized access to the BIOS utility.

3.7.2.1 Setting a Password

1. Make sure that JP11 is set to 1-2 (check password). This is the default setting.
2. Enter BIOS utility and select System Security.
3. Highlight the Setup Password parameter and press the  or  key. The password prompt appears:

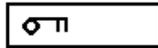
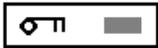


4. Type a password. The password may consist of up to seven characters.



Be very careful when typing your password because the characters do not appear on the screen.

5. Press . A prompt asks you to retype the password to verify your first entry.



6. Retype the password then press .

After setting the password, the system automatically sets the Setup Password parameter to **Present**.

7. Press  to exit the System Security screen and return to the main menu.
8. Press  to exit the BIOS utility. A dialog box appears asking if you want to save the CMOS data.
9. Select **Yes** to save the changes and reboot the system.

The next time you want to enter the BIOS utility, you must key-in your Setup password.

3.7.2.2 Changing or Removing the Setup Password

Should you want to change your setup password, do the following:

1. Enter the BIOS utility and select System Security.
2. Highlight the Setup Password parameter.
3. Press  or  to display the password prompt and key-in a new password.

or

Press  or  and select **None** to remove the existing password.

4. Press  to exit the System Security screen and return to the main menu.
5. Press  to exit the BIOS utility. A dialog box appears asking if you want to save the CMOS data.
6. Select **Yes** to save the changes.

3.7.2.3 Bypassing the Setup Password

If you forget your setup password, you can bypass the password security feature by hardware. Follow these steps to bypass the password:

1. Turn off and unplug the system.
2. Open the system housing and JP11 is set to 2-3 to bypass the password function.
3. Turn on the system and enter the BIOS utility. This time, the system does not require you to type in a password.



*You can either change the existing Setup password or remove it by selecting **None**. Refer to the previous section for the procedure.*

3.7.3 Power-on Password

The Power-on Password secures your system against unauthorized use. Once you set this password, you have to type it whenever you boot the system. To set this password, enter the BIOS utility, select System Security, then highlight the Power-on Password parameter. Follow the same procedure as in setting the Setup password.



Make sure that JP11 is set to 1-2 to enable the Power-on password.

3.7.3.1 Operation Mode

This function lets you enable or disable the password prompt display. When set to **Normal**, the password prompt appears before the system boots. When set to **Network**, the password prompt does not appear; however, the keyboard is locked after the system has booted and remains locked until the correct password is entered.

3.8 Date and Time

The real-time clock keeps the system date and time. After setting the date and time, you do not need to enter them every time you turn on the system. As long as the internal battery remains good (approximately seven years) and connected, the clock continues to keep the date and time accurately even when the power is off.

The following screen appears if you select Date and Time from the main menu.

Date and Time		Page 1/1
Date	[xxx xx xx, 199x]	
Time	[xx:xx:xx]	
↑↓ = Move Highlight Bar, ← → = Change Setting, F1 = Help		

3.8.1 Date

Highlight the items on the Date parameter and press  or  to set the date following the weekday-month-day-year format.

Valid values for weekday, month, day, and year are:

- Week days **Sun, Mon, Tue, Wed, Thu, Fri, Sat**
- Month **1 to 12**
- Day **1 to 31**
- Year ******

3.8.2 Time

Highlight the items on the Time parameter and press  or  to set the time following the hour-minute-second format.

Valid values for hour, minute, and second are:

- Hour **00 to 23**
- Minute **00 to 59**
- Second **00 to 59**

3.9 Remote Diagnostic Configuration

The Remote Diagnostic Configuration parameters allow you to configure your RDM settings. Refer to the RDM User's Guide for information on RDM.

3.10 Load Default Settings

Use this option to load the default settings for the optimized system configuration. When you load the default settings, some of the parameters are grayed-out with their fixed settings. These grayed parameters are not user-configurable.

The following dialog box appears when you select Load Setup Default Settings from the main menu.

```
Do you want to load default settings?  
  
[Yes]      [No]
```

Select **yes** to load the default settings.

Select **no** to ignore the message and return to the BIOS utility.

3.11 Abort Settings Change

Use this option to disregard the your changes to the BIOS and reload your previous settings.

The following dialog box appears when you select Abort Settings Change from the main menu.

```
Do you want to load previous settings?  
  
[Yes]      [No]
```

Select **yes** to disregard your changes and reload your previous settings. After reloading the previous settings, the main menu appears on screen.

Select **no** to ignore the message and return to the BIOS utility.

3.12 Reset Non-PnP ISA Device Setting

Selecting this option from the main menu resets all the Non-PnP ISA Device Configuration parameters to their default settings.

Refer to section 3.6.4 for details on the Non-PnP ISA device parameters.

3.13 Leaving Setup

Examine the system configuration values. When you are satisfied that all the values are correct, write them down. Store the recorded values in a safe place. In the future, if the battery loses power or the CMOS chip is damaged, you will know what values to enter when you rerun Setup.

Press **[ESC]** to leave the system configuration setup. The following screen appears:

```
Settings have been changed.  
Do you want to save CMOS settings?  
  
[Yes]          [No]
```

Use the arrow keys to select your response. Select **yes** to store the new data in CMOS. Select **no** to retain the old configuration values. Press **[ENTER]**.

Model Definition

Model Name : X3
 Brand Name : Acer
 Product Name : AcerAltos 19000Pro4
 Description : Quad Pentium Pro Server
 Model No. : F X XX X X - X X X

F X XX X X - X X X

- 0 : 400W SPS*1, w/o UPS, BP-W7 (L)*1, (TRAY & IFW)*7
- 1 : 400W SPS*2, w/ UPS, BP-W7 (L)*1, (TRAY & IFW)*7
- 2 : 400W SPS*2, w/o UPS, BP-W7 (L)*1, (TRAY & IFW)*7
- 3 : 400W SPS*2, w/ UPS, BP-W7 (L)*1 (R)*1, (TRAY & IFW)*14
- 4 : 400W SPS*2, w/o UPS, BP-W7 (L)*1 (R)*1, (TRAY & IFW)*14
- 5 : 400W SPS*3, w/ UPS, BP-W7 (L)*1 (R)*1, (TRAY & IFW)*14
- 6 : 400W SPS*3, w/o UPS, BP-W7 (L)*1 (R)*1, (TRAY & IFW)*14
- 7 : 400W SPS*2, w/o UPS & BP-W7 (L) (R) & (TRAY & IFW)
- 8 : w/o 400W SPS & UPS, BP-W7 (R)*1, (TRAY & IFW)*7

- 0 : 32-MB DIMM*2
- 1 : 32-MB DIMM*4
- 2 : 64-MB DIMM*2
- 3 : 32-MB DIMM*8
- 4 : 64-MB DIMM*4
- 5 : 128-MB DIMM*2
- 6 : 128-MB DIMM*4
- 7 : 64-MB DIMM*16
- 8 : 128-MB DIMM*16
- 9 : w/o DIMM

- 0 : (200/512K CACHE) * 1
- 1 : (200/512K CACHE) * 2
- 2 : (200/1024K CACHE) * 2
- 3 : (200/256K CACHE) * 4
- 4 : (200/512K CACHE) * 4
- 5 : (200/1024K CACHE) * 4

Q : X3 SYSTEM BOARD

X : IDX-2

20: 200/66 MHz

6 : PENTIUM PRO

Spare Parts List

Table B-1 *IDX-2 Housing Spare Parts*

No.	Part Name	Part No. *	Location	Quantity **
1	FAN DC12V 8*8*2.5 DFB0812M-R00	23.10007.111		5
2	FAN DC12V WFB1212M 250MM	23.10020.031		1
3	BUZZER QMX-05 W/O LABEL	23.60004.001	B1	50
4	C.A 10P 2C 730MM IDX-2	50.03601.001		50
5	C.A 10P 2C 540MM IDX-2	50.03601.011		50
6	W.A 2P 2C 820MM IDX-2	50.03602.001		50
7	C.A 14P 2C 780MM IDX-2	50.03603.001		5
8	C.A 16/12P 760MM IDX-2	50.03604.001		5
9	C.A 50P 4CONN 750+150+150MM	50.58607.002	(NARROW SCSI CABLE)	5
10	C.A 8P/4P*4 55CM	50.59901.012	(J12 FOR FDD/HDD)	5
11	CABLE ASSY 14P/14P 52CM	50.59903.002		50
12	C.A 14P/14P 65CM PWR SUB/F PNL	50.59903.022	(POWER SUBSYSTEM J11)	50
13	C.A 14P/14P 68CM F.P BD/SCSI	50.59903.042	(SCSI B.P. BD)	50
14	C.A 34P/34P 70CM MB/F PNL BD	50.59904.022	(FRONT PANEL BD)	50
15	C.A 34P/34P 47CM MB FLOP/FDD	50.59904.032	(FLOPPY)	50
16	C.A 40P 3C 59CM MB/HDD	50.59905.012	(IDE)	5
17	X3 FRONT PANEL BOARD 95381-2	55.59905.001		1
18	FDD 1.44 JU-256A046PL ACER 3M	56.01057.193		1
19	SPS 400W TECTR TC65SD-1123 V.D	56.04400.K11		1
20	LCD MODULE ED16222YLY EMERGING	56.07599.001		1
21	ASSY HOUSING IDX-2	60.03602.011		1
22	ASSY LOWER CASE IDX-2	60.03603.011		1
23	ASSY PANEL FDD 002 IDX-2	60.59903.001		5
24	ASSY DOOR FDD IDX-2	60.59904.001		1
25	ASSY PANEL HDD IDX-2	60.59905.001		1
26	ASSY SIDE DOOR L 002 IDX-2	60.59907.001		1

* Part numbers are subject to change without notice. Contact the Acer Spare Parts department for updates.

** Minimum ordering quantity

Table B-1 *IDX-2 Housing Spare Parts (continued)*

No.	Part Name	Part No. *	Location	Quantity **
27	ASSY SIDE DOOR R 002 IDX-2	60.59908.001		1
28	ASSY LOWER CASE IDX-2	60.59912.002		1
29	ASSY RDM 3.01 LED	60.02512.001		1
30	BP-W7 LEFT (-2)	55.59902.002		1
31	BP-W7 RIGHT (-2)	55.59902.012		1
32	CA 68P 2CONN 450MM IDUN	50.02506.001	(optional)	5
33	RDM BOARD V3.1 95422-3M	55.58704.071		1
34	CHARGER MODULE TECTROL X3	90.58728.003		1
35	X3 BATTERY BOX W/ BATTERY	91.58728.011		1

* Part numbers are subject to change without notice. Contact the Acer Spare Parts department for updates.

** Minimum ordering quantity

Table B-2 X3 System Board Spare Parts

No.	Part Name	Part No. *	Location	Quantity **
1	IC CPU INTEL P6 200MHZ PGA512K	01.I00P6.K0A		1
2	IC CPU GJ80521EX 200 1M/CACHE	01.I00P6.K0B		
3	IC EEPROM 29EE020-150 256K*8 5V	02.29020.060	U101	1
4	CONVERTER DC/DC 073-20715-02	19.21038.001		1
5	HOLDER BATTERY FOR CR2032 2012	22.70006.071	BT1	5
6	BATTERY LI 3V CR2032 200MAH	23.20023.001	BT1	50
7	XTAL 32.768KHZ 12.5PF D3*8L	23.30030.011	X3	50
8	XTAL 14.31818MHZ 32P 30PPM H5	23.31001.001	X1 X2	50
9	BUZZER QMX-05 W/O LABEL	23.60004.001	BU1	50
10	OSC 40MHZ	24.30007.001	X4	50
11	HEAT SINK REGULATOR COPR P1	34.41701.001	HT1	50
12	X3 MAIN BOARD	55.59901.001		1
13	IC CLK GEN CY2291-104 SO-W 20P	71.02291.00B	U40	5
14	IC SCSI CTRL AIC-7880 MQFP160P	71.07880.009	U111, U112	1
15	IC VGA CHIP 264VT2 (215VT2CA44)	71.264VT.F0E	U38	1
16	IC I/O CTRL FDC37C935 V.D QFP	71.37C93.B0E	U44	5
17	IC CLK GEN W49C65-04 SSOP 48P	71.49C65.A0I	U32	5
18	IC SRAM 6264 100NS 8K*8 SO-W	72.06264.042	U94	5
19	IC EEPROM 24C08 2K SO-N 8P	72.24C08.001	U1	50
20	IC DRAM 514265J-60 256K*16 EDO	72.54265.20C	U42, U51	5
21	IC EEPROM 93C56 256*8 SO-N 8P	72.93C56.001	U121	50
22	IC BUF DRV 74LVT16244 SSOP 48P	73.16244.027	U21, U60	5
23	FAN-SINK (FREQ/THERRMISTOR)X3	90.00028.389		5
24	IC CMOS 74HCT08 SO-N 14P	73.07408.0B1	U19	50
25	CONVERTER DC/DC 1M	19.21038.011		1

* Part numbers are subject to change without notice. Contact the Acer Spare Parts department for updates.

** Minimum ordering quantity

Table B-3 X3 Memory Board Spare Parts

No.	Part Name	Part No. *	Location	Quantity **
1	SKT DIMM 168P ST 71736-0011	22.10220.168		5
2	X1B MEMORY BD W/O DIMM	55.58702.031		1
3	DIMM 32MB (4M*4*18) EDO/ECC SAMSUN	55.11019.161		1
4	DIMM 64MB (4M*4*36) EDO/ECC SAMSUN	55.11019.171		1
5	128 MB (16M*4*18) EDO/ECC DIMM	55.11019.D81		1
6	IC DRAM 4M*4-6 EDO 3.3V 2K/RF	72.04104.209	U1-18	5
7	IC EEPROM 24C08 2K SO-N 8P	72.24C08.001	U17	50
8	IC BUF DRV 74LVT16244 SSOP 48P	73.16244.027	U1, U2, U3, U4, U9, U10, U11, U12, U13, U14	5

* Part numbers are subject to change without notice. Contact the Acer Spare Parts department for updates.

** Minimum ordering quantity

Schematics

1.1.1 System Board

Pages C-1a to C52a

1. LINK
2. PRIMARY PCI SLOT
3. SECONDARY PCI SLOT
4. SCSI CONTROLLER_1
5. SCSI CONTROLLER_2
6. SCSI CONNECTOR
7. EISA SLOT
8. EISA RESISTORS
9. EISA SA LATCH, XD&IO BUFFER
10. FLASH ROM, NVRAM
11. POWER_GD, BUZZER, LED, RST_CKT
12. POWER CNN
13. SMC 935
14. COM, KEYMOUSE, FDD, IDE
15. VGA and PRN CONNECTOR
16. 264 VT/GT
17. DISPLAY MEMORY
18. EISA CLK, APIC CLK
19. PCI CLK
20. P6 CLK
21. PCEB
22. ESC
23. SIOA, P6 P7 ARBITER
24. OPB 1
25. OPB 2
26. OMC_DC
27. OMC_DP
28. P6 SIDEBAND SIGNALS
29. GTL TERMINATION
30. MEMORY BUS
31. CPU 1
32. CPU 2
33. CPU 3
34. CPU 4
35. ITP AND BOUNDARY SCAN CHAIN
36. VRM CONNECTOR
37. SLOT DECOUP CAP
38. GENERIC DECOUP CAP
39. P6 VCCP DECOUP CAP
40. GTL/VREF DECOUP CAP
41. ORION DECOUP CAP
42. POWER PLANE DECOUP CAP
43. ASM(LM78-1), FEATURE CONN
44. ASM(LM78-2)
45. FUSE (I2C PORT 20), PORT 4A4 (I2C PORT 21,22)
46. PCI COUNTER, DECODER
47. PORT 4R1(FAN), 4R0
48. PORT 4A5, 4A7
49. IRQ MAPPER
50. FRONT PANEL
51. RDM
52. SHUTDOWN

1.1.2 Front Panel Board

Pages C-1b to C-5b

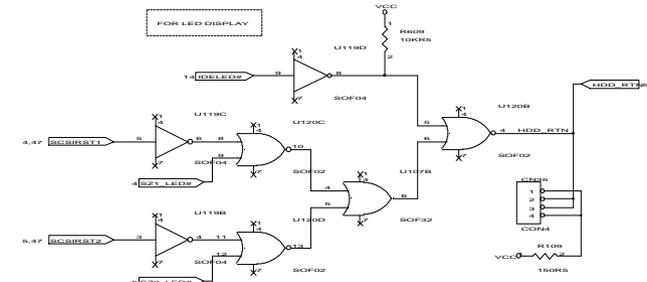
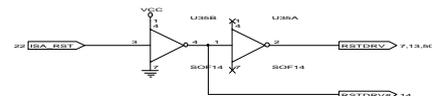
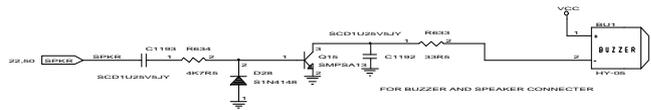
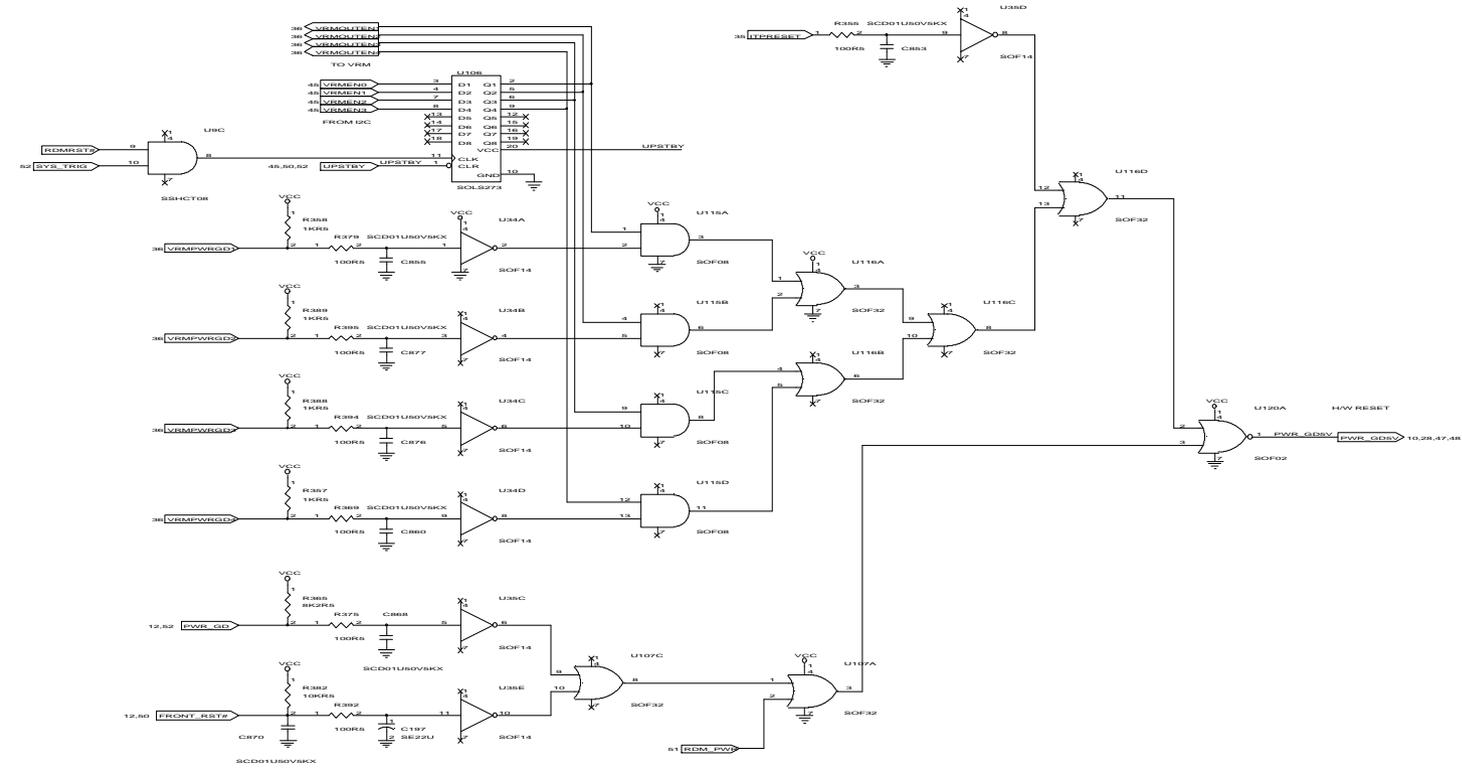
1. PS/BP interface
2. Fault LED, speaker
3. 180K OSC, 5V standby reset
4. Mainboard interface
5. Push-SW/LCD/LED

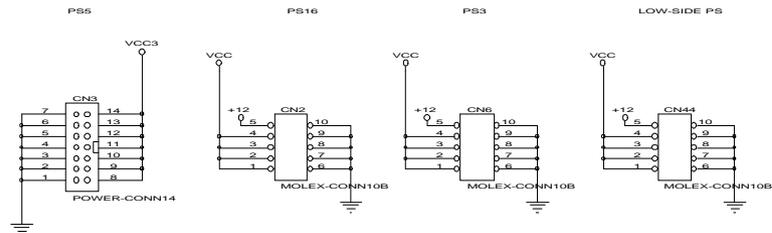
Memory Board

Pages C-1c to C-20c

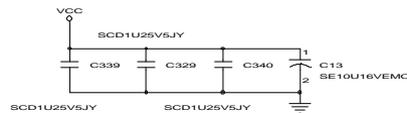
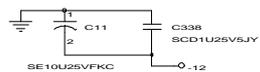
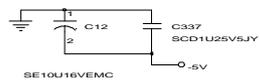
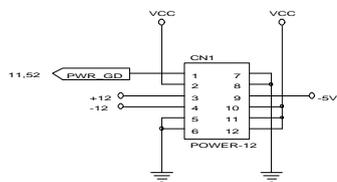
1. DIMM MEM BOARD LINK
2. GOLDEN FINGERS
3. MIC1, 2
4. MIC3, 4
5. RAS BUFFER
6. CAS BUFFER
7. WE BUFFER
8. MA BUFFER 1
9. MA BUFFER 2
10. BANK 1, 2
11. BANK 3, 4
12. BANK 5, 6
13. BANK 7, 8
14. BANK 9, 10
15. BANK 11, 12
16. BANK 13, 14
17. BANK 15, 16
18. DIMM DECOUP1
19. DIMM DECOUP2

20. MIC DECOUPLING

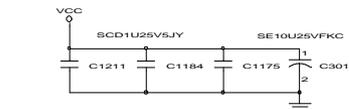
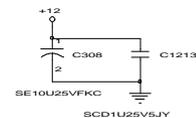




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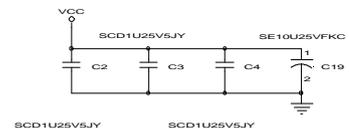
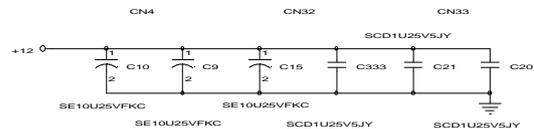
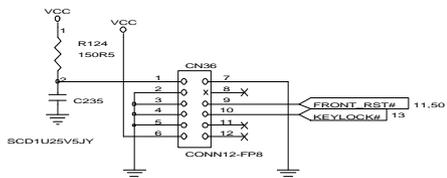


CN4

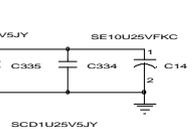
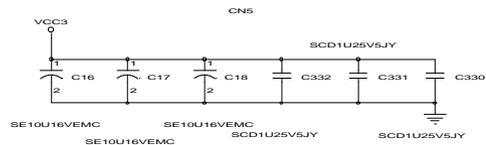


CN41

EXTENDED-CONTROLLER CNN

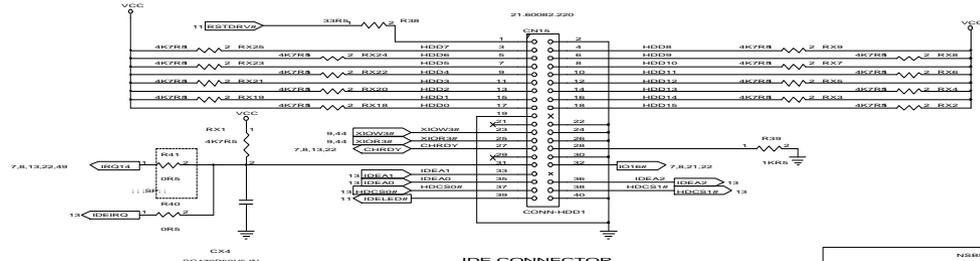
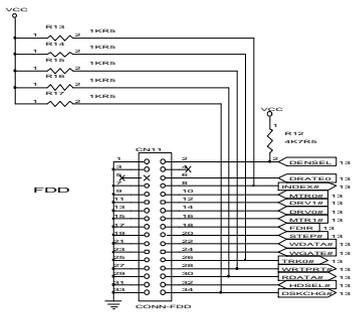
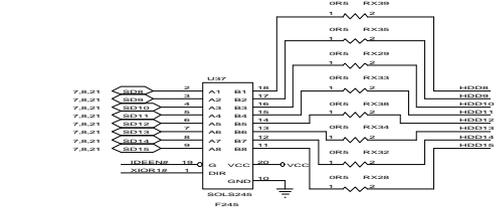
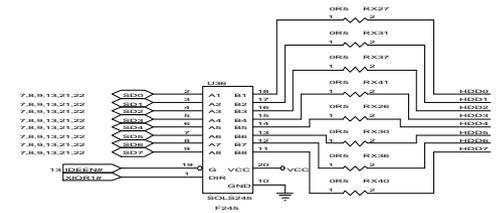
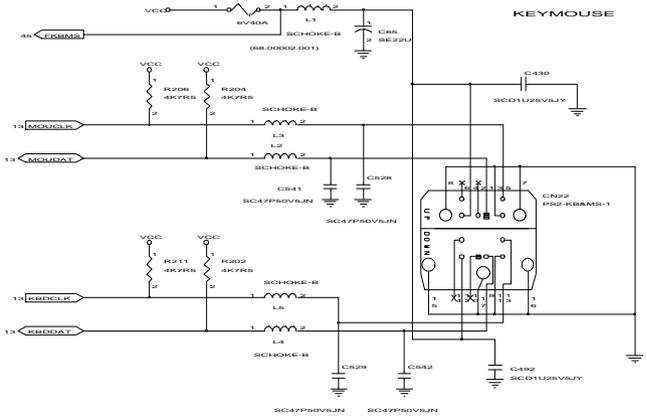
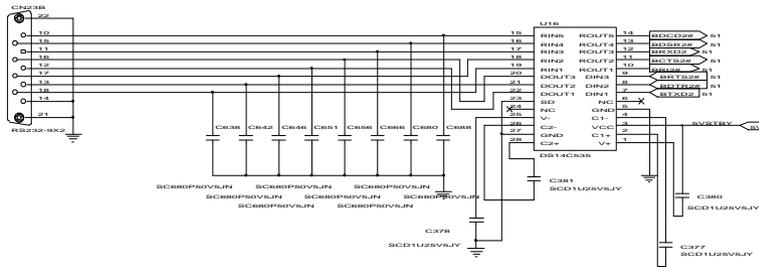
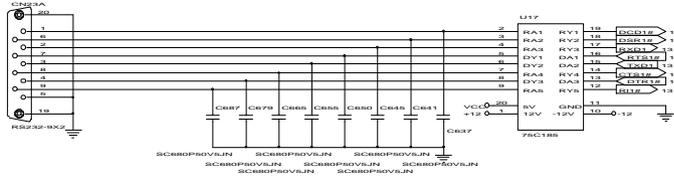


CN32



CN33

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POWER CNN		
Size	Document Number	REV
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Date:	October 16, 1997	Sheet 12 of 52

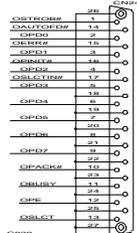
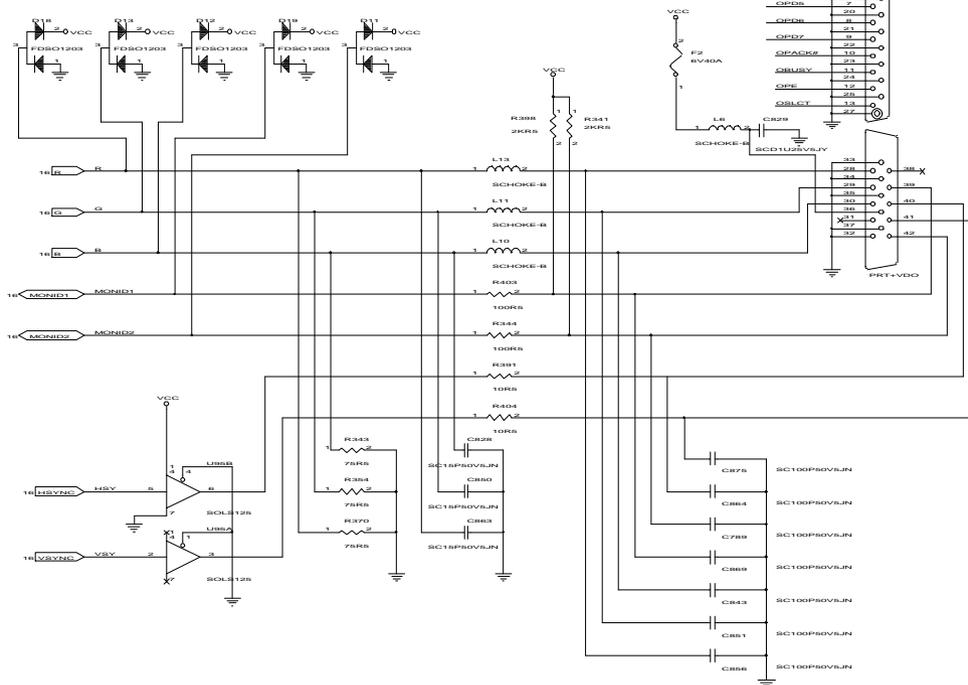
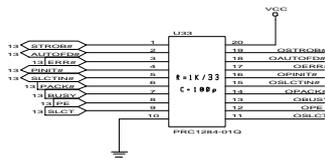
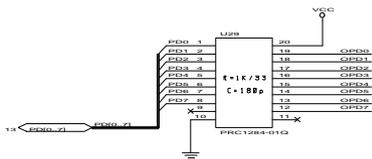


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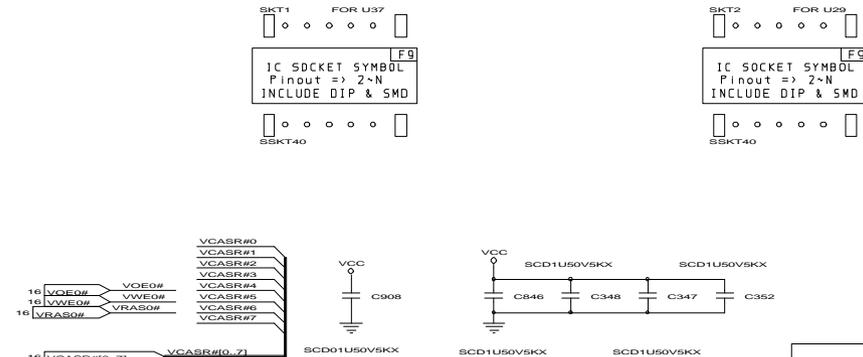
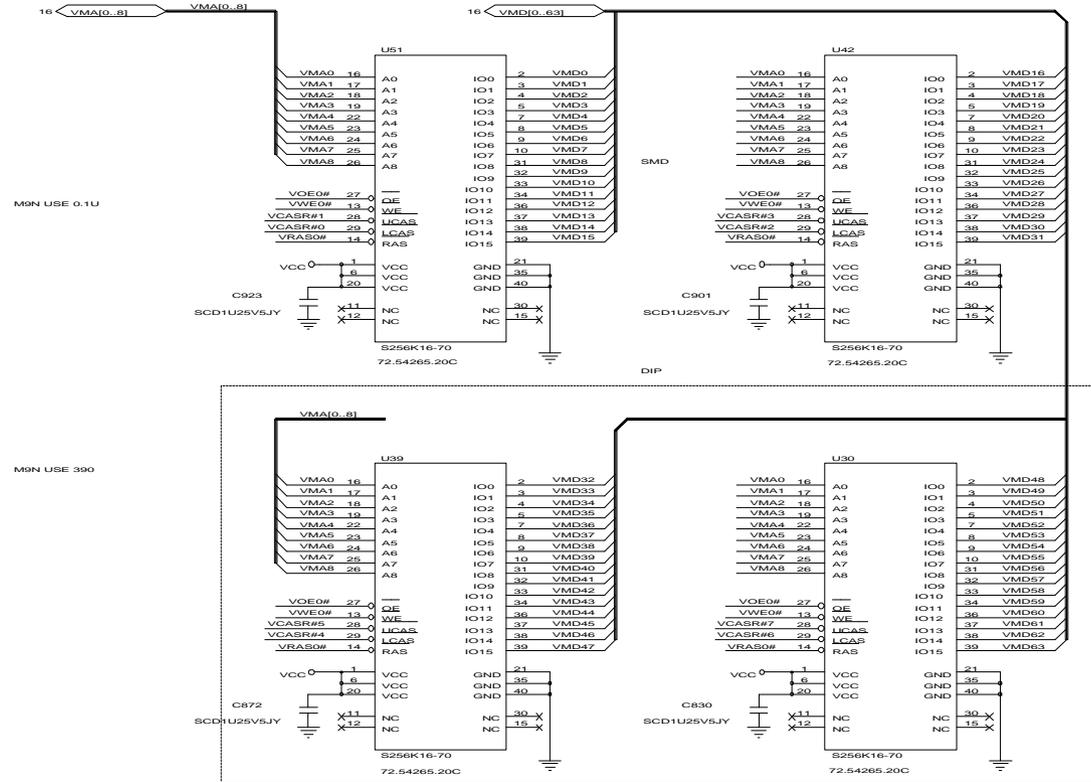
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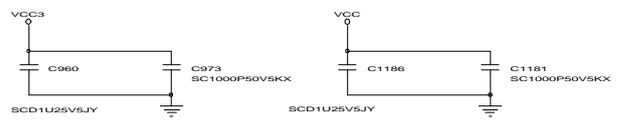
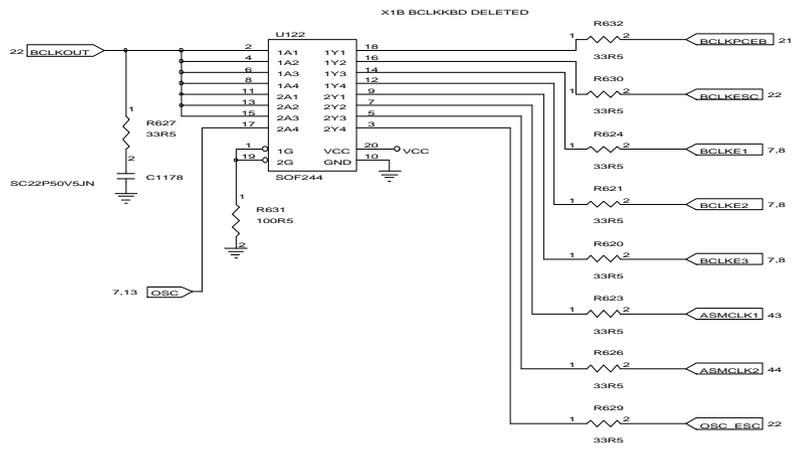
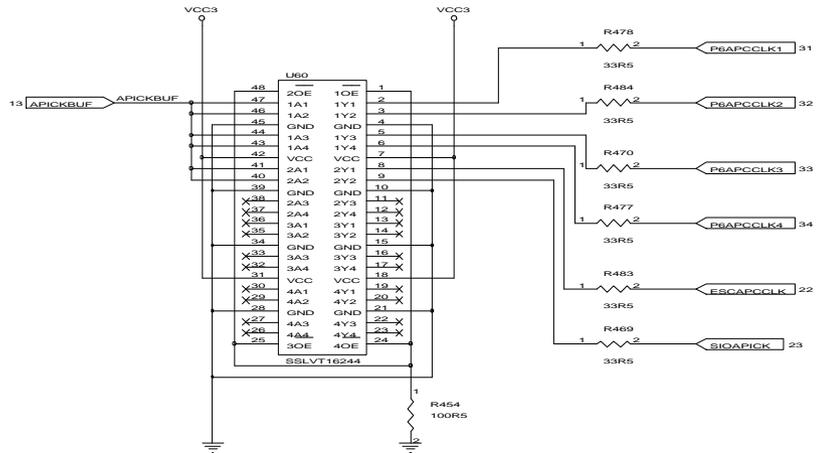
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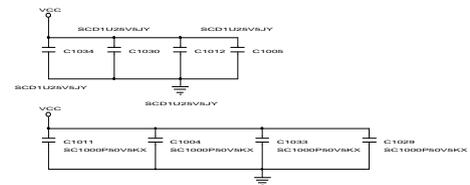
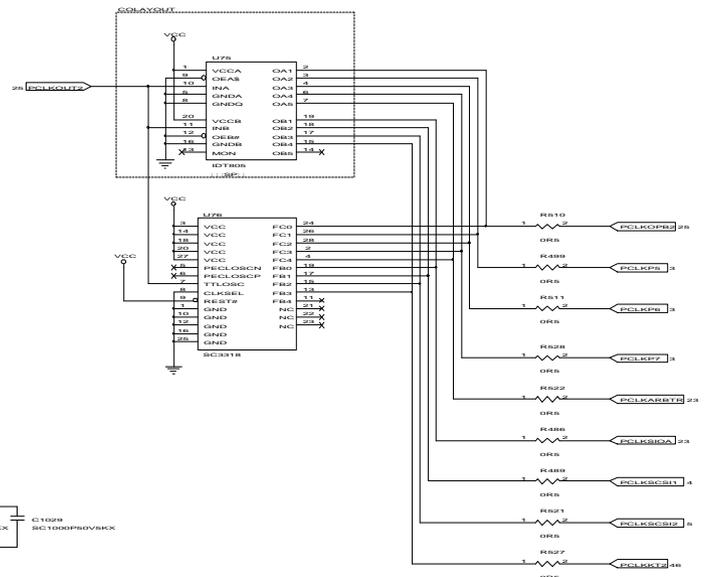
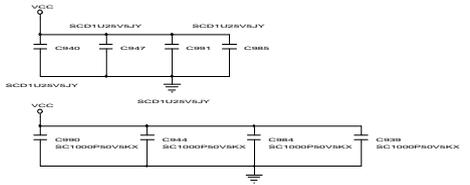
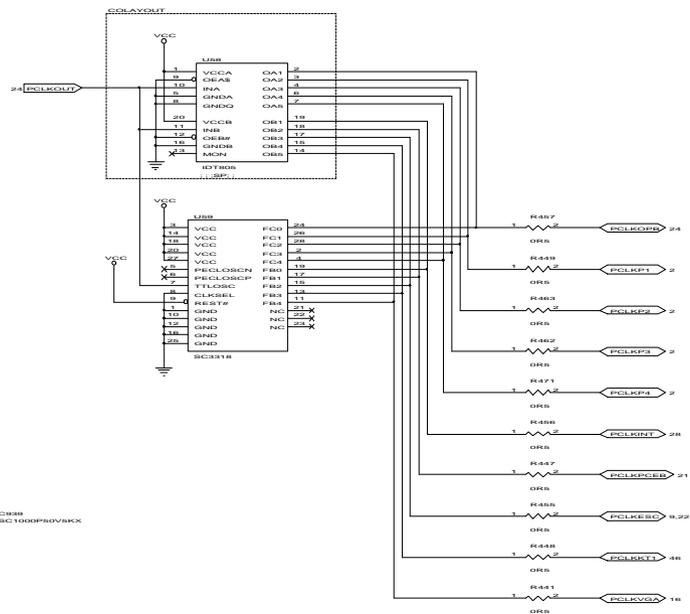


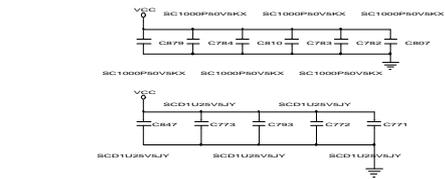
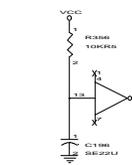
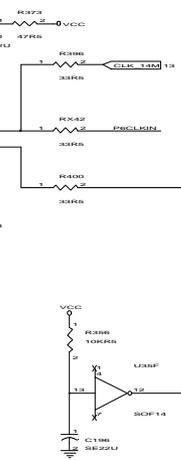
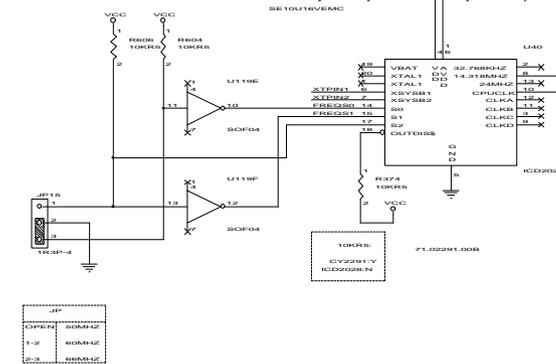
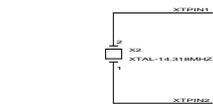
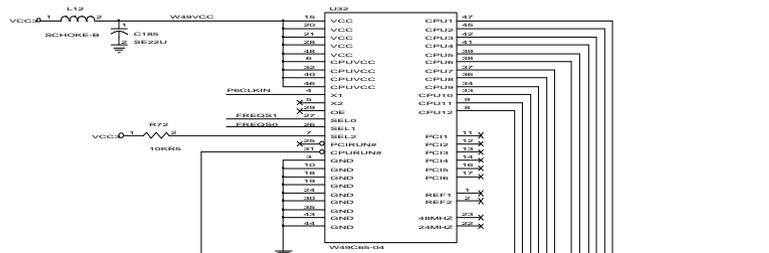
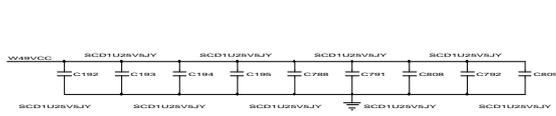
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M3	✓		✓	
M4		✓		✓
M5	0.01U	TOR	0.01U	TOR
M6	0.1U	OR	0.1U	OR
M7		✓		✓
M8	✓		✓	
M9				
M10	✓			
M11				
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M13	✓			
M14	✓			
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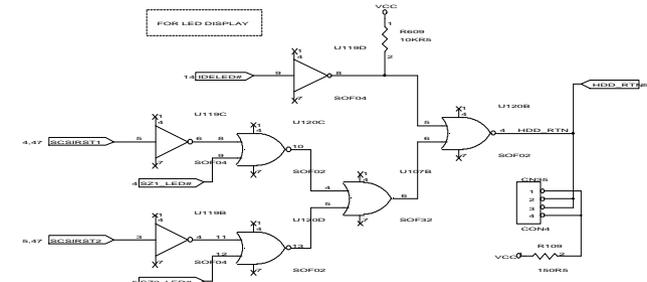
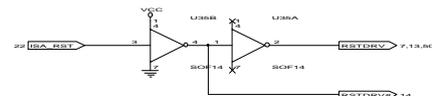
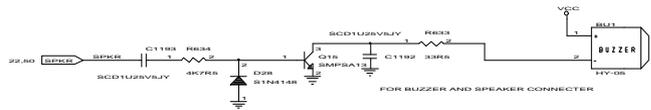
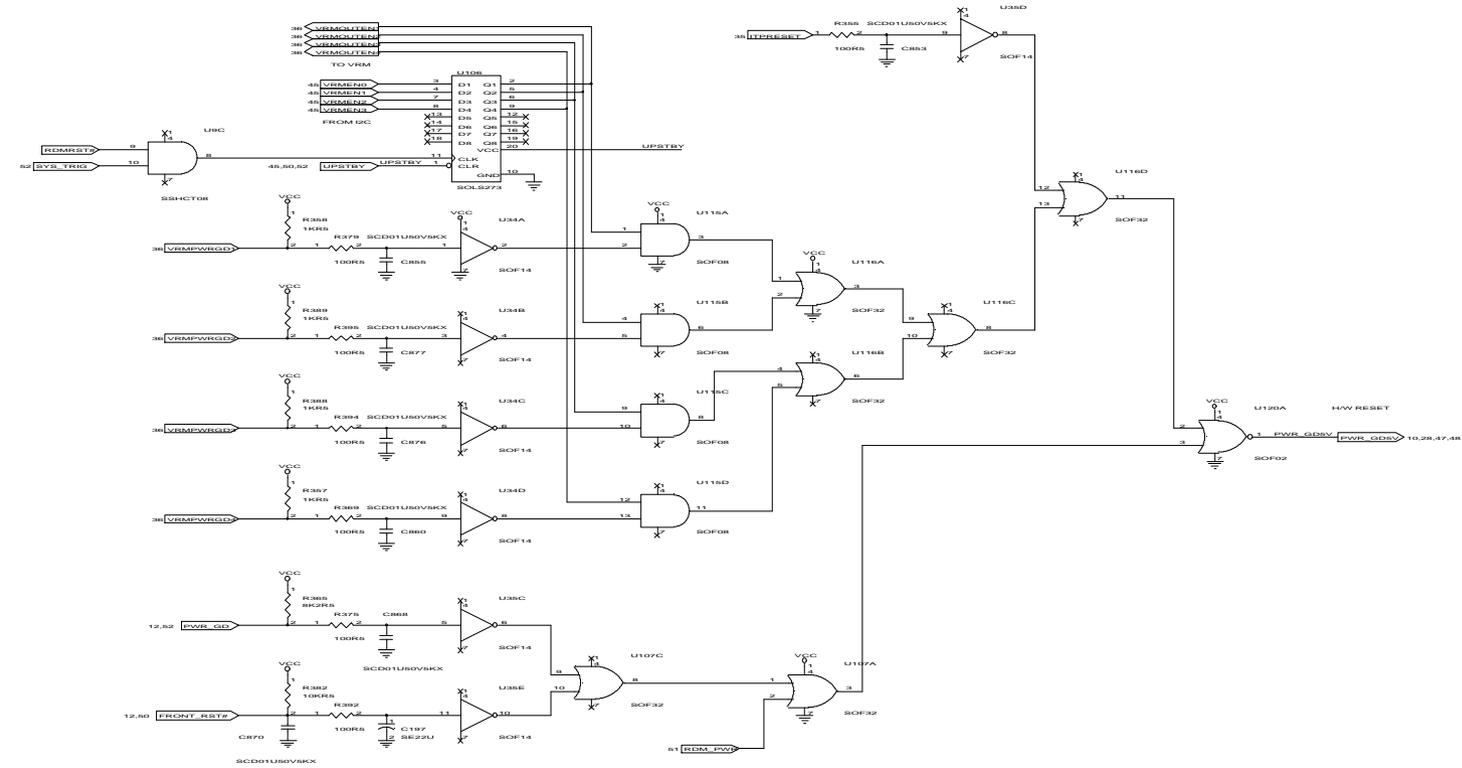


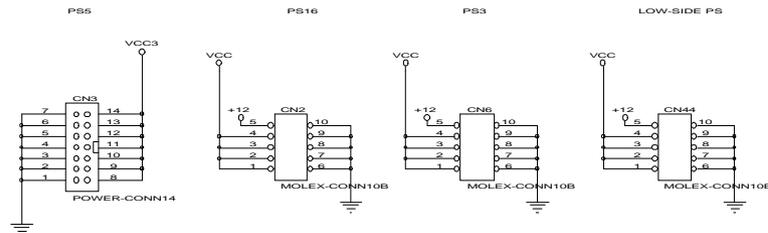
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Date:	October 16, 1997	Sheet	17 of 63



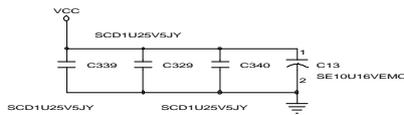
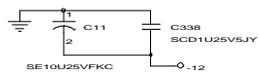
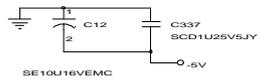
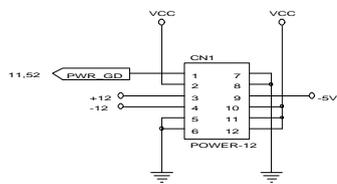




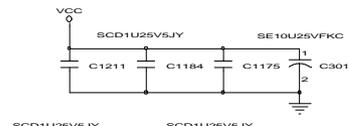
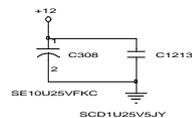




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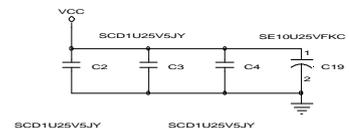
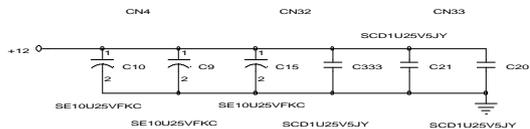
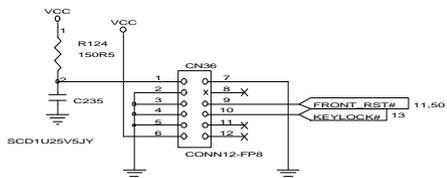


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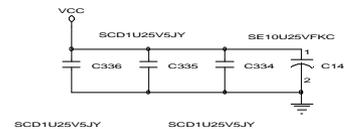
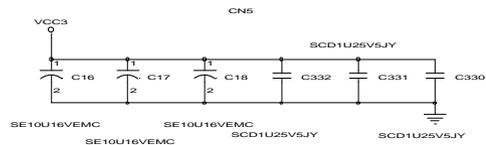


CN41

EXTENDED-CONTROLLER CNN

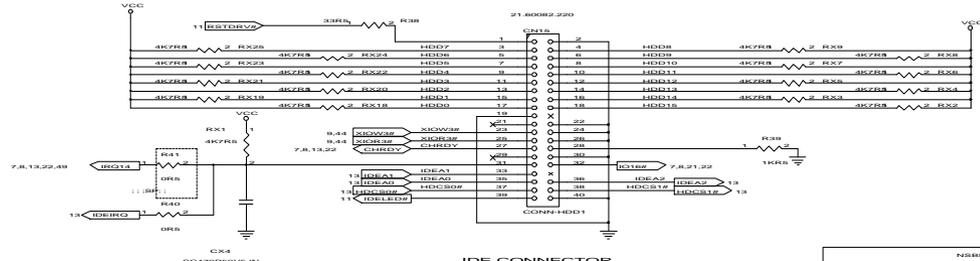
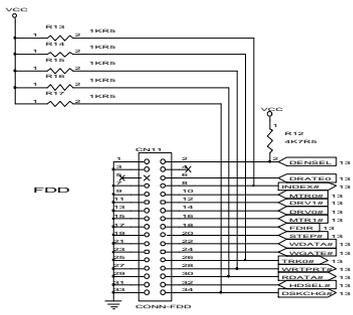
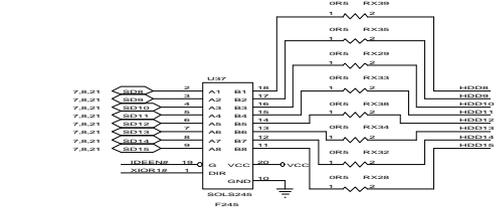
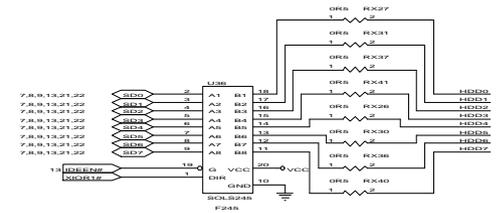
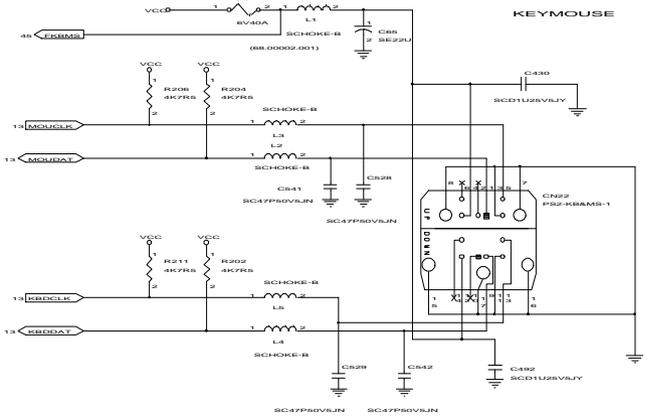
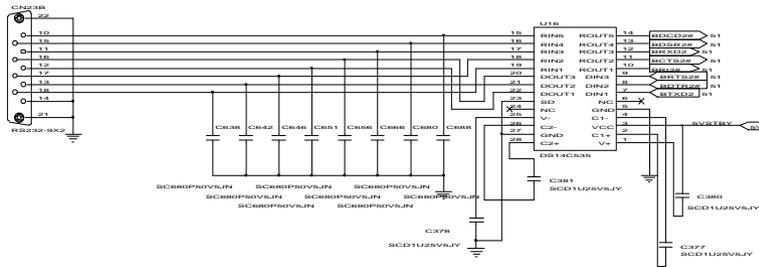
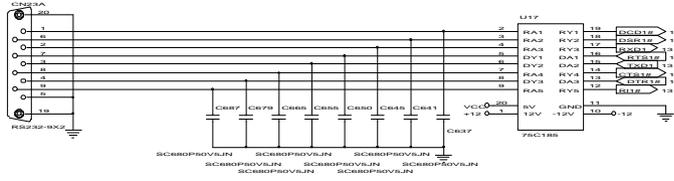


CN32



CN33

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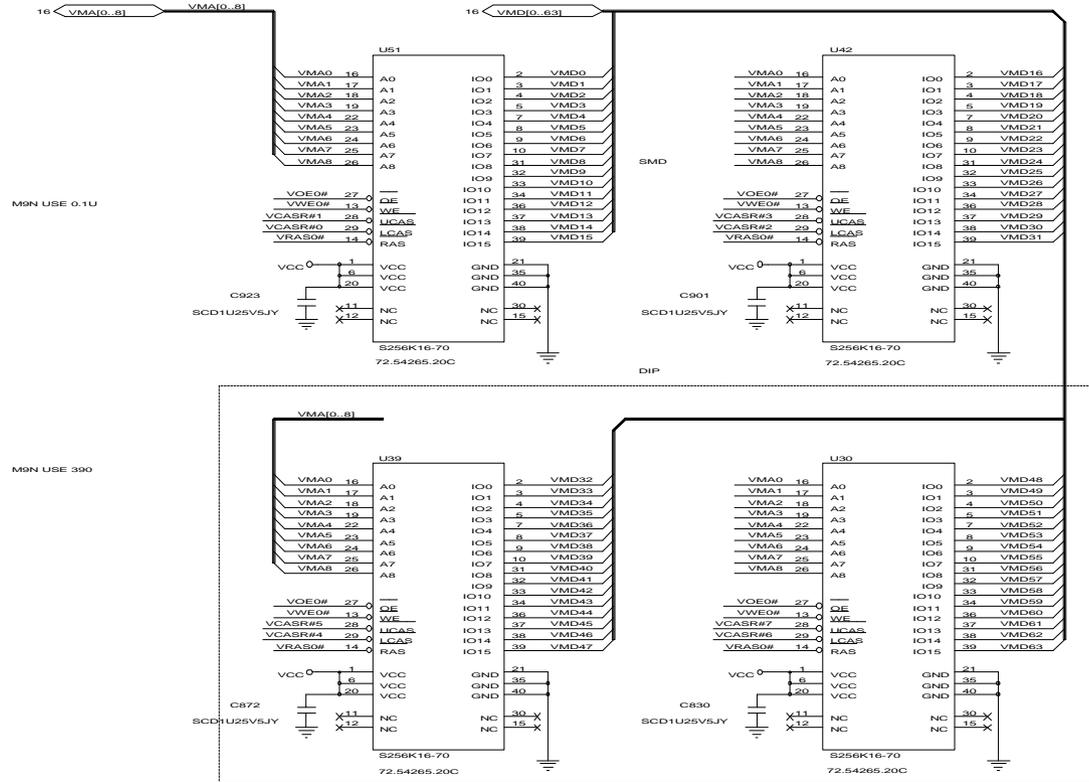


KEYMOUSE

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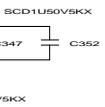
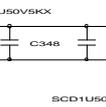
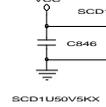
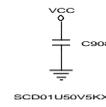
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M4		✓		✓
M5	0.01U	TOR	0.01U	TOR
M6	0.1U	OR	0.1U	OR
M7		✓		✓
M8	✓		✓	
M9				
M10	✓			
M11				
M12	✓			
M13	✓			
M14	✓			
M15	✓			
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M19				
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M21				

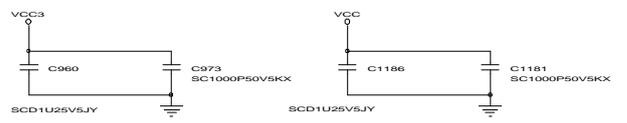
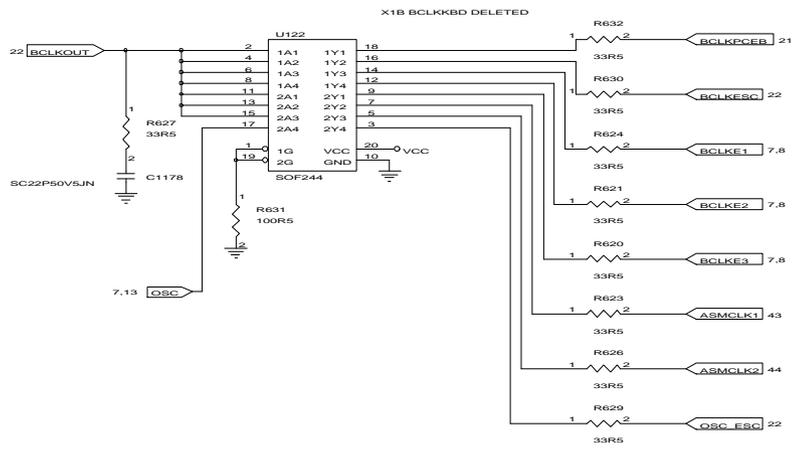
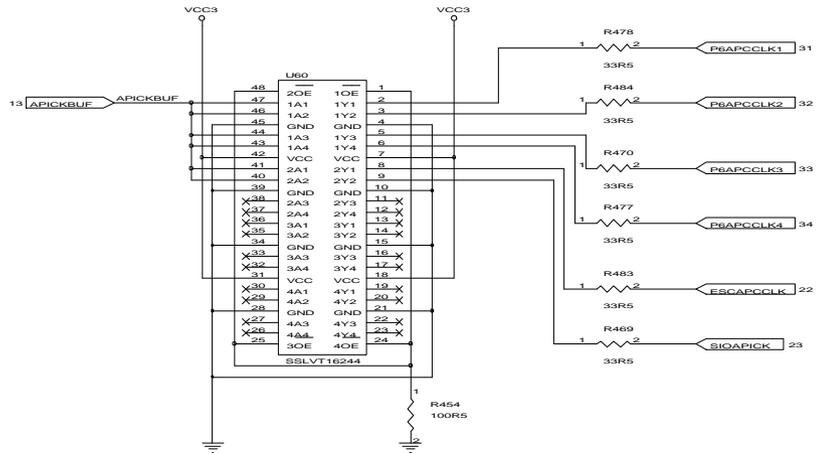


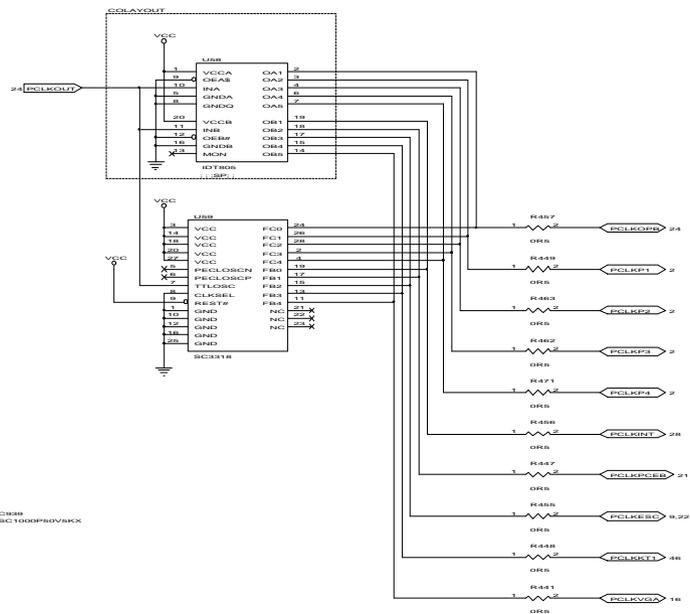
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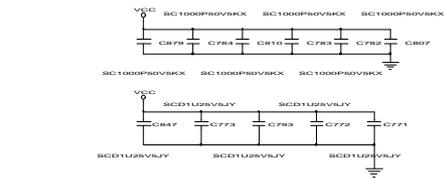
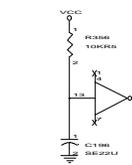
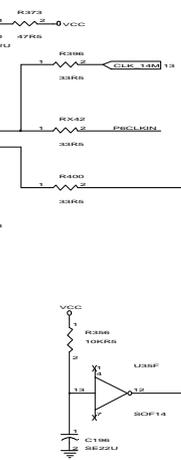
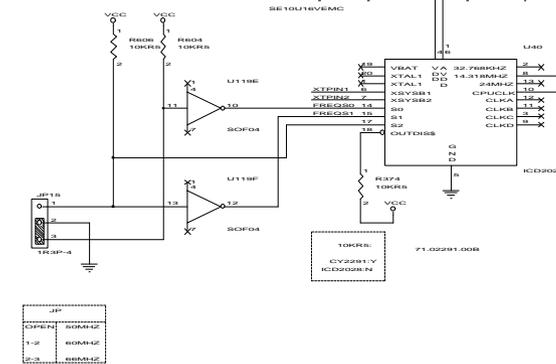
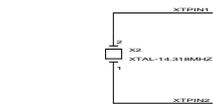
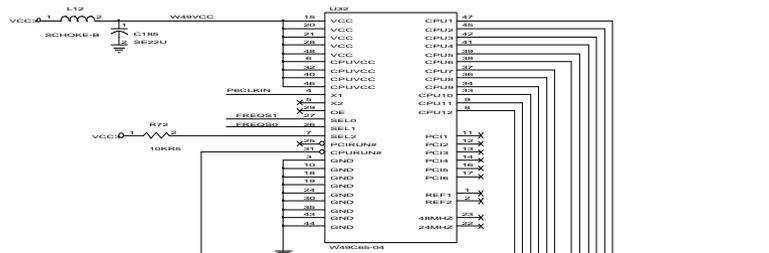
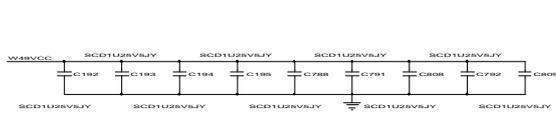
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INCLUDE DIP & SMD

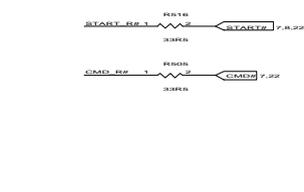
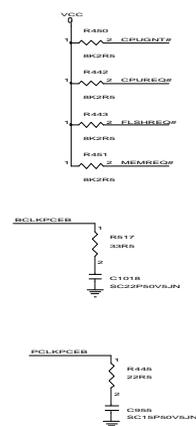
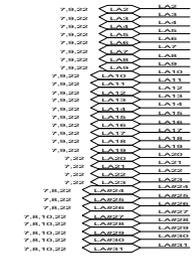
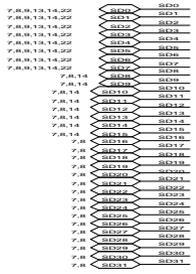
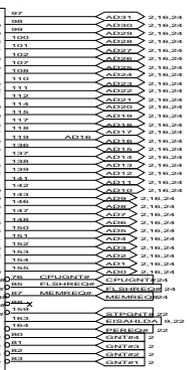
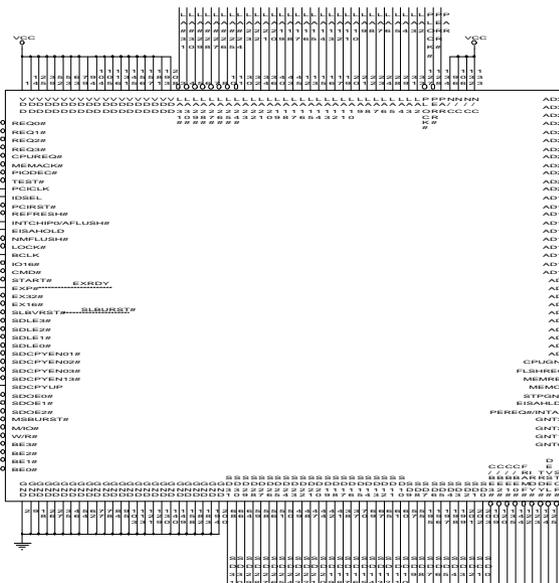
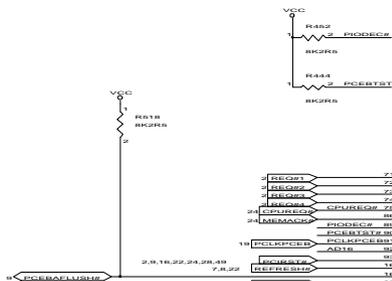


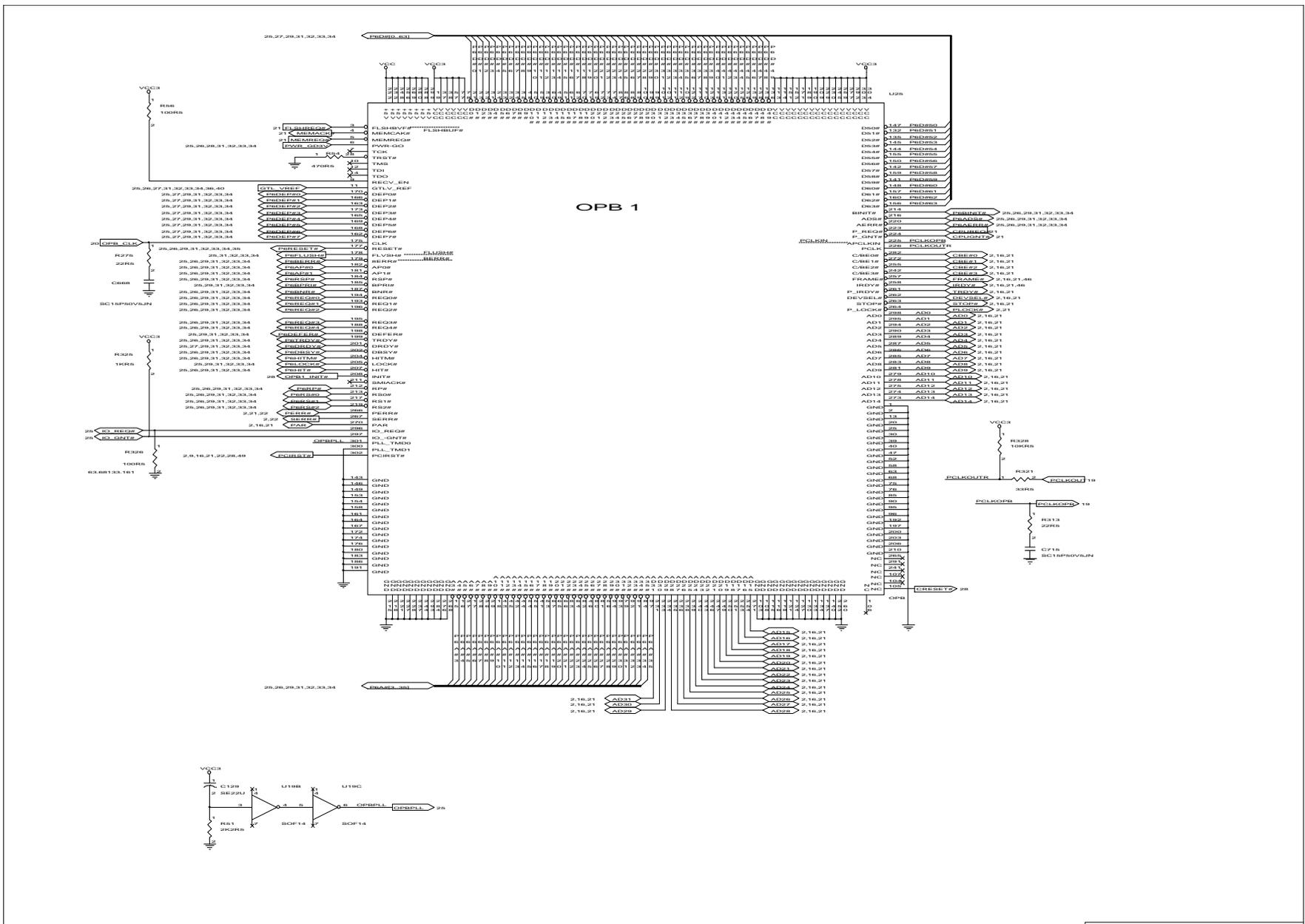
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Size	Document Number	REV	
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Date:	October 16, 1997	Sheet	17 of 63



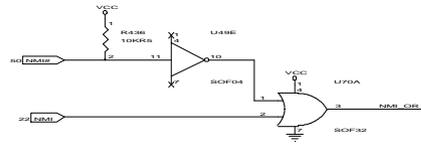




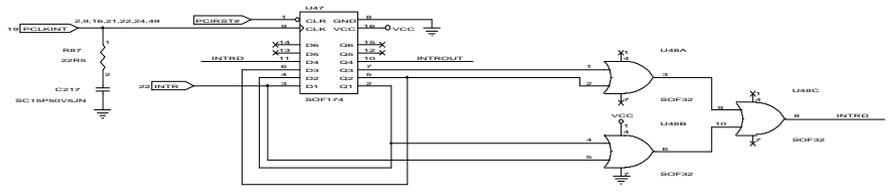
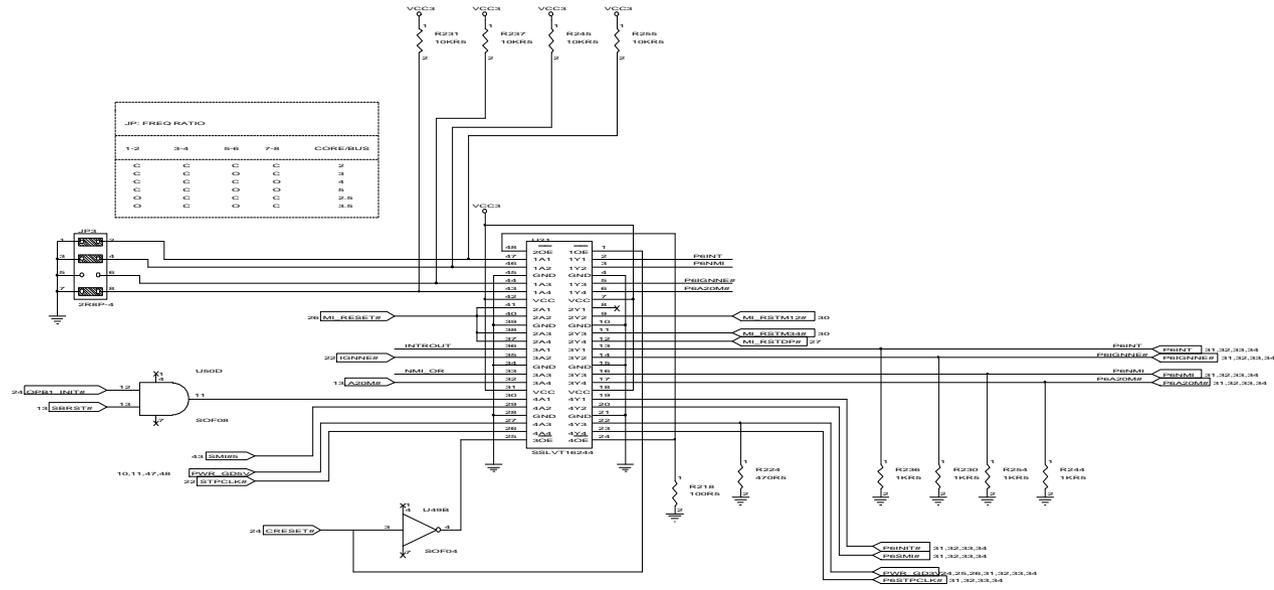


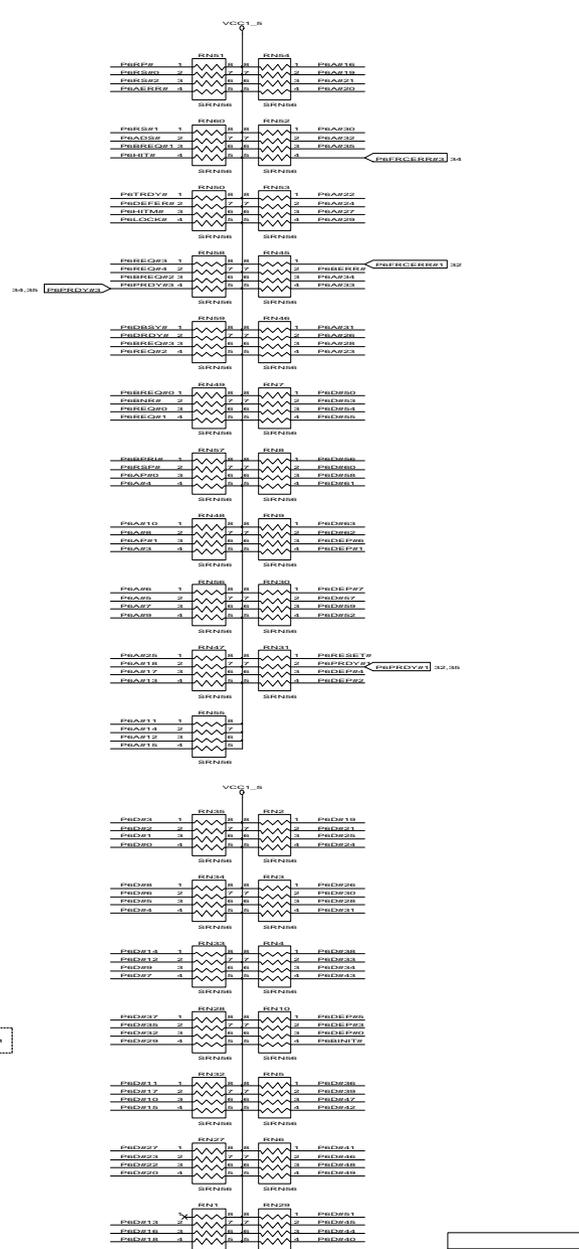
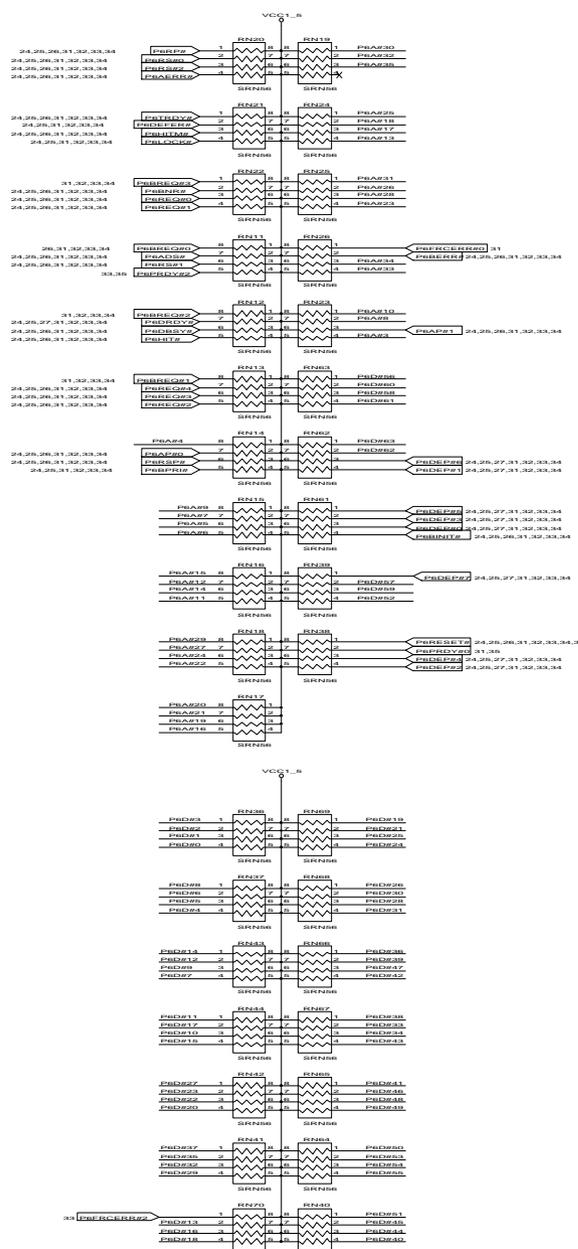


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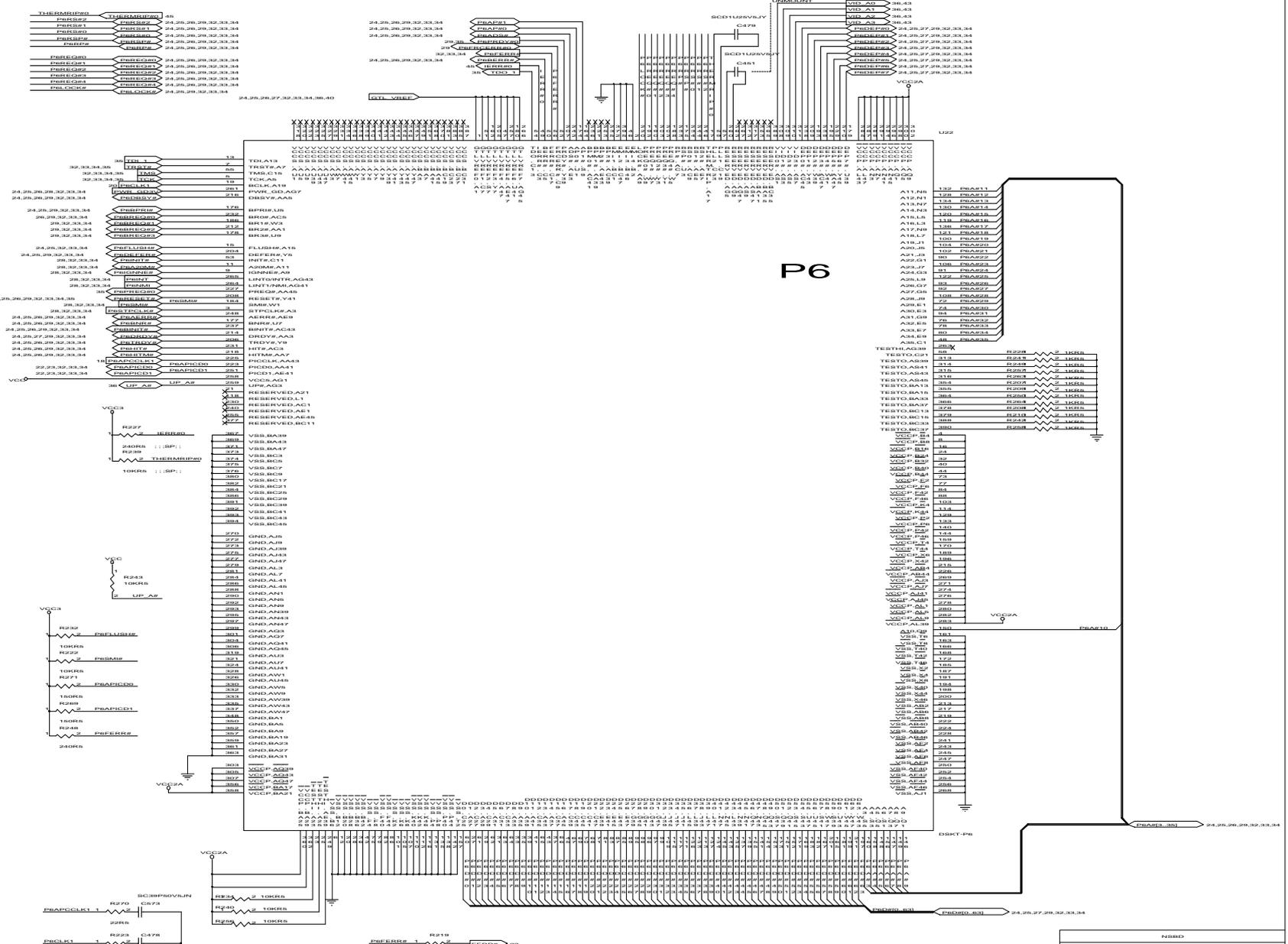


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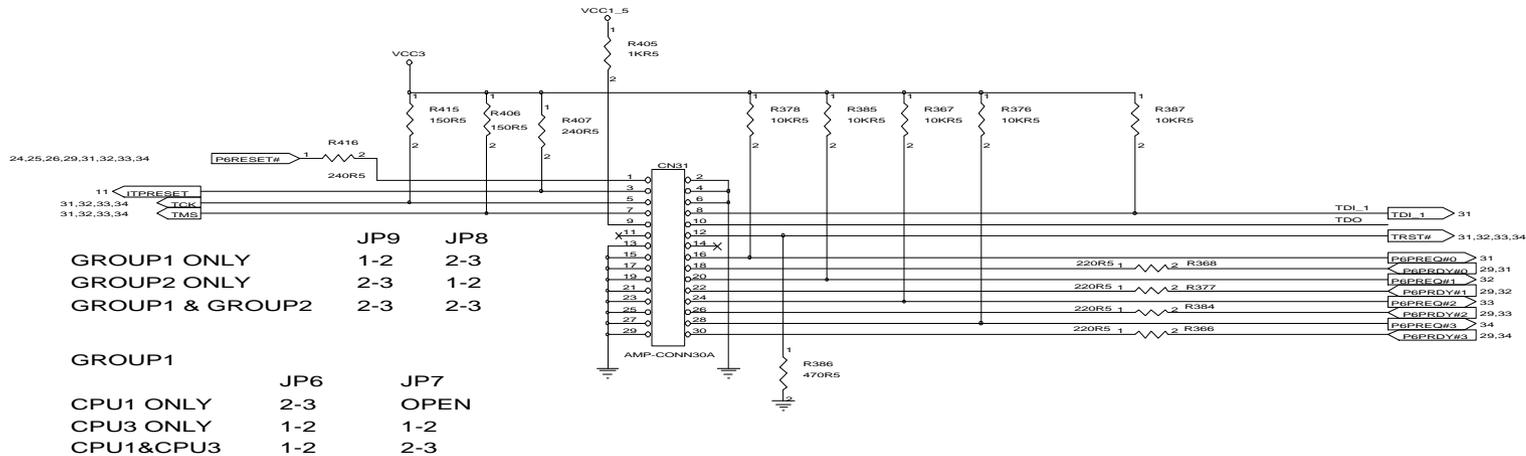




PHI CHINA



P6

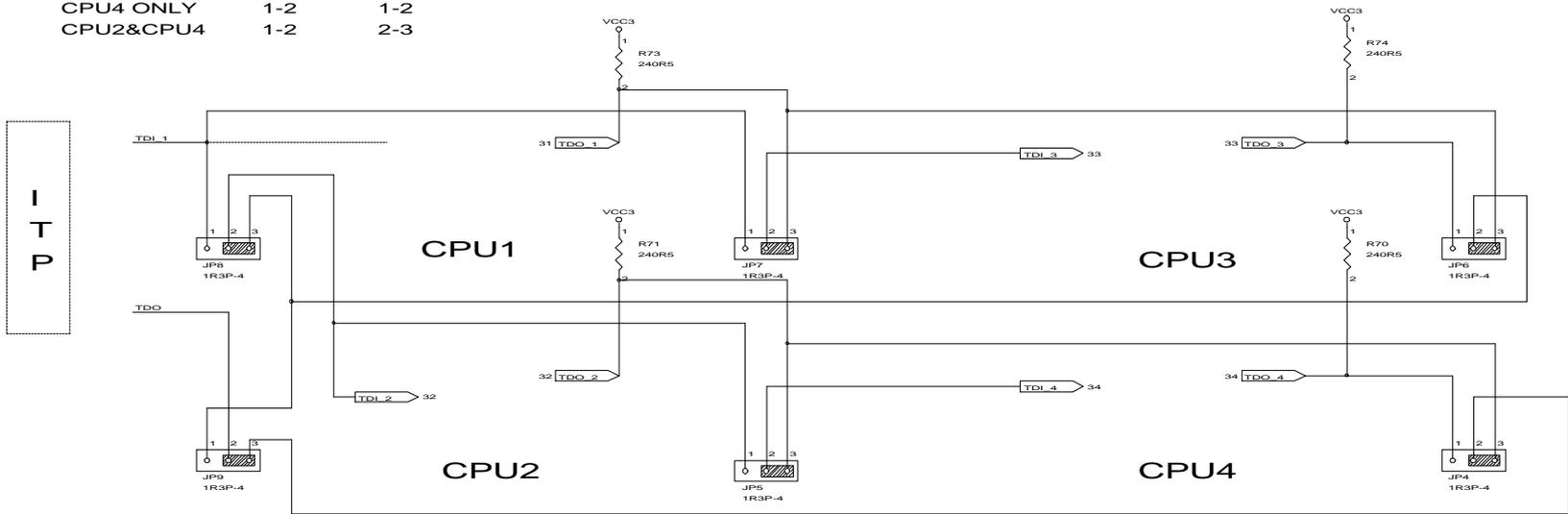


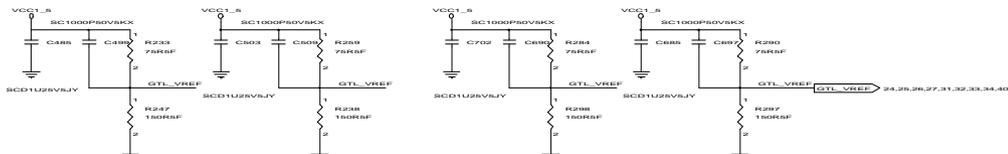
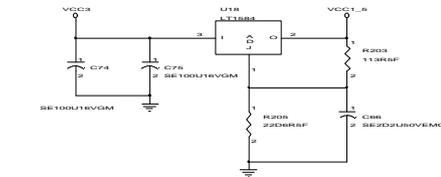
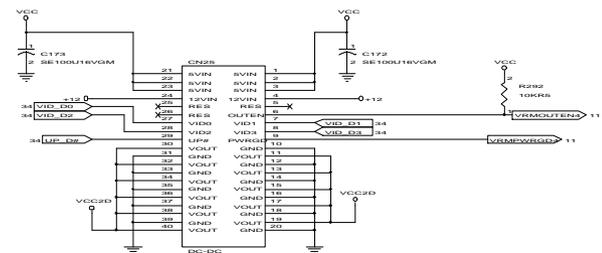
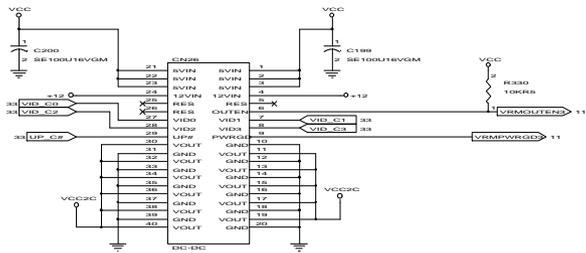
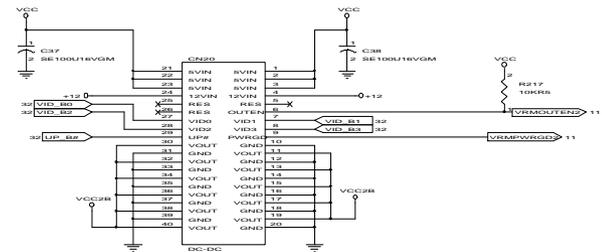
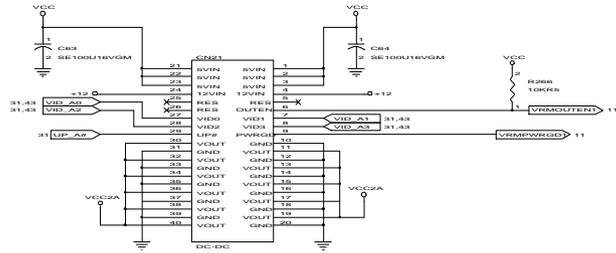
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GROUP2 ONLY	2-3	1-2
GROUP1 & GROUP2	2-3	2-3

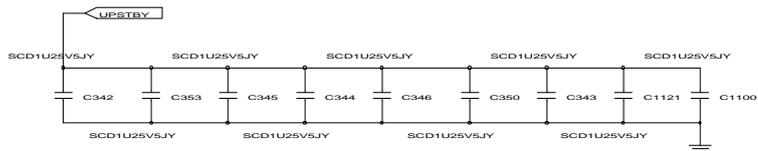
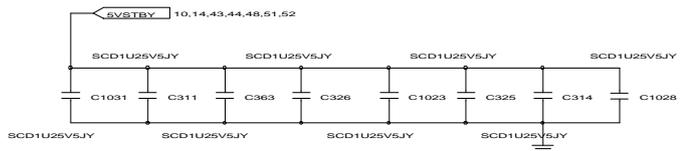
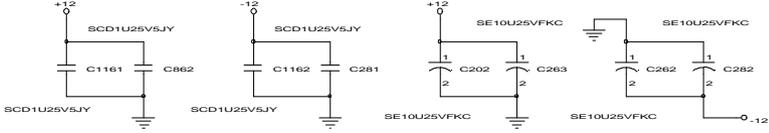
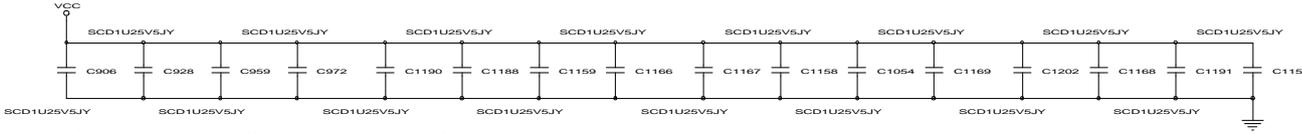
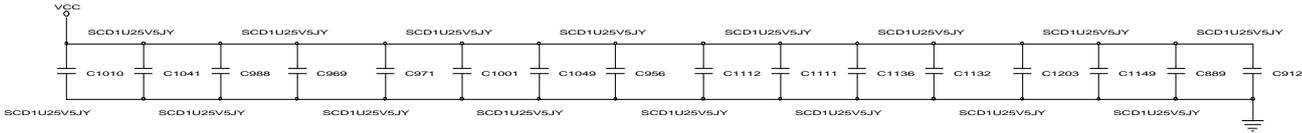
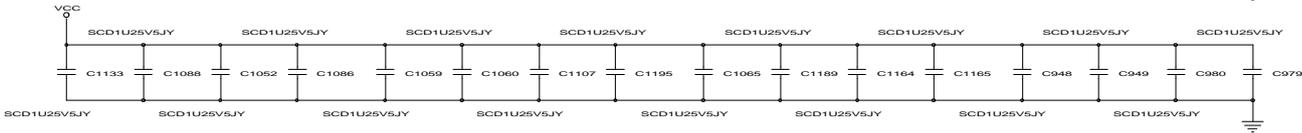
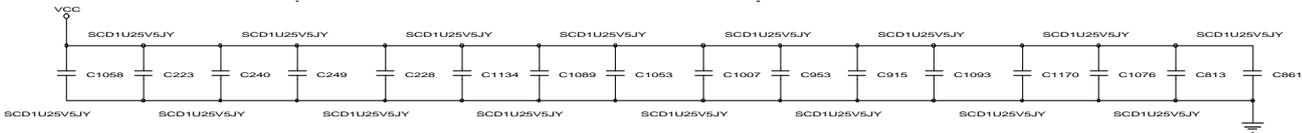
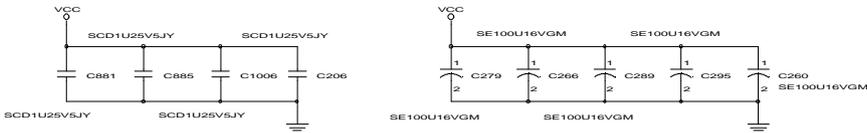
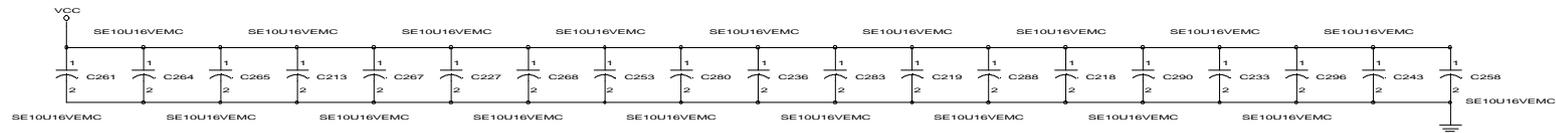
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CPU3 ONLY	1-2	1-2
CPU1&CPU3	1-2	2-3

ITP CONNECTER

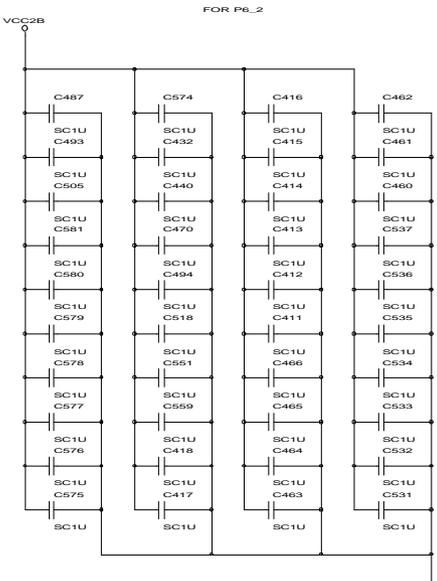
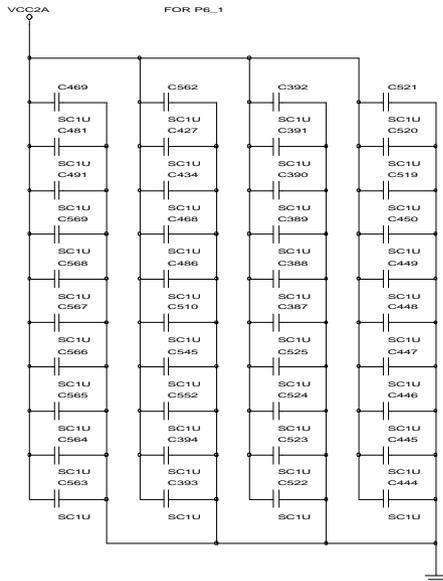
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CPU4 ONLY	1-2	1-2
CPU2&CPU4	1-2	2-3



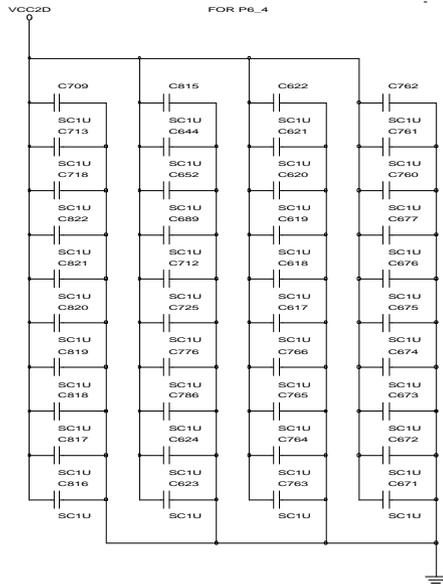
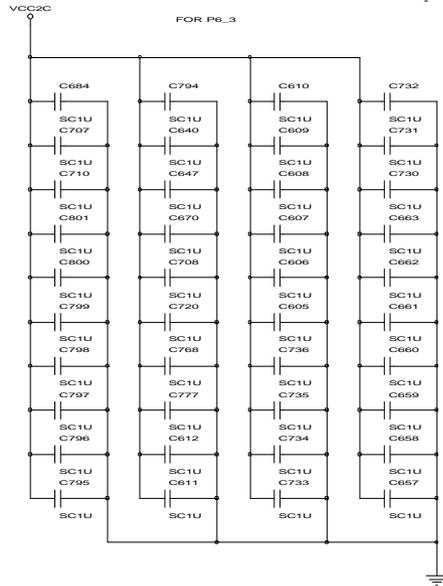




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SLOT DECOUP CAP		
Size	Document Number	REV
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Date:	October 16, 1997	Sheet 37 of 52

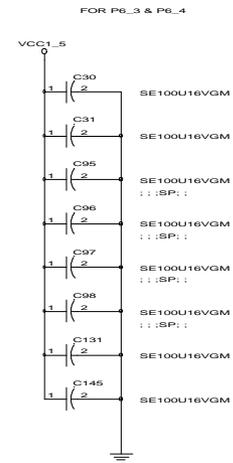
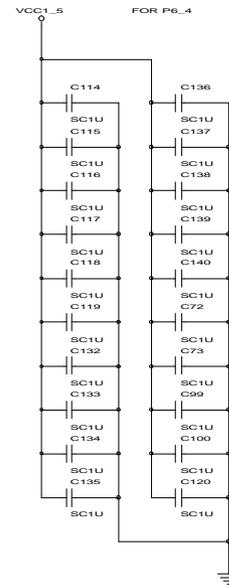
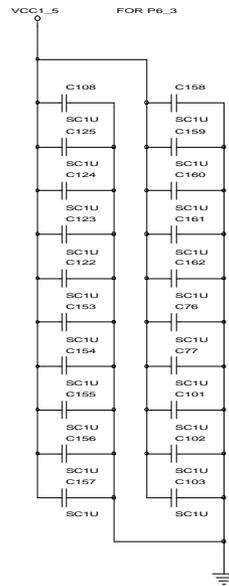
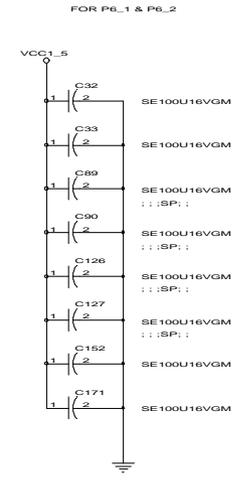
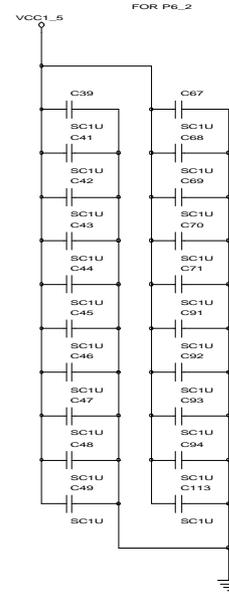
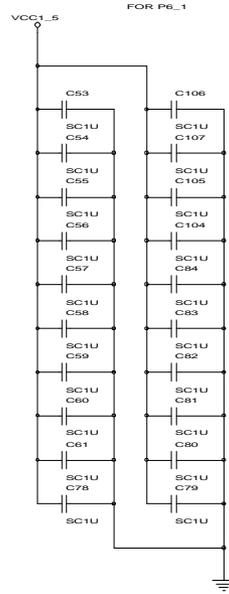
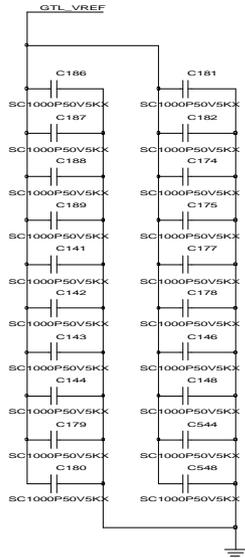
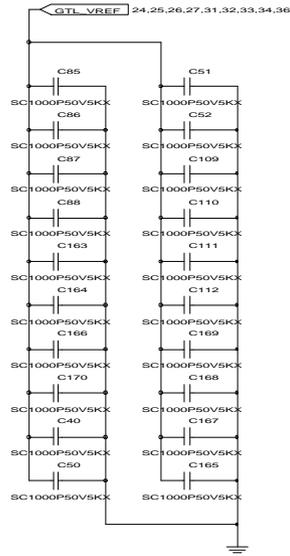


USE 1U, LOW ESR, SIZE 1206

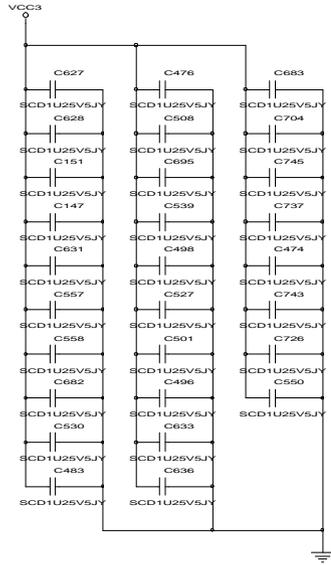


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Date	October 16, 1993	Sheet	30 of 33

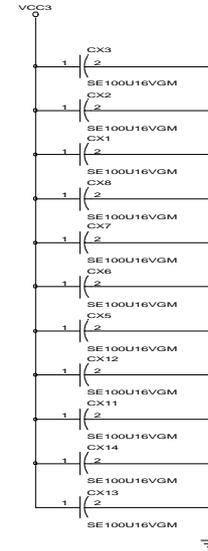
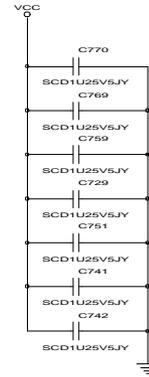
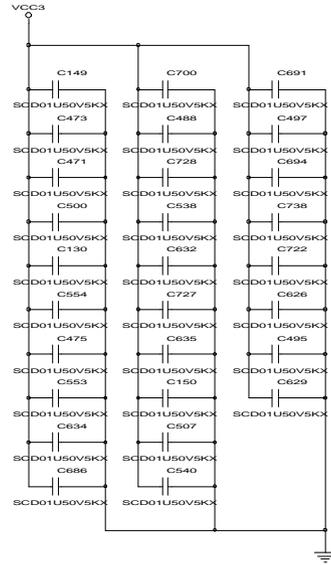
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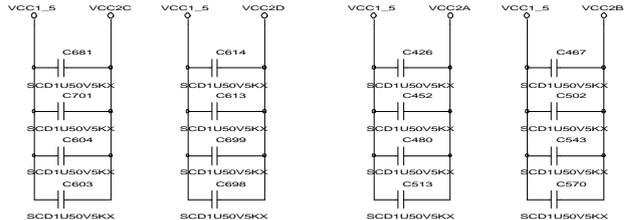
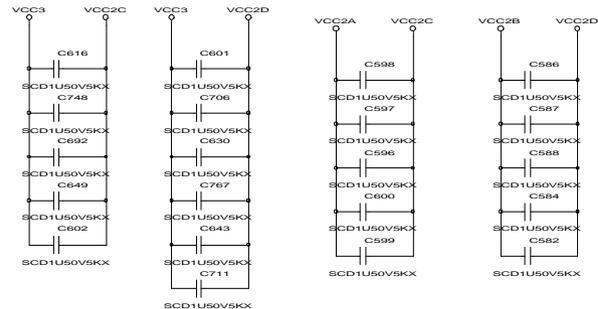
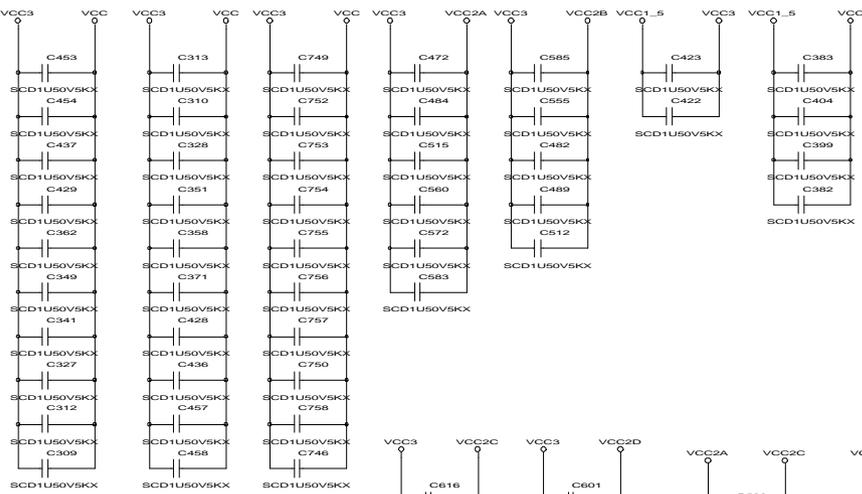
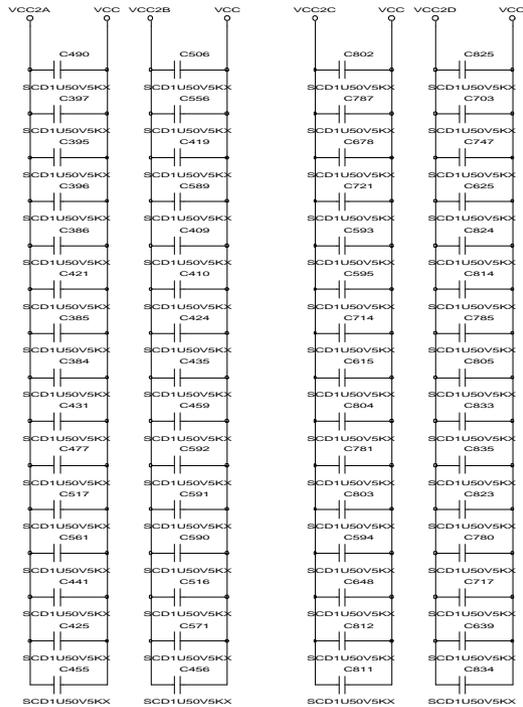
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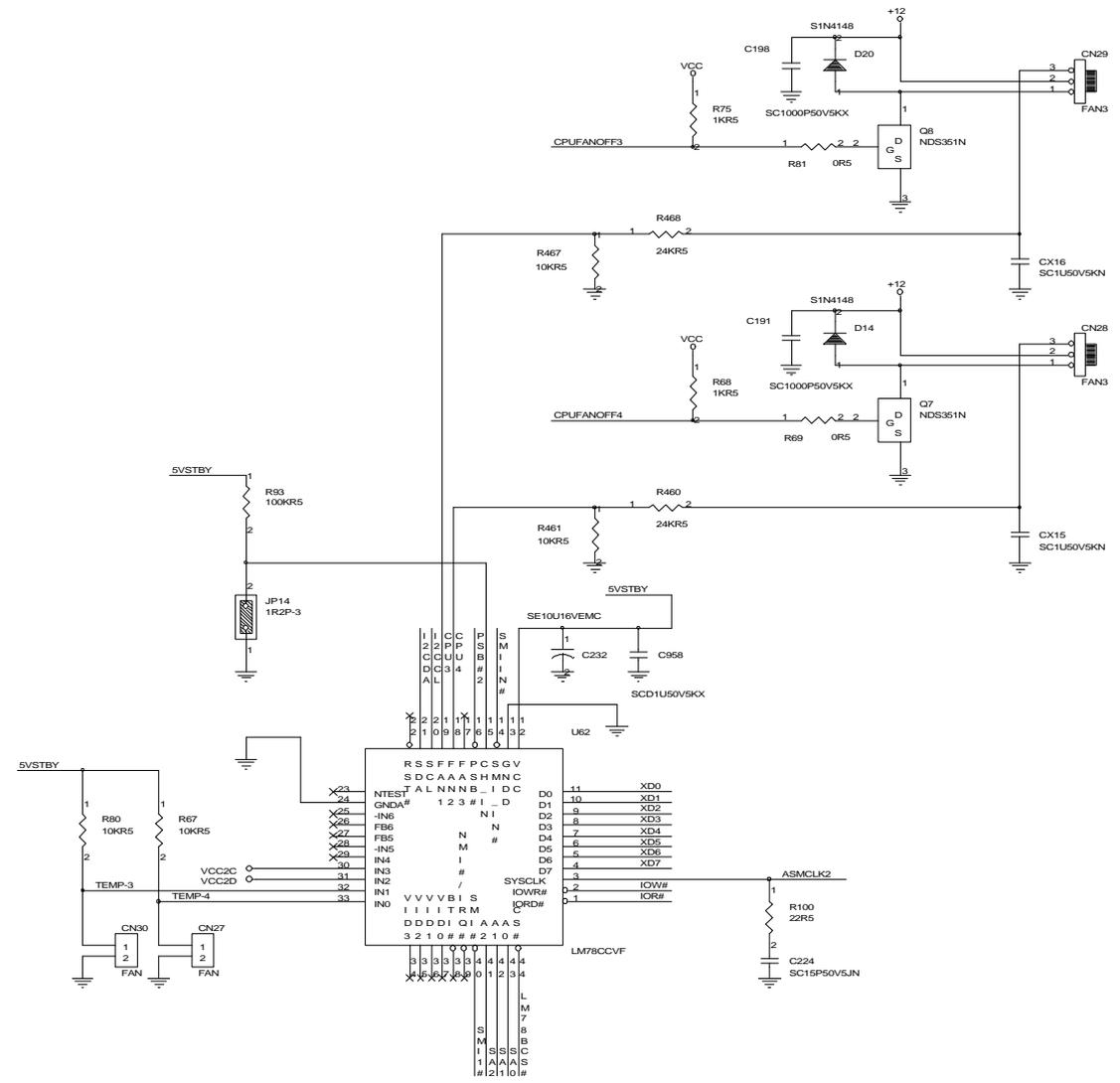
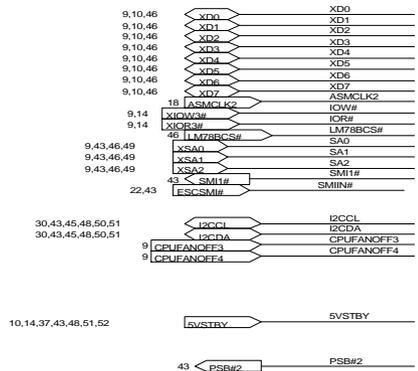


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 16 CAPS (0.1U*8, 0.01U*8) PER OMC

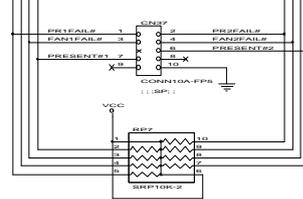
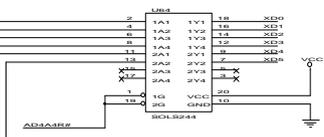
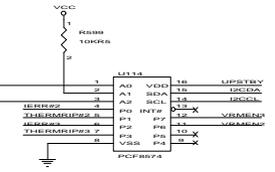
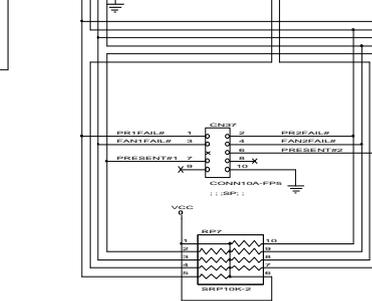
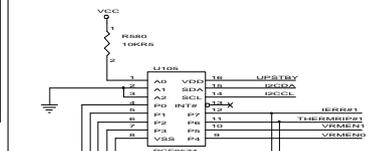
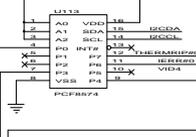
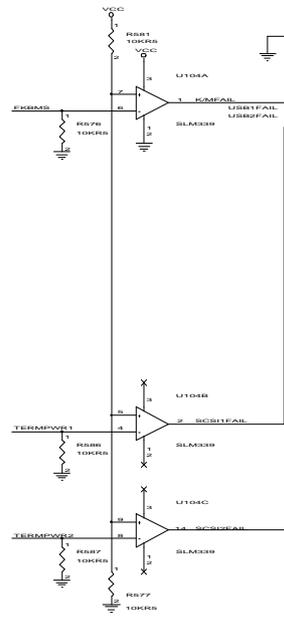
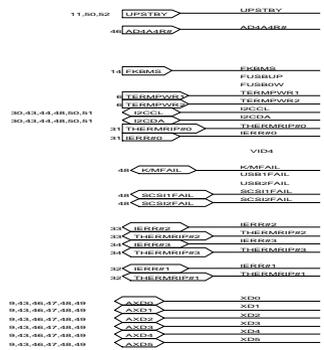


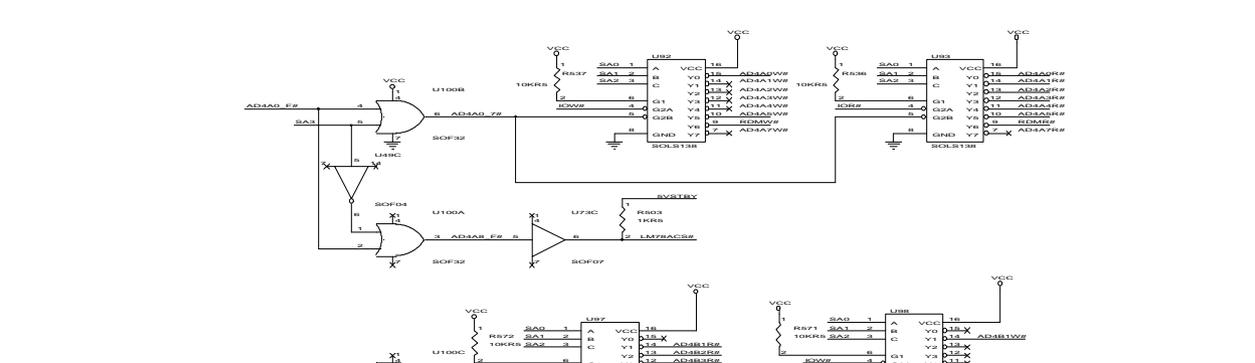
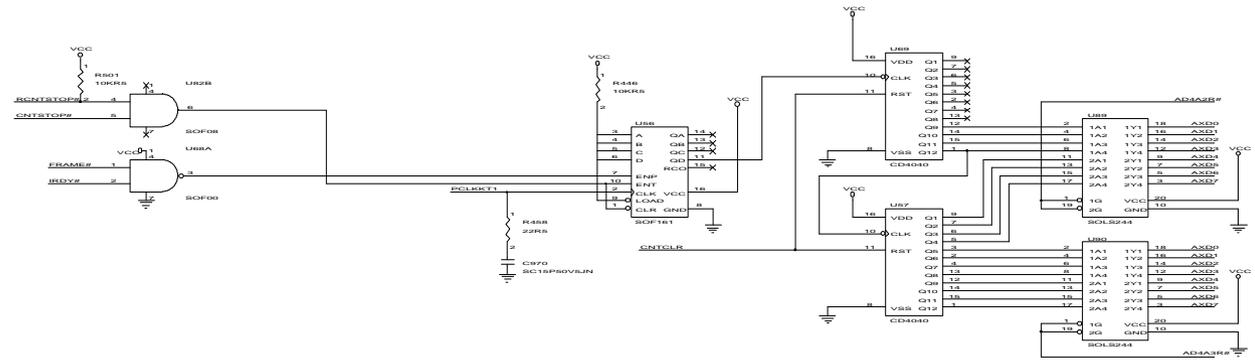
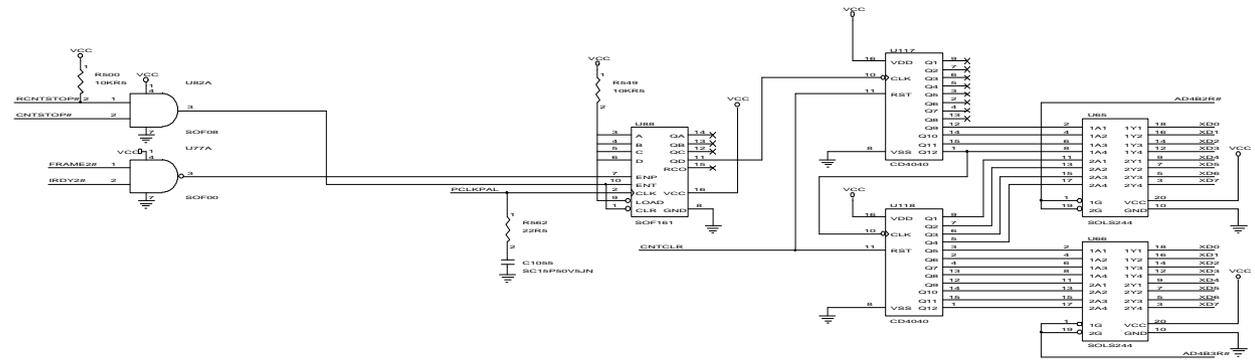
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Date	October 16, 1997	Sheet	41 of 83





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Date:	October 16, 1997	Sheet 44 of 52

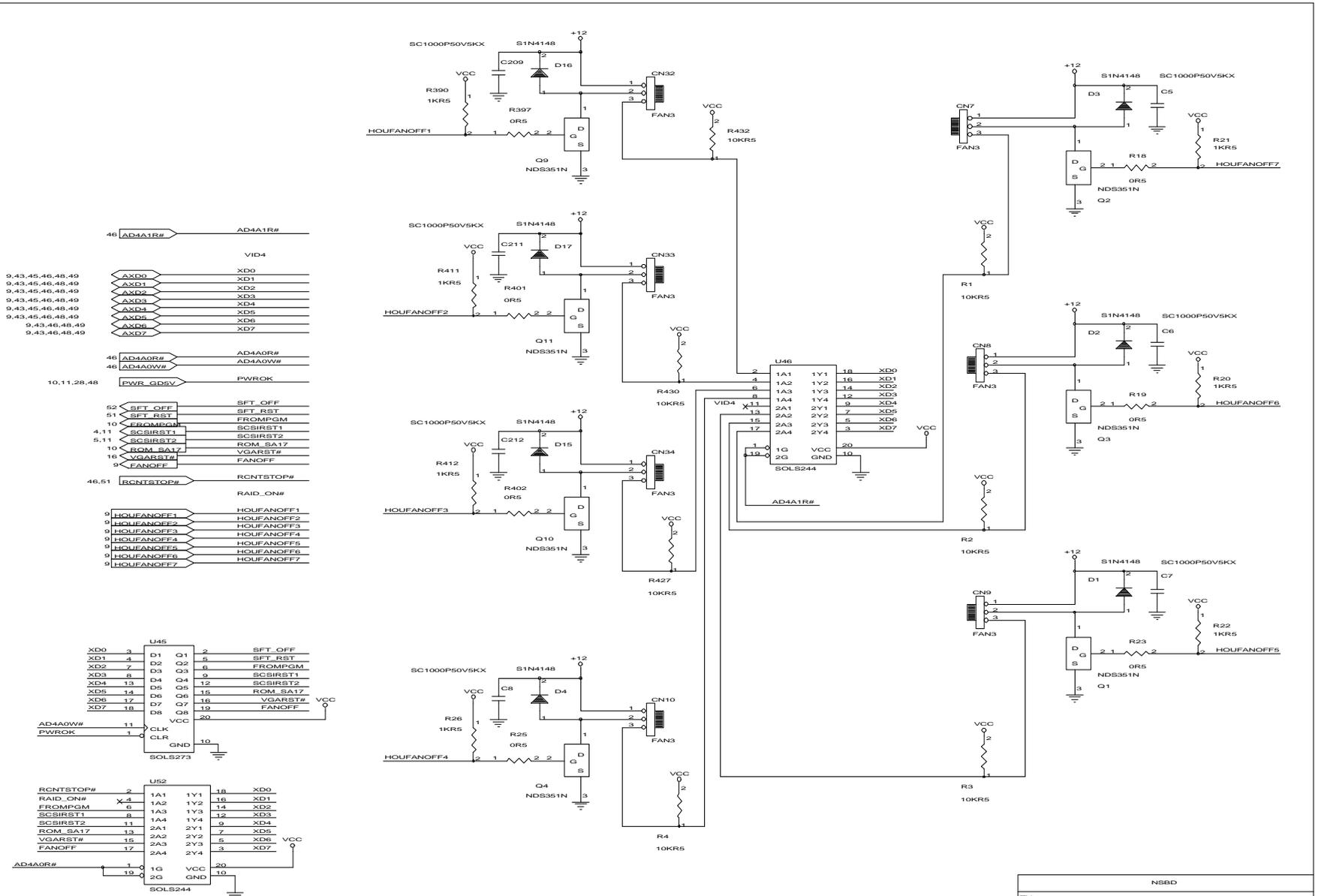




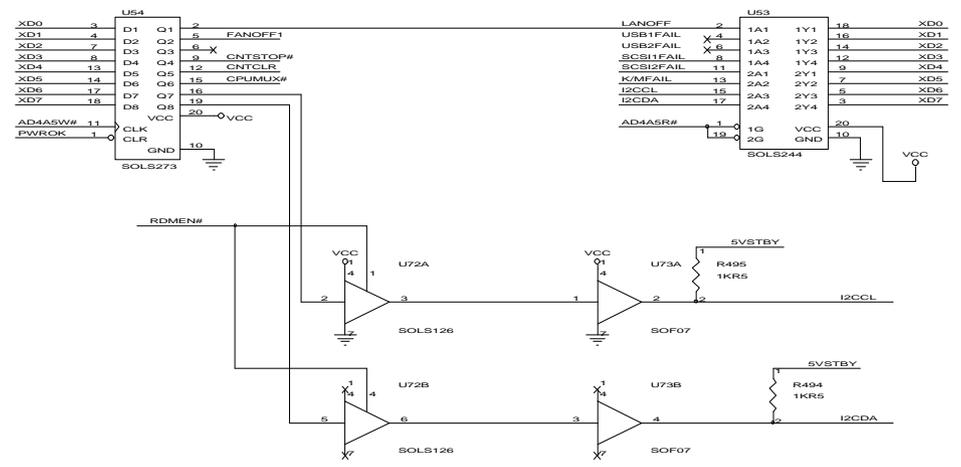
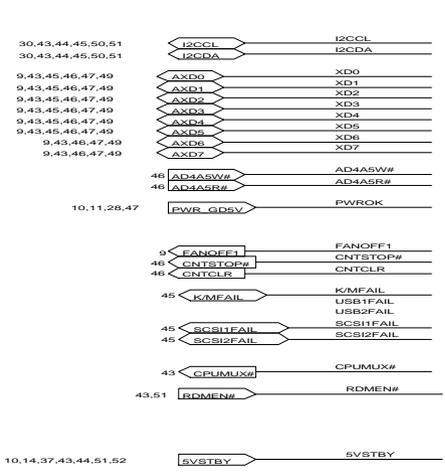
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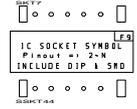
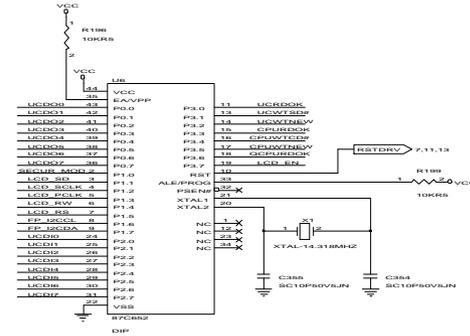
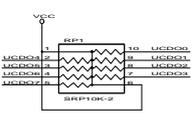
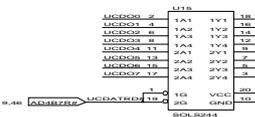
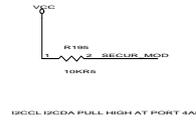
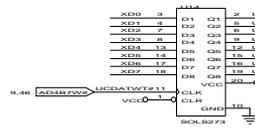
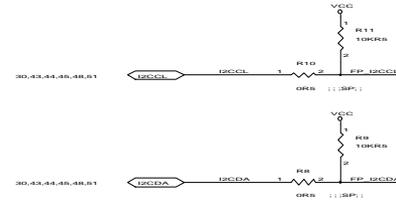
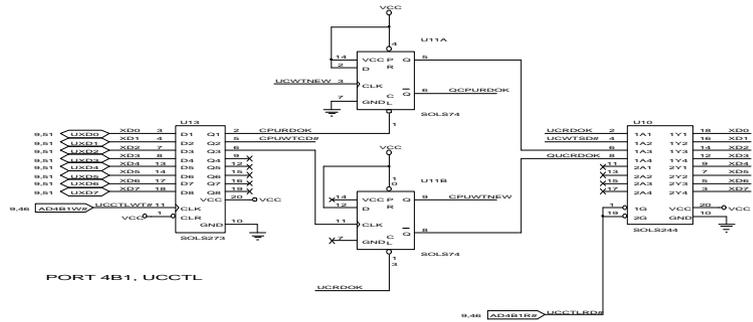


PORT 4A5

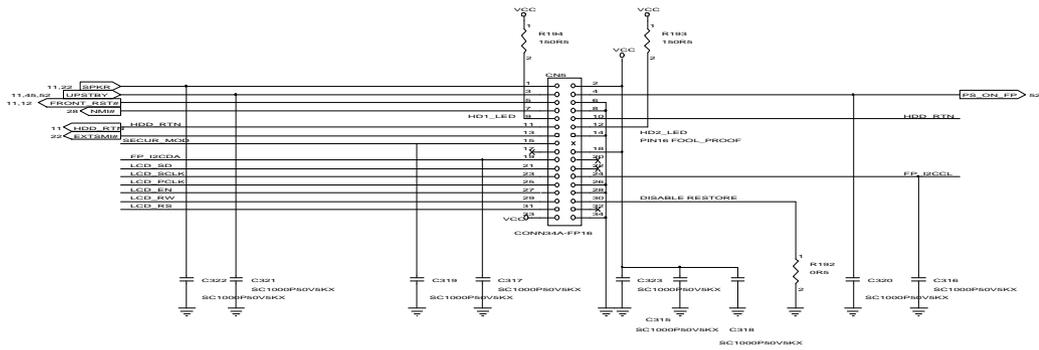


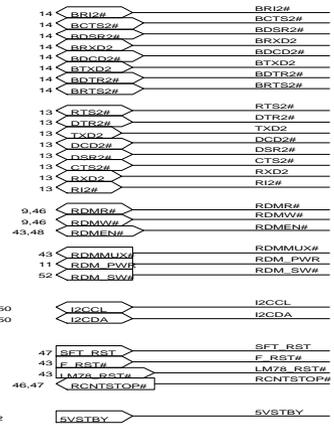
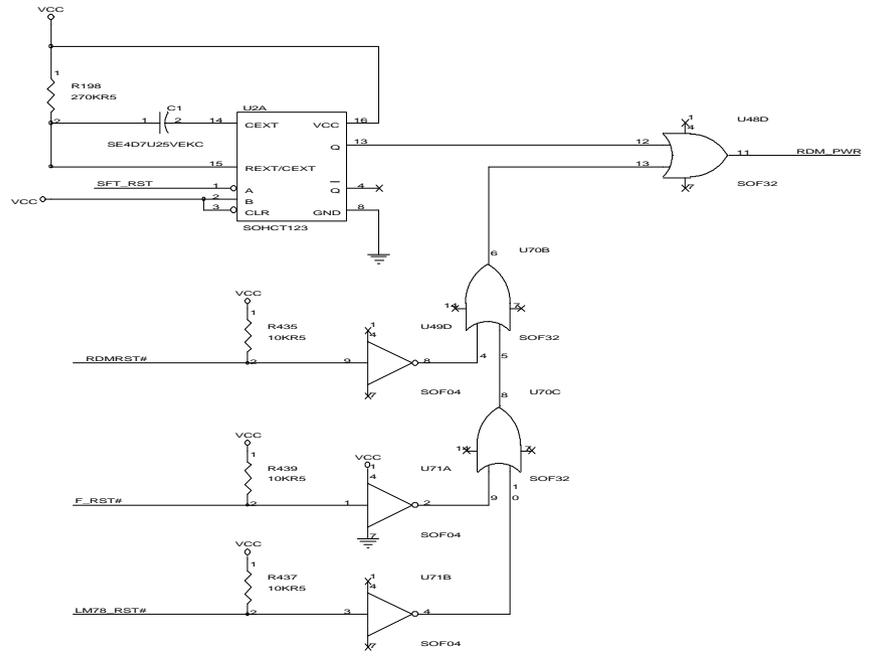
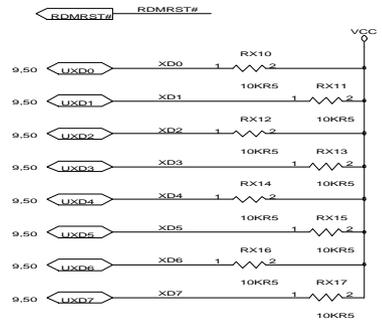
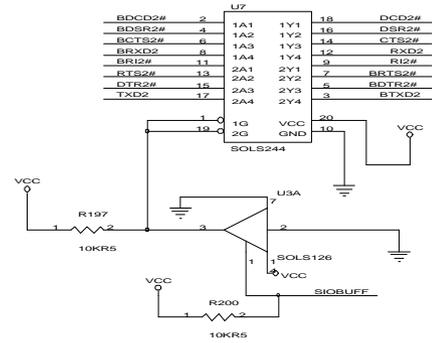
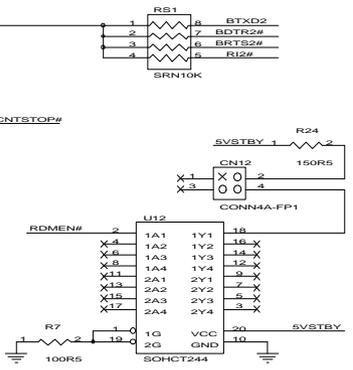
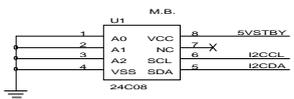
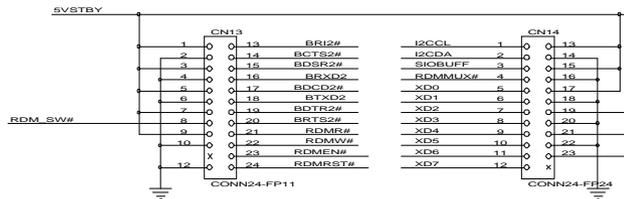
PORT 4A7 FOR BACKPLANE BOARD
 IDX NOT USE

NSBD		
Title PORT 4A5, 4A7		
Size	Document Number	REV
B	ASM14-4.SCH	1
Date:	October 16, 1997	Sheet 48 of 52



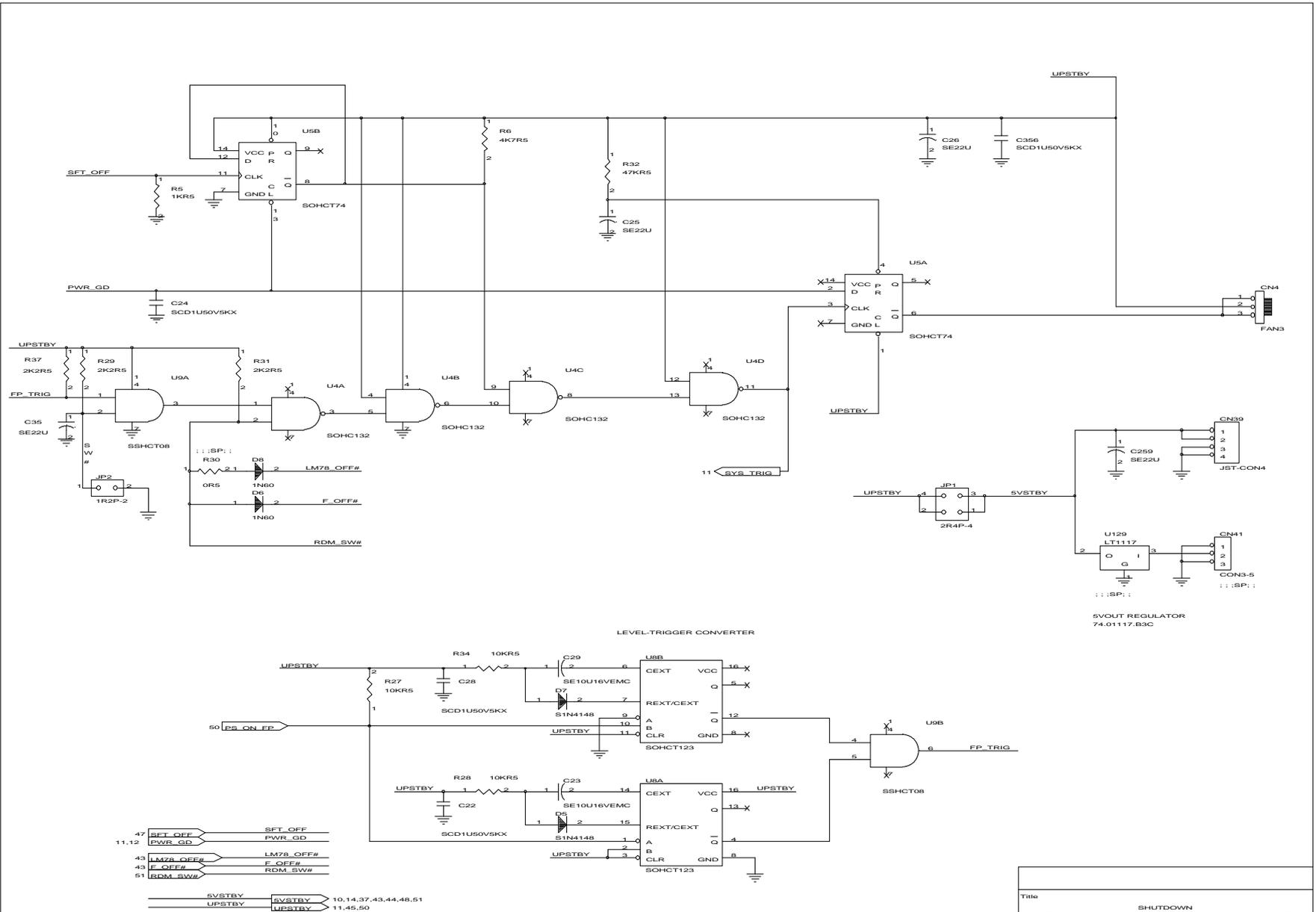
PORT 4B7, UCDA



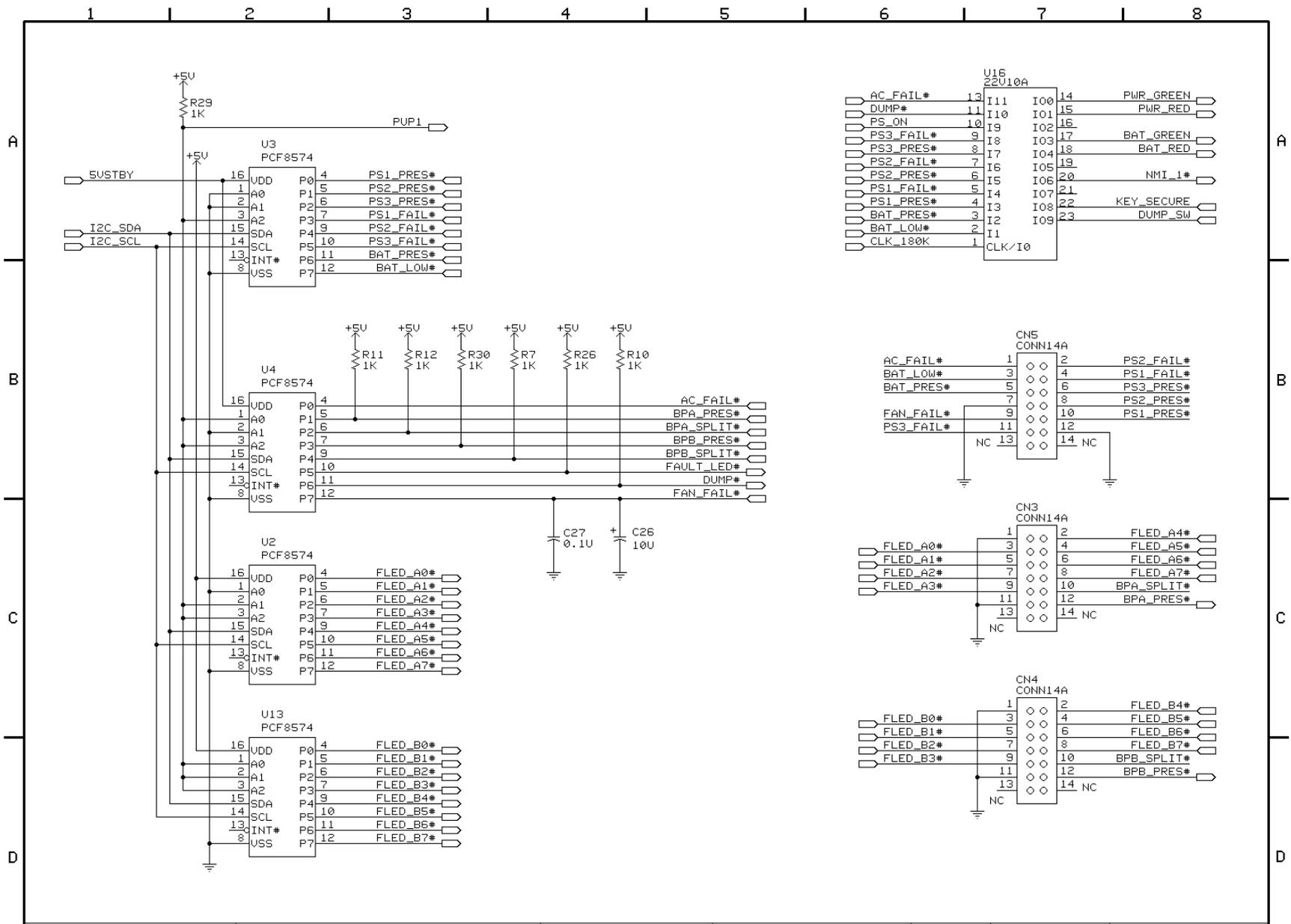


Title		
RDM		
Size	Document Number	REV
B	RDM-1.SCH	1
Date:	October 16, 1997	Sheet 51 of 52

10,14,37,43,44,48,52



Title			SHUTDOWN
Size	Document Number	REV	
B	RDM-2.SCH	1	
Date:	October 16, 1997	Sheet	52 of 52



U16
22V10A

AC_FAIL#	13	I11	I00	14	PWR_GREEN
DUMP#	11	I10	I01	15	PWR_RED
PS_ON	10	I9	I02	16	
PS3_FAIL#	9	I8	I03	17	BAT_GREEN
PS3_PRESENT#	8	I7	I04	18	BAT_RED
PS2_FAIL#	7	I6	I05	19	
PS2_PRESENT#	6	I5	I06	20	NMI_1#
PS1_FAIL#	5	I4	I07	21	
PS1_PRESENT#	4	I3	I08	22	KEY_SECURE
BAT_PRESENT#	3	I2	I09	23	DUMP_SW
BAT_LOW#	2	I1			
CLK_180K	1	CLK/I/O			

CN5
CONN14A

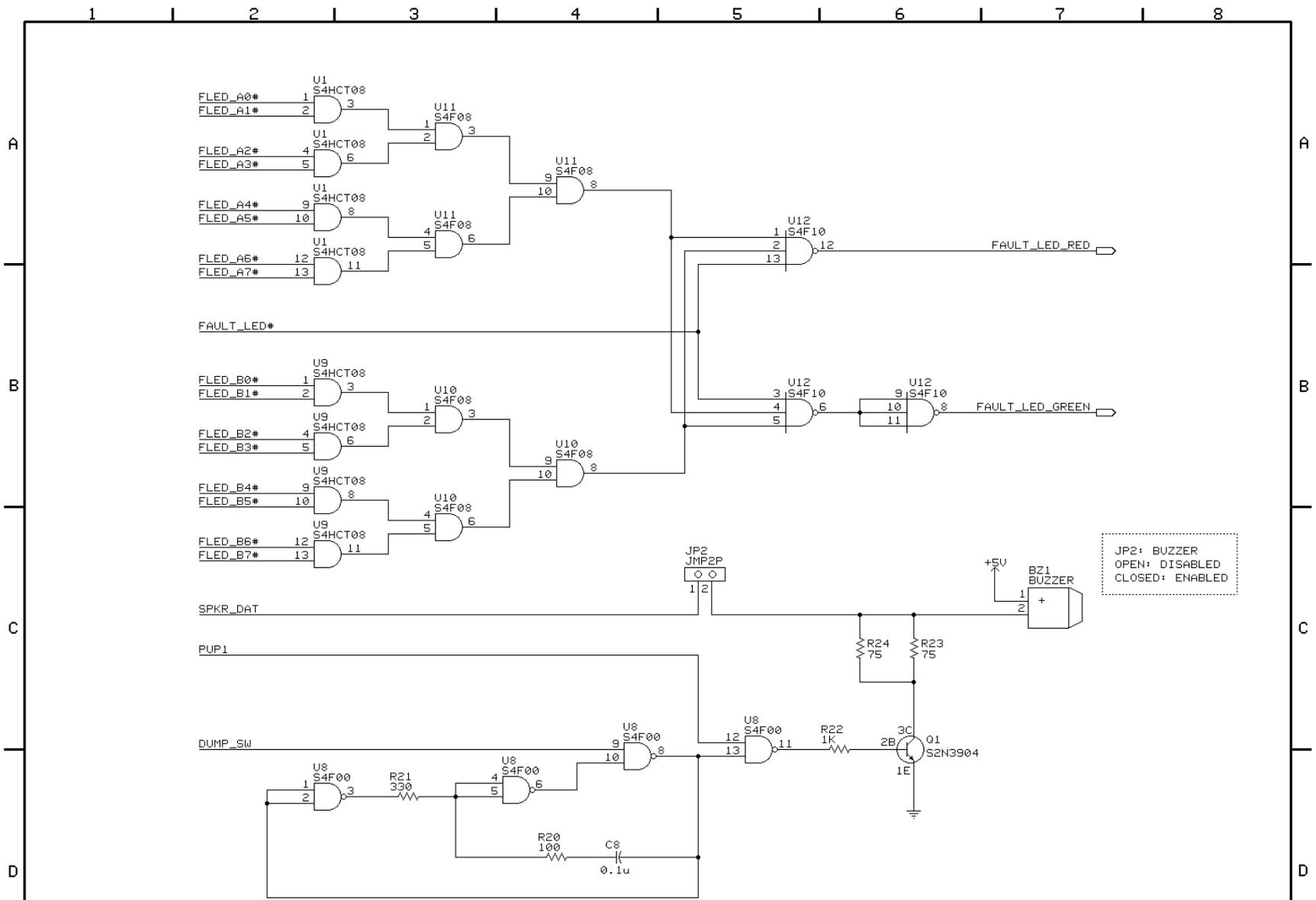
AC_FAIL#	1	2	PS2_FAIL#
BAT_LOW#	3	4	PS1_FAIL#
BAT_PRESENT#	5	6	PS3_PRESENT#
	7	8	PS2_PRESENT#
FAN_FAIL#	9	10	PS1_PRESENT#
PS3_FAIL#	11	12	
	NC 13	14	NC

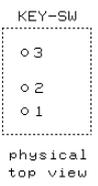
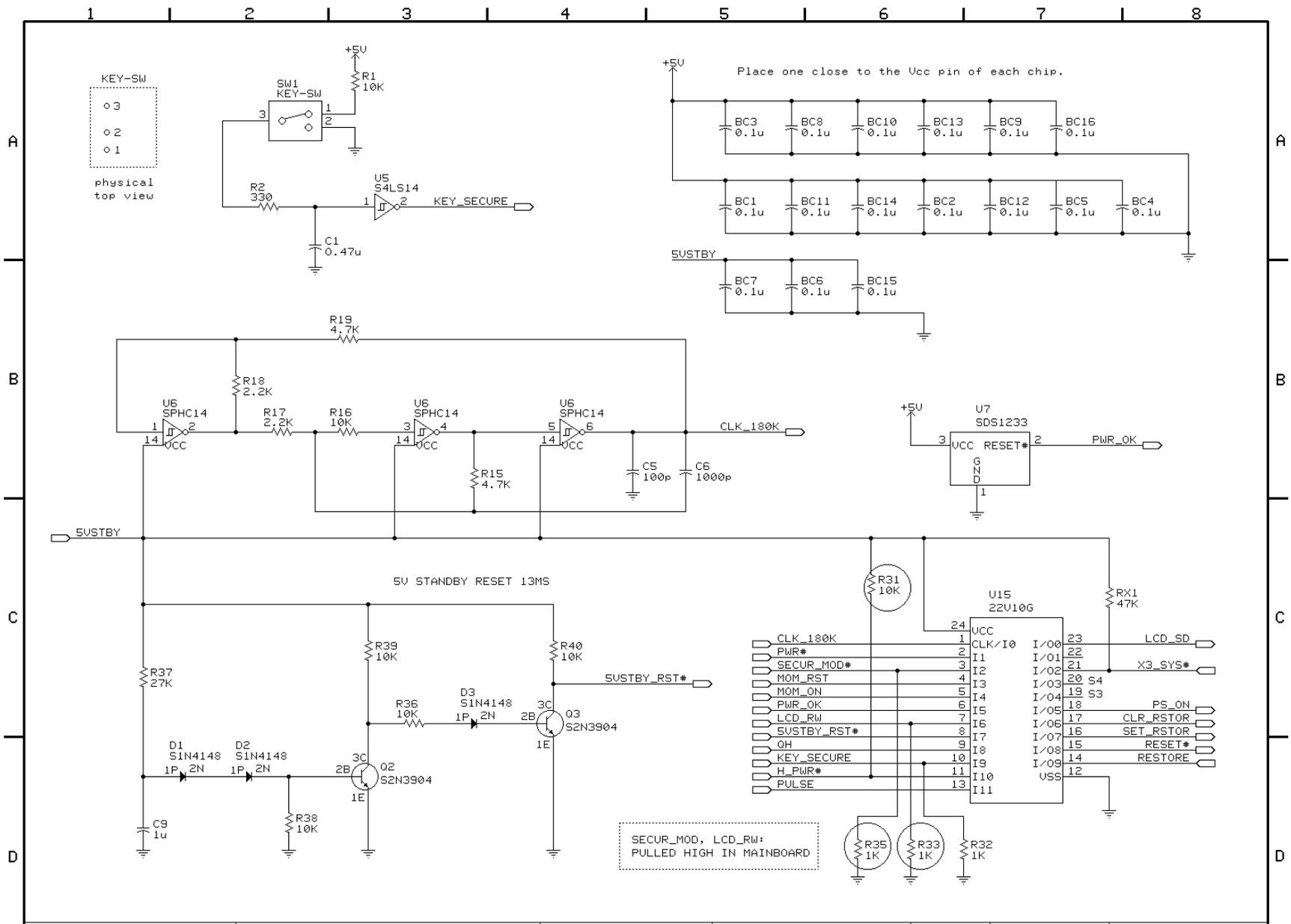
CN3
CONN14A

FLED_A0#	1	2	FLED_A4#
FLED_A1#	3	4	FLED_A5#
FLED_A2#	5	6	FLED_A6#
FLED_A3#	7	8	FLED_A7#
	9	10	BPA_SPLIT#
	11	12	BPA_PRESENT#
	NC 13	14	NC

CN4
CONN14A

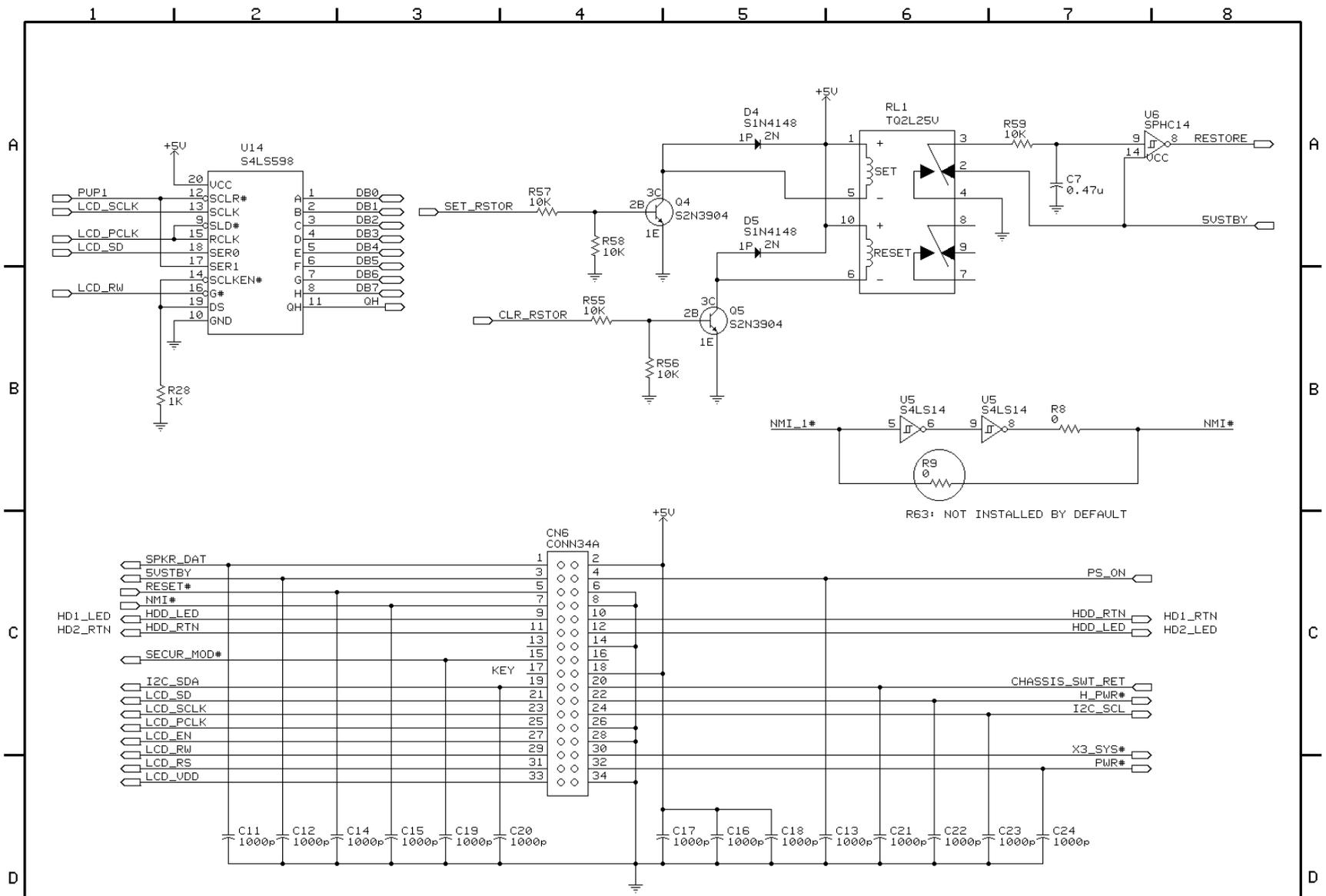
FLED_B0#	1	2	FLED_B4#
FLED_B1#	3	4	FLED_B5#
FLED_B2#	5	6	FLED_B6#
FLED_B3#	7	8	FLED_B7#
	9	10	BPB_SPLIT#
	11	12	BPB_PRESENT#
	NC 13	14	NC

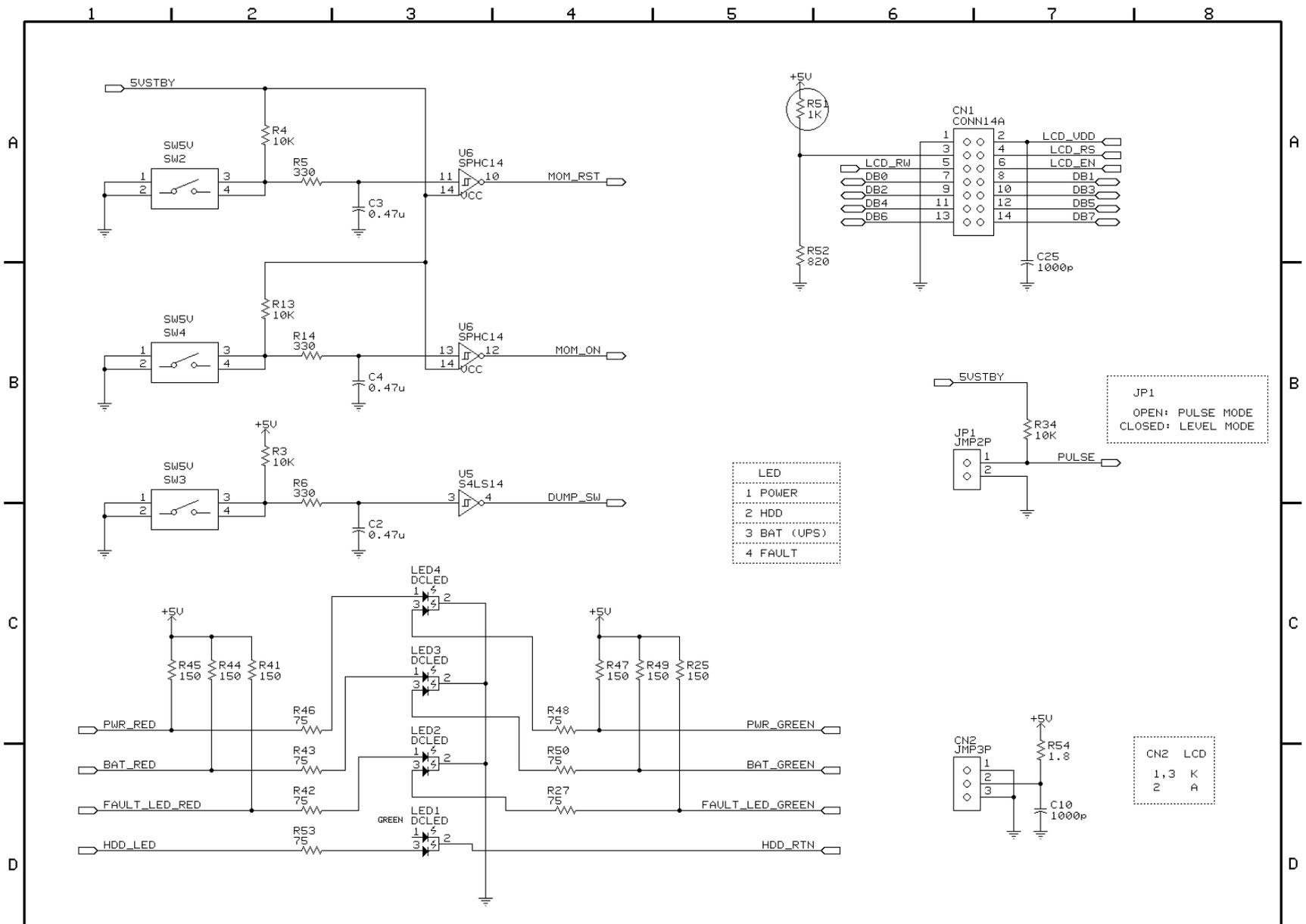




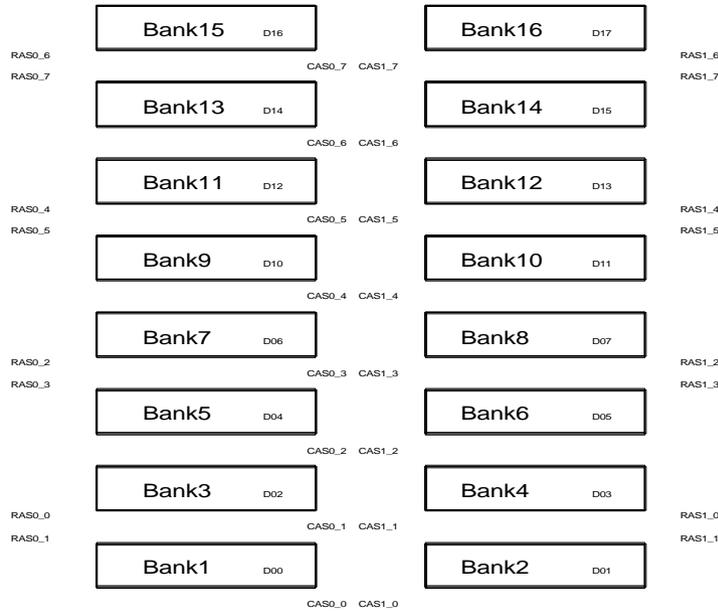
Place one close to the Ucc pin of each chip.

SECUR_MOD, LCD_RW:
PULLED HIGH IN MAINBOARD





LINK
 I/MEMBUS.SCH P.02
 I/MIC1.SCH P.03
 I/MIC2.SCH P.04
 I/RASBUF.SCH P.05
 I/CASBUF.SCH P.06
 I/WE.SCH P.07
 I/MABUF1.SCH P.08
 I/MABUF2.SCH P.09
 I/BANK0102.SCH P.10
 I/BANK0304.SCH P.11
 I/BANK0506.SCH P.12
 I/BANK0708.SCH P.13
 I/BANK0910.SCH P.14
 I/BANK1112.SCH P.15
 I/BANK1314.SCH P.16
 I/BANK1516.SCH P.17
 I/DIMMDEC1.SCH P.18
 I/DIMMDEC2.SCH P.19
 I/MICDEC.SCH P.20

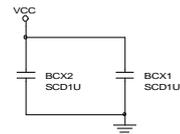


TRACE LENGTH (MIL)

MICCLK1 3811 MD_RDY0# 3365
 MICCLK2 3801 MD_RDY1# 4281
 MICCLK3 3801
 MICCLK4 3811

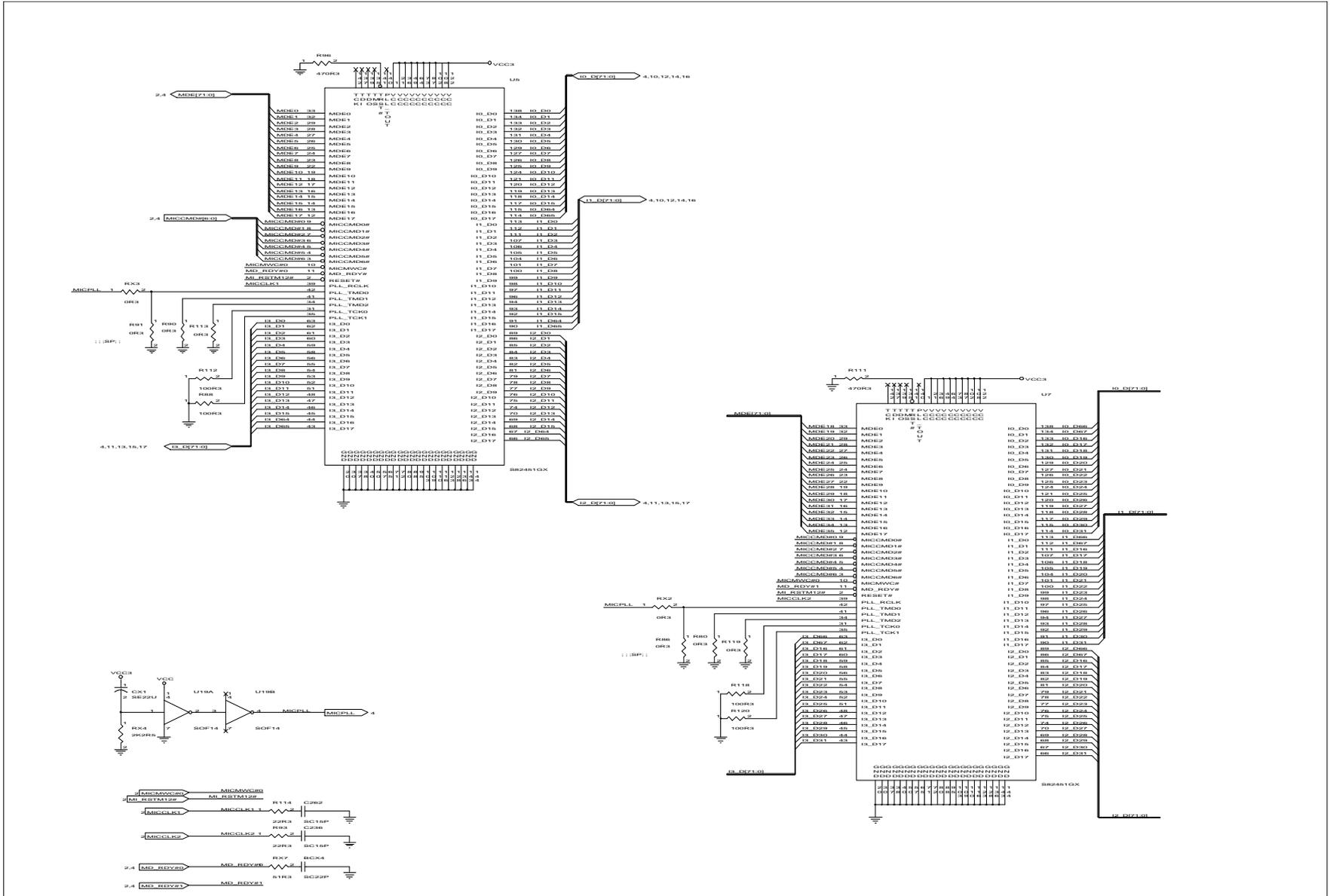
Sample D Revision Note:

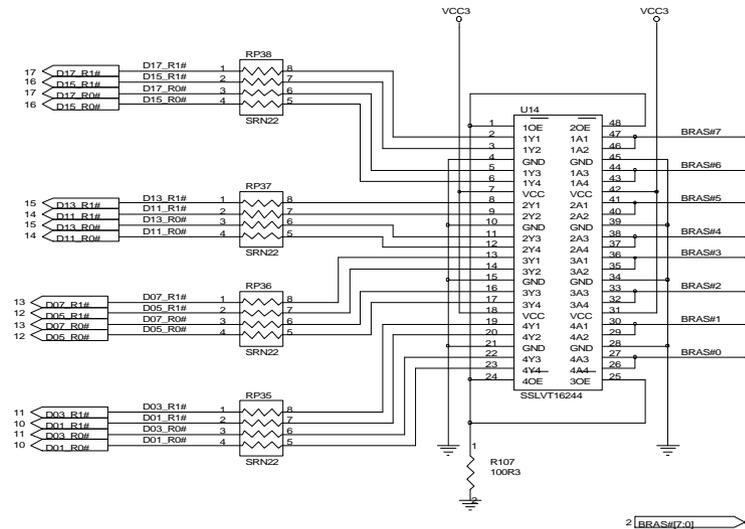
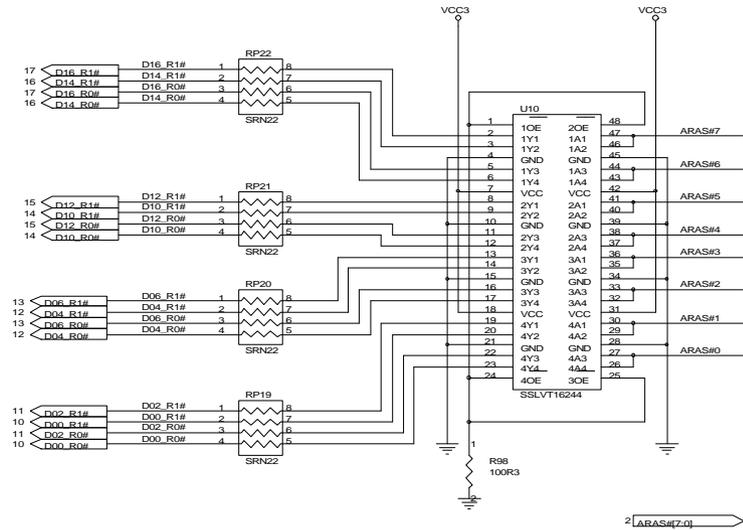
1. ADD 1 F08.
2. ADD RC(47 OHM, 39 PF) FOR MD_RDY#0 AND MD_RDY#1.
3. ADD VCC PIN 181, 184, 261, 264
4. DOUBLE RAS CAS CAP. FOR LAYER1,8 MOUNT SELECTING.
5. REMOVE RAS CAS OR RESISTOR.
6. CHANGE SOME RC TEXT LOCATION.
7. ADD 1 F14 FOR PLL.
8. CHANGE ONE TRACE(TOO CLOSE TO BOARD EDGE IN SC) TO ANOTHER LAYER.



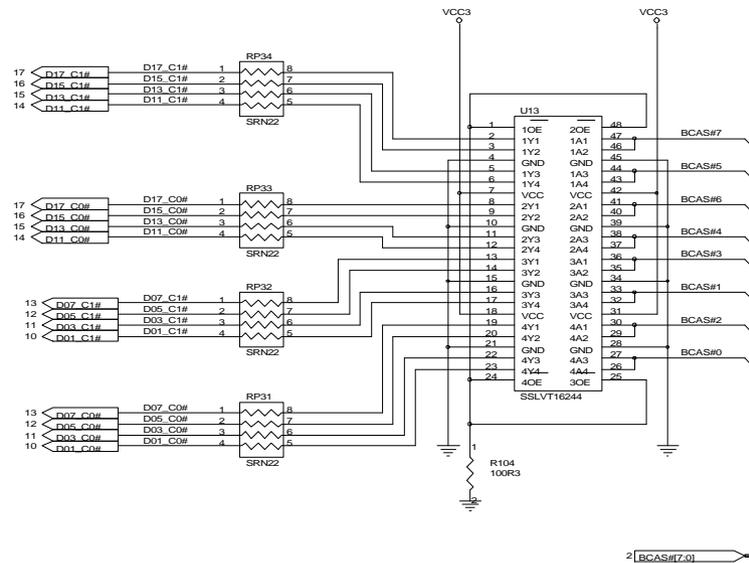
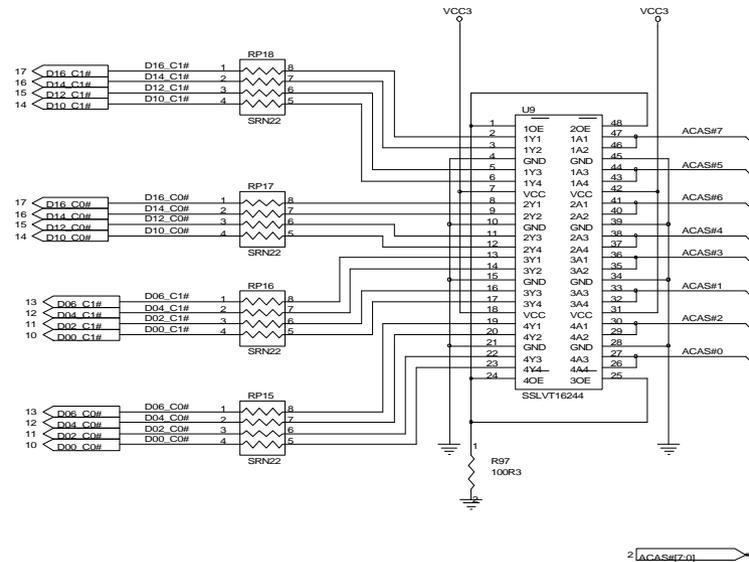
FOR F08, F14

Title		
DIMM MEM BOARD LINK		
Size	Document Number	REV
B		SD
Date:	July 29, 1997	Sheet 1 of 20

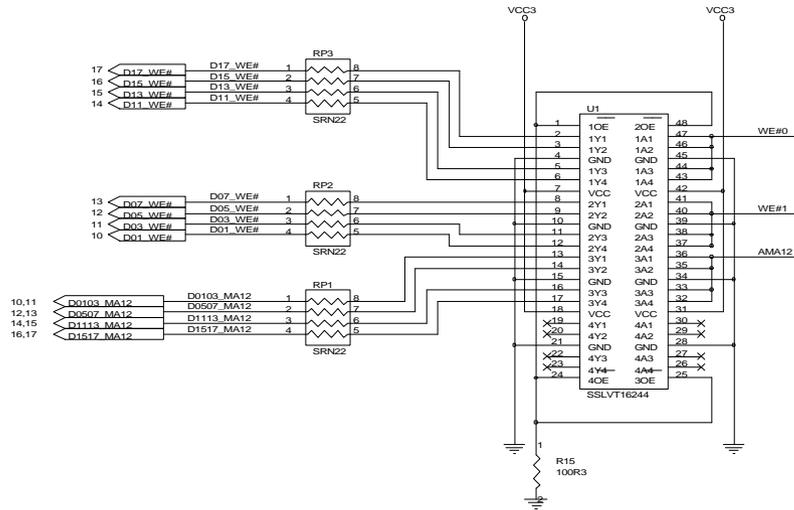
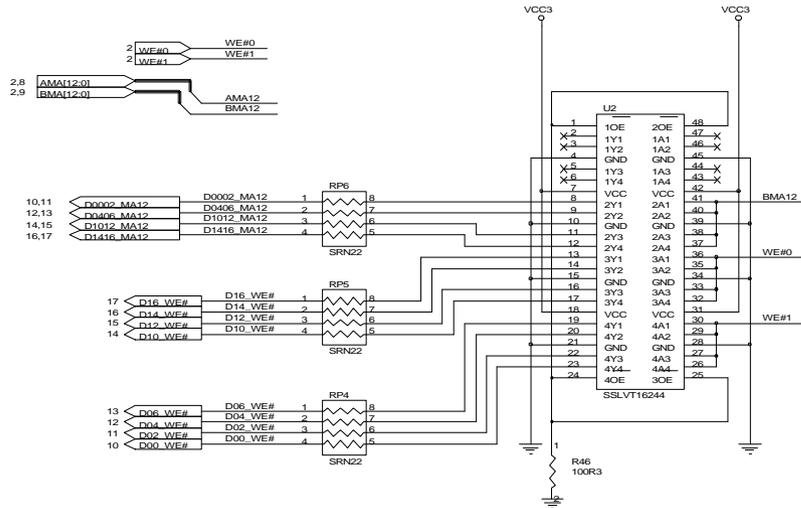




MODEL NO.		X1 DIMM MEM BOARD	
Title			
RAS BUFFER			
Size	Document Number		REV
B			
Date:	Jul 29, 1997	Sheet	5 of 20



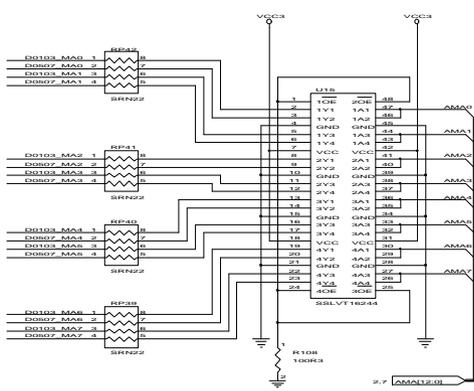
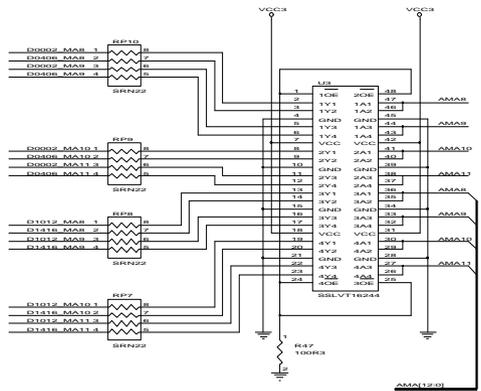
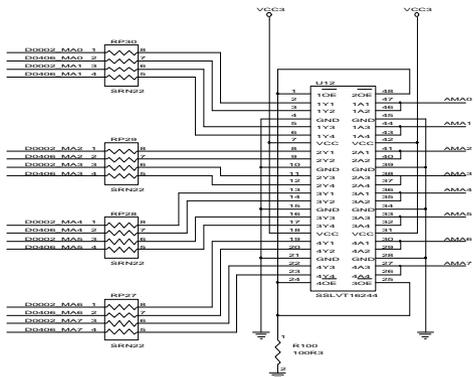
MODEL NO.		X1 DIMM MEM BOARD	
Title			
CAS BUFFER			
Size	Document Number	REV	
B			
Date:	July 28, 1997	Sheet	6 of 20



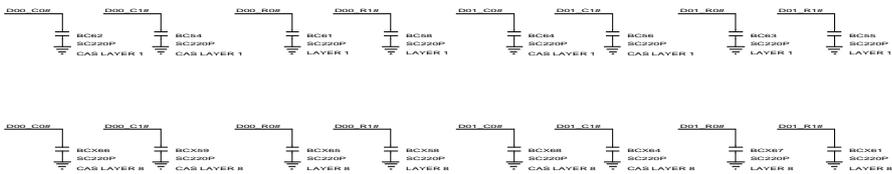
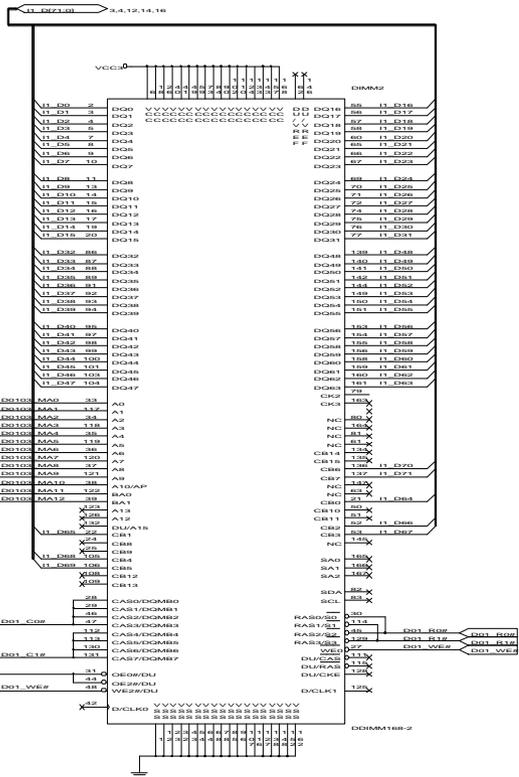
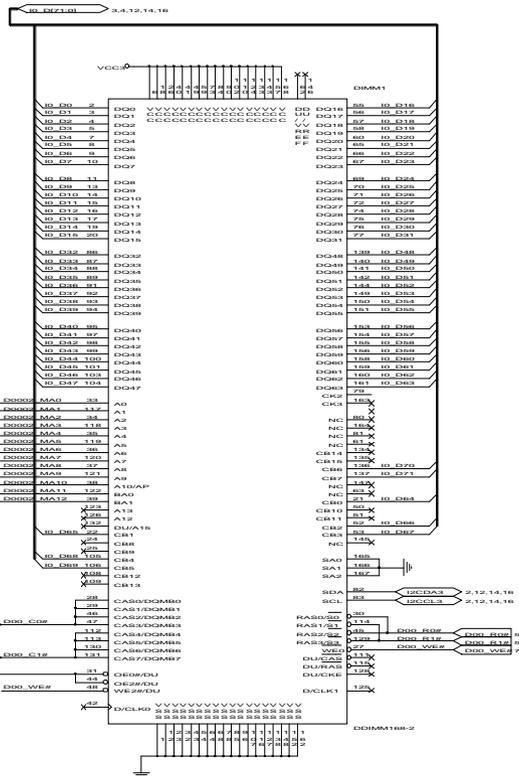
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X1 DIMM MEM BOARD

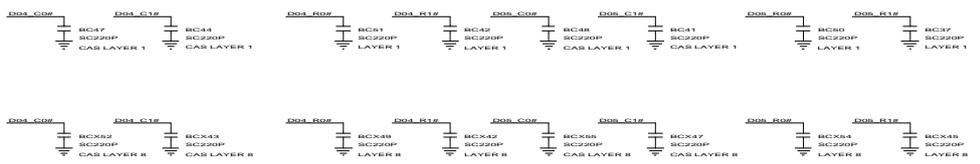
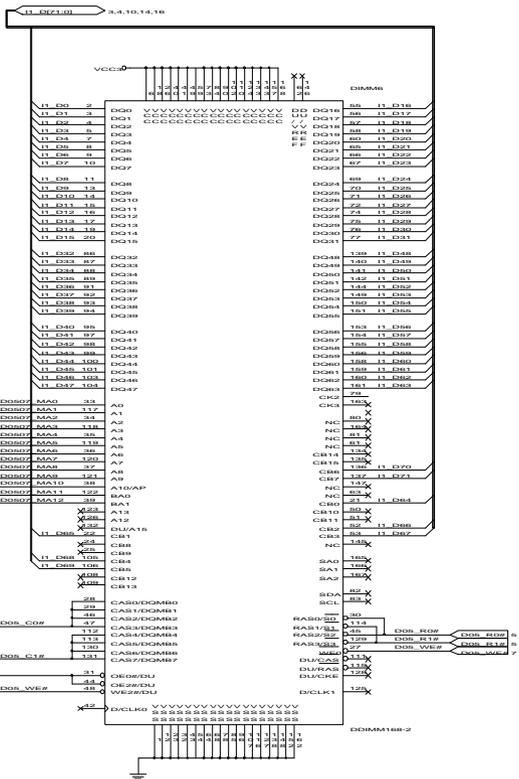
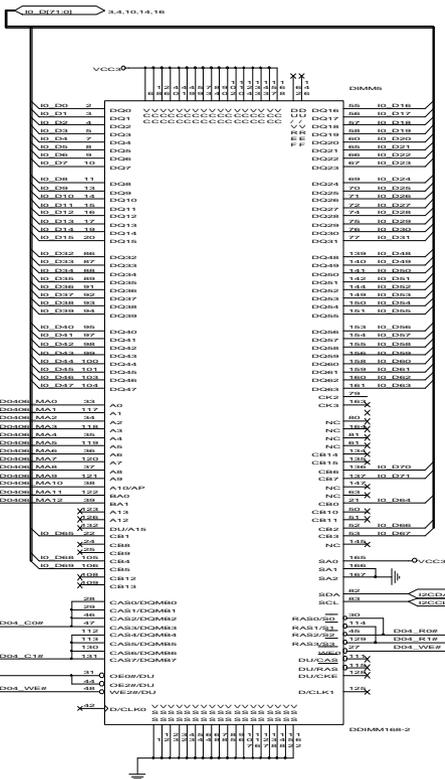
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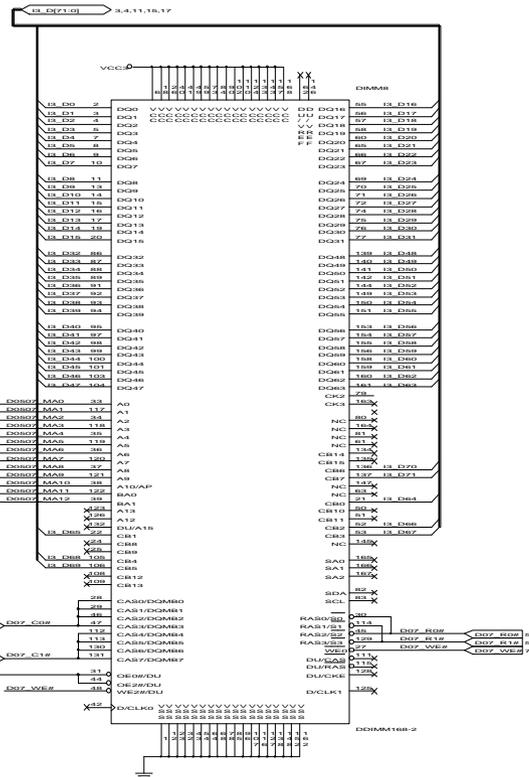
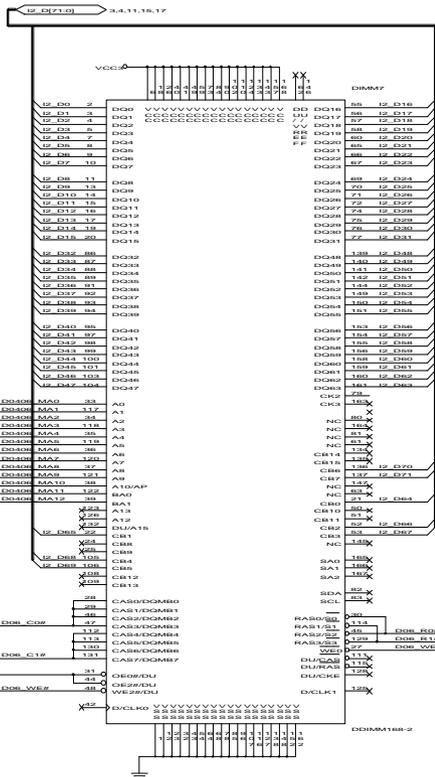
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B Date: July 29, 1997 Sheet 7 of 20

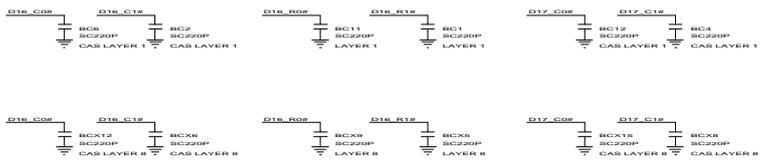
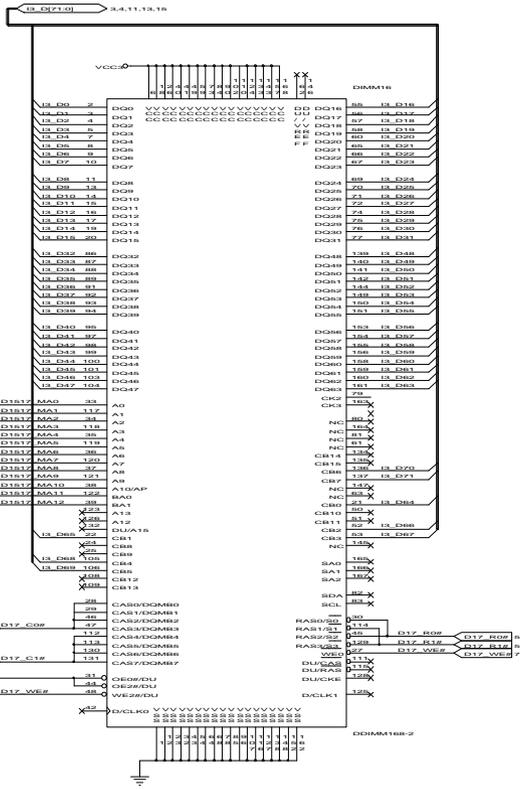
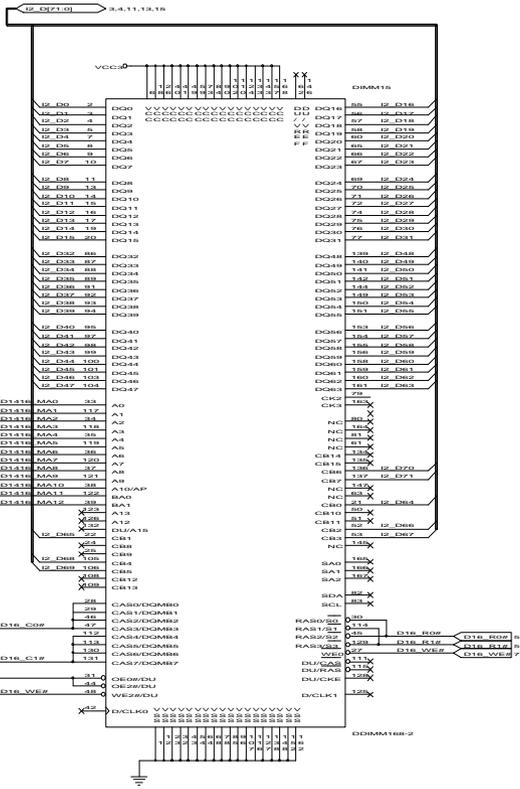


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10.11	END102_MMA6	END102_MMA6
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12.13	END102_MMA19	END102_MMA19
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12.13	END102_MMA25	END102_MMA25
10.11	END102_MMA26	END102_MMA26
12.13	END102_MMA26	END102_MMA26
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12.13	END102_MMA31	END102_MMA31



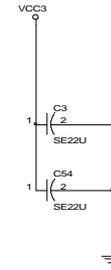
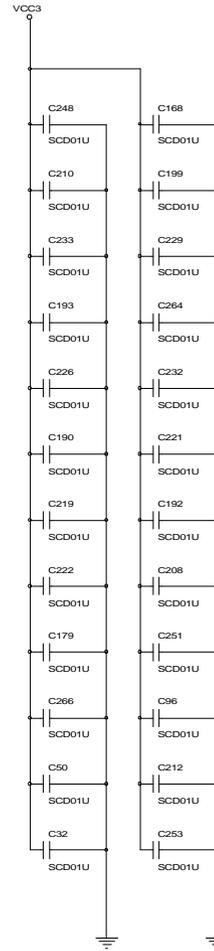
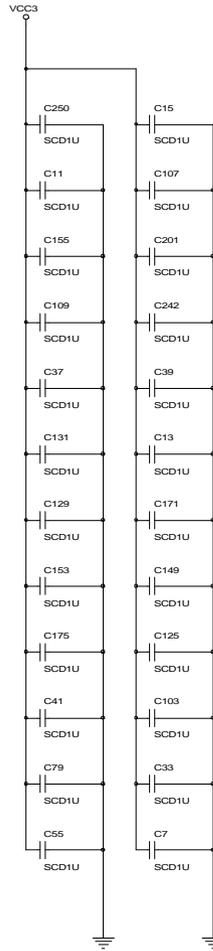
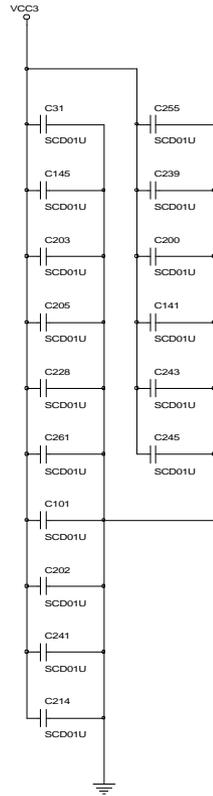
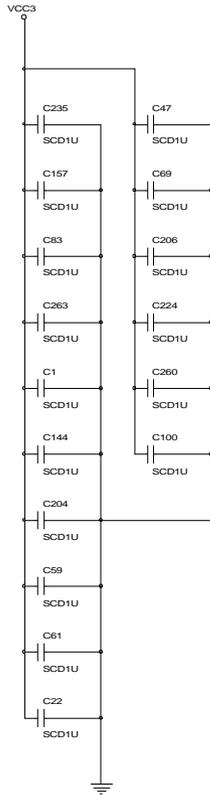






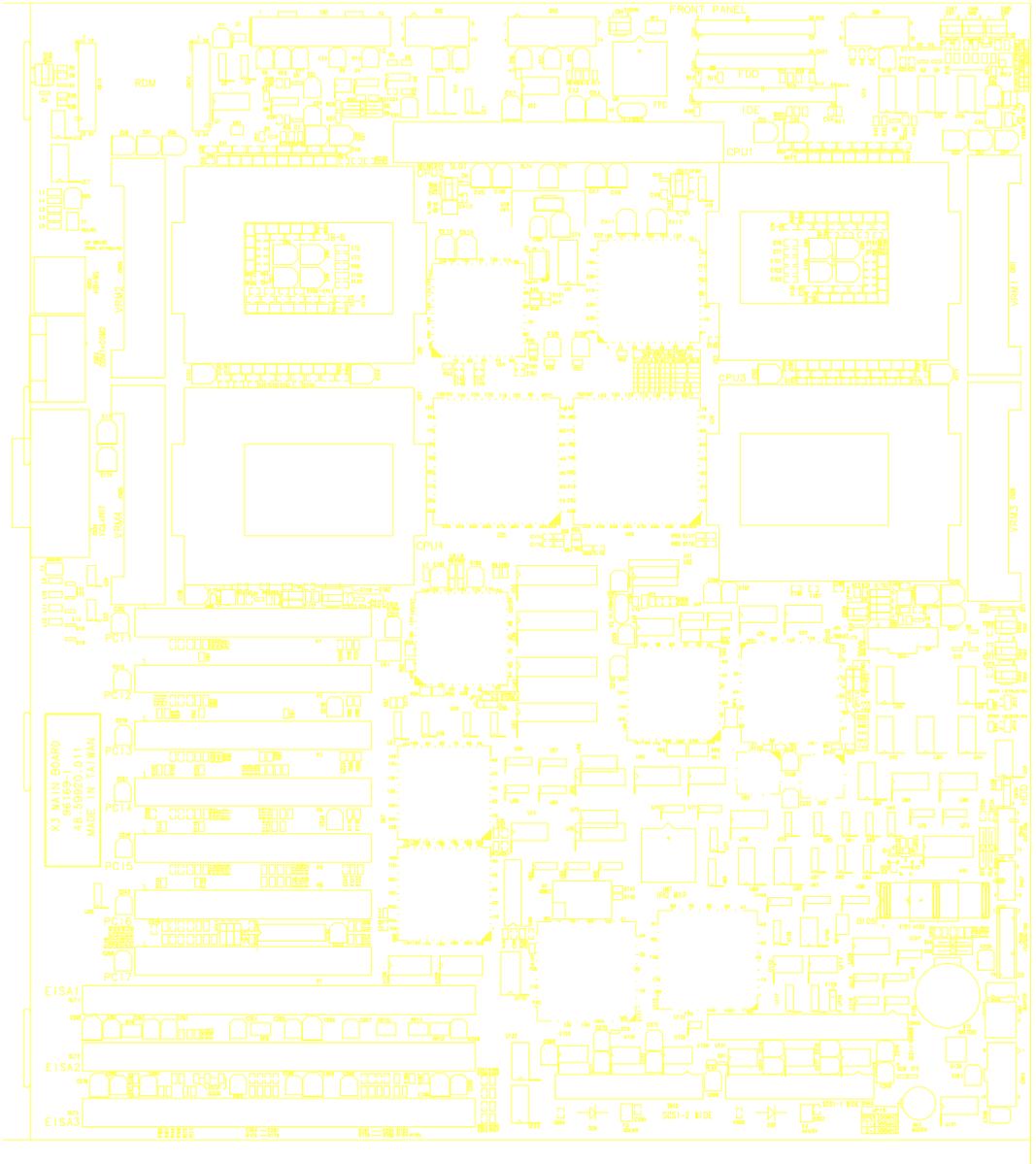
MIC DECOUPLING TO 3.3V, TOTAL 4 MICs
8 CAPS (0.1UF*4, 0.01UF*4) PER MIC

16244 DECOUPLING TO 3.3V, TOTAL 12 16244s
4 CAPS (0.1UF*2, 0.01UF*2) PER 16244
PLUS 2 CAPS OF 22UF



MODEL NO.		X1 DIMM MEM BOARD	
Title			
MIC DECOUPLING			
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Date:	March 28, 1997	Sheet	20 of 20

Silk Screen



96169-1 X3 MAINBOARD TSILK

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BIOS POST Check Points

E.1 Power-On Self-Test (POST)

The Power-On Self Test (POST) is a BIOS procedure that boots the system, initializes and diagnoses the system components, and controls the operation of the power-on password option. If POST discovers errors in system operations at power-on, it displays error messages, generates a check point code at port 80h or even halts the system if the error is fatal.

The main components on the system board that must be diagnosed and/or initialized by POST to ensure system functionality are as follows:

- Microprocessor with built-in numeric coprocessor and cache memory subsystem
- Direct memory access (DMA) controller (8237 module)
- Interrupt system (APIC and 8259 module)
- Three programmable timers (system timer and 8254 module)
- ROM subsystem
- RAM subsystem
- CMOS RAM subsystem and real time clock/calendar with battery backup
- Onboard serial interface controller
- Onboard parallel interface controller
- Embedded hard disk interface and one diskette drive interface
- Keyboard and auxiliary device controllers
- I/O ports
 - two RS232 serial ports
 - one parallel port
 - one PS/2-compatible mouse port
 - one PS/2-compatible keyboard port
- Remote diagnostic module initialization

E.1.1 Post Check Points

When POST executes a task, it uses a series of preset numbers called check points to be latched at port 80h, indicating the stages it is currently running. This latch can be read and shown on a debug board.

Table E-1 describes the Acer common tasks carried out by POST. Each task is denoted by a unique check point number. For other unique check point numbers that are not listed in the table, refer to the corresponding product service guide.

Table E-1 POST Check Points

Check Point	Descriptions
03h	<ul style="list-style-type: none">• Determines BSP
E0h	<ul style="list-style-type: none">• Initializes BSP
F0h	<ul style="list-style-type: none">• Waits for AP initialization
04h	<ul style="list-style-type: none">• Checks CPU ID• Dispatches shutdown path• Determines if the current booting procedure is from cold boot (press reset button or turn the system on), from warm boot, or from exiting BIOS setup. <p><i>Note: At the beginning of POST, port 64 bit 2 (8042 system flag) is read to determine whether this POST is caused by a cold or warm boot. If it is a cold boot, a complete POST is performed. If it is a warm boot, the chip initialization and memory test is eliminated from the POST routine.</i></p>
08h	<ul style="list-style-type: none">• Resets video frame buffer• Resets PIE (periodical interrupt enable), AIE (alarm interrupt enable), and UIE (update-ended interrupt enable) <p><i>Note: These interrupts are disabled in order to avoid any mis-action happened during the POST routine.</i></p>
09h	<ul style="list-style-type: none">• Initializes chipset settings according to CPUs
10h	<ul style="list-style-type: none">• Tests and initializes DMA (8237)
14h	<ul style="list-style-type: none">• Tests and initializes system timer (8254)
18h	<ul style="list-style-type: none">• Tests DRAM refresh cycle, sets default SS:SP= 0:400
1Ch	<ul style="list-style-type: none">• Verifies CMOS shutdown byte, battery and check sum <p><i>Note: Several parts of the POST routine require the system to be in protected mode. When returning to real mode from protected mode, the processor is reset, therefore POST is re-entered. In order to prevent re-initialization of the system, POST reads the shutdown code stored in location 0Fh in CMOS RAM. Then it jumps around the initialization procedure to the appropriate entry point. The CMOS shutdown byte verification assures that CMOS 0Fh area is fine to execute POST properly.</i></p>

Table E-1 POST Check Points (continued)

Check Point	Descriptions
1Ch continued	<ul style="list-style-type: none"> • Initializes default CMOS setting if CMOS is bad. • Initializes RTC time base <p style="margin-left: 40px;"><i>Note: The RTC has an embedded oscillator that generates 32.768 KHz frequency. To initialize RTC time base, turn on this oscillator and set a divisor to 32768 so that RTC can count time correctly</i></p>
1Eh	<ul style="list-style-type: none"> • Determines DRAM type
1Fh	<ul style="list-style-type: none"> • Initializes RDM (Phase I)
20h	<ul style="list-style-type: none"> • Tests KB controller (8041/8042) • Determines KB type • Write default command byte upon KB type
25h	<ul style="list-style-type: none"> • BIOS bootable setting
2Ch	<ul style="list-style-type: none"> • 128K base memory testing. Set default SS:SP= 0:400 <p style="margin-left: 40px;"><i>Note: The 128K base memory area is tested for POST execution. The remaining memory area is tested later</i></p>
30h	<ul style="list-style-type: none"> • System Shadow RAM
22h	<ul style="list-style-type: none"> • Initializes EISA slots
21h	<ul style="list-style-type: none"> • Initializes PCEB and ESC
24h	<ul style="list-style-type: none"> • Testing and Initialization PIC (8259)
34h	<ul style="list-style-type: none"> • DRAM sizing
36h	<ul style="list-style-type: none"> • Loads Pentium Pro CPU update code
3Ch	<ul style="list-style-type: none"> • Initializes interrupt vectors
4Ch	<ul style="list-style-type: none"> • Tests system board requests
35h	<ul style="list-style-type: none"> • Scans the PCI Device and Initialize PCI Slots
4Eh	<ul style="list-style-type: none"> • Scans PnP devices
4Fh	<ul style="list-style-type: none"> • Configures PnP devices
40h	<ul style="list-style-type: none"> • Initializes PCI (1), sets I/O range to OPB
41h	<ul style="list-style-type: none"> • Initializes PCI (2), memory
42h	<ul style="list-style-type: none"> • Initializes PCI (3), pre-memory
44h	<ul style="list-style-type: none"> • Initializes PCI (4)
51h	<ul style="list-style-type: none"> • Copies ROM code to RAM
50h	<ul style="list-style-type: none"> • Initialize video display
54h	<ul style="list-style-type: none"> • Shadows video BIOS if necessary
4Fh	<ul style="list-style-type: none"> • Configures PnP device
44h	<ul style="list-style-type: none"> • Initializes PCI (4)
45h	<ul style="list-style-type: none"> • Initializes PCI (5)

Table E-1 POST Check Points (continued)

Check Point	Descriptions
58h	<ul style="list-style-type: none"> • Sets POST screen mode (Graphic or Text) • Displays Acer (or OEM) logo if necessary • Displays Acer copyright message if necessary • Displays BIOS serial number
59h	<ul style="list-style-type: none"> • Hooks INT 1Ch for quiet boot
64h	<ul style="list-style-type: none"> • Resets KB device; checks KB status
5Ch	<ul style="list-style-type: none"> • Tests memory
5Eh	<ul style="list-style-type: none"> • Loads Pentium Pro CPU update code
8Ch	<ul style="list-style-type: none"> • Building MP system
5Ah	<ul style="list-style-type: none"> • Initializes SMRAM, SMI
70h	<ul style="list-style-type: none"> • Tests parallel port
74h	<ul style="list-style-type: none"> • Tests serial port
75h	<ul style="list-style-type: none"> • Initializes RDM (Phase II)
78h	<ul style="list-style-type: none"> • Resets math coprocessor
7Ch	<ul style="list-style-type: none"> • Checks and initializes pointing device
80h	<ul style="list-style-type: none"> • Sets security status
60h	<ul style="list-style-type: none"> • Sizes external cache • Tests external cache (SRAM and controller) • Enables internal cache if necessary • Enables external cache if necessary
82h	<ul style="list-style-type: none"> • Copies Setup code from ROM to shadow RAM
84h	<ul style="list-style-type: none"> • Initializes KB device • Sets KB led upon setup requests • Enables KB device
6Ch	<ul style="list-style-type: none"> • Tests FDD parameter table setup <p><i>Note: The FDD LED should flash once and its head should be positioned.</i></p>
88h	<ul style="list-style-type: none"> • Tests HDD parameter table setup
89h	<ul style="list-style-type: none"> • Tests CPU Internal frequency
90h	<ul style="list-style-type: none"> • Displays POST status if necessary • Changes POST mode to default text mode
93h	<ul style="list-style-type: none"> • Rehooks INT 1Ch for quiet boot
AEh	<ul style="list-style-type: none"> • Sets program chipset
AFh	<ul style="list-style-type: none"> • Sets program chipset

Table E-1 POST Check Points (continued)

Check Point	Descriptions
94h	<ul style="list-style-type: none"> • Initializes ISA expansion ROM • Shadows I/O ROM if setup requests • Builds up free expansion ROM table
96h	<ul style="list-style-type: none"> • Initializes PCI Card ROM • Shadows I/O ROM if setup requests • Builds up free expansion ROM table
A0h	<ul style="list-style-type: none"> • Sets time and date
A4h	<ul style="list-style-type: none"> • Initializes security feature
A0h	<ul style="list-style-type: none"> • Initializes timer counter for DOS use
ACh	<ul style="list-style-type: none"> • Enables NMI • Enables parity checking • Sets video mode
AFh	<ul style="list-style-type: none"> • Initializes RDM (Phase III)
B0h	<ul style="list-style-type: none"> • Checks power on password • Displays configuration table • Clears memory buffer used for POST • Selects boot device
BDh	<ul style="list-style-type: none"> • Shutdown 5
BEh	<ul style="list-style-type: none"> • Shutdown A
BFh	<ul style="list-style-type: none"> • Shutdown B

E.2 POST Error Messages

The power-on self-test (POST) is a program routine performed by the system BIOS. If there is any error during the POST routine, BIOS detects it and shows the corresponding error message on the CRT screen to guide the technical service engineer on the repair procedure.

Table E-2 POST Error Messages

Error Message	Possible Cause and Corrective Action
Memory Error at MMMM:SSSS:OOOOh (R:xxxxh, W:xxxxh)	<ul style="list-style-type: none">• DRAM, SIMMs, or add-on memory card may be defective. <p>➡ Replace the DRAM chips or the SIMMs</p>
Keyboard Interface Error	<ul style="list-style-type: none">• POST detects an error in the interface between the system board and the keyboard. The keyboard circuit module may be defective. <p>➡ Check the keyboard interface circuit or change the keyboard.</p>
Keyboard Error or Keyboard Not Connected	<ul style="list-style-type: none">• POST detects an error in the keyboard; or the keyboard is not connected. <p>➡ Reconnect or replace the keyboard.</p>
Keyboard Locked	<ul style="list-style-type: none">• The keyboard lock feature prevents any access to keyboard. <p>➡ Unlock the keyboard.</p>
Pointing Device Error	<ul style="list-style-type: none">• The pointing device installed may be bad or the device is improperly connected. <p>➡ Reconnect or replace the pointing device.</p>
Pointing Device Interface Error	<ul style="list-style-type: none">• POST detects an error in the interface between the system board and the pointing device. <p>➡ Check the keyboard interface circuit.</p>
Pointing Device IRQ Conflict	<ul style="list-style-type: none">• The IRQ setting of add-on card and/or system board conflicted with onboard pointing device. <p>➡ Enter SETUP and change the setting of IRQ12.</p>

Table E-2 POST Error Messages (continued)

Error Message	Possible Cause and Corrective Action
Hard Disk 0 Error Hard Disk 1 Error	<ul style="list-style-type: none"> • The hard disk drive may be bad, type mismatched, or not properly installed. ➤ Replace the disk drive or the hard disk drive controller. Check the HDD cable connections and CMOS setup configuration.
Diskette Drive A Type Mismatch Diskette Drive B Type Mismatch	<ul style="list-style-type: none"> • Diskette A (or B) may be bad, not properly installed, or type mismatched. ➤ Replace diskette drive, checking its cabling and its configuration in Setup.
Diskette Drive A Error Diskette Drive B Error	<ul style="list-style-type: none"> • Diskette A or B may be bad. ➤ Replace the diskette drive.
Diskette Drive Controller Error	<ul style="list-style-type: none"> • This error is caused by any of the following: <ol style="list-style-type: none"> (1) The power supply cable is not connected to the diskette drive connector. (2) The diskette drive cable is not plugged to the diskette drive interface on the system board. (3) The diskette drive controller is defective. ➤ Check the diskette drive cable and its connections. If the cable is good and properly connected, the diskette drive controller may be the problem. Change the diskette drive controller or disable the onboard controller by installing another add-on card with a controller.)
Serial Port 1 Conflict Serial Port 2 Conflict	<ul style="list-style-type: none"> • Onboard serial port address conflicts with the add-on card serial port. ➤ Change the onboard serial port address in Setup or change the add-on card serial port address.
Parallel Port Conflict	<ul style="list-style-type: none"> • Onboard parallel port address conflicts with the parallel port of add-on card. ➤ Change onboard parallel port address in CMOS SETUP or set the parallel port address of add-on card to others.
Real Time Clock Error	<ul style="list-style-type: none"> • POST detects a real-time clock error. ➤ Check RTC circuit or replace the RTC.
CMOS Battery Bad	<ul style="list-style-type: none"> • CMOS battery power lost. ➤ Replace the onboard lithium battery

Table E-2 POST Error Messages (continued)

Error Message	Possible Cause and Corrective Action
CMOS Checksum Error	<ul style="list-style-type: none"> • CMOS RAM error. ➤ Run Setup again and reconfigure the system.
NVRAM checksum Error	<ul style="list-style-type: none"> • The NVRAM in the EISA model contains EISA configuration information. Accidental data writes in the NVRAM area causes an error. POST detects the error and displays the corresponding error message. ➤ Run EISA configuration utility (ECU) to restore the original EISA configuration data.
PCI Device Error	<ul style="list-style-type: none"> • PCI device may be bad. ➤ Check the PCI card. Replace if bad.
System Resource Conflict	<ul style="list-style-type: none"> • Some system resources conflict with the resources required by the PCI device. ➤ Run Setup to reconfigure the system.
IRQ Setting Error	<ul style="list-style-type: none"> • Wrong IRQ setting for the PCI device. ➤ Run Setup to reconfigure the system.
Expansion ROM Allocation Fail	<ul style="list-style-type: none"> • The I/O expansion ROM fails to allocate for the PCI device. ➤ Change the I/O expansion ROM address.
BIOS Update code mismatch	<ul style="list-style-type: none"> • The BIOS update code version is mismatch with CPU ID ➤ Run Intel BIOS update utility under DOS mode.

E.3 NMI Error and Warning Messages

Non-Maskable Interrupt (NMI) causes the CPU routines to be interrupted and the system to be halted.

Table E-3 NMI Error Messages and Warning Messages

Error Message	Possible Cause and Corrective Action
RAM Parity Error	<ul style="list-style-type: none"> • DRAM chips, SIMMs, or add-on memory card may be defective. ➤ Replace the DRAM chips or SIMMs, or disable parity check in Setup if the model supports it.
I/O Parity Error	<ul style="list-style-type: none"> • The I/O access is not correct. ➤ Check all I/O related circuits (i.e. system I/O controller, memory controller, interrupt controller, DMA controller, etc.)
Press Ctrl_Alt_Esc key to enter SETUP or F1 key to Continue...	<ul style="list-style-type: none"> • A system configuration error is detected, or the hardware configuration does not match the Setup configuration data in CMOS. ➤ Press CTRL + ALT + ESC to reconfigure the system.
Press F1 key to enter SETUP or other key to continue...	<ul style="list-style-type: none"> • This message appears on the screen when a terminal instead of a console monitor is installed. ➤ Press F1 to enter Setup and check the configuration. Pressing any other key prevents entering Setup.
Press ESC to turn off NMI, or any key to reboot	<ul style="list-style-type: none"> • A Non-Maskable Interrupt (NMI) occurs. ➤ Press ESC to reject NMI error or press any other key to reboot the system.
Insert system diskette and press <Enter> key to reboot	<ul style="list-style-type: none"> • A non-bootable diskette is detected on the diskette drive when the system boots. ➤ Insert a bootable disk in the diskette drive or remove this disk if a hard disk drive is installed.

Table E-3 NMI Error Messages and Warning Messages (continued)

Error Message	Possible Cause and Corrective Action
Equipment Configuration Error	<ul style="list-style-type: none">• The hardware configuration does not match the Setup configuration data.➔ Run Setup and reconfigure the system.
EISA Configuration Error	<ul style="list-style-type: none">• This message appears in any one of the following conditions:<ol style="list-style-type: none">(1) An add-on card is plugged into the wrong expansion slot.(2) The ECU was not executed when a new add-on card is installed.(3) A old add-on card was move to another slot.➔ Run ECU.