megatel

Features:

Wildcard 88™

- Supports XT Turbo mode CPU clock speeds of 4.77 MHz, 7.15 MHz and 9.54 Mhz
- Supports up to 32k Bytes of onboard BIOS EPROM
- Small 2" x 4" form factor
- BIOS available for easy integration
- Onboard keyboard controller
- Reduces overall system costs and factory overhead
- Onboard DRAM controller for easy system design
- Supports up to 640k of system DRAM
- Reduces XT parts count by up to 75%
- Onboard configuration registers provide for customizations

The *Wildcard 88™* Family integrates all the functions of the IBM® PC XT* motherboard, except DRAM and DRAM drivers, onto a circuit card slightly larger than a business card. It provides the lowest cost, smallest footprint solution for designing an XT class system.

The Wildcard 88 Module reduces parts count by 75% over the standard IBM PC/XT implementation thus reducing both costs and boardspace while improving overall system reliability.

Wildcard 88 Module replaces the following system components:

80C88	8-bit CPU	DRAM Control Logic (CAS,RAS, and MUX)
82C37A-5	DMA Controller	XT I/O Channel Control and Buffers
82C53-5	Counter Timer Chip	DMA Page Register
82C55A	Parallel I/O	Keyboard Control
82C59A-2	Programmable Interrupt	Speaker Control
82C84A-5	Clock and Wait State Generator	Miscellaneous Discretes
82C88	Bus Controller	
8087	Numeric Data Processor Socket*	

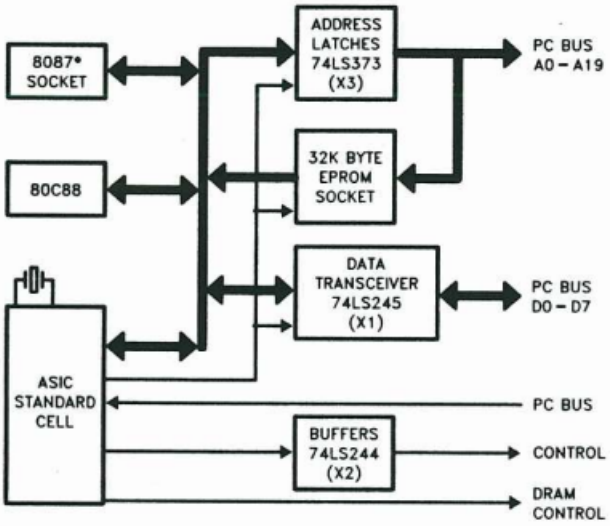
ORDERING INFORMATION

PRODUCT	CRYSTAL Freq (MHz)	8087 Socket	SPEED SELECTION (MHz)
Wildcard -88™	14.31818	NO	4.77, 7.15
Wildcard -88N™	14.31818	YES	4.77, 7.15
Wildcard -88 - 10N™	26.63636	YES	4,77, 7.15, 9.54

NOTE: Wildcard 88™ Family includes the above products. Further reference to Wildcard 88™ module includes all these products unless otherwise specified.

* Wildcard -88N™ and Wildcard -88- 10N™

2.0 WILDCARD-88™ BLOCK DIAGRAM



*Device's socket offered on the Wildcard-88N™ and Wildcard-88-10N™ modules only.

3.0 FUNCTIONAL DESCRIPTION

3.1 Wildcard-88™ Pinout Description

Symbol	Pin No.	Type	Name and Function
A19, A18, A0–A7, A17, A16, A15–A8	1, 2 3–10 19, 20 23–30	O	**BUFFERED CPU ADDRESS:** These lines provide the memory and I/O address for the entire bus cycle. These lines are always driven by the Wildcard-88™ module and are never allowed to float. These lines are active high.
D0–D7	11–18	I/O	**BI-DIRECTIONAL DATA BUS:** These lines constitute the Wildcard-88™ data bus. Data is input on these lines during memory, I/O, and interrupt acknowledge read cycles and data is output on these lines during memory and I/O write cycles. These lines are active high.
+DRQ2	21	I	**DMA REQUEST LINE 2 (Floppy):** DRQ2 is an individual asynchronous channel request input used by peripheral circuits to obtain DMA service. In the traditional PC/XT architecture this channel is used by the floppy disk controller. This line is active high.
+DRQ1	22	I	**DMA REQUEST LINE 1 (Spare):** DRQ1 is an individual asynchronous channel request input used by peripheral circuits to obtain DMA service. In the traditional PC/XT architecture this channel is unused. This line is active high.

3.1 Wildcard-88™ Pinout Description (Continued)

Symbol	Pin No.	Type	Name and Function
+ IRQ4	31	I	**INTERRUPT REQUEST 4 (COM1):** IRQ4 is an asynchronous input used to request interrupt service. An interrupt request is executed by raising IRQ4 (low to high) and holding it high until it is acknowledged (edge triggered mode), or by holding IRQ4 at a high level until it is acknowledged (level triggered mode). In the traditional PC/XT architecture this channel is used by the COM1 port.
+ IRQ3	32	I	**INTERRUPT REQUEST 3 (COM2):** IRQ3 is an asynchronous input used to request interrupt service. An interrupt request is executed by raising IRQ3 (low to high) and holding it high until it is acknowledged (edge triggered mode), or holding IRQ3 at a high level until it is acknowledged (level triggered mode). In the traditional PC/XT architecture this channel is used by the COM2 port.
+ 5V	33, 34	I	**MODULE + 5V POWER.**
GND	35, 36	I	**MODULE GROUND.**
+ IRQ2	37	I	**INTERRUPT REQUEST 2 (LPT2):** IRQ2 is an asynchronous input used to request interrupt service. An interrupt request is executed by raising IRQ2 (low to high) and holding it high until it is acknowledged (edge triggered mode), or holding IRQ 2 at a high level until it is acknowledged (level triggered mode). In the traditional PC/XT architecture this channel is used by the LPT2 port.
+ DRQ3	38	I	**DMA REQUEST LINE 3 (Fixed Disk):** DRQ3 is an individual asynchronous channel request input used by peripheral circuits to obtain DMA service. In the traditional PC/XT architecture this channel is used by the fixed disk controller. This line is active high.
− NMI	39	I	**NON-MASKABLE INTERRUPT:** NMI is used to indicate that an error occurred during an I/O operation on the expansion bus. If I/O checking in control register 0 is enabled AND parity is enabled in control register 2, a low on this line will generate an interrupt to the CPU. This line is active low. The traditional name for this signal is I/OCHCK.
+ I/O READY	40	I	**I/O READY:** I/O Ready is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. This line is active high. A low input on this line will insert wait-states into the processor's bus cycle.
+ KBDATA	41	I/O	**KEYBOARD DATA LINE:** KBDATA is the serial data line from the keyboard.
+ KBCLK	42	O	**KEYBOARD CLOCK LINE:** KBCLK is the clock line used to synchronize data transmission from the keyboard to the Wildcard-88™ Module.
+ IRQ5	43	I	**INTERRUPT REQUEST 5 (Fixed Disk):** IRQ5 is an asynchronous input used to request interrupt service. An interrupt request is executed by raising IRQ2 (low to high) and holding it high until it is acknowledged (edge triggered mode), or by holding IRQ5 at a high level until it is acknowledged (level triggered mode). In the traditional PC/XT architecture this channel is used by the fixed disk.

3.1 Wildcard-88™ Pinout Description (Continued)

Symbol	Pin No.	Type	Name and Function
+AEN	44	O	**ADDRESS ENABLE:** AEN is used to indicate that a DMA bus cycle is "in-progress". This signal is active high.
+CLOCK	45	O	**BUS CLOCK:** CLOCK is the processor clock. The speed of this clock is software selectable.
+OSC	46	O	**14.31818 MHz OSCILLATOR:** OSC is a constant speed clock.
+T/C	47	O	**DMA TRANSFER COMPLETE:** T/C indicates that the current DMA transfer has reached terminal count. This signal is active high.
−DAK3 to −DAK0	48–51	O	**DMA ACKNOWLEDGE LINES 3, 2, 1, and 0:** DAK is used to notify the individual peripheral when it has been granted a DMA cycle. **NOTE:** Because DMA channel 0 is dedicated to refreshing the DRAM, DAK0 can be used to indicate a DRAM refresh cycle is in progress. These signals are active low.
+IRQ6, +IRQ7	52, 53	I	**INTERRUPT REQUEST 6 (Floppy) and INTERRUPT REQUEST 7 (LPT1):** IRQ6 and IRQ7 are asynchronous inputs used to request interrupt service. An interrupt request is executed by raising IRQx (low to high) and holding it high until it is acknowledged (edge triggered mode), or by holding IRQx at a high level until it is acknowledged (level triggered mode). In the traditional PC/XT architecture IRQ6 is used by the floppy controller and IRQ7 is used by the LPT1 port.
+CAS	54	O	**COLUMN ADDRESS STROBE:** CAS is used to strobe the column address into the DRAM devices. It must be buffered and inverted before going to the DRAM array. This signal is active high.
+RAS0 – +RAS2	55–57	O	**ROW ADDRESS STROBE 0, 1, and 2:** RAS is used to strobe the row address into the DRAM devices. It must be buffered and inverted before going to the DRAM array. These signals are active high.
N/C	58		No Connect (Reserved for future option)*
− DRAM	59	O	**TRANSCEIVER ENABLE:** DRAM is used to enable the DRAM transceiver. It is intended to be connected directly to the Gate pin of a '245 transceiver. This signal is active low.
− IOR	60	O	**I/O READ:** IOR instructs an I/O device to place data onto the I/O channel. This signal is active low.
− IOW	61	O	**I/O WRITE:** IOW instructs an I/O device to read data off of the I/O channel. This signal is active low.
− MEMR	62	O	**MEMORY READ:** MEMR instructs the memory to place data onto the I/O channel. The signal is active low
− MEMW	63	O	**MEMORY WRITE:** MEMW instructs the memory to read data off of the I/O channel. This signal is active low.
+ ALE	64	O	**ADDRESS LATCH ENABLE:** ALE serves to strobe an address into the address latches. This signal is active high and latch occurs on the falling (high to low) transition. ALE is intended for use with transparent D type latches.

3.1 Wildcard-88™ Pinout Description (Continued)

Symbol	Pin No.	Type	Name and Function
+ RESET DRV	65	O	**RESET DRV:** RESET DRV indicates that a reset condition is in progress. This signal is active high.
+ SPKR	66	O	**SPEAKER DATA:** SPKR is meant to drive a speaker. The output must be conditioned by external circuitry.
+ MUX	67	O	**MULTIPLEXER CONTROL:** MUX is used to switch the address multiplexers driving the DRAM array. It is intended to be connected directly to the SEL inputs of '158 multiplexers.
N/C	68		No Connect (reserved for future option)*

*These two no-connects are for Wildcard-88™ and Wildcard-88-10™ modules only.

The following are pin descriptions of pins 58 and 68 on Wildcard-88N™ and Wildcard-88-10N™ modules only.

– RESET	58	I	**RESET:** RESET is used to force a hardware reset of Wildcard-88™ module. This signal is active low.
– VID0	68	I	**VIDEO SELECT:** VID0 is used to set video option selection externally.

3.2 Board Description

The Wildcard-88 module consists of 2 dice (CPU and ASIC), 6 octal buffers, BIOS EPROM socket, 8087 Numeric Data Processor (NDP or coprocessor) socket†, and miscellaneous discrete parts mounted on a PC board. Signals to and from the board are brought in and out via a 68 pin card edge connector on .050" spacings. The board is plugged into a high density SIM (Single In-line Module) card edge connector.

The board functions as an IBM PC/XT Planar replacement and hence faithfully reproduces the XT hardware and software environment. The Wildcard-88 module engine is an 80C88 microprocessor chip mounted in die form on the PCB.

The standard Intel LSI peripheral chips (82C37A, 82C53, 82C55A, 82C59A, 82C84A, and 82C88) required for PC/XT compatibility are replaced by an ASIC die mounted directly on the PCB. This ASIC die also includes miscellaneous glue logic required in a typical PC/XT system.

Signals from the ASIC are buffered onboard by 6 ALS SSI components. These buffers allow the Wildcard-88 module to interface directly to standard PC/XT peripheral cards.

†Supported on Wildcard-88N™ and Wildcard-88-10N™ modules only.
††Support on Wildcard-88-10™ and Wildcard-88-10N™ modules only.

3.3 BIOS EPROM

The Wildcard-88™ module includes a socket for up to 32K bytes of EPROM which allows sufficient space for customer specific BIOS implementations. The Wildcard-88™ module is designed to work with a 250 ns BIOS EPROM. The wait states versus CPU clock speed for EPROM accesses are:

Clock Speed	Wait States
4.77 MHz	0
7.15 MHz	2
9.54 MHz	4††

3.4 DRAM Requirements

The Wildcard-88 module supplies all memory control signals (including RAS, CAS, address multipexers and data path control) necessary to support 640K of system DRAM. Since the Wildcard-88 module contains the DRAM control circuitry, only off-board buffer logic is required.

The Wildcard-88 module requires 120 ns DRAMs and ALS buffer logic.

3.5 Option Jumpers

There are three jumpers on the Wildcard-88 module: J1, J2, and P1.

J1 and J2 provide customer specific video option selection as follows:

	Wildcard-88™ Wildcard-88-10™		Wildcard-88N™ Wildcard-88-10N™	
Video Mode	J1 (VID1)	J2 (VID0)	J1 (VID0)	J2 (VID1)
MONO or MONO and GRAPHICS	OUT	OUT	OUT	OUT
80 x 25 GRAPHICS	OUT	IN	IN	OUT
40 x 25 GRAPHICS	IN	OUT	OUT	IN
None	IN	IN	IN	IN

NOTE:
1 (logic high) represents jumper OUT and
0 (logic low) represents jumper IN.

The Wildcard-88N and Wildcard-88-10N modules allow the video option selection (VID0) to be set externally. Pin #68 of the edge connector provides a direct input for VID0 without having to jumper J1.

P1 provides a two pin header which allows for external reset of the Wildcard-88N module. By adding a switch across the stake pins of P1, the system can be reset.

The Wildcard-88N module also allows for reset on the edge connector. Pin #58 of the edge connector is a direct input to reset the system.

This is provided for systems where a front panel reset switch is required. The line is conditioned by a 10K pullup resistor and a 15 μF grounded capacitor.

3.6 8087 Coprocessor Socket (N and 10N Only)

The Wildcard-88N and Wildcard-88-10N modules provide a socket for installation of the 8087 coprocessor. The 8087 is a high speed numeric data processor that can speed up numeric calculations by a factor of 10 to 100.

3.7 Pullup Resistors Requirement

It is always required to connect a 4.7K ohm pullup resistors to pin #39 (NMI) and pin #40 (I/O Ready) of the system using the Wildcard-88 module. This requirement will insure compatability with PC/XT bus specifications.

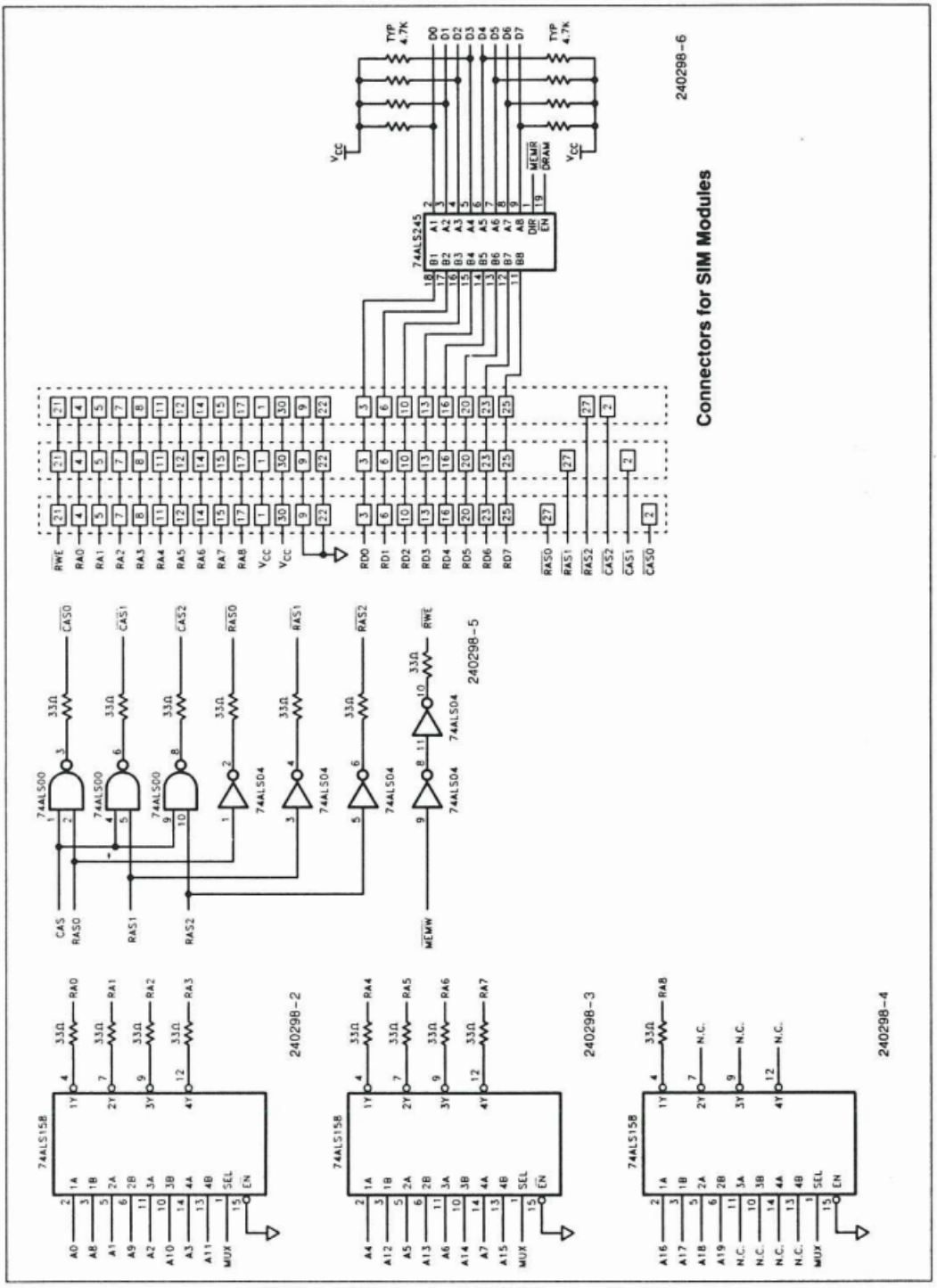
4.0 OPERATION DESCRIPTION

4.1 DRAM Controller

The Wildcard-88 module provides all the necessary signals to control 640K of DRAM using either 256K × 1 or 256K × 4 chips. Three decoded RAS lines are provided for selecting banks of DRAM. One MUX line is provided for controlling the memory address multiplexers. An undecoded CAS line is also provided.

A typical DRAM section, using the Wildcard-88 module, would require the following components:

Item	Qty	Description
001	3	I.C. 74ALS158
002	1	I.C. 74ALS245
003	1	I.C. 74ALS00
004	1	I.C. 74ALS04
005	3	256K x 8 DRAM modules 120 ns
006	2	RES DIP 16P 33 OHM SERIES
007	1	RES DIP 14P 4.7K PARALLEL
008	6	CAP .01 UF MONOLITHIC 50V
009	6	CAP .33 UF MONOLITHIC 50V



Wildcard-88™ Typical DRAM Memory Section

4.2 Speaker Control

The Wildcard-88 module provides a speaker control line compatible with the IBM PC/XT motherboard 8255/8253 combination. External logic is required to buffer the Wildcard SPKR signal to the speaker.

The following is a recommended circuit for the speaker control:

Item	Qty	Description
001	1	RES 33 OHM, ¼W, 5%
002	1	CAP .01 μF MONOLITHIC, 50V
003	1	HEADER, SIP, 4 PIN .100" CNTR
004	1	TRANSISTOR 2N2222
005	1	I.C. 74ALS04*

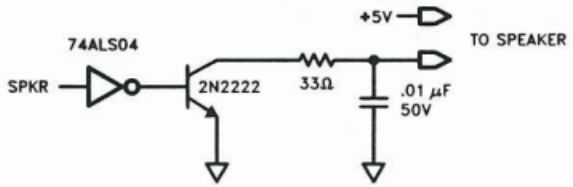
4.3 Keyboard Controller

The Wildcard-88 module supplies all the logic required to implement the PC/XT keyboard interface (8255 + glue). Signals +KBDCLK and +KBDATA are bi-directional lines for communicating with the keyboard. In addition, many OEM keyboards support an external −KBDRESET function. The Wildcard-88N Module +RESET DRV signal may be inverted to support this feature. The Wildcard-88 module +KBDATA and +KBCLK lines should both be conditioned using a 4.7K pullup resistor and a 47 pF, 50V capacitor to ground on each line.

Item	Qty	Description
001	2	RES 4.7K OHM, ¼W, 5%
002	2	CAP 47 pF MONOLITHIC, 50V
003	1	CONNECTOR, 5 PIN, FEMALE DIN, PCB MOUNT
004	1	I.C. 74ALS04*

*Only one gate of the 74ALS04 is required

Speaker Section Schematic



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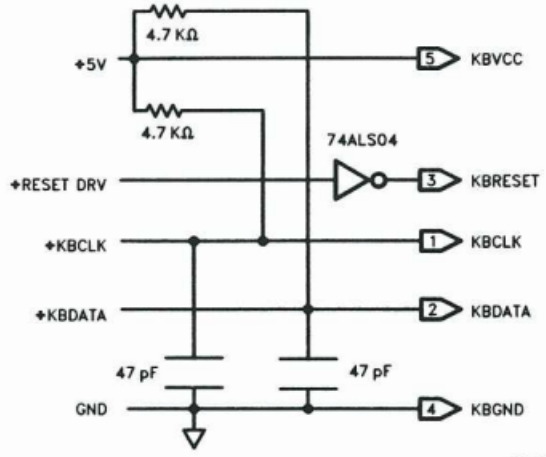
Keyboard Section Schematic



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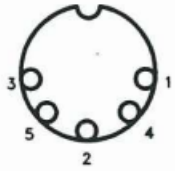
Front View



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DIN Socket
PCB Mount

4.4 I/O Map

Address	I/O Resource
00 – 0F	DMA Controller
010 – 01F	Reserved
020 – 021	Interrupt Controller
022 – 03F	Reserved
040 – 043	Timer
044 – 05F	Reserved
060	Keyboard Data Register
061	Control Register 0
062	Control Register 1
063	Control Register 2
064 – 06F	Reserved
070 – 07F	Unused
081 – 083	DMA Page Registers
084 – 09F	Reserved
0A0	NMI Mask Register
0A1 – 0FF	Reserved

The I/O space is decoded to be compatible with the IBM PC I/O decoding scheme. This means that the upper 6 address lines are not used in decoding the I/O address. To further clarify this, the address of the NMI Mask Register is located at XXXX XX00 1010 0000 binary. X indicates a "don't care" condition.

4.5 Keyboard Data Register

The Keyboard Data Register is a read only register that is used to read data from the keyboard. When a character is in the Keyboard Data Register, interrupt 1 will be sent to the Interrupt Controller. The Keyboard Data Register may be cleared by setting bit 7 of Control Register 0.

4.6 DMA Page Registers

The Page Registers are write only registers used to generate address bits 16 – 19 during a DMA transfer.

Address	Page Register
81	DMA Channel 2
82	DMA Channel 3
83	DMA Channel 1

Data Bit	Usage
0	Address Bit 16
1	Address Bit 17
2	Address Bit 18
3	Address Bit 19

4.7 NMI Mask Register

The NMI Mask Register (I/O Address 0A0H) is used to enable the NMI to the CPU.

Data Bit	Usage
0 – 6	Unused
7	1 = Enable NMI

4.8 Control Registers

Control Register 0 (I/O Address 061H) READ/ WRITE

Data Bit	Function
0	Timer 2 Gate
1	Enable Speaker
2*	Switch Select
3*	Not Used
4	Disable Parity Check
5	Disable I/O Check
6	Enable Keyboard Clock
7	Clear Keyboard Data Register

*Bits 2 and 3 are swapped when compared to the standard IBM PC architecture.

Control Register 1 (I/O Address 062H) WRITE

Data Bit	Function
0	Not Used
1	8087 Installed
2	On Board Memory Size
3	On Board Memory Size
4	Not Used
5	Not Used
6	Number of Floppies
7	Number of Floppies

Control Register 1 (I/O Address 062H) READ (Switch Select = 0)

Data Bit	Function
0	VID0
1	VID1
2	Control Register 1 Bit 6
3	Control Register 1 Bit 7
4	Timer 2 Output
5	Timer 2 Output
6	I/O Check
7	Parity Check

Control Register 1 (I/O Address 062H) READ (Switch Select = 1)

Data Bit	Function
0	Control Register 1 Bit 0
1	Control Register 1 Bit 1
2	Control Register 1 Bit 2
3	Control Register 1 Bit 3
4	Timer 2 Output
5	Timer 2 Output
6	I/O Check
7	Parity Check

Control Register 2 (I/O address 063H) WRITE ONLY

Data Bit	Function
0	Disable Parity Checker
1	Enable 8087 NMI
2	On Board RAM Size (bit 0)
3	Lock Control Register 2
4	On Board RAM Size (bit 1)
5	Fast Mode (0 RAM wait states)
6	7.15 MHz
7**	9.54 MHz

Wildcard-88 module requires data bit 0 to always be a one. Data bit 1 must always be zero when no 8087 is present and data bit 1 must always be a one when 8087 is present.

Setting Control Register 2 data bit 3 locks data bits 0–4 and locks Control Register 1. The Wildcard-88™ module must be reset in order to re-set the lock bit in Control Register 2.

On Board RAM size refers to the number of banks of memory supported by the Wildcard-88™ based DRAM controller.

CR2 Bit 4	CR2 Bit 2	Memory Banks	On Board Ram size
0	1	1	256K
1	0	2	512K
0	0	3	640K

Control Register 2 (CR2)

CR2 Bit 7	CR2 Bit 6	CR2 Bit 5	CPU Speed (MHz)	Wait States I/O	Wait States Memory On Board	Wait States Memory Bus
0	0	X	4.77	1	0	0
0	1	0	7.15	4	0	2
0	1	1	7.15	4	0	0
1	1	0**	9.54	6	0	4
1	1	1**	9.54	6	0	0

**Configuration for Wildcard-88-10™ and Wildcard-88-10N™ modules only.

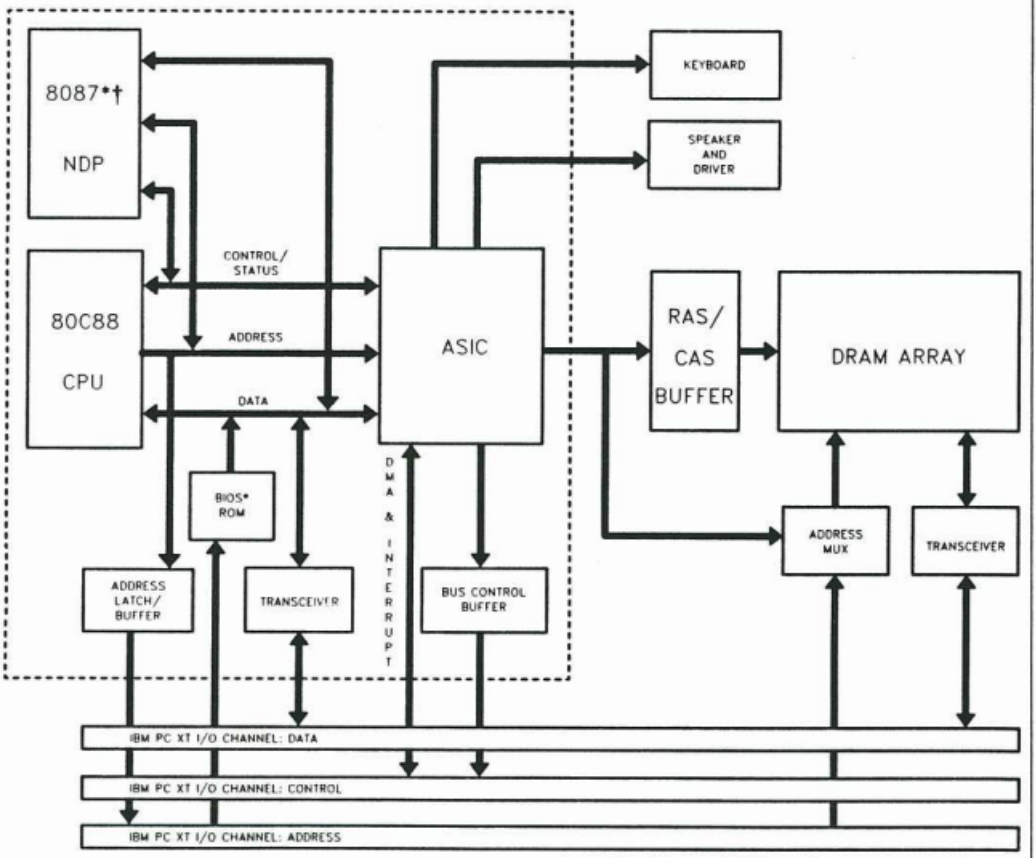
4.9 Counter/Timer Control

The timer section of the Wildcard-88 module is similar in design to the Intel 8235 Programmable Interval Timer. The timer inputs are internally connected to a 1.19 MHz clock and the outputs are appropriately connected to configure the timer for the PC/XT architecture. Channel 0 is used by the system to provide a real time clock to interrupt 0. Channel 1 is directly connected to the DMA channel 0 request line and provides timing for the Dynamic RAM refresh. An I/O read from port 41H turns refresh on and an I/O write to port 43H selecting counter 1 turns refresh off. The channel 2 output is connected to the SPKR signal and provides tone generation.

The timer may be programmed in the same manner as the 8253. It should be noted, however, that the modes of the timer defined above are hardwired in the component and can not be changed. The timer has four registers located at I/O addresses 40H to 43H.

5.0 DESIGNING WITH WILDCARD-88™ MODULE

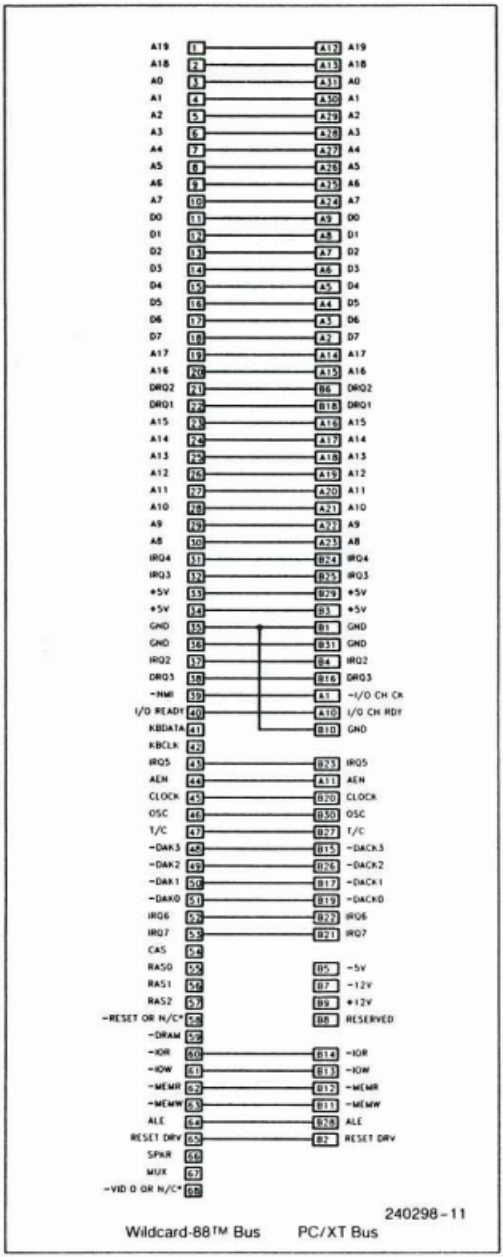
5.1 PC System Block Diagram



NOTE:
*Devices not included, sockets only.
†Socket option offered on Wildcard-88-N™ and Wildcard-88-10N™ modules only.
Wildcard-88™ modules contained within dotted area.

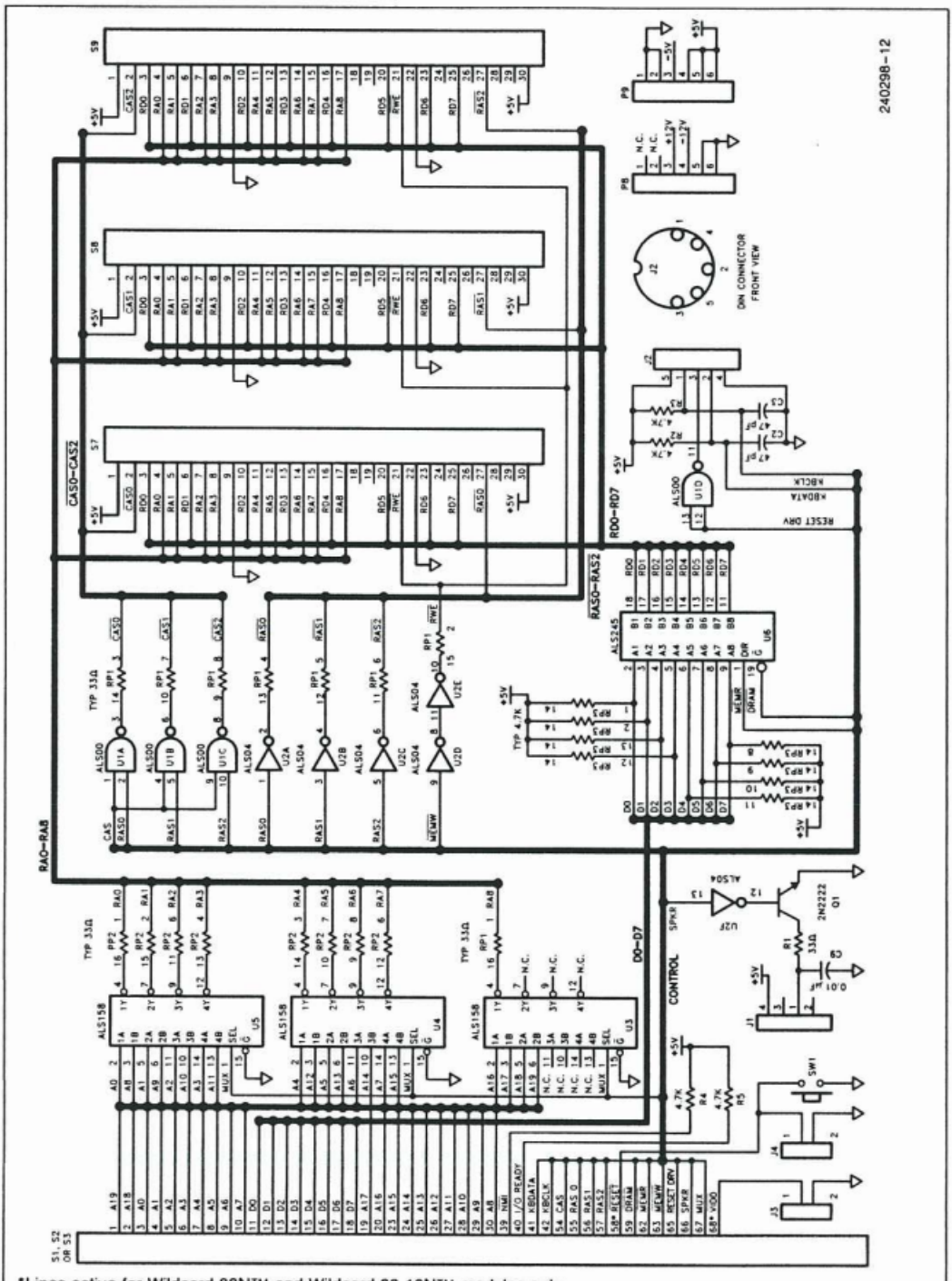
5.2 Typical PC System Design

The following two diagrams, Wildcard-88™ Bus To PC/XT Bus Translation and Wildcard-88™ Evaluation Board Schematic, represent a typical PC system design.



Wildcard-88™ Bus to PC/XT Bus Translation

The following diagram is a schematic of an evaluation board that can be used for Wildcard-88™ module prototype development. The Wildcard-88™ Evaluation Board is a backplane that provides Wildcard connectors, XT expansion slots, keyboard connector, power connectors, and SIMM memory connectors. The evaluation board also provides the logic that is required to interface the Wildcard-88™ module to DRAM. The evaluation board requires 256K x 8, 120 ns DRAM modules. The evaluation board allows immediate on target development with the addition of standard PC system peripherals and a power supply.



Wildcard-88™ Evaluation Board Schematic

6.0 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings

Ambient Temperature Under Bias	5 - 45 degrees C
Storage Temperature	0 – 70 degrees C
Supply Voltage (VDD)	5.25 Volts
Voltage on Input Pin with Respect to Ground	0V – (VDD + .3V)
Voltage on Output Pin with Respect to Ground	0V – (VDD + .3V)

6.2 D.C. Characteristics

Test Conditions: (V_{DD} = 5V ±5%, T_A = 5°C–45°C)

Current Consumption (All Values Listed in mA)

Freq (MHz)	Wildcard-88™ Module		Module + 8087	
	Max	Typ	Max	Typ
4.77	250	185	725	485
7.15	270	200	745	505
9.54	290	220	765	525

Typical data based on Wildcard-88™ Evaluation Board, 768K System DRAM, BIOS in a 2764A-2, a mono-graphics card, a floppy disk, and a keyboard.

Capacitance (f_C = 1 MHz)	
Input Pin Capacitance	15 pF
I/O Pin Capacitance	15 pF
Capacitive Drive (Outputs)	50 pF

7.0 MECHANICAL SPECIFICATIONS

7.1 Mounting Holes [Wildcard-88N™ and -10N™]

The Wildcard-88™ module provides two additional mounting holes at both top corners of the board. The size of the hole is .125" DIA. and the clearance for a screw and a bracket is .275" × .275". It is recommended to use a screw and/or a bracket in either one or both holes as an additional precaution against shock and vibration.

7.2 Shock Test Result

The Wildcard-88 module passes [redacted] requirement for shock test. The test was performed by applying a 50 G acceleration on each axis (both + and – directions) of a sample. The sample was placed in a standard socket and mounted to a fixture using the two button mounting holes.

Molex 68-pin 15-82-0168 High Density SIMM socket and AMP 68-pin 821824-7 Micro-Edge SIMM socket pass Intel mechanical impact of shock test specification:

Pulse Duration	11.0 + / – 1.0 milliseconds
Type of Pulse	half sinusoidal waveform
Gravity	50 G
Number of Shocks	+, –, each axis, 18 shocks total

7.3 Physical Clearance

In order to provide for compatible Wildcard-88 module family derivations. Designers are asked to leave spacing for a part which is 1.100" in width (.550" each side of center). Future derivations may utilize the backside of the card and require the full 1.100" allowance.

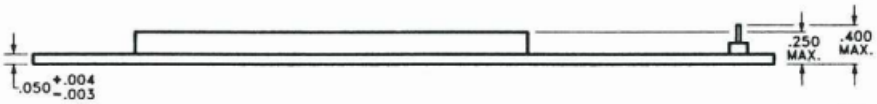
7.4 Weight

Weight: (without EPROM and/or 8087 NDP)

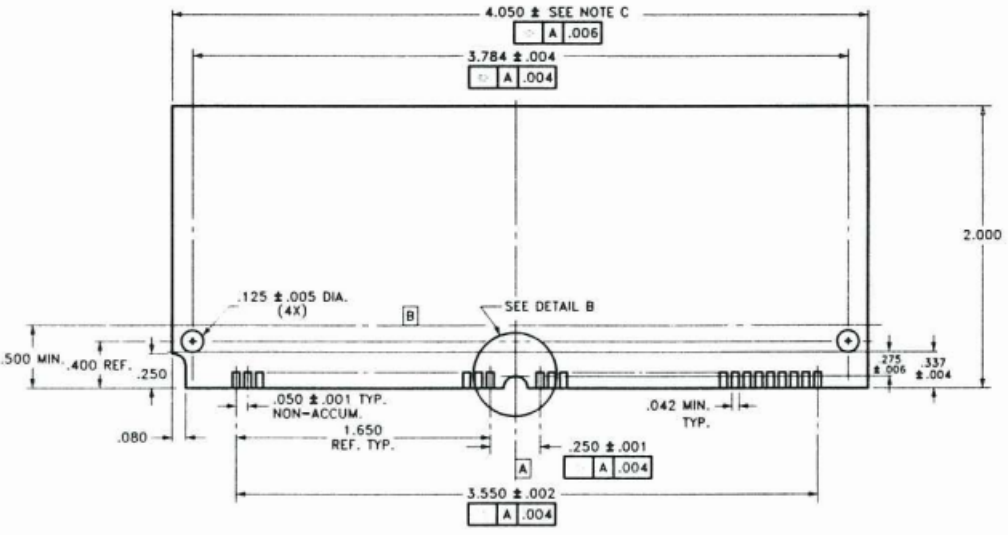
Wildcard-88™	0.8 oz
Wildcard-88-10™	0.8 oz
Wildcard-88-N™	0.9 oz
Wildcard-88-10N™	0.9 oz

7.5 Wildcard-88™ Detailed FAB Drawing

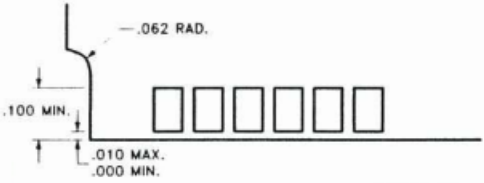
Wildcard-88™ and 88-10™ Module



240298-13

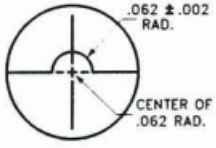


240298-14



240298-15

Connector Contact Detail



240298-16

Detail B

All Dimensions in Inches

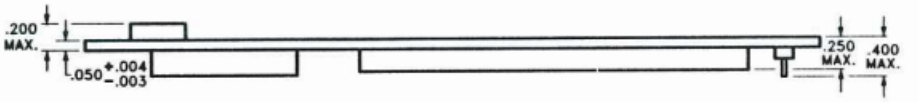
Materials:	0.047 Fiberglass, Natural
Plating:	Tin
Layers:	2
Tolerances:	.xxx 0.010
Scale:	Not to Scale
Misc.	Chamfer all Edges
Solder Mask:	Both Sides, Clear
Legend:	Chip On Board Side White Epoxy 8 pt. Helvetica
Max Warpage:	0.010 Bow

Note C: Tolerance below the B Datum line is ±0.005. Tolerance above the B Datum line is ±0.020.

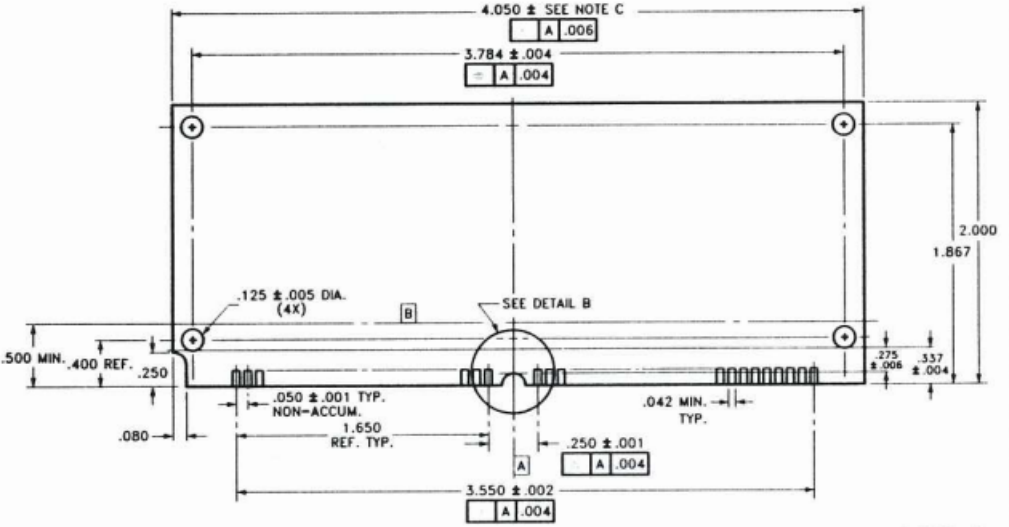
The A flag refers to tolerance with respect to the center line of the P.C. board. Half of the tolerance is to be applied to either end of the dimension.

7.5 Wildcard-88™ Detailed FAB Drawing (Continued)

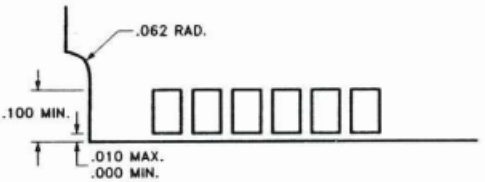
Wildcard-88N™ or 88-10N™ Module



240298-18

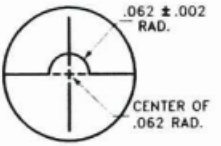


240298-19



240298-20

Connector Contact Detail



240298-21

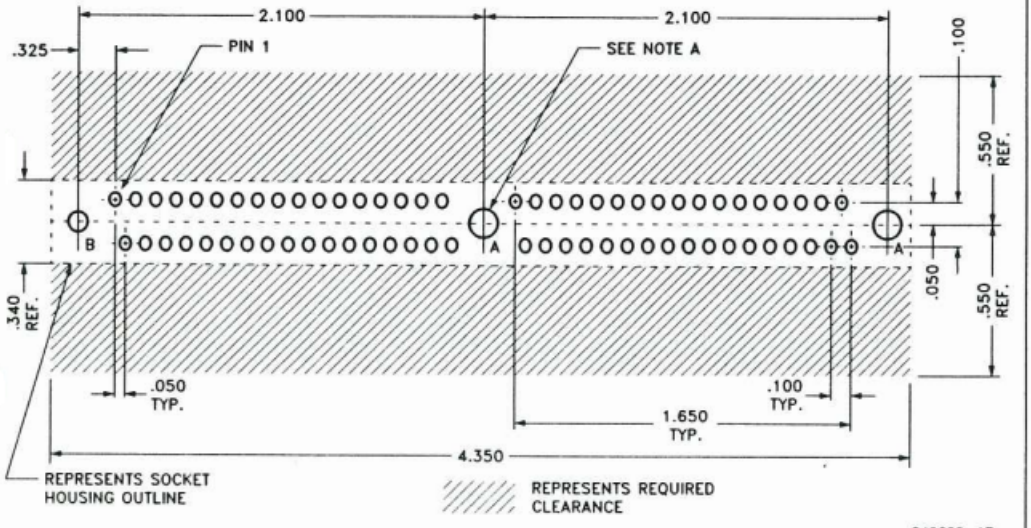
Detail B

All Dimensions in Inches

Materials:	0.047 Fiberglass, Natural
Plating:	Tin
Layers:	2
Tolerances:	.xxx 0.010
Scale:	Not to Scale
Misc.	Chamfer all Edges
Solder Mask:	Both Sides, Clear
Legend:	Chip On Board Side White Epoxy 8 pt. Helvetica
Max Warpage:	0.010 Bow

Note C: Tolerance below the B Datum line is ±0.005. Tolerance above the B Datum line is ±0.020.

The A flag refers to tolerance with respect to the center line of the P.C. board. Half of the tolerance is to be applied to either end of the dimension.



Note A: Not required for some sockets
All dimensions ±0.003.

Hole Sizes
A = 0.093 (0.096 for Burndy)
B = 0.062 (0.080 for Burndy)
Others = 0.040

Wildcard 88™ Connector Footprint

7.6 Connector Footprint and Drawings

The Wildcard-88™ module is designed to mate with the following connectors. This is not a recommendation to use these specific vendors.

Vendor	Part Number	Description
Molex	15-82-0168	High Density SIMM Socket
AMP	821824-7	Micro-Edge SIMM Socket
Burndy	SIME68PS-5TW1	Memory-Mate SIMM Socket

8.0 Environmental Specifications

The module complies with the following environmental specifications:

Operating Temperature	5 – 45 degrees C
Non-Operating Temperature	0 – 70 degrees C
Humidity	20% – 80%