

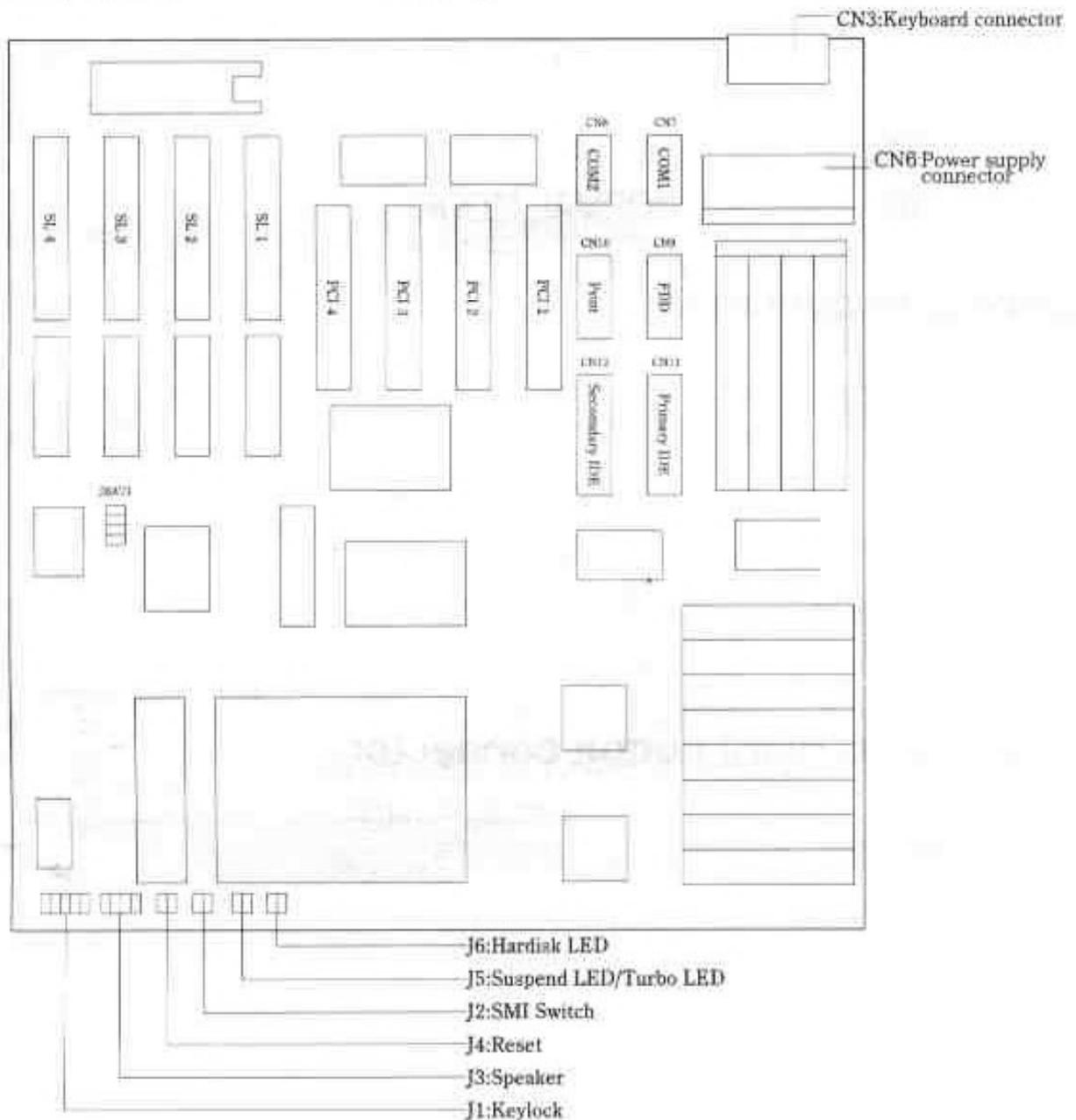
## 1-2 SPECIFICATION

- \* 64 bit P54C,Pentium ,K86(K5),and M1 interface
- \* 3.3 v or 5v CPU and cache interface
- \* support CPU external write-back cache
- \* Cyrix M1 linear burst and cache to cache transfer (DP) support
- \* On board cache memoery size support for 256/512/1024k
- \* interleaved SRAM access
- \* Direct map write back or write through secondary cache
- \* On board memory expandable to 256 MB,Using Mixed 256k/512k/1M/2M/4M/8M/16M\*N DRAMs
- \* 2 bank, 4 \*72 pin SIMM socket,any bank can be single /double side support
- \* 8 expansion slot : 4 ISA solts(16bit) + 4 PCI soft
- \* 2 on board Enhanced IDE(32bit) + 1 on board FDD(8bit) interface
- \* On board 2 serial(com1,com2) + 1 parallel(print) port
- \* Legal AWARD BIOS
- \* Real time clock & Keyboard controller: Internal within VT82C416MV
- \* Power Management Unit including the APM Mechanism and SMI(system management interrupt)
- \* Chipset : VT82C575MV System controller  
VT82C576MV PCI controller  
VT82C577MV data controller  
VT82C416MV Integrated ISA BUS controller  
W83787,W83758 ISA I/O controller

# CHAPTER 2 INSTALLATION

## 2-1 CONNECTORS

J1:Power LED & Keylock connector	SL1-SL4:ISA Slot	CN8:COM2
J2:SMI Switch connector	PCI1-PCI4:PCI Slot	CN9:Floppy Disk connector
J3:Speaker connector	JBAT1:Battery connector	CN10:Print
J4:Hardware reset button connector	CN3:Keyboard connector	CN11:Primary IDE
J5:Suspend LED / Turbo LED connector	CN6:Power supply connector	CN12:Secondary IDE
J6:Hard Disk LED connector	CN7:COM1	



## **J5:Suspend LED / Turbo LED connector**

PINOUT	ASSIGNMENTS
1	LED OUTPUT
2	GROUND

## **J6:Hard Disk LED connector**

PINOUT	ASSIGNMENTS
1	LED OUTPUT
2	GROUND

## **SL1-SL4:ISA Solt**

Please refer section 4-3 for information relating

PCI1-PCI4:PCI Solt

Please refer section 4-3 for information relating

## **JBAT1:Battery connector**

PINOUT	ASSIGNMENTS
1	EXTERNAL BATTERY INPUT
2	ON BOARD RECHARGEABLE BATTERY
3	DISCHARGE PIN
4	GROUND

## 2-2 JUMPER

JCK1-3: System clock selection  
 JCLK:

JP1-JP2: CPU frequency Fraction/Ratio

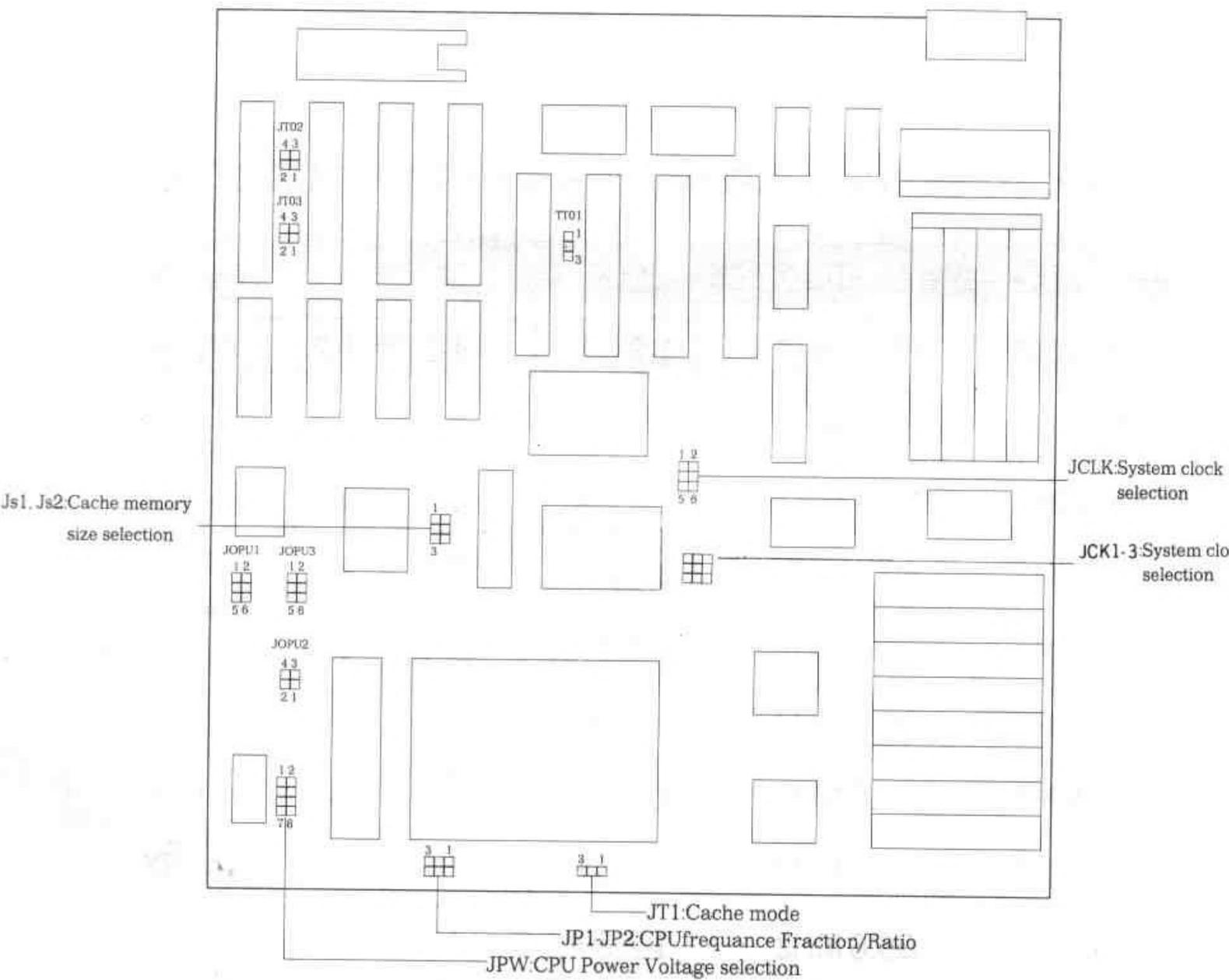
JPW: CPU Power Voltage selection

JCPU1-JCPU3: CPU type selection

JT1: Cache mode

JS1-JS2: Cache memory size selection

JIO1-JIO3: FOR ECP mode



**JCLK: System clock selection & JP1-JP2: CPU frequency  
Fraction/Ratio**

JCLK JUMPER	Frequency	JP1	JP2	CPU	Fraction/Ratio
1-2	50 MHZ	1-2	1-2	1.5X	
1-2,5-6	60 MHZ	2-3	1-2	2X	
1-2,3-4,5-6	66.6MHZ	1-2	2-3	3X	
3-4,5-6	80 MHZ	2-3	2-3	2.5X	

**QUICK TO SETTING CPU CLOCK & SYSTEM BUS CLOCK**

CPU CLOCK	SYSTEM BUS CLOCK	JCLK	JP1	JP2	Fraction/Ratio
75 MHZ	50 MHZ	1-2	1-2	1-2	1.5X
90 MHZ	60 MHZ	1-2,5-6	1-2	1-2	1.5X
100 MHZ	66.6 MHZ	1-2,3-4,5-6	1-2	1-2	1.5X
120 MHZ	60 MHZ	1-2,5-6	2-3	1-2	2X
133 MHZ	66.6 MHZ	1-2,3-4,5-6	2-3	1-2	2X
150 MHZ	60 MHZ	1-2,5-6	2-3	2-3	2.5X
166 MHZ	66.6 MHZ	1-2,3-4,5-6	2-3	2-3	2.5X
180 MHZ	60 MHZ	1-2,5-6	1-2	2-3	3X
200 MHZ	66.6 MHZ	1-2,3-4,5-6	1-2	2-3	3X

## JCK1-3: System clock selection & JP1-JP2: CPU frequency Fraction/Ratio

JCK3	JCK2	JCK1	Frequency	JP1	JP2	CPU Fraction/Ratio
2-3	1-2	2-3	50 MHZ	1-2	1-2	1.5X
1-2	1-2	1-2	60 MHZ	2-3	1-2	2X
1-2	2-3	2-3	66.6 MHZ	1-2	2-3	3X

## QUICK TO SETTING CPU CLOCK & SYSTEM BUS CLOCK

CPU CLOCK	SYSTEM BUS CLOCK	JCK3	JCK2	JCK1	JP1	JP2	Fraction/Ratio
75 MHZ	50 MHZ	2-3	1-2	2-3	1-2	1-2	1.5X
90 MHZ	60 MHZ	1-2	1-2	1-2	1-2	1-2	1.5X
100 MHZ	66.6 MHZ	1-2	2-3	2-3	1-2	1-2	1.5X
120 MHZ	60 MHZ	1-2	1-2	1-2	2-3	1-2	2X
133 MHZ	66.6 MHZ	1-2	2-3	2-3	2-3	1-2	2X
150 MHZ	60 MHZ	1-2	1-2	1-2	2-3	2-3	2.5X
166 MHZ	66.6 MHZ	1-2	2-3	2-3	2-3	2-3	2.5X
180 MHZ	60 MHZ	1-2	1-2	1-2	1-2	2-3	3X
200 MHZ	66.6 MHZ	1-2	2-3	2-3	1-2	2-3	3X

JPW	CPU Power Voltage
1-2	4.0V
3-4	3.6V
5-6	3.45V
7-8	3.3V

### JCPU1-JCPU3:CPU type selection

CPU TYPE	JCPU1	JCPU2	JCPU3
P54C - 1	1-3,2-4	OPEN	1-3,2-4
P54C - 2	1-3,2-4	3-4	3-5,4-6
P55C	3-5,4-6	1-2	1-3,2-4
P55CT	OPEN	OPEN	1-3,2-4

### JT1:Cache mode

JT1	CACHE MODE
1-2	Write-Back
2-3	Write-Through

CACHE SIZE	1024K	512K	256K
DATA SRAM	128K*8	64K*8	32K*8
TAG SRAM	32K*8	16K*8 or 32K*8	8K*8 or 32K*8
JS1	2-3	1-2	1-2
JS2	2-3	2-3	1-2

### JIO1-JIO3:FOR ECP mode

JTO1 : PRINT	
JIO1	PRINT
1-2	IRQ7
2-3	IRQ5

JTO2 : PDRQ		JTO3 : PDACK		STATE
JIO2	DRQ	JIO3	PDACK	DMA
1-3	DRQ1	1-3	ACK1	DMA 1
2-4	DRQ3	2-4	ACK3	DMA 3

## 2-3 MEMORY INSTALLATION

1. This board supports up to 2 banks of DRAM with size up to 256 MByte and Mixed 256K/512K/1M/2M/4M/8M/16M\*N DRAM.
2. We can supports single modules DRAM on the SIM4 location
3. Normal and EDO DRAM support in a flexible /mixed combination
4. Single /Double density 72 pin (\*36) SIMM module support
5. The memory configuration is as follows:

BANK 0		BANK 1		TOTAL
SIM4	SIM3	SIM2	SIM1	MEMORY
1M				1M
1M	1M			2M
		1M	1M	2M
4M				4M
1M	1M	1M	1M	4M
4M	4M			8M
		4M	4M	8M
16M				16M
16M	16M			32M
		16M	16M	32M
32M				32M
16M	16M	16M	16M	64M

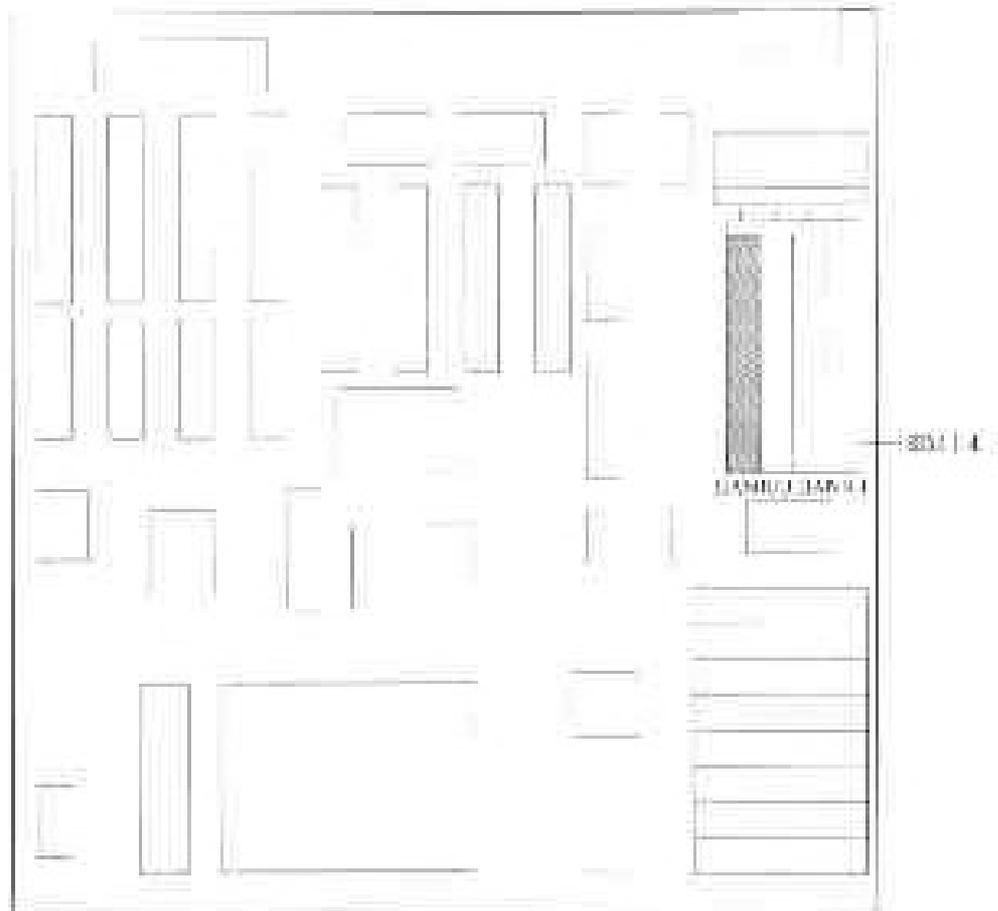
32M	32M			64M
64M		32M	32M	64M
64M	64M			128M
		64M	64M	128M
64M	64M	64M	64M	256M

# WARNING!

FOR VT82C51MM PCI/ISA MODE VER2.0  
 DON'T SUPPORT SINGLE MODULES!

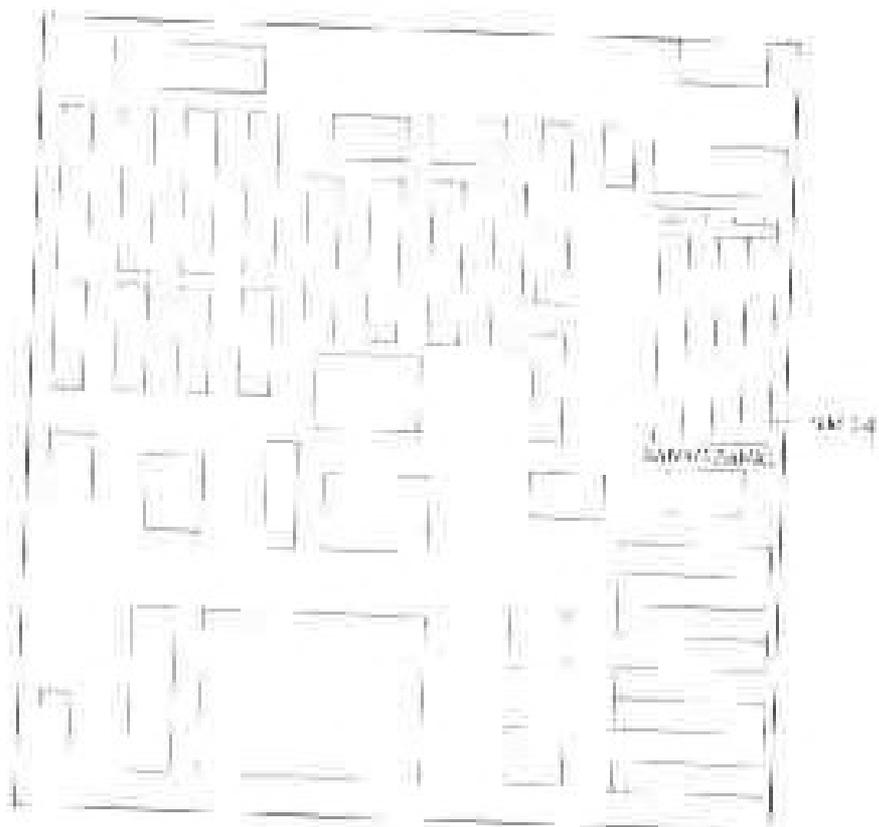
if you install single modules DRAM ,location and memory size are as follows:

BANK 0		BANK 1		TOTAL
SIM4	SIM3	SIM2	SIM1	MEMORY
1M				1M
4M				4M
8M				8M
16M				16M
32M				32M
64M				64M
128M				128M



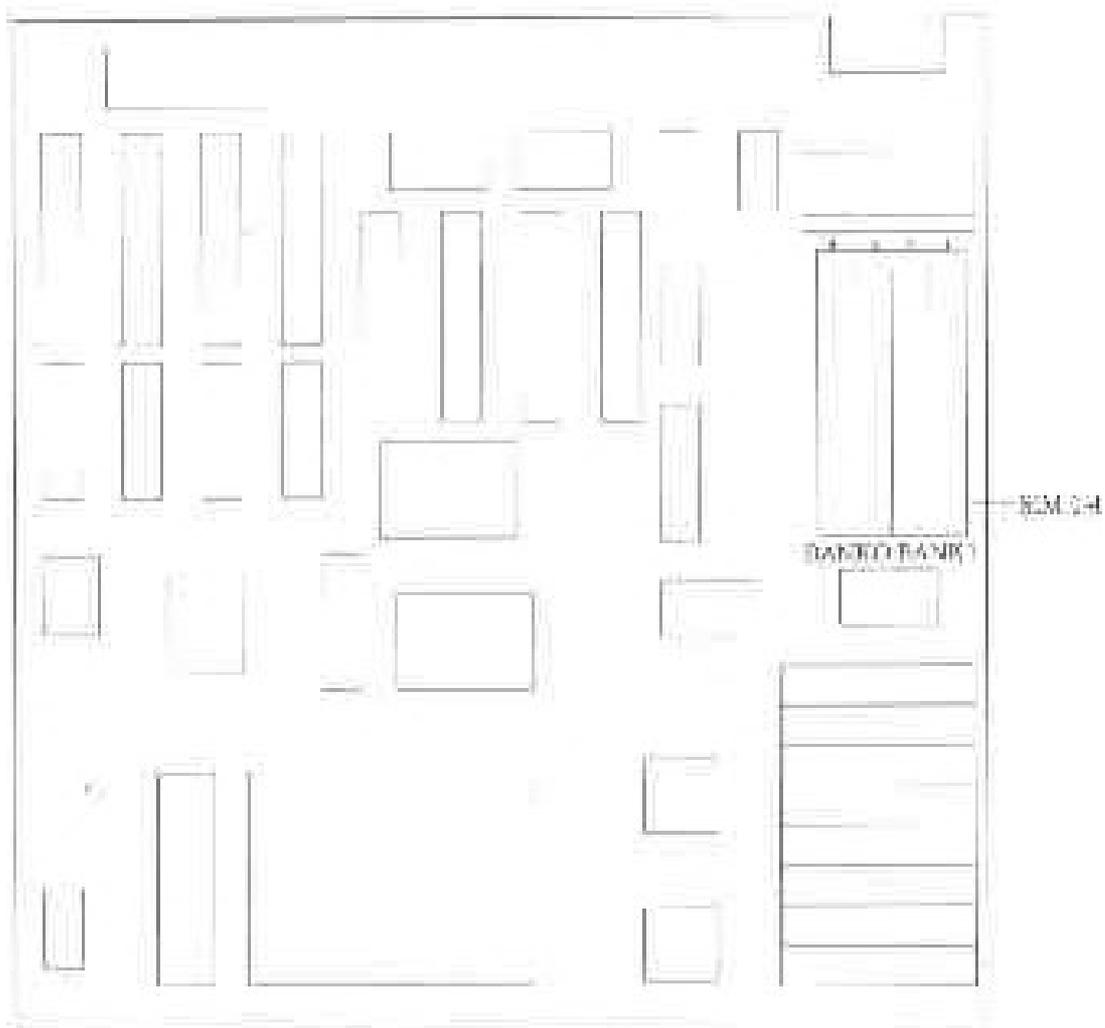
if you install one bank DRAM , location and memory size are as follows:

BANK 0		BANK 1		TOTAL
SIM4	SIM3	SIM2	SIM1	MEMORY
1M	1M			2M
		1M	1M	2M
4M	4M			8M
		4M	4M	8M
8M	8M			16M
		8M	8M	16M
16M	16M			32M
		16M	16M	32M
32M	32M			64M
		32M	32M	64M
64M	64M			128M
		64M	64M	128M



if you install two bank DRAM ,location and memory size are as follows:

BANK 0		BANK1		TOTAL
SIM4	SIM3	SIM2	SIM1	MEMORY
1M	1M	1M	1M	4M
4M	4M	4M	4M	16M
8M	8M	8M	8M	32M
16M	16M	16M	16M	64M
32M	32M	32M	32M	128M
64M	64M	64M	64M	256M



## 2-4 CACHE MEMORY INSTALLATION AND JUMPER SETTING

### 2-4-1 Cache Memory Installation

The VT5065 main board accept optional 256k,512k or 1024k of SRAM for cache memory support.

The table below lists all the possible SRAM location and the total of cache RAM memory amount for each option.

TYPE	DATA RAM	TAG RAM	TOTAL
Option	M6,M7,M8,M9 & M2,M3,M4,M5	M1	Cache size
1	32K*8	8K*8 or 32K*8	256K
2	64K*8	16K*8 or 32K*8	512K
3	128K*8	32K*8	1024K

### JS1~JS2:Cache memory size selection

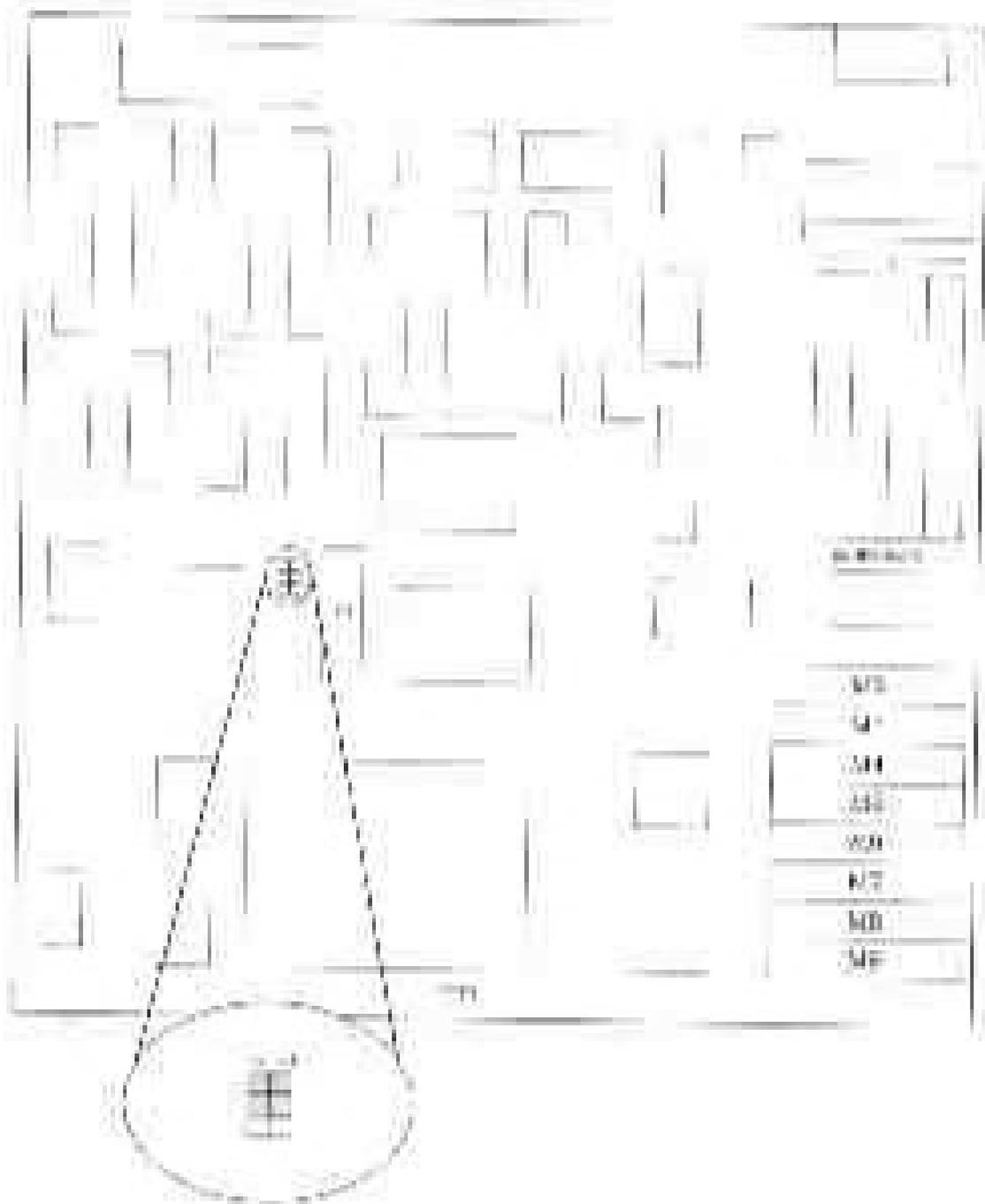
CACHE SIZE	1024K	512K	256K
DATA SRAM	128K*8	64K*8	32K*8
TAG SRAM	32K*8	16K*8 or 32K*8	8K*8 or 32K*8
JS1	2-3	1-2	1-2
JS2	2-3	2-3	1-2

### JT1:Cache mode

JT1	CACHE MODE
1-2	Write-Back
2-3	Write-Through

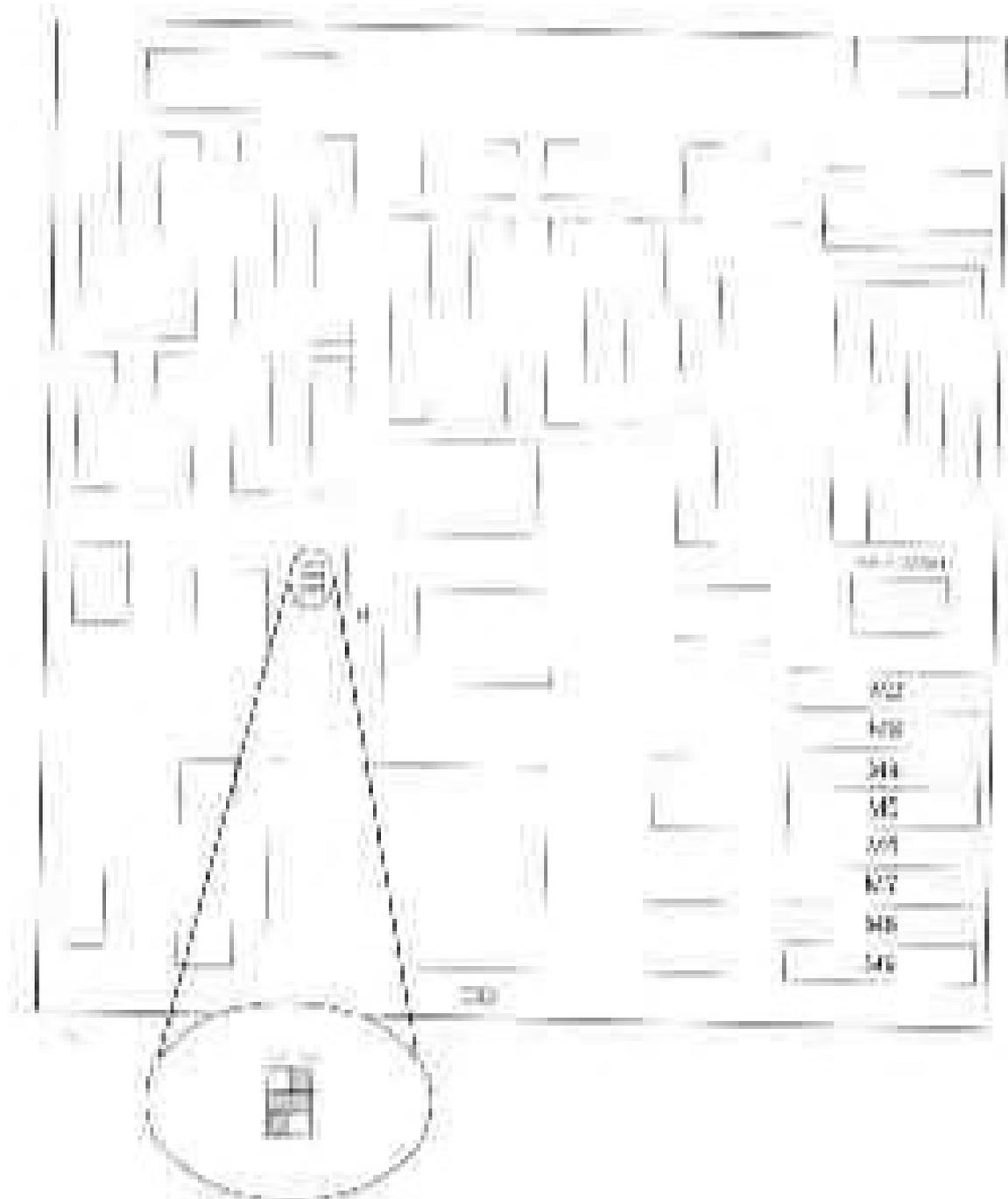
## 2-4-2 Installation of 256KB Cache Memory and one 8k\*8 or 32k\*8 TAG RAM

Installation of the 256kb cache memory is as shown in the diagram below. install one 8k\*8 bit SRAM at M1 and eight 32k\*8 bit SRAM at M2-M9. Jumper setting as cache memory size table shown as section 2-4.



### 2-4-3 Installation of 512KB Cache Memory and one 16\*8 or 32k\*8 TAG RAM

Installation of the 258kb cache memory is as shown in the diagram below. Install one 32k\*8 bit SRAM at M1 and eight 128k\*8 bit SRAM at M2-M9. Jumper setting as cache memory size table shown as section 2-4



## 2-4-4 Installation of 1024KB Cache Memory and one 32k\*8 TAG RAM

Installation of the 258kb cache memory is as shown in the diagram below. Install one 32k\*8 bit SRAM at M1 and eight 128k\*8 bit SRAM at M2-M9. Jumper setting as cache memory size table shown as section 2-4

