

**VLSI-5 16MHz  
Zero-Wait Half 286  
MAIN BOARD  
USER'S MANUAL**

## **TABLE OF CONTENTS:**

### **FEATURES**

I.	INSTALLATION.....	P- 3
	0. Mother Board.....	P- 3
	1. Power Supply.....	P- 5
	2. Display.....	P- 6
	3. Keyboard.....	P- 6
	4. FDD/HDD.....	P- 6
	5. Setup.....	P- 7
II.	SYSTEM MEMORY MAP.....	P- 8
III.	I/O ADDRESS MAP.....	P- 9
IV.	SYSTEM TIMERS.....	P-10
V.	SYSTEM INTERRUPTS.....	P-11
VI.	SYSTEM DMA.....	P-12
VII.	REAL TIME CLOCK AND NONVOLATILE RAM.....	P-13
VIII.	CHIP SET INFORMATION.....	P-14

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## **FEATURES:**

- \* Four layer implementation for low noise operation.
- \* 5 VLSI chip set full low power consumption CMOS.
- \* 8/16MHz CPU clock speed.
- \* 0/1 Wait State memory write operations.
- \* 0/1 wait state memory read operations.
- \* 4 Mega bytes memory on board use SIMM and /or DIP RAM mixedly.
- \* 32K (27128x2) or 64K (27256x2) ROM BIOS.
- \* 80287 socket.
- \* CMOS clock and calendar.
- \* Ni-Cd Rechargeable battery on board and external battery connector.
- \* 16-Level interrupts.
- \* 7-channel Direct Memory Access (DMA).
- \* 3 programmable timers.
- \* 4 16-bit slots and 2 8-bit slots for I/O expansion.

## I. INSTALLATION

### Other Hardware Requirements:

- DRAM 640K bytes or more.
- Power supply
- Display card (Monochrome, Color, EGA or VGA) and monitor.
- Keyboard, AT.
- FDD and /or HDD controller and FDD/HDD.

### Software Requirement:

- Disk Operating System (DOS).

### PROCEDURES:

#### 0. MOTHER BOARD -

Both 256K/1M RAM Module (SIMM) and 44256/4464 RAM can be mixed used. That is, if bank 0 use DIP RAM, bank 1 can use DIP RAM or RAM Module, and vice versa.

#### JUMPER SETTING AND CONNECTOR

J3 Turbo LED

J4 Reset Connector

J5 Speaker

J6 1,2 ON: Parity Enable  
2,3 ON: Parity Disable

J9 Turbo Switch  
ON : Turbo Mode  
OFF: Normal Mode

**J10 Power LED & Keylock Connector**

Pin 1 LED +  
2 Key  
3 LED -  
4 Keylock  
5 GND

**J16 ON : REMAP Enable  
OFF: REMAP Disable**

J17	J19	J18	Total RAM
ON	ON	ON	TEST MODE
ON	ON	OFF	512K
ON	OFF	ON	1M (640K)
ON	OFF	OFF	2M
OFF	ON	ON	TEST MODE
OFF	ON	OFF	2M
OFF	OFF	ON	4M

**J20 ON : ROM 2 WAIT STATES  
OFF: ROM 3 WAIT STATES**

**J21 RAM WRITE WAIT STATES  
ON : 0 WAIT STATE  
OFF: 1 WAIT STATE**

**J25 EXTERNAL BATTERY CONNECTOR**

Pin 1: PLUS POLE  
2: KEY  
3: GND  
4: GND

**J26 ON : Enable Internal Battery  
OFF: Disable Internal Battery**

**J27 ROM SIZE  
ON : 27256  
OFF: 27128**

**J28 ON : Color Display  
OFF: Monochrome Display**

J32 RAM READ Wait State  
ON : 0 Wait State  
OFF: 1 Wait State

J33 IOCHRDY SIGNAL QUALICATION  
1,2 ON Normal Operation  
2,3 ON If 1,2 ON cause some ADDON  
cards Erroneous operation, let pin 2,3  
ON.

J38 Power Connector  
PIN 1 Power Good (Orange)  
2 +5V (Red)  
3 +12V (Yellow)  
4 -12V (Blue)  
5 Ground (Black)  
6 Ground  
7 Ground  
8 Ground  
9 -5V (White)  
10 +5V (Red)  
11 +5V  
12 +5V

J39 Keyboard Connector  
Pin 1 Keyboard clock  
2 Keyboard Data  
3 Not Used  
4 Ground

1. POWER SUPPLY - Make sure the power supply input voltage match with the wall outlets voltage (110V or 220V), and the switch is off, plug the power cord one end into the power supply and one end into the wall outlets.

Connect two power cables to power connector, make sure black wires on two cables come close. (reference the power connector J1).

2. DISPLAY - Insert display card on any slot, usually on the most left slot. Connect monitor signal cable to display card and power cable to power outlets on the back of power supply or other available power outlets.
3. KEYBOARD - Plug the keyboard cable into the keyboard connector. If the keyboard is XT/AT switchable, check the switch on the back of keyboard if it is on correct position.
4. FDD/HDD - Insert FDD/HDD controller on any 16-bit slot (usually most right 16-bit slot).

There are one 34-pin flat cable for FDD, one 34-pin and one 20-pin flat cables for HDD and/or another 20-pin flat cable for second HDD.

Connect cables' one end on the control card's pin headers respectively (cable with red or blue on one side is pin 1). Connect cables' another end to the FDD and HDD(s).

There are two connectors on both 34-pin flat cable for two drivers each. Use outer one for driver 1 and inner one for driver 2. Connect cables' another end to edge connectors of drivers (pin 1 is coles to etch side of edge connectors). On the FDD and HDD, check that the drive select jumper is on position 1 (among 0,1,2,3)

5. **SETUP** - System configuration is stored on nonvolatile RAM and backed up by battery.

Setup program is stored in ROM BIOS and includes: Date, Time, FDD, HDD Display Keyboard and Shadow memory.

If any loss of the battery power, setup information will lose, resetup is necessary.

To enter setup program, when power on press <Del> key as the display showed, do as the instruction to complete setup.

## II. SYSTEM MEMORY MAP

<u>ADDRESS RANGE</u>	<u>START - END</u>	<u>FUNCTION</u>
000000-03FFFF	000K- 256K	System memory (256K)
040000-07FFFF	256K- 512K	System memory (256K)
080000-09FFFF	512K- 640K	System memory (128K)
0AFFFF-0BFFFF	640K- 768K	Display card buffer (128K)
0C0000-0DFFFF	768K- 896K	Expansion ROM (128K)
0E0000-0EFFFF	896K- 960K	System usage (64K)
0F0000-0FFFFF	960K- 1024K	BIOS (64K)
100000-3FFFFFFF	1024K- 4096K	Expansion RAM (3072K)

### III. I/O ADDRESS MAP

<u>Addr. Range</u>	<u>Function</u>
000-01F	DMA controller 1
020-03F	Interrupt controller 1
040-05F	Timer
060-06F	8042 (keyboard)
070-07F	Real time clock, NMI mask
080-08F	DMA page register
0A0-0BF	Interrupt controller 2
0C0-0DF	DMA controller 2
0F0	Clear 80287 Math Coprocessor busy
0F1	Reset 80287 Math Coprocessor
0F8-0FF	80287 Math Coprocessor
1F0-1F8	Hard disk
200-20F	Game I/O
278-27F	Parallel printer port 2
2F8-2FF	Serial port 2
300-31F	Prototype card
360-36F	Reserved
378-37F	Parallel printer port 1
380-38F	SDLC, bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome display/printer port 0
3C0-3CF	Reserved
3D0-3DF	Color/Graphics display
3F0-3F7	Floppy diskette controller
3F8-3FF	Serial port 1

#### **IV. SYSTEM TIMERS**

The system has three programmable timer/counters. These are channels 0 through 2, defined as follows:

Channel 0: System timer with 1.19MHz clock input and generate IRQ to interrupt controller.

Channel 1: Refresh Generator with 1.19MHz and generate a 15 us period signal.

Channel 2: Speaker tone Generator with 1.19 MHz clock input and output to drive speaker.

## V. SYSTEM INTERRUPTS

IRQ 0	Timer output 0
IRQ 1	Keyboard (Output buffer full)
IRQ 2	Cascaded Interrupt from Interrupt controller 2
IRQ 3	Serial port 2 (COM2)
IRQ 4	Serial port 1 (COM1)
IRQ 5	Parallel port 2 (LPT2)
IRQ 6	Floppy disk controller
IRQ 7	Parallel port 1 (LPT1)
IRQ 8	Real time clock
IRQ 9	Software redirected t INT 0AH
IRQ 10	Reserved
IRQ 11	Reserved
IRQ 12	Reserved
IRQ 13	80287
IRQ 14	Hard disk controller
IRQ 15	Reserved

## **VI. SYSTEM DMA**

Ch 0 - Spare  
Ch 1 - SDLC  
Ch 2 - Floppy disk  
Ch 3 - Spare  
Ch 4 - Cascade for DMA controller 1  
Ch 5 - Spare  
Ch 6 - Spare  
Ch 7 - Spare

## VII. REAL TIME CLOCK AND NONVOLATILE RAM

The real time also includes 64 bytes of RAM backedup by battery. The internal clock uses 14 bytes while the rest is allocated to system configuration (seyup).

<u>ADDRESS</u>	<u>DESCRIPTION</u>
00	Seconds
01	Second alarm
02	Minutes
03	Minutes alarm
04	Hours
05	Hours alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown
10	Diskette drive type byte - driver A and B
11	Reserved
12	Fixed disk type byte - driver C and D
13	Reserved
14	Equipment byte
15	Low base memory
16	High base memory
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2 byte CMOS checksum
30	Low expansion memory byte
31	High expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-3F	Reserved

## VIII. CHIP SET INFORMATION

### 82C100 PERIPHERAL CONTROLLER

- 84 pin PLCC package
- 7 DMA channels (8237 x 2)
- 14 external interrupt requests (8257 x 2)
- 3 timer/counter (8254)

### 82C201 SYSTEM CONTROLLER

The 82C201 replaces an 82284 clock controller and 82288 bus controller, an 8284 clock generator, two PAL16L8 (memory decoders).

### 82C202 MEMORY CONTROLLER

- 84pin PLCC package
- Generates row and column decodes to support DRAM
- Support from 512K to 8M system RAM
- Generates chip select for ROM and RAM
- Drives the system's speaker
- Supports 384K shadow BIOS and display

### 82C203 ADDRESS BUFFER

- 84 pin PLCC package
- 17 bigirection system bus drivers with 24mA sinking (60 LS loads)
- 16 bidirection peripheral bus driver with 8mA sinking
- Refresh support 256K-bit and 1M-bit DRAMS

### 82C204 DATA BUFFER

- 68 pin PLCC package
- 16 bidirection system data bus drivers with 24mA of sinking
- 8 bidirectional peripheral bus drivers with 8mA of sinking

