ECS UM4980 Ver 1.1 (should work on Ver 2.1)

Settings below are for the AMD 5x86 133mhz Processor with Write
Back cache enabled.

Set voltage to 3.45 per MTL Manual.
Set bus speed to desired, 33mhz default again per MTL Manual.
Set the following jumpers as below.

JP14: 1-2 , 3-4
JP15: 1-2 , 3-4
JP16: 1-2
JP17: 3-4
JP18: 1-2 , 4-5
JP19: 1-2 , 3-4

This was tested with the Award BIOS on the motherboard's TRW
page. I see no reason why it wouldn't work with the Phoenix BIOS.
NOTE: In the Advanced Settings where you adjust memory timing,
you will see "Write Through" selected and will be unable to
change it.
Boot into DOS and run CTCM.EXE to verify cache functionality. My
personal motherboard also reports the cache incorrectly in the
Post display.
This too shows correct in CTCM.

Below are some of the traces from that jumper block to the UM8498
and UM8496 chipset.

HITM# is pin A-12: JP17, pin 4
WB/WT# is pin B-13:JP18, pin 4
INV   is pin A-10: JP19, pin 4

JumperPin 3Pin 4Pin5
JP17:3: UM8498F-#2 & UM8496F-#184: A12cpu-HITM#5: +5v,10kOhm
JP18: 3: JP14-Pin 1 & UM8498F-#214: B13cpu-WB/WT#5: +5v, 0Ohm
JP19:3: UM8498F-#1434: A10cpu-INV 5: +5v, 0Ohm