

TI-168
OPERATION
MANUAL

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--- CHAPTER-1 GENERAL DESCRIPTION ---

1.1 DESCRIPTION

The AT mother board fits horizontally in the base of the system unit and is approximately 22 by 26cm(9 by 10.6inches). It is a4-layer printed circuit board(PCB). The DC power and a signal from the switching power supply enter the system board through two 12-pin connectors. Other connectors on the board are for attaching the keyboard, speaker, keylock, battery, H/W speed switch and reset button.

IBM PC/AT compatible

- O CHIPS SET : T.I. TACT82301, TACT82302, TACT82303
- O SPEED : 6/12MHz, 0/1 Wait State, Change 6/12MHz by S/W,
H/W, Change 0/1 wait state by H/W
- O CPU : 80286-10/12
- O DRAM : 1MB/4MB On Boards
 - a. 44256-10 DIP
 - b. 41256-10 or 411000-10 SIMM
- O ROM : 32K Byte read-only memory (ROM) subsystem, expandable to 64KB
- O INTERRUPT : 16-Level Interrupt
- O DMA : 7-Channel Direct Memory Access
- O TIMER : 3 Channels TIMER for sound and clock

Speaker attachment

CMOS memory (RAM) to maintain system configuration
3.6V rechargable battery backup for CMOS configuration table and Real-Time Clock

Keyboard attachment

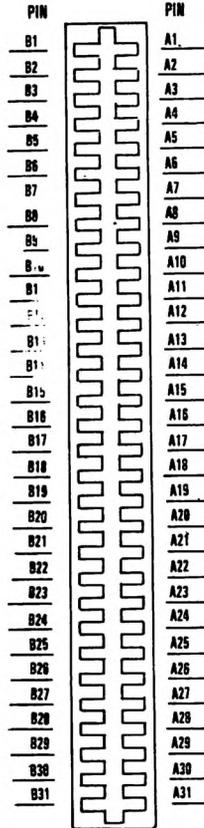
8 Input/Output (I/O) slots:

- 5 with a 36-pin and a 62-pin card-edge socket
- 3 with only the 62-pin card-edge socket

Suitable BIOS: AMI, Award, Phonenix.

Socket for 80287 (-10) mathematical co-processor

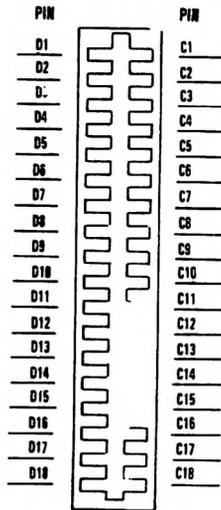
The following figure shows the pin numbering for I/O channel connectors SLOT 1 through SLOT 8



COMPONENT SIDE

I/O CHANNEL PIN NUMBERING (SLOT 1 - SLOT 9)

The following figure shows the pin numbering for I/O Channel connectors SLOT 9 through SLOT 13



COMPONENT SIDE
I/O CHANNEL PIN NUMBERING (SLOT 9 - SLOT 13)

The following figure summarize pin assignment for the I/O channel connectors.

I/O PIN	SIGNAL NAME	I/O
A1	-IOCHECK	IN
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	-IOCHRDY	IN
A11	AEN	I/O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O
A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

I/O CHANNEL (A-SIDE, SLOT 1 THROUGH SLOT 8)

I/O PIN	SIGNAL NAME	I/O
B1	GND	GROUND
B2	RESET DRV	0
B3	+5 Vdc	POWER
B4	IRQ 9	1
B5	-5 Vdc	POWER
B6	DRQ 2	1
B7	-12 Vdc	POWER
B8	OWS	1
B9	+12 Vdc	POWER
B10	GND	GROUND
B11	-SMEMW	0
B12	-SMEMR	0
B13	-10W	I/O
B14	-10R	I/O
B15	-DACK 3	OUT
B16	DRQ3	IN
B17	-DACK 1	OUT
B18	DRQ1	IN
B19	-REFRESH	I/O
B20	CLK	OUT
B21	IRQ 7	IN
B22	IRQ 6	IN
B23	IRQ 5	IN
B24	IRQ 4	IN
B25	IRQ 3	IN
B26	-DACK 2	OUT
B27	T/C	OUT
B28	BALE	OUT
B29	+5 Vdc	POWER
B30	OSC	OUT
B31	GND	GROUND

I/O CHANNEL (B-SIDE, SLOT 1 THROUGH SLOT 8)

I/O PIN	SIGNAL NAME	I/O
C1	SBHE	I/O
C2	IA23	I/O
C3	IA22	I/O
C4	IA21	I/O
C5	IA20	I/O
C6	IA19	I/O
C7	IA18	I/O
C8	IA17	I/O
C9	-MEMR	I/O
C10	-MEMW	I/O
C11	SD08	I/O
C12	SD09	I/O
C13	SD10	I/O
C14	SD11	I/O
C15	SD12	I/O
C16	SD13	I/O
C17	SD14	I/O
C18	SD15	I/O

I/O CHANNEL (C-SIDE, SLOT 9 THROUGH SLOT 13)

I/O PIN	SIGNAL NAME	I/O
D1	-MEMCS16	IN
D2	-I/OCS16	IN
D3	IRQ10	IN
D4	IRQ11	IN
D5	IRQ12	IN
D6	IRQ13	IN
D7	IRQ14	IN
D8	-DACK0	OUT
D9	DRQ0	IN
D10	-DACK5	OUT
D11	DRQ5	IN
D12	-DACK6	OUT
D13	DRQ6	IN
D14	-DACK7	OUT
D15	DRQ7	IN
D16	+5 Vdc	POWER
D17	-MASTER	IN
D18	GND	GROUND

I/O CHANNEL (D-SIDE, SLOT 9 THROUGH SLOT 13)

1.5 I/O CHANNEL SIGNAL DESCRIPTION

The following is a description of the system board's I/O channel signals. All signal lines are TTL-compatible. I/O adapters should be designed with a maximum of two low-power Shottkey (IS) loads per line.

SA0 through SA19 (I/O)

Address bits 0 through 19 are used to address memory and I/O devices within the system. These 20 address lines, in addition to IA17 through IA23, allow access of up to 16MB of memory. SA0 through SA19 are gated on the system bus when "BALE". These signals are generated by the microprocessor or DMA controller. They also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

IA17 through IA23 (I/O)

These signals (unlatched) are used to address memory and I/O devices within the system. They give the system up to 16MB of addressability. These signals are valid when "BALE" is high. IA17 through IA23 are not latched during microprocessor cycles and therefore do not stay valid for the whole cycle. Their purpose is to generate memory decodes for 1 wait-state memory cycles. These decodes should be latched by I/O adapters on the falling edge of "BALE". These signals also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

CLK(O)

This is the 6MHz system clock. It is a synchronous microprocessor cycle clock with a cycle time of 167 or 83 nanoseconds. The clock has a 50% duty cycle. This signal should only be used for synchronization. It is not intended for uses requiring a fixed frequency.

RESET DRV (O)

"Reset drive" is used to reset or initialize system logic at power-up time or during a low line-voltage outage. This signal is active high.

SD0 through SD15 (I/O)

These signals provide bus bits 0 through 15 for the microprocessor, memory, and I/O devices. SD0 is the least-significant bit. All 8-bit devices on the I/O channel should use SD0 through SD7 for communications to the microprocessor. The 16-bit devices will use SD0 through SD15. To support 8-bit devices, the data on SD8 through SD15 will be gated to SD0 through SD7 during 8-bit transfers to these devices; 16-bit microprocessor transfer to 8-bit devices will be converted to two 8-bit transfer.

BALE (O) (Buffered)

"Address latch enable" is provided by the 82288 Bus Controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. It is available to the I/O channel as an indicator of a valid microprocessor or DMA address (when used with "AEN"). Microprocessor addresses SA0 through SA19 are latched with the falling edge of "BALE". "BALE" is forced high during DMA cycles.

-I/OCHK (I)

"-I/O Channel Check" provides the system board with parity (error) information about memory or devices on the I/O channel. When this signal is active, it indicates an uncorrectable system error.

I/OCHRDY (I)

"I/O Channel Ready" is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of clock cycles (125 nanoseconds). This signal should be held low for more than 2.5 microseconds.

IRQ3-IRQ7, IRQ9-IRQ12 AND IRQ14 THRU 15 (I)

Interrupt Requests 3 thru 7, 9 thru 12 and 14 thru 15 are used to signal the microprocessor that an I/O device needs attention. The interrupt requests are prioritized, with IRQ9 thru IRQ12 and IRQ14 thru IRQ15 having the highest priority (IRQ9 is the highest) and IRQ3 thru IRQ7 having the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request (Interrupt Service Routine). Interrupt 13 is used on the system board and is not available on the I/O channel. Interrupt 8 is used for the real-time clock.

-IOR (I/O)

"-I/O Read" instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is active low.

-IOW (I/O)

"-I/O Wire" instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is active low.

-SEMER (O) -MEMR (I/O)

These signals instruct the memory devices to drive data onto the data bus. "-SEMER" is active only when the memory decode is within the low 1MB of memory space. "-MEMR" is active on all memory read cycles. "-MEMR" may be driven by any microprocessor or DMA controller in the system. "-SEMER" is driven from "-MEMR" and the decode of the low 1MB of memory. When a microprocessor on the I/O channel wishes to drive "-MEMR", it must have the address lines valid on the bus for one system lock period before driving "-MEMR" active. Both signals are active low.

DRQ0-DRQ3 AND DRQ5-DRQ7 (I)

DMA Request 0 thru 3 and 5 thru 7 are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service (or control of the system). They are prioritized, with "DRQ0" having the highest priority and "DRQ7" having the lowest. A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding "DMA Request Acknowledge" (DACK) line goes active. "DRQ0" thru "DRQ3" will perform 8-bit DMA transfers, "DRQ5" thru "DRQ7" will perform 16-bit transfers. "DRQ4" is used on the system board and is not available on the I/O channel.

-DACK0 TO -DACK3 AND -DACK5 TO -DACK7 (O)

-DMA Acknowledge 0 to 3 and 5 to 7 are used to acknowledge DMA requests (DRQ0 thru DRQ7). They are active low.

AEN (O)

"Address Enable" is used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active, the DMA controller has control of the address bus, the data-bus Read command lines (memory and I/O), and the Write command lines (memory and I/O).

-REFRESH (I/O)

This signal is used to indicate a refresh cycle and can be driven by a microprocessor on the I/O channel.

T/C (O)

"Terminal Count" provides a pulse when the terminal count for any DMA channel is reached.

SBHE (I/O)

"Bus High Enable" (system) indicates a transfer of data on the upper byte of the data bus, SD8 through SD15. Sixteen-bit devices use "SBHE" to condition data bus buffers tied to SD8 through SD15.

-MASTER (I)

This signal is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a "-DACK", an I/O microprocessor may pull "-MASTER" low, which will allow it to control the system address, data, and control lines (a condition known as tri-state). After "-MASTER" is low, the I/O microprocessor must wait one system clock period before driving the address and data lines, and two clock periods before issuing a Read or Write command. If this signal is held low for more than 15 microseconds, system memory may be lost because of a lack of refresh.

-MEMCS16 (I)

"-MEM 16 Chip Select" signals the system board if the present data transfer is a 1 wait-state, 16-bit, memory cycle. it must be derived from the decode LA17 through LA23. "-MEMCS16" should be driven with an open collector or tri-state driver capable of sinking 20mA.

I/OCS16 (I)

"I/O 16 bit Chip Select" signals the system board that the present data transfer is a 16 bit, 1 wait-state, I/O cycle. It is derived from an address decode. "-I/OCS16" is active low and should be driven with an open collector or tri-state driver capable of sinking 20mA.

OSC (O)

"Oscillator" (OSC) is a high-speed clock with a 70-nanosecond period, 14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle.

OWS (I)

The "Zero Wait State" (OWS) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16-bit device without wait cycles, "OWS" is derived from an address decode gate with a Read or Write command. In order to run a memory cycle to an 8-bit device with a minimum of two wait states, "OWS" should be driven active one system clock after the Read or Write command is active gated with the address decode for the device. Memory Read and Write commands to an 8-bit device are active on the falling edge of the system clock. "OWS" is active low and should be driven with an open collector or tri-state driver capable of sinking 20mA.

The following figure is an I/O address map

<u>HEX RANGE</u>	<u>DEVICE</u>
000-01F	DMA controller 1, 8237A-5
020-03F	Interrupt controller 1, 8259A, Master
040-05F	Timer, 8254-2
060-06F	8042 (Keyboard)
070-07F	Real-time clock, NMI (Non-Maskable interrupt) mask
080-09F	DMA page register, 74LS612
0A0-0BF	Interrupt controller 2, 8237A-5
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2
2F8-2FF	Serial Port 2
300-31F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	SDLC, Bi-synchronous 2
3A0-3AF	Bi-synchronous 1
3B0-3BF	Monochrome Display & Printer Adapter
3C0-3CF	Reserved
3D0-3DF	Color/Graphics Monitor Adapter
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1

- CHAPTER - 2 SET-UP MOTHER BOARD

- 2.1 TURBO : TURBO SWITCH
- 2.2 TURBOLED : TURBO-LED
- 2.3 RESET : HARDWARE RESET
- 2.4 SPKER : SPEAKER CONNECTOR

<u>PINOUT</u>	<u>SIGNAL NAME</u>
1	SPEAKER OUT
2	NO CONNECTOR
3	VCC
4	+5V

2.5 KEYLOCK & POWER LED CONNECTOR

<u>PINOUT</u>	<u>SIGNAL NAME</u>
1	+POWER LED
2	NO CONNECTOR
3	-POWER LED
4	KEYLOCK
5	GND

2.6 POWER CONNECTOR

<u>PINOUT</u>	<u>SIGNAL NAME</u>
1	POWER GOOD
2	+5V
3	+12V
4	-12V
5	GND
6	GND
7	GND
8	GND
9	-5V
10	+5V
11	+5V
12	+5V

2.7 JP2 : DISPLAY CARD SELECTION

Short = Color card
Open = Monochrome card

2.8 JP17: 6V EXTERNAL BATTERY BACKUP CONNECTOR

<u>PINOUT</u>	<u>SIGNAL NAME</u>
1	+6V
2	EXT BATT +4.5V
3	NO CONNECTOR
4	GND

2.9 J1 : 0 WAIT / 1 WAIT

Short : 0 wait
Open : 1 wait

2.9 J2 : 1M/256K DRAM SELECT

Short : 256K DRAM TYPE
Open : 1M DRAM TYPE

2.9 J3 : Parity Check

Short : Parity check disable
Open : Parity check enable

--CHAPTER-3 RAM BLOCK DESCRIPTION--

There are two kinds of RAM blocks of the MINI-AT main board. Each block can work independly or combined together without crossing the banks.

BLOCK 1 : Can use 256K-4bit, 64K-4bit DIP Ram

PARITY CHECH	BANK 0	BANK 1	TOTAL MEMORY
41256 X 2	44256	BLANK	512K
41256 X 2 +4164 X2	44256	4464	640K
41256 X 4	44256	44256	1024K

BLOCK 2 : Can use 256K or 1MB Simm RAM Modules

BANK 0	BANK 1	TOTAL MEMORY
256K SIMM	BLANK	512K
256K	256K	1024K
1MB	BLANK	2048K
1MB	1MB	4096K

---CHAPTER-4 BIOS SYSTEM SETUP---

THIS CHAPTER TELLS USER HOW TO USE THE BIOS SETUP UNDER THE AWARD BIOS. PLEASE DEFINITELY READ CLEARLY.

AFTER POWER-ON AND SYSTEM TESTS, PLEASE PRESS "ALT+CTL+ESC" KEYS, THE PROGRAM WILL GO ON TO TEXT SCREEN IN THE FOLLOWING.

AWARD SOFTWARE CMOS SETUP

DATE (MM/DD/YY)	6/14/90				
TIME (HH/MM/SS)	9:50:53				
DISKETTE 1	1.2M				
DISKETTE 2	NONE				
		CYLS.	HEADS	SECTORS	PRECOMP
DISK 1	2	615	4	17	300
DISK 2	NONE				
VIDEO	EGA				
BASE MEMORY	640				
EXTENDED MEMORY	384				
ERROR HALT	HALT ON ALL ERRORS				
SPEED SELECT	HIGH				

USE " " " " AND "ENTER" TO SELECT THE OPTIONS YOU WANT.

1. DATE :
TYPE THE RIGHT VALUE ACCORDING TO THE RULE IN THE LEFT PARENTHESIS.
2. TIME :
TYPE THE RIGHT VALUE ACCORDING TO THE RULE IN THE LEFT PARENTHESIS.
3. DISKETTE 1 AND DISKETTE 2 :
ONLY "NONE" 360K, 1.2M, 720K AND 1.4M CAN BE SELECTED, USE " " " " TO SELECT.
4. DISK 1 AND DISK 2 :
TYPE THE RIGHT TYPE OF THE HARD DISK OR USE " " " " TO SELECT.
THE OPTIONS CAN BE FOUND IN THE APENDIX A.
5. VIDEO :
ONLY MONO, COLOR 40, COLOR 80, AND EGA CAN BE SELECTED, USE " " " " TO SELECT. IF YOU USE A VGA OR MULTISYNC CARD, JUST SELECT EGA TYPE.
6. BASE MEMORY :
TYPE THE RIGHT MEMORY SIZE IN THE MAIN BOARD, ONLY 256, 512, AND 640 CAN BE ACCEPTED.
7. EXTENTED MEMORY :
TYPE THE RIGHT EXTENTED MEMORY SIZE IN THE MAIN BOARD, ACTUALLY YOU CAN REFER THE EXPANSION MEMORY SIZE IN THE SYSTEM TEST WHEN SYSTEM IS IN THE COLD START UP.
8. ERROR HALT :
ONLY HALT ON ALL ERRORS, NO HALT ON ANY ERRORS, NO KEYBOARD ERROR HALT, NO DISK ERROR HALT CAN BE SELECTED. USE " " " " TO SELECT.
9. SPEED SELECT :
ONLY NO CHANGE, HIGH, LOW CAN BE SELECTED. USE " " " " TO SELECT.

--- APPENDIX-A HARD DISK TABLE

TYPE	CYLIN- DERS	HEADS	PRE- COMP	LAND ZONE	SEC- TORS	SIZE MEGS
1	306	4	128	305	17	10.1
2	615	4	300	615	17	20.4
3	615	6	300	615	17	30.6
4	940	8	512	940	17	62.4
5	940	6	512	940	17	46.8
6	615	4	-1	615	17	20.4
7	462	8	256	511	17	30.6
8	733	5	-1	733	17	30.4
9	900	15	-1	901	17	112.0
10	820	3	-1	820	17	20.4
11	855	5	-1	855	17	35.4
12	855	7	-1	855	17	49.6
13	306	8	128	319	17	20.3
14	733	7	-1	733	17	42.5
16	612	4	0	663	17	20.3
17	977	5	300	977	17	40.5
18	977	7	-1	977	17	56.7
19	1024	7	512	1023	17	59.5
20	733	5	300	732	17	30.4
21	733	7	300	732	17	42.5
22	733	5	300	733	17	30.4
23	306	4	0	336	17	10.1
24	977	5	-1	976	17	40.5
25	1024	9	-1	1279	17	76.5
26	1224	7	-1	1223	17	71.1
27	1224	11	-1	1223	17	111.7
28	1224	15	-1	1223	17	152.4
29	1024	8	-1	1023	17	68.0
30	1024	11	-1	1023	17	93.5
31	918	11	-1	1023	17	83.8
32	925	9	-1	926	17	69.1
33	1024	10	-1	1023	17	85.0
34	1024	12	-1	1023	17	102.0
35	1024	13	-1	1023	17	110.5
36	1024	14	-1	1023	17	119.0
37	1024	2	-1	1023	17	17.0
38	1024	16	-1	1023	17	136.0
39	918	15	-1	1023	17	114.3
40	820	6	-1	820	17	40.8

