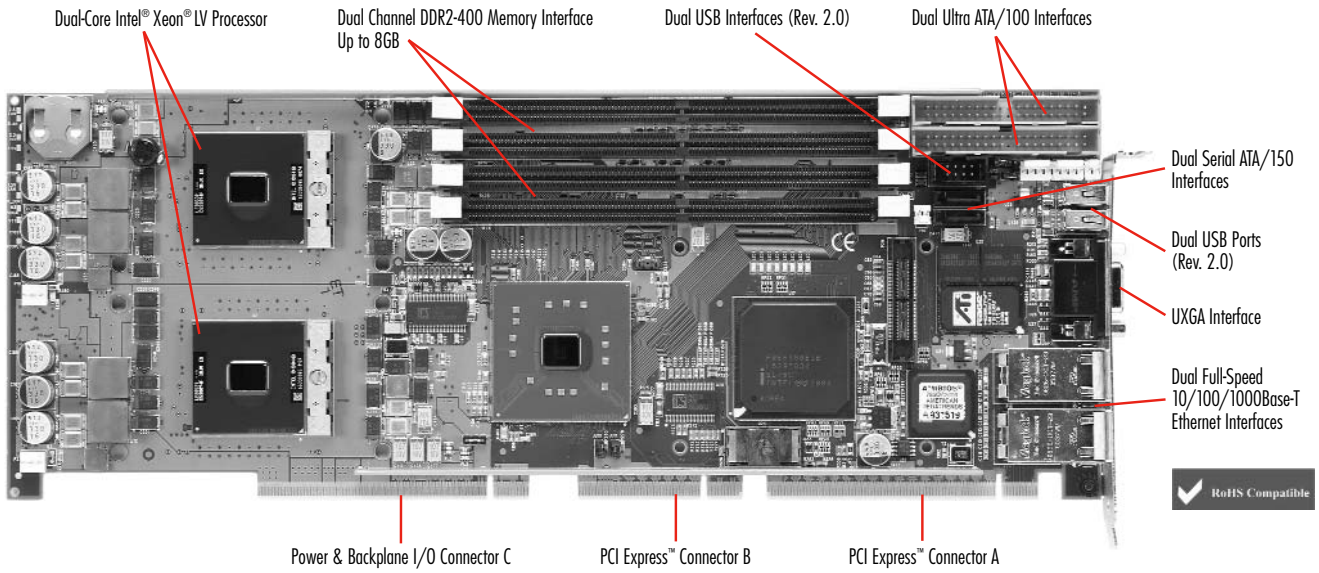
SLT

PRODUCT DATA SHEET

SLT (SHB Express™) SYSTEM HOST BOARD



Chassis Plans' SLT system host board (SHB) features two, dual-core processors that together provide four execution cores per SLT. The SLT's two Dual-Core Intel® Xeon® LV processors deliver superior processing capability and system performance using about half as much power as compared to previous generations of low voltage Intel Xeon processors. The SLT is a server-class PICMG® 1.3 SHB that supports one x4 and two x8 PCI Express links to a PICMG 1.3 backplane. An additional x4 PCIe link to a backplane is available using Chassis Plans' IOB31 expansion module. These links support PCI Express, PCI and PCI-X option cards on a PICMG 1.3 server-class backplane.

PROCESSORS:

Dual-Core Intel® Xeon® LV Processors at 1.66GHz to 2.0GHz*
Processor Package: Micro-FCPGA (478-pin)

*Higher speeds as available

The Dual-Core Intel® Xeon® LV processors on the SLT support a 667MHz system bus as well as the Intel® Chip Multi-Processing (CMP) based architecture. Intel® CMP makes dual-core functionality on each processor possible. This new architecture along with the processors' advanced power management optimizes the CPUs millions of instructions per second per watt (MIPS/Watt) specification which in turn maximizes the SLT's system performance without generating excessive heat. Other processor features include:

- Dual Core, 2MB L2 Cache
- 31W Thermal Design Power
- Enhanced Intel SpeedStep Technology (EIST)

CHIPSET:

Increased system performance is made possible by the Intel® E7520 chipset's ability to support a 667MHz system bus. The chipset configuration on Chassis Plans' SLT board supports two registered DDR2-400 memory channels. Data bottlenecks are reduced by the three PCI Express™ interfaces that provide high bandwidth (4GB/s)connections between the ports on the Memory Controller Hub (MCH) and external I/O devices or option cards.

PCI EXPRESS™ INTERFACES:

High-speed serial links that make up PCI Express(PCIe) interfaces typically have data rates twice that of PCI interfaces. A basic PCIe link consists of at least one pair of differentially driven transmit and receive signal lines. PCI Express link bandwidth is increased linearly by adding signal pairs to form multiple lanes or wider lane widths. The most common PCIe links used today are configured to have lane widths of x1, x4, x8 or x16. Chassis Plans' SLT system host board provides two x8 PCI Express links, one x4 PCI Express link and five PCIe reference clocks on edge connectors A and B. Chassis Plans' optional IOB31 module used with the SLT provides an additional x4 PCIe link to the backplane. The PCI Express links are used on PICMG 1.3 backplanes to support PCI Express option cards and bridge chips that provide PCI/PCI-X option card support. During system initialization the SLT automatically negotiates with the PCI Express cards connected to the PCIe links in order to set up communication between the devices. The net result is that the SLT system host board supports communication to x1, x4, x8, x16 PCI Express boards as well as PCI/PCI-X cards via PCI Express-to-PCI/PCI-X bridge chip technology on the backplane.

DDR2-400 MEMORY:

The DDR2-400 interface is a dual channel interface originating at the Memory Controller hub with each channel terminating at two DIMM module sockets, for a total of four memory sockets. The SLT uses ECC registered PC2-3200 DIMMs and supports a maximum memory capacity of 8GB and a minimum memory interface bandwidth of 3.2GB/s per channel. The total effective memory interface bandwidth increases to 6.4GB/s when at least one PC2-3200 DIMM is used in each memory channel.

STANDARDS:

- PCI Express™ Base Specification 1.0a
- SHB Express™ System Host Board PCI Express Specification - PCI Industrial Computer Manufacturers Group (PICMG®) 1.3

PCI EXPRESS™ CONFIGURATION AND BUS SPEEDS:

PCI Express - Edge Connectors A & B	- Two x8 links, one x4 link - Five reference clocks
PCI Express - (on-board only)	- One x4 link
PCI-X (on-board only)	- 64-bit/66MHz
PCI (on-board only)	- 32-bit/33MHz
Hub Link 1.5	- 266MB/s
System or FSB	- 667MHz

SERIAL ATA/150 PORTS (DUAL):

The primary and secondary Serial ATA (SATA) ports on the SLT boards comply with the SATA 1.0 specification and support two independent SATA storage devices such as hard disks and CD-RW devices. SATA technology provides lower-pin counts, reduced signaling voltages, simplified cabling, CRC error detection and hot-plug device support. SATA produces higher performance interfacing by providing data transfer rates up to 150MB per second on each port.

DUAL ETHERNET INTERFACES - 10/100/1000BASE-T:

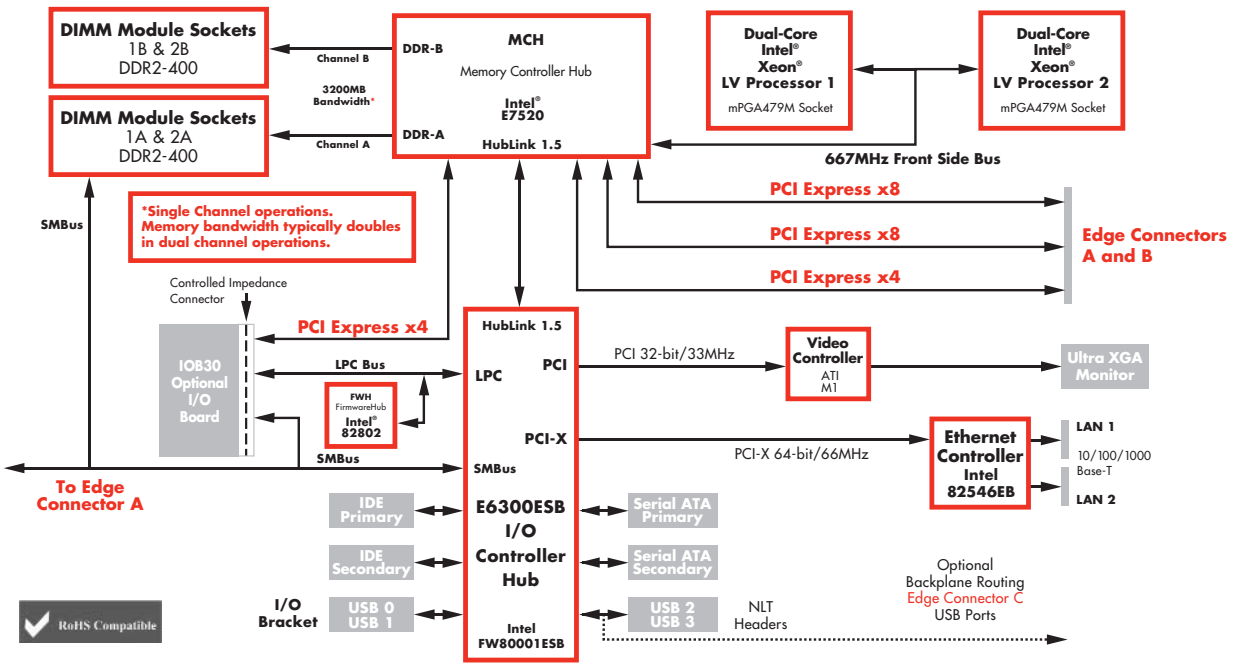
The SLT uses an internal PCI-X bus to connect the I/O Controller hub to the Ethernet controller chip. This design feature provides high-speed dual Gigabit Ethernet on LAN ports 1 and 2. The SHB also supports 10Mb/s or 100Mb/s Ethernet networks. RJ-45 connectors on the I/O bracket provide the mechanical interface to the Ethernet networks.

CHASSIS PLANS®
The Original Industrial Computer Source®

CHASSIS PLANS • 8295 Aero Place, San Diego, California, 92123 • Sales: (858) 571-4330 • Fax: (858) 571-6146
E-mail: Saleseng@chassisplans.com • Web: www.chassisplans.com

SLT

PRODUCT DATA SHEET



ULTRA XGA INTERFACE:

The SLT is equipped with the third generation ATI® RAGE™ MOBILITY™ M1 video controller. The M1 enables 2D/3D video acceleration and provides 8MB of integrated video memory. In 2D mode the video controller supports pixel resolutions up to 1600 x 1200, and in 3D mode the maximum resolution provided is 1280 x 1024. The maximum color depth supported at these extremes is 16.7 million colors. Software drivers are available for popular operating systems.

QUAD UNIVERSAL SERIAL BUS INTERFACES (USB 2.0):

Two USB 2.0 interface ports are located on the I/O bracket of the SLT. Two additional USB 2.0 headers are available on the SHB. Ask Chassis plans about optional USB routing to the backplane via SLT edge connector C.

BIOS (FLASH):

The SLT uses AMIBIOS8®; the flash BIOS resides in the SHB's Firmware Hub (FWH). AMIBIOS8 contains features such as:

- Support for flash devices for BIOS upgrading
- Integrated support for USB mass storage devices such as USB, CD-ROM, CD-RW, etc.
- Boot from network, USB mass storage devices, IDE or ATAPI
- Serial port console redirection to support headless operation (requires optional IOB30, part number 6391-000)
- SATA/ATA/ATAPI support includes 48-bit LBA addressing to support SATA/ATA/IDE hard drive capacities over 137GB

AGENCY APPROVALS:

Designed for UL60950, CAN/CSA C22.2 No. 60950-00, EN55022:1998 Class B, EN61000-4-2:1995, EN61000-4-3:1997, EN61000-4-4:1995, EN61000-4-5:1995, EN61000-4-6:1996, EN61000-4-11:1994

SLT APPLICATION CONSIDERATIONS:

Power Requirements:

Typical Values - CPU Idle State:

CPU	+5V	+12V	+3.3V
1.66GHz	3.00A	1.70A	3.00A
2.0GHz	3.00A	2.10A	3.00A

Typical Values - 100% CPU Stress State:

CPU	+5V	+12V	+3.3V
1.66GHz	3.00A	3.20A	3.25A
2.0GHz	3.00A	4.20A	3.25A

-12V @ < 100mA

Tolerance for all voltages is +/- 5% and must be applied by the PICMG 1.3 backplane to edge connector C.

Temperature/Environment:

Operating Temperature:	0Þ to 60Þ C.
Airflow Requirement:	350LFM continuous airflow when using the passive heat sink
Storage Temperature:	-40Þ to 70Þ C.
Humidity:	5% to 90% non-condensing

Mechanical:

PASSIVE COOLING SOLUTION: The SLT has a board stack-up height of .76" (1.93cm) with the SHB's passive heat sink cooling solution. Airflow of at least 350LFM must always be present across the SHB's passive heat sink.

ACTIVE COOLING SOLUTION: The SLT's optional active cooling solution has a cooling fan mounted on each CPU's heat sink resulting in a board stack-up height of 2.3" (5.84cm). Order the SLT with active cooling when 350LFM or more of continuous airflow is not available for the processors.

The overall SLT dimensions are 13.330" (33.86cm) L x 4.976" (12.64cm) H. The relative PICMG 1.3 SHB height off the backplane is the same as a PICMG 1.0 SBC due to the shorter PCI Express backplane connectors.

ADDITIONAL SLT FEATURES:

System Hardware Monitor:

- The functions monitored are:
  - Voltage: +3.3V, +/-12V, +5V and VCORE
  - Fan speed
  - Temperature

I/O Features:

- Two EIDE Ultra ATA/100 interfaces
- Optional IOB30 I/O plug-in expansion board includes:
  - Enhanced bi-directional parallel interface
  - PS/2 mouse and keyboard interface (mini DIN connector)
  - Floppy drive interface
  - Two high-speed serial ports

Watchdog Timer:

- The programmable watchdog timer is supported directly by the I/O Controller Hub. Two operating modes, free-running and one-shot, are available with this two-stage watchdog timer. Stage one can generate IRQ, SMI or SCI. Stage two generates a programmable watchdog timer reset with a total range of 1ms to 10 minutes.

ORDERING INFORMATION:

Model Name: SLT

Model #	CPU Speed	Embedded CPU
S6515-104-xM	1.66GHz	Yes
S6515-106-xM	2.0GHz	Yes

(xM = Memory)

The stated bus speed, memory and communication interface speeds are component maximums; actual system performance may vary.

CHASSIS PLANS®
The Original Industrial Computer Source®

PICMG 1.3 SYSTEMS
PCI EXPRESS

CHASSIS PLANS • 8295 Aero Place, San Diego, California, 92123 • Sales: (858) 571-4330 • Fax: (858) 571-6146
E-mail: Saleseng@chassisplans.com • Web: www.chassisplans.com

May 1, 2006