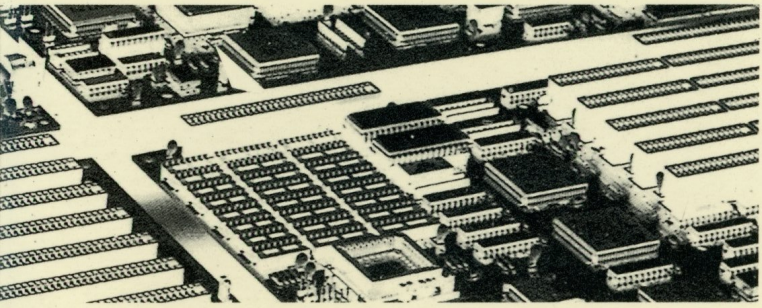
SI5PI AIO

(for Award BIOS)



USER'S MANUAL

SI5PI AIO
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(for Award BIOS)

Trademarks

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1 Introduction

The SI5PI AIO is a Pentium™ PCI Bus mainboard. It uses the SiS 85C501, 85C502, 85C503 system chipset, CMD PCI0640B PCI Bus IDE Controller, and SMC 37C665 Super I/O Controller. Other on-board specifications include 4 AT Bus slots and 4 PCI slots, 2 memory banks with memory sizes of up to 128MB, and cache sizes from 256KB to 1MB.

1.1 General Specifications

Processor:	Intel Pentium™
Chipset:	SiS 85C501 (PCI/ISA Cache Memory Controller) SiS 85C502 (PCI Local Data Buffer) SiS 85C503 (PCI System I/O) CMD PCI0640B (PCI Bus IDE Controller) SMC 37C665 (Super I/O Controller) UMC 82C865 (I/O TTL Integration)
External Cache:	256/512 KB or 1MB cache supporting write back or write-through policies
Memory Size:	2 banks of DRAM with memory size capacity of up to 128MB, all supporting double-sided SIMMs
BIOS:	Award
Slots :	Four 16-bit ISA slots Four PCI slots
Connectors:	Power Keylock & Power LED Hardware Reset Speaker Turbo LED Turbo Switch
Form Factor:	Baby-AT
PCB :	4 layers

System Chipset

SiS 85C501

- Supports Pentium™ processor at 60/66 MHz bus speed
- Integrated second level (L2) cache modes
- write-through and write-back cache modes
- direct mapped organization
- supports standard and burst SRAMs
- supports 128KB to 2MB cache sizes
- cache read/write cycle of 3-2-2-2 or 4-3-3-3 using standard SRAM at 66MHz
- Integrated DRAM controller
- supports 2MB to 128MB of cacheable main memory
- 1 level posted write buffer of 4 Qwords deep
- concurrent write back
- CAS#-before-RAS# transparent DRAM refresh
- 256K/1M/4M/16M*N 70ns fast page mode DRAM support
- programmable DRAM speed

SiS 85C502

- Three integrated posted write buffers and two read buffers increase system performance
- 1 level CPU-to-Mem posted write buffer with 4 Qwords deep
- 4 levels CPU-to-PCI posted write buffer with 4 Dwords deep
- 1 level PCI-to-Mem posted write buffer with 1 Qword deep
- 1 level Mem-to-CPU read buffer with 1 Qword deep
- 1 level Mem-to-PCI read buffer with 1 Qword deep
- Provides a 64-bit Pentium™, DRAM data bus and 32-bit PCI data bus
- Operates synchronously to the 66.7MHz CPU and 33.3MHz PCI clocks
- Provides parity generation for memory writes

SiS 85C503

- Integrated bridge between PCI Bus and ISA Bus
- translates PCI Bus cycles into ISA Bus cycles
- translates ISA master or DMA cycles into PCI Bus cycles
- provides PCI-to-ISA memory one Dword posted write buffer
- Integrated ISA Bus compatible logic
- Supports reroutability of four PCI interrupts to any unused IRQ interrupt
- Supports Flash ROM

CMD PCI0640B

- Fully compatible with the latest PCI IDE and ATAPI specifications
- The most complete 32-bit driver support in the industry (DOS, Windows 3.1 Past Disk, Windows NT, OS/2, Novell & SCO Unix 32-bit driver support)
- Programmable data transfer timing supports customized setting for 4 IDE devices
- Read-ahead and write-back buffers enhance transfer rates and allow concurrent operations
- Suitable for PCI motherboard or PCI expansion card applications
- Fully supports and surpasses enhance IDE Mode-3
- Supports program I/O function

SMC 37C665

- Super I/O controller
- Two 16C550 compatible UARTs
- One multi-mode parallel port which include EPP and ECP support

2 System Memory

SI5PI AIO accepts a minimum of 2MB and a maximum of 128MB on-board. There are two memory banks which support 256/512 KB or 1/2/4/8/16 MB 72-pin type, single- and/or double-density modules.

Important: *DRAM insertion on every bank should come in pair and of the same type. For instance, if you only have two DRAM modules, you cannot install one DRAM module in socket SIM1 and another DRAM module of the same type on SIM3. Likewise, memory type mixing is NOT allowed within a bank.*

The following table lists all the possible DRAM module combinations and the total memory amount for each option.

Bank 0		Bank 1		Total Memory Size
SIM3	SIM4	SIM1	SIM2	
256K x 36	256K x 36	None	None	2MB
256K x 36	256K x 36	256K x 36	256K x 36	4MB
512K x 36	512K x 36	None	None	4MB
512K x 36	512K x 36	512K x 36	512K x 36	8MB
1M x 36	1M x 36	None	None	8MB
1M x 36	1M x 36	1M x 36	1M x 36	16MB
2M x 36	2M x 36	None	None	16MB
512K x 36	512K x 36	2M x 36	2M x 36	20MB
2M x 36	2M x 36	2M x 36	2M x 36	32MB
4M x 36	4M x 36	None	None	32MB
512K x 36	512K x 36	4M x 36	4M x 36	36MB
1M x 36	1M x 36	4M x 36	4M x 36	40MB
2M x 36	2M x 36	4M x 36	4M x 36	48MB
4M x 36	4M x 36	4M x 36	4M x 36	64MB
8M x 36	8M x 36	None	None	64MB
2M x 36	2M x 36	8M x 36	8M x 36	80MB
8M x 36	8M x 36	8M x 36	8M x 36	128MB
16M x 36	16M x 36	None	None	128MB

Table 2-1. Memory Configurations and Requirements

Cache Memory Subsystems

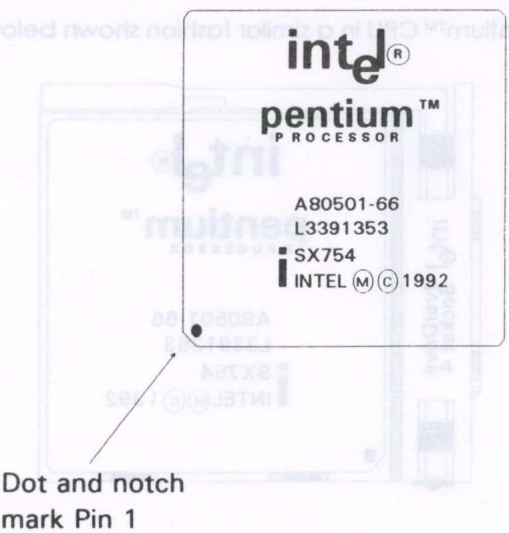
Cache Size	TAG RAM	Cache Bank0 (U34 . . . U41)	Cache Bank1 (U23 . . . U30)
256KB	8Kx8	32Kx8	None
512KB	32Kx8	32Kx8	32Kx8
512KB	32Kx8	64Kx8	None
1MB	32Kx8	64Kx8	64Kx8
1MB	32Kx8	128Kx8	None

Table 2-2. Second Level Cache Memory Configurations

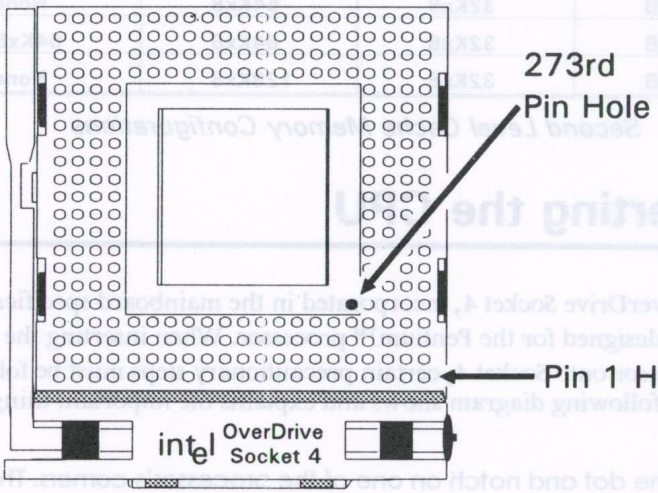
3 Inserting the CPU

The Intel OverDrive Socket 4, incorporated in the mainboard specifications, is specially designed for the Pentium™ processor. When inserting the Pentium™ processor onto Socket 4, certain precautionary steps must be followed. The following diagram shows and explains the important things to note.

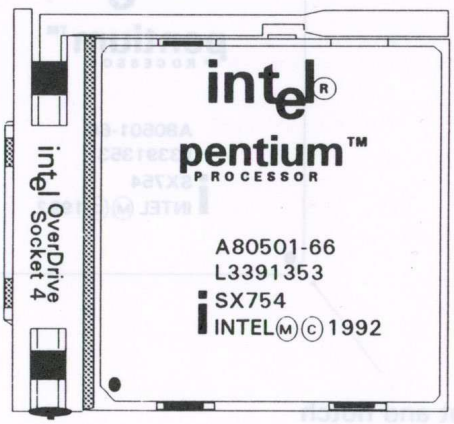
1. Locate the dot and notch on one of the processor's corners. These markings indicate Pin 1 of the processor.



2. Examine the Intel OverDrive Socket 4. The 273rd pin hole is seated at the inner portion of the socket. You will be able to easily identify this pin hole because there are no other pin holes beside it. Pin 1 of the processor is designated on the corner pin hole adjacent to that of the 273rd pin hole. Refer to the diagram on the following page for the respective indicators on the Intel OverDrive Socket 4.



3. Insert the Pentium™ CPU in a similar fashion shown below.



4 Jumper Settings and Connectors

4.1 Setting the Jumpers

The table below summarizes the functions and jumper settings on the SI5PI AIO.

Function		Jumper Settings
CPU Clock Select	60MHz (default)	**JP5** short 1-2 **JP6** short 2-3 **JP7** short 1-2
	66MHz	**JP5** short 2-3 **JP6** short 1-2 **JP7** short 2-3
CPU Signal Select	L1 Write-back	**JP19** short 1-2
	L1 Write-through	**JP19** short 2-3
	Always invalidated	**JP20** short 1-2
	Write to invalidated	**JP20** short 2-3
BIOS	Flash ROM (+12V)	**JP11** short 1-2 & 5-6
	EPROM (default)	**JP11** short 2-3 & 4-5
PCI0640B Signal Select	Enable IDE	**JP2** open
	Disable IDE	**JP2** short
On-board Multi I/O	Enabled	**JP1** short 1-2
	Disabled	**JP1** short 2-3
ECP Mode	ECP Mode Parallel Port DRQ1 DACK1 Selection	**JP9** short 2-3 **JP10** short 1-2
	ECP Mode Parallel Port DRQ3 DACK3 Selection	**JP9** short 1-2 **JP10** short 2-3
Parallel Port Mode Select	Normal Mode	**JP8** open
	ECP Mode	**JP8** short
Parallel Port IRQ Select	IRQ7	**JP21** short 1-2
	IRQ5	**JP21** short 2-3

Table 4-1. Jumper Settings (Continued . . . . .)

Function		Jumper Settings
External Cache Memory Settings	256KB (with 32Kx8 SRAMs in Bank0)	**JP13** open **JP14** open **JP15** open **JP16** short 1-2 & 3-4
	512KB (with 32Kx8 SRAMs in Banks 0&1)	**JP13** open **JP14** short **JP15** open **JP16** short 2-3 & 4-5
	512KB (with 64Kx8 SRAMs in Bank0)	**JP13** open **JP14** short **JP15** short 1-2 **JP16** short 1-2 & 3-4
	1MB (with 64Kx8 SRAMs in Banks 0&1)	**JP13** short **JP14** short **JP15** short 2-3 **JP16** short 2-3 & 4-5
	1MB (with 128Kx8 SRAMs in Bank0)	**JP13** short **JP14** short **JP15** short 1-2 & 3-4 **JP16** short 1-2 & 3-4
DRAM Configuration	2MB memory size with 256Kx36 on Bank0	**JP4** short 2-3
	4MB memory size with 256Kx36 on Bank0 and Bank1	**JP4** short 2-3
	4MB memory size with 512Kx36 on Bank0	**JP4** short 1-2, 3-4
	8MB memory size with 512Kx36 on Bank0 and Bank1	**JP4** short 1-2, 3-4
	8MB memory size with 1Mx36 on Bank0	**JP4** short 2-3
	16MB memory size with 1Mx36 on Bank0 and Bank1	**JP4** short 2-3
	16MB memory size with 2Mx36 on Bank0	**JP4** short 1-2, 3-4
	20MB memory size with 256Kx36 on Bank0 and 2Mx36 on Bank1	**JP4** short 1-2, 3-4
	32MB memory size with 2Mx36 on Bank0 and Bank1	**JP4** short 1-2, 3-4

Table 4-1. Jumper Settings (Continued . . . . .)

Function		Jumper Settings
DRAM Configuration	32MB memory size with 4Mx36 on Bank0	**JP4** short 2-3
	36MB memory size with 512Kx36 on Bank0 and 4Mx36 on Bank1	**JP4** short 1-2, 3-4
	40MB memory size with 1Mx36 on Bank0 and 4Mx36 on Bank1	**JP4** short 2-3
	48MB memory size with 2Mx36 on Bank0 and 4Mx36 on Bank1	**JP4** short 1-2, 3-4
	64MB memory size with 4Mx36 on Bank0 and Bank1	**JP4** short 2-3
	64MB memory size with 8Mx36 on Bank0	**JP4** short 1-2, 3-4
	80MB memory size with 2Mx36 on Bank0 and 8Mx36 on Bank1	**JP4** short 1-2, 3-4
	128MB memory size with 8Mx36 on Bank0 and Bank1	**JP4** short 1-2, 3-4
	128MB memory size with 16Mx36 on Bank0	**JP4** short 2-3
Parity Check Select (for SI5PI AIO PCB Rev. 1.1 only)	Enabled	**JP22** short 1-2
	Disabled	**JP22** short 2-3

Table 4-1. Jumper Settings

4.2 Connectors

There are several connectors located on the SI5PI AIO. Their functions are listed below.

Connector	Function
J1	PS/2 Keyboard Connector (optional)
J2	PS/2 Mouse Connector (optional)
J3	AT Keyboard Connector
J4	Power Connector
J5	Floppy Connector
J6	IDE Primary Connector
J7	COM1 Port Connector
J8	COM2 Port Connector
J9	Printer Port Connector
J10	IDE Secondary Connector
J11	HDD LED Connector
J12	Keylock Connector & System Power LED
J13	Speaker Connector
J14	Hardware Reset Connector
J15	Turbo LED Connector
J16	Turbo Switch

Table 4-2. Mainboard Connectors

4.3 Board Layouts

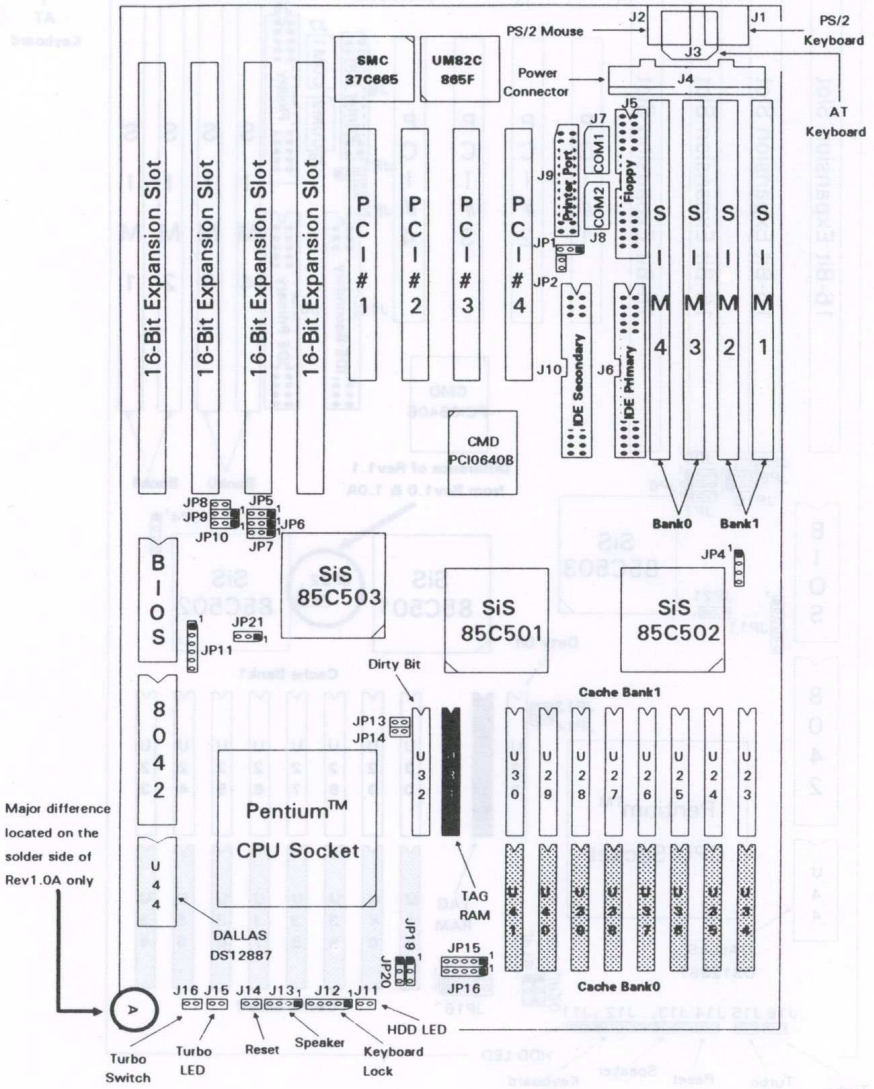


Figure 4-1. SI5PI AIO Mainboard Layout (PCB Rev. 1.0 & 1.0A)

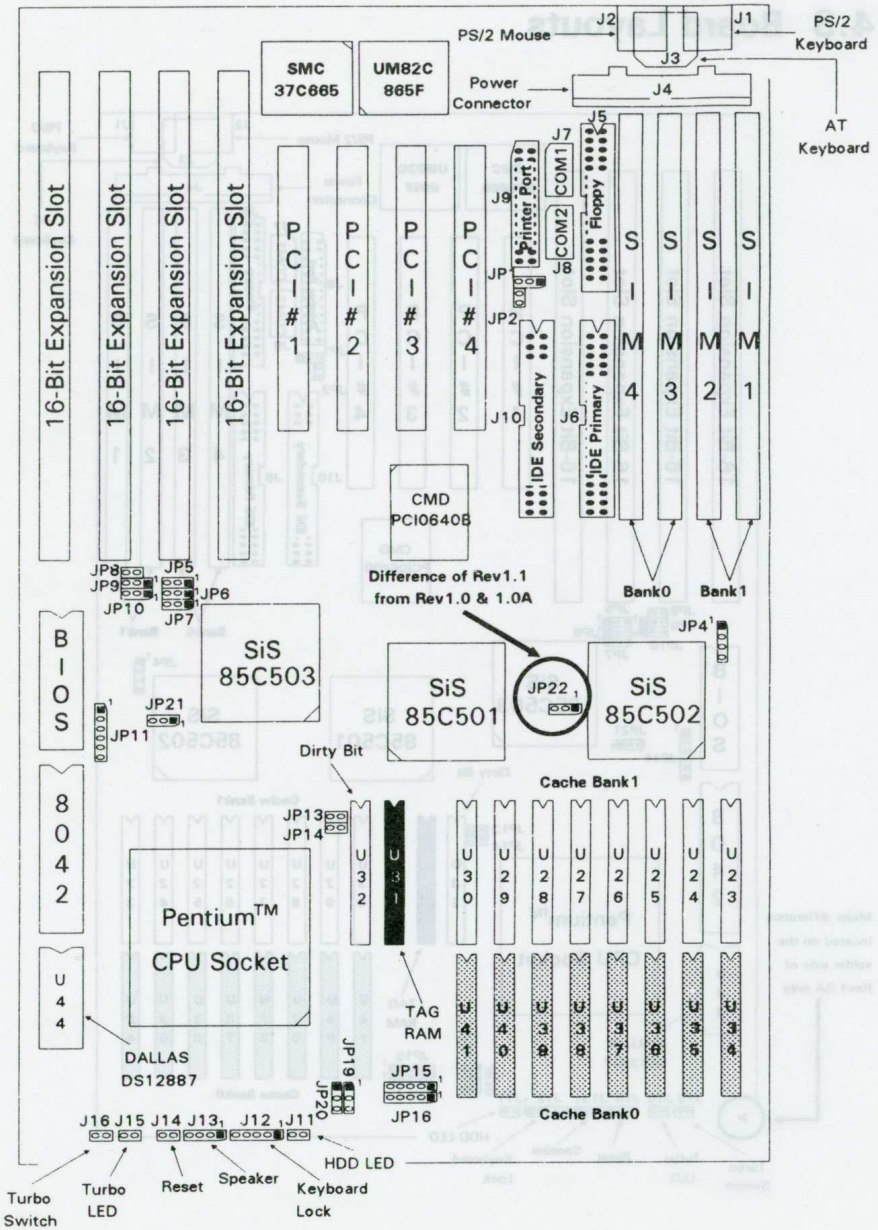


Figure 4-2. SI5PI AIO Mainboard Layout (PCB Rev. 1.1)

Distinct Characteristics of SI5PI AIO Rev1.0, Rev1.0A, and Rev1.1.

Rev 1.0: *supports the parity check function which means that **parity checking is always enabled** and there is no alternative way to turn it off. Therefore you **must** install parity DRAMs only. Installing non-parity DRAMs instead will cause parity check error.*

Rev. 1.0A: *does not support the parity check function which means that **parity check is always disabled** and there is no alternative way to turn it on. However, there are no constraints as to the type of DRAM you can install because SI5PI AIO will not check the parity anyway. Therefore, this means that **either** parity or non-parity DRAM types can be installed.*

Rev 1.1: *supports the parity check function which may be enabled or disabled. In effect, **non-parity and parity DRAMs may be installed** under the condition that this parity checking option is enabled when installing parity DRAMs and disabled when using non-parity DRAMs. Likewise, if you install parity DRAMs with the parity check function disabled, SI5PI AIO will not check for the parity bit.*

5 Built-in BIOS SETUP Program

5.1 SETUP Program

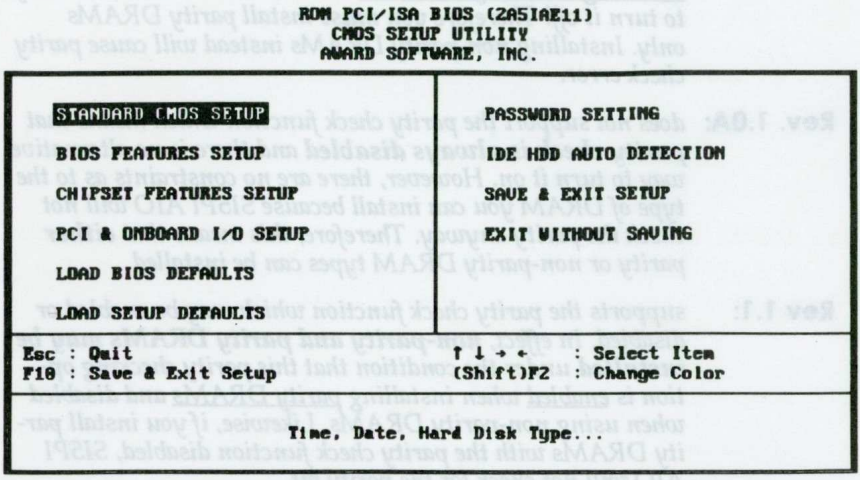


Figure 5-1. SETUP Main Menu

It is highly recommended that you list down all the values of the SETUP program before making any changes. Doing so will save a lot of time restoring the system back in the event of a configuration memory loss.

Note: *On-screen instructions at the bottom of each screen explain how to use the program.*

- **Standard CMOS SETUP** - allows checking or modification of general configuration information.
- **BIOS Features SETUP** - used to set the various system options for the user, including the virus warning, internal/external cache memory functions, quick power on self test, boot operations, gate A20 option, memory parity, security option, typematic rate settings, and BIOS shadowing.
- **Chipset Features SETUP** - dedicated for the user who wishes to program the chipset registers of the DRAM, cache, cacheable BIOS, non-cacheable block 1 size/start address etc.

- **PCI & Onboard I/O SETUP** - used to set the various system functions and internal addresses of the PCI devices and onboard PCI IDE controller.
- **Load BIOS Defaults** - allows for automatic configuration of all the options in the Standard CMOS SETUP/BIOS Features SETUP/Chipset Features SETUP with the BIOS defaults.
- **Load SETUP Defaults** - loads the SETUP default values which would allow safe booting of the system in the event a BIOS configuration memory loss.
- **Password Setting** - required when entering the SETUP program or booting your system. The user can change the current password stored in the CMOS by accessing this option.
- **IDE HDD Auto Detection** - allows for automatic detection of the hard disk drive type(s) including the number of cylinders and heads, write precompensation time, read/write head landing zone, and number of sectors per track.
- **Save & Exit SETUP** - saves the changes you have made in the SETUP program, then exits and reboots the system.
- **Exit Without Saving** - abandons all previous settings then exits and reboots the system.

To choose an item from the SETUP main menu, move the cursor using the <Left/Right> and <Up/Down>arrow keys and press <Enter>. To modify the setting of an option, simply press the <PgUp> or <+> and the <PgDn> or <-> keys. Press the <F2> key when changing the color setting, <F1> for a context sensitive help function, and the <ESC> key when quitting SETUP.

5.2 Standard CMOS SETUP

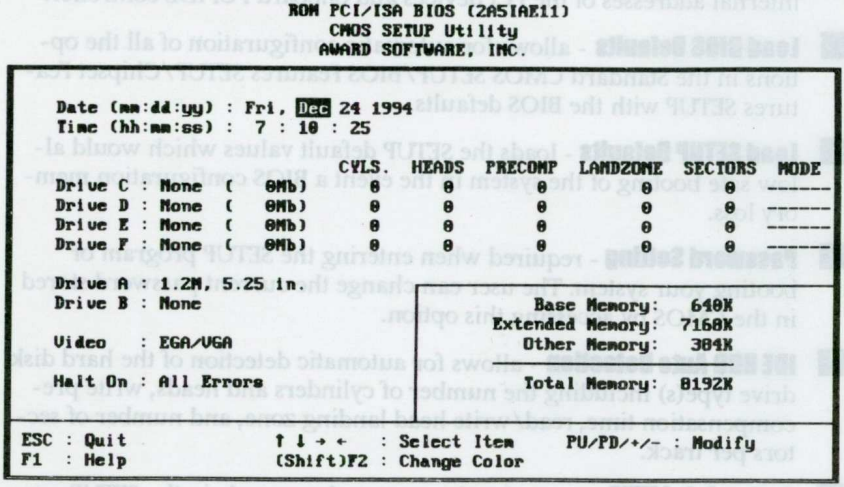


Figure 5-2. Standard CMOS SETUP Screen

Date - allows manual setting of the electronic calendar on the mainboard.

Time - sets the system's internal clock which includes hour, minutes, and seconds.

Drive C:/D:/E:/F: - specify the physical and electronic properties of the standard hard disk drives installed. Relevant specifications include the type, number of cylinders (CYLS.), heads (HEADS), write pre-compensation time (PRECOMP), read/write head landing zone (LANDZONE), number of sectors per track (SECTORS), and HDD mode (MODE). Selecting **"AUTO"** in the hard disk type item avoids the necessity of loading the HDD specifications and the function of the IDE HDD Auto Detection option in the main menu. The system BIOS will automatically detect the hard drive(s) installed on the system upon bootup.

Drive A:/B: - specify the capacity and format of the floppy drives installed in your system.

Video - specifies the display adapter installed.

Halt On - enables the system to halt on several conditions/options. The default value is set at **"All Errors"**.

Base/Extended/Other Memory - A small section in the lower right corner of the screen displays important information about your system which includes the base, extended, and other memory sizes. They are updated automatically by the SETUP program according to the status detected by the BIOS self-test. This section of the Standard CMOS SETUP screen is for viewing purpose only and manual modifications are not allowed.

5.3 BIOS Features SETUP

```
                ROM PCI/ISA BIOS (2A5IAE11)
                BIOS FEATURES SETUP
                AWARD SOFTWARE, INC.

Virus Warning                 : Disabled     Video BIOS Shadow     : Enabled
CPU Internal Cache            : Enabled      C8000-CBFFF Shadow    : Disabled
External Cache                : Enabled      CC000-CFFFF Shadow    : Disabled
Quick Power On Self Test      : Enabled      D0000-D3FFF Shadow    : Disabled
Boot Sequence                 : A,C          D4000-D7FFF Shadow    : Disabled
Swap Floppy Drive             : Disabled     D8000-DBFFF Shadow    : Disabled
Boot Up Floppy Seek           : Enabled      DC000-DFFFF Shadow    : Disabled
Boot Up NumLock Status        : On           E0000-E3FFF Shadow    : Disabled
Boot Up System Speed          : High         E4000-E7FFF Shadow    : Disabled
Gate A20 Option               : Fast         E8000-EBFFF Shadow    : Enabled
Typematic Rate Setting        : Disabled     EC000-EFFFF Shadow    : Enabled
Typematic Rate (Chars/Sec)    : 6
Typematic Delay (Msec)        : 250
Security Option               : Setup

ESC : Quit                    ↑↓→←: Select Item
F1  : Help                    PU/PD/+/- : Modify
F5  : Old Values              (Shift)F2 : Color
F6  : Load BIOS Defaults
F7  : Load Setup Defaults
```

Figure 5-3. BIOS Features SETUP Screen

Virus Warning - allows the virus warning feature for the hard disk boot sector to display a warning message and produce a beep sound whenever an attempt is made to write on the hard disk's boot sector. The default value for this option is **"Disabled."**

CPU Internal Cache - enables the internal 16KB code/data cache of the Intel Pentium™ CPU when set to **"Enabled"** (default).

External Cache - enables the on-board secondary cache (either standard non-burst or burst cache) when set to **"Enabled"** (default).

Quick Power On Self Test - allows the power on self test to run at either a fast or a normal speed. The available options are:

- Disabled (default)
- Enabled

Boot Sequence - selects the drive where the system would search for the operating system to run with. The available options are:

- A,C (default)
- C,A

Swap Floppy Drive - **"Enabled"** will effectively change the A: drive to B: and the B: to A: drive. **"Disabled"** (default) sets the floppy drives in their default states.

Boot Up Floppy Seek - checks whether the floppy drives installed on the system are correct or not. This option's operation usually occurs when the magnetic heads of the floppy drives produce a sound during power on self test. The available options are:

- Enabled (default)
- Disabled

Boot Up NumLock Status - sets the Num Lock key to either on or off during system boot-up. The available options are:

- On (default)
- Off

Boot Up System Speed - sets the speed of the system during power on self test sequence. The available options are:

- High (default)
- Low

Gate A20 Option - boosts the performance of systems with softwares using the 80286 protected mode such as OS/2 or UNIX. This option determines the accessibility of the extended memory. The available options are:

- Fast (default)
- Normal

Typematic Rate Setting - defines the setting of the keyboard's typematic rate. The available options are:

- Enabled
- Disabled (default)

Typematic Rate (Chars/Sec) - specifies the key repeat rate, in seconds, of keyboard characters. The available options are:

- 2/sec
- 6/sec (default)
- 10/sec
- 13.3/sec
- 18.5/sec
- 21.8/sec
- 26.7/sec
- 30/sec

Typematic Delay (Msec) - selects the delay, in milliseconds, before a key repeats itself. The available options are:

- 1/4 sec
- 1/2 sec (default)
- 3/4 sec
- 1 sec

Security Option - determines whether the password will be asked for in every boot (**System**), or when entering into the SETUP program (**Setup** - default). Refer to the section entitled Password Setting for the password setting procedure.

Video BIOS Shadow - enables the system shadowing and achieve the best performance of the system. The available options are:

- Enabled (default)
- Disabled

C8000-CBFFF, CC000-CFFFF, D0000-D3FFF, D4000-D7FFF, D8000-DBFFF, DC000-DFFFF, E0000-E3FFF, E4000-E7FFF Shadow - if you have a shadowing of the BIOS at any of the above segments, you may set the appropriate memory cacheable function to**"Enabled"**. Otherwise, select **"Disabled"** (default).

E8000-EBFFF, EC000-EFFFF Shadow - are both reserved for the NCR 53C810 BIOS shadowing. The default value for both of these segments is **"Enabled"**.

5.4 Chipset Features SETUP

```
                    ROM PCI/ISA BIOS (2A5IAE11)
                  CHIPSET FEATURES SETUP
                  AWARD SOFTWARE, INC.

Auto Configuration          : Enabled

Read CAS Pulse Width        : 4T
DRAM Write CAS Width        : 2T
L2 Cache Update Mode        : WB
L1 Cache Update Mode        : WB
DRAM Relocate (2,4 & 8M)    : Disabled
SRAM Speed Option           : Slower
SRAM Burst R/W Cycle        : 3T
Burst SRAM Burst Cycle      : 4-1-1-1

Refresh RAS Active Time     : 5T
DRAM RAS to CAS Delay       : 4T
DRAM RAS Precharge Time     : 5T
Gate A20 Emulation          : Enabled
Fast Reset Emulation        : Enabled
Slow Refresh (1:4)          : Disabled
System BIOS Cacheable       : Enabled
Video  BIOS Cacheable       : Enabled
Turbo/Deturbo Switch        : Enabled

Latency from ADSs status    : 2T
Refresh When CPU Hold       : Disabled
Snoop Filter                : Disabled
Post Write CAS Active       : 1T
CPU/PCI Post Write Delay    : 1T
PCI Clock Frequency         : CPUCLK/2
Max. Burstable Range        : 0.5Kb
CPU/PCI Burst Mem. Write    : Disabled
CPU/PCI Post  Mem. Write    : Disabled
ISA Bus Clock Frequency     : PCICLK/4

Non-Cacheable Block 1       : Disabled
  Block 1 Start Address     : 0000000H
  Block 1 Size              : 64KB

ESC : Quit          ↑↓→←: Select Item
F1  : Help          PU/PD/+/- : Modify
F5  : Old Values    (Shift)F2 : Color
F6  : Load BIOS Defaults
F7  : Load Setup Defaults
```

Figure 5-4. Chipset Features SETUP Screen

Auto Configuration - loads the default values, if **"Enabled"** (default), for the following DRAM and cache options. Otherwise, **"Disabled"** allows you to program each option as required.

Read CAS Pulse Width - determines the pulse width length of the CAS during DRAM read cycles. The available options are:

- 2T
- 3T
- 4T (default)

DRAM Write CAS Width - determines the pulse width length of the CAS during DRAM write cycles. The available options are:

- 2T (default)
- 3T

L2 Cache Update Mode - determines the mode wherein the external (L2) cache will operate. Choosing **"WB"** will set the cache in its fastest mode since writes as well as reads are cached. The available options are:

- WT
- WB (default)

L1 Cache Update Mode - sets the state of the (L1) internal cache of the Pentium™ CPU and determines the mode wherein data will be updated. The available options are:

- WB (default)
- WT

DRAM Relocate (2,4 & 8M) - remaps the 256K DRAM region to the top of the DRAM size. This option is only applicable when the D & E segments are not shadowed, and when total on-board memory is 2MB, 4MB, or 8MB. The available options are:

- Enabled
- Disabled (default)

SRAM Speed Option - specifies the speed of the standard SRAM cache during normal read/write operations. The available option are:

- Slower (default)
- Faster
- Fastest

SRAM Burst R/W Cycle - defines the speed of the cache SRAM burst read/write cycles. The available options are:

- 3T (default)
- 2T

Burst SRAM Burst Cycle - pertains to the total number of cycles the external (L2) cache is programmed to write-through a whole cache line. The available options are:

- 4-1-1-1 (default)
- 3-1-1-1

Refresh RAS Active Time - defines the amount of active time needed for the row address strobe (RAS), during DRAM refresh time, to be refreshed. The available options are:

- 5T (default)
- 6T

DRAM RAS To CAS Delay - defines the amount of time required after which a CAS# will be succeeded by RAS# signal during normal DRAM operations. The available options are:

- 3T
- 4T (default)

DRAM RAS Precharge Time - sets the amount of time for DRAM RAS recovery. The available options are:

- 4T
- 5T (default)

Gate A20 Emulation - allows access and increases the speed of the Gate A20 feature incorporated in the on-board chipset. When enabled, the SiS85C501 responds the cycle by asserting DEVSEL# in slowest timing. Otherwise, the cycle is subtractively decoded by SiS85C503, and then is passed to 8042 on the ISA Bus. The available options are:

- Enabled (default)
- Disabled

Fast Reset Emulation - enhances the speed of the software reset by delaying the assertion of INIT or CPURST by 2μs or 6μs, and holding them for 25 CPUCLK. The available options are:

- Enabled (default)
- Disabled

Slow Refresh (1:4) - allows you to turn the DRAM's slow refresh feature to on or off. The available options are:

- Enabled
- Disabled (default)

System BIOS Cacheable - allows caching of the different segments where there is system BIOS shadowing. The available options are:

- Enabled (default)
- Disabled

Video BIOS Cacheable - allows caching of the different segments where there is video BIOS shadowing. The available options are:

- Enabled (default)
- Disabled

Turbo/Deturbo Switch - enables the hardware turbo switch on-board and/or the keyboard control when changing the system speed.

- Enabled (default)
- Disabled

Latency from ADS# status - determines the CPU to PCI Post write speed. When this is set to **"3T"**, the Post write rate is 5T for each double word. When this option is set to **"2T"** (default), the rate is 4T per double word. For a Qword PCI memory write, the post write rate is 7T (2T) or 8T (3T).

- 2T (default)
- 3T

Refresh When CPU Hold - enables the refresh cycle when the CPU is in HOLD state. The available options are:

- Enabled
- Disabled (default)

Snoop Filter - prevents the need of multiple inquiries to the same line if the line was inquired previously. The available options are:

- Enabled
- Disabled (default)

Post Write CAS Active - defines the pulse width of CAS# when the PCI master writes to DRAM. The available options are:

- 1T (default)
- 2T

CPU/PCI Post Write Delay - pertains to the delay time before the CPU writes data into the PCI Bus. The available options are:

- 1T (default)
- 2T

PCI Clock Frequency - selects the timing of the PCI Bus clock. The available options are:

- CPUCLK/1.5
- CPUCLK/2 (default)
- 14Mhz

Max. Burstable Range - defines the maximum bursting length for each FRAME# asserting. The available options are:

- 0.5Kb (default)
- 1Kb

ISA Bus Clock Frequency - specifies the speed of the ISA Bus clock of the system. The available options are:

- PCICLK/3
- PCICLK/4 (default)
- 7.159Mhz

CPU/PCI Burst Mem. Write - If enabled, back-to-back sequential CPU memory write cycles to PCI are translated to PCI burst memory write cycles. If disabled, each single write to PCI will have an associated FRAME# sequence. The available options are:

- Enabled
- Disabled (default)

CPU/PCI Post Memory Write - enabling allows up to 4 Dwords of data to be posted to PCI. Disabling this option not only disables the buffering but also limits the completion of CPU write (CPU write does not complete until the PCI transaction completes). In general, this option enhances the performance of the PCI slots when **"Enabled"** (default).

- Enabled
- Disabled (default)

Non-cacheable Block 1 - allow a certain block of the local DRAM to be classified as non-cacheable. The available options are:

- Enabled
- Disabled (default)

Block 1 Start Address - accommodates ISA devices that have their memory mapped into the 1MB to 15.5MB range (i.e., an ISA LAN card or an ISA frame buffer), and defines a hole in main memory that transfers the cycles in this address space to the PCI Bus instead of main memory. This area is not cacheable and its default is **"0000000H."**

Block 1 Size - defines the size or Block 1. If the frame buffer range is programmed below 16MB and within main memory space, this option must include the frame buffer range. The amount of main memory specified in the following options is remapped to the top of main memory. The options are:

- 64KB (default)
- 128KB
- 256KB
- 512KB
- 1MB
- 2MB
- 4MB
- 8MB

5.5 PCI Configuration SETUP

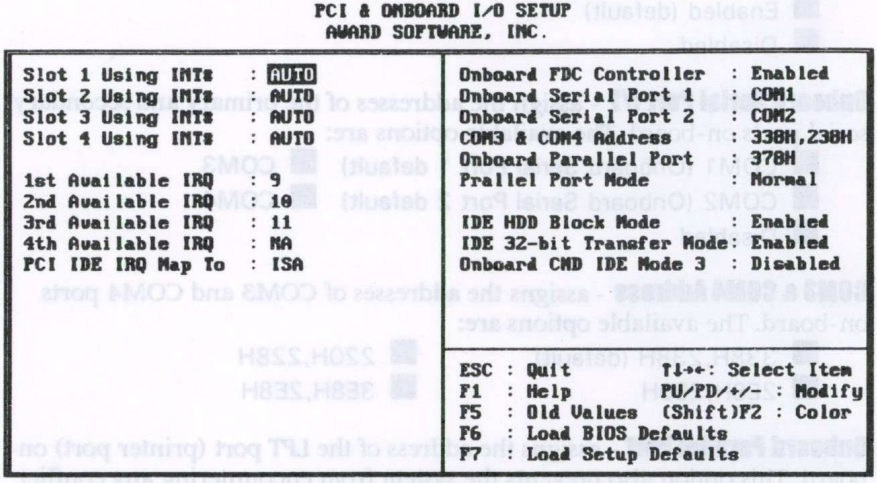


Figure 5-5. PCI Slot Configuration Screen

PCI Slot 1/2/3/4 Using INT# - defines the INTx# assigned to every PCI slot. The available options are:

- AUTO (default)
- A
- B
- C
- D

1st/2nd/3rd/4th Available IRQ - specify the IRQ for the PCI devices. The end user should assign an available IRQ if the PCI device needs an IRQ service. The available options are:

- NA (4th Available IRQ default)
- 3
- 4
- 5
- 7
- 9 (1st Available IRQ default)
- 10 (2nd Available IRQ default)
- 11 (3rd Available IRQ default)
- 12
- 14
- 15

PCI IDE IRQ Map To - defines the CMD PCI0640B IRQ Routing either from the **PCI** Bus or the **ISA** Bus. The default setting of this option is **"ISA."**

Onboard FDC Controller - sets the diskette controller mode of the CMD PCI0640B PCI Bus IDE controller chip to either on or off. The available options are:

- Enabled (default)
- Disabled

Onboard Serial Port 1/2 - assign the addresses of the primary and secondary serial ports on-board. The available options are:

- COM1 (Onboard Serial Port 1 default)
- COM2 (Onboard Serial Port 2 default)
- COM3
- COM4
- Disabled

COM3 & COM4 Address - assigns the addresses of COM3 and COM4 ports on-board. The available options are:

- 338H,238H (default)
- 2E8H,2E0H
- 220H,228H
- 3E8H,2E8H

Onboard Parallel Port - assigns the address of the LPT port (printer port) on-board. This option also prevents the system from encountering any conflict when an add-on card with parallel port is installed in the future. The available options are:

- 278H
- Disabled
- 3BCH
- 378H (default)

Parallel Port Mode - specifies the mode under which the parallel port is assigned to operate. In **"ECP+EPP"** mode, EPP can be selected through the ECR register of ECP mode 100. **"Normal"** (default) however can be selected through the ECR register as mode 000. The available options are:

- Normal (default)
- EPP
- ECP + EPP
- ECP

IDE HDD Block Mode - sets the IDE block mode which is dependent on the size of the hard drive cache. Enabling this option prevents multiple IRQ request lines to be sent in order to read more than 512 bytes. The available options are:

- Enabled (default)
- Disabled

IDE 32-bit Transfer Mode - refers to the setting of the 32-bit transfer rate of hard disk drives. Normally, I/O transfer cycles are accessed in 16 bits however by enabling this option, system transfer cycles perform faster because the BIOS reads hard disk data **twice** before it sends request signals to the CPU. The available options are:

- Enabled (default)
- Disabled

Onboard CMD IDE Mode 3 - permits access into the option ROM at segment E800 of the system BIOS. The option ROM then **programs** the timing registers of the CMD PCI0640B into a faster speed (minimum of 180ns - to IDE Mode 3 hard drives only), and turns on the Mode 3 feature of the installed hard drive. In the event that the installed hard disk drive does not support Mode 3, the option ROM will still program the timing registers to an acceptable rate compared to the chip's default timings. In general, this option enhances the hard drive's performance. The available options are:

- Enabled
- Disabled (default)

5.6 Load BIOS Defaults

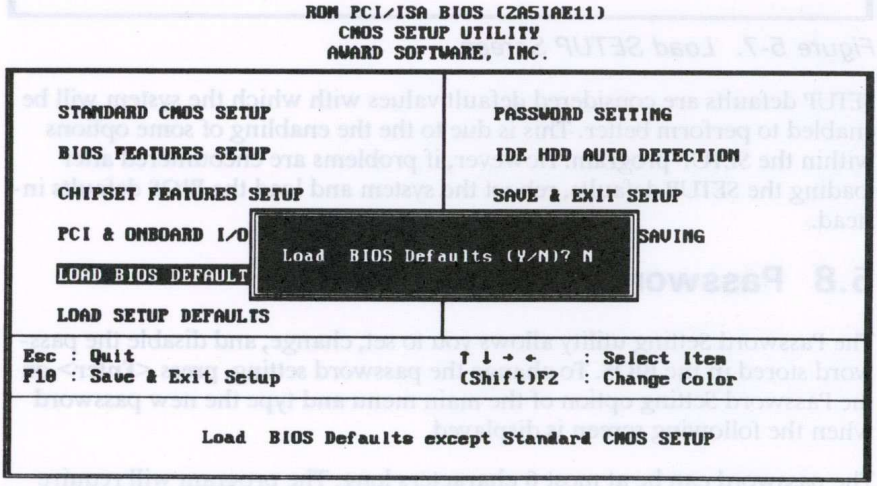


Figure 5-6. Load BIOS Defaults Screen

In the event of a loss in memory on the configuration SETUP, the user can restore the information on the BIOS by loading its default values. Loading the BIOS defaults provides safe booting of the system.

Important : *This option may not be able to configure all the values within the SETUP program according to the installed equipments (i.e., floppy drives A: & B:, hard disk drives C: & D:).*

5.7 Load SETUP Defaults

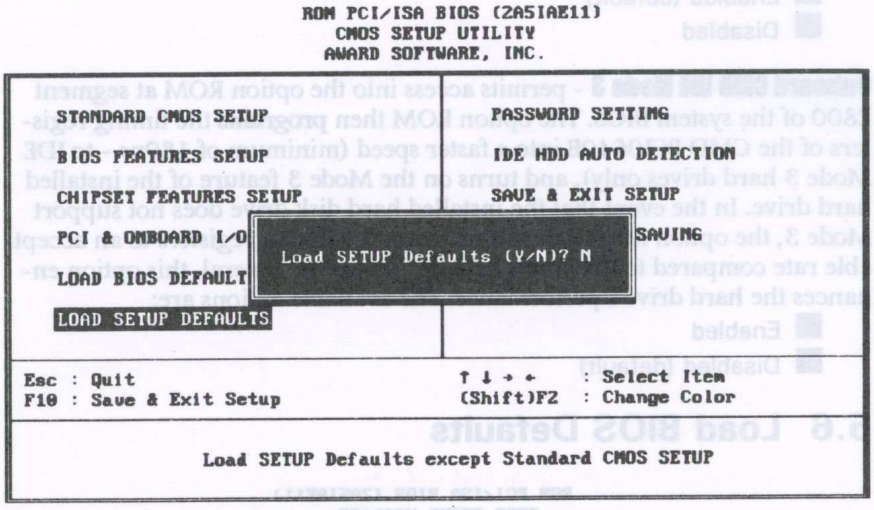


Figure 5-7. Load SETUP Screen

SETUP defaults are considered default values with which the system will be enabled to perform better. This is due to the the enabling of some options within the SETUP program. However, if problems are encountered after loading the SETUP defaults, reboot the system and load the BIOS defaults instead.

5.8 Password Setting

The Password Setting utility allows you to set, change, and disable the password stored in the BIOS. To change the password setting, press <Enter> on the Password Setting option of the main menu and type the new password when the following screen is displayed.

The password can be at most 6 characters long. The program will require you to confirm the new password before it exits and enables the utility. To disable the password setting, press the <F1> once the program asks you to enter the new password.

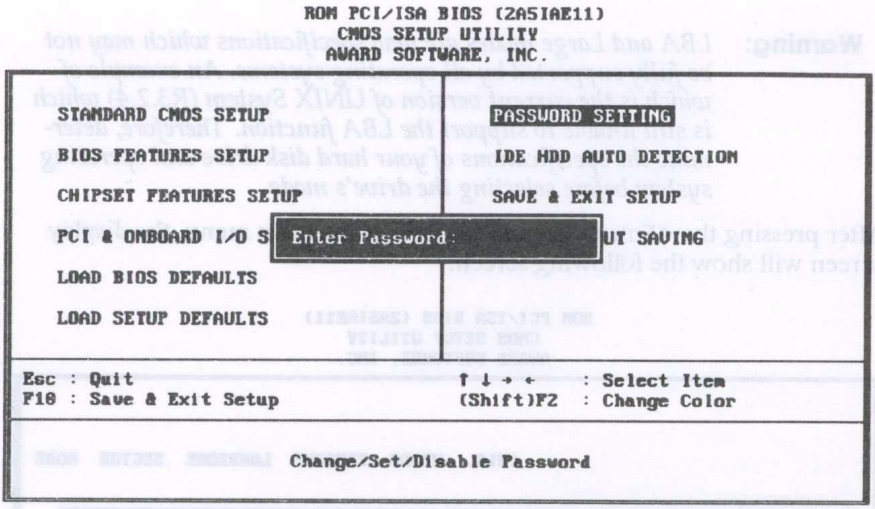


Figure 5-8. Password Setting Screen

Note : *Configure the Security Option within the BIOS Features Setup corresponding to the setting in this utility.*

5.9 IDE HDD Auto Detection

The IDE HDD Auto Detection provides auto configuration of the hard drive installed in the system. It supports LBA, Large, and Normal modes. If the system's hard disk drive has a capacity of over 528MB and supports LBA functions, you may enable either the LBA mode or the Large mode. On the other hand, if the hard disk drive's capacity is over 528MB but does support LBA functions, you may enable the Large mode in order to use over 528MB.

Note:

a. *The **LBA** and **Large** modes will only appear on the screen when the installed hard disk drive is specified to support the LBA mode.*

b. *In the case when a hard disk drive's cylinder specification exceeds 1024, and does not support the LBA functions, only the **Large** mode will be displayed on the screen.*

c. *With a hard disk drive supporting cylinders below 1024, only the **Normal** mode will appear on the screen. The **Normal** mode will also be shown on the screen under conditions a & b above.*

d. *Hard disk drives with less than 528MB total capacity must be set to **Normal** mode when combined with either old BIOS versions or the Award BIOS.*

Warning: *LBA and Large modes are new specifications which may not be fully supported by all operating systems. An example of which is the current version of UNIX System (R3.2.4) which is still unable to support the LBA function. Therefore, determine the specifications of your hard disk drive and operating system before selecting the drive's mode.*

After pressing the <Enter> key on this item of the main menu, the display screen will show the following screen.

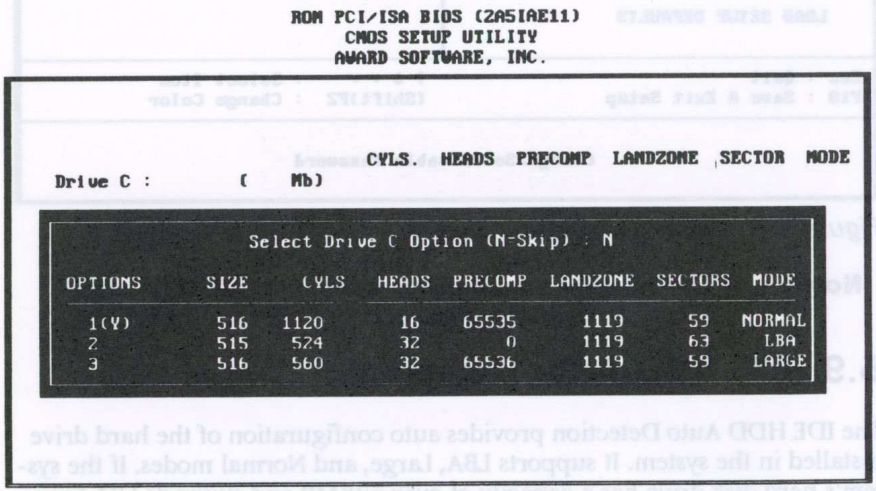


Figure 5-9. IDE HDD Auto Detection Screen

Once the program detects the type of hard disk installed, it will display the relative information such as the type, cylinders, heads, write pre-compensation, landing zone, number of sectors per track, size and mode. A message asking you to accept the IDE HDD detected will also be flashed on the screen.

5.10 Quitting SETUP

After making all modifications in the SETUP program, go to the option "Save & Exit SETUP" then press the <Enter> key. The program will display the following screen.

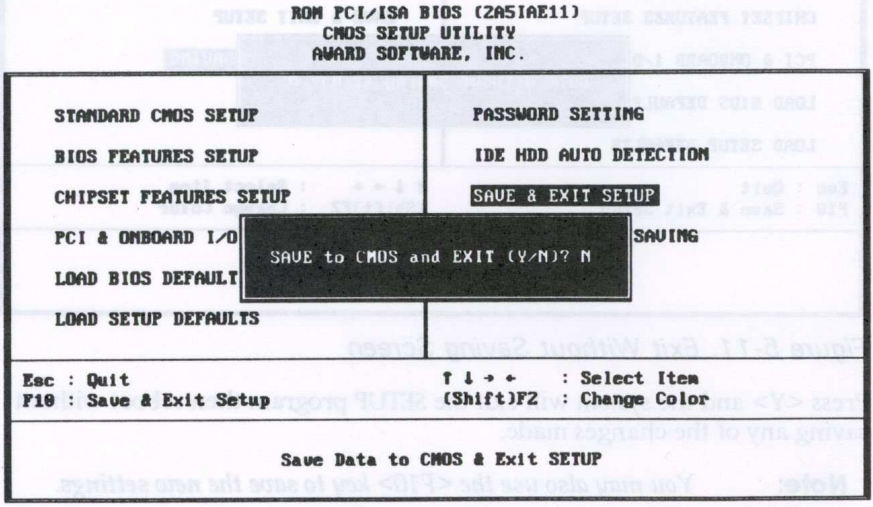


Figure 5-10. Save & Exit SETUP Screen

Press <Y> to confirm the changes made, and the <N> or the <ESC> keys if further modifications are still necessary before exiting the SETUP program. Once the <Y> key is pressed, the system will automatically exit the program and reboot. However, if you want to cancel all changes made under the SETUP program, go to the option "Exit Without Saving". The system will display the following screen.

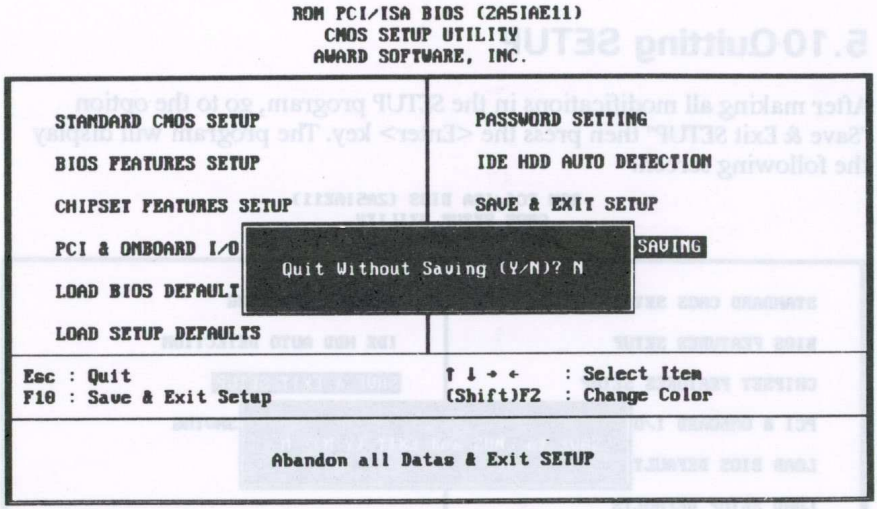


Figure 5-11. Exit Without Saving Screen

Press <Y> and the system will exit the SETUP program then reboot without saving any of the changes made.

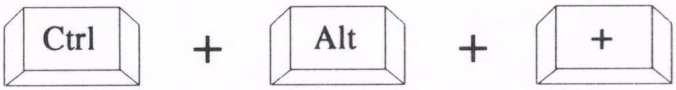
Note: *You may also use the <F10> key to save the new settings.*

Appendix A
Setting the System Speed

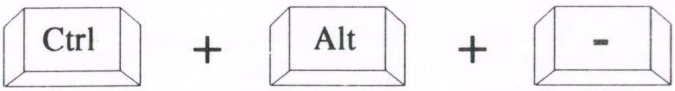
There is two methods in changing the system processing speed of your SI5PI AIO. The first method is implemented through the hardware connector designated as J16. The second method is done with the simultaneous pressing of several special keys on the keyboard known as hot-keys. You may change the speed during normal operation while working with your application program.

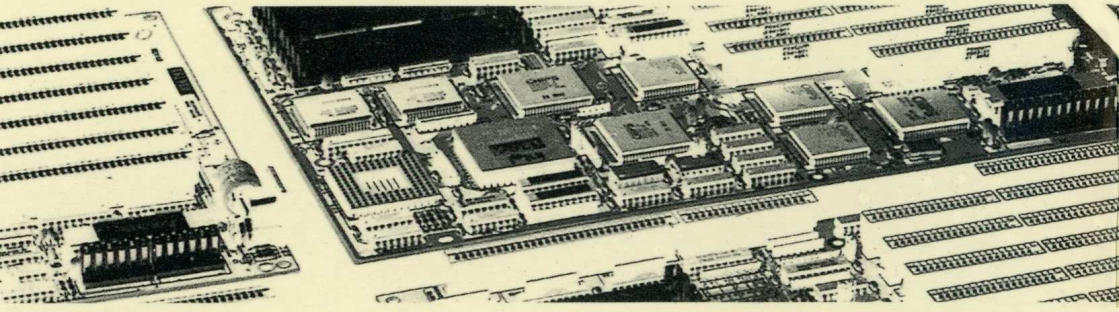
The hot-key combinations for setting the system speed on your SI5PI AIO are shown on the following diagrams.

High Speed



Low Speed





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