

# TEMPUSTECH, INC.

**VMAX® SBC 301**  
Single Board Computer

**TECHNICAL GUIDE**

Revision D (2)

## CONTENTS

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Copyright Statement  
Notice  
Trademarks  
U.S. Government Restricted Rights  
Warranty  
FCC Notice

### Section 1: INTRODUCTION

- 1.0 OVERVIEW
- 1.1 TECHNICAL SPECIFICATIONS MODEL 301
- 1.2 UNPACKING

### Section 2: HARDWARE SETUP

- 2.1 LOCATION OF JUMPERS, CONNECTORS & SOCKETS
- 2.2 JUMPERS
- 2.3 SINGLE INLINE MEMORY MODULES (SIMM)
- 2.4 SOLID STATE DISK MEMORY SELECTION
  - 2.4.1 Memory Chip Type
  - 2.4.2 Memory Chip Options
  - 2.4.3 Chip Installation
- 2.5 CABLE CONNECTIONS
  - 2.5.1 Turbo Switch Connector J1
  - 2.5.2 Speaker Connector J2
  - 2.5.3 Turbo LED Connector J3
  - 2.5.4 Reset Connector J4
  - 2.5.5 External Battery Connector J5
  - 2.5.6 Keyboard Connector J6
  - 2.5.7 Hard Drive Activity LED Connector J7
  - 2.5.8 IDE Hard Drive Connector J8
  - 2.5.9 PC/104 Expansion Port Connector J9, J10
  - 2.5.10 Floppy Disk Connector J11
  - 2.5.11 Com Port B Connector J12
  - 2.5.12 Com Port A Connector J13
  - 2.5.13 Parallel Port Connector J14
  - 2.5.14 External Power Connector P1

### Section 3: BIOS SETUP

- 3.1 BIOS OVERVIEW
- 3.2 ENTERING THE BIOS SETUP PROGRAM
- 3.3 BIOS SETUP PROGRAM
  - 3.3.1 Setup
  - 3.3.2 Extended BIOS Features
  - 3.3.3 System Information

### Section 4: ON BOARD PERIPHERALS

- 4.1 SERIAL PORTS
- 4.2 PARALLEL PORT
  - 4.2.1 Parallel Port Addressing
  - 4.2.2 Data Register
  - 4.2.3 Status Register
  - 4.2.4 Control Register
- 4.3 FLOPPY DISK DRIVE CONTROLLER
- 4.4 IDE HARD DISK INTERFACE

## CONTENTS

---

### Section 5: EXPANSION PORTS

- 5.1 PC/104 EXPANSION PORT (J9 & J10)
  - 5.1.1 PC/104 Module Dimensions

### Section 6: FLASH FILE SYSTEM

- 6.0 OVERVIEW
- 6.1 SEQUENCE OF STEPS
- 6.2 FFS INSTALLATION MENUS
  - 6.2.1 Menu Item - CONFIGURATION
  - 6.2.2 Menu Item - INSTALL
  - 6.2.3 Menu Item - FORMAT
- 6.3 FLASH FILE ERROR CODES
- 6.4 ERASE FLASH
- 6.5 DRIVE STORAGE CAPACITY

### Section 7: APPENDICES

- 7.1 PC/104 EXPANSION PORT PINOUT J9, J10
- 7.2 MECHANICAL DRAWING
- 7.3 POST CODE
- 7.4 BEEP CODE

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## FCC NOTICE

This equipment generates and uses radio frequency. If not installed and used in accordance with manufacturer's instructions, it may cause interference with radio and television reception. The user is responsible for ensuring that his product meets the limits of a Class A (or Class B, depending upon application) computing device in accordance with specifications in Subpart J of Part 15 of FCC rules, when installed in a suitably shielded case.

These rules are designed to provide reasonable protection against radio and television interference in a residential/business installation; however, there is no guarantee that interference will not occur. If this equipment should cause interference to radio or television reception, which can be determined by turning the equipment on and off, the user is encouraged to try to correct the interference by one of the following methods:

1. Reorient the receiving antenna
2. Move the computer
3. Plug the two devices into different outlets so that they are on different branch circuits
4. If necessary, consult the dealer or an experienced radio or television technician for additional suggestions.

*How to Identify and Resolve Radio and Television Interference Problems* is a booklet prepared by the Federal Communications Commission and is available from the U.S. Government Printing Office, Washington, D.C. 20402, Stock Number 004-000-00345-4.

### NOTE

In order for an installation of this product to maintain compliance with the limits for a Class A device, it is recommended that shielded cables be used for connecting any external devices and the cables must be properly grounded.

## Section 1: INTRODUCTION

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### 1.0 OVERVIEW

The 301 industrial grade CPU card brings optimum efficiency together with 100% IBMAT compatibility and enhanced features, without the physical size limitations encountered with conventional full size cards. Using less space and energy, the 301 possesses extensive capabilities.

The 301 will operate in any 16 bit passive ISA BUS backplane, enabling you to create a state of the art personal or industrial computing system. The slot card design of the 301 simplifies upgrades and repairs by being quick and easy to install and remove.

The 301 is a half-sized, low cost CPU card. Its +5v only operation and low power make it ideal for power critical operations. With the capability of up to 16 Meg of DRAM and a PC104 port, the 301 can be expanded to handle even the largest of tasks.

The 301 offers an excellent price/performance ratio and a wide range of features that include a 486SXLC PC compatible CPU operating at 66MHz, compact size (XT height), a 6.5 Meg Solid State Disk, 2 RS-232 serial ports, a bi-directional parallel port, hard and floppy disk controllers, PC104 expansion connectors, and 64KB of cache memory.

## Section 1: INTRODUCTION

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### 1.1 TECHNICAL SPECIFICATIONS MODEL 301

<b>PROCESSOR</b>	* <input type="checkbox"/> 486SXLC Processor
<b>CLOCK SPEED</b>	* <input type="checkbox"/> 66 Mhz Turbo / 33 MHz Deturbo
<b>L2 CACHE MEMORY</b>	* <input type="checkbox"/> 0K, or 64K, 0 wait state
<b>MAIN MEMORY</b>	* <input type="checkbox"/> 512K to 16 Meg, using standard 30 pin SIMMs SIMMs are 256K x 9, 1Meg x 9, or 4Meg x 9 * <input type="checkbox"/> Memory Speed 70ns (2 wait state)
<b>PARALLEL PORT</b>	* <input type="checkbox"/> Configurable as Output only, Input only or Bi-directional, Centronics compatible. DB25 connector. Addressed as: LPT1, LPT2, LPT3.
<b>COM PORT A</b>	* <input type="checkbox"/> RS232, DB9 connector
Signals	* <input type="checkbox"/> TX, RX, RTS, CTS, DTR, DCD
BAUD Rate	* <input type="checkbox"/> 50 to 56,000
Data Bits	* <input type="checkbox"/> 5, 6, 7 or 8
Parity	* <input type="checkbox"/> Odd, Even, None
Labels	* <input type="checkbox"/> COM1, COM2, COM3, or COM4
<b>COM PORT B</b>	* <input type="checkbox"/> RS232, 10 pin header connector.
Signals	* <input type="checkbox"/> TX, RX, RTS, CTS, DTR, DCD
BAUD Rate	* <input type="checkbox"/> 50 to 56,000
Data Bits	* <input type="checkbox"/> 5, 6, 7 or 8
Parity	* <input type="checkbox"/> Odd, Even, None
Labels	* <input type="checkbox"/> COM1, COM2, COM3, or COM4
<b>AT FLOPPY CONTROLLER</b>	* <input type="checkbox"/> Supports up to two floppy drives of 360K, 720K, 1.2Meg or 1.44Meg densities.
<b>IDE HARD DRIVE CONTROLLER</b>	* <input type="checkbox"/> Supports up to two IDE drives.
<b>SOLID STATE DISK</b>	* <input type="checkbox"/> Emulate up to two Disk Drives with a total capacity of 6.5 Meg.
Config. One	* <input type="checkbox"/> Drive 1: up to 6 Meg FLASH, Drive 2: up to 512K SRAM
Config. Two	* <input type="checkbox"/> Drive 1: up to 4 Meg FLASH, Drive 2: up to 2 Meg FLASH
<b>REAL TIME CLOCK BATTERY</b>	* <input type="checkbox"/> ± 5 min/month
Life	* <input type="checkbox"/> 3.6 VDC @ 0.7Ah on board * <input type="checkbox"/> 3 year minimum / 5 year typical
<b>BUS EXPANSION BUS</b>	* <input type="checkbox"/> Standard 16-bit ISA Bus operating at 6.6 MHz. * <input type="checkbox"/> PC/104 bus operating at 6.6 MHz
<b>LOW VOLTAGE MONITOR CONNECTIONS PROVIDED</b>	* <input type="checkbox"/> Resets the system if voltage drops below 4.65 VDC * <input type="checkbox"/> Reset Switch, Turbo Switch, Turbo LED, Hard Drive Activity LED, Keyboard, 2 Serial Ports,

IDE Drive, Floppy Drive, Parallel Port, PC104 expansion bus and power connector.

## Section 1: INTRODUCTION

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### 1.1 TECHNICAL SPECIFICATIONS MODEL 301

<b>POWER</b>	* □ + 5 VDC ± 5% @ 1.6 Amps max (1.4A typical)
<b>PHYSICAL SIZE</b>	* □ 4.2" X 7.9" X 0.85"
<b>OPERATING TEMP.</b>	* □ 0 to 60° C
<b>RELATIVE HUMIDITY</b>	* □ 0 to 95 % Non-Condensing

### 1.2 UNPACKING

Please unpack and inspect the 301 board when it is received.

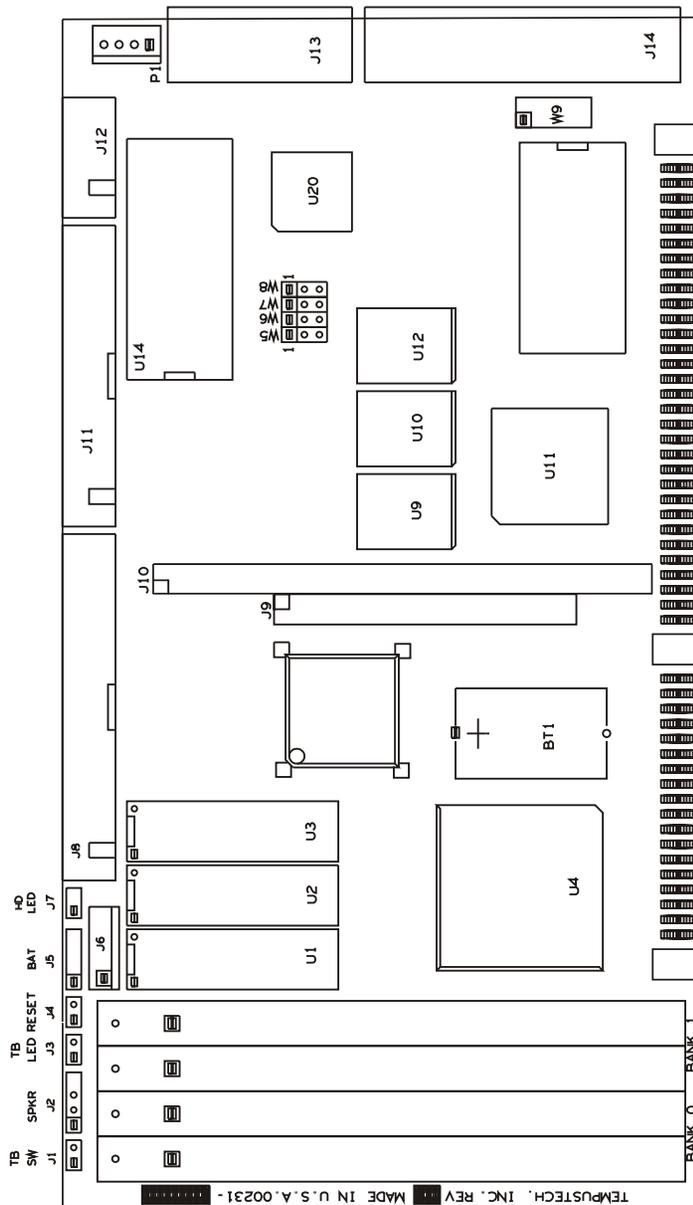
- \* □ Remove all documentation (packing lists, manuals, utility disks, etc.) from the shipping container.
- \* □ Carefully remove the packing material from around the 301 and lift it from the shipping container.
- \* □ Check the following list to be sure all items have been received.
  - 301 Single Board Computer
  - Technical Guide
  - 301 Utility Diskette(s)
  - Warranty Information (within Technical Guide)
  - Floppy Drive Cable
  - IDE Hard Drive Cable
  - Serial Port Cable
  - Keyboard Cable
- \* □ Inspect the items received for any visible damage that may have occurred during shipping.
- \* □ If an item is missing, or there is any damage, immediately notify the carrier concerned and the Customer Service Department at Tempustech, Inc., (941) 643-2424 or (800) 634-0701. Alternatively, you may notify us by E-mail. The address is **Service@Tempustech.com**

#### CAUTION

Your Tempustech, Inc. Card contains components that may be damaged by static electricity. To avoid problems with static electricity keep your 301 card in its antistatic bag prior to installation, and ground yourself prior to handling the card or touching any of the components on the card.

## Section 2: HARDWARE SETUP

### 2.1 LOCATION OF JUMPERS, CONNECTORS & SOCKETS



## Section 2: HARDWARE SETUP

### 2.2 JUMPERS

Pin 1 of all of the jumpers will be up or to the left when looking at the board with the gold fingers down, the bracket on the right, and the SIMM sockets on the left. All jumper(s) and connector(s) are conveniently labeled on the 301's silk-screen. Jumper positions will be at their default settings when shipped.

W9 Closing (shorting across pins) connects a peripheral to an interrupt, opening the jumper disconnects the peripheral from the interrupt.

#### W9 301 Interrupt Settings

- 1-2 Open: Parallel Port is on IRQ7
- 3-4 Close: Floppy Disk Drives are on IRQ6 (Default)
- 5-6 Close: Parallel Port is on IRQ5 (Default)
- 7-8 Close: Com Port A is on IRQ4 (Default)
- 9-10 Close: Com Port B is on IRQ3 (Default)

#### W5 Enable/disable of the FLASH chips in the Solid State Disk

- 1-2 Solid State Disk Enable
- 2-3 Solid State Disk Disable

#### W6 Solid State Disk configuration

- 1-2 The Solid State Disk is configured as Drive 1 has 3 FLASH chips and Drive 2 has 1 Static RAM chip (Default)
- 2-3 The Solid State Disk is configured as Drive 1 has 2 FLASH chips and Drive 2 has 1 FLASH chip

#### W8 W7 Memory Map Location for Solid State Disk

- |     |     |                      |       |
|-----|-----|----------------------|-------|
| 1-2 | 1-2 | SSD Address Location | D8000 |
| 1-2 | 2-3 | SSD Address Location | D0000 |
| 2-3 | 1-2 | SSD Address Location | C8000 |
| 2-3 | 2-3 | DO NOT USE           |       |

### 2.3 SINGLE INLINE MEMORY MODULES (SIMM)

The 301 card contains two memory banks of two SIMMs each, for a total of 4 SIMMs. SIMMs are installed to access up to 16 Meg of DRAM storage. SIMMs of **256K**, **1M**, and **4M** sizes may be used. SIMM sizes may be mixed between the 2 memory banks, but, the 2 SIMMs in a bank must be the same size. Total memory options are: 512K, 1M, 2M, 2.5M, 4M, 8M, 10M, and 16M.

Industry standard 30 pin, 9 bit wide SIMM memory modules are used. Memory BANK 0 consists of sockets M1 and M2, these are the left most two SIMM sockets. BANK 1 consists of sockets M3 and M4, these are the right two SIMM sockets. If only two SIMMs are going to be installed, Bank 0 should be used.

## Section 2: HARDWARE SETUP

### 2.3 SINGLE INLINE MEMORY MODULES (SIMM)

NOTE: SIMM modules must be installed in sets of two.

For efficient operation, DRAM with an access time of 100 nano-seconds or less should be used. Memory wait states should be set as follows:

For a 301 (66 MHz processor)	
DRAM	WAIT STATE
<u>SPEED</u>	<u>SETTING</u>
100NS	3
80NS	2
70NS	2
60NS	1
50NS	1

NOTE: The wait state setting must be made based on the **slowest** SIMM used on the board.

Refer to Section 3.3.1 for setting Memory Wait States.

To install a SIMM into a memory socket, place the connector edge of the SIMM into the slot of the memory socket. Press the SIMM into the socket so that the brackets on the memory socket lock the SIMM into place.

### 2.4 SOLID STATE DISK MEMORY SELECTION

#### 2.4.1 Memory Chip Type

##### SRAM Chips

Static RAM (SRAM) is memory which retains data integrity while power is applied to the 301. Non-volatility is achieved by using a battery to maintain power to the SRAM memory chip when system power is turned off.

SRAM chips have a virtually unlimited number of read and write cycles. The SRAM chip does not have to be erased before it is re-written. The old data is simply written over with new data. Data can be written to a SRAM very fast. SRAM Solid State Disk drives are the best choice when data is written frequently or very fast.

##### FLASH Chips

FLASH memory chips can be electronically erased and re-programmed while installed in the 301 card. FLASH memory is relatively slow to erase and reprogram, it can take several seconds to erase and completely rewrite a FLASH chip. FLASH memory does not require any power to retain data. FLASH is the best choice for data that will not be changed very often.

The 301 card comes with all the utilities needed to program and erase the FLASH devices while installed in the board. This is done with the Flash File System software which makes the FLASH chips act just like a disk drive to the system.

## Section 2: HARDWARE SETUP

### 2.4 SOLID STATE DISK MEMORY SELECTION

#### 2.4.1 Memory Chip Type

Although purely chip dependent, the lifetime of standard FLASH EPROM chips is between 10,000 erase/program cycles and 100,000 erase/program cycles.

#### 2.4.2 Memory Chip Options

The Solid State Disk Drive emulator on the 301 supports two memory chips. MAX.

#	<u>CHIP TYPE</u>	<u>SIZE</u>	<u>OF CHIPS</u>	<u>PACKAGE TYPE</u>
	FLASH	2 Meg x 8	3	48 pin TSOP
	SRAM	512K x 8	1	32 pin DIP

All memory chips should have an access time of 200ns or less.

The following chips have been approved for use.

Size	Type	Manufacturer	Part Number
2 Meg	FLASH	AMD	AM29F016
512K	FLASH	SST	NH29EE010
512K	SRAM	Dense Pac	DPS512S8P/LL

NOTE: Chips other than those listed above MUST be pin for pin compatible, including programming voltages and algorithms.

#### 2.4.3 Chip Installation

Up to two drives may be emulated. These drives are referred to as Drive 1 and Drive 2. The chip locations are labeled U9, U10, U12, and U14. Refer to the drawing in Section 2.1.

The emulated drives can be configured in two ways. Jumper W6 selects the desired configuration. Also see Section 2.2 for jumper settings.

##### **Configuration 1** (W6 Jumper across 1-2)

Drive 1 consists of up to three (3) FLASH chips.

Drive 2 consists of up to one (1) SRAM chip.

##### **Configuration 2** (Jumper across 2-3)

Drive 1 consists of up to two (2) FLASH chips.

Drive 2 consists of up to one (1) FLASH chip.

## Section 2: HARDWARE SETUP

### 2.4.3 Chip Installation

Zero to the maximum number of chips may be used in each drive.

**Configuration 1:** (Drive 1 up to 3 FLASH chips, Drive 2 up to 1 SRAM chip)

For the Drive 1 FLASH chips: Use U9 first, then U10, then U12.

For the Drive 2 SRAM chip: Use U14.

**Configuration 2:** (Drive 1 up to 2 FLASH chips, Drive 2 up to 1 FLASH chip)

For the Drive 1 FLASH chips: Use U9 first, then U10.

For the Drive 2 FLASH chip: Use U12.

### 2.5 CABLE CONNECTIONS

Once the CPU board is installed in your system, you may need to connect various peripherals and I/O devices to it. The following paragraphs describe the various external connections that may be made to the 301 CPU Board.

All of the headers on the 301 are the same type. The headers have 0.025" x 0.025" pins, 0.318" long on 0.1" centers. (They are similar to Dupont Bergstik connectors.)

Suggested mating connector families are:

Dupont® Bergcon #65039 Housing & Crimp Pin

Dupont® Quickie IDC #71602 Ribbon cable

All headers have Pin 1 to the left and down when the board is in its standard orientation of gold fingers down.

#### 2.5.1 Turbo Switch Connector J1

This is the connection for a turbo/det turbo switch. When the pins are open, the system runs at full speed, when they are shorted together, it runs at half speed.

Header: Single row 2 position (1 x 2).

Pinout: 1 2

##### J1 Turbo Switch Connections

<u>PIN</u>	<u>SIGNAL</u>	<u>DESCRIPTION</u>
1	Gnd	Signal ground.
2	Turbo Sw.	Open = Turbo mode (Full speed). Connected to Pin 1=Deturbo (Half speed).

## Section 2: HARDWARE SETUP

### 2.5 CABLE CONNECTIONS

#### 2.5.2 Speaker Connector J2

An external speaker may be connected here. The output drive is 2 Vp-p at 8 ma minimum. This output will drive a standard PC type speaker.

Header: Single row 4 position (1 x 4).

Pinout: 1 2 3 4

##### J2 Speaker Connections

<u>PIN</u>	<u>SIGNAL</u>	<u>DESCRIPTION</u>
1	Speaker	Output signal used to drive the speaker.
2	Not used	(key)
3	Gnd	Signal ground.
4	+5VDC	+5 Volt DC power.

#### 2.5.3 Turbo LED Connector J3

Use this connector to connect a turbo/det turbo indicator light. It is intended to power a LED. The LED will be ON when the system is operating at full speed and OFF when operating at half speed.

Header: Single row 2 position (1 x 2).

Pinout: 1 2

##### J3 Turbo LED Connections

<u>PIN</u>	<u>SIGNAL</u>	<u>DESCRIPTION</u>
1	LED Anode	A 24 ma current sinking driver.
2	LED Cathode	+5 VDC through a 330 OHM resistor.

#### 2.5.4 Reset Connector J4

This is the connection for a reset switch. A normally open momentary push button switch should be used.

Header: Single row 2 position (1 x 2).

Pinout: 1 2

##### J4 Reset Connections

<u>PIN</u>	<u>SIGNAL</u>	<u>DESCRIPTION</u>
1	Gnd	Signal ground.
2	Reset Sw.	Reset Switch used to initiate a system reset.

#### 2.5.5 External Battery Connector J5

The battery supplies power for the Real Time Clock, CMOS configuration memory and the optional SRAM Solid State Disk when the system is powered down.

The onboard battery provides power to the board through Connector J5. When this battery is being used, a jumper connects pins 1 and 2. This jumper can be removed when the board will be in storage for a long time to minimize battery drain. The jumper can be stored on pins 3 and 4.

In the event the on board battery discharges, the jumper may be removed and an external battery may be connected. The battery's output should be between 3.2 VDC and 3.6 VDC at 1 AH minimum, with a 3.6 VDC, 1.9 AH lithium battery preferred.

## Section 2: HARDWARE SETUP

### 2.5 CABLE CONNECTIONS

#### 2.5.5 External Battery Connector J5

Header: Single row 4 position (1 x 4).

Pinout: 1 2 3 4

##### J5 Battery Connections

PIN	SIGNAL	DESCRIPTION
1	External Battery Connection	Battery + terminal.
2	Onboard battery	Battery + terminal
3	Gnd	Signal ground.
4	Gnd	Signal ground (battery - terminal).

#### 2.5.6 Keyboard Connector J6

The signals on this connector will interface with a standard AT keyboard.

Header: Single row 5 position (1 x 5).

Pinout: 1 2 3 4 5

##### J6 Keyboard Connections

PIN	SIGNAL	DESCRIPTION
1	Kbclk	Keyboard Clock used as a bi-directional signal to synchronize the keyboard logic.
2	Kbdat	Keyboard Data used for bi-directional data transfer.
3	Not used	(key)
4	Gnd	Signal ground.
5	+5VDC	+5 Volt DC power.

#### 2.5.7 Hard Drive Activity LED Connector J7

Use this connector to connect a hard drive activity indicator. It is intended to power a LED. The LED will light when disk activity is occurring.

Header: Single row 2 position (1 x 2).

Pinout: 1 2

##### J7 Hard Drive Activity LED Connections

PIN	SIGNAL	DESCRIPTION
1	LED Anode	A 24 ma current sinking driver.
2	LED Cathode	+5 VDC through a 330 OHM resistor.

#### 2.5.8 IDE Hard Drive Connector J8

The IDE hard disk drive interface supports up to 2 disk drives. This is a standard IDE interface.

Header: Shrouded dual row 40 position (2 x 20).

Pinout: 2 4 6 ... 38 40  
1 3 5 ... 37 39

#### 2.5.9 PC/104 Expansion Port Connectors J9 & J10

This is a standard 16 Bit PC/104 Expansion Port. A PC/104 port is the AT ISA bus on a header connector instead of edge card fingers. A PC/104 expansion board would mount on the 301 as a daughter board. There are two mounting holes provided to attach to the PC/104 board to the 301.

## Section 2: HARDWARE SETUP

### 2.5 CABLE CONNECTIONS

#### 2.5.9 PC/104 Expansion Port Connectors J9 & J10

Header: Dual row female 62 position (2 x 32). Dual row female 40 position (2 x 20).

Pinout: B32 B31 B30 B29... B3 B2 B1  
A32 A31 A30 A29... A3 A2 A1  
C20 C19 C18 C17... C3 C2 C1 C0  
D20 D19 D18 D17... D3 D2 D1 D0

Refer to Section 5.1 for more details about the PC/104 expansion port, and Section 7.1 for signal descriptions.

#### 2.5.10 Floppy Disk Connector J11

The floppy disk drive interface supports any combination of 5 1/4" or 3 1/2" disk drives. 360K, 720K, 1.2M, and 1.44M floppy drives are supported. The interface is a standard XT/AT floppy disk interface.

Header: Shrouded dual row 34 position (2 x 17).

Pinout: 2 4 6 ... 32 34  
1 3 5 ... 31 33

#### 2.5.11 Com Port B Connector J12

This is the RS232 communication connector for Serial Port B.

Header: Shrouded dual row 10 position (2 x 5)

Pinout: 2 4 6 8 10  
1 3 5 7 9

##### J12 Com Port B RS232 Connections

J12 DB9		DESCRIPTION	
PIN	SIGNAL	PIN	DESCRIPTION
1	DCD	1	Data Carrier Detect. A low input indicates the data carrier is detected by the modem or data set.
2	RX	2	Receive Data. The input serial data from the peripheral link.
3	TX	3	Transmit Data. The output serial data to the peripheral link.
4	DTR	4	Data Terminal Ready. When low, this output indicates to the peripheral that the Model 301 is ready to establish a link.
5	Gnd	5	Signal Ground.

## Section 2: HARDWARE SETUP

### 2.5 CABLE CONNECTIONS

#### 2.5.11 Com Port B Connector J12

J12 DB9			
PIN	PIN	SIGNAL	DESCRIPTION
6	6	DSR	Data Set Ready. When low, this input indicates that the peripheral is ready to establish a link.
7	7	RTS	Request To Send. When low, this output indicates to the peripheral that the Model 301 is ready to output data.
8	8	CTS	Clear To Send. When low, this input indicates that the peripheral is ready to exchange data.
9	9	RI	Ring Indicator. When low, this input indicates that a telephone signal has been received by the modem or data set.
10	10		Not Used.

**NOTE:** The DB9 connector referred to in the table above is the DB9 connector on the serial cable Tempustech provides.

#### 2.5.12 Com Port A Connector J13

This is the RS232 communication connector for Com Port A.

Header: DB9 Male

Pinout: 1 2 3 4 5  
6 7 8 9

#### J13 Com Port A RS232 Connections

J13			
PIN	SIGNAL	Description	
1	DCD	Data Carrier Detect. A low input indicates the data carrier is detected by the modem or data set.	
2	RX	Receive Data. The input serial data from the peripheral link.	
3	TX	Transmit Data. The output serial data to the peripheral link.	
4	DTR	Data Terminal Ready. When low, this output indicates to the peripheral that the Model 301 is ready to establish a link.	
5	Gnd	Signal Ground.	
6	DSR	Data Set Ready. When low, this input indicates that the peripheral is ready to establish a link.	
7	RTS	Request to Send. When low, this output indicates to the peripheral that the Model 301 is ready to output data.	
8	CTS	Clear To Send. When low, this input indicates that the peripheral is ready to exchange data.	
9	RI	Ring Indicator. When low, this input indicates that a telephone signal has been received by the modem or data set.	

## Section 2: HARDWARE SETUP

### 2.5 CABLE CONNECTIONS

#### 2.5.13 Parallel Port Connector J14

This connector can be configured as a printer port, a parallel input port or a bi-directional port.

**PRINTER PORT:** This is a standard CENTRONICS compatible parallel printer port.

**INPUT PORT:** In this mode, parallel data is input on the port's 8 data bits. The control signals all function normally. The input data is not latched and must be held until the processor has read it.

**BI-DIRECTIONAL PORT:** In this mode, the direction of data flow is controlled by a bit in the parallel port's control register. See Section 4.2 for more information on controlling the port's direction. The control signals all function normally.

Connector: DB25 Female

Pinout: 13 12 11 10 9 8 7 6 5 4 3 2 1  
25 24 23 22 21 20 19 18 17 16 15 14

#### J14 Parallel Port Connections

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	/Stb	Data Strobe-Output.	10	/Ack	Acknowledge Input.
2	PD0*	Data Bit 0 Output.	11	Busy	Busy Input.
3	PD1*	Data Bit 1 Output.	12	PE	Paper End Input.
4	PD2*	Data Bit 2 Output.	13	Slct	Printer Select Input.
5	PD3*	Data Bit 3 Output.	14	/Afd	Auto Feed Output.
6	PD4*	Data Bit 4 Output.	15	/Err	Error Input.
7	PD5*	Data Bit 5 Output.	16	/Inlt	Initialize Output.
8	PD6*	Data Bit 6 Output.	17	/Slin	Select In Output.
9	PD7*	Data Bit 7 Output.	18-25	Gnd	Signal Ground

\* **PD7 - PD0** are data inputs when the port is configured as an input port. They are bi-directional when the port is configured as a bi-directional port.

#### 2.5.14 External Power Connector P1

This connector is provided for single board computer operation. When power is provided thru this connector, the 301 will operate without an ISA backplane.

#### P1 External Power Connections

PIN	NAME
1	+12 volts
2	- 12 volts
3	Ground
4	+5 volts

## Section 3: BIOS SETUP

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### 3.1 BIOS OVERVIEW

The 301 contains a BIOS produced by Phoenix Technologies Ltd. It runs in accordance with the industry standard AT BIOS. Since the BIOS is only 8 bits wide, it is recommended that the user shadow it in DRAM for better system performance.

Upon power-up, the Power-On Self Test (POST) routines are performed. Whenever a recoverable error occurs during the POST, the system BIOS will display an error message describing the problem. The message should explain the problem in sufficient detail so that the problem can be corrected. Some errors are audible rather than displayed. The audible error generated during POST is one long tone followed by two short tones. This audible error will result from either a failing video configuration (no or faulty video card installed) or an external ROM that does not properly checksum to zero. Any other audible errors consisting of one long tone followed by a series of short tones will be from an external ROM (a BIOS extension).

During the POST, the BIOS signals a checkpoint by outputting a code to I/O address 80H. This code can be used to establish how far the BIOS executed through the power on sequence and what test is currently being performed. This is done to help to troubleshoot faulty boards. Refer to Section 7.3 for more information on POST codes and their meanings.

A record of the 301's system configuration parameters (such as amount of memory, disk drives installed, and peripheral addressing) is stored in CMOS memory. When the board is powered down, a back-up battery provides power to the CMOS RAM, so it retains the system configuration parameters.

### 3.2 ENTERING THE BIOS SETUP PROGRAM

Each time the system is powered-on, it is configured according to the settings saved in CMOS memory. The settings can be modified by running the Phoenix Setup program. The Phoenix Setup program is resident in the ROM BIOS so it is available upon every power-up.

To enter the BIOS setup program: Press F2 during the powerup routines.

When running the BIOS Setup program only items surrounded by square brackets "[ ]" may be edited.

## Section 3: BIOS SETUP

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### 3.2 ENTERING THE BIOS SETUP PROGRAM

Use these keys throughout the BIOS Setup Program.

Esc Exit to the previous screen.

Cursor Keys Use to select the desired item.

F5 / F6 These keys cycle through the options for the highlighted feature.

F1 Displays the help screen for the selected feature.

F9 Automatically configures the system. This will determine the amount of memory in the system and set default values for the system memory, extended memory, shadow memory, EMS memory, wait states, ROM/RAM BIOS control, and video type. Auto configuration for the fixed disk is not always performed and must sometimes be done separately.

F10 Save the current configuration. The configuration, with the exception of the time and date, is not saved until F10 is pressed.

### 3.3 BIOS SETUP PROGRAM

The initial screen of the BIOS Setup Program is:

Extended BIOS Software Copyright 1989-92 Quadtel Corp.
Setup Extended BIOS Features System Information
Move <b>Enter</b> Select <b>Esc</b> Exit

**Setup** - Set date and time, type and size of disk drives, memory size and wait states, shadow Ram, cache and port addressing.

**Extended BIOS Features** - Set keyboard repeat rate, turn on the screen saver and park the hard disk heads.

**System Information** - Displays BIOS revision, processor type, memory size and port address information.

## Section 3: BIOS SETUP

### 3.3 BIOS SETUP PROGRAM

#### 3.3.1 Setup

When **Setup** is selected, the following window will be displayed:

BIOS Setup - Copyright 1989-92, Quadtel Corporation			
Current Date: [1/28/1990]	Video System: [Monochrome]		
Current Time: [15:23:01]	Power Up Speed: [Normal ]		
[ 640K] System Memory	BIOS Shadow: [System in ROM ]		
[ 1024K] Extended Memory	[Video in ROM ]		
OK Shadow Memory	Wait States: [Write 3 ]		
384K Reserved Memory	[Read 3 ]		
Internal COM A: [COM1, 3F8H]	Internal Floppy: [Enabled ]		
Internal COM B: [COM2, 2F8H]	Internal IDE: [Enabled ]		
Internal LPT: [LPT1, 378H ]	System Memory Cache: [Enable ]		
Diskette Drive A: [1.2 MB, 5 1/4 ]	Non-Cacheable Area: [1] of 2		
Diskette Drive B: [360 KB, 5 1/4 ]	Start: [192K] Size: [ 0K]		
Fixed Disk C: Type:[36] CY: 1024 HD: 8 ST: 17 LZ: 1024 WP: None			
Fixed Disk D: Type:[None]			
<b>F1</b> Move	<b>F5</b> Previous Value	<b>F9</b> Automatic Configuration	
<b>Esc</b> Help	<b>F6</b> Next Value	<b>F10</b> Save Configuration	
<b>Esc</b> Exit			

**Current Time** - Sets the hours, minutes, and seconds of the real time clock by using F5/F6 or typing in a new value. During the power up sequence, the time is read from the real time clock.

**Current Date** - Sets the month, day of the month, and year of the real time clock by using F5/F6 or typing in a new value. This information is read by DOS to determine the current date.

**System Memory Size** - Sets the system memory size. The system memory size will be 512K, or 640K.

**Extended Memory Size** - This option sets the extended memory size in increments of 64K. The maximum amount of extended memory is 15 Meg. The RAM on board can be partitioned or allocated between system memory, extended memory, and shadow memory. The setup program will only allow you to select valid combinations of these types of memory. You may press F9 to automatically resize memory and to select default memory values.

**Shadow Memory Size** - This indicates the amount of memory which is used for shadow memory. Shadow memory is used to copy the system and/or video BIOS into RAM to improve system performance.

## Section 3: BIOS SETUP

### 3.3 BIOS SETUP PROGRAM

#### 3.3.1. Setup

**COM and LPT General Information** - The automatic configuration (F9) will select the first logical COM and LPT port addresses which do not conflict with any other communication ports in your system.

**Internal COM A** - This selects the port address for the DB9 Com Port A, connector J13. The options that may be selected are COM1 (3F8H), COM2 (2F8H), COM3 (3E8H), COM4 (2E8H), and OFF.

**Internal COM B** - This selects the port address for the internal COM Port B (Com Port B, connector J12). The options that may be selected are COM1 (3F8H), COM2 (2F8H), COM3 (3E8H), COM4 (2E8H), and OFF.

**Internal LPT** - This selects the port address for the DB25 LPT port. The choices are 378H, 278H, 3BCH and OFF. Choose off to disable the on-board parallel port. Select one of the three hex address to enable the parallel port. The BIOS does a search of the three possible printer port address and assigns the designators "LPT1", "LPT2" and "LPT3". The addresses are searched in this order, 3BCH first, then 378H, then 278H. The first port found is assigned to LPT1, the second found to LPT2 and the third to LPT3. NOTE: If there is one printer port in the system it will be assigned "LPT1" no matter what its address.

**Diskette Drive** - Configures Floppy drives A and B to be a 360K, 1.2Meg, 720K, 1.44Meg, 2.88Meg drive or Not Installed. The 360K and 1.2Meg drives are 5 1/4" drives and the 720K, 1.44Meg, and 2.88Meg drives are 3 1/2" drives.

**Fixed Disk** - Configures fixed disk drives C and D to be one of 45 drive types, User Defined, Auto or Not Installed. All 45 drive types can be displayed on the screen by pressing F1 for help and then F2. The **User** defined fixed disk drive type allows you to create a drive type that is not in the standard fixed disk drive tables. When **User** is selected in the fixed disk type field for either drive C or drive D, the number of cylinders, heads, sectors per track, write precompensation cylinder, and landing zone cylinder become editable. Move the cursor to each field and type in or use **F5** and **F6** to select the appropriate number in each case. Consult your fixed disk drive manual for details on the number of cylinders, heads, sectors per track, write precompensation cylinder, and landing zone cylinder. Drives C and D can both be user defined and have different values for the various parameters. When **Auto** is selected the system will try to automatically determine which fixed disk drive type is attached.

## Section 3: BIOS SETUP

### 3.3 BIOS SETUP PROGRAM

#### 3.3.1 Setup

The drive types are identified by the following characteristics:

Type:	This is the number designation for a drive with certain identification parameters.
CY:	This is the number of cylinders found in the specified drive type.
HD:	This is the number of heads found in the specified drive type.
ST:	Sectors are the number of blocks of data on a track.
LZ:	Landing zone for the heads. This number determines the cylinder location where the heads will park when the system is shut down.
WP:	Write Precompensation is a read delay circuitry parameter which takes into account the timing differences between the inner and outer edges of the surface of the disk platter. The number designates the cylinder at which the compensation starts.
Capacity:	The formatted capacity of the drive. The capacity can be calculated by the following formula: (# of heads) x (# of cylinders) x (# secs/cyl.) x (512 bytes/sec).

## Section 3: BIOS SETUP

### 3.3 BIOS SETUP PROGRAM

#### 3.3.1 Setup

The Standard Drive Types are:

TY	CY	HD	ST	LZ	WP	Capacity
1	306	4	17	305	128	10MB
2	615	4	17	615	300	70MB
3	615	6	17	615	300	131MB
4	940	8	17	940	512	62MB
5	940	6	17	940	512	47MB
6	615	4	17	615	None	20MB
7	462	8	17	511	256	31MB
8	733	5	17	733	None	30MB
9	900	15	17	901	None	112MB
10	820	3	17	820	None	20MB
11	855	5	17	855	None	35MB
12	855	7	17	855	None	50MB
13	306	8	17	319	128	20MB
14	733	7	17	733	None	43MB
15	Reserved					
16	612	4	17	663	0	20MB
17	977	5	17	977	300	41MB
18	977	7	17	977	None	57MB
19	1024	7	17	1023	512	60MB
20	733	5	17	732	300	30MB
21	733	7	17	732	300	43MB
22	733	5	17	732	300	30MB
23	306	4	17	336	0	10MB
24	612	4	17	663	305	20MB
25	612	2	17	612	300	10MB
26	614	4	17	614	None	20MB
27	820	6	17	820	None	40MB
28	977	5	17	977	None	40MB
29	1218	15	36	1218	None	321MB
30	1224	15	17	1224	None	152MB
31	823	10	17	823	512	68MB
32	809	6	17	809	128	40MB
33	830	7	17	830	None	48MB
34	830	10	17	830	None	68MB
35	1024	5	17	1024	None	42MB
36	1024	8	17	1024	None	68MB
37	615	8	17	615	128	40MB
38	1024	8	26	1024	None	104MB
39	925	9	17	925	None	69MB
40	1024	9	17	1023	None	76MB
41	918	15	17	917	None	114MB
42	1024	15	17	1023	None	127MB
43	823	10	17	822	None	136MB
44	969	5	34	969	None	80MB
45	969	7	34	969	None	112MB

## Section 3: BIOS SETUP

### 3.3 BIOS SETUP PROGRAM

#### 3.3.1 Setup

**Video Type** - The video system can be set to one of four configurations. The video types are Monochrome, 40 X 25 CGA, 80 X 25 CGA, EGA/VGA.

**Power Up Speed** - This setting has no effect on the system.

**BIOS Shadow** - Normally the BIOS executes from an EPROM. If Shadow Ram is available, the BIOS can be copied into DRAM and executed. This substantially increases BIOS execution speed. The System BIOS and/or the Video BIOS may be shadowed.

**Wait States** - This allows the user to select 0, 1, 2, or 3 wait states for on board DRAM memory. Read and Write wait states may be different from each other, but we recommend they always be made the same. Selecting fewer wait states than required for your DRAM speed may cause the system to malfunction.

DRAM Speed	Wait State Setting
50 ns	1
60 ns	1
70 ns	2
80 ns	2
100 ns	3

**Internal Floppy** - This Enables or Disables the on board floppy disk controller.

**Internal IDE** - This Enables or Disables the on board IDE (hard) disk controller.

**On Chip Cache** - The 486 SXLC2-66 processor has 8K-byte, 32 bit on-chip cache. It is write-through unified instruction/data cache with lines that are allocated only during memory read cycles. The cache is configured as two-way set associative and the organization consists of 1024 sets each containing two lines of four bytes each.

**System Memory Cache** - This allows you to Enable or Disable the level 2 cache memory. If you have the optional on board Level 2 cache, this option should be Enabled to increase system performance.

**Non-Cacheable Area** - If System Memory Level 2 Cache is Enabled then, there are two non-cacheable areas that can be defined. This setting selects which area is being configured. Refer to Start and Size below.

**Start and Size** - This feature allows you to set a block of memory where memory caching will not take place. Set the size of the block and the starting address.

**NOTE:**

The Level 1 Cache Memory is always enabled.

## Section 3: BIOS SETUP

### 3.3 BIOS SETUP PROGRAM

#### 3.3.1. Setup

**Start and Size** - The block size may be set to 0K, 64K, 128K, 256K, 512K, 1024K, 2048K, 4096K or 8192K. The starting address may be set to any 64K boundary. This option can only be used if System Memory Cache is enabled. The following table shows standard Hex memory addresses and their Decimal equivalents.

Hex Address	Equivalent	Decimal Address
A0000		640K
B0000		704K
C0000		768K
D0000		832K
E0000		896K
F0000		960K

#### 3.3.2 Extended BIOS Features

The Extended BIOS Features offers a number of functions which normally require separate utility programs. If the Extended BIOS Features are selected, the menu below is displayed:

Extended BIOS Features- Copyright 1989, Quadtel Corp			
Auto-park Disk:	[No]	Keyboard Click:	[No ]
Quick Boot:	[No]	Keyboard Delay:	[1/4 Sec ]
Screen Saver:	[Disabled]	Keyboard Rate:	[30/Sec ]
		Numlock Boot State:	[Auto ]
Move	F5 Previous Value	F9	Auto Configuration
Esc Exit	F6 Next Value	F10	Save Configuration

**Auto-park Disk** - This option selects whether or not the system BIOS should automatically park the fixed disk drive. If the option is enabled (set to Yes), after several seconds of inactivity, the system BIOS will park the fixed disk drive heads. Parking the heads helps save the disk media when the system is powered on or when the system is moved. This option can be incompatible with some types of fixed disk drives which are not BIOS compatible and could cause problems with programs which do not utilize the BIOS for fixed disk input and output.

**Quick Boot** - When this option is enabled (set to Yes), the system BIOS will bypass the floppy disk drive tests, memory tests and floppy disk drive boot on power-on or soft reset. This will cause the system to initialize and boot from the fixed disk in only a few seconds. If the fixed disk becomes inoperable, it will then seek floppy disk drive A. If this option is selected memory will not be tested and the floppy disk drive types defined in the Setup window (see above) must be correct.

## Section 3: BIOS SETUP

### 3.3 BIOS SETUP PROGRAM

#### 3.3.2 Extended BIOS Features

**Screen Saver** - This option provides a way of blanking the screen after a specified period of system inactivity. You can select 10 minutes, 30 minutes, one hour or disable the option. If no keyboard activity is detected by the BIOS during the duration selected, the screen will be blanked. When you return to work on your system and the screen is blank, press any key on the keyboard and the screen will be redisplayed. Screen Saver will prevent the data displayed on the screen from "burning" the monitor.

**WARNING:** Some programs do not use the BIOS for keyboard handling. The most notable among these is Microsoft Windows. Do not use the Screen Saver if you are using any of these programs.

In the event that you use Screen Saver with Windows or another program like it, the screen will blank after the selected duration of time regardless of whether or not you have pressed a key. In addition, pressing a key after the screen is blank will not bring the screen back. The system will continue to work and you should be able to exit from the program at which time the screen will return.

**Keyboard Click** - This option, if selected, will cause the BIOS to click through the system speaker each time a key is pressed. This provides an audible feedback which indicates that a key has been pressed.

**Keyboard Delay** - The keyboard delay is the amount of time which will elapse after a key is depressed before the key starts to repeat. The smaller the time which is selected, the sooner the key will start to repeat. You may select 1/4 second, 1/2 second, 3/4 second, or 1 second.

**Keyboard Rate** - This option defines the rate at which the keyboard repeats while a key is depressed. The number you select is the number of keys per second that the keyboard will generate. The following values may be selected: 2, 6, 10, 13, 18, 22, 27, or 30.

**Numlock Boot State** - This option defines how the Numlock key should be defined by the BIOS on power up or soft reset. The Numlock key on the keyboard is used to determine whether the cursor keys or the numeric keys are active on the keypad. If Auto is selected for the Numlock Boot State, the BIOS will set the Numlock (select the numeric keys) if a 101 or 102 key keyboard is detected on power up or if an 84 key keyboard is detected the Numlock will be turned off (cursor keys selected). You may also select On to always select the numeric keys regardless of the keyboard or Off to always select the cursor movement keys.

## Section 3: BIOS SETUP

### 3.3 BIOS SETUP PROGRAM

#### 3.3.3 System Information

The System Information Screen looks like:

System Information, Copyright 1989, Quadtel Corp			
Processor:	80386/SX	LPT1 Address:	0378H
Coprocessor:	None	LPT2 Address:	Unused
		LPT3 Address:	Unused
BIOS ID:	487070000B	COM1 Address:	03F8H
BIOS Revision:	03.07.06	COM2 Address:	02F8H
Programmable Memory:	2048K	COM3 Address:	Unused
Other Memory:	0K	COM4 Address:	Unused
		Internal Mouse:	No
Press <any key> to exit.			

**Processor** - Indicates what type of processor the BIOS has detected in the 301. **Note:** The 486SXL Processor displays as an 80386SX.

**BIOS ID** - Is a special code which tells a number of items about your system BIOS.

**BIOS Revision** - Shows what version of the system BIOS you are using.

**Programmable Memory** - Is the amount of memory which is controlled by the BIOS. This is memory which the BIOS programs on power-on or soft reset.

**Other Memory** - Is memory which has been detected by the BIOS but is not under BIOS control. The sum of programmable memory and other memory is the total memory in your system. It will not include any EMS or other types of memory in your system.

The **LPT** and **COM** indicators will show which communication ports are installed and what their addresses are in your system.

After you have reviewed the items in the window, press **Esc** to exit.

## Section 4: ON BOARD PERIPHERALS

The 301 has several standard on board peripherals. The peripheral functions are described in the following sections.

### 4.1 SERIAL PORTS

Each of the serial port UARTs is the equivalent to a 16450 UART. Both UARTs perform serial-to-parallel conversion on data characters received from the RS-232 port and parallel-to-serial conversion on data characters received from the CPU. Each serial port has its own register set and can be independently configured.

#### Communication Parameters Supported

BAUD Rates: 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19200, 28400, 56000  
 Parity: Odd, Even, None  
 Data Bits: 5, 6, 7 or 8  
 Stop Bits: 1 or 2

**Com Port A (J13)** is a full duplex RS232 port. Connection to it is provided by a DB9 connector. RS232 signals supported are TX, RX, RTS, CTS, DCD, DSR, DTR and RI. Refer to Section 2.5.12 for connector pinout. Com Port A can be addressed as COM1, COM2, COM3, COM4 or disabled (Refer to Section 3.3.1).

**Com Port B (J12)** is a full duplex RS232 port. Com Port B can be addressed as COM1, COM2, COM3, COM4 or disabled (Refer to Section 3.3.1).

The RS232 connection is provided through J12, a 10-pin header. The RS232 signals supported are TX, RX, RTS, CTS, DCD, DSR, DTR and RI. Refer to Section 2.6.11 for complete pinout information.

### 4.2 PARALLEL PORT

The parallel port can be operated as a printer port, input port or bi-directional port. Selection of which type of port is done through software. The port defaults to a standard parallel printer port, but the user's software may modify the operation of the port as described below. The parallel port connector is J14, refer to Section 2.6.13 for the connector pinout.

## Section 4: ON BOARD PERIPHERALS

### 4.2 PARALLEL PORT

**PRINTER PORT:** This is a standard CENTRONICS compatible parallel printer port.

**INPUT PORT:** In this mode, parallel data is input on the port's 8 data bits. The control signals all function normally. The input data is not latched and must be held until the processor has read it.

**BI-DIRECTIONAL PORT:** In this mode, the direction of data flow is controlled by a bit in the parallel port's control register. The control signals all function normally.

#### 4.2.1 Parallel Port Addressing

The parallel port is compatible with standard ISA parallel printer ports and can be addressed as (3BCH-3BFH) or (378H-37BH) or (278H-27BH).

**TABLE 4-1. Parallel Interface Register Addresses**

			Register	Access
3BCH	378H	278H	Data	Read/Write
3BDH	379H	279H	Status	Read
3BEH	37AH	27AH	Control	Read/Write
3BFH	37BH	27BH	TRI-STATE	-

#### 4.2.2 Data Register

This is a bidirectional data port that transfers 8-bit data. The direction is determined by the Control Register Bit 5.

#### 4.2.3 Status Register

This register provides status for the signals listed below. It is a read only register. Writing to it is an invalid operation that has no effect.

Bits 0,1 Reserved, these bits are always 1.

Bit 3 This bit is the IRQ STATUS bit. If the Control Register Bit 4 = 1, then this bit is latched low when the ACK signal makes a transition from low to high. Reading this bit sets it to a one.

Bit 4 This bit represents the current state of the printer error signal (ERROR). The printer sets this bit low when there is a printer error. This bit follows the state of the ERR pin.

## Section 4: ON BOARD PERIPHERALS

### 4.2 PARALLEL PORT

#### 4.2.3 Status Register

- Bit 5 This bit represents the current state of the printer paper end signal (PE). The printer sets this bit high when it detects the end of the paper. This bit follows the state of the SLCT pin.
- Bit 6 This bit represents the current state of the printer acknowledge signal (ACK). The printer pulses this signal low after it has received a character and is ready to receive another one. This bit follows the state of the ACK pin.
- Bit 7 This bit (BUSY) represents the current state of the printer busy signal. The printer sets this bit low when it is busy and cannot accept another character. This bit is the inverse of the (BUSY) pin.

#### 4.2.4 Control Register (CTR)

This register provides all output signals to control the printer. It is a read and write register, except for bit 5, which is write only.

- Bit 0 This bit (STB) directly controls the data strobe signal to the printer via the STB pin. This bit is the inverse of the STB pin.
- Bit 1 This bit (AFD) directly controls the automatic feed signal to the printer via the AFD pin. Setting this bit high causes the printer to automatically feed after each line is printed. This bit is the inverse of the AFD pin.
- Bit 2 This bit (INIT) directly controls the signal to initialize the printer via the INIT pin. Setting this bit low initializes the printer. This bit follows the INIT pin.
- Bit 3 This bit (SLIN) directly controls the select in signal to the printer via the SLIN pin. Setting this bit high selects the printer. This bit is the inverse of the SLIN pin.
- Bit 4 This bit enables the parallel port interrupt. Setting the bit low puts IRQ5 or IRQ7 into TRI-STATE and clears any pending interrupts. Which interrupt depends on which interrupt was selected by W9 (refer to Section 2.2). When this bit is set high, the appropriate IRQ signal follows the ACK signal and latches high on a 0 to 1 transition.
- Bit 5 This bit determines the parallel port direction. The default condition results in the parallel port being in the output mode. This is a WRITE ONLY bit. See Table 4-2 for further details.

## Section 4: ON BOARD PERIPHERALS

### 4.2 PARALLEL PORT

#### 4.2.4 Control Register (CTR)

A write operation to the data register causes the data to be latched. If the bit is 0, the latched data is presented to the I/O pins; if it is 1 the data is only latched. When the bit is 0, a read of the register allows the CPU to read the last data it wrote to the port. With the bit set to a 1 (input), a read operation of this register causes the port to present the data on I/O pins PD0-PD7. By switching the bit the user can make the port act as a bi-directional I/O port.

TABLE 4-2. Data Register Read and Write Modes

BIT 5	RD	WR	Result
0	1	0	Data Written to I/O pins PD0-PD7
1	1	0	Data written is latched internally
0	0	1	Data Read from the internal data register
1	0	1	Data Read from I/O pins PD0-PD7

Bits 6,7 Reserved. These bits are always 1.

Normally when the Control Register is read, the bit values are provided by the internal output data latch. These bit values can be superseded by the logic level of the STB, AFD, INIT, and SLIN pins, if these pins are forced high or low by an external voltage. In order to force these pins high or low the corresponding bits should be set to their inactive state (e.g., AFD = STB = SLIN = 0, INIT = 1).

#### 4.3 FLOPPY DISK DRIVE CONTROLLER

The 301 features a full function two drive floppy disk controller. The controller incorporates a precision analog data separator. It recognizes both low and high density drives including 360K, 720K, 1.2M, 1.44M and 2.88M drive sizes. Connection to the floppy drives is provided by J11, a standard connector header on the 301 board.

#### 4.4 IDE HARD DISK INTERFACE

The 301 provides an IDE hard disk interface for up to two drives. A standard IDE interface header (J8) is provided on the board. There is also a header (J7) provided for a drive activity LED.

## Section 5: EXPANSION PORTS

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### 5.1 PC/104 EXPANSION PORT (J9 & J10)

This expansion port is a compact version of the IEEE P996 PC bus (ISA bus), it is optimized for the unique requirements of embedded systems applications. This port is commonly referred to as a 16 bit PC/104 port. The pinout of this port is detailed in Section 7.1. The connector is a 64 pin (32x2) socket connector and a 40 pin (20x2) socket. Basically the signals are the same as for the 16-bit (AT) ISA connector with the addition of two ground pins on each connector (A32, B32, C0 and D0).

A brief description of the PC/104 daughter boards:

- Form factor of 3.6" by 3.8".
- Self-stacking bus.
- Minimum power consumption (typically 1-2 Watts per board).
- Bus drive on most signals of 4mA.

The 301's PC/104 port is intended for use by customers who need additional peripheral functions, such as a video controller, internal modem, network card, etc. without using a passive backplane.

#### 5.1.1 PC/104 Module Dimensions and Bus Options

There are several different variations of PC/104 modules. The modules that are intended for use on the 301 are the 8 or 16 bit bus type. A detailed mechanical drawing of the board is provided on the next page. The 301 uses the "stackthrough" type of modules. The height between stacked modules is 0.6". Spacing between the 301 to the first PC/104 piggyback module is also 0.6". Mounting holes (0.125" dia.) are provided for the PC/104 module spacers.

A PC/104 stackthrough module is a module which has a female connector on one side of the board and a male connector on the other side. This enables the module to be connected to the 301 and another module can be connected to the first. A PC/104 non-stackthrough module is a module with only the female connector.

## Section 5: EXPANSION PORTS

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### 5.1 PC/104 EXPANSION PORT (J9 & J10)

#### 5.1.1 PC/104 16-Bit Module Dimensions

## Section 6: FLASH FILE SYSTEM

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### 6.0 OVERVIEW

The 301's Flash File System is a software package that makes a FLASH or SRAM memory Solid State Disk work just like a regular rotating disk drive. DOS commands like copy, delete, and rename will all work on a Flash File System Solid State Disk drive. Additionally, application programs can read and write files just like they do rotating disk drives. The utility to install the Flash File System is named FFS.EXE.

### 6.1 SEQUENCE OF STEPS

1. Configure the 301's jumpers for your application, refer to Section 2.2. Then install the 301 board in a system and connect a disk drive to it. The disk drive is only needed to initialize the Solid State Disk, it may be removed after initialization.
2. Select the drive and directory where the Flash File System utilities reside. Type FFS <enter> to run the Flash File System installation utility.
3. Pull down the CONFIGURATION Menu item and select the SET-UP option. Make the necessary changes to SET-UP to match your board's configuration.
4. Select the INSTALL option from the main menu.
5. Select the installation method you desire. If you wish to emulate a bootable Drive A, then you must use the **Floppy Drive** method. The **Device Driver** method requires that you have a bootable rotating disk drive in the final system. If you wish to emulate a hard drive, select the **Hard Drive** method. An emulated hard drive designated as C can be bootable. The Flash File System is automatically activated after reset for the **Floppy Drive** and **Hard Drive** methods. For the **Device Driver** method the Flash File System is user activated.
6. Select the FORMAT option from the main menu to format the emulated drive designated in the INSTALL option.
7. Re-boot the system after formatting is complete to activate all the emulated drives.
8. Copy any files desired to the Solid State Disk.

## Section 6: FLASH FILE SYSTEM

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### 6.2 FFS INSTALLATION MENUS

To install the Flash File System type **FFS** <enter> from the directory where the utilities reside. The Flash File utility has three main menu items: CONFIGURATION, INSTALL, and FORMAT. Each of these is explained in the following sections. While running the FFS.EXE installation utility **F1** will display help screens and **ESC** will exit the current screen.

#### 6.2.1 Menu Item - CONFIGURATION

The CONFIGURATION menu item contains several sub-menus. The purpose of the CONFIGURATION section is to assist the user in configuring the software settings to coincide with the hardware settings.

**PROCEDURE:** A step-by-step guide to configuring the Solid State Disk, installing the Flash File System and formatting the Solid State Disk Drive(s).

**AUTO STEP:** The auto step option will automatically guide you to each screen necessary to complete the process of installing the Flash File System. Auto step will continue to the next process unless you abort one of the steps along the way.

**CURRENT:** Displays the current software settings for: number of drives to emulate, emulated drive letters (for Floppy and Hard Drive methods only), number of FLASH chips and the number of SRAM chips.

**NOTE:** This option does not read the actual jumper settings. It displays the software settings. The user must verify that the hardware settings and the software settings are the same.

**SETUP:** Setup the software settings for the Emulated Drive type (Floppy or Hard), size and type of memory chips and drive letter designation.

When using the sub-menu SETUP, the first selection box prompts the user to select the type of Drive Emulation, Floppy or Hard drive. The next prompt is for selecting the number of Solid State Disk drives. The third prompt is for the emulated drive letter assignment, the possible selections for this depends on the drive type and number of drives selected. For Hard drive emulation the drive assignment is automatically determined. For example, if your system does not contain an actual hard drive the emulated hard drives will be assigned the letters C and D.

## Section 6: FLASH FILE SYSTEM

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### 6.2 FFS INSTALLATION MENUS

#### 6.2.1 Menu Item - CONFIGURATION

**SETUP:** For floppy drive emulation of one drive the selections will be A, B, C and D. When emulating two floppy drives the selections will be: A-B, B-C or C-D. For the Device Driver configuration the next available drive letters will be used automatically. The fourth prompt is for selecting the type of chip in the Solid State Disk drive designated as Drive 2 (FLASH or SRAM). The fifth prompt is for selecting the number of chips installed in the Solid State Disk drive designated as Drive 1.

**NOTE:** Drive 1 will always be considered the FLASH drive. Drive 2 may be SRAM or FLASH.

The Configuration settings may be saved in a file by pressing the <F2> key. Using the <Esc> key exits this menu without saving the file.

#### 6.2.2 Menu Item - INSTALL

Once the board jumper and software configuration settings have been made, installation is the next step in enabling the Flash File System. First, the user is prompted to select between the Floppy Drive, Hard Drive and Device Driver methods of installation.

**NOTE:** The Floppy Drive or Hard Drive methods are the methods most people will want to use.

#### Floppy Drive

When the Flash File System is installed as a Floppy Drive the driver software is stored in the first 32k of the first FLASH chip. With this method of installation the Solid State Disk Drives look like floppy disk drives to the system. Floppy drive commands must be used to talk to the Solid State Disk. When emulating a floppy disk drive a bootable Solid State Disk must be designated as Drive A. Benefits of the Floppy Drive method of installation are: The driver software is recognized and loaded as a BIOS extension and there does not have to be any rotating disks in the system.

When the Floppy Drive method is selected, an information box shows the progression of the function. The FLASH memory is erased and programmed with the configuration values currently selected. The Flash File System is then automatically activated and you can proceed to the format option.

## Section 6: FLASH FILE SYSTEM

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### 6.2 FFS INSTALLATION MENUS

#### 6.2.2 Menu Item - INSTALL

##### Device Driver

When the Flash File System is installed as a Device Driver, a Device Driver statement must be inserted into the system's Config.Sys file. Features of the Device Driver method of installation are: You must have a rotating disk drive in the final system to boot from (the Solid State Disk Drives can not be made bootable) and it is easy to disable the Solid State Disk Drives by removing the Device Driver statement from the Config.sys file.

The Flash File System utilities will insert the Device Driver statement into the Config.sys file for you. First, the system will prompt the user for the drive where the Config.Sys file resides. Next, the path where the Flash File System utilities reside is needed. When the system's Config.Sys file is changed, the original Config.Sys file will be saved in a file called Config.FFS. Once the Config.Sys file is modified you may choose to activate the FFS and proceed to the format option.

Upon boot-up, the Device Driver within the Config.Sys file displays the emulated drive parameters. Most of the parameters were designated in the SET-UP menu option, but the drive labels were DOS generated. You need to note the Drive 1 and/or Drive 2 label assignments the system made. (A, B, C, D, etc.)

##### Hard Drive

When the Hard Drive method is selected, the driver software is stored in the first 32k of the first FLASH chip. With this method of installation the Solid State Disk Drives look like Hard Disk drives to the system. Hard Drive commands must be used to talk to the Solid State Disk. A bootable Solid State Disk must be designated as Drive C. Benefits of the Hard Drive method of installation are: The driver software is recognized and loaded as a BIOS extension and there does not have to be any rotating disks in the system.

When the Hard Drive method is selected, an information box shows the progression of the installation. The FLASH memory is erased and programmed with the configuration values currently selected. The Flash File System is automatically activated and you can proceed to the format option.

### 6.2 FFS INSTALLATION MENUS

#### 6.2.2 Menu Item - Install

**NOTE:** The drive assignments made at this time may be different than the ones you have specified. The temporary assignments are made so they will not interfere with your current hard drive assignments. By using the temporary drive assignments, you will be able to format the emulated hard drive and copy any necessary files to it. Make note of the temporary assignments and format the emulated hard drive(s) using these letters. The correct drive assignments will be made when you reboot the system. Complete Hard Drive Emulation is achieved after the format is completed and the system has been rebooted.

#### 6.2.3 Menu Item - FORMAT

The FORMAT function is the final step in enabling the FLASH File System. After the emulated drive(s) are formatted, normal rotating disk drive handling is possible. If your configuration has two Solid State Drives, you need to do the FORMAT procedure twice, once for each drive.

The first drive (Drive 1) is always the FLASH drive. Drive 2 may be FLASH or SRAM. A volume label may be selected, but is optional. The Format Information screen outlines your selections. Once the FORMAT function is initiated, the procedure will take 10 to 30 seconds to complete depending upon the your system speed and the FLASH chip size. The FORMAT utility does not display any error messages.

**Caution:**

If the drive formatting appears to be done instantly, it is likely that the drive did not format.

### 6.3 FLASH FILE ERROR CODES

The following is a list of Flash File System error codes and their meanings:

- Error 01: Cannot locate address for emulated drives (i.e. cannot find the board)
- Error 02: FLASH write past memory limit
- Error 03: FLASH write past memory limit
- Error 04: Cannot read status byte for chip type verification
- Error 05: Chip not properly erased
- Error 06: Chip not properly erased
- Error 07: FLASH read past memory limit
- Error 08: FLASH erasure failed - verify correct configuration setup or possible corrupted chip
- Error 09: BIOS extension header erasure failed - verify correct configuration setup or possible corrupted chip
- Error 10: The Image File selected 'filename' was not found in the current directory
- Error 11: BIOS extension header programming failed - verify for correct configuration
- Error 99: Flash File System was not purchased for this board.

### 6.4 ERASE FLASH

The Flash File System utility provides the ability to erase the FLASH memory chips. Normally the user does not need to worry about erasing the FLASH chips, since the installation utilities automatically do any erasing that is needed. If you are changing the installation method from the Floppy or Hard drive method to the Device Driver method, then it is necessary to perform the ERASE FLASH function to eliminate the BIOS extension that resides in the first 32K of the first FLASH chip.

The ERASE function will erase all FLASH devices in the designated Solid State Disk drive when selected, without damaging the Flash File System's initialization.

## Section 6: FLASH FILE SYSTEM

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### 6.5 DRIVE STORAGE CAPACITY

The amount of memory the Flash File System uses, varies with the size and number of FLASH chips in a Solid State Disk Drive.

Using 2Meg (29F016) FLASH chips, the system has 128K of overhead, when using one of the BIOS extension methods and 64K of overhead when using the Device Driver method. The overhead is 8K for all SRAM configurations.

#### Drive Storage Capacity for Floppy and Hard Drive methods

Number of chips in Drive	Drive uses 29F016 (2Meg)chips	Drive uses 512K SRAM chips
1	1870K	504K
2	3868K	N/A
3	5866K	N/A

#### Drive Storage Capacity for Device Driver method

Number of chips in Drive	Drive uses 29F016 (2Meg)	Drive uses 512K SRAM chips
1	1934K	504K
2	3932K	N/A
3	5930K	N/A

## Section 7: APPENDICES

### 7.1 PC/104 EXPANSION PORT PINOUT J9 & J10

This is a standard 16 bit PC/104 expansion connector. It allows a daughter board to be attached to the Model 301. The signals are the same as for a 16 bit (XT) ISA bus connector, with four additional pins. Pins A32, B32, C0 and D0 are added as additional grounds.

Signal	Pin Number	Pin Number	Signal
//OCHCK	> A1	B1	Ground
SD7	<> A2	B2	> RESETDR
SD6	<> A3	B3	+5 Volts
SD5	<> A4	B4	< IRQ9
SD4	<> A5	B5	-5 Volts
SD3	<> A6	B6	< DRQ2
SD2	<> A7	B7	-12 Volts
SD1	<> A8	B8	< /OWS
SD0	<> A9	B9	+12 Volts
I/O CHRDY	> A10	B10	Ground
AEN	< A11	B11	> /SMEMW
SA19	<> A12	B12	> /SMEMR
SA18	<> A13	B13	<> //IOW
SA17	<> A14	B14	<> //IOR
SA16	<> A15	B15	> /DACK3
SA15	<> A16	B16	< DRQ3
SA14	<> A17	B17	> /DACK1
SA13	<> A18	B18	< DRQ1
SA12	<> A19	B19	> /DACK0
SA11	<> A20	B20	> CLK
SA10	<> A21	B21	< IRQ7
SA9	<> A22	B22	< IRQ6
SA8	<> A23	B23	< IRQ5
SA7	<> A24	B24	< IRQ4
SA6	<> A25	B25	< IRQ3
SA5	<> A26	B26	> DACK2
SA4	<> A27	B27	> T/C
SA3	<> A28	B28	> BALE
SA2	<> A29	B29	+5 Volts
SA1	<> A30	B30	> OSC
SA0	<> A31	B31	Ground
Ground	A32	B32	Ground

## Section 7: APPENDICES

### 7.1 PC/104 EXPANSION PORT PINOUT J9 & J10

Ground	D0	C0	Ground
/MEMCS16	< D1	C1	< /SBHE
/IOCS16	< D2	C2	<> LA23
IRQ10	< D3	C3	<> LA22
IRQ11	< D4	C4	<> LA21
IRQ12	< D5	C5	<> LA20
IRQ15	< D6	C6	<> LA19
IRQ14	< D7	C7	<> LA18
/DACK0	> D8	C8	<> LA17
DRQ0	< D9	C9	< /MEMR
/DACK5	> D10	C10	< /MEMW
DRQ5	< D11	C11	<> SD8
/DACK6	> D12	C12	<> SD9
DRQ6	< D13	C13	<> SD10
/DACK7	> D14	C14	<> SD11
DRQ7	< D15	C15	<> SD12
+5 Volts	D16	C16	<> SD13
/MASTER	< D17	C17	<> SD14
Ground	D18	C18	<> SD15
Ground	D19	C19	*KEY*

**NOTE:** Where: <> is a bidirectional signal;  
 >Bxx is an input; <Bxx is an output;  
 Axx< is an input; Axx> is an output;

7.2 MECHANICAL DRAWING

**7.3 POST CODES (During normal ROM scan)**

The POST (Power On Self Test) routines are performed each time the system is powered on. The purpose of these routines is to detect system errors. During the POST, the BIOS signals a checkpoint by outputting a code to I/O address 80H. This code can be used to establish how far the BIOS has executed through the power on sequence and what test is currently being performed. This is done to help to troubleshoot faulty boards.

If the BIOS detects a fatal error condition, it will halt the POST process and attempt to display the checkpoint code on the monitor screen. The checkpoint code written to the screen will match the code written to port 80H. The code will be written repeatedly to the screen which may cause "hash" on some systems.

If the system hangs before the BIOS detects the fatal error, the value at port 80H will be the test being performed. In this case the fatal error cannot be displayed on the screen.

The following is a list of the checkpoint codes which are written before their respective tests:

<u>Check Point</u>	<u>Check Point Description</u>
02	CPU Flag test
04	CPU Register test
06	System hardware initialization
08	Initialize chip set registers
0A	BIOS ROM checksum
0C	DMA page register test
0E	8254 timer test
10	8254 timer initialization
12	8237 DMA controller test
14	8237 DMA initialization
16	Initialize 8259/Reset coprocessor
18	8259 interrupt controller test
1A	Memory refresh test
1C	Base 64KB address test
1E	Base 64KB memory test
20	Base 64KB test (upper 16 bits)
22	8742 Keyboard self test
24	MC146818 CMOS test
26	Verify/Load NVRAM Parameters
28	Start first protected mode test
2A	Memory Sizing test/AutoSize memory chips
2C	Chip interleave enable test
2E	First protected mode test exit
30	Unexpected shutdown
32	System board memory size
34	Relocate shadow ram if configured
36	Configure EMS system
38	Configure wait states

## Section 7: APPENDICES

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### 7.3 POST CODES (During normal ROM scan)

<u>Check Point</u>	<u>Check Point Description</u>
3A	Retest 64K base ram
3C	CPU speed calculation
3E	Get switches from 8042
40	Configure CPU speed
42	Initialize interrupt vectors
44	Verify video configuration
46	Initialize video system
48	Test for unexpected interrupts
4A	Start second protected mode test
4C	Verify LDT instruction
4E	Verify TR instruction
50	Verify LSL instruction
52	Verify LAR instruction
54	Verify VERR instruction
56	Unexpected exception
58	Address line 20 test
5A	Keyboard ready test
5C	Determine AT or XT keyboard
5E	Start third protected mode test
60	Base memory test
62	Base memory address test
64	Shadow memory test
66	Extended memory test
68	Extended address test
6A	Determine memory size
6C	Display error messages
6E	Copy BIOS to shadow memory
70	8254 clock test
72	MC146818 real time clock test
74	Keyboard stuck key test
76	Initialize hardware interrupt vectors
78	Math Coprocessor test
7A	Determine COM ports available
7C	Determine LPT ports available
7E	Initialize BIOS data area
80	Determine floppy/fixed controller
82	Floppy disk test
84	Fixed disk test
86	External ROM scan
88	System key lock test
8A	Wait for FI key pressed
8C	Final system initialization
8E	Interrupt 19 boot loader
B0	Unexpected/Unknown interrupt occurred

## Section 7: APPENDICES

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### 7.4 BEEP CODE (During normal ROM scan)

The audible error generated during POST is one long tone followed by a two short tones. This audible error will result from either a failing video configuration (no card installed or faulty video card) or an invalid external ROM module that does not properly checksum to zero. Any other audible errors consisting of one long tone followed by a series of short tones will be from an external BIOS extension ROM (e.g. VGA).