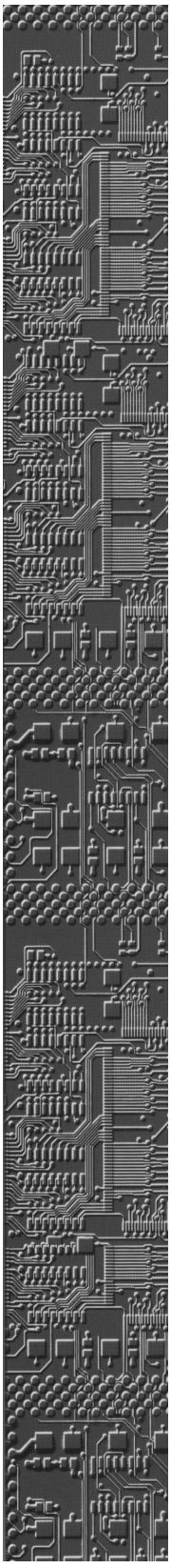

TEKNOR
INDUSTRIAL COMPUTERS INC.

PCI-943

Pentium II/III - SECC 2/3 SBC

TECHNICAL REFERENCE MANUAL **VERSION 1.1**
April 1999

ref.: M943_1.1

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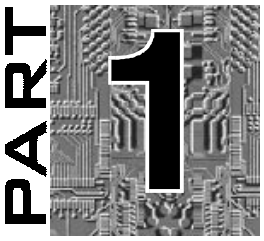


PRODUCT DESCRIPTION

1. PRODUCT OVERVIEW

The PCI-943 PCI-ISA full-featured, full-sized single board computer is based on the Intel Pentium® II SECC Pentium® III SECC 2 (Single Edge Contact Cartridge) processor, the Intel 440BX chipset and the Chips & Tech B69000 CRT video interface with 2MB embedded video memory (SDRAM) and AGP (Accelerated Graphics Port) interface.

The PCI-943 board provides a flush-mounted design that allows you to use all your ISA backplane slots (whether or not all your PCI slots can be used will depend on your particular PICMG PCI-ISA backplane). Flush-mounting withstands higher shocks and vibration and has better thermal characteristics than the usual edge mounted design.

The board provides:

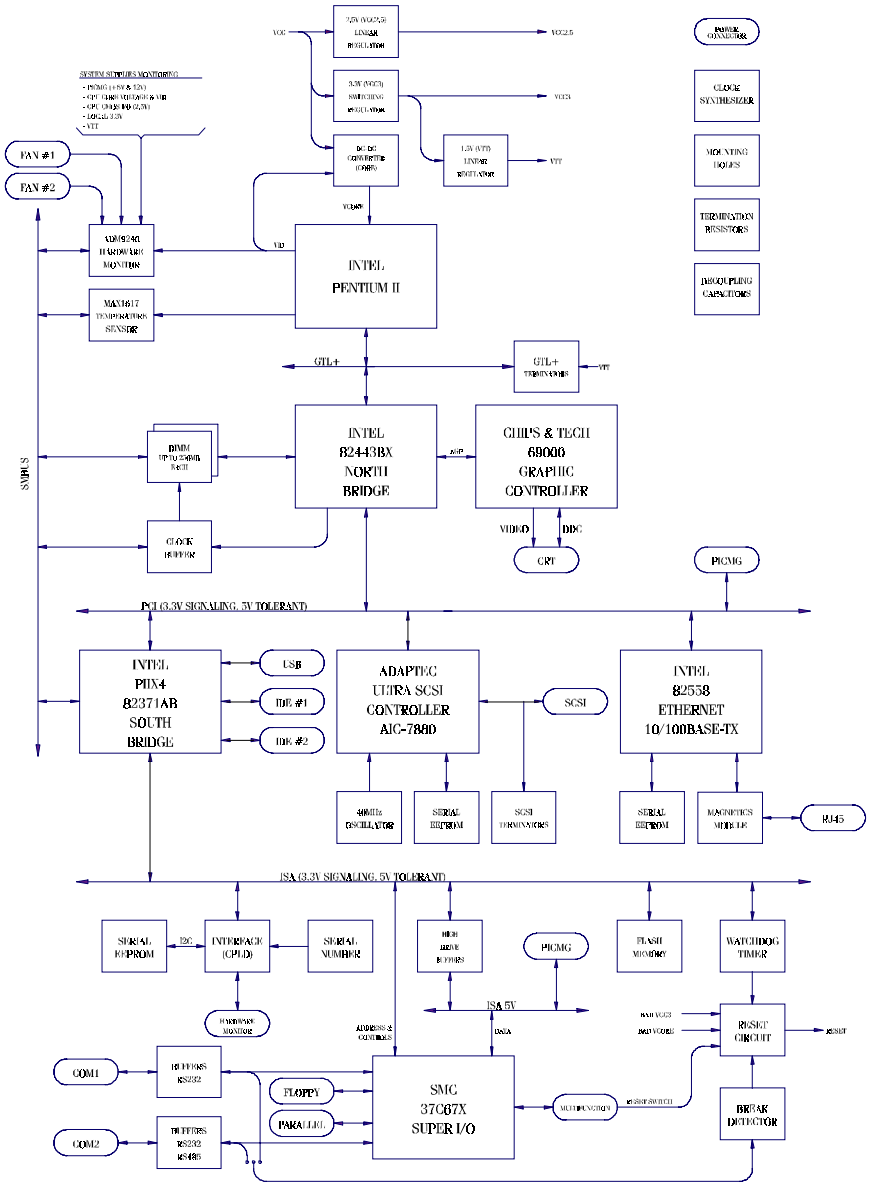
. Support for the Pentium II SECC processor at 350, 400, and 450MHz
. Up to 512MB of SDRAM shared on two 168-pin DIMM sockets
. 512KB of L2 cache memory
. PCI 10Base-T/100Base-TX Ethernet
. PCI Wide-Ultra SCSI
. Floppy controller
. Dual EIDE Ultra DMA/33 interface
. USB 1.0 port supporting two connectors with optional cable/assembly bracket
. Two serial ports, parallel port, speaker port, mouse port and keyboard port.

It plugs into a PICMG PCI-ISA passive backplane and provides 100% PC compatibility for system expansion slots.

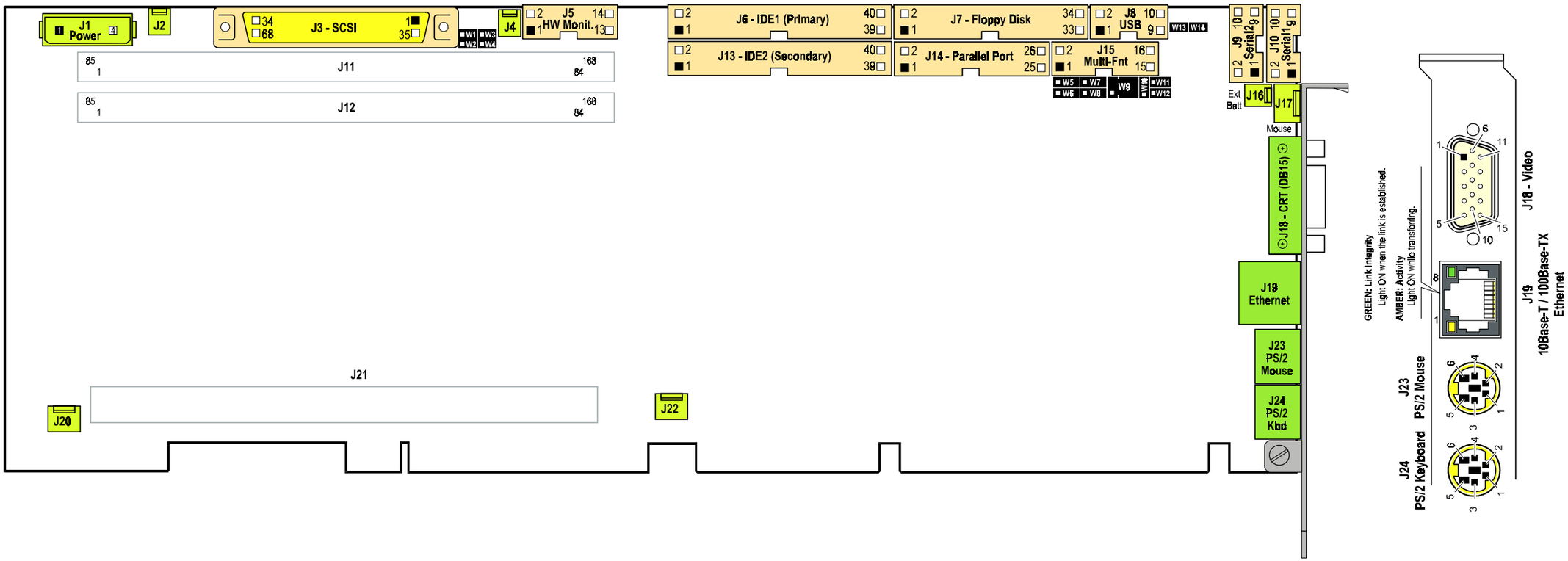
The SBC and backplane assembly is used as a substitute for the standard PC motherboard, and in general includes all of the standard interfaces and peripherals that are normally included in a top of the line PC. This compact solution allows an industrial user the possibililty of designing a system that uses standard x86 software and peripherals, but in an industrial environment where reliability, integration and service are of major concern.

2. FEATURE DESCRIPTIONS

PCI-943: Block Diagram



PCI-943 Connector and Jumper Locations



2.1 SYSTEM CORE

2.1.1 Processors

The Pentium® II SECC processor and its dual-fan cooling assembly are factory installed. The speed of the processor is preset to its nominal value (maximum internal speed).

Related Jumpers

W2 CPU Core Frequency Configuration Mode
W6 CPU Front Side Bus Speed
Setups are described in Section 5 – *Setting Jumpers*

BIOS Setups

See Section 6-13: *AWARD Setup Program, CPU/Board Features Setup* option

---

The processor must be mounted to the board using the J21 connector. Two fan connectors are provided to provide the power voltage to the dual-fan cooling assembly: they are referred to as J20 and J22 and are independently fused.

The CPU Core Frequency Configuration Mode (W2 jumper installed) is a hardware configuration method which forces the processor(s) to run at twice the Front Side Bus (FSB) speed (66MHz or 100MHz). This mode will be helpful to boot the board and run the BIOS Setup program after you have installed a new processor.
The new processor speed values must be set using the *CPU/Board Features Setup - Current Processor(s) Speed* option (Section 6-13).

Once the new parameters have been saved, exit the AWARD Setup program, power off the board, remove the W2 jumper and reboot the system for the new processor speed to take effect.

⚠ **CAUTION**

Setting the processor(s) speed, in AWARD's CPU/Board Features Setup, higher than the nominal speed (maximum internal speed) may cause damage to the processor(s).

2.1.2 Memory

The board supports up to 512MB of 64/72-bit Synchronous DRAM (SDRAM) divided up into two DIMM sockets (J11, J12).

Related Jumpers
None

BIOS Setups
See 6-8 - *AWARD Setup Program, Chipset Features Setup* option

The following SDRAM modules are supported:

- 16MB (2Mx64 or 2Mx72)
- 32MB (4Mx64 or 4Mx72)
- 64MB (8Mx64 or 8Mx72)
- 128MB (16Mx64 or 16Mx72)
- 256MB (32Mx64 or 32Mx72)

NOTE

The total size of the system memory available on the board is equal to the sum of the memory module sizes installed in the DIMM sockets.

The SDRAM DIMMs must conform to the following:

- 3.3V only, single-sided or double-sided.
- Unbuffered 100 MHz SDRAM.
- Serial Presence Detect (SPD) EEPROM.
- 64-bit and 72-bit DIMMs.
- Error Checking and Correction (ECC) or parity bit, with 72-bit DIMMs.
- Compliance with Intel's PC-100 SDRAM unbuffered DIMM specification, Rev. 1.0.

The list of tested DIMM devices is provided below. Many other models are available and function equally well. Users are encouraged to check with their local distributors for comparable substitutes.

DIMM	VENDOR	PART NUMBER
16MB (2M*72) SDRAM 100MHz	CENTON	CINT16M/P100S1
32MB (4M*72) SDRAM 100MHz	CENTON	CINT32M/P100S1
64MB (8M*72) SDRAM 100MHz	CENTON	CINT64M/P100S1
128MB (16M*72) SDRAM 100MHz	CENTON	CINT128M/P100S1
256MB (32M*72) SDRAM 100MHz	CENTON	CINT256M/P100S1

Installation

- On an anti-static plane, place the board so that you are facing the DIMM sockets (the edge bracket must be located on the right).
- Insert the DIMM into the socket, aligning the keys on the module with the socket's key inserts.
- Push vertically the DIMM into the socket until the retaining clips on each side snap on. Repeat these steps to populate the other sockets.

To remove a DIMM from a socket, push down the retaining clips on each side of the socket, to release the module. Pull the module upward to remove.

2.1.3 Battery

The battery is required to keep the BIOS settings and the real-time clock stored into the CMOS RAM. The board is shipped from factory with the battery electrically disconnected from the board. Prior to first powering the board, the battery must be connected using the W5 Battery jumper.

Related Jumpers
W5: Onboard Battery
Setups are described in Section 5 – *Setting Jumpers*

BIOS Settings
None

The battery specifications are as follows:

- 3.6V Lithium battery, 0.37A/h

Installation

Connect the battery to the B1 header. The positive pin of the battery is located at the center.

The onboard battery power can be replaced by an external power source by connecting a 3.6V power to the J16 External Battery connector, W5 jumper must be set to position 2-3.

2.2 ETHERNET

The Ethernet interface is available through the J19 RJ-45 connector located on the edge bracket.

The 10MBps or 100MBps (10Base-T, 100Base-Tx) network speed is automatically detected and selected.

Related Jumpers
None

BIOS Settings
The onboard Ethernet feature is enabled by default.
To change settings, see Section 6-14: *AWARD Setup Program, Integrated Peripherals* option

---

The 10Base-T interface uses UTP (Unshielded Twisted Pair) cables, category 5, 4 or 3 (5 is better) while the 100Base-TX interface uses only category 5 UTP cables.

NOTE

The board is capable of booting from LAN by enabling this function using the BIOS Setup Program, *BIOS Features Setups*, *Boot From LAN First* option.

The Ethernet controller has specific drivers for various operating systems and software. To install these drivers, refer to the Utility Disk containing the Ethernet drivers for your operating system (more detail in Section 8 - *Installing Drivers*).

2.3 I/O DEVICES

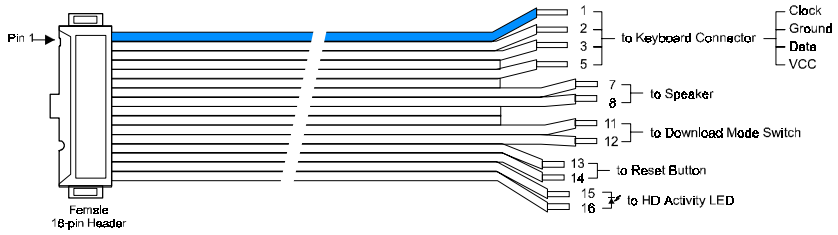
2.3.1 I/O Connections

Standard AT keyboard, speaker port, reset button and hard disk LED signals are issued on the J15 Multi-Function header.
A 22" keyboard flat cable (TEKNOR part number 150-018-01) is provided with the board for connecting the respective devices.

Related Jumpers
None

BIOS Settings
None

Signals on the flat cable are issued as follows:



2.3.2 Keyboard

The simplest way to connect a PS/2 keyboard to the board is to use the J24 standard PS/2 keyboard connector on the edge bracket. No additional cabling is required.

Related Jumpers
None

BIOS Settings
To setup keyboard typematic features, refer to Section 6-6: *AWARD Setup Program, BIOS Features Setup* option

CAUTION

While it is also possible to connect a keyboard through the Multi-function header (J15), do not connect two keyboards simultaneously to the board. This can damage the keyboard interface.

2.3.3 PS/2 Mouse

The simplest way to connect a PS/2 mouse to the board is to use the J23 standard PS/2 mouse connector on the edge bracket. No additional cabling is required.

Related Jumpers
None

BIOS Settings
To enable automatically the PS/2 mouse when installed, refer to Section 6-14: *AWARD Setup Program, Integrated Peripherals* option

A PS/2 mouse header (J17) is also provided onboard. To connect a mouse through this header, a shielded PS/2 mouse adapter cable is required. It is available from TEKNOR as 18" shielded mouse cable, part number 150-337-00.

CAUTION

While it is also possible to connect a keyboard through the J17, PS/2 Mouse header, do not connect two PS/2 mice simultaneously to the board. This can damage the keyboard interface.

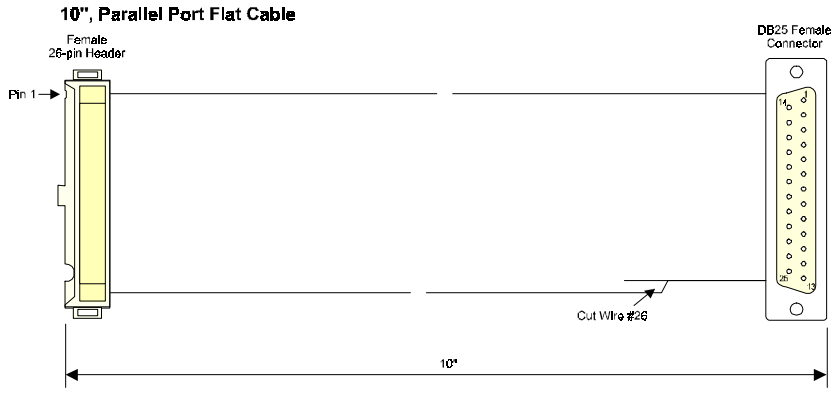
2.4 PARALLEL PORT

The Parallel Port is available through the J14 26-pin connector. It is bi-directional and supports the standard, EPP and ECP operating modes.

Related Jumpers
None

BIOS Settings
To setup the Parallel Port, refer to Section 6-14: *AWARD Setup Program, Integrated Peripherals* option

The usual way to use the parallel port is to issue signals from the J14 26-pin connector to a standard 25-pin D-Sub connector using an adapter cable. Such a cable is available from TEKNOR (Part Number: 150-172). One is provided with your board.



2.5 POWER SUPPLY

The main power supply can be drawn to the board using the J1 Power connector or through the edge connector, from the backplane to which it can be connected. If more power is required it is also possible to combine both power sources.

Related Jumpers
None

BIOS Settings
See Power Management options described in Section 6-10: *AWARD Setup Program, Power Management* option

The power requirements are specified as follows:

	Pentium II			Pentium III	
	350	**400**	**450**	**450**	**500**
Icc Typ. +5V	5.06A	5.64A	5.80A	5.82A	6.24A
Icc Susp. +5V	3.24A	3.49A	3.56A	3.64A	3.69A
+12V	200mA	200mA	200mA	200mA	200mA
Measured with 64MB DRAM, keyboard, floppy disk, and hard disk.					

2.6 REMOTE RESET

A remote hardware reset of the PCI-943 is possible by sending a break on the Serial Port 1 or Serial Port 2 (depending on W7 jumper setting). A break is simply an abnormally long start bit (100ms or more) on the incoming data line. A break signal is embedded in the data, so no special wire is required.

Related Jumpers

W7 to select whether the serial port 1 or 2 is used to control the remote reset

BIOS Settings

To provide a hardware reset through the Serial Port 2, it must be set for RS-232 or RS-422 modes. Refer to Section 6-14: *AWARD Setup Program, Integrated Peripherals* option

The remote reset will work in RS-232 and RS-422 modes. It will also work with a modem, since the modem will repeat the break signal over the telephone network. All major telecommunication software have the capability of sending a break signal, usually by pressing the CTRL-B keys or the ALT-B keys on the keyboard. Only a standard telephone line and a modem in auto-answer mode are needed. The only limitation is that the communication speed must be 1200bps or more. If the communication speed is too slow, a false reset can occur.

The break signal is entirely detected by hardware. The processor can be dead and buried and the break detector will still work.

Since the remote reset has the same function as the push button reset, it is considered the same by the reset history circuit which is described in Section 3 – *Registerx92h*.

For truly remote operation, use the VT100 mode, which allows remote BIOS setup and console redirection (see Section 21).

2.7 SERIAL PORTS

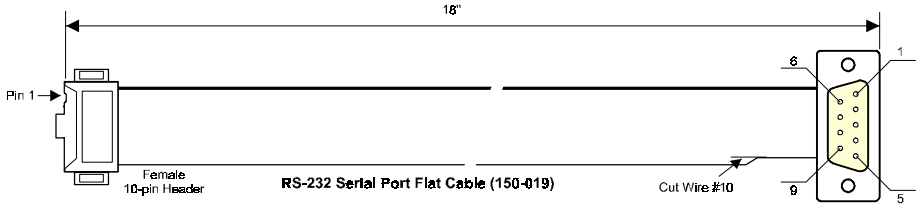
2.7.1 Serial Port 1

The Serial Port 1 is available through the J10, 10-pin connector and supports RS-232 operation mode.

Related Jumpers
None

BIOS Settings
To setup the Serial Port 1, refer to Section 6-14 – *AWARD Setup Program, Integrated Peripherals* option

The usual way to access to the serial port is to issue its signals through a 10-pin header/9-pin D-Sub adapter cable. An 18 inches 10-pin header/9-pin D-Sub adapter cable is available from TEKNOR: Part number 150-019. Two are provided with your board.



While adapter cables are provided form various sources, the pinout is often different. The direct crimp design offered by TEKNOR allows the simplest cable assembly. All cables are available from TEKNOR by contacting the Sales Department

2.7.2 Serial Port 2

The Serial Port 2 is available through the J9 10-pin connector, and support both RS-232 and RS-422/485 operation modes.

Related Jumpers

W13 and W14: to connect/disconnect Serial Port 2 termination resistors
Setups are described in Section 5 – *Setting Jumpers*

BIOS Settings

To setup the Serial Port 2, refer to Section 6-14: *AWARD Setup Program, Integrated Peripherals* option

The usual way to use the serial port, is to issue signals through a 10-pin header/9-pin D-Sub adapter cable (see description provided for the Serial Port 1).

RS-232 Mode

By default, the Serial Port 2 is configured for RS-232 operation mode. To change the operating mode, use the BIOS CMOS setup program – *Integrated Peripherals*.

RS-422/RS-485 Modes

Use the BIOS CMOS setup program, *Integrated Peripherals*, to select the operation mode within RS-232, RS-422 or RS-485.

In RS-422 and RS-485 modes, transmitting and receiving use differential signals in either full-duplex (RS-422) or party line (RS-485) communication.

Communicating with differential signals requires one pair of wires for RS-485 and two pairs for RS-422 (one for transmission, one for reception).

For a better noise rejection, the use of twisted pair cable is highly recommended. This will enable faster serial transmissions over greater distances than with the common RS-232 protocol.

If the board is installed at one end of the network and the Serial Port 2 is configured for communicating in RS-422 or RS-485 mode, use the W13 and W14 jumpers to connect the RS-485/RS-422 termination resistors (120 ohms) while the board is terminating the network.

RS-422 - Full Duplex Operation: The RS-422 protocol uses both RX and TX lines during a communication session. Upon power-up or reset, the Serial Port 2 interface circuits are automatically configured for full duplex operation. Pins 3 and 4 of J9 act as the receiver lines and pins 5 and 6 act as the transmitter lines.

In RS-422 mode, ¸the software should not use the handshake signals (e.g., DSR, DTR), since they are not connected. However, software handshaking can be used (e.g., XON-XOFF).

RS-485 - Party Line Operation: The RS-485 offers to multiple station the ability to transmit and receive over the same pair of wires (RX outputs: pins 3 and 4 of J11), and share the same communication line with multiple stations.

The RS-485 protocol offers some advantages such as increased speed over long distances, improved reliability over similar RS-232 setups, the ability to share transmission line, less cabling requirements than the RS-422 protocol.

In this configuration, only one system takes control of the communication at a time.

Upon power-up or reset, the transceiver is by default in "receiver mode" to avoid line perturbation.

2.8 STORAGE DEVICES

2.8.1 Floppy Disk Drives

Two floppy disk drive units can be connected to the board through the J7 Floppy Disk connector using a standard IBM 34-pin flat ribbon cable. An 18" floppy disk cable is available from TEKNOR: part number 150-051. One is provided with your board.

Related Jumpers

None

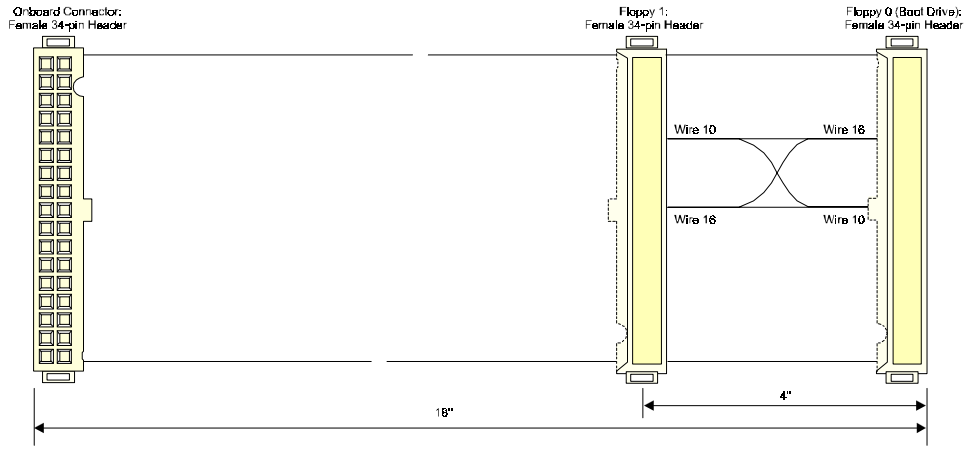
BIOS Settings

To define the Floppy Disk installation, refer to Section 6-5: *AWARD Setup Program, Standard CMOS Setup* option

To enable/disable the system to boot from the floppy disk A, refer to Section 6-6: *AWARD Setup Program, BIOS Feature Setup* option

---

The floppy disk cable is illustrated below:



2.8.2 IDE Devices

Two IDE interfaces are provided to support up to four IDE devices, such as CD-Rom, ZIP drives, and hard disks. The interfaces are referred to as Primary (J6 connector) and Secondary (J13 connector). Connections are supported through 40-pin dual row headers.

Related Jumpers

None

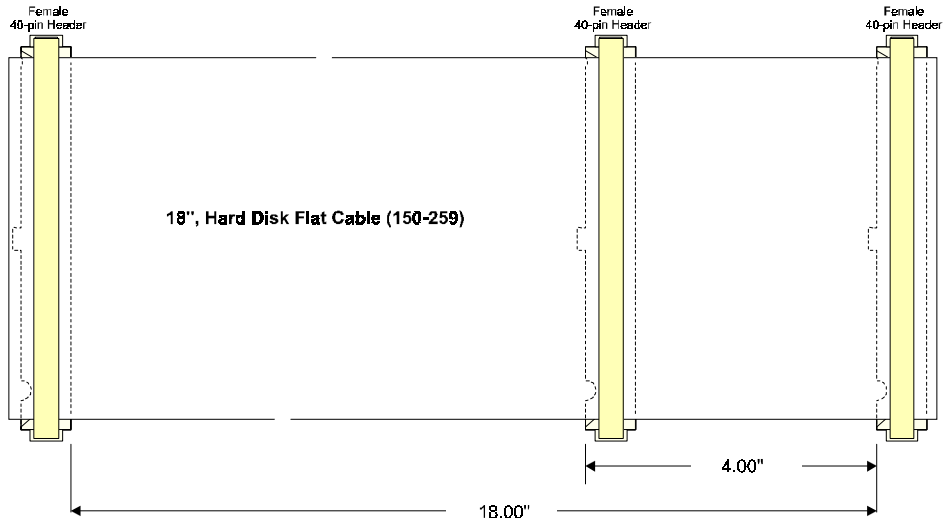
BIOS Settings

To detect a hard disk drive type, refer to Section 6-5: *AWARD Setup Program, Standard CMOS Setup* option

Setups are also available enable/disable the system to boot from the floppy disk A, refer to Section 6-6: *AWARD Setup Program, BIOS Feature Setup* option

To connect one IDE interface, use a 40-pin flat ribbon cable. An 18 inches length cable is available from TEKNOR: part number 150-259. One is provided with your board.

The cable is illustrated below:



2.8.3 SCSI Devices

SCSI devices must be connected to the PCI Wide-Ultra SCSI interface using a cable with 68-pin high-density connectors. Such a cable is available from TEKNOR (Part number: 150-371-00). One is provided with your board.

Related Jumpers

W4 to determine the SCSI mode (8-bit or 16-bit)
W6 to set the board as terminated or not
Setups are described in Section 5 – *Setting Jumpers*

BIOS Settings

The onboard SCSI interface is enabled by default.
To change setups, see Section 6-14: *AWARD Setup Program, Integrated Peripherals* option

---

The SCSI activity status signal is available through J2 (2-pin lock header). Connect the LED as follows: anode on pin 1 and cathode on pin 2. No external current limiting resistor is required since it is already present on the board (330 ohm resistor).

50-pin Fast SCSI and Fast-20 SCSI devices are also supported using a 68-pin to 50-pin adapter cable

NOTE

Ensure that the onboard SCSI controller is enabled in the AWARD BIOS Setup program, *Integrated Peripherals* option. By default, the SCSI feature is enabled, however, it may be disabled if an external SCSI card is required.

To boot from the SCSI device, please refer to the AWARD BIOS Setup program, *BIOS Features* option.

The Adaptec SCSISelect configuration software is provided with the board to configure or view the default SCSI settings of the host adapter (See Section 7 – *Configuring SCSI*). It replacdes the <Ctrl-A> feature on standard Adaptec controlers

The EZ-SCSI software is provided with the board to install the appropriate driver according to your specific operating system.

2.9 USB PORTS

The board provides a dual-USB interface through the J8 10-pin header. To connect standard USB devices, a USB cable/bracket assembly is required. It is available from TEKNOR: part number 150-316-00. One is provided with your board.

Related Jumpers

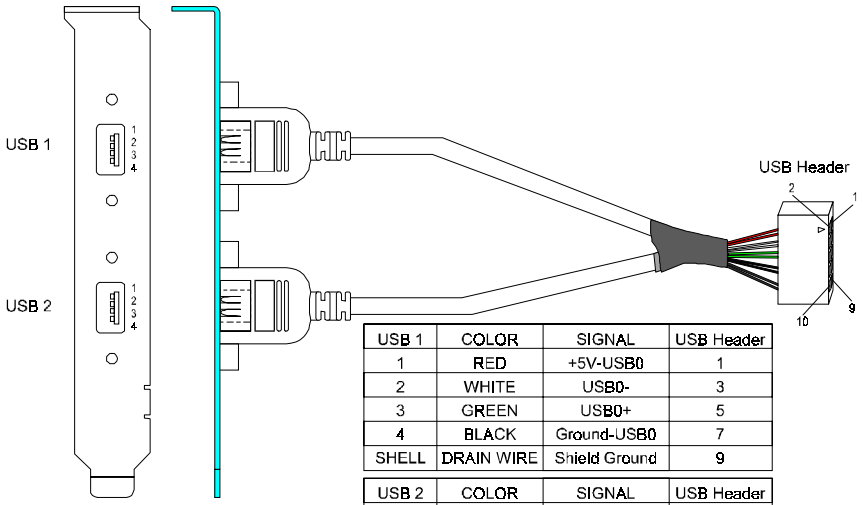
None

BIOS Settings

If required USB keyboard support for DOS and BIOS can be activated at the BIOS level.

Refer to Section 6-14: *AWARD Setup Program, Integrated Peripherals* option

The USB cable/bracket assembly is described as follows:



USB 1	COLOR	SIGNAL	USB Header
1	RED	+5V-USB0	1
2	WHITE	USB0-	3
3	GREEN	USB0+	5
4	BLACK	Ground-USB0	7
SHELL	DRAIN WIRE	Shield Ground	9

USB 2	COLOR	SIGNAL	USB Header
1	RED	+5V-USB1	2
2	WHITE	USB1-	4
3	GREEN	USB1+	6
4	BLACK	Ground-USB1	8
SHELL	DRAIN WIRE	Shield Ground	10

2.10 VIDEO FEATURES

The video onboard is CRT only. The CRT display connects directly to the J18 standard VGA 15-pin D-Sub connector located on the edge bracket.

Related Jumpers

W1 to enable or disable the AGP interface
W11 to enable or disable the onboard video controller
W12 to assign the PCI INTA to the onboard video controller
Setups are described in Section 5 – *Setting Jumpers*

BIOS Settings

Refer to Section 6-8: *AWARD Setup Program, Chipset Features* options for RAM cache and video BIOS shadow capabilities

When the PCI INTA is assigned to the video controller (W12 shorted), the video controller will issue an interrupt request signal when the end of an active field (VSYNC pulse to the CRT monitor) is reached.
By default the interrupt is disabled.

NOTE

Both W1 and W11 jumpers must be set together.

To enable the onboard video controller, ensure that both W1 (AGP) and W11 (video controller) jumpers are removed.

By default, the onboard video is enabled; however if an external video card is required for testing or other purposes, the controller can be disabled by shorting both W1 and W11 jumpers.

3. SUPERVISOR REGISTERS

The Supervisor Registers consist of six I/O registers provided for configuring and controlling special features of the board, such as the Analog Watchdog, the Programmable Watchdog and the Power Fail Detection.

These registers are 8-bit wide and can be located at three different I/O base addresses: 190h, 290h or 390h.

When setting Register x90h at one base address, all the other registers are located at the same base address plus one, two, three and so on. To select the base address, use the AWARD Chipset Features Setup.

This section includes a description of each I/O register and bit available for programming and configuring the PCI-943.

3.1 REGISTER X90H: SERIAL PORT

Bit	7	6	5	4	3	2	1	0
Reset				0	0	0		
Read				RS485	RS232	ST1		
Write				RS485	RS232	ST1		

Used by the BIOS during the POST only.

Serial port 2 configuration/use

ST1 Enable RTS2 to be used as 485TX enable when in 485 mode (1: enable, 0: disable).

RS232 Enable RS-232 mode for serial port 2 (1: enable, 0: disable).

RS485 Enable RS-422/RS-485 mode for serial port 2 (1: enable, 0: disable).

NOTE

The bits RS232 and RS485 are initialized by the BIOS during POST. If modification of these bits is required, be aware that there is a hardware protection so that RS232 and RS485 buffers cannot be activated at the same time. This protection is done at the register level. If you write to x90h register with bits 3 and 4 set, you will actually write 0 in both of these bits. This condition can be read back.

3.2 REGISTER X91H: RESET HISTORY & CPU FAULT

Bit	7	6	5	4	3	2	1	0
Reset				0				
Read	PBRES		WDO	CpuFlt				
Write				CpuFlt				

Used by the BIOS at runtime; do not write to this register.

Reset history

PBRES This bit is set when the push button reset is pressed and when a remote reset occurs. It is cleared at power-up and when the bit CLRHIS* is "0" (see register x92h).

WDO This bit is set when a reset is produced by the watchdog. It is cleared at power-up and when the bit CLRHIS* is "0" (see register x92h description).

Hardware monitoring

CpuFlt CPU Fault: When a "1" is written to CpuFlt, the corresponding pin on the monitor connector (CpuFlt*) is pulled to ground. The BIOS will report any system error by setting this bit to "1". The application software should leave this bit to the exclusive use of the BIOS for write but can read it as a general board status. The faults that will cause the activation of CpuFlt are:

- Overheating of the CPU detected through thermal sensor on the CPU.
- Overheating of the base board.
- Wrong voltage on CPU, 3.3V, 5V or 12V.
- CPU fan stopped (if fan speed monitoring is enabled in the BIOS setup).

* = Active low signal

3.3 REGISTER X92H: CLEARING RESET HISTORY & LOCK FOR WATCHDOG

Bit	7	6	5	4	3	2	1	0
Reset						1		1
Read						LOCK		CLRHIS*
Write						LOCK		CLRHIS*

Not used by the BIOS.

Reset history

CLRHIS* A 0-1 pulse will clear all reset history bits (see register x91h description in section 15.1.2). In normal operation, always keep the CLRHIS* bit to "1" otherwise the reset source will not be captured (the history latch are disabled when CLRHIS* is "0").

Programmable watchdog

LOCK When set, the state of the enable bit for the programmable watchdog (WDEN) cannot be changed.

* = Active low signal

3.4 REGISTER X93H: SILICON ID CHIP INTERFACE, LOCAL I²C, SYSTEM MONITOR CONNECTOR INTERFACE

Bit	7	6	5	4	3	2	1	0
Reset	1	1	1		1		1	1
Read	AppFlt	GPIO2 (pin)	GPIO1 (pin)		IDCHIP (pin)		SCL (pin)	SDA (pin)
Write	AppFlt	GPIO2 (reg.)	GPIO1 (reg.)		IDCHIP (reg.)		SCL (reg.)	SDA (reg.)

Not used by the BIOS.

Silicon ID chip

IDCHIP Used to read the onboard silicon serial number using the Dallas Semiconductor one-wire protocol.

User EEPROM

SCL/SDA Clock and data I²C link to user EEPROM.

Monitor connector interface

AppFlt Application Fault: When AppFlt is set, the corresponding pin on the system monitor connector (AppFlt*) is pulled to ground. The BIOS does not use this bit at all. Upon a reset, the bit is active (a reset is a fault). The end-user software has to clear this bit to "0" in order to remove the fault condition on the system monitor connector.

GPIO[2,1] General Purpose I/O. Open collector output with pin readback connected to the system monitor connector. Can be used to make an I²C link.

* = Active low signal

3.5 REGISTER X94H & X95H

These registers are reserved.

3.6 REGISTER X96H: PROGRAMMABLE WATCHDOG

Bit	7	6	5	4	3	2	1	0
Reset	0	1	1	1				
Read	WDEN	WDS2	WDS1	WDS0				
Write	WDEN	WDS2	WDS1	WDS0				

Not used by the BIOS.

WDEN When this bit is set, the programmable watchdog is enabled with the current timeout specified by WDS[2..0] (see dual-stage programmable watchdog description).
To avoid accidental deactivation of the watchdog, the bit WDEN is normally locked by the bit LOCK of register x92h (see register x92h description).

WDS[2..0] Timeout selection.

3.7 REGISTER X97H: NMI SOURCES & MASK

Bit	7	6	5	4	3	2	1	0
Reset	0		0		0		0	
Read	BatFltEn	BatFlt	FanFltEn	FanFlt	ExtFltEn	ExtFlt	WdNmiEn	WdNmi
Write	BatFltEn		FanFltEn		ExtFltEn		WdNmiEn	

Not used by BIOS.

WdNmi	Watchdog NMI: NMI from the Watchdog timeout.
WdNmiEn	Enable NMI from the Watchdog.
ExtFlt	External Fault: NMI from external source on the system monitor connector.
ExtFltEn	Enable NMI from ExtFlt.
FanFlt	Fan Fault: NMI from external fan motion detector on the system monitor connector.
FanFltEn	Enable NMI from FanFlt.
BatFlt	Battery Fault: NMI from power failure detection.
BatFltEn	Enable NMI from BatFlt.

All bits are active "1" regardless of the electrical state of the signal. Inversion is provided by the hardware when required. When an NMI source is enabled, the corresponding event is latched until the enable bit is cleared. When the enable bit is cleared, the status bit reflects the signal (not latched).

The NMI itself is generated through the IOCHK* signal. As a result, it can be monitored on the ISA backplane, and the NMI handler must reset the IOCHK* latch.

NOTE

When a watchdog NMI occurs, the CPU must trigger or disable the watchdog within 1ms or the watchdog will generate a master reset. Knowing that an NMI is the highest priority interrupt on the CPU, if the CPU cannot answer the NMI within 1ms then there is a major problem and the best thing to do is to reset everything. Normally, the CPU will answer the NMI and re-trigger the watchdog for the time it needs to shut down properly.

* = Active low signal

4. SUPERVISION FEATURES

4.1 WATCHDOG

The function of a watchdog is to reset the CPU board, if the processor is not able to generate a trigger for longer than the watchdog timeout period. This feature is useful in embedded systems where human supervision is not required or impossible.

The PCI-943 provides a two-stage digital watchdog with software programmable timeout period.

Following a reset of any source, the watchdog is disabled. The watchdog can be enabled by software.

4.1.1 Dual-stage Watchdog

Enabling the Programmable Watchdog

To enable the programmable watchdog, first unlock the enable bit by clearing the lock bit in register 0x92h, then set the bit WDEN in register x96h and re-lock it by setting the lock bit in register 0x92h. The following is an example in C language.

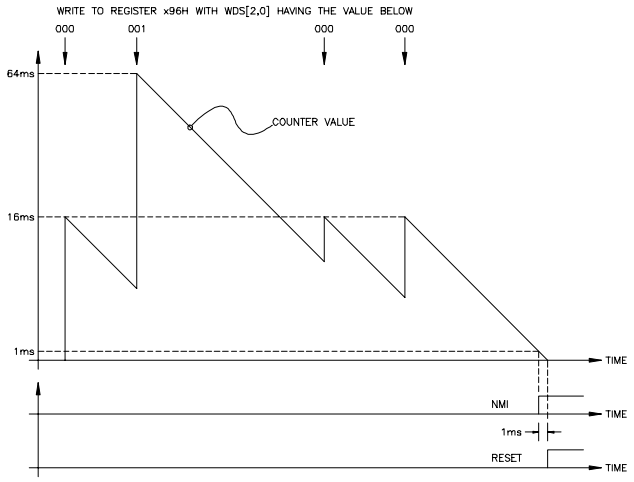
```
#define TekReg 0x190                // define base address (0x190, 0x290 or 0x390)

void ArmWatchdog(void)
{
   outp(TekReg+2,inp(TekReg+2) & 0xFB);        // unlock watchdog enable bit
   outp(TekReg+6,inp(TekReg+6) | 0xF0);        // enable & trigger at max timeout
   outp(TekReg+2,inp(TekReg+2) | 0x04);        // lock watchdog enable bit
}
```

Triggering the Programmable Watchdog

To trigger the programmable watchdog, the processor writes to register x96h. The action of writing to the register is the trigger and the value written to the register tells the watchdog the current timeout to use (see register x96h description). For a fixed timeout, the processor simply writes a constant in register x96h.

A variable refresh is possible as shown below:



The programmable watchdog can be viewed as a decrementing counter that is initialized by a write to register x96h. The processor must initialize the counter to prevent it from reaching count 0 (timeout).

The following C language procedure can be used to trigger the programmable watchdog.

```
#define TekReg 0x190                    // define base address (0x190, 0x290 or 0x390)
void TrigWatchdog(timeout)     // select timeout at runtime: 0x80, 0x90, 0xA0, ... 0xF0
{
   outp(TekReg+6,(inp(TekReg+6) & 0x0F) | (timeout & 0xF0));
}
```

Timeout

The programmable watchdog has two stages: the first stage has a variable timeout while the second stage has a fixed one.

The first stage timeout is chosen at runtime from eight preset values (see table below). The first stage timeout generates an NMI interrupt (if enabled in register x97h). An appropriate NMI handler must be written, otherwise this will be treated as a parity error by the default BIOS NMI handler; see register x97h description for a suggestion on how to this.

The second stage times-out 1ms after the first one and generates a master reset.

WDS[2,0]	NMI Timeout	RESET Timeout
000	0.016s	0.016s + 1ms
001	0.065s	0.065s + 1ms
010	0.261s	0.261s + 1ms
011	1.044s	1.044s + 1ms
100	4.174s	4.174s + 1ms
101	16.69s	16.69s + 1ms
110	66.79s	66.79s + 1ms
111	267.1s	267.1s + 1ms

The actual timeout values can be up to 20% longer than the values provided in the previous table, but they will not be shorter.

When the NMI is enabled, if the processor is still running and memory content is not corrupted, the processor can answer the NMI and trigger the watchdog again to gain time for a gracefull shutdown.

A reset from the programmable watchdog is latched for reset source identification; see reset history description in Section 4.3.

4.2 POWER FAILURE DETECTION

The board has many power failure detection features (* = active low signal):

1. It always monitors the +5V, +3.3V and V_{CORE} power supply voltages. When one of these voltages drops below a typical threshold value, the system is reset.
2. It can monitor the onboard battery. Jumper W5(1-2) must be shorted to connect the onboard battery. Jumper W8:2-3 must be shorted to enable power fail detection on the battery. When the battery is in a low condition (below 2.9V typical), the BatFlt bit at I/O address x97h, will read 1 (x97h, bit 6: 1 = failed, 0 = good). To generate an NMI (non-maskable interrupt) when the battery fails, the BatFltEn bit must contain a 1 (x97h, bit 7: 1 = enable NMI, 0 = disable NMI). The interrupt can then be serviced by an interrupt handler. If you choose not to generate an NMI, you can still use an algorithm to detect a low battery condition at x97h, bit 6, and respond accordingly.
3. It can monitor an offboard 3.6V battery. Jumper W5(2-3) must be shorted to connect the offboard battery. Jumper W8(2-3) must be shorted to enable power fail detection on the battery. The offboard battery, when it replaces the onboard battery, is monitored exactly as explained for the onboard battery in item 2. A 3.6V battery is recommended.
4. It can monitor a user defined offboard battery (or other power source) with an user-defined threshold. In such a case, the onboard battery still needs to be connected to power the CMOS RAM and real time clock, but it will not be monitored for low voltage:

   . Short the W5(1-2) jumper to connect the onboard battery.
   . Short the W8(1-2) jumper to enable power fail detection on the user defined offboard battery.

The user-defined threshold is determined by the value of the through hole resistor you install at R3 on the PCI-943. Use this formula to calculate the resistance needed, for the desired threshold:

$$R3 = (7692 \times V_T) - 10000$$

R3 is the value in ohms of the resistor you must add.
V_T is the voltage that will produce the alarm.

For example, to set an alarm when the offboard battery reaches 10V, a 66920Ω resistor is needed (R3 = 7692 x 10V – 10000 = 66920Ω).
The closest standard resistor for 1% tolerance is a 68.1kΩ resistor. If we reverse the formula, we find that the actual threshold is $V_{T=}$ (68100Ω + 10000) / 7692 = 10.15V.

When the threshold is crossed, the BatFlt bit at I/O address x97h, will read 1 (x97h, bit 6: 1 = failed, 0 = good).

To generate an NMI (non-maskable interrupt) when the battery fails, the BatFltEn bit must contain a 1 (x97h, bit 7: 1 = enable NMI, 0 = disable NMI).
The interrupt can then be serviced by an interrupt handler.

If you choose not to generate an NMI, you can still use an algorithm to detect a power fail / low battery condition and respond accordingly.

4.3 RESET HISTORY

Following a reset, the application software can read register x91h and examine the bits PBRES and WDO. Based on the values of those bits, the following conclusion can be drawn about the reset source.

PBRES	WDO	RESET Source
0	0	Power up, Ctrl-Alt-Del or software runaway
1	0	Reset switch or remote reset
0	1	Programmable watchdog
1	1	Watchdog followed by a reset switch.

For proper operation, the bit CLRHIS* of register x92h should be pulsed (0-1) immediately after reading the history bits.

4.4 THERMAL MANAGEMENT

The processor module includes a user-defined temperature sensor / alarm function, which provides thermal monitoring of the processor.

Thermal management is software configurable through the AWARD CPU/Board Features Setup option.

4.5 SYSTEM MONITOR

The system monitor connector is used to get information from the chassis or the outside world and to report the state of the PCI-943 and the application software. The following table describes the signals on the system monitor connector.

Please refer to the register definition (x91h, x93h and x97h) for software use.

Signal	Type	Description
PWRBTN*	Input / output **	Reserved for ATX power supply control
SoftOFF*	output **	Reserved for ATX power supply control
GPIO1 **GPIO2**	Input / output ** 10k pull-up onboard	General purpose I/O, fully software controllable. Can be used as input, output or bidirectional link. End-user can implement an I2C or SMBus type link with those bits.
AppFlt*	output ** 10k pull-up onboard	Application fault Set to "high" by end-user software, set to "low" by reset. Indicate hardware and software functionality. The function "watchdog fail" is implicitly included because a watchdog reset will automatically force the signal in the faulty condition.
CpuFlt*	output ** 10k pull-up onboard	CPU board fault Minor fault detected on PCI-943 board. This bit is a combination of all sources of the onboard monitor (thermal alert, fan, supplies, critical error during POST, etc.). It is asserted (low) by the BIOS under a fault condition. Can be wired-or with AppFlt* to generate an "any fault" signal.
IntAlert*	Input Active low	Intruder Alert Reserved.
ExtFlt*	TTL input Pull-up onboard	External fault. Can be generated by the power supply (Advanced Power Fail) or an external monitor board that detected a critical problem. This signal can generate an NMI; see register x97h.
FanFlt*	TTL input Pull-up onboard	Fan fault. Although a non specific fault input, this one is intended to generate an NMI based on the output of an external fan monitoring circuit. See register x97h.

* Active Low Signal

** Open Collector output

NOTE

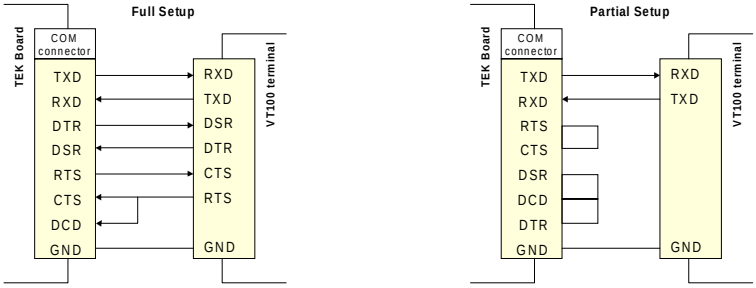
Any unused feature on the system monitor connector **must** be left unconnected.

5. VT100 MODE

The VT100 mode may be required to communicate with the board using a remote terminal through a serial communication link.

In this configuration, the remote terminal must emulate VT100 or ANSI terminal and support an emulation program such as Telix or Procomm.

The serial cable must conform to one of the following:



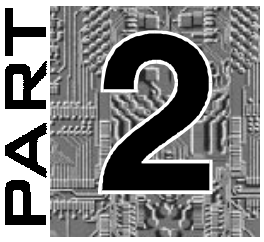
5.1 SETUP AND CONFIGURATION

Follow these steps for setting up VT100 Mode:

- Power off your board and install the jumper W9 (3-4) to enable the VT100 Mode. Note: both Serial Port 1 and Serial Port 2 support the VT100 Mode.
- Connect the serial cable. Note: if a full setup cable is not required a partial cable by only the TXD and RXD lines can be used. Simply loop back the control lines according to the partial setup cable diagram.
- Power on your board and run the BIOS Setup program, Integrated Peripherals option, and select a communication baud rate.
- The remote terminal must be set to support the following protocol:
  8 Bits / No Parity / Echo Off.

5.2 RUNNING WITHOUT A TERMINAL

The board can boot up without a screen or terminal attached. However, if VT100 Mode is desired, but the terminal is to be disconnected, you must ensure the control lines are in an active state. Failing this, the system may "hang" while waiting for the control lines to become active. Wiring the system according to the diagram provided previously allows the lines to remain active. This does not apply if the VT100 jumper is not set.



JUMPER SETUPS

6. SETTING JUMPERS

6. SETTING JUMPERS

Thirteen jumpers are provided to setup the board. Their functions are summarized as follows:

PCI-943 - CPU Related Jumpers
* Default Setting

W2

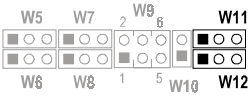
W2 - Bus / Core Frequency	
Default Value Previously Set and Saved in CMOS *	off
Force the Core Speed to Twice the Front Side Bus Speed	on

W3

W3 - Front Side Bus Speed	
66MHz Override	on
66MHz or 100MHz, depending on the processor *	off

Careful attention should be taken when installing and setting the processor: Faulty jumper settings may damage both your processor and your board.

PCI-943 - Video Related Jumpers
* Default Setting



W1 - AGP Feature	
Enable AGP *	off
Disabled AGP	on

W11 - Onboard Video	
Enabled *	off
Disabled	on

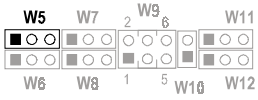
W12 - INTA Assigned to Video Controller	
Enabled	on
Disabled *	off

Setting Jumpers (continued)

W4

W4 - SCSI Mode	
16-bit: Wide Ultra SCSI II *	on
8-bit: Fast SCSI II and Fast-20 SCSI II	off

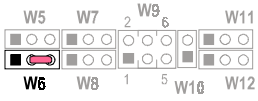
W5



W5 - CMOS Backup Source	
Onboard Battery	1-2
External Power (3.6V only)	2-3
No Power (clear CMOS) *	off

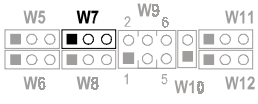
There is a danger of explosion if the battery is incorrectly replaced.
Replace only with the same or equivalent type recommended by the manufacturer (3.6V, 370mAh lithium battery).
Dispose of used batteries according to the manufacturer's instructions .

W6



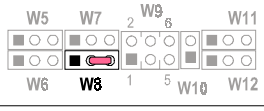
W6 - SCSI Termination	
Controlled by Software	1-2
Board is hardware Terminated *	2-3
No Termination	off

W7



W7 - Remote Reset Source	
Controlled by RXD 1 (COM1)	1-2
Controlled by RXD 2 (COM2)	2-3
Disabled *	off

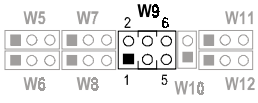
W8



W8 - Power Fail Source Selection	
User Defined Source	1-2
CMOS Backup Source (see W12) *	2-3

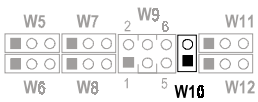
To prevent the board from inopportune PFI, the jumper cap must always be installed at either 1-2 or 2-3 position.

W9



W9 - User Definable		
	on	off
1-2	User Defined	User Defined *
3-4	VT-100 Mode	Normal Mode *
5-6	Download Mode	Normal Mode *

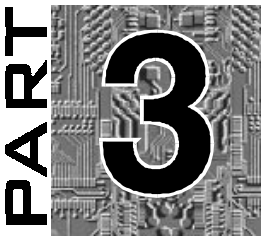
W10



W10 - SCSI and EIDE Leds	
Combined	on
Independant *	off

W13, W14

W13, W14 - Serial Port 2 Termination		
(set In RS-485 Mode only)	W13	W14
Termination Enabled	on	on
Termination Disabled *	off	off



SOFTWARE SETUPS

7. AWARD BIOS SETUP PROGRAM

All relevant information for operating the board and peripherals it is connected to are stored in the BIOS CMOS memory. A battery stores this information when the board is powered off, and the BIOS Setup program is required to make changes to the setup.

Make sure the BIOS is properly configured prior to installing the operating system and its drivers.

To boot from the Ethernet interface, ensure the Boot From LAN option to Enabled at the BIOS level (BIOS Features Setup option), and refer to the installation procedure in the LAN Boot & SCSI Utility diskettes.

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.
The BIOS default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP default values provide optimum performance settings for all devices and system features.

CAUTION

Both BIOS and SETUP Default Values have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

7.1 RUNNING THE SETUP PROGRAM

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the PCI-943 single board computer. The interface provided by AWARD is 100% compatible with the non-industrial PCs. All functions accept similar inputs and provide the same results, although the program code itself is different.

The PCI-943 uses the AWARD Setup program, a setup utility in flash memory that is accessed by pressing the DELETE key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

Before modifying the AWARD CMOS setup parameters, ensure that the battery jumper is installed to enable the data to be saved. Removing the battery will clear the CMOS setup and load the default setups, only you will have to reconfigure the BIOS again.

To run the AWARD Setup program incorporated in the Flash BIOS:

- Turn on or reboot the system.
- Hit the DELETE key before or when the message - "Press DEL To Enter SETUP" appears near the bottom of the screen.
- The main menu of the AWARD BIOS CMOS Setup Utility appears on the screen.

```
                    ROM PCI/ISA BIOS
                 CMOS SETUP UTILITY
               AWARD SOFTWARE, INC.

STANDARD CMOS SETUP                  LOAD BIOS DEFAULTS
BIOS FEATURES SETUP                  LOAD SETUP DEFAULTS
CHIPSET FEATURES SETUP               SUPERVISOR PASSWORD
POWER MANAGEMENT SETUP               USER PASSWORD
PNP/PCI CONFIGURATION                IDE HDD AUTO DETECTION
CPU/BOARD FEATURES SETUP             SAVE & EXIT SETUP
INTEGRATED PERIPHERALS               EXIT WITHOUT SAVING

Esc      :    Quit                   ↑ ↓ → ←     :    Select Item
F10      :    Save & Exit Setup      (Shift)F2   :    Change Color

                  Time, Date, Hard Disk Type . . .
```

7.1.1 Main Menu

The Main Menu includes the following categories:

Category	Description
Standard CMOS Setup	This Setup page includes all the items in a standard, AT-compatible BIOS (date, time, hard disk type, floppy disk type, video adapter type, memory…).
BIOS Features Setup	This Setup page includes all the items of AWARD's special enhanced features.
Chipset Features Setup	This Setup page includes all the items of the chipset's special features.
Power Management Setup	This Setup page sets power conservation options.
PnP/PCI Configuration	This Setup page sets plug and play and PCI configuration options.
CPU/Board Features Setup	This Setup page sets processor speeds, thermal management and board monitoring options.
Integrated Peripherals	I/O susbsystems that depend on the integrated peripherals controller in your system.
Load Bios Defaults	The BIOS defaults are fail safe settings which consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.
Load Setup Defaults	The Setup defaults are the optimal settings that provide the optimum performance for all devices and system features. If the CMOS RAM is corrupted, the Setup defaults are loaded automatically.
Supervisor/User Password Setting	Changes, sets, or disables the password. It allows you to limit the access to the system and the Setup, or just to the Setup.
IDE HDD Auto Detection	Forces the detection of the IDE dard disk drives parameters and puts them in the Standard CMOS Setup page.

7.1.2 Saving & Exiting Operations

Use one of the following options available from the Main Menu:

Function	Description
Save & Exit	After having modified the AWARD Setup, you can save the configuration in CMOS RAM and the Flash BIOS, by selecting this option.
Exit Without Saving	This option is used to exit AWARD Setup without saving the configuration to CMOS RAM.

7.2 SETUPS

The arrow keys (↑ ↓ → ←) are used to highlight items on the menu and the PAGEUP and PAGEDOWN keys are used to change the entry values for the highlighted item. To select an entry, press the ENTER key. Also, you can press the F1 key to obtain help information or the ESC key to leave an option, close a menu or to quit the program.

Key	Function
↑	Moves to previous item.
↓	Moves to next item.
←	Moves to the item in the left hand.
→	Moves to the item in the right hand.
ESC	When in the Main Menu: Quits program (Answer 'Y' to save changes into CMOS). When in other screens: Exits and returns to the Main Menu.
PAGEUP or +	Increases the numeric value or changes value.
PAGEDOWN or -	Decreases the numeric value or changes value.
F5	When in the Main Menu: Restores the previous setup values for all the BIOS parameters (except Standard CMOS) which were displayed when you entered the program. When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, Thermal Management Setup, PNP/PCI Setup or Integrated Peripherals Setup: Restores the previous setup values for that setup screen only.
F6	When in the Main Menu: Loads the BIOS Defaults of all the BIOS parameters (except Standard CMOS). The BIOS Defaults are fail safe settings which consist of the safest set of parameters. When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, Thermal Management Setup, PNP/PCI Setup or Integrated Peripherals Setup: Loads the BIOS Defaults for all the BIOS parameters for that setup screen only.
F7	When in the Main Menu: Loads the Setup Defaults for all the BIOS parameters (except Standard CMOS). When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, Thermal Management Setup, PNP/PCI Setup or Integrated Peripherals Setup: Loads the Setup Defaults for all the BIOS parameters for that setup screen only.
F10	When in the Main Menu: Saves all the CMOS changes.

7.2.1 Standard CMOS Setups

Function	Description
Date/Time	The current values for each category are displayed. Enter new values through the keyboard.
Hard Disks	Two IDE controllers are defined on the PCI-943 board. The Primary and Secondary controller can have two disks: Master Disk or Slave Disk. The disks are bootable in this order: 1) Primary Master, 2) Primary Slave, 3) Secondary Master, and 4) Secondary Slave. Only three settings are available for the hard disk type: Auto, 47 (user defined) and None. Type 1 to 46 are not predefined in the system: Use auto-detect or enter the parameters for the type in the user-defined type 47.
Drive A / Drive B	Select the type of floppy disk installed for drive A and drive B.
Video	This option specifies the basic type of display adapter card installed in the system.
Halt on	This option specifies the type of errors that will stop the system during the BIOS booting procedure. A message asks that you press F1 to continue or press the DELETE key to enter Setup. The settings are: All errors, No errors, All but keyboard, All but diskette, and All but disk/key (default setting).
Memory	This display-only option indicates the amount of Base, Extended and other types of memory installed in the system.

7.2.2 BIOS Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Virus Warning	Dis.	Dis.	En./Dis.	When Enabled, you receive a warning message if a program (specifically, a virus) attempts to write to the boot sector or the partition table of the hard disk drive. You should then run an anti-virus program. Keep in mind that this feature protects only the boot sector, not the entire hard drive. **Note: Many disk diagnostic programs and OS setups (e.g., Win95 setup), that access the boot sector table, can trigger the virus warning message. If you plan to run such a program, we recommend that you first disable the virus warning.**
CPU Internal Cache	Dis.	En.	En./Dis.	Enables or Disables the CPU Internal Cache (L1 cache).
External Cache	Dis.	En.	En./Dis.	Enables or Disables the External Cache (L2 cache).
CPU L2 Cache ECC Checking	Dis.	En.	En./Dis.	Enables or Disables ECC Checking for L2 cache. **Note: processors provided by TEKNOR support ECC. However, not all Pentium® II processors support ECC. Check Intel's website to know if your processor supports ECC:** http://developer.intel.com/support/processors/pentiumII/identify.htm.
Quiet POST	Dis.	Dis.	En./Dis.	At the power on self test (POST), only the AWARD logo and the "Press DEL to enter SETUP" message appear.
Quick Power On Self Test	Dis.	En.	En./Dis.	Select Enabled to reduce the amount of time required to run the POST. A quick POST skips certain steps. We recommend that you enable quick POST to save time, since most major OS do their own tests
Full Screen Logo Show	Dis.	Dis.	En./Dis.	When enabled, a full screen bitmap (.BMP) picture will appear during the POST (only available if ordered).
Boot From LAN First	Dis.	Dis.	En./Dis.	If Enabled, the BIOS will first attempt to boot from the LAN. The complete procedure for this function is available on the Boot From LAN utility diskette.
Raid Card Boot First	Dis.	Dis.	En./Dis.	If Enabled, the BIOS will first attempt to boot from the RAID disk card.
Boot Sequence	A,C, SCSI	C,A, SCSI	A,C,SCSI; C,A,SCSI; C,CDROM,A; CDROM,C,A; D,A,SCSI; E,A,SCSI; F,A,SCSI; SCSI,A,C; SCSI,C,A; C only; LS/ZIP,C.	This option defines the searching order in the BIOS for the boot device(s). **Note: The Boot From LAN First and Raid Card Boot First options take precedence over this option.**
Swap Floppy Drive	Dis.	Dis.	En./Dis.	Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B. If there is only one floppy on the system, it could be assigned to B with this option.
Boot Up Floppy Seek	En.	Dis.	En./Dis.	When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360KB floppy drives have 40 tracks; drives with 720KB, 1.2MB, and 1.44MB capacity all have 80 tracks. Because very few modern PCs have 40 track floppy drives, we recommend that you set this field to "Disabled" to save time.
Drive A Boot Permit	En.	En.	En./Dis.	When Disabled, this option will not permit booting from Drive A.
Floppy Disk Access Control	R/W	R/W	R/W, Read Only	When Read Only, this option will not permit writing to the floppy disk.

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BIOS Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Report No FDD For Win 95	No	No	Yes, No	Select Yes to release IRQ6 when the system contains no floppy drive, for compatibility with Windows 95 logo certification. In the Integrated Peripherals screen, select Disabled for the Onboard FDC Controller option.
Hard Disk Write Protect	Dis.	Dis.	En./Dis.	When Enabled, this option will not permit writing to the hard disk.
HDD S.M.A.R.T. Capability	Dis.	En.	En./Dis.	When Enabled, the Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.) features of the HDD are supported. S.M.A.R.T is used for prediction of device degradation and/or faults.
Delay For HDD (Secs)	0	0	0-15	This number of seconds inserted prior to HDD initialization. 0 is disabled.
PCI/VGA Palette Snoop	Dis.	Dis.	En./Dis.	Palette snooping allows multiple VGA devices operating on different buses to handle data from the CPU on each set of palette registers. When set to Enabled, data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA device's palette registers, permitting the palette registers of both to be identical. When set to Disabled, data read and written by the CPU is only directed to the PCI VGA device's palette registers.
OS Select For DRAM > 64MB	Non-OS/2	Non-OS/2	Non-OS/2, OS/2	Select OS2 only if you are running OS/2 with greater than 64MB of RAM.
Gate A20 Option	Normal	Fast	Normal, Fast	When Fast, enables fast switching of Gate A20 via the 440BX chipset, instead of the keyboard controller.
Security Option	Setup	Setup	Setup, System	If you have set a password, select whether the password is required every time the system boots ("System" option), or only when you enter Setup ("Setup" option).
Diskette Access For	All	All	All, Supervisor	When this option is set to Supervisor and the Security option to System, all floppy disk accesses (read/write) are limited to the Supervisor (supervisor password required).
Save CMOS in Flash	Dis.	Dis.	En./Dis.	When this option is set to "Enabled", the CMOS RAM Setup will be restored from the Flash BIOS at each power up. If the battery fails, only the date and time could be lost.
Boot Up NumLock Status	On	On	On, Off	Toggle between On or Off to control the state of the NumLock key when the system boots. When toggled On, the numeric keypad generates numbers instead of controlling cursor operations.
Typematic Rate Setting	Dis.	En.	En./Dis.	When Disabled, the following two items (Typematic Rate and Typematic Delay) are irrelevant. Keystrokes repeat at a rate determined by the keyboard controller in your system. When Enabled, you can select a typematic rate and a typematic delay.
Typematic Rate (Chars/s)	30	30	6-30 char/sec.	When the typematic rate setting is Enabled, you can select a typematic rate (the rate at which characters repeat when you hold down a key).
Typematic Delay (msec)	250	250	250-1000 ms	When the typematic rate setting is Enabled, you can select a typematic delay (the delay before key strokes begin to repeat).

7.2.3 Chipset Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
SDRAM RAS-to-CAS Delay	3	3	2, 3	**Note: Upon boot-up, the BIOS will detect and display the optimal value for the SDRAM options (first four options in this menu), if it is different from the Setup value. You must enter the AWARD Setup, and set the options at the suggested value if you want the best performance.** This option inserts a timing delay between the CAS and RAS strobe signals, used when SDRAM is written to, read from, or refreshed. The number selected is the number of clocks to be inserted between a row activate command and either a read or write command.
SDRAM RAS Precharge Time	3	3	2, 3	Selects the number of CPU clocks for the RAS precharge. If an insufficient number of cycles is allowed for the RAS to accumulate its charge before SDRAM refresh, the refresh may be incomplete and the DRAM may fail to retain data.
SDRAM CAS Latency Time	3	3	2, 3	This option controls the number of clocks between when a a read command is sampled by the SDRAMs and when the chipset samples read data from the SDRAMs. Select 3 for 3 DCLKs and 2 for 2 DCLKs. If a given row is populated with a registered SDRAM DIMM, an extra clock is inserted between the read command and when the chipset samples read data.
SDRAM Precharge Control	Dis.	Dis.	En./Dis.	When Enabled, all CPU cycles to SDRAM result in an All Banks Precharge Command on the SDRAM interface.
DRAM Data Integrity Mode	Non-ECC	ECC	ECC, Non-ECC	When set to ECC, allows auto-correction of the data read from memory. The ECC error flags' status register and the error pointer are updated if error correction occurs in this mode. When set to Non-Ecc, no error checking or error reporting is done.
System BIOS Cacheable	Dis.	En.	En./Dis.	Selecting Enabled allows caching of the system BIOS ROM at F0000h-FFFFFh, resulting in better system performance. However, if any program writes to this memory area, a system error may occur.
Video BIOS Cacheable	Dis.	En.	En./Dis.	Selecting Enabled allows caching of the video BIOS ROM at C0000h plus the VGA BIOS size, resulting in better video performance. However, in any program writes to this memory area, a system error may occur.
Video RAM Cacheable	Dis.	En.	En./Dis.	When Enabled, video memory region is cacheable. Some offboard video card drivers may behave strangely; in such a case, disable this option.
8 Bit I/O Recovery Time	3	1	1-8, NA	The I/O recovery mechanism adds bus clock cycles between PCI-originated I/O cycles to the ISA bus. This delay takes place because the PCI bus is so much faster than the ISA bus. These two fields let you add recovery time (in bus clock cycles) for 16-bit and 8-bit I/O.
16 Bit I/O Reccovery Time	2	1	1-4, NA	
Memory Hole At 15M-16M	Dis.	Dis.	En./Dis.	You can reserve this area of system memory for ISA adapter ROM. When this area is reserved, it cannot be cached. The user information of peripherals that need to use this area of system memory usually discusses their memory requirements.
Passive Release	En.	En.	En./Dis.	When Enabled, CPU to PCI bus accesses are allowed during passive release otherwise the arbiter only accepts another PCI master access to local SDRAM.
Delayed Transaction	Dis.	Dis.	En./Dis.	The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specifications version 2.1.

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Chipset Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Supervisor I/O Base Addr.	190h	190h	190h, 290h, 390h	This option determines the base address for the Supervisor I/O Register, which is used for such functions as power fail detection and the watchdog timer.
Power-Supply Type	AT	ATX	AT, ATX	This option selects the type of power supply.
AGP Aperture Size (MB)	64	64	4 to 256	This option selects the size in MB of the AGP Aperture.
Video BIOS Shadow	Dis.	En.	En./Dis.	Software that resides in a read-only memory (ROM) chip on a device is called *firmware*. Award permits shadowing of firmware such as the system BIOS, video BIOS, and similar operating instructions that come with some expansion peripherals. Shadowing copies from ROM into system RAM, where the CPU can read it through the 64-bit DRAM bus. Firmware not shadowed must be read by the system through the 8 or 16-bit ISA bus. Shadowing improves the performance of the system BIOS and similar firmware for expansion peripherals. Enable shadowing into each section of memory separately. Many system designers hardwire shadowing of the system BIOS and eliminate a System BIOS Shadow option. Note that on a PCI VGA card (onboard or offboard), the VGA BIOS is always shadowed. Video BIOS shadows into memory area C0000 plus the VGA BIOS size. The remaining areas between C0000 and DFFFF shown on the BIOS Features Setup screen may be occupied by other expansion card firmware. If an expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies to shadow it into the correct area of RAM.
C8000-CBFFF	Dis.	Dis.	En./Dis.	
CC000-CFFFF	Dis.	Dis.	En./Dis.	
D0000-D3FFF	Dis.	Dis.	En./Dis.	
D4000-D7FFF	Dis.	Dis.	En./Dis.	
D8000-DBFFF	Dis.	Dis.	En./Dis.	
DC000-DFFFF	Dis.	Dis.	En./Dis.	

7.2.4 Power Management Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
ACPI Function	Dis.	En.	En./Dis.	When Enabled and the OS supports ACPI or OSPM (e.g., Win98, Window NT 5), power management functionality moves to the OS. **Note: When Enabled, all other options in the Power Management Setup will not be used.**
Power Management	User Def.	User Def.	Min Saving, Max Saving, User Define, Disable	This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. Max Saving: Maximum power savings. Inactivity period is 1 minute in each mode. Min Saving: Minimum power savings. Inactivity period is the maximum setting in each mode (1 hour for Doze, Standby and Suspend). User Define: Set each mode individually. Select time-out periods in the PM Timers section (see below).
PM Control by APM	Yes	Yes	Yes, No	If Yes, the OS will control the PM by APM calls. If No, the BIOS will control the PM and APM calls from the OS will be ignored.
Video Off Method	V/H SYNC + Blank	V/H SYNC + Blank	V/H SYNC+Blank, DPMS, Blank Screen	Determines the manner in which the monitor is blanked. V/H SYNC + Blank: System turns off vertical and horizontal synchronization ports and writes blanks to the video buffer. DPMS Support: Select this option if your monitor supports the Display Power Management Signaling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsytem to select video power management values. Blank Screen: System only writes blanks to the video buffer.
Video Off After	Stand by	Stand by	Doze, Standby, Suspend, NA	As the system moves from lesser to greater power-saving modes, select the mode in which you want the monitor to blank.
Modem Use IRQ	3	3	N/A, 3, 4, 5, 7, 9, 10, 11	Name the IRQ line assigned to the modem (if any) on your system. Activity of the selected IRQ always awakens the system.
PM Timers:				The following modes are Green PC power saving functions. They are user-configurable only during User Defined Power Management mode.
Doze Mode	Dis.	20min	1min to 1h, Disable	After the selected period of system inactivity (1 minute to 1 hour), the CPU clock runs at lower speed while all other devices still operate at full speed.
Standby Mode	Dis.	40min	1min to 1h, Disable	After entering Doze mode and the selected period of system inactivity (1 minute to 1 hour) has elapsed, the video shuts off while all other devices still operate at full speed.
Suspend Mode	Dis.	1hour	1min to 1h, Disable	After entering Standby mode and the selected period of system inactivity (1 minute to 1 hour) has elapsed, all devices including the CPU shut off and the system waits for an event to wake them up again.
HDD Power Down	Dis.	15 Min	1-15min, Disable	After the selected period of drive inactivity (1 to 15 minutes), the hard disk drive powers down while all other devices remain active. The HDD power down mode is only available if the hard drive has this capability.
HDD Down When Suspend	En.	En.	En./Dis.	When Enabled and the system goes in Suspend Mode, the hard disk is shut down.
Throttle Duty Cycle	75.0%	75.0%	12.5%-75.0%	When the system enters Doze mode, the CPU clock runs only part of the time. You may select the percentage of time that the clock does not run.
PCI/VGA Act-Monitor	Dis.	Dis.	En./Dis.	When Enabled, continuous video activity restarts the global timer for Standby mode.
Soft-OFF by PWR-BTTN	Instant-off	Instant-off	Instant-off, Delay 4 sec.	This option only works with an ATX power supply. It allows two configurations for the power button: Instant-off for power supply on/off switch, or Delay 4 sec. for entering Suspend Mode after pressing the button at least 4 seconds.

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Power Management Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Resume by Ring	Dis.	En.	En./Dis.	When Enabled and a modem is connected to a COM port, allows a modem ring to re-activate the CPU when in Suspend mode.
IRQ 8 Break Suspend	Dis.	En.	En./Dis.	When Enabled, the RTC alarm interrupt is monitored to allow an interrupt to awaken the system when in Doze, Standby or Suspend Mode.
Resume by Alarm	Dis.	Dis.	En./Dis.	When Enabled, allows setup of a time to re-activate the CPU when in Suspend mode with the options Date (of Month) Alarm and Time (hh:mm:ss) Alarm. **Note: The IRQ 8 Break Suspend option in this setup screen must be Enabled to use the RTC alarm.**
Date (of Month) Alarm	-	-	0 -31	This option appears only if Resume by Alarm is enabled. It specifies the date in the month for the RTC alarm.
Time (hh:mm:ss) Alarm	-	-	0:0:0-23:59:59	This option appears only if Resume by Alarm is enabled. It specifies time of day for the RTC alarm.
Reload Global Timer Events:				When any of the options below is Enabled, monitoring of the interrupt will occur to allow an interrupt to awaken the system when in Doze, Standby or Suspend Mode.
IRQ[3-7,9-15], NMI	Dis.	En.	En./Dis.	
Primary IDE 0	Dis.	En.	En./Dis.	
Primary IDE 1	Dis.	En.	En./Dis.	
Secondary IDE 0	Dis.	En.	En./Dis.	
Secondary IDE 1	Dis.	En.	En./Dis.	
Floppy Disk	Dis.	En.	En./Dis.	
Serial Port	En.	En.	En./Dis.	
Parallel Port	Dis.	En.	En./Dis.	

7.2.5 PnP/PCI Configuration

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
PNP OS Installed	Yes	No	Yes, No	If the operating system (OS) is Plug and Play (for example Windows 95), select "Yes" if you want the OS to allocate resources according to Plug and Play standards, or "No" if you want the same resource allocations at every system boot-up. Select "No" when the OS is not Plug and Play (for example, DOS). **Note: When set to "Yes", only the boot devices will get an IRQ.**
Resources Controlled By	Auto	Man.	Auto, Man.	The Award Plug and Play BIOS can automatically configure all the boot and Plug and Play-compatible devices. If you select Auto, all the interrupt requests (IRQs) and DMA assignment fields disappear, as the BIOS automatically assigns them.
Reset Configuration Data	Dis.	Dis.	En./Dis.	Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.
IRQ *n* Assigned To	PCI/ISA PnP	PCI/ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific interrupt, such as IRQ4 for serial port 1. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for an IRQ line, this resource will not be available for PCI/ISA PnP.
DMA *n* Assigned To	PCI/ISA PnP	PCI/ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system DMA channel as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific DMA channel. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for a DMA channel, this resource will not be available for PCI/ISA PnP.
Init Display First	Onboard	Onboard	PCI Slot, Onboard, AGP (not supported)	Initializes the specified video display. The chosen display becomes the primary display. Other display devices are ignored by the BIOS and configured by the OS.
Assign IRQ For VGA	Dis.	Dis.	En./Dis.	When Enabled, the video card is assigned an IRQ.
Assign IRQ For USB	En.	En.	En./Dis.	When Enabled, the USB is assigned an IRQ. When Disabled, the IRQ is freed up for another purpose.
PCI Latency Timer	32	32	0-255 (integers)	This option specifies the value of the Latency Timer for the PCI bus master, in units of PCI bus clocks.
Special PCI Routing	En.	En.	En./Dis.	Disable this option if the backplane into which the board is installed conforms to the PICMG specifications. When enabled the board will attempt to detect a special PCI routing configuration.
Slot [number] Use IRQ No.	Auto	Auto	Auto, 3, 4, 5, 7, 9, 10, 11, 12, 14, 15	When Auto, the BIOS automatically assigns an IRQ for the specified PCI slot number (in the option title: 1, 2, 3 or 4). When set to one of the numbers (in possible settings), that IRQ number is assigned to the PCI slot.
Used MEM Base Address	N/A	N/A	N/A, C800, CC00, D000, D400, D800, DC00	Select a base address for the memory area used by any peripheral that requires high memory.
Used MEM Length	8K	8K	8K, 16K, 32K, 64K	Select a length for the memory area specified in the previous field. This field does not appear if no base address is specified.

7.2.6 CPU/Board Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Current Processor(s) Speed	-	-	Varies	This option displays the current processor speed.
Front Side Bus Speed	-	-	66, 100	This option displays the current FSB speed.
Processor(s) Speed Setting	-	-	FSB=100: 350, 400, 450, 500. FSB=66: 233, 266, 300, 333.	You can set the processors' speed with this option. Set the option to the maximum internal speed or lower. If the board does not boot, refer to section 7.1 for processor jumper information.
MPS Version Control For OS	1.4	1.4	1.1, 1.4	The BIOS supports versions 1.1 and 1.4 of the Intel multiprocessor specification. Select the version supported by the operating system running on this computer.
Thermal Management Options:				
. Thermal Manag.	Dis.	Dis.	En./Dis.	When this option is enabled, the CPU temperature is monitored. Whenever the CPU overheats, the CPU slows down to lower the temperature.
. Thermal Audio Alarm	Dis.	Dis.	En./Dis.	When the Thermal Management option and this option are enabled, a continuous audible alarm is sounded when the temperature specified in the Overheat Alarm options is reached. Such an alarm may not be supported by the Operating System.
. CPU 1 Die T°C	-	-	Varies	Displays the current die (internal) CPU temperature, when Thermal Management is enabled.
. Resume Alarm (°C)	42	42	10-70	The CPU will be slowed down (Doze mode) when it reaches the selected Overheat Alarm (°C) temperature. Full speed (Normal mode) will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 4° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm.
. Overheat Alarm (°C)	50	50	30-90	
. CPU 1 Case T°C	-	-	Varies	Displays the current case (external) CPU temperature, when Thermal Management is enabled.
. Resume Alarm (°C)	42	42	10-70	The CPU will be slowed down (Doze mode) when it reaches the selected Overheat Alarm (°C) temperature. Full speed (Normal mode) will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 4° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm.
. Overheat Alarm (°C)	50	50	30-90	
Shutdown Temp. (°C)	60	60	60-75	This option allows you to set the board temperature at which the system will shut down (only available for ATX power supply and ACPI operating system.
Board Monitoring: . Current CPU Fan 1 Speed	-	-	Varies	Value displayed.
. Current CPU Fan 2 Speed	-	-	Varies	Value displayed.
. Current Vcpp1 (V)	-	-	Varies	CPU1 core voltage value displayed
. Current Vin12 (V)	-	-	Varies	12V input voltage value displayed
. Current Vin5 (V)	-	-	Varies	5V input voltage value displayed
. Current Vin3.3 (V)	-	-	Varies	3.3V input voltage value displayed
. Current Vin2.5 (V)	-	-	Varies	2.5V input voltage value displayed

7.2.7 Integrated Peripherals

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
On-Chip Primary/Secondary PCI IDE:	En.	En.	En./Dis.	Select Enabled to activate the Primary/Secondary IDE channel. The four options below appears only if the On-Chip Primary option is enabled.
IDE Primary/Secondary Master/Slave PIO	Auto	Auto	Modes 0-4 Auto	Use this option to set a PIO mode (0-4) for each of the onboard IDE devices. Modes 0 through 4 provide successively increased performance and speed. In Auto mode, the system automatically determines the best mode for each device. If you select a mode that the drive does not support, it may not work, so choose a lesser value or Auto to see the best mode for the drive.
IDE Primary/Secondary Master/Slave UDMA	Dis.	Auto	Auto, Dis.	Ultra DMA/33 implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If your hard drive and your system software both support Ultra DMA/33, select Auto to enable BIOS support.
On-Chip Secondary PCI IDE:	En.	En.	En./Dis.	Select Enabled to activate the Secondary IDE channel. The four options below appears only if the On-Chip Secondary option is enabled.
IDE HDD Block Mode	Dis.	En.	En./Dis.	Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.
Onboard PCI SCSI Chip	En.	En.	En./Dis.	Enables/disables the onboard SCSI controller.
Ethernet Controller	En.	En.	En./Dis.	Enables/disables the onboard Ethernet controller.
USB Keyboard Support	Dis.	Dis.	En./Dis.	This option is for DOS and BIOS support only (Win 95 has it is own drivers). **It does not enable or disable the USB controller.**
PS/2 Mouse Function Control	Auto	Auto	Auto/Dis.	When set to Auto, the PS/2 mouse is automatically enabled, if it is present.
Onboard FDC Controller	Enabled	Enabled	Enabled, Disabled	Select Disabled to disable the onboard floppy disk controller (FDC).
Onboard Serial Port 1/2	Auto	Auto		Select a COM port address and IRQ# for the first and second serial ports. Possible settings are: Dis., 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3, Auto
Serial Port 2 Mode	RS-232	RS-232		Select the operation mode for Serial Port 2. within RS-232,RS-422, and RS-485
VT100 Mode on Serial Port	1	1	1, 2	Selects the communication port for VT100 mode: Serial Port 1 or 2.
Onboard Parallel Port	378/IRQ7	378/IRQ7		Select a LPT address and IRQ# for the physical parallel (printer) port. Possible settings are: Disabled, 3BC/IRQ7, 378/IRQ7, 278/IRQ5,
Parallel Port Mode	ECP + EPP1.9	ECP + EPP1.9		Select an operating mode for the onboard parallel port. Select ECP or EPP unless you are certain both your hardware and software does not support ECP or EPP mode. Possible settings are SPP, EPP1.9+SPP, ECP, ECP+EPP1.9, Normal, EPP1.7+SPP, ECP+EPP1.7
ECP Mode Use DMA	3	3	1, 3	Select a DMA channel for the port.

8. CONFIGURING SCSI

The Adaptec SCSISelect Configuration Utility allows you to configure or view the SCSI host adapter settings. It also allows you to run SCSI disk utilities, such as a low-level disk format. The various menus and options of the SCSISelect Configuration Utility program are described in this Section.

The Adaptec SCSISelect Configuration Utility is a DOS program available on the LAN Boot & SCSI Utility 2 diskette (file name 7880cfg.exe).

Refer to Section 2.7.3 *Storage Devices, SCSI Devices* to install and connect SCSI devices on the board. Also, follow the installation instructions provided with your SCSI peripheral.

NOTE

The onboard Ethernet controller resides on the PCI bus and is therefore Plug and Play by default. No IRQ manual configuration is required.

Each device being installed must be assigned a unique identifier called a SCSI Target ID (this is done by jumper on the device or through the SCSISelect Configuration Utility when supported). SCSI peripherals that support the SCAM protocol can have SCSI IDs automatically assigned to them, if the Plug and Play SCAM Support option in the SCSISelect's Advanced Configuration Options is set to Enabled.

8.1 FIRST SCREEN

To run the SCSISelect program, type `7880cfg.exe` at the DOS prompt, then press the <Enter> key.

Two options are available from this screen:

1. **Configure/View Host Adapter Settings:** This option allows configuring and viewing host adapter settings. The default settings are indicated with an asterisk (*) in the pop-up windows: These settings are appropriate for most systems.
2. **SCSI Disk Utilities:** This option includes low level formatting of SCSI hard disks and verifying disk media.

NOTE

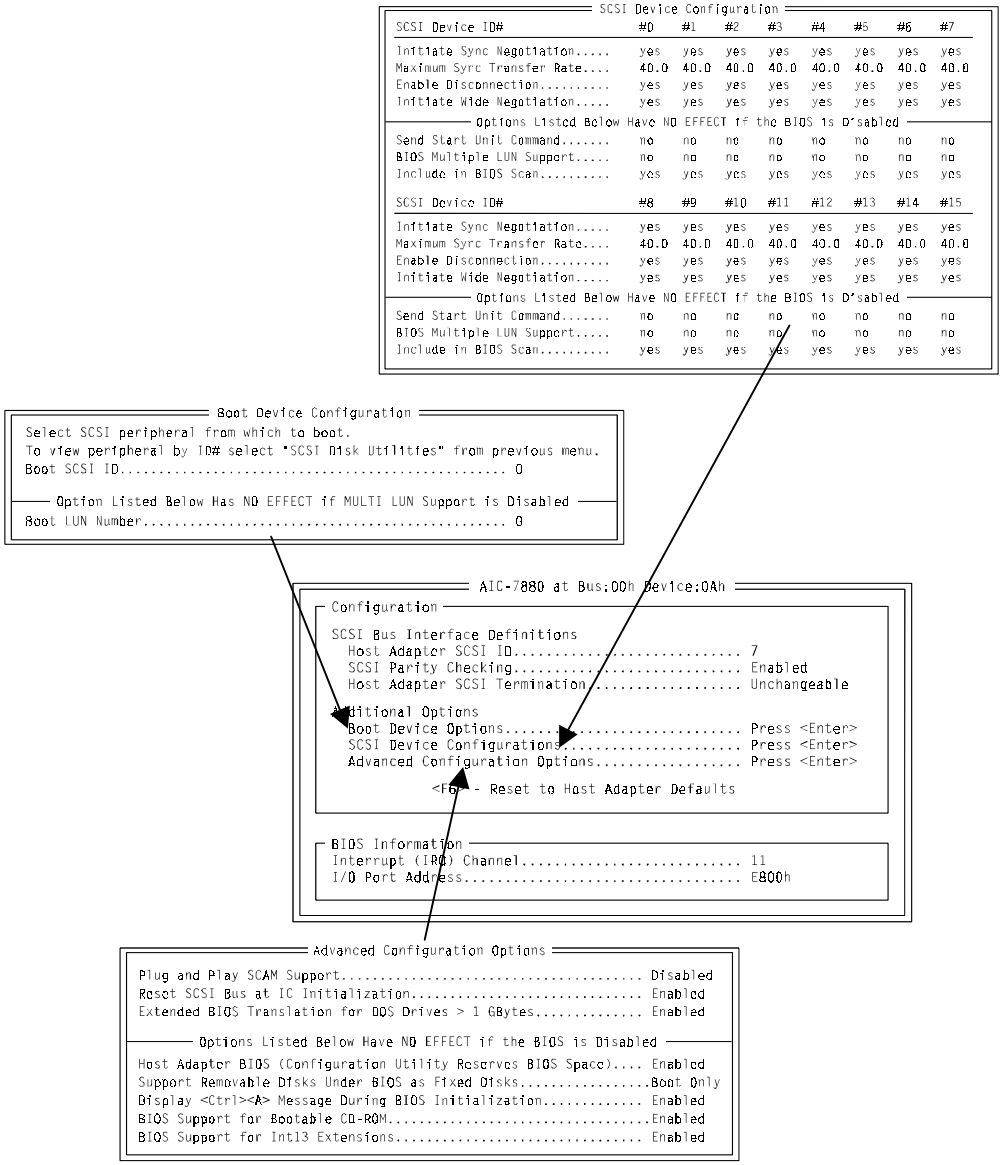
Depending on the W11 SCSI Mode jumper, the number of SCSI devices appearing on the screens will vary.

The 16-bit mode allows 16 SCSI ID numbers between 0 and 15 (7 is the host adapter, with the highest priority; the priority of the remaining IDs, in descending order, is 6 to 0, 15 to 8). The 8-bit mode allows 8 SCSI ID numbers between 0 and 7 (7 is the host adapter; the priority of the remaining IDs, in descending order, is 6 to 0).

Please note that the following sections will show only the 16-bit screens with their default settings. However, in the description of the options, we will indicate any differences with the 8-bit screens.

8.2 CONFIGURE / VIEW HOST ADAPTER SETTINGS

The Configure/View Host Adapter Settings menu is described below:



Configure/View Host Adapter Settings

SCSI Bus Interface Definitions/Configuration	
Host Adapter SCSI ID	Sets the SCSI ID for the PCI-943 SCSI interface. The SCSI interface is set at 7, which gives it the highest priority on the SCSI bus. We recommend you do not change this setting.
SCSI Parity Checking	When set to Enabled, verifies the accuracy of data transfer on the SCSI bus. Leave this setting enabled unless any SCSI peripheral connected to the SCSI interface does not support SCSI parity.
Host Adapter SCSI Termination	This option cannot be changed when the W10 jumper is installed. BIOS setups are required. To enable or disable the SCSI termination .
SCSI Bus Interface Definitions/Additional Options	
Boot Device Options	**Press the ENTER key to open the pop-up window.**
. *Boot SCSI ID*:	Specifies the SCSI ID of your boot device.
. *Boot LUN num*	Specifies which LUN (Logical Unit Numbers) to boot from on your boot device. Multiple LUN Support must be enabled (see SCSI Device Configuration Options below).
SCSI Device Configurations	**Press the ENTER key to open the pop-up window.**
. *Initiate Sync Negociation*	When set to Yes, initiates synchronous data transfer negotiation (Sync Negotiation) between the peripheral and SCSI interface. Leave this setting to Yes unless any attached SCSI peripheral connected to the SCSI interface does not support synchronous negotiation.
. *Max. Sync Transfer Rate*	Determines the maximum synchronous data transfer rate the SCSI interface supports. The default maximum value for Wide-Ultra 16-bit is 40.0 (W11 jumper shorted). If your peripheral is not Wide, select a transfer rate of 20.0 (when W11 jumper is open, 20 is the maximum default).
. *Enable Disconnection*	When set to Yes, allows the SCSI peripheral to disconnect from the SCSI bus. Leave the setting at Yes if two or more SCSI peripherals are connected to the SCSI interface. If only one SCSI peripheral is connected, changing the setting to No results in slightly better performance.
. *Initiate Wide Negotiation*	This option does not appear if the W11 SCSI Mode jumper is set to 8-bit (jumper open). When set to Yes, the SCSI interface attempts 16-bit data transfer (wide negotiation). When set to No, the SCSI interface uses 8-bit data transfer unless the SCSI peripheral requests wide negotiation.
. *Send Start Unit Command*	When set to Yes, sends the Start Unit Command to the SCSI peripheral at bootup.
. *BIOS Multiple LUN Support*	When set to Yes, the SCSI BIOS provides boot support for a SCSI peripheral with multiple LUNs. Leave this setting to No if your boot device does not have multiple LUNs.
. *Include in BIOS Scan*	When set to Yes, the SCSI BIOS includes the peripheral as part of its BIOS scan at bootup.

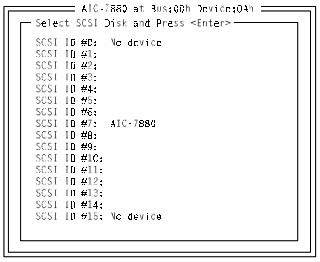
•••

Configure/View Host Adapter Settings (continued)

Advanced Config. Options	**Press the ENTER key to open the pop-up window.**
. *Plug-and-Play SCAM Support*	When set Enabled, the SCSI interface automatically assigns SCSI IDs to SCSI peripherals that support the SCAM protocol. The default is Disabled, but you can set it to Enabled even if you have a non-SCAM peripheral.
. *Reset SCSI Bus at IC Initialization*	When set to Enabled, the SCSI interface generates a SCSI bus reset during its power-on initialization and after a hard reset.
. *Extended BIOS Translation for DOS Drives > 1 GByte*	When set to Enabled, provides an extended translation scheme for SCSI hard disks with capacities greater than 1 GByte. This setting is necessary only for MS-DOS 5.0 or above; it is not required for other operating systems, such as NetWare or UNIX. The extended translation scheme supports disk drives as large as 8 GBytes. To partition a disk larger than 1 GByte controlled by the SCSI card BIOS, use the MS-DOS Fdisk command. **Back up your disk drives before changing the translation scheme.**
. *Host Adapter BIOS (Configuration Utility Reserves BIOS Space)*	Enables or disables the SCSI interface BIOS. Set it to Enabled, if you boot from a SCSI disk drive connected to the SCSI interface. Set it to Disabled if the peripherals on the SCSI bus (for example, CD-ROM drives) are controlled by software drivers and do not need the BIOS.
. *Support Removable Disks Under BIOS as Fixed Disks*	Determines which removable-media drives are supported by the SCSI card BIOS. Choices are as follows: Boot Only - Only the removable-media drive designated as the boot device is treated as a hard disk drive. All Disks - All removable-media drives supported by the BIOS are treated as hard disk drives. Disabled - No removable-media drives are treated as hard disk drives. Software drivers are required because the drives are not controlled by the BIOS. **Do not remove a removable-media cartridge from a SCSI drive controlled by the SCSI card BIOS while the drive is on. You may lose data. To allow removability of the media while the drive is on, install the removable-media software driver and set Support Removable Disks Under BIOS as Fixed Disks to Disabled.**
. *Display <Ctrl> <A> Messages during BIOS Initialization*	The setting does not affect the board, since the program is not part of the BIOS, but invoked as a DOS utility.
. *BIOS Support for Bootable CD-ROMs*	When set to Enabled, the SCSI BIOS allows booting from a CD-ROM drive.
. *BIOS Support for Int 13 Extensions*	When set to Enabled, the SCSI BIOS supports Int 13h extensions as required by Plug-and-Play. The setting can be either enabled or disabled if your system is not Plug-and-Play.

8.3 SCSI DISK UTILITIES

Once the SCSI Disk Utilities option is selected from the SCSISelect's first screen, the program scans the SCSI bus to determine the devices installed and displays a list of all SCSI IDs and the devices assigned to each ID, as follows:



Use the ↓ and ↑ keys to move the cursor to a specific ID and device, then press ENTER. A pop-up window appears, displaying these options:

SCSI Bus Interface Definitions/Additional Options	
Format Disk	Allows you to perform a low-level format on a hard disk drive. Each hard disk drive must be low-level formatted before you can use your operating system's partitioning and file preparation utilities, such as MS-DOS Fdisk and Format. **A low-level format will destroy all data on the drive. Be sure to back up your data before performing this operation. You cannot abort a low-level format once it is started**.
Verify Disk Media	Allows you to scan the media of a hard disk drive for defects. If the utility finds bad blocks on the media, it prompts you to reassign them; if you select yes, those blocks are no longer used. You can press Esc at any time to abort the utility.

9. INSTALLING DRIVERS

9.1 SCSI DRIVERS

To install the appropriate driver for your specific operating system, use the EZ-SCSI software located on the SCSI Utility Disk 1 (provided with your board).

9.2 VIDEO DRIVERS

Various drivers are provided for different operating systems and software. To install a driver, refer to the Setup program located on the Utility Disk (provided with your board).

9.3 ETHERNET DRIVERS

Various driver are provided for different operating systems and software. To install a driver, refer to the Setup program and the ReadMe.bat file located on the Utility Disk (provided with your board).

9.4 CHIPSET DRIVER FOR WINDOWS 95

The Windows 95 driver for the PIIX4 chipset is on the PIIX4 is provided on the Driver utility diskette.

9.5 OTHER DRIVERS

For other operating system drivers and installation instructions, or for more information, contact TEKNOR's Technical Support department.

10. UPDATING THE BIOS

The UBIOS 3.0 utility is provided for BIOS file operations within a disk and the Flash BIOS device. The program can be executed in one of two modes:

- **Interactive Mode**: which is a menu-driven program.
- **Batch Mode**: which makes possible to run online commands directly from the DOS prompt or using a Batch file.

NOTE

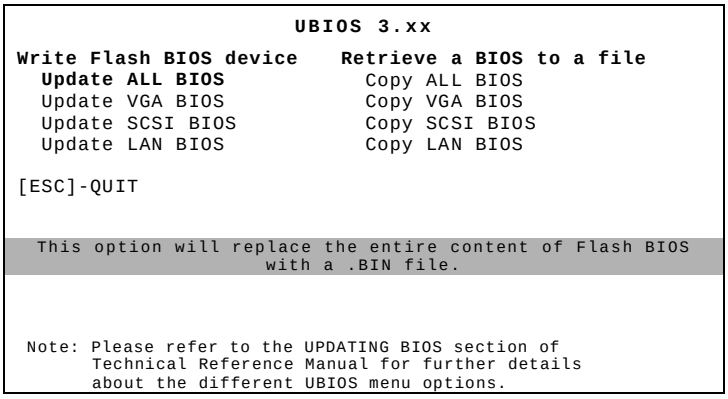
Using UBIOS will clear the CMOS Setup in Flash BIOS. Therefore, it is recommended that you take note of your Setup parameters (especially Hard Disk parameters), so you can reset them afterwards.

To update the BIOS files, these files must be in the same directory as the UBIOS.EXE program. Therefore, prior to running the program, make sure the files you wish to update and the UBIOS program file are in the same directory.

When you enter UBIOS, only the current directories are available. Within the UBIOS program, you can change the drive, but not the directory.

10.1 INTERACTIVE MODE

At the DOS prompt, type "UBIOS" from the DOS prompt, then press the ENTER key. At the presentation screen, hit any key to continue. The main menu appears as follows:



The main menu displays two groups of options: *Write Flash BIOS device* and *Retrieve a BIOS to a file*. The first group allows you to update the Flash BIOS device with a BIOS file stored on disk. The second group allows you to copy the contents of the Flash BIOS device to files on disk.
Use the arrow keys to move from one option to another. To select an option, press the ENTER key. To exit the program, press the ESC key (when at the main menu).

Four types of BIOS files are listed at the main menu:

ALL BIOS File This file combines all BIOS files contained in the Flash BIOS device in a single file. It has the .BIN extension.

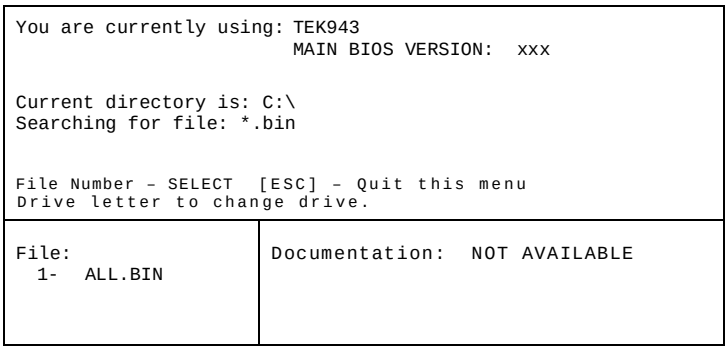
VGA BIOS File This file contains the VGA BIOS section of the Flash BIOS. There are two possible types of VGA BIOS files: files with the .VGA extension (supports CRT displays only) and files with the .BFP extension (supports CRT and Flat Panel displays).

SCSI BIOS File This file contains the SCSI BIOS section of the Flash BIOS. It has the .BIN extension.

LAN BIOS File This file contains the LAN BIOS section of the Flash BIOS. It has the .BIN extension.

10.1.1 Flash BIOS Updates

The **Update** options is similar to the following:



The files located in the current directory and corresponding to the type selected previously in the main menu are listed in the **File** window.

To change directory, type the drive letter. If there are any files of the type you selected in this directory, they will be displayed in the **File** window.

The **Documentation** window displays “NOT AVAILABLE”. It will be used in the future for displaying the contents of a .doc file.

To return to the previous menu, press the ESC key.

To begin the update process, type the item number corresponding to the file to transfer (**File** window). A confirmation message is displayed. Type “Y” to confirm and start the update operation, or type “N” to cancel.

The update status is displayed while data are transfered into the Flash. When the update is completed, the following screen appears:

```
                    FLASH BIOS UPDATE

Reading file:  all.bin                  100 %
PLEASE WAIT – Writing to Flash…                 100 %


Do you really want to update BIOS ? (Y/N)
```

```
Make sure that the watchdog is disabled by JUMPER DURING the next boot
ONLY.

Just to ensure a good CPLD update.
After the next boot you can enable the watchdog.
Please REBOOT as soon as possible …
Note:  Please refer to the UPDATING BIOS section of Technical Reference
       Manual.


Hit any key to continue …
```

Hit any key to return to the main menu.

NOTE

There may be slight changes to the Flash BIOS Update screen compared to those shown here for an Update ALL BIOS operation. Also, if an error occurs, these will be indicated on the screen.

Though the above screen mentions disabling the watchdog by jumper, on the PCI-943 it is only enabled/disabled by software. See section 15.3 for more detail.

10.1.2 Copying Flash BIOS

If you select one of the **Copy** options from the main menu, a screen similar to the following is displayed:

```
                    FLASH BIOS COPY

Enter filename for Flash BIOS (*.bin): 9nnall.bin

PLEASE WAIT – Writing ALL BIOS to 941all.bin  100%

DONE – Press any key to continue.
```

To begin a Flash Copy operation, type a filename (including the extension) for the file you are creating. It must be the same extension as the one indicated in parentheses on the screen. In the above example, the filename entered was "9nnall.bin".

Press ENTER to proceed.

The progress of the operation will display on the screen in percentage completed.

If the filename entered for the BIOS file already exists, the following message will appear on the screen:

File already exits! Overwrite? (Y/N)

If you choose to overwrite the existing file, its content will be lost.

To return to the main menu, hit any key on the keyboard.

NOTE

There may be slight changes to the Flash BIOS Copy screen compared to those shown here for a Copy ALL BIOS operation. Also, if an error occurs, it will be indicated on the screen.

10.2 BATCH MODE

While files can be manually selected using the Interactive Mode, Flash BIOS Update or Copy can be achieved through Batch Mode. The command line format is as follows:

`UBIOS -B [operation] [filetype] [filename] [options]`

where:

`-B` specifies that this is a Batch Mode command.

`[operation]` is the Flash BIOS operation you wish to perform, and can be replaced with one of three letters:

- `U` Update,
- `C` Copy, or
- `V` Verify (used to compare the contents of the Flash BIOS device and the specified BIOS file).

`[filetype]` is the filetype of the BIOS file to program (with an update operation) or to create (with a copy operation), and can be replaced with one of the following:

- `ALL` All BIOS files in a single file with the .BIN extension,
- `VGA` VGA BIOS file with the .VGA or .BFP extension,
- `SCSI` SCSI BIOS file with the .BIN extension,
- `LAN` for LAN BIOS file with the .BIN extension.

`[filename]` is the name of the BIOS file (including the extension) to program (with an update operation) or to create (with a copy operation), and can be replaced with the filename which corresponds to the filetype. For example, if "VGA" was listed as filetype, then the filename could be "FLAT.BFP".

`[options]` these are optional parameters that may be added:

- `/C` This option will not clear the CMOS Setup when updating main BIOS (AMIBIOS), however this is not recommended since the CMOS Setup should be updated when the main BIOS is changed.
- `/R` Instructs UBIOS to reset the board upon completion of an operation.
- `/?` To get a summary of the Batch Mode options from UBIOS. It will display a Batch options summary of valid UBIOS command lines. The same help information will also be displayed each time UBIOS detects an error in the command line.

10.3 CPLD UPGRADE AFTER THE BIOS UPDATE

At the first bootup following the update the Boot Block Flash BIOS using the UBIOS, the BIOS may need to upgrade the CPLD devices.

This message appears on the screen while the BIOS writes to the devices:

```
A hardware upgrade will be performed on some CPLDs. Follow the instructions
below with special care. Do not disturb the process.

DO NOT RESET OR POWER DOWN THE BOARD!!!

   □□□ Device 1 □□□   0% □□□□□□□□□□□□□□□□□□□□ 100%
   □□□ Device 2 □□□   0% □□□□□□□□□□□□□□□□□□□□ 100%

Status :
        Please wait...
```

The color of the boxes displayed in the message indicates these functions:

Device OK	Green
Device busy	Blue
Device will be updated	Red

If the upgrade was successful, the following message is displayed prior to rebooting:

```
Update complete successfully, wait for the automatic reboot.
Rebooting in 5 second(s).
```

If the update was not successful, the following message appears:

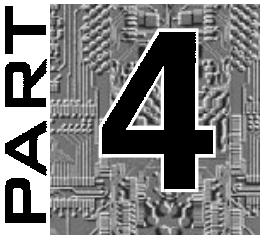
```
ERROR: general failure programming CPLDs!
Please contact Teknor Industrial Computers technical support.
```

You must contact TEKNOR's technical support for further instructions.

WARNING

After a BIOS update, the system must be restarted.

Do not interrupt the system in any way (power down, reset, mouse or keyboard functions) while the BIOS performs a CPLD hardware upgrade. This will damage the onboard devices and make your board inoperative !



APPENDIXES

A. BOARD SPECIFICATIONS

B. BOARD DIAGRAMS

C. CONNECTOR LOCATION & PINOUTS

D. LIST OF APPROVED VENDORS

E. MEMORY AND I/O MAPS

F. IRQLINES AND DMA CHANNELS

G. BIOS SETUP ERROR CODES

H. EMERGENCY PROCEDURE

A. BOARD SPECIFICATIONS

FEATURES	DESCRIPTIONS
Processor Option	One Intel Pentium® II SECC or Pentium® III SECC 2 processor at 333, 350, 400 and 450 MHz (maximum internal CPU clock speeds). Upgradable with future processor speeds. Supports Front Side Bus (FSB) speeds of 66 and 100MHz. The processor flush-mounted using Teknor's FlexMount™ mounting bracket (242-pin straight slot adapter).
Chipset	The Intel 82440BX AGPset
Internal Secondary Cache	512 KB, internal 64-bit wide ZPB non-blocking ECC Level 2 running at half the maximum internal CPU clock speed.
System Memory	Two vertical 168-pin DIMM sockets support SDRAM (Synchronous DRAM) memory configurations from 16 to 512 MB cacheable Supports 100 MHz SDRAM. Uses 3.3V, single-sided or double-sided 168-pin DIMMs. Supports 16MB, 32MB, 64MB, 128MB and 256MB DIMM modules (64-bit and 72-bit). ECC and parity supported with 72-bit modules.
Data Path	64-bit on CPU and memory bus 32-bit on the PCI bus 16-bit on the ISA bus
Bus Interfaces	Front Side Bus 100MHz PCI Bus 33MHz ISA Bus 8.33MHz High drive ISA buffers to support up to 20-slot backplane
Interrupts	11 edge sensitive and configurable 4 PCI level sensitive, configurable to any interrupt vector for PnP compatibility All ISA onboard interrupts are PnP compliant
Floppy Interface	Supports two floppy disk drives from 360KB to 1.44MB.
Enhanced IDE Ultra DMA/33 Interface	Can drive up to four enhanced IDE devices in master/slave configuration. Supports PIO mode 4 and Ultra DMA/33 with S.M.A.R.T. capability.
PCI Ethernet Interface	Intel 82558 Ethernet controller (Intel EthernetExpress Pro100+ equivalent) supports 10Base-T and 100Base-Tx Ethernet interface options via an RJ-45 connector on the board's I/O bracket. LED indicators are supported on the connector. Software drivers are supported for the most popular operating systems.

FEATURES	DESCRIPTIONS
PCI SCSI Interface	The SCSI controller – Adaptec AIC-7880 (AHA-2940AU equivalent)- supports Wide-Ultra SCSI (16-bit, 40MB per second) via the 68-pin Wide-Ultra SCSI connector. It also supports Fast SCSI II (8-bit, 10MB per second) and Fast-20 SCSI II (8-bit, 20MB per second) with accessory adapter cables available from TEKNOR. Active termination is provided onboard (enabled by jumpers). A SCSISelect Configuration Utility is available. Software drivers are supported for the most popular operating systems.
Serial Ports	Supports two RS-232 serial ports, with RS-422/RS-485 available on Serial Port 2. They are 16C550 compatible with internal 16-byte FIFO buffers for more efficient data transfers. The serial ports support VT100 mode for remote BIOS setup and console redirection.
Parallel Port	Supports multiple modes (Standard, EPP and ECP).
Universal Serial Bus (USB)	Supports two USB ports with optional cable/assembly bracket. The USB is an interface allowing for connectivity to many standard PC peripherals via an external port.
Video Support	C&T 69000, PCI 64-bit CRT video controller - Frame Accelerated Graphics Port (AGP) SVGA CRT controller with 2 MB video memory (SDRAM). CRT only with resolution up to 800x600x16M colors 1024x768x64K colors 1280x1024x256 colors Software drivers are available for the most popular operating systems.
Basic Interface Devices	Supports PS/2 keyboard, PS/2 mouse, AT standard keyboard, speaker, reset switch and hard disk LED
Serial ID Number Device	The 48-bit serial number device contains the board's unique serial number. The number can be read by software. For instructions on accessing this device, contact TEKNOR's Technical Support.
4KB Serial EEPROM	The 4KB serial EEPROM device is non-volatile memory. This storage area is completely user-defined. For instructions on accessing this device, contact TEKNOR's Technical Support.
Watchdog Timer	A two-stage software programmable watchdog timer drives a NMI on 1st stage, and the system reset on 2nd stage. Time out from 16ms to 4.5min.
Power Fail Detection	The power fail detector can monitor either the real time clock and CMOS RAM power source (3.6V onboard or offboard battery), or an offboard battery of arbitrary voltage (a resistor must be installed to provide the appropriate voltage attenuation).

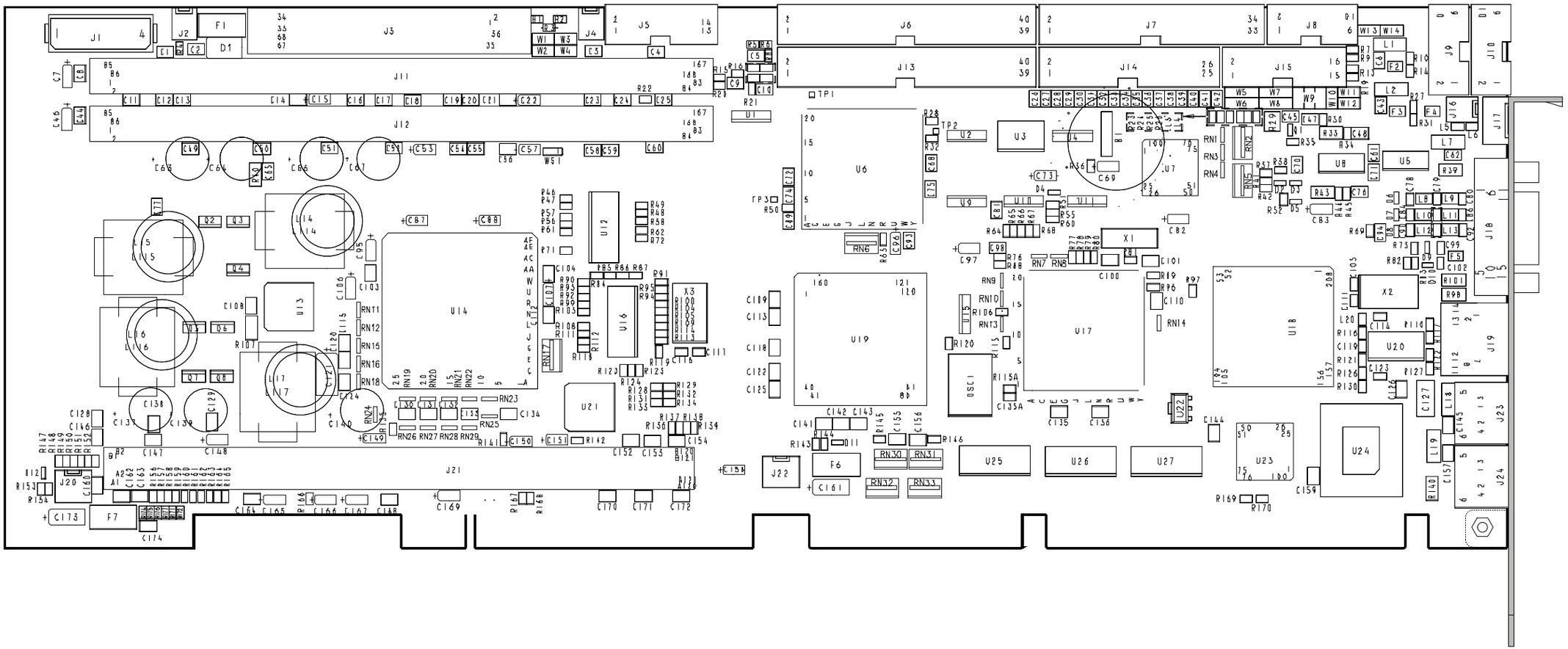
FEATURES	DESCRIPTIONS
ACPI	Supports ACPI (Advanced Configuration and Power Management Interface) Rev. 1.0.
Thermal Management	CPU temperature sensor / alarm included in the processor module.
Hardware Monitoring System	A system hardware circuit monitors all system voltages, ambient temperature, fan speeds and "cover open" discrete input.
Remote Reset	Remote reset from serial port console redirection on serial port on VT-100 mode.
Battery	A built-in lithium battery is provided for data retention of CMOS memory.
Operating Systems	Supports all operating systems developed for x86 and Pentium processors. These operating systems are to be validated on the product: MS-DOS® 6.2x, Windows® 3.11, Windows® 95/98, Windows® 95 OSR2, Windows® NT 4.0/5.0, QNX™.
Boot Block Flash BIOS	The 256KB boot block flash device contains all the board's BIOSes and is used for storing the nonvolatile configuration required for Plug and Play. The protected boot block section allows for the reprogramming of the BIOS. The main BIOS is an AWARD BIOS with ACPI, APM, DMI, Green and PnP features.
Power Supply	Voltage: +5V ±5% ; +12V ±5% *Pentium II* / *Pentium III* Current: 350MHz = 5.06A / 450MHz = 5.82A 400MHz = 5.64A / 500MHz = 6.24A 450MHz = 5.80A
Mechanical	Board Dimensions: 13.30" x 4.8" (338mm x 122mm)
Environmental	Operating: 0 to 55ºC (32 to 131F) with air flow @ 5 to 95% R.H. @ 40ºC Storage: -40 to +70ºC @ 5 to 95% R.H. @ 40ºC
Reliability	M.T.B.F.: over 80 000hours @ 40ºC (MIL-HDBK-217F) Designed to meet or exceed: Safety: UL 1950 ; CSA C22.2 No 950 ; EN 60950, IEC 950 EMI/EMC: FCC 47 CFR Part 15/CISPR22 CE Mark to EN55022/EN50082

B. BOARD DIAGRAMS

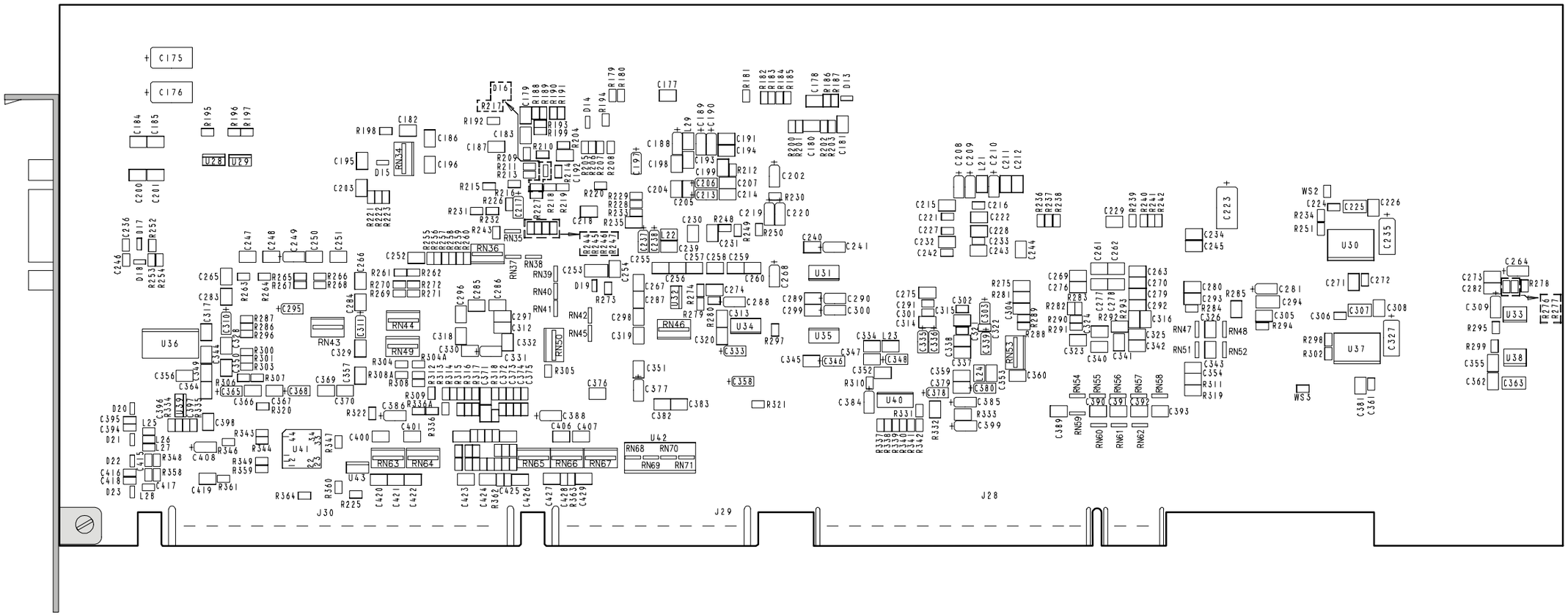
The following board diagrams are provided:

Number	Title
B-1	PCI-943 Assembly Diagram (Top)
B-2	PCI-943 Assembly Diagram (Bottom)
B-3	PCI-943 Mechanical Specifications Diagram

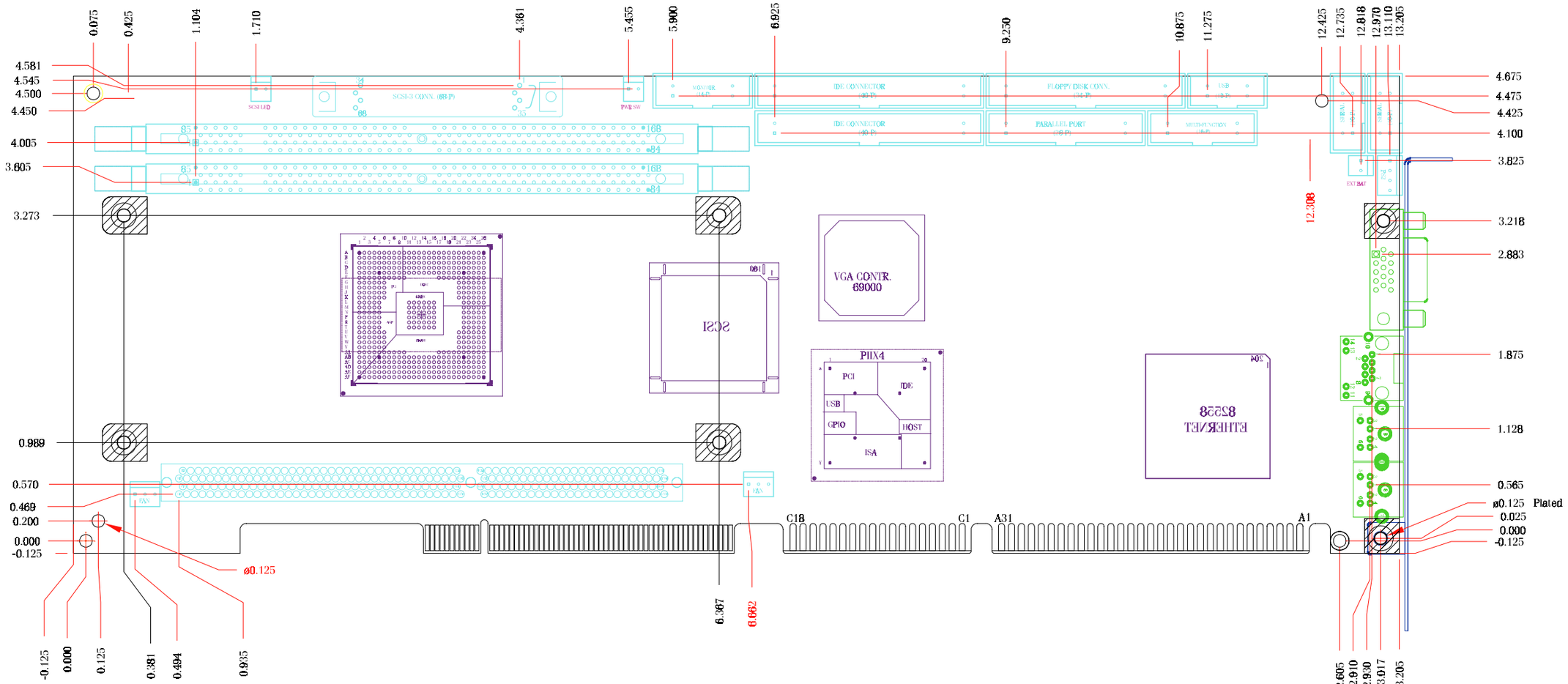
B.1 PCI-943 ASSEMBLY DIAGRAM (TOP)



B.2 PCI-943 ASSEMBLY DIAGRAM (BOTTOM)



B.3 PCI-943 MECHANICAL SPECIFICATION DIAGRAM



C. CONNECTOR PINOUTS

C.1 POWER SUPPLY CONNECTOR (J1)

Signal	
+12V	1
GND	2
GND	3
VCC	4

Top View

C.2 SCSI LED HEADER (J2)

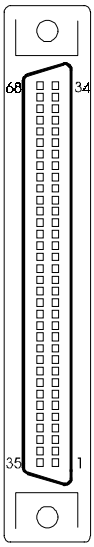
Signal	
+5V fused	1
LED signal	2

Front View

C.3 PCI WIDE-ULTRA SCSI INTERFACE CONNECTOR (J3)

Pin Number	Signal
1	GND
2	GND
3	GND
4	GND
5	GND
6	GND
7	GND
8	GND
9	GND
10	GND
11	GND
12	GND
13	GND
14	GND
15	GND
16	GND
17	Term Power
18	Term Power
19	Not Connected
20	GND
21	GND
22	GND
23	GND
24	GND
25	GND
26	GND
27	GND
28	GND
29	GND
30	GND
31	GND
32	GND
33	GND
34	GND

Top View



Pin Number	Signal
35	D12*
36	D13*
37	D14*
38	D15*
39	DPH*
40	D0*
41	D1*
42	D2*
43	D3*
44	D4*
45	D5*
46	D6*
47	D7*
48	DPL*
49	GND
50	GND
51	Term Power
52	Term Power
53	Not Connected
54	GND
55	ATN*
56	GND
57	BSY*
58	ACK*
59	RST*
60	MSG*
61	SEL*
62	C/D*
63	REQ*
64	I/O*
65	D8*
66	D9*
67	D10*
68	D11*

* Active Low Signal

C.4 POWER SWITCH HEADER (J4)

Signal	
Switch	1
GND	2

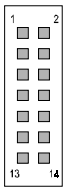
Front View

C.5 SYSTEM MONITOR CONNECTOR (J5)

Pin Number	
Signal	
GND	1
SOFTOFF*	3
GPIO1	5
APPFLT*	7
EXTFLT*	9
FANFLT*	11
CHASINT*	13

* Active Low Signal

Top View



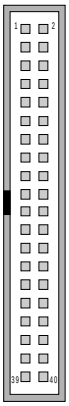
Pin Number	
	Signal
2	PWRBTN*
4	GND
6	GPIO2
8	CPUFLT*
10	GND
12	N.C.
14	GND

C.6 PRIMARY & SECONDARY EIDE CONNECTOR (J6 & J13)

Pin Number	
Signal	
RESET*	1
DD7	3
DD6	5
DD5	7
DD4	9
DD3	11
DD2	13
DD1	15
DD0	17
GND	19
DMARQ	21
DIOW*	23
DIOR*	25
IORDY	27
DMACK*	29
INTRQ	31
DA1	33
DA0	35
CS0*	37
LED (DASP*)	39

* Active Low Signal

Top View

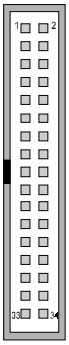


Pin Number	
	Signal
2	GND
4	DD8
6	DD9
8	DD10
10	DD11
12	DD12
14	DD13
16	DD14
18	DD15
20	Not Connected (KEY)
22	GND
24	GND
26	GND
28	GND (CSEL)
30	GND
32	Not Connected (IOCS16*)
34	Not Connected (PDIAG*)
36	DA2
38	CS1*
40	GND

C.7 FLOPPY DRIVE CONNECTOR (J7)

Pin Number	Signal
GND	1
GND	3
GND	5
GND	7
GND	9
GND	11
GND	13
GND	15
Not Connected	17
GND	19
GND	21
GND	23
GND	25
Not Connected	27
PRESENT* (GND)	29
GND	31
Not Connected	33

Top View



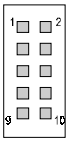
Pin Number	Signal
2	DRVEND*
4	Not Connected
6	Not Connected
8	INDEX*
10	MTR0*
12	FPDS1*
14	FPDS0*
16	MTR1*
18	FPDIR*
20	STEP*
22	WDATA*
24	WGATE*
26	TRK0*
28	WRTPRT*
30	RDATA*
32	HDSEL*
34	DSKCHG*

* Active Low Signal

C.8 USB HEADER (J8)

Pin Number	Signal
+5V fused	1
USBP0-	3
USBP0+	5
GND	7
GND	9

Top View

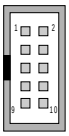


Pin Number	Signal
2	+5V fused
4	USBP1-
6	USBP1+
8	GND
10	GND

C.9 SERIAL PORT 2 & 1 - (J9 & J10) RS-232

Pin Number	Signal
1	DCD
3	RXD*
5	TXD*
7	DTR
9	GND

Top View



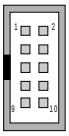
Pin Number	Signal
2	DSR
4	RTS
6	CTS
8	RI
10	Not Connected

* Active Low Signal

C.10 SERIAL PORT 2 - (J9) RS-422/RS-485

Pin Number	Signal
1	Leave Floating
3	RX(-)
5	TX(-)
7	Leave Floating
9	GND

Top View



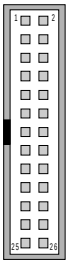
Pin Number	Signal
2	Leave Floating
4	RX(+)
6	TX(+)
8	Leave Floating
10	Not Connected

* Active Low Signal

C.11 PARALLEL PORT CONNECTOR (J14) - STANDARD MODE

Pin Number	Signal
1	STB*
3	PD0
5	PD1
7	PD2
9	PD3
11	PD4
13	PD5
15	PD6
17	PD7
19	ACK*
21	BUSY
23	PE
25	SLCT

Top View



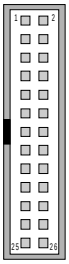
Pin Number	Signal
2	ALF*
4	ERR*
6	INIT*
8	SLCTIN*
10	GND
12	GND
14	GND
16	GND
18	GND
20	GND
22	GND
24	GND
26	GND

* Active Low Signal

C.12 PARALLEL PORT CONNECTOR (J14) - EPP MODE

Pin Number	Signal
1	WRITE*
3	PD0
5	PD1
7	PD2
9	PD3
11	PD4
13	PD5
15	PD6
17	PD7
19	INTR
21	WAIT*
23	N.C.
25	N.C.

Top View



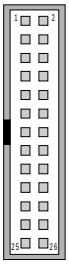
Pin Number	Signal
2	DATASTB*
4	N.C.
6	N.C.
8	ADDRSTRB*
10	GND
12	GND
14	GND
16	GND
18	GND
20	GND
22	GND
24	GND
26	GND

* Active Low Signal

C.13 PARALLEL PORT CONNECTOR (J14) - ECP MODE

Pin Number	Signal
1	STROBE*
3	PD0
5	PD1
7	PD2
9	PD3
11	PD4
13	PD5
15	PD6
17	PD7
19	ACK*
21	BUSY, PERIPHACK[2]
23	PERROR, ACKREVERSE[2]
25	SELECT

Top View



Pin Number	Signal
2	AUTOFD*, HOSTACK[2]
4	FAULT*[1], PERIPHRQST*[2]
6	INIT*[1], REVERSERQST*[2]
8	SELECTIN*[1,2]
10	GND
12	GND
14	GND
16	GND
18	GND
20	GND
22	GND
24	GND
26	

* Active Low Signal
[1] Compatible Mode
[2] High Speed Mode

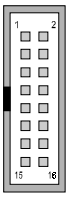
NOTE

For more information on the ECP protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard (available from Microsoft Corporation) or contact our Technical Support department.

C.14 MULTI-FUNCTION CONNECTOR (J15)

Pin Number	
Signal	
KCLK	1
KDAT	3
+5V fused	5
SPKR	7
Not connected	9
DOWNLD*	11
PBRES*	13
HDACT*	15

Top View



Pin Number	
	Signal
2	GND
4	GND
6	+5V fused
8	+5V fused
10	GND
12	GND
14	GND
16	+5V fused

* Active Low Signal

C.15 OFFBOARD BATTERY HEADER (J16)

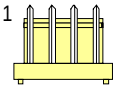
Signal	
Battery (+)	1
Battery (-)	2

Front View

C.16 PS/2 MOUSE HEADER (J17)

Pin Number	
Signal	
MCLOCK	1
GND	2
MDATA	3
+5V fused	4

Front View



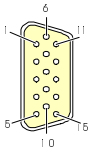
C.17 CRT VGA INTERFACE CONNECTOR (J18)

Signal	
RED	1
GREEN	2
BLUE	3
Not Connected	4
GND	5

Signal	
Analog GND	6
Analog GND	7
Analog GND	8
Not Connected	9
GND	10

Signal	
Not Connected	11
DDC data	12
HSYNC	13
VSYNC	14
DDC clock	15

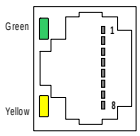
Front View



C.18 ETHERNET 10BASE-T/100BASE-TX CONNECTOR (J19)

Signal	
TX+	1
TX-	2
RX+	3
Not Connected	4
Not Connected	5
RX-	6
Not Connected	7
Not Connected	8

Front View



C.19 FAN HEADERS (J20 & J22)

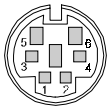
Signal	
SENSE	1
+12V fused	2
GND	3

Front View

C.20 PS/2 MOUSE CONNECTOR (J23)

Signal	
MDATA	1
Not Connected	2
GND	3
5V fused	4
MCLOCK	5
Not Connected	6

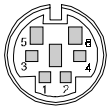
Front View



C.21 PS/2 KEYBOARD CONNECTOR (J24)

Signal	
KDATA	1
Not Connected	2
GND	3
+5V fused	4
KCLOCK	5
Not Connected	6

Front View



C.22 PCI BUS EDGE CONNECTOR

Pin Number		Pin Number		Pin Number		Pin Number	
component side			solder side	component side			solder side
+5V (TRST*)	E1	F1	N.C. (-12V)	C/BE0*	E52	F52	AD08
+12V	E2	F2	N.C. (TCK)	N.C. (3.3V)	E53	F53	AD07
N.C. (TMS)	E3	F3	GND	AD06	E54	F54	N.C. (+3.3V)
TD	E4	F4	TD	AD04	E55	F55	AD05
+5V	E5	F5	+5V	GND	E56	F56	AD03
INTA*	E6	F6	+5V	AD02	E57	F57	GND
INTC*	E7	F7	INTB*	AD00	E58	F58	AD01
+5V	E8	F8	INTD*	+5V	E59	F59	+5V
CLKC	E9	F9	REQ3*	REQ64*	E60	F60	ACK64*
+5V	E10	F10	REQ1*	+5V	E61	F61	+5V
CLKD	E11	F11	GNT3*	+5V	E62	F62	+5V
GND	E12	F12	GND				
GND	E13	F13	GND				
GNT1*	E14	F14	CLKA				
RST*	E15	F15	GND				
+5V (I/O)	E16	F16	CLKB				
GNT0*	E17	F17	GND				
GND	E18	F18	REQ0*				
REQ2*	E19	F19	+5V				
AD30	E20	F20	AD31				
N.C. (+3.3V)	E21	F21	AD29				
AD28	E22	F22	GND				
AD26	E23	F23	AD27				
GND	E24	F24	AD25				
AD24	E25	F25	N.C. (+3.3V)				
GNT2*	E26	F26	C/BE3*				
N.C. (+3.3V)	E27	F27	AD23				
AD22	E28	F28	GND				
AD20	E29	F29	AD21				
GND	E30	F30	AD19				
AD18	E31	F31	N.C. (+3.3V)				
AD16	E32	F32	AD17				
N.C. (+3.3V)	E33	F33	C/BE2*				
FRAME*	E34	F34	GND				
GND	E35	F35	IRDY*				
TRDY*	E36	F36	N.C. (+3.3V)				
GND	E37	F37	DEVSEL*				
STOP*	E38	F38	GND				
N.C. (+3.3V)	E39	F39	LOCK*				
SDONE (Not	E40	F40	PERR*				
Supported)	E41	F41	N.C. (+3.3V)				
SBO* (Not	E42	F42	SERR*				
Supported)	E43	F43	N.C. (+3.3V)				
GND	E44	F44	C/BE1*				
PAR	E45	F45	AD14				
AD15	E46	F46	GND				
N.C. (+3.3V)	E47	F47	AD12				
AD13	E48	F48	AD10				
AD11	E49	F49	GND				
GND							
AD09							

* Active Low Signal, N.C. Not Connected

C.23 ISA BUS EDGE CONNECTOR

Pin Number component side		Pin Number solder side		Pin Number component side		Pin Number solder side	
IOCHK*	A1	B1	GND	SBHE*	C1	D1	MEMCS16*
SD7	A2	B2	RESETDRV	LA23	C2	D2	IOCS16*
SD6	A3	B3	+5V	LA22	C3	D3	IRQ10
SD5	A4	B4	IRQ9	LA21	C4	D4	IRQ11
SD4	A5	B5	N.C. (-5V)	LA20	C5	D5	IRQ12
SD3	A6	B6	DRQ2	LA19	C6	D6	IRQ15
SD2	A7	B7	N.C. (-12V)	LA18	C7	D7	IRQ14
SD1	A8	B8	ZEROWS*	LA17	C8	D8	DACK0*
SD0	A9	B9	+12V	MEMR*	C9	D9	DRQ0
IOCHRDY	A10	B10	GND	MEMW*	C10	D10	DACK5*
AEN	A11	B11	SMEMW*	SD8	C11	D11	DRQ5
SA19	A12	B12	SMEMR*	SD9	C12	D12	DACK6*
SA18	A13	B13	IOW*	SD10	C13	D13	DRQ6
SA17	A14	B14	IOR*	SD11	C14	D14	DACK7*
SA16	A15	B15	DACK3*	SD12	C15	D15	DRQ7
SA15	A16	B16	DRQ3	SD13	C16	D16	+5V
SA14	A17	B17	DACK1*	SD14	C17	D17	MASTER*
SA13	A18	B18	DRQ1	SD15	C18	D18	GND
SA12	A19	B19	REFRESH*				
SA11	A20	B20	SYSCLK				
SA10	A21	B21	IRQ7				
SA9	A22	B22	IRQ6				
SA8	A23	B23	IRQ5				
SA7	A24	B24	IRQ4				
SA6	A25	B25	IRQ3				
SA5	A26	B26	DACK2*				
SA4	A27	B27	TC				
SA3	A28	B28	BALE				
SA2	A29	B29	+5V				
SA1	A30	B30	OSC				
SA0	A31	B31	GND				

* Active Low Signal, N.C. Not Connected

D. LIST OF APPROVED VENDORS

The following is list of recommended devices and connectors for use on the PCI-943. Many other models are available and function equally well. Users are encouraged to check with their local distributors for comparable substitutes.

D.1 RECOMMENDED DRAM DEVICES

Recommended DRAM devices for the 168-pin sockets have these features:

- 3.3V only, single-sided or double-sided.
- Unbuffered 100 MHz SDRAM.
- Serial Presence Detect (SPD) EEPROM.
- 64-bit and 72-bit DIMMs.
- Error Checking and Correction (ECC) or parity bit, with 72-bit DIMMs.
- Compliant with Intel's PC SDRAM Unbuffered DIMM Specification, Rev 1.0.

The recommended DRAM devices are listed below:

DIMM	VENDOR	PART NUMBER
16MB (2M*72) SDRAM 100MHz	CENTON	CINT16M/P100S1
32MB (4M*72) SDRAM 100MHz	CENTON	CINT32M/P100S1
64MB (8M*72) SDRAM 100MHz	CENTON	CINT64M/P100S1
128MB (16M*72) SDRAM 100MHz	CENTON	CINT128M/P100S1
256MB (32M*72) SDRAM 100MHz	CENTON	CINT256M/P100S1

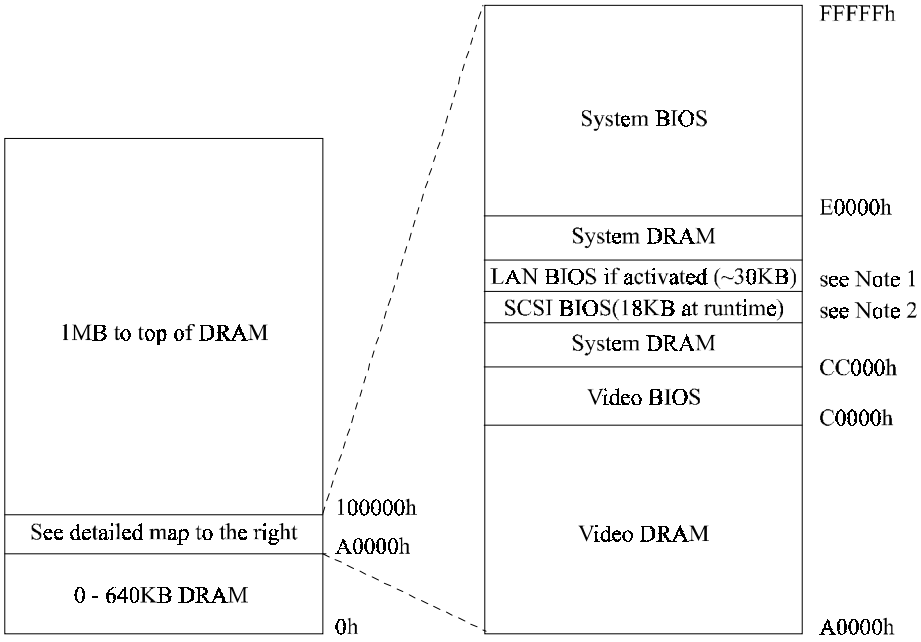
D.2 CABLES, ADAPTERS & MATING CONNECTORS

The following cable assembly and mating connectors are recommended for interfacing with the I/O devices. The mating parts shown here do not have a strain relief but one may be added.

Connector	Cable & Adapter: TEKNOR Part No.	Mating Part: Vendor Part No.
SCSI LED (J2)	Not Available	Molex 22-01-3027 (housing), Molex 08-50-0114 (crimp).
SCSI (J3)	SCSI cable 3-feet 68-pin male to 68-pin male: 150-359-00. SCSI cable 6-feet 68-pin male to 68-pin male: 150-360-00. 2-position SCSI cable 50-pin: 150-183. SCSI adapter 68-pin male to 50-pin male: 150-357-00. SCSI adapter 68-pin female to 50-pin female: 150-358-00.	50-pin flat cable connector: AMP 1-746285-0 [optional strain relief: 499252-4], Robinson Nugent IDS-C50PK-TG, Thomas & Betts 622-5030 [optional strain relief: 622-5041.
IDE Hard Disks (J6, J13)	IDE double connector HD cable 18": 150-259.	40-pin flat cable connector: AMP 746285-9 [optional strain relief: 499252-1], Robinson Nugent IDS-C40PK-TG, Thomas & Betts 622-4030 [optional strain relief: 622-4041].
Floppy Disk (J7)	Floppy disk cable 18": 150-051.	34-pin flat cable connector: Amp 746285-8 [optional strain relief: 499252-6], Robinson Nugent IDS-C34PK-TG, Thomas & Betts 622-3430 [optional strain relief: 622-3441].
USB (J8)	Universal Serial Bus (USB) cable / bracket: 150-316-00.	-
Serial Ports 2/1 (J9, J10)	COM to DB9 cable 18": 150-019	10-pin flat cable connector: Amp 746285-1 [optional strain relief: 499252-5], Robinson Nugent IDS-C10PK-TG, Thomas & Betts 622-1030 [optional strain relief: 622-1041].
Parallel Port (J14)	Printer cable 10" with bracket: 150-172.	26-pin polarized IDC female socket connector: Amp 746285-6 [optional strain relief: 499252-3], Robinson IDS-C26PK-TG, Thomas & Betts 622-2630 [optional strain relief: 622-2641].
Multi-Function (J15)	22' keyboard cable: 150-018-01.	16-pin flat cable connector: Amp 746285-3 [optional strain relief: 499252-8], Robinson Nugent IDS-C16PK-TG, Thomas & Betts 622-1630 [optional strain relief: 622-1641].
PS/2 Mouse (J17)	PS/2 mouse cable shielded: 150-337-00.	Molex 22-01-3047 (connector), Molex 20-50-0114 (crimp).

E. MEMORY AND I/O MAPS

E.1 MEMORY MAP



Note 1: LAN BIOS address may vary.

Note 2: SCSI BIOS address may vary.
Size only 2KB if no device.

Address	Function
00000-9FFFF	0-640 KB DRAM
A0000-BFFFF	Video DRAM
C0000-CBFFF	Video BIOS
D8000-FFFFF	System DRAM
	LAN BIOS around 30KB if activated, address may vary
	SCSI BIOS 18KB at runtime, 2KB if no device, address may vary
100000-Top of DRAM	1 MB - Top of DRAM

E.2 I/O MAP

Address	Optional Address	Optional Address	Optional Address	Function
000-01F				DMA Controller 1
020-03F				Interrupt Controller 1
040-05F				Timer
060-06F				Keyboard
070-07F				Real-time clock
080-09F				DMA Page Register
0A0-0BF				Interrupt Controller 2
0C0-0DF				DMA Controller 2
0F0-0F1, 0F8-0FF				Math Coprocessor
190-197	290-297	390-397		TEKNOR Control Port
1F0-1F7, 3F6				Primary IDE
170-177, 376				Secondary IDE
3F0-3F7	370-377			Floppy Disk
378-37A	3BC-3BE	278-27A		Parallel Port (LPT1 by default)
3F8-3FF (COM1)	2F8-2FF (COM2)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 2 (COM2 by default)
3C0-3CF, 3D0-3DF, 3B0-3BB				Graphics Controller (I2C Port)

NOTE

The I/O addresses for the onboard Plug and Play Ethernet device are automatically allocated by the System BIOS.

F. IRQ LINES AND DMA CHANNELS

F.1 IRQ LINES

The PCI-943 board is fully PC compatible with interrupt steering for PCI plug and play compatibility. The IRQ lines are assigned as follows:

Controller # 1		Controller # 2	
IRQ 0	Timer Output 0	IRQ 8	Real-Time Clock
IRQ 1	Keyboard (Output Buffer Full)	IRQ 9	Available [1]
IRQ 2	Cascade Controller # 2	IRQ 10	Available [1]
IRQ 3	Serial Port 2 *	IRQ 11	Available [1]
IRQ 4	Serial Port 1 *	IRQ 12	PS/2 Mouse
IRQ 5	Parallel Port 2 * or Available [1]	IRQ 13	Coprocessor Error
IRQ 6	Floppy Controller *	IRQ 14	Primary IDE * or available [1]
IRQ 7	Parallel Port 1 * or Available [1]	IRQ 15	Secondary IDE * or available [1]

* All functions marked with an asterisk (*) can be disabled or reconfigured.
[1] Available lines service on board and external PCI/ISA PnP devices or a Legacy ISA device.

F.2 DMA CHANNELS

The PCI-943 features the functionality of two 8237 DMA controllers. Eight DMA channels are available.

According to Plug and Play standards, the system BIOS automatically allocates DMA Channel 1 or 3 for the parallel port's ECP mode. Channel 2 is reserved for the floppy controller and Channel 4 is used to cascade Channels 0 through 7 to the microprocessor.

The DMA channels are assigned as follows:

DMA Channel	Function
DMA 0	Available
DMA 1	PnP available (ECP)
DMA 2	Floppy controller
DMA 3	PnP available (ECP)
DMA 4	Cascade controller # 1
DMA 5	PnP available
DMA 6	PnP available
DMA 7	PnP available

G. BIOS SETUP ERROR CODES

G.1 POST MESSAGES

During the Power On Self Test (POST), if the BIOS detects an error requiring your attention, it will either sound a beep code, display a message, or both.

If a message is displayed, it will be accompanied by:
"**PRESS F1 TO CONTINUE, DEL TO ENTER SETUP**".

Post Code	Description
xx	Post code counter displaying emergency file block number loaded from floppy.
11	Begin the flash reprogramming process.
22	Error when getting the boot block flash ID code.
33	Error when erasing the boot block flash.
44	Error when programming the boot block flash.
55	Success of the boot block recovery code .

G.2 POST BEEP

Currently there is only one beep code in the Main BIOS (more in Emergency Procedure, Appendix H.3). This code indicates that a video error has occurred and BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps.

Post Code	Beepcode	Description
41	**-*	Enterring the boot block recovery code (i.e. Main BIOS checksum error).
22	*-*-*	Error when getting the boot block flash ID code.
33	*-*-*-*	Error when erasing the boot block flash.
44	*-*-*-*-*	Error when programming the boot block flash.
55	*-*	Success of the boot block recovery code. The board is ready to be manually reset.

* 1 Beep code
\- Silence

G.3 ERROR MESSAGES

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

CMOS BATTERY HAS FAILED

CMOS battery is no longer functional and should be replaced, or battery jumper is removed and should be installed.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This can indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace it if necessary. It can also happen if the battery jumper is removed: in such a case, it should be installed.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP

Type of diskette drive installed in the system is different from CMOS definition. Run Setup to reconfigure the drive type correctly.

DISPLAY TYPE HAS CHANGED SINCE LAST BOOT

Since last powering off the system, the display adapter has been changed. You must configure the system for the new display type.

ERROR ENCOUNTERED INITIALIZING HARD DRIVE

Hard drive cannot be initialized. Be sure the adapter is installed correctly and all cables are correctly and firmly attached. Also be sure the correct hard drive type is selected in Setup.

ERROR INITIALIZING HARD DRIVE DISK CONTROLLER

Cannot initialize controller. Make sure the cord is correctly and firmly installed on the CPU board. Be sure the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set on the hard drive.

FLOPPY DISK CNTRLR ERROR OR NO CNTRLR PRESENT

Cannot find or initialize the floppy drive controller. Make sure the controller is installed correctly and firmly. If there are no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause BIOS to ignore the missing keyboard and continue the boot.

MEMORY ADDRESS ERROR AT ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory.

MEMORY PARITY ERROR AT ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory.

MEMORY VERIFY ERROR AT ...

Indicates an error verifying a value already written to memory. You can use this location along with the memory map for your system to find and replace the bad memory.

OFFENDING SEGMENT

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

PRESS A KEY TO REBOOT

This will be displayed at the bottom of the screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a non-maskable interrupt condition during boot, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

RAM PARITY ERROR - CHECKING FOR SEGMENT ...

Indicates a parity error in Random Access Memory.

G.4 POST CODES

NOTE

ISA POST codes are output to port address 80h.

POST (hex)	Name	Description	
01	BOOT BLOCK	Boot Block in EMERGENCY : Clear Base Memory Area.	
03	Initialize Chips	1. Clear CMOS shutdown byte. 2. Initialize EISA extended registers. (Not for us since we don't have EISA bus.)	
04	Test Memory Refresh Toggle	RAM must be periodically refreshed in order to keep the memory from decaying.	
05	Blank Video, Initialize Keyboard	1. Clear CMOS reset status byte. 2. Early Keyboard initialization.	Boot Block in EMERGENCY: Initialize Keyboard Controller.
06	EPROM Checksum	1. Test F000h segment shadow readable and writeable for POST access correct. If not, show POST FE and beep continuously… 2. Autodetect Flash EPROM.	
07	Test CMOS Interface and Battery Status	1. Install the TEKNOR segment. 2. Verifies CMOS is working correctly (walking bit test). 3. Restore CMOS from Flash if option is enabled. 4. Check for OVERRIDE KEY (INSERT key).	
08	Program Chipset default	Program Chipset default (show POST BEh).	
09	Early Cache Initialization	1. Check for Intel's and/or Cyrix CPU. 2. Early Cache Initialization when cache is separated from chipset. 3. Turn off Gate A20.	
0A	Setup Interrupt Vector Table	1. Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize int. 00h-1Fh according to INT_TBL. 2. Early Power Management Initialization.	
0B	Test CMOS RAM Checksum	1. Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize int. 00h-1Fh according to INT_TBL. 2. Early Power Management Initialization.	
0C	Initialize Keyboard	1. Open Xilinx I/O Port location to x90h (X=1,2 or 3) inside the chipset (if necessary). 2. Disable (if necessary). Thermal Management. 3. Disable (if necessary) Ethernet Chip.Set IDE Detect counter to 0. 4. Set CD-ROM found variable to 0. 5. Initialize zone 40:0h for the keyboard buffer.	Boot Block 1st : Verify BIOS checksum. Boot Block in EMERGENCY 2nd : Init. vector 00h through 77h.

POST (hex)	Name	Description	
0D	Initialize Video Interface & Chipset	1. On M1 set the cache for the memory installed. 2. On PCI, do a PCI ROM init. 3. On P6, Init. Apic. 4. Init. Chipset. 5. Turn ON CPU Cache. 6. Set Maximum Speed. 7. Measure CPU Clock Speed. 8. Restore Speed. 9. Turn Off CPU Cache. 10. Early Video Shadow. 11. Read CMOS location 14h to find out type of video to use. Detect and initialize Video Adapter. 12. Init. T380 if necessary.	Boot Block in EMERGENCY: Try to init. Video Card…
0E	Test Video Memory	1. If CGA or MONO, test video memory. 2. Beep the speaker. 3. Show the LOGO. 4. Install VT100 driver if necessary. 5. Write sign-on message to screen. 6. Write Copyright message to screen. 7. Write Evaluation message to screen. 8. Show CPU type and speed.	
0F	Test DMA Controller 0	Test DMA Controller 0.	
10	Test DMA Controller 1	Test DMA Controller 1.	
11	Test DMA Page Registers	Test DMA Page Registers.	
12	Reserved	Reserved for 8254 Counter 0 - Not implemented.	
13	Reserved	Reserved for 8254 Counter 1 - Not implemented.	
14	Test Timer Counter 2	Test 8254 Timer 0 Counter 2.	
15	PIC Test 8259-1 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	
16	PIC Test 8259-2 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	
17	Test Struck 8259's Interrupt Bits	Nothing	
18	Test 8259 Interrupt functionality	Force an interrupt and verify that the interrupt occurred (IRQ 0 - clock int. 8h).	
19	Test Struck NMI Bits (Parity/ IO check)	Nothing.	
1A – 1E	Reserved	Reserved	
1F	Set EISA Mode	If EISA non-volatile memory checksum is good, execute EISA initialization. If no, execute ISA test and clear EISA mode flag. Test EISA Configuration Memory integrity (checksum & communication interface).	
20 – 2F	Enable Slot 0	Initialize slot 0 (System Board).to slot 15	
30	Size Base & Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB.	
31	Test Base & Extended Memory	1. Test base memory from 256K to 640K and extended memory above 1MB using various patterns. 2. The last test is filling memory with 0's. 3. On a quick memory test or if user press the ESC key while testing memory, only the last test is performed.	
32	Test EISA Extended Memory	If EISA Mode flag is set, then test EISA memory found in slots Initialization. NOTE 1: This will be skipped in ISA mode. NOTE 2: This POST also Detect & Report I/O PORTS and also Init. Super IO.	
33 – 3B	Reserved	Reserved	
3C	Setup Enable		
3D	Initialize & Install PS/2 Mouse	Detect if mouse is present. Initialize mouse. Install interrupt vector.	
3E	Setup Cache Controller	Initialize cache controller.	
3F - 40	Reserved	Reserved	

POST (hex)	Name	Description	
41	Initialize Floppy Drive & Controller	1. Verify if we should enter setup. If so, enter setup. 2. Initialize floppy disk drive controller and any drive.	Boot Block in EMERGENCY: Scan for Floppy for emergency disk…
42	Initialize Hard Drive & Controller	Initialize hard drive controller and any drive. (Call HD_INSTALL).	
43	Detect & Initialize Serial/Parallel/Joystick ports	Initialize any serial, parallel and game ports.	
44	Reserved	Reserved	
45	Detect & Initialize Math Coprocessor	Initialize Math Coprocessor.	
46	Reserved	Reserved	
47	Set Speed for Boot	Set Speed for Boot.	
48 – 4C	Reserved	Reserved	
4D	Init. PC-Speaker to LINE OUT	Enable access to PC-Speaker to LINE OUT and Enable/Disable it. (T934).	
4E	Manufacturing POST Loop or display Messages	1. Reboot if Manufacturing POST Loop pin is set. 2. Otherwise display any messages (i.e., any non-fatal errors that were detected during POST). 3. Enter SETUP if needed.	
4F	Security Check	Ask password security if needed.	
50	Write CMOS	Write all CMOS values back to CMOS-RAM and clear screen.	
51	Pre-Boot Enable	1. Enable Parity checker. 2. Enable NMI. 3. Enable cache before boot.	
52	Initialize Option (ROM scan)	1. Call POST 81 2. Initialize any ROMs present from C8000h to DBFFFh. Disable POST code from segment E0000h. 3. Initialize any ROMs present from DC000h to E0800h. NOTE: When FSCAN option is enabled, will initialize from C8000h to F7FFFh.	
53	Initialize Time Value	Initialize Time value in 40h: BIOS area.	
54 - 5F	Reserved	Reserved	
60		Store boot partition of head & cylinder.	
61	Final Init	For last µs detail before boot.	
62	Num Lock ON	Put Num Lock ON and Daylight Saving.	
63	Boot Attempt	1. Call POST 82. 2. Set Low stack. 3. Boot via int 19h.	
64 – 7F	Reserved	Reserved	
80	Teknor Segment Move 1	Install the Teknor segment from Flash to DC00:0h.	
81	Teknor Segment Move 2	Install the Teknor segment from DC00:0h to 7000:0h.	
82	Teknor Segment Move 3	Install the Teknor segment from 7000:0h to EC00:0h.	
83	Check & Program CPLD	Check & Program CPLD for valid UserCode & IDCode.	
84	Teknor CRC Check	Check if Teknor block have a valid CRC. If not, the Emergency procedure is launched.	
85 - AF	Reserved	Reserved	
B0	Spurious	If interrupt occurs in protected mode.	
B1	Unclaimed NMI	If unmasked NMI occurs, display: Press F1 to disable NMI, F2 reboot.	
B2 - BD	Reserved	Reserved	
BE	Early Prog Chipset Def.	Going to early program chipset to default values (called from POST_8s).	
BF	Program Chip Set	Called early at POST 0Dh to program chipset from CT-TABLE.	
C0	Turn ON/OFF Cache	OEM Specific - Cache control.	Boot Block: First POST.
C1	Memory presence	OEM Specific - Test to size on-board memory test.	Boot Block: Search for Boot Block Signature '*BBSS*".
C2	Early Memory Initialization	OEM Specific - Board Initialization.	
C3	Extended Memory Initialization	OEM Specific - Turn ON extended memory DRAM select.	Boot Block: Expand compressed BIOS
C4	Special Display Switch Handling	OEM Specific - Display/Video switch handling so that display switch errors never occur.	

POST (hex)	Name	Description	
C5	Early Shadow	OEM Specific - Early Shadow enable for fast boot.	Boot Block: Early Shadow System BIOS.
C6	Cache Programming	OEM Specific - Routine for programming which region are cacheable.	Boot Block: Cache Sizing
C7	Reserved	Reserved	
C8	Special Speed Switching	OEM Specific - Routine to handle speed switching.	
C9	Special Shadow Handling	OEM Specific - Normal Shadow routine.	
CA	Very Early Initialization	OEM Specific – Initialize hardware before any other hardware initialization.	
CB - CF	Reserved	Reserved	
D0	Power Management Full speed	Trying to go back or into full speed mode.	
D1	Power Management -- Doze mode	Trying to go or in Doze mode.	
D2	Power Management --Sleep mode	Trying to go or in Sleep mode.	
D3	Power Management – Suspend mode	Trying to go or in Suspend mode.	
D4 - DF	Debug	Available POST codes for use by source code customers during development.	
E0	Reserved	Reserved	
E1 - EE	Setup Page	Page 1 to 14	
EF	Shadow Error	In POST 6 to signal a Shadow Error.	
F0 - FE	Reserved	Reserved	
FF	Boot	The system is now booted or waiting for an OS.	

H. EMERGENCY PROCEDURE

Follow this procedure only in case of emergency such as a critical error during the boot block flash BIOS update (when using UBIOS utility program or saving AWARD parameters in flash) or if you meet one of the following symptoms at anytime.

H.1 SYMPTOMS

- No POST code on a power up (when using a POST code card).
- System stops at POST 41h (when using a POST code card; refer to the previous section), associated beep code is generated and the system tries to read from the floppy drive.
- Board does not boot, even after following all the steps indicated in Section 16.3.

H.2 GENERATE AN EMERGENCY DISKETTE

Use a system that has a 1.44 MB floppy drive A.

1. Insert the TEKNOR EMERGENCY diskette in drive A:
2. Copy the two files WDISK.COM and EMERDISK.TEK from drive A: to your hard drive (those files are available in your TEKNOR diskette package).
3. Remove the TEKNOR EMERGENCY diskette
4. Format a diskette in drive A:
5. At the DOS prompt of your hard drive (the same directory as the two files WDISK.COM and EMERDISK.TEK), type **`WDISK EMERDISK.TEK`** and then press Enter.

The program may display one of the following messages:

`"Emergency Code transferred"`

The emergency diskette has been successfully created. Take the appropriate actions and restart from step 4 if you see the following messages:

`"Write to disk failure!"`

Verify if your floppy diskette is write-protected.

`"The file to program in flash was not found"`

Be sure that EMERDISK.TEK file is in your current directory.

`"Unable to read the binary file" or "Unable to close the opened file"`

Possible floppy diskette corruption or bad data transfer between floppy disk and host system.

`"Unable to allocate a memory block of 256 Kbytes"`

Not enough memory to run the WDISK program.

H.3 EMERGENCY PROCEDURE

Running an EMERGENCY PROCEDURE.

1. Remove battery jumper (even if it is set to onboard or offboard).
2. Install the EMERGENCY diskette in the floppy drive A (1.44 MB) connected to the PCI-943 board.
3. Power on the board. (Nothing appears on the screen.)
4. Boot block flash update will be completed when you see POST code 55 (when using a POST code card; see Appendix-G) or hear the associated beep code or when the floppy drive stops. If you see POST code 22, 33 or 44, an error has occurred. You should repeat the emergency procedure. If repeated attempts at updating the boot block flash fail, i.e., you are unable to generate POST code 55, contact TEKNOR's Technical Support.
5. After the procedure is successfully completed, power down the board, set your battery jumper as it was previously and power up the board. Your PCI-943 boot block flash BIOS should be correctly programmed and the system should run properly.

NOTE

If the emergency disk has been lost, refer to the previous paragraph: Generate an Emergency Floppy Diskette.

GETTING HELP

At TEKNOR we take great pride in our customer's successes. We strongly believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, you may contact our Technical Support department at:

CANADIAN HEADQUARTERS

Tel.: (450) 437-5682

Fax: (450) 437-8053

If you have any questions about TEKNOR, our products or services, you may reach us at the above numbers or by writing to:

TEKNOR INDUSTRIAL COMPUTERS INC.

616 Cure Boivin

Boisbriand, Quebec

J7G 2A7 CANADA

LIMITED WARRANTY

TEKNOR INDUSTRIAL COMPUTERS INC. ("the seller") warrants its boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

Returning Defective Merchandise

If your TEKNOR product malfunctions, please do the following before returning any merchandise:

1) Call our Technical Support department in Canada at (450) 437-5682. Make certain you have the following at hand: the TEKNOR Invoice #, your Purchase Order #, and the Serial Number of the defective board.

2) Give the serial number found on the back of the board and explain the nature of your problem to a service technician.

3) If the problem cannot be solved over the telephone, the technician will further instruct you on the return procedure.

4) Prior to returning any merchandise, make certain you receive an RMA # from TEKNOR's Technical Support and clearly mark this number on the outside of the package you are returning. To request a number, follow these steps: make a copy of the request form on the following page, fill it out and fax it to us.

5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. **Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.**

6) When returning a TEKNOR board:

   i) Make certain that the board is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.

   ii) Ship prepaid to (but not insured, since incoming units are insured by TEKNOR):

TEKNOR INDUSTRIAL COMPUTERS INC.

616 Cure Boivin
Boisbriand, Quebec
J7G 2A7 CANADA

TEKNOR
INDUSTRIAL COMPUTERS INC.

RETURN TO MANUFACTURER AUTORIZATION REQUEST

Contact Name: _____

Company Name: _____

Street Address: _____

City: _____ **Province / State:** _____

Country: _____ **Postal / Zip Code:** _____

Phone Number: _____ **Fax Number:** _____

Extension: _____

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

ref.: RMA-03

Fax this form to TEKNOR's Technical Support department in Canada at (450) 437-8053