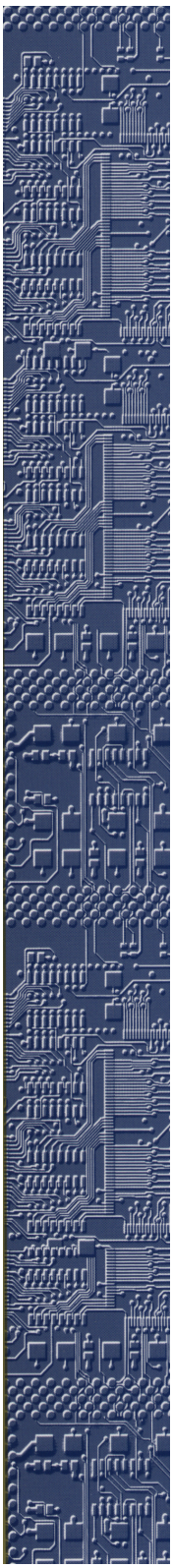

TEKNOR
INDUSTRIAL COMPUTERS INC.

PCI-941

MOBILE PENTIUM II INDUSTRIAL SBC

TECHNICAL REFERENCE MANUAL **VERSION 1.3**
November 1998

ref.: M941_1-3

FOREWORD

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Printed in Canada.

READ ME FIRST

EXERCISE CAUTION WHILE REPLACING LITHIUM BATTERY

WARNING

There is a danger of explosion if the battery is incorrectly replaced.

Replace the battery only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

ATTENTION

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie.

Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabriquant.

ACHTUNG

Explosionsgefahr bei falschem Batteriewechsel.

Verwenden Sie nur die empfohlenen Batterietypen des Herstellers. Entsorgen Sie die verbrauchten Batterien laut Gebrauchsanweisung des Herstellers.

ATENCION

Puede explotar si la pila no este bien reemplazada.

Solo reemplazca la pila con tipas equivalentes segun las instrucciones del manifacturo. Vote las pilas usadas segun las instrucciones del manifacturo.

OTHER WARNINGS

Please heed the following warnings concering the PCI-941 board:

⚠ BIOS Update & Automatic CPLD Hardware Upgrade

During the first system bootup after you update the Flash BIOS device with the BIOS utility, the BIOS may need to upgrade the CPLD devices. **Prior to the first system bootup after updating the BIOS, ensure that the watchdog is disabled (remove W7 jumper). During the bootup, do not interrupt the system in any way (power down, reset, mouse or keyboard functions). The devices will be damaged and your board rendered inoperative if the CPLD hardware upgrade process is disturbed!**

If your device upgrade was successful, the following message is displayed under the "Status:" line prior to rebooting:

```
Update complete successfully, wait for the automatic reboot.
Rebooting in 5 second(s).
```

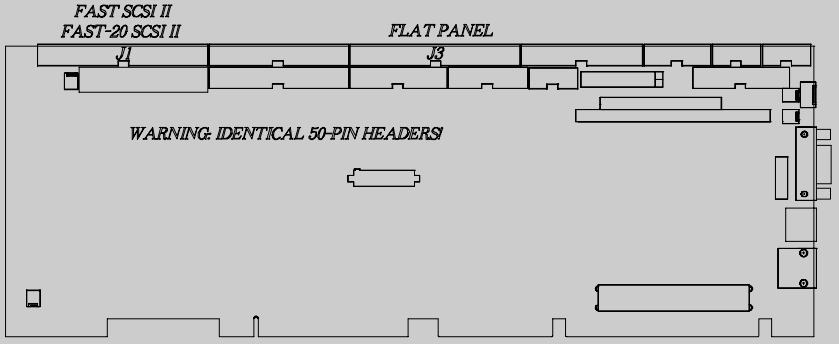
If the update is not successful, the following message appears under the "Status:" line:

```
ERROR: general failure programming CPLDs!
Please contact Teknor Industrial Computers technical support.
```

You must contact TEKNOR's technical support for further instructions.

⚠ Identical 50-pin SCSI and Flat Panel Connectors

Connect the Fast SCSI II cable and the Flat Panel cable to the PCI-941 board carefully, since both the J1 SCSI connector and the J3 Flat Panel connector are 50-pin headers.

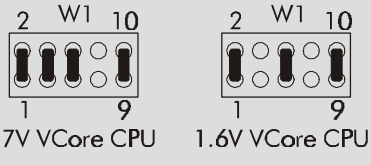


Faulty cable connections will damage the board!

Proper Setting of Processor Core Voltage

The VCORE jumper setting depends on the Core voltage (1.6V or 1.7V) of the CPU. For more information refer to Section 6 – *Setting Jumpers*:

W1 VCORE for Specific MPII Processors



Mobile Pentium II	
INTEL S-Spec	Core Voltage
SL2KH	1.7V
SL2KJ	1.7V
SL2RS	1.6V
SL2RR	1.6V
SL2RQ	1.6V

WARNING: Incorrect core voltage setting can cause damage to the processor!

Selecting the Right Flat Panel Power Voltage

Make sure you select the correct power voltage for your Flat Panel with the W9 jumper.

Incorrect power voltage can damage your Flat Panel!

IMPORTANT INFORMATION

Before operating your Single Board Computer, please note the following:

Award's Chipset Features Setup Parameters

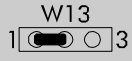
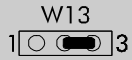
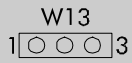
These parameters have been provided in Section 19 to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

Battery Configuration

Your computer board is equipped with a standard non-rechargeable lithium battery. To preserve the useful life of the battery, **the jumper which enables the battery is not installed when you receive the board**. If you need a jumper cap, we suggest you use the one on the Watchdog Timer jumper since it is rarely needed; if you wish to purchase jumper caps, you can contact TEKNOR's Sales department to order them.

CMOS Battery Backup

Before modifying CMOS setup parameters, ensure that the W13 battery selection jumper is installed to enable the CMOS battery back-up (* = factory setting).

W13	Battery Selection	
		 Onboard Battery
		 Offboard Battery
		 Battery Disconnected *

Connecting Flat Panel Video Display

The PCI-941 board supports many different types of Flat Panel displays. TEKNOR has fully tested a number of these panels and provides all the BIOS software support and the technical information needed.

If you have access to the Internet, many video BIOS files in a binary format and related interconnection charts in a PDF format are available on our web site. You can download these files, if you are a customer of TEKNOR and have a password from TEKNOR. If you do not have your password, contact TEKNOR's Technical Support to obtain it.

To download a video BIOS file or its interconnection chart file, follow this procedure:

1. Access the TEKNOR web site. Our address is http://www.teknor.com .
2. Go to the Support & Services section.
3. Scroll down the list of products until you find the name of your board and click on it. This selection is a link to the board's support area.
4. Click on the Video BIOS link.
5. The list of tested Flat Panel displays appears. If you find your particular display, you can then ask to download the associated BIOS or interconnection chart files by clicking the appropriate link.
6. A pop-up window appears. You must enter your password (case sensitive) and click the SUBMIT button. Entering your e-mail address is optional. Follow the instructions in subsequent pop-ups to download the file.

If you do not have access to our web site, or if you do not see the name of your Flat Panel, then you need to contact TEKNOR's Technical Support department. Since we are always testing new flat panels, it is possible that we have tested your particular type of panel display. Even if we have not tested it, TEKNOR's Technical Support can do it for you and supply the video BIOS and the technical information you need.

Flat Panel Cable Length

The Flat Panel Cable length for the SBC should be cut on the unconnected end to a recommanded maximum length of 18 inches from the high density connector. Though some Flat Panels may support longer flat cables, and TEKNOR has made allowance for this by providing more than 18 inches of cable, it is the customer's responsability to ensure that the additional length is fully supported by the Flat Panel's specifications.

Flat Panel Voltage Selection & V-PORT Connector

When the voltage level for the Flat Panel Control signal is set at 3.3V via the W9 jumper, only 3.3V logic levels can be used for the V-PORT connector.

Powering up the system

If you should encounter a problem, verify the following items:

- Make sure that all connectors are properly connected. On the standard flat ribbon cable used for the floppy connector, pin 1 is indicated by small red stripe. Verify that this red stripe is located on the appropriate side of the connector.
- Verify your boot diskette. It must be a system disk and it must be in proper working order.
- If the system still does not start up properly, you should try booting your system with only the power cord and video monitor connected to the board (this is the minimum required to see if the board is working).
- If you still are not able to start up your system, please refer to the Emergency Procedure in Appendix J.
- If you still are not able to get your board up and running, contact our Technical Support department for assistance.

Preventing Viruses

TEKNOR INDUSTRIAL COMPUTERS takes every precaution against computer viruses. For your protection, we have *safety sealed* all utility diskettes. If the seal is broken, **do not use the diskette**. Destroy the diskette immediately and contact our Technical Support department for further instructions at (450) 437-5682 (Canada) or at +49 811 / 600 15-0 (Germany).

To safeguard against computer viruses in general, do not freely lend your utility diskettes and regularly perform virus scans on all your computer systems.

Serial Ports Adapter Cables

When connecting serial ports, the use of Taïwanese adapter cables is not recommended, since the pinout is often incorrect. The direct crimp design offered by TEKNOR allows the simplest cable assembly. All these cables are available from TEKNOR by contacting the Sales department.

Using the J26 PS/2 Connector With Other Connectors

If J26 is jumper configured as a PS/2 mouse (W16:1-3, 2-4 shorted):

- Do not connect a PS/2 keyboard cable on the J26 connector.
- Do not connect two PS/2 mice simultaneously, one on the J16 mouse connector and the other on the J26 connector. Only one PS/2 mouse connector should be used.

If J26 is jumper configured as a PS/2 keyboard (W16: 3-5, 4-6 shorted):

- Do not connect a PS/2 mouse cable on the J26 connector.
- Do connect two keyboards simultaneously, one on the J5 multi-function connector (AT keyboard) and the other on the J26 connector (PS/2 keyboard).

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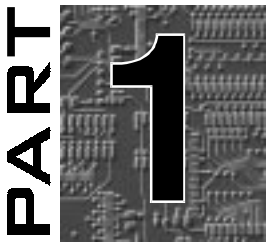
PART 4 - APPENDIXES



PRODUCT DESCRIPTION

1. PRODUCT OVERVIEW
2. FEATURES
3. COMPATIBILITY WITH TEKNOR SBC PRODUCTS

1. PRODUCT OVERVIEW

The PCI-941 PCI-ISA full-featured, full-sized single board computer is based on the Intel Mobile Pentium II (MPII) processor, the Intel 440BX chipset and the Cirrus Logic GD7556 PCI CRT / Flat Panel video interface with 2MB video memory (EDO DRAM).

The PCI-941 also features PCI 10Base-T/100Base-TX Ethernet, PCI Wide-Ultra SCSI, support for up to 768MB of system memory (with Registered SDRAM) on three 168-pin DIMM sockets, 512KB L2 cache, floppy controller, dual EIDE Ultra DMA/33 interface, upgradeable CompactFlash support, an USB 1.0 port supporting two connectors with optional cable/assembly bracket, two serial ports, parallel port, mouse port and keyboard port.

This high performance SBC plugs into a PICMG PCI-ISA passive backplane and provides 100% PC compatibility for system expansion slots. The board also provides expansion through the onboard PC/104 and PC/104-Plus connectors.

The SBC and backplane assembly is used as a substitute for the standard PC motherboard, and in general includes all of the standard interfaces and peripherals that are normally included in a top of the line PC. This compact solution allows an industrial user the possibililty of designing a system that uses standard x86 software and peripherals, but in an industrial environment where reliability, integration and service are of major concern.

2. FEATURES

The PCI-941 includes the following features:

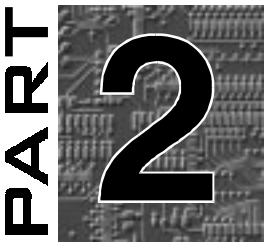
- **CPU Module Option**: The Intel Mobile Pentium II (MPII) processor at 233, 266, and 300MHz (maximum internal CPU clock speeds). Upgradable with future MPII processor speeds via the 240-pin BGA socket.
- **Internal Secondary Cache:** 512 KB, pipelined burst cache, operates at half the maximum internal CPU clock speed, Error Checking and Correction (ECC) capable.
- **System Memory:**
  - From 8 to 384MB using Synchronous DRAM (SDRAM), or from 8 to 768MB using Registered SDRAM (RSDRAM).
  - Three vertical 168-pin DIMM.
  - 3.3V, single-sided or double-sided 168-pin DIMMs.
  - Supports 8MB, 16MB, 32MB, 64MB, 128MB, and 512MB modules (64-bit and 72-bit). ECC and parity supported with 72-bit modules.
- **Floppy Interface:** Supports two floppy disk drives from 360KB to 2.88MB.
- **Enhanced IDE Ultra DMA/33 Interface:** Can drive up to four enhanced IDE devices. Supports PIO mode 4 and Ultra DMA/33 with S.M.A.R.T. capability.
- **CompactFlash Disk Option:** This module is a daughterboard with available capacities of 4, 10, 15, 20 or 24 MB. The CompactFlash is connected to the secondary IDE interface and configured as a master or slave disk. It is bootable and completely user upgradable (will support higher capacities when available).
- **PCI SCSI Interface:** The SCSI controller - Adaptec AIC-7880 - supports Wide-Ultra SCSI (16-bit, 40MB per second) via the 68-pin Wide-Ultra SCSI connector. It also supports Fast SCSI II (8-bit, 10MB per second) and Fast-20 SCSI II (8-bit, 20MB per second) via the 50-pin SCSI header. Active termination is provided onboard (enabled by jumpers). A SCSISelect Configuration Utility is available. Software drivers are supported for the most popular operating systems.
- **PCI Ethernet Interface:** Intel 82558 Ethernet controller supports 10Base-T and 100Base-Tx Ethernet interface options via an RJ-45 connector on the board's I/O bracket. LED indicators are supported on the connector. Software drivers are supported for the most popular operating systems.
- **Bus Support:**
  - ISA Bus IEEE P996 Specification: 16-bit standard, high drive ISA buffers.
  - PCI Local Bus Specification, Revision 2.1.
  - PCI Industrial Computer Manufacturers Group (PICMG) 2.0 Specification.
- **PC/104 and PC/104-Plus:** PC/104 ISA expansion header and PC/104-Plus PCI expansion header are available onboard.

- **Video Option:** The video system includes an integrated PCI 64-bit CRT / Flat Panel video controller (CL-GD7556) with 2 MB video memory (EDO DRAM). Software drivers are available for the most popular operating systems. These onboard video connectors are available: CRT, Flat Panel, PanelLink, TV-OUT and V-PORT. The V-PORT connector supports TEKNOR's TEK-380 Video Camera Interface Module (VIPer Vision).
- **Serial Ports:** Supports two RS-232 serial ports, with RS-422/RS-485 available on Serial Port 2. Serial ports are 16C550 compatible with internal 16-byte FIFO buffers for more efficient data transfers.
- **Parallel Port:** Supports multiple modes (Standard, EPP and ECP).
- **Universal Serial Bus (USB):** Supports two USB ports with optional cable/assembly bracket. The USB is an interface allowing for connectivity to many standard PC peripherals via an external port.
- **Basic Interface Devices:** Supports PS/2 keyboard, PS/2 mouse, AT standard keyboard, speaker, reset switch and hard disk LED.
- **In-Target Probe (ITP) Connector Footprint:** The board provides the footprint to allow the user to install an ITP connector, typically used for connection to an In-Circuit Emulator (ICE). For more detail, contact TEKNOR's Technical Support.
- **Serial ID Number Device:** The 48-bit serial number device contains the board's unique serial number. The number can be read by software. For instructions on accessing this device, contact TEKNOR's Technical Support.
- **4KB Serial EEPROM:** The 4KB serial EEPROM device is non-volatile memory. This storage area is completely user-defined. For instructions on accessing this device, contact TEKNOR's Technical Support.
- **Supervisor Utilities:** Include a two-stage Watchdog Timer supervisory circuit, a power fail / low battery detector circuit, and a CPU temperature sensor / alarm included in the processor module.
- **Battery:** A built-in lithium battery is provided for data retention of CMOS memory.
- **Voltage Regulators:** Onboard switching regulator used for 1.7V (VCORE and GTL+ termination) and for 3.3VDC (VIO) power supplies. Also linear regulators for L2 cache (1.8V) and processor module CMOS pull-up voltages (2.5V).
- **Operating Systems:** Supports all operating systems developed for x86 and Pentium processors: DOS, Windows 3.1, OS/2, Windows 95, Windows NT, UNIX, QNX, Novell 4.10, etc.
- **Boot Block Flash BIOS:** The 256KB boot block flash device contains all the board's BIOSs and it is used for storing the nonvolatile configuration required for Plug and Play. Protected boot block section allows for reprogramming of BIOS. The main BIOS is an AWARD BIOS with ACPI, APM, DMI, Green and PnP features.

3. COMPATIBILITY WITH TEKNOR SBC PRODUCTS

The PCI-941 single board computer is an upgraded version of the PCI-936 which is also a full-featured,full-sized PICMG PCI-ISA single board computer including onboard Ethernet, SCSI, video and USB interfaces. The PCI-941 is based on the Intel Mobile Pentium II processor and the Intel 82443BX chipset, while the PCI-936 is based on the Intel Pentium processor and the Intel 430 HX (Triton II) chipset.

New features include the Intel Mobile Pentium II processor in a Ball Grid Array (BGA) package, the Intel 82443BX north bridge and the PIIX4 PCI-to-ISA bridge in BGA packages, the Intel 82558 single chip PCI 10Base-T/100Base-TX Ethernet, and the Cirrus Logic GD7556 video chip in a BGA package. It is the first TEKNOR SBC with four BGA packages.



HARDWARE INSTALLATION & CONNECTIONS

4. STATIC ELECTRICITY PRECAUTIONS

Since static electricity can damage a board, the following precautions should be taken whenever you handle the PCI-941:

- Keep the board in its antistatic package, until you are ready to install it.
- Touch a grounded surface before removing the board from its package or wear a grounding wrist strap; this will discharge any static electricity that may have built up on your body.
- Handle the board by the edges.

5. UNPACKING

Follow these recommendations while unpacking:

- Observe the Static Electricity Precautions (Section 4).
- After opening the box, save it and the packing material for possible future shipment.
- Remove the board from its antistatic wrapping and place it on a grounded surface.

Inspect the board for damage. If there is any damage, or items are missing, notify TEKNOR immediately.

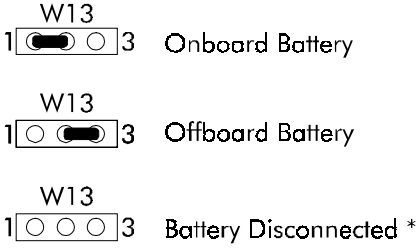
6. SETTING JUMPERS

6.1 CONNECTING THE BATTERY

To enable the onboard battery, you must short pins 1 and 2 on jumper W13. An offboard battery may be used. In such a case, pins 2 and 3 of jumper W13 should be shorted.

The jumper settings for W13 appear below (* = factory setting).

W13 Battery Selection



NOTE

Removing the W13 jumper cap has the same effect as putting the battery in storage. TEKNOR always ships its board with the battery jumper removed in order to increase the life of the battery.

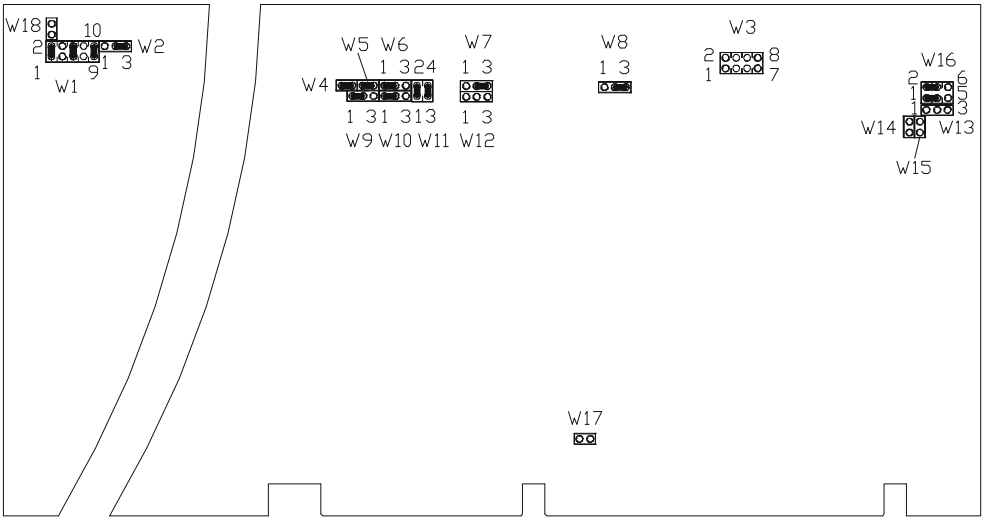
6.2 JUMPER SETTINGS ON THE PCI-941

Diagram 6-1 shows the jumper locations on the PCI-941 board. On this diagram, jumpers appear as rectangular boxes containing small circles which represent the pins. The jumpers are numbered on the diagram, as well as on the board.

The jumpers are shown with factory settings (the black strips over the pins indicate that those pins are shorted by jumper caps).

Table 6-1, Table 6-2 and Table 6-3 on the following pages show all the PCI-941 jumper settings (factory settings are indicated with an *).

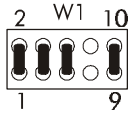
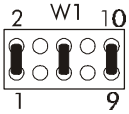
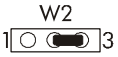
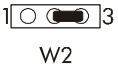
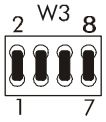
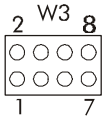
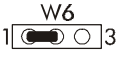
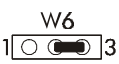
DIAGRAM 6-1: Jumper Locations With Factory Settings



WARNING

The W1 setting shown is only for 233, 266, and 300MHz CPU with 1.6V Core voltage.
INCORRECT CORE VOLTAGE SETTING CAN CAUSE DAMAGE TO THE PROCESSOR

TABLE 6-1: Jumper Settings: W1 - W6

NAME	FUNCTION	CONFIGURATION (FACTORY SETTING: *)
W1	VCORE for Specific MPII Processors	 1.7V VCore CPU  1.6V VCore CPU **WARNING: Incorrect core voltage setting can cause damage to the processor!**
W2	Active SCSI Termination	 Controlled by software  Board is terminated *  No termination
W3	User-Definable Jumpers: 1-2 Jumper 1 3-4 Jumper 2 5-6 VT100 Mode 7-8 Reserved	 1-2 Not used 3-4 Not used 5-6 VT100 Mode 7-8 Reserved  1-2 Not used * 3-4 Not used * 5-6 Standard Mode * 7-8 Reserved *
W4	CompactFlash Disk: Secondary IDE Master/Slave Selection	 Master *  Slave
W5	Enable/Disable Onboard Video Controller	 Enable onboard video controller *  Disable onboard video controller
W6	Flat Panel: Clock Polarity	 Non-inverted *  Inverted

Mobile Pentium II

INTEL S-Spec	Core Voltage
SL2KH	1.7V
SL2KJ	1.7V
SL2RS	1.6V
SL2RR	1.6V
SL2RQ	1.6V

TABLE 6-2: Jumper Settings: W7 - W12

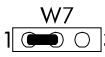
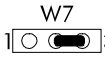
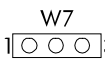
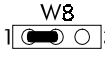
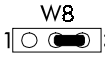
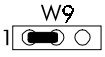
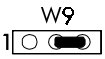
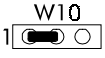
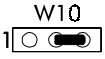
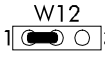
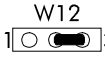
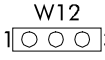
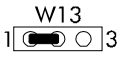
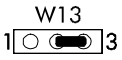
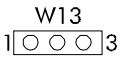
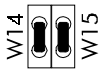
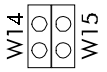
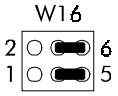
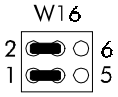
NAME	FUNCTION	CONFIGURATION (FACTORY SETTING: *)
W7	Watchdog Timer	 Dual-Stage Watchdog  Single-Stage Watchdog *  Watchdog Disabled
W8	Power Fail: Source Selection	 Offboard Battery (user defined power fail)  Onboard or offboard battery (depending on W13 jumper) when less than 3V *
W9	Flat Panel Power Voltage and Interface Level	 5V *  3.3V **NOTE: To know which level to select, refer to the Flat Panel voltage specification.**
W10	PanelLink Cable: Differential Voltage Amplitude	 750mV *  250mV
W11	Latch Select for PanelLink Interface	 1-2: Latch on falling edge of control signals * 3-4: Latch on falling edge of data signals *  1-2: Latch on rising edge of control signals 3-4: Latch on rising edge of data signals
W12	IOCHK Signal: Source Selection	 Power Fail Output  Watchdog Output (Stage 1)  Disabled *

TABLE 6-3: Jumper Settings: W13 - W18

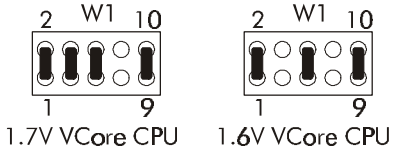
NAME	FUNCTION	CONFIGURATION (FACTORY SETTING: *)
W13	Battery Selection	 Onboard Battery  Offboard Battery  Battery Disconnected *
W14 W15	Serial Port 2 Termination Resistors	 RS-422/RS-485 with termination resistors  RS-422/RS-485 without termination resistors * **WARNING:** **Do not install these jumpers when operating in RS-232 mode.**
W16	PS/2 Connector Function	 PS/2 keyboard  PS/2 mouse * **WARNING:** **The board will not start up properly if the W16 jumper is not set up correctly.**
W17	Video Controller: PCI Interrupt B	 Disable *  Enable
W18	SCSI Mode (16-bit, 8-bit)	 16-bit: Wide-Ultra SCSI  8-bit: Fast SCSI II and Fast-20 SCSI II *

7. MPII PROCESSOR INSTALLATION INFORMATION

The Mobile Pentium II processor, the heatsink and fan assembly, and the thermal plate are factory installed. When the board is shipped from TEKNOR, the processor's VCORE voltage is set with jumper W1 for the specific processor installed on the board.

The Core Voltage value of the CPU depends on its reference (printed on a label located at the bottom of the CPU). The VCORE jumper setting appears below (* = default):

W1 VCORE for Specific MPII Processors

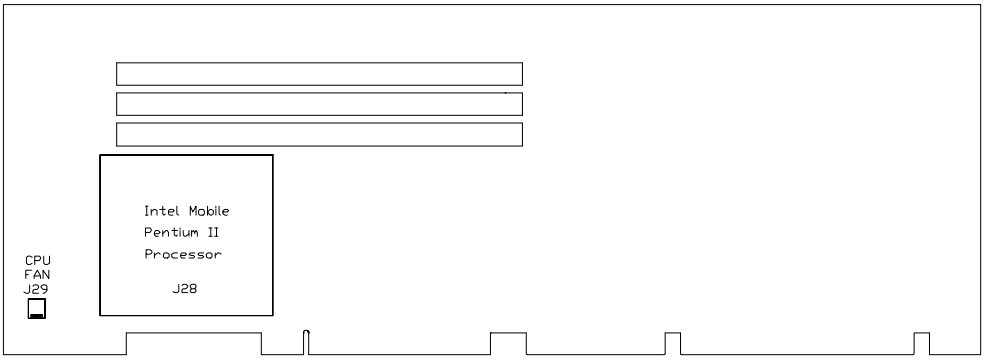


Mobile Pentium II	
INTEL S-Spec	Core Voltage
SL2KH	1.7V
SL2KJ	1.7V
SL2RS	1.6V
SL2RR	1.6V
SL2RQ	1.6V

WARNING: Incorrect core voltage setting can cause damage to the processor!

The processor is installed in the J28 connector (240-pin BGA connector). The processor's cooling fan is installed in the J29 connector (male 2-pin lock header). The location of the processor module connector and the fan connector appear in Diagram 7-1 below.

DIAGRAM 7-1: Location of Processor Module and Fan Connectors



The connector pinout for J29 fan connector appears in Table 7-1.

TABLE 7-1: Fan Connector (J29) - Pinout

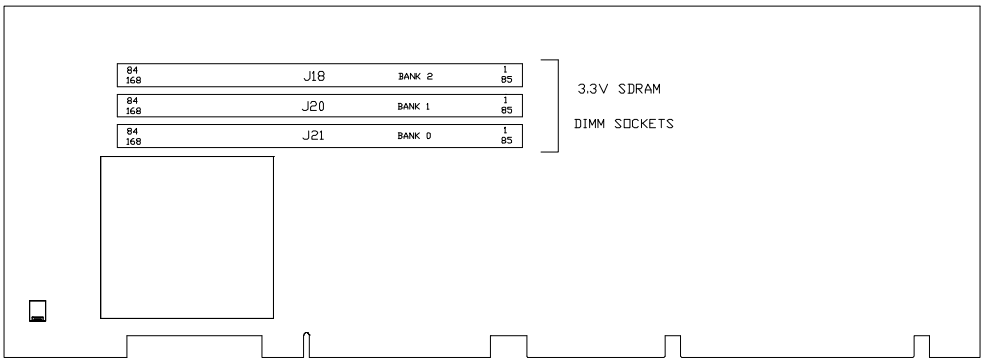
Pin Number	Signal
1	+5V
2	GND

8. INSTALLING SYSTEM MEMORY

8.1 168-PIN SOCKETS LOCATION

The location of the three 168-pin vertical DIMM (Dual In-line Memory Module) sockets appears on Diagram 8-1 and they are labeled Bank 0, Bank 1 and Bank 2.

DIAGRAM 8-1: DIMM Sockets Location



8.2 SUPPORTED SYSTEM MEMORY CONFIGURATIONS

The DRAM interface is a 64/72-bit path that supports up to 384MB of Synchronous DRAM (SDRAM) or 768MB of Registered SDRAM (RSDRAM). Memory can be installed in one, two or three DIMM sockets.
The following SDRAM modules are supported: 8MB (1Mx64/72), 16MB (2Mx64/72), 32MB (4Mx64/72), 64MB (8Mx64/72), 128MB (16Mx64/72) and 256MB (32Mx64/72).

Memory modules must conform to the following:

- 3.3V only, single-sided or double-sided.
- Registered/Unregistered 66MHz modules.
- Serial Presence Detect (SPD) EEPROM.
- 64-bit and 72-bit DIMMs.
- Error Checking and Correction (ECC) or parity bit, with 72-bit DIMMs.
- Compliant with Intel's PC SDRAM Unbuffered DIMM Specification (66MHz), Revision 1.0.

8.3 DIMM INSTALLATION

When you are ready to install the DIMMs in the sockets, follow the steps outlined below:

1. With the board flat on the table, turn it so that the sockets are at the end of the board farthest from you.
2. Hold the module vertically and turn it so that one of the two bottom connector keys is on the right. Insert the connector into the socket (Bank 0, Bank 1 or Bank 2, depending on the configuration chosen - see Table 8-1), aligning the keys on the module with the socket's key inserts.
3. Snap the retaining clips on each side of the socket to a vertical position to lock the module into place. Repeat steps 2 and 3 if you are populating other sockets.

To remove a DIMM from a socket, push down the retaining clips situated on each side of the socket, to release the module. Pull the module upward to remove.

DIMM modules can be installed in any socket and order. The total system memory is equal to the sum of the memory module size installed in the three DIMM sockets.

When populating more than one memory module, each socket must be installed with the same memory type (64 or 72 bits), however the capacity of each module can be different from the other.

Eexamples of recommended DIMM devices are listed below. Many other models are available and function equally well. Users are encouraged to check with their local distributors for comparable substitutes.

TABLE 8-1: Recommended DIMM Devices

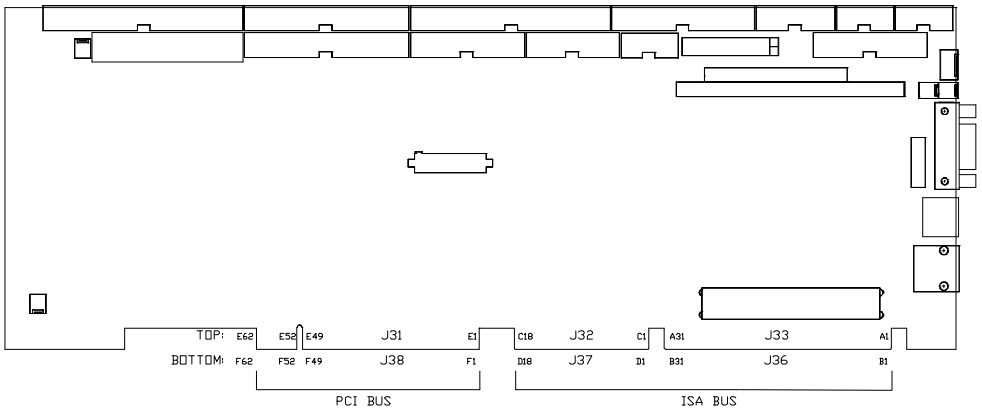
DIMM	VENDOR	PART NUMBER
2M*72 (SDRAM) 16MB module	CENTON	CFDKG1TTNVU367G
4M*72 (SDRAM) 32MB module	ROCKY MOUNTAIN RAM	4x72CQ2x8S4E
	CENTON	CFEKG1TTNVU367G
8M*72 (SDRAM) 64MB module	CENTON	CKFKJ1TT4VU346G
16M*72 (SDRAM) 128MB module	CENTON	CKGKJ1TT4VU371G
	ROCKY MOUNTAIN RAM	16x72CQ8x8S4E

9. INSTALLING PCI-941 BOARD IN A SYSTEM

The PCI-941 has a PCI bus connector and an ISA bus connector so it can be installed in a standard ISA or PCI-ISA backplane.

Diagram 9-1 displays the location of the PCI bus and the ISA bus on the PCI-941 board.

DIAGRAM 9-1: PCI Bus and ISA Bus



9.1 BACKPLANE INSTALLATION

The PCI-941 will work on any PCI-ISA backplane, provided it complies with the PCI INDUSTRIAL COMPUTER MANUFACTURERS GROUP (PICMG), Revision 2.0 specification. The available PCI and ISA slots on the backplane provide the possibility of expansion through PCI and ISA add-on cards.

Since the PCI-941 is also fully IBM AT compatible, it can also be installed on any standard ISA passive backplane, if PCI expansion slots are not needed.

Expansion is also provided through the board's PC/104 connector for ISA modules or through the PC/104-Plus for PCI modules. A number of PC/104 and PC/104-Plus modules can be installed on the PCI-941 since these modules are stackable mezzanine cards.

The pinout for the PCI bus appears in Appendix C – *Connector Location & Pinouts.*

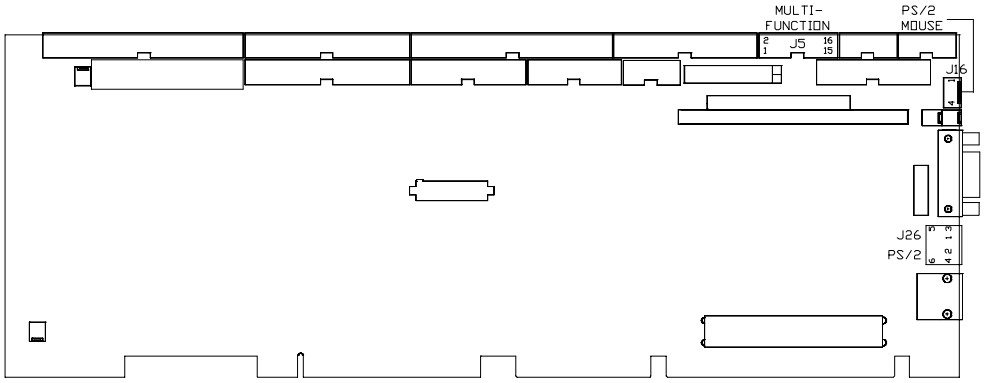
10. INSTALLING & CONNECTING I/O DEVICES (KEYBOARD, SPEAKER, RESET, HD LED, MOUSE)

The J5, J16 and J26 connectors connections on the PCI-941 board are used for the following I/O connections:

- The J5 multi-function header allows connections for the standard AT keyboard, speaker port, suspend button, reset button and hard disk LED.
- The J16 PS/2 mouse header allows connection for a PS/2 mouse.
- The J26 PS/2 connector allows connection for a PS/2 mouse or a PS/2 keyboard depending on the W16 jumper setting (see section 10.1 below).

The location of the J5, J16 and J26 connectors appears below in Diagram 10-1.

DIAGRAM 10-1: J5, J16 & J26 Connector Location



10.1 W16 JUMPER SETTINGS FOR SELECTING PS/2 CONNECTOR FUNCTION: KEYBOARD OR MOUSE

The W16 jumper is used for selecting the J26 PS/2 connector function, keyboard or mouse, as shown below (* = factory setting):

W16	PS/2 Connector Function
W16 2 ○ ▬ 6 1 ○ ▬ 5	PS/2 keyboard
W16 2 ▬ ○ 6 1 ▬ ○ 5	PS/2 mouse *

WARNING:
The board will not start up properly if the W16 jumper is not correctly set.

10.2 J5, J16 & J26 CONNECTIONS

10.2.1 J5 MULTI-FUNCTION CONNECTIONS

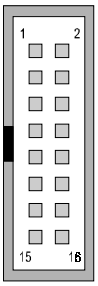
The AT keyboard, speaker, suspend button, reset button and HD LED functions are grouped together on the J5 multi-function connector. The cable used for connecting these devices is the 22" keyboard cable (TEKNOR part number 150-018-01).

Though TEKNOR supplies a cable for the J5 connector as mentioned above, you can build your own. The following are recommended for the mating connector:

Amp 746285-3 [optional strain relief: 499252-8],
Robinson Nugent IDS-C16PK-TG,
Thomas & Betts 622-1630 [optional strain relief: 622-1641].
(16-pin flat cable connector).

All functions on the J5 connector are conveniently summarized in the following diagram showing the J5 connector and a table of the keyboard cable's 16 pins and their connections. More detailled explanation follows on the next page.

DIAGRAM 10-2: J5 Multi-Function Connector & Flat Ribbon Cable Connections



Pin	Signal Name	Description
1	KBCLK	Standard AT Keyboard: Use the keyboard DIN connector on TEKNOR's keyboard cable (part # 150-018-01).
2	GND	
3	KBDATA	
4	GND	
5	VCC (+5V)	
6	VCC (+5V)	
7	SPEAKER	Speaker: Use an 8 ohm speaker.
8	VCC (+5V)	
9	Not Connected	Not Used.
10	GND	
11	PWRBT*	Suspend Button: Short to toggle between Suspend and Normal Modes.
12	GND	
13	PBRES*	Push Button Reset: Short to reset the computer board.
14	GND	
15	ACTIVE*	Hard Disk Activity LED: No external limiting resistor is required.
16	VCC (+5V)	

* Active low signal

The following functions are available on the J5 connector:

Keyboard Pins 1 to 6 are already connected to the 150-018-01 keyboard cable's DIN connector.

Speaker: An 8 ohm speaker can be directly connected to pins 7 and 8. All necessary drivers are on the board.

Suspend Button: You can connect pins 11 and 12 to an external push button switch. Shorting pins 11 and 12 by pressing the push button is a convenient way of placing your system in Suspend Mode, or of returning to Normal Mode when in Suspend Mode. The J19 connector has the same function (see Section 17).

Push Button Reset: You can connect pins 13 and 14 to an external push button switch. Shorting pins 13 and 14 by pressing the push button is a convenient way of performing a hardware reset on the board.

Hard Disk LED: The onboard IDE interface can activate an external LED. The LED must be connected anode on pin 16 and cathode on pin 15. No external current limiting resistor is required since a 330 ohm resistor is already present on the board.

The pinout for the J5 connector appears in Table 10-1 below.

TABLE 10-1: Multi-Function Header (J5) - Pinout

Function	Pin Number				Pin Number		
	Signal Flow					Signal Flow	
	Signal						Signal
AT Keyboard	KBCLK	I/O	1		2	-	GND
	KDATA	I/O	3		4	-	GND
	VCC (+5V)	-	5		6	-	VCC (+5V)
8 Ohm Speaker	SPEAKER	O	7		8	-	VCC (+5V)
	Not Used	-	9		10	-	GND
Suspend Button	PWRBT*	I	11		12	-	GND
Push Button Reset	PBRES*	I	13		14	-	GND
Hard Disk LED	ACTIVE*	O	15		16	-	VCC(+5V)

* Active low signal

10.2.2 J16 PS/2 MOUSE CONNECTION

If you use the PS/2 mouse header, a shielded PS/2 mouse cable is needed. It is available from TEKNOR: part number 150-337-00.

You may want to create your own cable for the mouse header. The following are recommended for the mating connector:

Molex 22-01-3047 (connector),
Molex 20-50-0114 (crimp).

The pinout for the J16 PS/2 mouse header appears below in Table 10-2.

TABLE 10-2: Mouse Header (J16) - Pinout

Pin Number	Signal Flow	Signal
1	I/O	MCLK
2	-	GND
3	I/O	MDATA
4	-	VCC (+5V)

10.2.3 J26 PS/2 CONNECTIONS

The PCI-941's I/O bracket includes a standard PS/2 mini DIN connector for connecting a PS/2 keyboard or mouse (depending on W16 jumper setting). No additional cabling is required. The pinout for the J26 connector appears below in Table 10-3.

TABLE 10-3: PS/2 Connector (J26) - Pinout

Pin Number	Signal Flow	Signal
1	I/O	KDATA when W16 jumper pins 3-5 and 4-6 are shorted, or MDATA when W16 jumper pins 1-3 and 2-4 are shorted.
2	-	Not Connected
3	-	GND
4	-	VCC (+5V)
5	I/O	KBCLK when W16 jumper pins 3-5 and 4-6 are shorted, or MCLK when W16 jumper pins 1-3 and 2-4 are shorted.
6	-	GND

CAUTION

If J26 is jumper configured as a PS/2 mouse (W16:1-3, 2-4 shorted):

- Do not connect a PS/2 keyboard cable on the J26 connector.
- Do not connect two PS/2 mice simultaneously, one on the J16 mouse connector and the other on the J26 connector. Only one PS/2 mouse connector should be used.

If J26 is jumper configured as a PS/2 keyboard (W16: 3-5, 4-6 shorted):

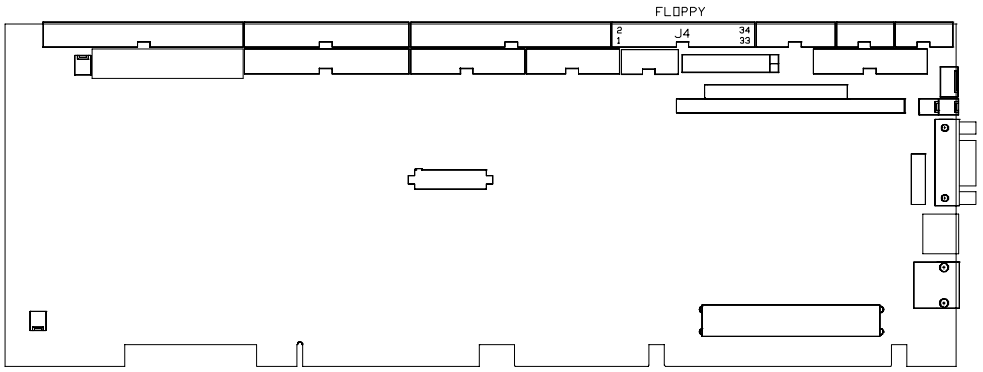
- Do not connect a PS/2 mouse cable on the J26 connector.
- Do connect two keyboards simultaneously, one on the J5 multi-function connector (AT keyboard) and the other on the J26 connector (PS/2 keyboard).

11. INSTALLING & CONNECTING STORAGE DEVICES (FLOPPY, IDE, SCSI)

11.1 J4 FLOPPY CONNECTION

The J4 floppy drive connector is a 34-pin dual row header. Its location appears below in Diagram 11-1.

DIAGRAM 11-1: J4 Floppy Drive Connector Location



NOTE

When all the hardware connections are completed on the PCI-941, you will need to setup onboard controllers and installed devices by software. For the floppy controller and devices, software setup includes:

1. Ensuring that the onboard floppy controller is enabled in the AWARD Integrated Peripheral Setup. By default, the onboard floppy is automatically enabled by the BIOS.
2. Other AWARD setup for the floppy drives includes defining the floppy type in the Standard CMOS Setup and other floppy options in the BIOS Features Setup.

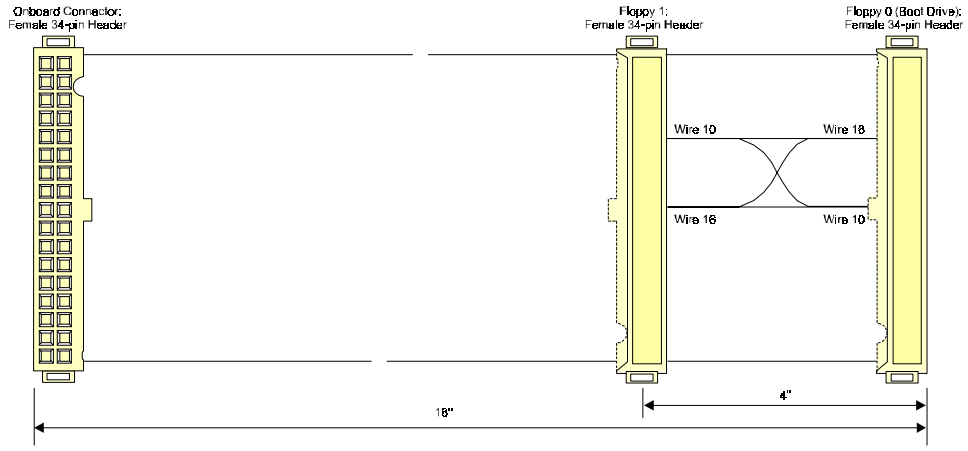
11.1.1 J4 FLOPPY CABLE CONNECTION

The installation of the floppy drives is done via a standard IBM 34-pin flat ribbon cable. This cable allows the installation of two floppy devices on the J4 header.

An 18" floppy disk cable is available from TEKNOR: part number 150-051.

Diagram 11-2 shows a floppy disk cable with the floppy 1 and floppy 0 mating connectors. Note that wire 10 to wire 16 are twisted between the floppy 1 and floppy 0 connectors.

DIAGRAM 11-2: Floppy Disk Cable



You may want to create your own cable for the J4 floppy header. The following are recommended for the mating connectors:

Amp 746285-8 [optional strain relief: 499252-6],
Robinson Nugent IDS-C34PK-TG,
Thomas & Betts 622-3430 [optional strain relief: 622-3441].
(34-pin flat cable connector).

The pinout for the J4 floppy connector appears below in Table 11-1.

TABLE 11-1: Floppy Drive Connector (J4) - Pinout

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	-	GND	2	O	DRV DENS. SEL. 0*
3	-	GND	4	-	Not Connected
5	-	GND	6	-	Not Connected
7	-	GND	8	I	INDEX*
9	-	GND	10	O	MOTOR ON 0,1*
11	-	GND	12	O	DRIVE SELECT B*
13	-	GND	14	O	DRIVE SELECT A*
15	-	GND	16	O	MOTOR ON 2*
17	-	Not Connected	18	O	DIR CONTROL*
19	-	GND	20	O	STEP*
21	-	GND	22	O	WRITE DATA*
23	-	GND	24	O	WRITE ENABLE*
25	-	GND	26	I	TRACK 0*
27	-	Not Connected	28	I	WRITE PROTECT*
29	-	FLOPPY DETECT	30	I	READ DATA*
31	-	GND	32	O	HEAD SELECT*
33	-	Not Connected	34	I	DSKCHG*

* Active low signal

11.2 IDE CONNECTIONS: J2/J10 HARD DISK & J22 COMPACTFLASH DISK

Three connectors on the PCI-941 are dedicated to IDE devices: J2 Primary IDE hard disk, J10 Secondary IDE hard disk, and J22 for the CompactFlash disk.

A total of four IDE devices can be connected to the PCI-941 IDE connectors. If your system comes with a CompactFlash disk, it counts as one IDE device, leaving the possibility of installing three IDE hard disks: two on the Primary IDE connector and one on the Secondary IDE connector, since the CompactFlash disk is connected to the secondary IDE interface.

NOTE

With the CompactFlash disk option, the J10 secondary IDE connector only supports one hard disk, since the CompactFlash disk is connected to the secondary IDE interface. The W4 jumper is used to configure your CompactFlash disk as a secondary master or slave disk.

NOTE

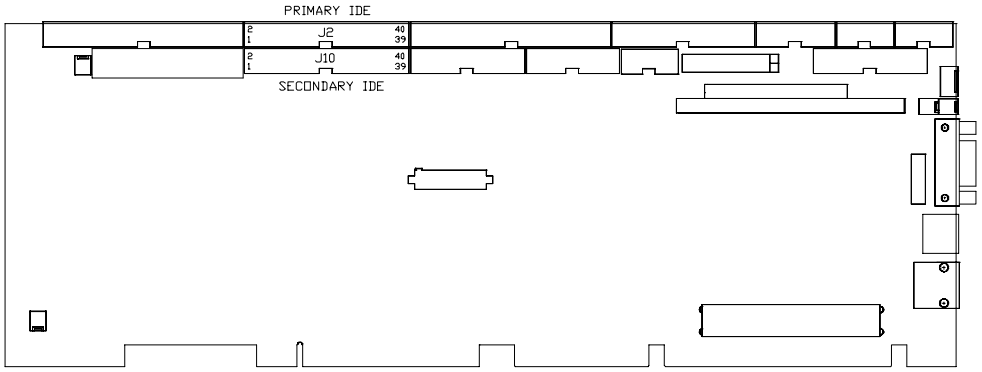
When all the hardware connections are completed on the PCI-941, you will need to setup the installed devices by software. The software setup for IDE devices includes:

1. Configuring the disks with the AWARD Standard CMOS Setup or by performing a hard disk auto-detect from the AWARD Main Menu, and setting IDE options in the AWARD Integrated Peripheral Setup. The AWARD Setup treats the CompactFlash disk as an IDE hard disk, and must therefore be configured in exactly the same way.
2. Since the CompactFlash disk's data is accessed like it would on an IDE drive, no specific CompactFlash disk driver is required for various operating systems.

11.2.1 J2/J10 IDE HARD DISK CABLE CONNECTIONS

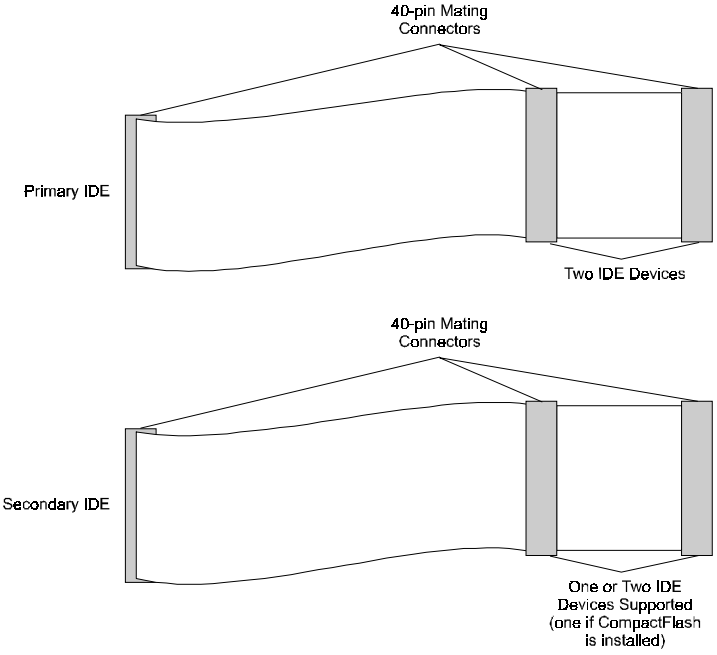
The J2 primary IDE hard drive connector and the J10 secondary IDE hard drive connector are both 40-pin dual row headers. The location of the J2 and J10 connectors appears below in Diagram 11-3.

DIAGRAM 11-3: Location of J2 & J10 IDE Hard Disk Connectors



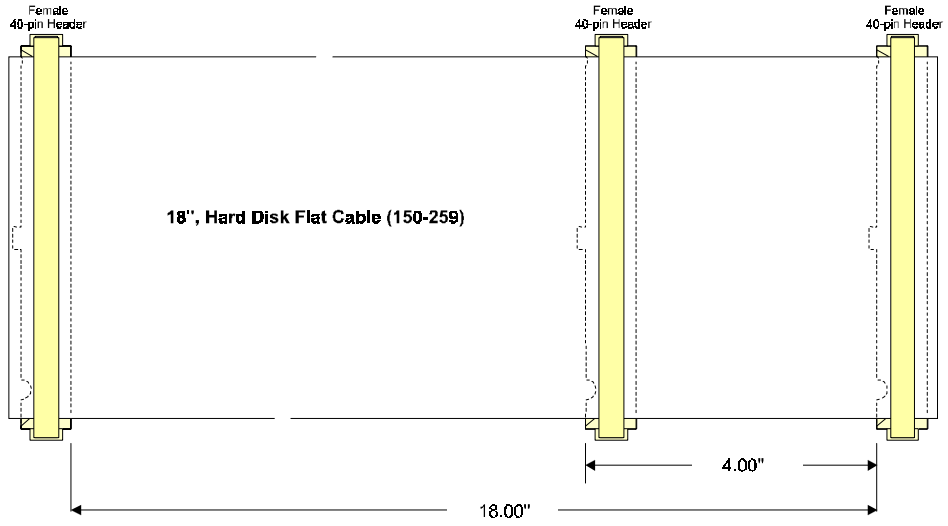
The J2 and J10 connectors allow up to four enhanced IDE devices (three if the CompactFlash disk is installed) with flat ribbon cables and mating connectors, as shown below.

DIAGRAM 11-4: IDE Hard Disk Connectors and Devices



The cables needed to hook up the J2 and J10 connectors are 40-pin flat ribbon cable (shown in Diagram 11-4 and Diagram 11-5). This 40-pin cable handles all command, data and status I/O lines. Its recommended maximum length is 18 inches from the IDE device to the 40-pin connector. The cable is available from TEKNOR: part number 150-259.

DIAGRAM 11-5: IDE Hard Disk Cable



You may want to make your own cable with a 40-pin flat ribbon cable and 40-pin flat cable mating connectors. Following is a list of approved vendors for the mating connectors:

AMP 746285-9 [optional strain relief: 499252-1],
Robinson Nugent IDS-C40PK-TG,
Thomas & Betts 622-4030 [optional strain relief: 622-4041].
(40-pin flat cable connector).

The pinouts for the J2 primary and J10 secondary IDE connectors appear in Table 11-2 and 11-3.

TABLE 11-2: Primary Enhanced IDE Connector (J2) - Pinout

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	RESET*	2	-	GND
3	I/O	DATA 7	4	I/O	DATA 8
5	I/O	DATA 6	6	I/O	DATA 9
7	I/O	DATA 5	8	I/O	DATA 10
9	I/O	DATA 4	10	I/O	DATA 11
11	I/O	DATA 3	12	I/O	DATA 12
13	I/O	DATA 2	14	I/O	DATA 13
15	I/O	DATA 1	16	I/O	DATA 14
17	I/O	DATA 0	18	I/O	DATA 15
19	-	GND	20	-	Not Connected
21	I	DRQ 0	22	-	GND
23	O	IOW*	24	-	GND
25	O	IOR*	26	-	GND
27	I	IORDY	28	O	PRIM. PDI[1]
29	O	DACK 0*	30	-	GND
31	I	IRQ 14	32	-	Not Connected
33	O	ADD 1	34	-	Not Connected
35	O	ADD 0	36	O	ADD 2
37	O	CS 1P*	38	O	CS 3P*
39	I	IDEACTP*	40	-	GND

TABLE 11-3: Secondary Enhanced IDE Connector (J10) - Pinout

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	RESET*	2	-	GND
3	I/O	DATA 7	4	I/O	DATA 8
5	I/O	DATA 6	6	I/O	DATA 9
7	I/O	DATA 5	8	I/O	DATA 10
9	I/O	DATA 4	10	I/O	DATA 11
11	I/O	DATA 3	12	I/O	DATA 12
13	I/O	DATA 2	14	I/O	DATA 13
15	I/O	DATA 1	16	I/O	DATA 14
17	I/O	DATA 0	18	I/O	DATA 15
19	-	GND	20	-	Not Connected
21	I	DRQ 1	22	-	GND
23	O	IOW*	24	-	GND
25	O	IOR*	26	-	GND
27	I	IORDY	28	O	SEC. PDI[1]
29	O	DACK 1*	30	-	GND
31	I	IRQ15	32	-	Not Connected
33	O	ADD 1	34	I/O	SDIAG*
35	O	ADD 0	36	O	ADD 2
37	O	CS 1S*	38	O	CS 3S*
39	I	IDEACTS*	40	-	GND

* Active low signal
[1] 470 ohm pull-down

11.2.2 J22 COMPACTFLASH INSTALLATION & CONNECTIONS

11.2.2.1 CompactFlash Disk Jumper

The W4 configuration jumper allows you to select if the CompactFlash disk is a secondary master or secondary slave IDE disk. Settings are shown below (* = factory setting):

W4 CompactFlash Disk: Secondary IDE Master/Slave Selection

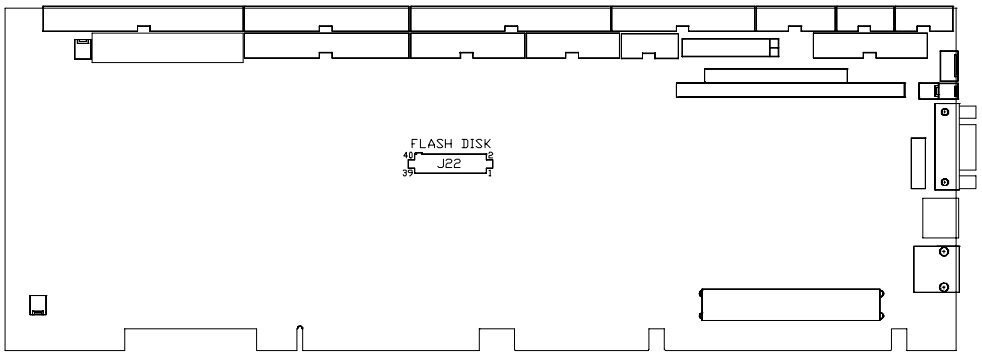
Master *

Slave

11.2.2.2 CompactFlash Disk Installation on TEK-069 Daughterboard & J22 Connection

The CompactFlash Disk's IDE connector is located at J22 as shown below in Diagram 11-6.

DIAGRAM 11-6: CompactFlash Disk IDE Connector (J22) Location

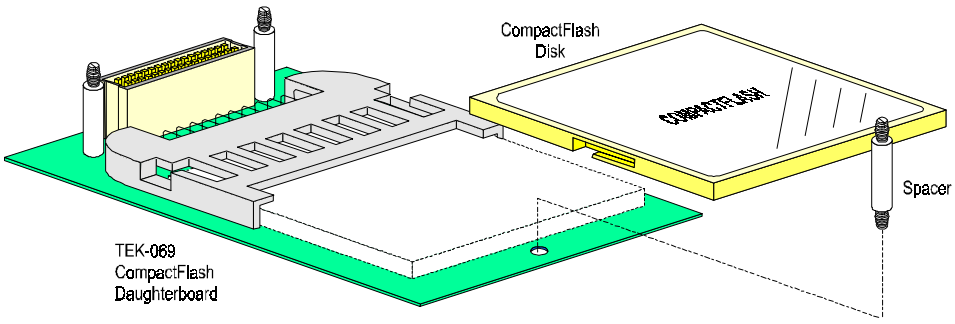


Installing a Compact Flash disk on the PCI-941 requires the TEK-069 daughterboard that connects to the PCI-941 board's J22 CompactFlash connector.

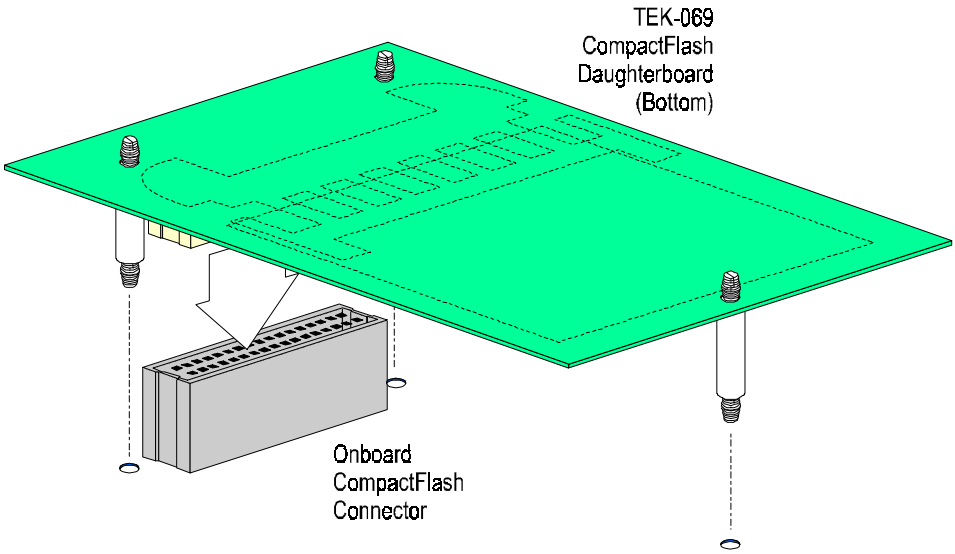
If the TEK-069 daughterboard is already installed on your PCI-941 board, you must first remove it prior to installing or replacing a CompactFlash disk on the daughterboard.

Follow this procedure to install a CompactFlash disk on the TEK-069 and to install the TEK-069 on the PCI-941:

1. Slide the Compact Flash disk into its receptacle and press gently to ensure a good insertion and connection.



2. Clip the spacers into their mounting holes: two are located close to the interface connector, and a third one is located near the flash disk. The spacer located near the flash disk acts as a retension mechanism to the flash disk and prevents it from accidently sliding out.
3. To connect the daughterboard to the PCI-941, simply line up the J22 connector and the interface connector, then press the daughterboard firmly into the Single Board Computer's connector to engage the connector and the spacers.



The pinout for the CompactFlash connector appears in Table 11-4.

TABLE 11-4: CompactFlash IDE Connector (J22) - Pinout

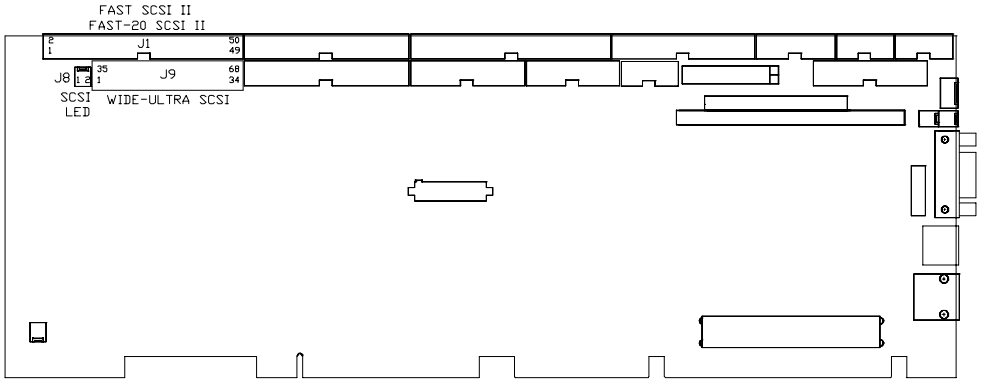
Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	I/O	DD11	2	-	GND
3	I/O	DD12	4	I/O	DD3
5	I/O	DD13	6	I/O	DD4
7	I/O	DD14	8	I/O	DD5
9	I/O	DD15	10	I/O	DD6
11	O	CS3*	12	I/O	DD7
13	-	Not Connected	14	O	CS1*
15	-	Not Connected	16	O	IOR*
17	I/O	SDIAG*	18	O	IOW*
19	I	IRQ15	20	-	VCC (+5V)
21	-	VCC (+5V)	22	-	VCC (+5V)
23	-	GND	24	-	GND
25	O	RESET*	26	-	GND
27	O	W4 Jumper Select	28	O	DA2
29	O	DA1	30	I	ACTIVE*
31	O	DA0	32	-	Not Connected
33	I/O	DD0	34	I/O	DD8
35	I/O	DD1	36	I/O	DD9
37	I/O	DD2	38	I/O	DD10
39	-	Not Connected	40	-	GND

* Active low signal

11.3 J1, J8 & J9 SCSI CONNECTIONS

The J1 Fast SCSI II connector is a 50-pin header. The J9 PCI Wide-Ultra SCSI Interface connector is a 68-pin high density SCSI connector. The J8 SCSI LED connector is a 2-pin lock header. The location of the J1, J8 and J9 connectors appears below on Diagram 11-7.

DIAGRAM 11-7: Location of the J1, J8 & J9 SCSI Connectors



NOTE

When all the hardware connections are completed on the PCI-941, you will need to setup onboard controllers and installed devices by software. For the SCSI controller and devices, software setup includes:

1. Ensuring that the onboard SCSI controller is enabled in the AWARD Integrated Peripherals Setup. By default, the onboard SCSI is enabled, however, it may be disabled if an external SCSI card is required for testing or other purposes.
2. If you want your SCSI device to be the boot device, this must be defined in the AWARD BIOS Features Setup.
3. The Adaptec SCSISelect Configuration Utility allows you to configure or view the default configuration settings for the SCSI host adapter (more detail in Section 20).
4. The EZ-SCSI software allows you to install the appropriate driver for your specific operating system (more detail in Section 21).

11.3.1 SCSI JUMPERS

Make sure the SCSI jumpers are properly configured.

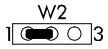
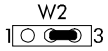
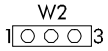
The W18 jumper determines whether the SCSI mode is 16-bit (Wide-Ultra) or 8-bit (Fast SCSI II / Fast-20 SCSI II). The settings for the W18 jumper are (* = factory setting):

W18	SCSI Mode (16-bit, 8-bit)	W18 	16-bit: Wide-Ultra SCSI
		W18 	8-bit: Fast SCSI II and Fast-20 SCSI II *

NOTE

You must configure the PCI-941 board for either the 16-bit or 8-bit mode, depending on the SCSI device(s) to install on the board. 16-bit devices connect to the 68-pin J9 PCI Wide-Ultra SCSI Interface connector; 8-bit devices connect to the 50-pin J1 SCSI header (a flat ribbon cable is needed).

The W2 jumper determines whether the PCI-941 board is terminated. The settings are (* = factory setting):

W2	Active SCSI Termination	W2 	Controlled by software
		W2 	Board is terminated *
		W2 	No termination

NOTE

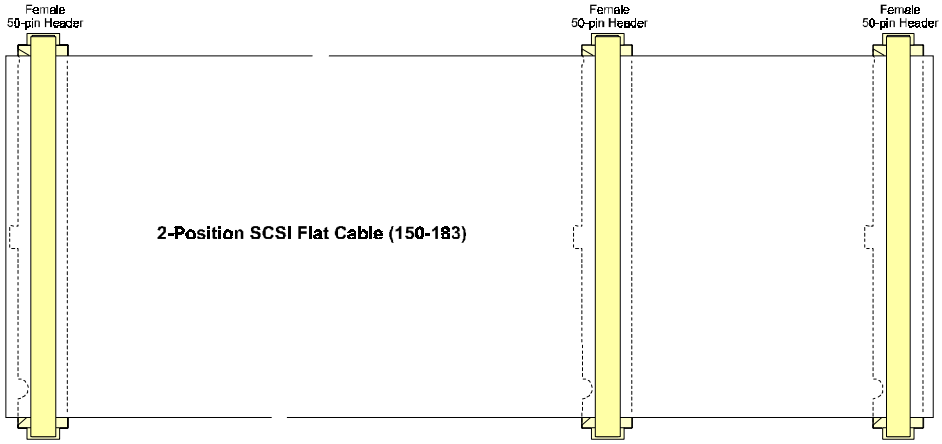
Make sure that both ends of the SCSI cable are terminated and that all devices in between the ends are not terminated. If the PCI-941 board is located at the end of the SCSI cable, it should be terminated by properly configuring the W2 jumper.

11.3.2 J1, J8 & J9 SCSI CABLE CONNECTIONS

11.3.2.1 J1 SCSI Header (50-Pin)

The cable needed to connect your Fast SCSI II device(s) to the PCI-941's J1 connector is a 50-pin flat ribbon cable, like the one shown on Diagram 11-8. The cable is available from TEKNOR: part number 150-183.

DIAGRAM 11-8: Fast SCSI II Device Cable



You may want to make your own cable with a 50-pin flat ribbon cable and 50-pin flat cable mating connectors. Following is a list of approved vendors for the mating connectors:

AMP 1-746285-0 [optional strain relief: 499252-4],
Robinson Nugent IDS-C50PK-TG,
Thomas & Betts 622-5030 [optional strain relief: 622-5041].
(50-pin flat cable connector).

WARNING

Connect the Fast SCSI II cable and the Flat Panel cable to the PCI-941 board carefully, since both the J1 SCSI connector and the J3 Flat Panel connector are 50-pin headers.

Faulty cable connections will damage the board!

The pinout for the J1 SCSI header appears below in Table 11-5.

TABLE 11-5: Fast SCSI Interface Connector (J1) - Pinout

Pin Number	Signal	Pin Number	Signal
1	GND	2	SD0*
3	GND	4	SD1*
5	GND	6	SD2*
7	GND	8	SD3*
9	GND	10	SD4*
11	GND	12	SD5*
13	GND	14	SD6*
15	GND	16	SD7*
17	GND	18	SDP*
19	GND	20	GND
21	GND	22	GND
23	Not Connected	24	GND
25	Not Connected	26	Term Power
27	Not Connected	28	GND
29	GND	30	GND
31	GND	32	SATN*
33	GND	34	GND
35	GND	36	SBSY*
37	GND	38	SACK*
39	GND	40	SRST*
41	GND	42	SMSG*
43	GND	44	SSEL*
45	GND	46	SCD*
47	GND	48	SREQ*
49	GND	50	SIO*

* Active low signal

11.3.2.2 J8 SCSI LED (2-Pin)

The onboard SCSI interface can activate an external LED. This LED must be connected to the J8 SCSI LED connector as follows: anode on pin 1 and cathode on pin 2. No external current limiting resistor is required since a 330 ohm resistor is already present on the board.

The cable needed to connect your SCSI LED to the PCI-941's J8 connector is a 2-wire cable. Following is a list of approved vendors for the mating connector:

Leoco 2530 S020013 (housing),
Leoco 2533 TCB00A0 (crimp).

Molex 22-01-3027 (housing),
Molex 08-50-0114 (crimp).

The pinout for the SCSI LED connector appears below in Table 11-6.

TABLE 11-6: SCSI LED Connector (J8) - Pinout

Pin Number	Signal Flow	Signal
1	-	VCC (+5V)
2	O	SCLED*

* Active low signal

11.3.2.3 J9 High Density SCSI Connector (68-Pin)

Connect your Wide-Ultra SCSI device cable directly to the 68-pin J9 high density SCSI connector.

The pinout of the J9 SCSI connector appears below in Table 11-7.

TABLE 11-7: PCI Wide-Ultra SCSI Interface Connector (J9) - Pinout

Pin Number	Signal	Pin Number	Signal
1	GND	35	SD12*
2	GND	36	SD13*
3	GND	37	SD14*
4	GND	38	SD15*
5	GND	39	SDPH*
6	GND	40	SD0*
7	GND	41	SD1*
8	GND	42	SD2*
9	GND	43	SD3*
10	GND	44	SD4*
11	GND	45	SD5*
12	GND	46	SD6*
13	GND	47	SD7*
14	GND	48	SDP*
15	GND	49	GND
16	GND	50	GND
17	Term Power	51	Term Power
18	Term Power	52	Term Power
19	Not Connected	53	Not Connected
20	GND	54	GND
21	GND	55	SATN*
22	GND	56	GND
23	GND	57	SBSY*
24	GND	58	SACK*
25	GND	59	SRST*
26	GND	60	SMSG*
27	GND	61	SSEL*
28	GND	62	SCD*
29	GND	63	SREQ*
30	GND	64	SIO*
31	GND	65	SD8*
32	GND	66	SD9*
33	GND	67	SD10*
34	GND	68	SD11*

* Active low signal

12. INSTALLING & CONNECTING VIDEO

This Section covers video connections found on the PCI-941: video controller jumpers (section 12.1), CRT display (12.2), Flat Panel display (12.3), PanelLink (12.4), V-PORT (12.5) and TV-OUT (12.6).

NOTE

When all the hardware connections are completed on the PCI-941, you will need to setup onboard controllers and installed devices by software. For the video controller and display, software setup includes the following:

1. There are two video options on the AWARD Standard CMOS Setup screen: Video (for video controller) and CRT&LCD (for displays).
2. The video controller has specific video drivers for various operating systems and software. To install these drivers, you must use the Utility Disk containing the video drivers for your operating system (more detail in Section 21).
3. BIOS updates for specific Flat Panel devices are available from TEKNOR. They need to be copied to the Flash BIOS using the UBIOS utility (Section 22).

12.1 VIDEO CONTROLLER JUMPERS

12.1.1 ENABLE / DISABLE VIDEO CONTROLLER JUMPER

The W5 configuration jumper allows you to select if the onboard video controller is enabled or disabled. Settings are shown below (* = factory setting):

W5	Enable/Disable Onboard Video Controller	W5 	Enable onboard video controller *
		W5 	Disable onboard video controller

NOTE

Ensure that the onboard video controller is enabled with the W5 jumper installed. By default, the onboard video is enabled, however, it may be disabled by removing the W5 jumper, if an external video card is required for testing or other purposes.

12.1.2 ENABLE / DISABLE PCI INTERRUPT FOR THE VIDEO CONTROLLER

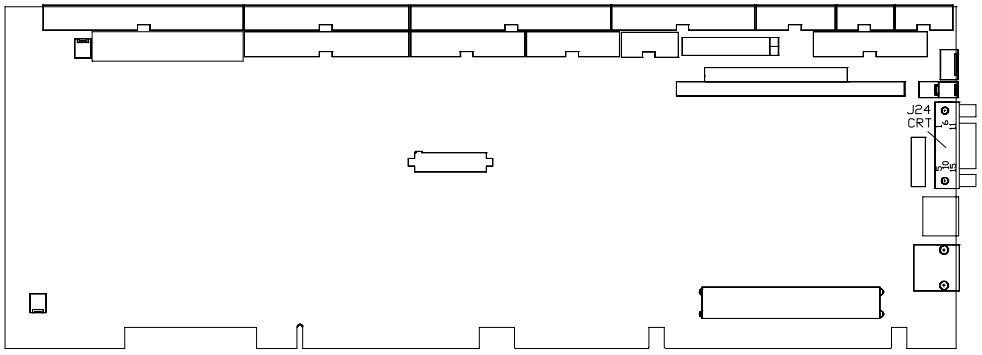
The W17 configuration jumper allows you to select if the video controller will generate an interrupt request signal to indicate that the controller has reached the end of an active field (VSYNC pulse to the CRT monitor). The interrupt is connected to the PCI interrupt B line, and is enabled by removing the W17 jumper. By default the interrupt is disabled. Settings are shown below (* = factory setting):

W17	Video Controller: PCI Interrupt B	W17 	Disable *
		W17 	Enable

12.2 J24 CRT CONNECTION

The J24 CRT connector is a standard 15-pin high density, right angle VGA connector. Its location is on the I/O bracket. It appears below on Diagram 12-1.

DIAGRAM 12-1: CRT Connector Location



Connecting a CRT video display to the PCI-941 is simple. Merely connect the display cable's standard VGA DB15 male connector to the PCI-941's J24 female connector.

The pinout for the J24 CRT connector appears in Table 12-1.

TABLE 12-1: CRT VGA Interface Connector (J24) - Pinout

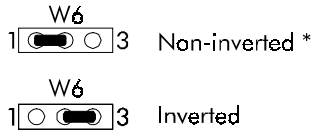
Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	RED	6	-	ANALOG GND	11	-	Not Connected
2	O	GREEN	7	-	ANALOG GND	12	O	I2CDATA
3	O	BLUE	8	-	ANALOG GND	13	O	RHSYNC
4	-	Not Connected	9	-	Not Connected	14	O	RVSYNC
5	-	GND	10	-	GND	15	O	I2CCLK

12.3 J3 & J11 FLAT PANEL CONNECTIONS

12.3.1 FLAT PANEL JUMPERS

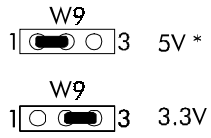
The W6 configuration jumper allows you to select the polarity for the Flat Panel clock signal. Settings are shown below (* = factory setting):

W6 Flat Panel: Clock Polarity



The W9 configuration jumper allows you to select the power voltage and interface level for the flat panel. The PCI-941 supplies the flat panel with sequenced 5 volts or 3.3 volts. Settings are shown below (* = factory setting):

W9 Flat Panel Power Voltage and Interface Level



NOTE: To know which level to select, refer to the Flat Panel voltage specification.

WARNING

Make sure you select the correct power voltage for your Flat Panel with the W9 jumper.

Incorrect power voltage can damage your Flat Panel!

CAUTION

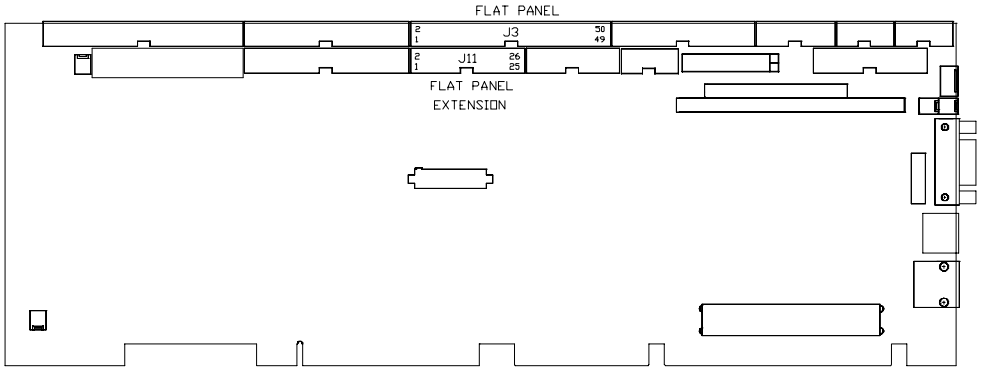
When the voltage level for the Flat Panel Control signal is set at 3.3V via the W9 jumper, only 3.3V logic levels can be used for the V-PORT connector.

12.3.2 FLAT PANEL CONNECTORS & CABLING

12.3.2.1 General Information

There are two Flat Panel connectors on the PCI-941: The J3 Flat Panel connector is a 50-pin dual row header and the J11 Flat Panel Extension connector is a 20-pin dual row header. These connectors appear below on Diagram 12-2.

DIAGRAM 12-2: Location of Flat Panel Connectors



These connectors are to be used as follow:

- For panel resolutions of 800x600 or less, use the 50-pin Flat Panel (J3) connector.
- For panel resolutions higher than 800x600, use both the Flat Panel (J3) connector and the 20-pin Flat Panel Extension (J11) connector.

The Flat Panel Extension (J11) connector is only needed for XGA TFT 2-pixels/clock panels.

The pinouts for the Flat Panel connectors appear in Table 12-2 and 12-3.

TABLE 12-2: Flat Panel Connector (J3) - Pinout

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	FP2	2	O	FP3
3	O	FP4	4	O	FP5
5	O	FP8	6	O	FP9
7	O	FP10	8	O	FP11
9	O	FP13	10	O	FP12
11	O	FP7	12	O	FP6
13	O	FP17	14	O	FP16
15	O	FP15	16	O	FP14
17	-	GND	18	-	FPVDCK (Shift Clock)
19	-	GND	20	O	FP25
21	-	GND	22	O	LFS (Frame Start)
23	O	FP1	24	O	FP18
25	-	GND	26	O	FPDE (Data Enable)
27	-	GND	28	-	GND
29	O	FP24	30	O	GP0 (Control 0)
31	O	GP1 (Control 1)	32	-	GND
33	O	FPVEE (Enable VEE)	34	-	GND
35	O	LLCLK (Line clock)	36	-	GND
37	O	FPVEE (Enable VEE)	38	-	FPVCC (Enable VCC)
39	O	FP0	40	O	GP2 (Control 2)
41	I	STNDBY*	42	O	FP30
43	O	FP19	44	O	FP31
45	I	ACTI	46	O	FPDECTL
47	-	FPVCC (3.3/5V Select)	48	-	FPVCC (3.3/5V Select)
49	-	+12V	50	-	+12V

* Active low signal

TABLE 12-3: Flat Panel Extension Connector (J11) - Pinout

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	FP20	2	-	GND
3	O	FP21	4	-	GND
5	O	FP22	6	-	GND
7	O	FP23	8	-	GND
9	O	FP26	10	-	GND
11	O	FP27	12	-	GND
13	O	FP28	14	-	GND
15	O	FP29	16	-	GND
17	O	FP32	18	-	GND
19	O	FP33	20	-	FPVCC (3.3/5V Select)
21	O	FP34	22	-	FPVCC (3.3/5V Select)
23	O	FP35	24	O	Contrast Ctrl Out (0 - 3.85 V)
25	I/O	Contrast Ctrl Pot. Hi [1]	26	I/O	Contrast Ctrl Pot. Lo [1]

1 This variable voltage output is used for adjusting contrast. Adjustment of these outputs are performed using the onboard I2C bus. For more information, contact TEKNOR's Technical Support department.

12.3.2.2 Connecting Flat Panel Video Display

The PCI-941 board supports many different types of Flat Panel displays. TEKNOR has fully tested a number of these panels and provides all the BIOS software support and the technical information needed to properly interface your PCI-941 board with your selected Flat Panel display.

12.3.2.3 Downloading Files From the TEKNOR Web Site

If you have access to the Internet, many video BIOS files in a binary format and related interconnection charts in a PDF format are available on our web site. You can download these files, if you are a customer of TEKNOR and have a password from TEKNOR. If you do not have your password, contact TEKNOR's Technical Support to obtain it.

To download a video BIOS file or its interconnection chart file, follow this procedure:

1. Access the TEKNOR web site. Our address is http://www.teknor.com .
2. Go to the Support & Services section.
3. Scroll down the list of products until you find the name of your board and click on it. This selection is a link to the board's support area.
4. Click on the Video BIOS link.
5. The list of tested Flat Panel displays appears. If you find your particular display, you can then ask to download the associated BIOS or interconnection chart files by clicking the appropriate link.
6. A pop-up window appears. You must enter your password (case sensitive) and click the SUBMIT button. Entering your e-mail address is optional. Follow the instructions in subsequent pop-ups to download the file.

12.3.2.4 More Available From TEKNOR

If you do not have access to our web site, or if you do not see the name of your Flat Panel display on our site for your specific TEKNOR board, then you need to contact TEKNOR's Technical Support department. Since we are always testing new flat panels, it is possible that we have tested your particular type of panel display. Even if we have not tested it, TEKNOR's Technical Support can do it for you and supply the video BIOS and the technical information you need.

12.3.2.5 BIOS File

The BIOS files are self-extracting files (VXX_XXX.EXE), each including two files: the flat panel BIOS file (VXX_XXX.BFP) and a DOS text file (VXX_XXX.DOC) for the BIOS update utility program.

The letters which form the BIOS name are made up of the following parts:

V	XX	_	XX	X
Video BIOS	Video Controller		Version	Revision

Once you have the correct video BIOS file, you need to copy the video BIOS file to your board's Flash BIOS device. This is done with the BIOS update utility program; see Section 22 to learn how to perform a video BIOS file update with this TEKNOR utility.

12.3.2.6 Technical Information File

The related technical information file, which includes the interconnection chart, is a PDF (Portable Document Format) file. The name of this file identifies the Flat Panel and the TEKNOR board with its video controller.

Note:
The column labeled EXTERNAL in the Display Interconnection table of the PDF file refers to the external circuitry or supplies which are needed in certain cases. This is usually an external power supply or an inverter frequently used in the clock circuit "SHFCLK" (in the case of V_{LCD} and V_{ADJ}, consult the manufacturer's flat panel data sheet for the actual voltage). An inverter is shown as  . When no special circuits are shown in this column, connections are direct.

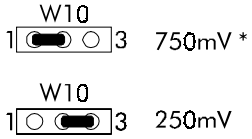
12.4 J12 PANELLINK CONNECTION

The PCI-941 provides a low voltage differential signal (LVDS) interface, also known as PanelLink, for connecting flat panel displays. The major advantage of this high speed interface is to enable a flat panel display to be connected as far as 6 feet from the board using a twisted flat cable of 3 data pairs and a clock pair.

12.4.1 PANELLINK JUMPERS

The W10 configuration jumper allows you to select the differential voltage amplitude for the PanelLink cable: 250mV, 500mV or 750mV. A higher amplitude requires higher supply current but provides greater noise immunity. Settings are shown below (* = factory setting):

W10 PanelLink Cable: Differential Voltage Amplitude

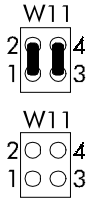


You can modify the values for the W10:1-2 setting and the W10:2-3 by changing the appropriate resistor: R35 for W10:1-2 and R34 for W10:2-3. Use this formula to determine the resistance required for the voltage you desire:

*Voltage Required (mV) = (500mV) * (500 ohm / R3x (ohm))*

The W11 configuration jumper allows you to select the PanelLink's latching on video controller signals (control and data). Latching can be on the falling edge or on the rising edge. Settings are shown below (* = factory setting):

W11 Latch Select for PanelLink Interface



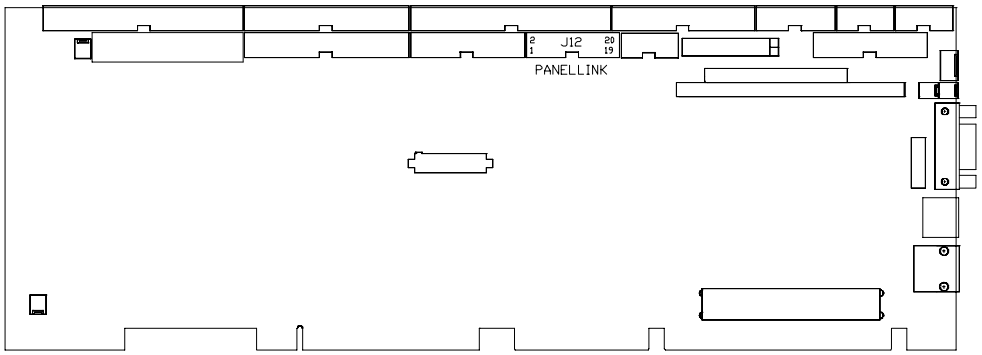
1-2: Latch on falling edge of control signals *
3-4: Latch on falling edge of data signals *

1-2: Latch on rising edge of control signals
3-4: Latch on rising edge of data signals

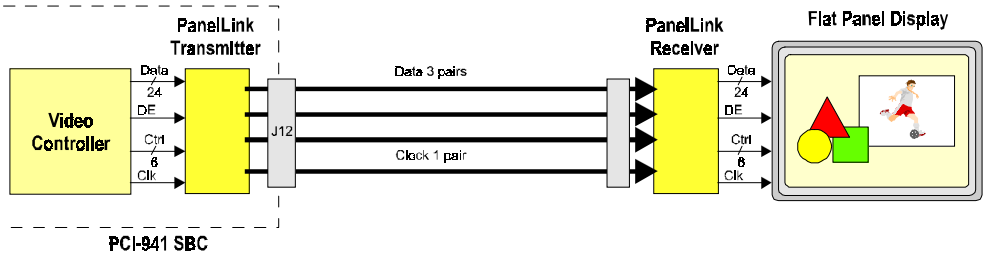
12.4.2 PANELLINK CONNECTOR & CABLING

The J12 PanelLink connector is a 20-pin dual row header. This connector appears below on Diagram 12-3.

DIAGRAM 12-3: PanelLink Connector Location



The onboard PanelLink interface and connections may be represented as follows:



Connecting a flat panel via the PanelLink connector (J12) requires and an 8-pair cable with a 20-pin dual row female header at one end and an adequate connector at the other end to connect to a PanelLink receiver. The PanelLink receiver decodes the serial data and transmits it in parallel to the flat panel.

The pinout for the PanelLink connector appears in Table 12-4.

TABLE 12-4: PanelLink Connector (J12) - Pinout

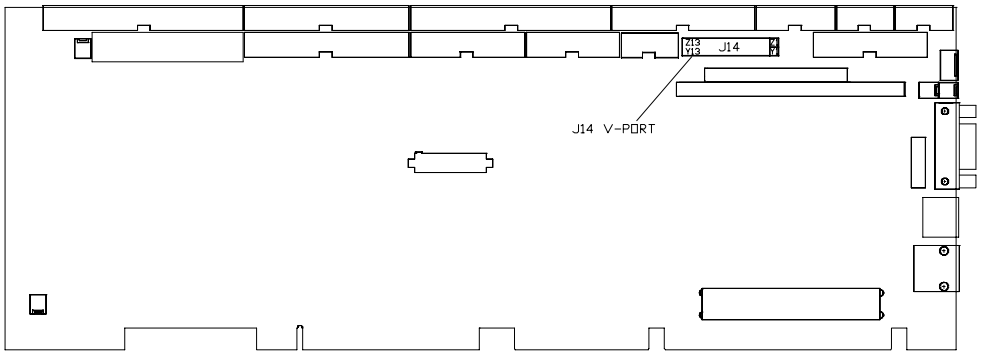
Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	GP0	2	-	+12V
3	O	GP1	4	-	GND
5	O	GP2	6	-	GND
7	-	VCC	8	-	VCC
9	O	TXC-	10	O	TXC+
11	-	VCC3	12	-	VCC3
13	O	TX0-	14	O	TX0+
15	O	TX1-	16	O	TX1+
17	O	TX2-	18	O	TX2+
19	-	FPVCC (3.3/5V Select)	20	I	PD (Power Down)

12.5 J14 V-PORT CONNECTION

The J14 connector supports the 8-bit V-PORT, with options such as live video capture (TV in a window) or hardware MPEG decode. V-PORT eliminates the need for an external video frame buffer and additional hardware. It also enables video multimedia add-in card solutions. It is compatible with TEKNOR's VIPer Vision TEK-380 Video Camera Interface module.

The J14 V-PORT connector is a 26-pin dual row header. It appears below on Diagram 12-4.

DIAGRAM 12-4: V-PORT Connector Location



The connector's pinout appears below in Table 12-5.

TABLE 12-5: V-PORT Connector (J14) - Pinout

I/O Pin	Signal Flow	Signal Name	I/O Pin	Signal Flow	Signal Name
Y1	I	VPC0	Z1	-	GND
Y2	I	VPC1	Z2	-	GND
Y3	I	VPC2	Z3	-	GND
Y4	I	VPC3	Z4	O	I2C_DATA
Y5	I	VPC4	Z5	I	VP_VSYNC
Y6	I	VPC5	Z6	O	EN_CAM*
Y7	I	VPC6	Z7	-	VCC
Y8	I	VPC7	Z8	-	GND
Y9	O	I2C_CLK	Z9	-	GND
Y10	I	VP_HSYNC*	Z10	-	GND
Y11	O	VP_OUT	Z11	-	GND
Y12	I	VP_IN	Z12	O	ZVPCLK
Y13	-	GND	Z13	I	VACTI

* Active low signal

12.6 J23 TV-OUT CONNECTION

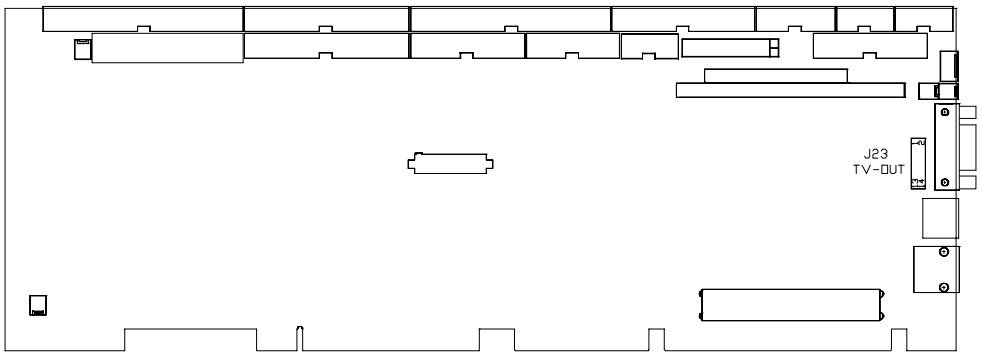
The TV-OUT connector provides signals to be used by an external encoder for the generation of NTSC-compatible outputs.

NOTE

When an external encoder (connected to the TV-OUT interface) and a CRT display are used simultaneously, only one of the two devices should be terminated.

The J23 TV-OUT connector is a 14-pin dual row header. It appears on Diagram 12-5.

DIAGRAM 12-5: TV-OUT Connector Location



The pinout for the TV-OUT connector appears below in Table 12-6.

TABLE 12-6: TV-OUT Connector (J23) - Pinout

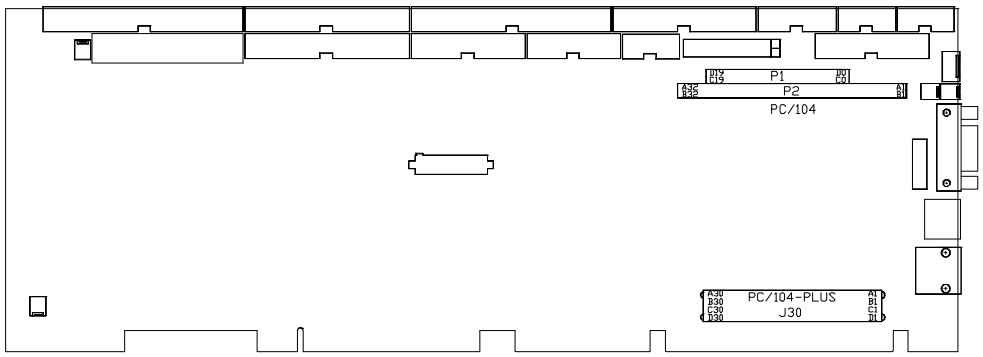
Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	RED	2	-	DAC GND
3	O	GREEN	4	-	DAC GND
5	O	BLUE	6	-	DAC GND
7	O	CSYNC	8	-	GND
9	O	TVON	10	-	GND
11	O	NTSC_PAL	12	-	GND
13	O	HSYNC	14	O	VSYNC

Please contact the Technical Support department for more information.

13. INSTALLING PC/104 & PC/104-PLUS MODULES

The PCI-941 accepts PC/104 and PC/104-Plus expansion modules. PC/104 modules provides expansion for the ISA bus and PC/104-Plus modules for the PCI bus. PC/104 and PC/104-Plus connectors are shown below in Diagram 13-1.

DIAGRAM 13-1: PC/104 & PC/104-Plus Connectors



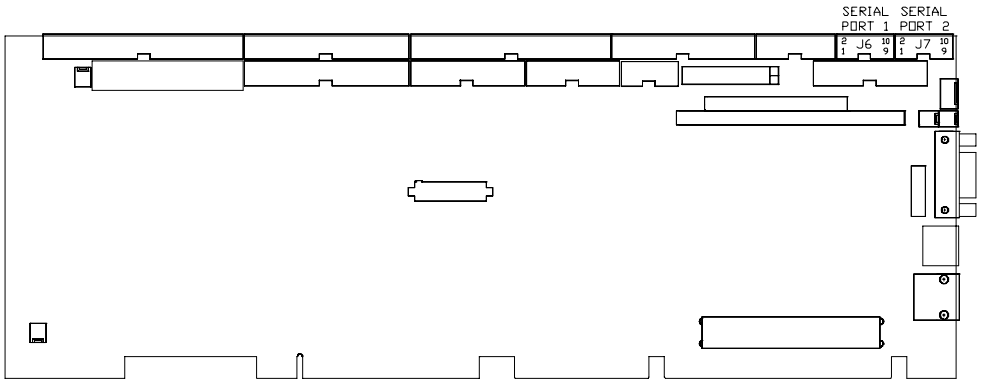
The pinouts for the PC/104 connectors are provided in the Appendix C – *Connector Location & Pinouts*.

14. INSTALLING & CONNECTING OTHER PERIPHERALS (SERIAL, PARALLEL, USB)

14.1 J6, J7 SERIAL PORT CONNECTIONS

The J6 Serial Port 1 and J7 Serial Port 2 connectors are both 10-pin dual row headers. The location for these serial ports appears below on Diagram 14-1.

DIAGRAM 14-1: Serial Ports Location



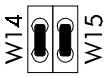
NOTE

When all the hardware connections are completed on the PCI-941, you will need to setup installed devices by software. For the serial ports, software setup includes configuring serial port 1 and serial port 2 in the AWARD Intergrated Peripherals Setup screen.

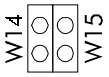
14.1.1 SERIAL PORT 2 (J7) JUMPER

In RS-485 mode, only both ends of the network must be terminated (120 ohms resistors). Termination resistors (R88 and R89) are available on the PCI-941. If the board is installed at the end of the network, use the W14 and W15 jumpers to connect the RS-485 termination resistors. Settings are shown below (* = factory setting).

W14 W15 Serial Port 2 Termination Resistors



RS-422/RS-485 with termination resistors



RS-422/RS-485
without termination resistors *

WARNING:
Do not install these jumpers when operating in RS-232 mode.

14.1.2 J6, J7 SERIAL PORT CABLE CONNECTIONS

14.1.2.1 J6/J7 RS-232 Serial Port

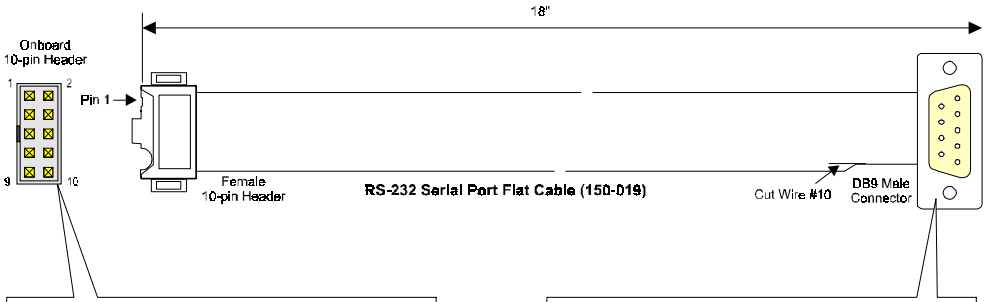
With the IBM 9-pin DSUB Standard, the J6 and J7 serial ports are 100% compatible with the IBM-AT serial port.

To connect devices on the J6 or J7 serial port, you need a 10-pin header to 9-pin DSUB cable. This cable is available from TEKNOR: part number 150-019. You can also make your own cable with a 10-pin flat ribbon cable, a 10-pin mating connector and a 9-pin DSUB.

The following list includes approved vendors for the mating connector:
Amp 746285-1 [optional strain relief: 499252-5],
Robinson Nugent IDS-C10PK-TG,
Thomas & Betts 622-1030 [optional strain relief: 622-1041].
(10-pin flat cable crimp header).

Diagram 14-2 shows the J6 / J7 serial port cable, connectors and pinouts.

DIAGRAM 14-2: J6 / J7 Serial Port Cable and Connector Pinouts



I/O	Signal	Pin #	Pin #	Signal	I/O
I	DCD	1	2	DSR	I
I	RXD	3	4	RTS	O
O	TXD	5	6	CTS	I
O	DTR	7	8	RI	I
-	GND	9	10	N.C.	-

Onboard Serial Port Connector

I/O	Signal	Pin #	Pin #	Signal	I/O
I	DSR	6	1	DCD	I
O	RTS	7	2	RX	I
I	CTS	8	3	TX	I
I	RI	9	4	DTR	O
			5	GND	-

9-pin Male DSUB Connector according to IBM-AT standard

CAUTION

The use of Taïwanese adapter cables is not recommended, since the pinout is often incorrect. The direct crimp design offered by TEKNOR allows the simplest cable assembly. All these cables are available from TEKNOR by contacting the Sales department.

14.1.2.2 J7 RS-422/RS-485 Serial Port

Serial Port 2 (J7) can be configured for RS-422 or RS-485 operation in the AWARD Setup program. Select the desired operation mode for Serial Port 2 in AWARD's Integrated Peripherals screen's COM2 Operation Mode option: RS-422 or RS-485.

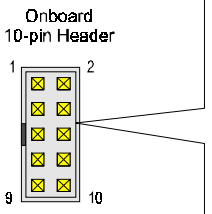
In RS-422 and RS-485 modes, the J4 serial port can transmit and receive differential signals, in either full-duplex (RS-422) or party line (RS-485) communication.

Communicating with differential signals requires one pair of wires for RS-485 and two pairs for RS-422 (one for transmission, one for reception).

For a better noise rejection, the use of twisted pair cable is highly recommended. This will enable faster serial transmissions over greater distances than with the common RS-232 protocol.

The connector pinout for Serial Port 2 when in RS-422 or RS-485 mode appears below.

DIAGRAM 14-3: RS-422 / RS-485 Pinout

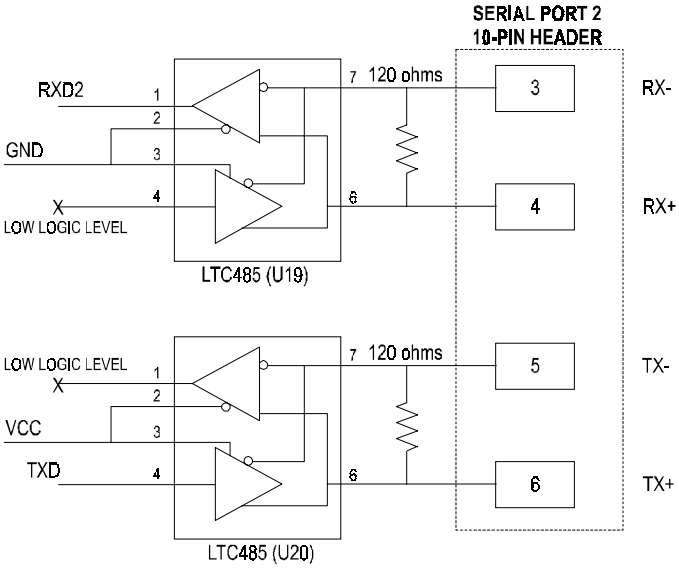


I/O	Signal	Pin #	Pin #	Signal	I/O
I	DCD	1	2	DSR	I
I/O	RX(-)	3	4	RX(+)	O
O	TX(-)	5	6	TX(+)	I
O	DTR	7	8	RI	I
-	GND	9	10	N.C.	-

Onboard Serial Port Connector set as RS-485

RS-422 - Full Duplex Operation: The RS-422 protocol uses both RX and TX lines during a communication session. Upon power-up or reset, the Serial Port 2 interface circuits are automatically configured for full duplex operation. Pins 3 and 4 of J7 act as the receiver lines and pins 5 and 6 act as the transmitter lines, as shown below.

DIAGRAM 14-4: RS-422 Signals

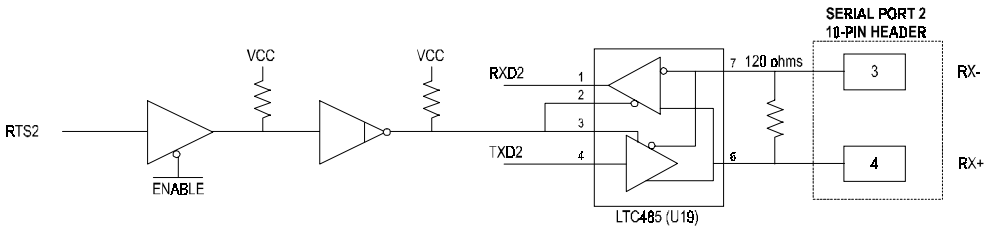


In RS-422 mode, software should not use the handshake signals (e.g., DSR, DTR), since they are not connected. However, software handshaking can be used (e.g., XON-XOFF).

RS-485 - Party Line Operation: The RS-485 offers the ability to transmit and receive over the same pair of wires (RX outputs: pins 3 and 4 as shown below), and share the same communication line with multiple stations.

The RS-485 protocol offers some advantages such as increased speed over long distances, improved reliability over similar RS-232 setups, ability to share transmission line, less cabling requirements than the RS-422 protocol.

DIAGRAM 14-5: RS-485 Signals



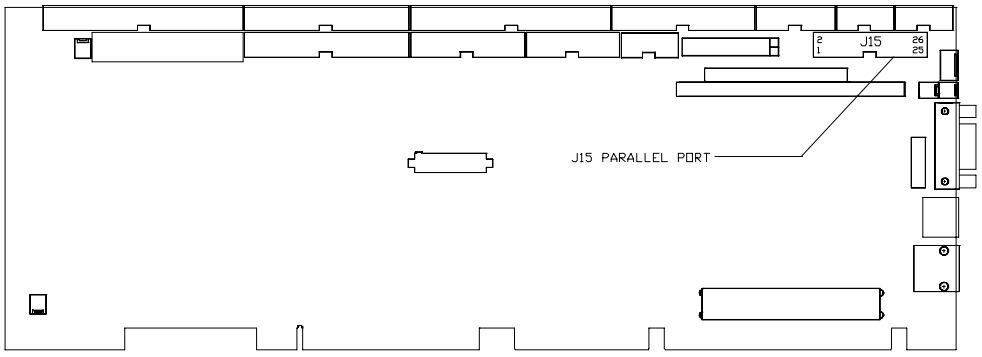
To ensure this configuration, only one system takes control of the communication at a time.

Upon power-up or reset, the transceiver is by default in "receiver mode" in order to prevent unwanted perturbation on the line.

14.2 J15 PARALLEL PORT CONNECTION

The J15 Parallel Port connector is a 26-pin dual row header. Its location is shown below on Diagram 14-6.

DIAGRAM 14-6: Parallel Port Location



NOTE

When all the hardware connections are completed on the PCI-941, you will need to setup installed devices by software. For the parallel port, software setup includes configuring the port in the AWARD Integrated Peripherals Setup screen.

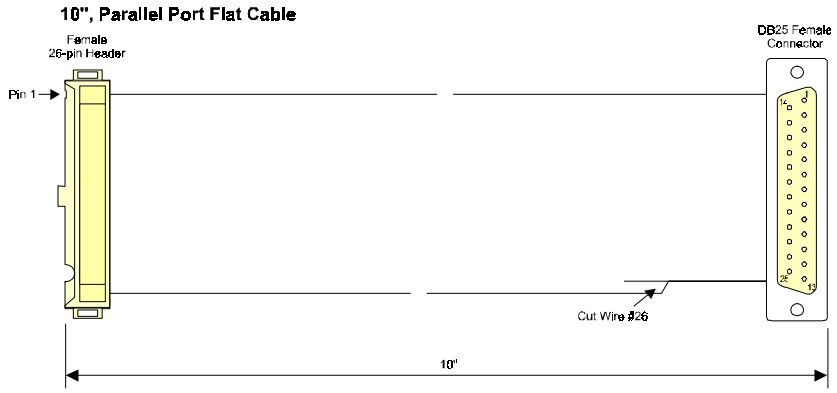
14.2.1 J15 PARALLEL PORT CABLE CONNECTION

Before connecting a device, you will need a 26-pin flat ribbon cable, a mating connector and a DB25 connector. This parallel port cable is available from TEKNOR: part number 150-172. You can also make your own cable.

The following list includes approved vendors for the flat cable mating connector:
Amp 746285-6 [optional strain relief: 499252-3],
Robinson Nugent IDS-C26PK-TG,
Thomas & Betts 622-2630 [optional strain relief: 622-2641].
(26-pin polarized IDC female socket connector).

The J15 parallel port cable with the mating connector and DB25 connector appears in Diagram 14-7.

DIAGRAM 14-7: J15 Parallel Port Cable



14.2.2 PARALLEL PORT MODES

14.2.2.1 Standard Mode

The Standard Mode is an unidirectional parallel port. It is used for compatibility with the IBM PC standard.

The following table shows the pinout for the J15 connector when it is in Standard mode:

TABLE 14-1: Parallel Port Header (J15) - Standard Mode

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	STROBE*	2	O	AUTOFD*
3	I/O	PD0	4	I	ERROR*
5	I/O	PD1	6	O	INIT*
7	I/O	PD2	8	O	SELECTIN*
9	I/O	PD3	10	-	GND
11	I/O	PD4	12	-	GND
13	I/O	PD5	14	-	GND
15	I/O	PD6	16	-	GND
17	I/O	PD7	18	-	GND
19	I	ACK*	20	-	GND
21	I	BUSY	22	-	GND
23	I	PE	24	-	GND
25	I	SELECT	26	-	GND

* Active low signal

14.2.2.2 EPP (Enhanced Parallel Port) Mode

To operate in EPP mode, the peripheral must be designed to operate in this mode and the BIOS setup must be configured to support it.

The EPP mode consists of a hardware independent method of accessing a parallel port. It provides support for single I/O cycle as well as high performance block I/O transfers.

The following table shows the pinout for the J15 connector when it is in EPP mode:

TABLE 14-2: Parallel Port Connector (J15) - EPP Mode

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	WRITE*	2	O	DATASTB*
3	I/O	PD0	4	-	Not Connected
5	I/O	PD1	6	-	Not Connected
7	I/O	PD2	8	O	ADDRSTRB*
9	I/O	PD3	10	-	GND
11	I/O	PD4	12	-	GND
13	I/O	PD5	14	-	GND
15	I/O	PD6	16	-	GND
17	I/O	PD7	18	-	GND
19	I	INTR	20	-	GND
21	I	WAIT*	22	-	GND
23	-	Not Connected	24	-	GND
25	-	Not Connected	26	-	GND

* Active low signal

14.2.2.3 ECP (Extended Capabilities Port) Mode

To operate in ECP mode, the peripheral must be designed to operate in this mode and the BIOS setup must be configured to support it.

While the EPP mode may intermix read and write operations without any overhead or protocol handshaking, the ECP mode negotiates data transfers using a request from the host and an acknowledgement from the peripheral.

The following table shows the pinout for the J15 connector when it is in ECP mode:

TABLE 14-3: Parallel Port Connector (J15) - ECP Mode

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	STROBE*	2	O	AUTOFD*, HOSTACK[2]
3	I/O	PD0	4	I	FAULT*[1], PERIPHRQST*[2]
5	I/O	PD1	6	O	INIT*[1], REVERSERQST*[2]
7	I/O	PD2	8	O	SELECTIN*[1,2]
9	I/O	PD3	10	-	GND
11	I/O	PD4	12	-	GND
13	I/O	PD5	14	-	GND
15	I/O	PD6	16	-	GND
17	I/O	PD7	18	-	GND
19	I	ACK*	20	-	GND
21	I	BUSY, PERIPHACK[2]	22	-	GND
23	I	PERROR, ACKREVERSE[2]	24	-	GND
25	I	SELECT	26	-	GND

* Active low signal
[1] Compatible Mode
[2] High Speed Mode

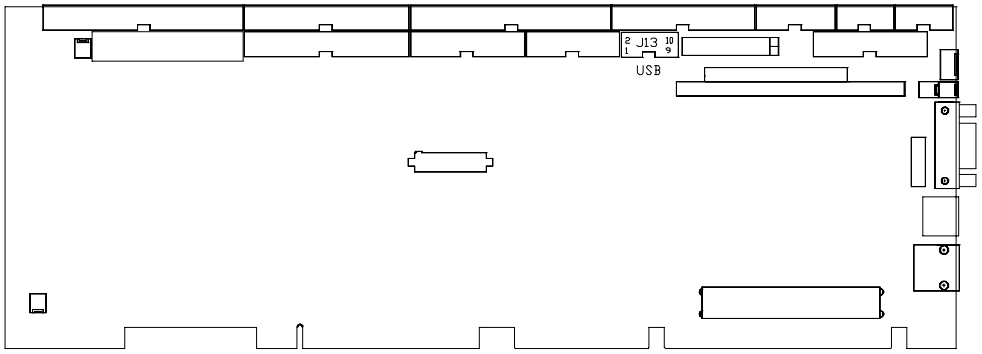
NOTE

For more information on the ECP protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard (available from Microsoft Corporation) or contact our Technical Support department.

14.3 J13 USB PORT CONNECTION

The Universal Serial Bus (USB) connector on the PCI-941 is a 10-pin dual row header which permits the direct connection of two USB connectors with an external hub. The location of the J13 USB port is shown below in Diagram 14-8.

DIAGRAM 14-8: J13 USB Port Location



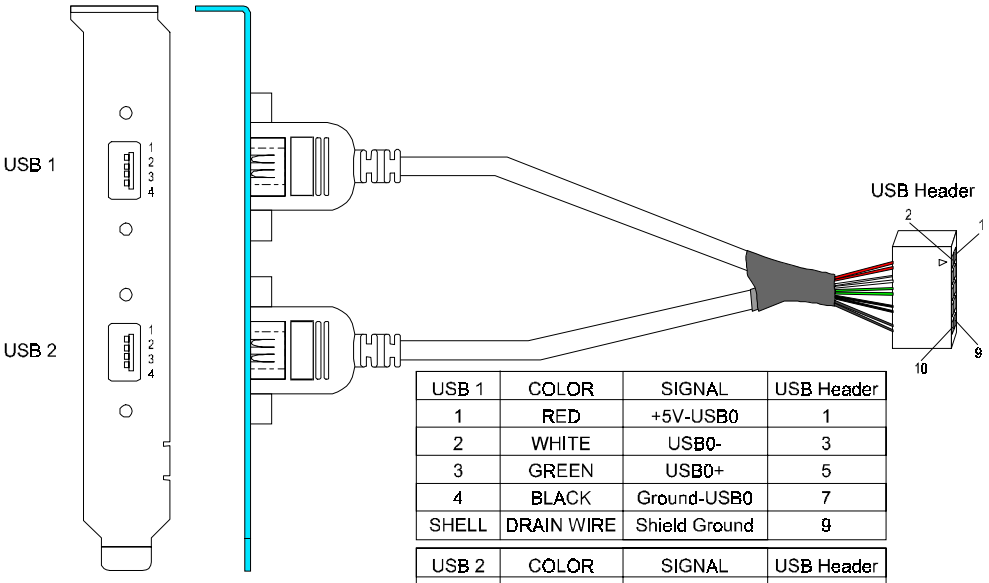
NOTE

When all the hardware connections are completed on the PCI-941, you will need to setup installed devices by software. For DOS and BIOS support, software setup includes enabling the USB Keyboard Support option in the AWARD Integrated Peripherals Setup screen.

14.3.1 USB PORT CABLE CONNECTION

Before connecting an USB device, you need to install special cabling and a bracket to the J13 connector. An USB cable/bracket assembly is available from TEKNOR: part number 150-316-00. This cable assembly appears below in Diagram 14-9. The diagram also shows the connections between the J13 10-pin header and the two external USB connectors.

DIAGRAM 14-9: USB Cable / Bracket Assembly



USB 1	COLOR	SIGNAL	USB Header
1	RED	+5V-USB0	1
2	WHITE	USB0-	3
3	GREEN	USB0+	5
4	BLACK	Ground-USB0	7
SHELL	DRAIN WIRE	Shield Ground	9

USB 2	COLOR	SIGNAL	USB Header
1	RED	+5V-USB1	2
2	WHITE	USB1-	4
3	GREEN	USB1+	6
4	BLACK	Ground-USB1	8
SHELL	DRAIN WIRE	Shield Ground	10

The J13 connector has the following pinout.

TABLE 14-4: USB Header (J13) - Pinout

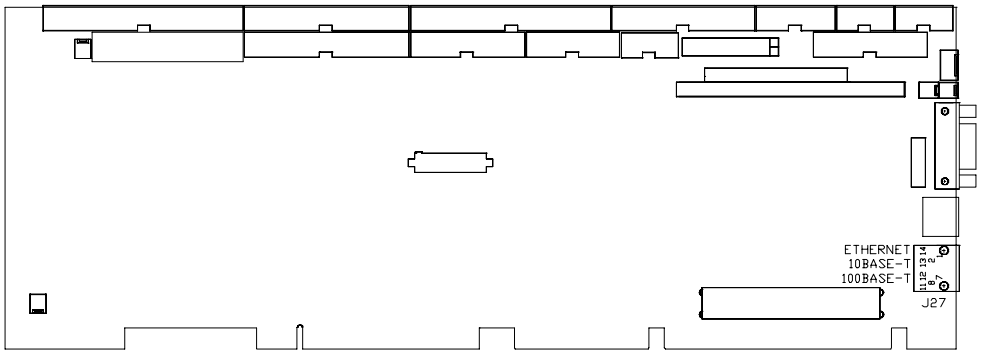
Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	-	+5V-USB0	2	-	+5V-USB1
3	I/O	USB0-	4	I/O	USB1-
5	I/O	USB0+	6	I/O	USB1+
7	-	GND-USB0	8	-	GND-USB1
9	-	SHIELD GND	10	-	SHIELD GND

15. INSTALLING & CONNECTING ETHERNET

15.1 J27 ETHERNET CONNECTION

The J27 10Base-T/100Base-TX Ethernet interface connector is an 8-pin shielded RJ-45 connector. Its location is on the I/O bracket and appears below on Diagram 15-1.

DIAGRAM 15-1: J27 Ethernet Connector Location



NOTE

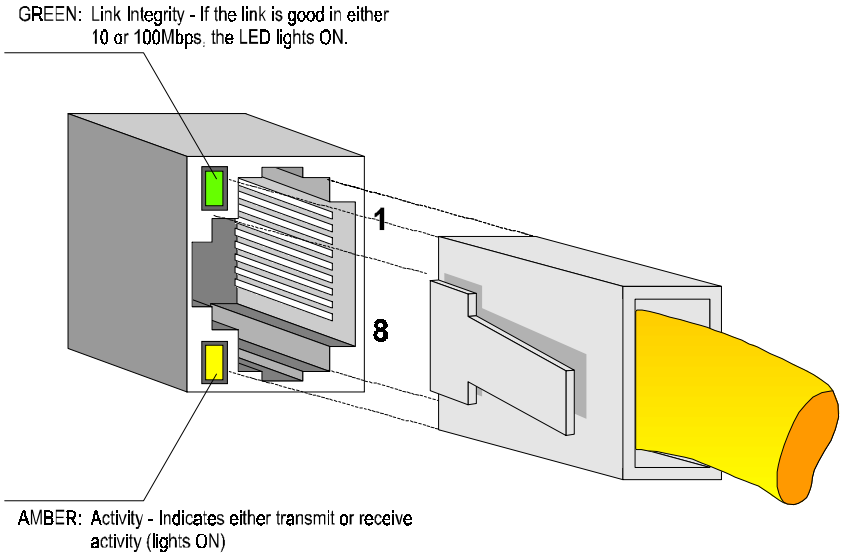
When all the hardware connections are completed on the PCI-941, you will need to setup onboard controllers and installed devices by software. The Ethernet controller on the PCI-941 resides on the PCI bus and is therefore Plug and Play by default. No manual configuration is required. For the Ethernet interface, software setup includes:

1. Ensuring that the onboard Ethernet controller is enabled in the AWARD Integrated Peripherals Setup screen. By default, the onboard Ethernet is enabled, however, it may be disabled if an external LAN card is required for testing or other purposes.
2. To configure your system to first attempt to boot from LAN: Set the Boot From LAN First option to Enabled in the AWARD Setup's BIOS Features Setup, and follow the complete procedure in the Boot From LAN utility diskette.
3. The Ethernet controller has specific drivers for various operating systems and software. To install these drivers, you must use the Utility Disk containing the Ethernet drivers for your operating system (more detail in Section 21).

15.1.1 J27 ETHERNET CABLE CONNECTION

The cable connection is made directly to the J27 RJ-45 connector on the I/O bracket. This connector is shown below in Diagram 15-2.

DIAGRAM 15-2: RJ-45 Connector



The 10Base-T interface uses UTP (Unshielded Twisted Pair) cables, category 5, 4 or 3 (5 is better).

The 100Base-TX interface uses only UTP cables category 5 and it must comply with the IEEE 802.3 10Base-T standard for two pairs.

The pinout for the 10Base-T/100Base-TX RJ-45 connector appears in Table 15-1.

TABLE 15-1: Ethernet 10Base-T/100Base-TX RJ-45 Connector (J27) - Pinout

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	TX+	2	O	TX-
3	I	RX+	4	-	RJ1[1]
5	-	RJ1[1]	6	I	RX-
7	-	RJ2[1]	8	-	RJ2[1]

[1] These lines are terminated with 75 ohm resistors.

16. INSTALLING SUPERVISOR UTILITIES

16.1 SUPERVISOR I/O REGISTERS

Two PCI-941 chips contain programmable I/O registers: the Intel PIIX4 at I/O addresses 4030h - 4037h and the XILINX CPLD at I/O 190h - 193h (may be reprogrammed in the AWARD Chipset Features Setup to 290h - 293h or 390h - 393h). Only those register bits which are needed to program the power fail detection and watchdog functions are described below.

Table 16-1 shows registers 4030h - 4037h and Table 16-2 registers 190h - 193h.

TABLE 16-1: Registers 4030h - 4037h

Register	Bit #	Function	Software Programming
4030h	0-7	Reserved	Reserved
4031h	0, 2-7	Reserved	Reserved
	1	Power Fail Output (Internal/External Battery or External Power Source)	Read: 0 = Failed, 1 = Good
4032h	0, 2-7	Reserved	Reserved
	1	Watchdog Stage 1 Status	Read: 0 = Timed out, 1 = Normal
4034h	0-7	Reserved	Reserved
4035h	0-1, 4-7	Reserved	Reserved
	2	Watchdog enable	Write: 1 = Disable, 0 = Enable
	3	Watchdog reset	Write: 1-0-1 (toggle) to activate the watchdog (when enabled)
4036h	0-7	Reserved	Reserved
4037h	0-7	Reserved	Reserved

TABLE 16-2: Registers 190h - 193h[1]

Register	Bit #	Function	Software Programming
190h	0-7	Reserved	Reserved
191h	0-4, 6	Reserved	Reserved
	5	Watchdog reset history status	Read: 1 = Last system reset caused by the watchdog timeout
	7	Push button reset history status	Read: 1 = Last system reset caused by the push button reset switch
192h	0	Clear history status (watchdog and push button)	Read/Write: 0 = Clear, 1 = Normal
	1-7	Reserved	Reserved
193h	0-7	Reserved	Reserved

[1] May be reprogrammed in the AWARD Chipset Features Setup to 290h - 293h or 390h - 393h.

16.2 POWER FAIL DETECTION

The board has various power fail detection features (* = active low signal):

1. It always monitors the +5V power supply. When it drops below 4.65 (typical), the system is reset.
2. It can monitor the onboard battery. When the battery is in a low condition (below 2.9 typical), the PFO* (power fail output) signal goes low. The status of the PFO* signal can be read at I/O address 4031h, bit 1 (0 = failed, 1 = good). The PFO* signal can also be connected to the IOCHK* signal to generate an NMI (non-maskable interrupt). The interrupt can then be serviced by an interrupt handler. If you choose not to generate an NMI, you can still use an algorithm to detect a low battery condition and respond accordingly.
3. It can monitor an external 3.6V battery. The external battery, when it replaces the onboard battery (i.e., the battery selection jumper is set to external battery), is monitored exactly as explained for the onboard battery in item 2. We recommend you use a 3.6V battery.
4. It can monitor an external battery (or other power source) with an user-defined threshold. In such a case, the onboard battery can still be connected, but it will not be monitored for low voltage. The user-defined threshold is determined by a resistor network, made up of R13, a fixed 1KΩ resistor connected to ground, and the R14 resistor installed by the user. Use this formula to calculate the right resistance needed for R14:

   $R14 = 1K\Omega \frac{(VI - 1.3)}{1.3}$ where VI is the input voltage on pin 1 of J1 (external battery).

   When the threshold is crossed, the PFO* signal goes low. The PFO* signal can also be connected to the IOCHK* signal to generate an NMI. The interrupt can then be serviced by an interrupt handler. If you choose not to generate an NMI, you can still use an algorithm to detect a power fail / low battery condition and respond accordingly.

   For more information, contact the Technical Support department.

The pinout for the external battery connector (J17) is given in Table 16-3.

TABLE 16-3: External Battery Connector (J17) - Pinout

Pin Number	Signal Flow	Signal
1	I	EXTBAT
2	-	GND

16.2.1 JUMPER SETTINGS FOR POWER FAIL DETECTION OPTIONS

Options * :

A. Onboard Battery Connected & Monitored for Low Battery

W13	Battery Selection	W13 1 ● ○ 3	Onboard Battery
W8	Power Fail: Source Selection	W8 1 ○ ● 3	Onboard or offboard battery (depending on W13 jumper) when less than 3V

B. Onboard Battery Disconnected, Offboard Battery Connected & Monitored for Low Battery

W13	Battery Selection	W13 1 ○ ● 3	Offboard Battery
W8	Power Fail: Source Selection	W8 1 ○ ● 3	Onboard or offboard battery (depending on W13 jumper) when less than 3V

C. Onboard Battery Connected, Offboard Battery / Power Source Monitored

W13	Battery Selection	W13 1 ● ○ 3	Onboard Battery
W8	Power Fail: Source Selection	W8 1 ● ○ 3	Offboard Battery (user defined power fail)

* All these options drive the power fail output (PFO) low when a low battery / power fail occurs. To generate a non-maskable interrupt (NMI) on the PFO, set the W12 jumper as follows:

W12	IOCHK Signal: Source Selection	W12 1 ● ○ 3	Power Fail Output

16.3 WATCHDOG TIMER

The PCI-941 provides a watchdog timer to monitor the processor's inactivity. The watchdog issues a failure signal if the processor fails to refresh the watchdog within the timeout period (1.6 seconds).

The PCI-941 offers a single-stage watchdog and a dual-stage watchdog (jumper selectable).

The single-stage watchdog has one watchdog timer: when it times out, a system reset is generated.

The dual-stage watchdog has two watchdog timers in cascade: when the first watchdog times out, the second watchdog becomes operational, granting the system an additional 1.6 seconds prior to system reset. When the W12: 2-3 jumper is installed, the first watchdog will generate an NMI (non maskable interrupt) when it times out. The interrupt can then be serviced by an interrupt handler.

Follow this procedure to set up the watchdog timer:

1. Enable the single-stage or dual-stage watchdog timer with the W7 jumper.
2. If you enabled the dual-stage watchdog, you can connect the IOCHK* signal to the first watchdog when it times out, so that an NMI is generated. This is done by shorting pins 2-3 of jumper W12.
3. The watchdog timer must be enabled by software. This can be done through a routine. To enable the watchdog timer by software, write "0" at I/O address 4035h bit 2.
4. The watchdog timer must be activated (refreshed) by software every 1.6 seconds. This can be done through a routine. To refresh the watchdog timer by software, write "0" and "1" at I/O address 4035h bit 3, every 1.6 seconds.
5. If a failure occurs, the single-stage watchdog generates a system reset. In the case of a dual-stage watchdog, another 1.6 seconds is provided (if IOCHK* is connected to Watchdog Stage 1, an NMI is generated and an interrupt handler can respond). The status of Watchdog Stage 1 can be read at I/O address 4032h bit 1 (0 = Timed out, 1 = Normal).

Registers 191h and 192h (see Table 14-2) are used for reading and clearing the history status. Read 191h: if bit 5 is "1", the last reset was caused by the watchdog; if bit 7 is "1", the last reset was caused by the push button reset switch. To clear the history status, write "0" to bit 0 of 192h.

NOTE

The default timeout period is 1.6 seconds; however, the timeout period can be changed. Shorting C258 and leaving R205 open changes the timeout to 100 ms. Shorting R205 and installing a capacitor at C258 will change the timeout period according to the following formulae:

$$\text{Timeout (milliseconds)} = \frac{400}{47\text{pF}} \times C$$

or

$$C258 = \frac{\text{Timeout (milliseconds)} \times 47\text{pF}}{400\text{ms}}$$

For instance, an external capacity of 100pF will lengthen the timeout to 851ms and a capacity of 1000pF will bring it to 8.5 seconds.

The watchdog can be toggle during the BIOS Power-On Self Test (POST) sequence by setting an option in the CMOS Setup program – *BIOS Features* option. When enabled, the toggle operation can be set to remain active after the BIOS POST sequence.

NOTE

The watchdog toggle routine is handled by the Timer Tick Interrupt (Int08h). Be aware that software may also require this interrupt. When operating with the watchdog, ensure there is no conflict between each part.

16.4 THERMAL MANAGEMENT

The processor module includes an user-defined temperature sensor / alarm function, which provides thermal monitoring of the processor.

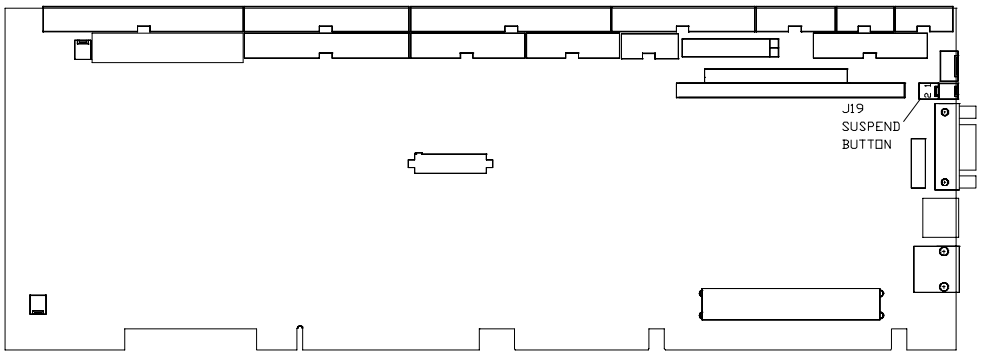
Thermal management is software configurable through the AWARD Thermal Management Setup screen. The options are:

- Thermal Management: To enable / disable the thermal management function. When enabled, the temperature sensors always monitors the die (internal) and case (external) CPU temperature. The next functions are only available when this option is enabled.
- Thermal Audio Alarm: To enable / disable a continuous audible alarm when the temperature specified in the Overheat Alarm options is reached. Such an alarm may not be supported by the Operating System.
- CPU Die Temperature (°C): Displays the current CPU die temperature.
- (CPU Die Temperature) Resume Alarm (°C): To set the internal CPU temperature's low limit. When the CPU is in Doze Mode, it will resume Normal Mode operation, when it reaches the temperature specified in the Resume Alarm option.
- (CPU Die Temperature) Overheat Alarm (°C): To set the CPU die temperature's high limit. When the CPU is in Normal Mode and it reaches the temperature specified in the Overheat Alarm option, it will go into Doze Mode.
- CPU Case Temperature (°C): Displays the current CPU case temperature.
- (CPU Case Temperature) Resume Alarm (°C): To set the CPU case temperature's low limit. When the CPU is in Doze Mode, it will resume Normal Mode operation, when it reaches the temperature specified in the Resume Alarm option.
- (CPU Case Temperature) Overheat Alarm (°C): To set the CPU case temperature's high limit. When the CPU is in Normal Mode and it reaches the temperature specified in the Overheat Alarm option, it will go into Doze Mode.

17. CONNECTING SUSPEND BUTTON

The J19 Suspend Button connector is a 2-pin lock header. Its location appears below in Diagram 17-1.

DIAGRAM 17-1: Suspend Button Connector Location



The connector is used for installing a push button switch for power management purposes. Shorting pins 1 and 2 places the system in Suspend Mode (maximum power management mode), or returns to Normal Mode when in Suspend Mode. Note that pins 11 and 12 of the J5 Multi-Function connector has the same function (see section 10.2.1).

The connector's pinout appears below in Table 17-1.

TABLE 17-1: Suspend Button Connector (J19) - Pinout

Pin Number	Signal Flow	Signal
1	I	PWRBT*
2	-	GND

* Active low signal

18. POWERING UP THE SYSTEM & TROUBLESHOOTING

18.1 POWER SOURCE FOR THE PCI-941

The PCI-941 Single Board Computer is powered via the ISA bus when it is installed on a passive backplane.

18.2 POWER UP PROCEDURE

You are now ready to power up your system.

1. Insert a bootable diskette in drive A to start your system with DOS.
2. Hit the DELETE key before or when this message appears near the bottom of the screen: ″Press DEL to enter SETUP″. This will bring you to the Main Menu of the AWARD BIOS CMOS Setup Utility. Use the arrow keys to select among the items and press ENTER to accept.
   - Select ″STANDARD CMOS SETUP″ to set the date and time.
     More detail on the AWARD Setup is given in Section 19 of this manual.
   - Select ″LOAD SETUP DEFAULTS″ to reset the setup.
   - Select ″SAVE & EXIT SETUP″ to continue the boot procedure.
3. Once the boot procedure is completed, reboot the system to make sure everything works properly.

18.3 TROUBLESHOOTING

If you should encounter a problem, verify the following items:

- Make sure that all connectors are connected properly. On the standard flat ribbon cable used for the floppy connector, pin 1 is indicated by a small red stripe. Verify that this red stripe is located on the appropriate side of the connector.
- Verify your boot diskette. It must be a system disk and it must be in proper working order.
- If the system still does not start up properly, you should try booting your system with only the video monitor connected to the board (this is the minimum required to see if the board is working).
- If you still are not able to start up your system, please refer to the Emergency Procedure in Appendix J.
- If you still are not able to get your board up and running, contact our Technical Support department for assistance.

PART 3

SOFTWARE & ONBOARD UTILITIES

19. AWARD SETUP PROGRAM

Normally the software setup will follow all system hardware connections in order to configure controllers and installed devices.

Also, software setup should come before any operating systems and drivers are installed.

NOTE

Make sure you setup the AWARD software prior to installing your operating system and your drivers.

NOTE

For systems which need the BIOS to first attempt to boot from LAN, follow these steps:

1. Set the Boot From LAN First option to Enabled in the AWARD Setup's BIOS Features Setup.
2. Follow the complete procedure in the LAN Boot & SCSI Utility diskettes.

19.1 ACCESSING THE AWARD SETUP PROGRAM

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the PCI-941 single board computer. The interface provided by AWARD is 100% IBM AT compatible. All functions accept similar inputs as IBM and provide the same results, although the program code itself is different.

The PCI-941 uses the AWARD Setup program, a setup utility in flash memory that is accessed by pressing the DELETE key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

CAUTION

Before modifying CMOS setup parameters, ensure that the W13 battery selection jumper is installed to enable the CMOS battery back-up (settings in section 6.1).

To run the AWARD Setup program incorporated in the ROM BIOS:

1. Turn on or reboot the system.
2. Hit the DELETE key before or when the message - "Press DEL To Enter SETUP" appears near the bottom of the screen.
3. The main menu of the AWARD BIOS CMOS Setup Utility appears on the screen.

ROM PCI/ISA BIOS (2A69LB39)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.

STANDARD CMOS SETUP	LOAD BIOS DEFAULTS
BIOS FEATURES SETUP	LOAD SETUP DEFAULTS
CHIPSET FEATURES SETUP	SUPERVISOR PASSWORD
POWER MANAGEMENT SETUP	USER PASSWORD
THERMAL MANAGEMENT SETUP	IDE HDD AUTO DETECTION
PNP/PCI CONFIGURATION	SAVE & EXIT SETUP
INTEGRATED PERIPHERALS	EXIT WITHOUT SAVING
Esc : Quit F10 : Save & Exit Setup	↑ ↓ → ← : Select Item (Shift)F2 : Change Color
Time, Date, Hard Disk Type . . .	

19.2 USING AWARD SETUP

The arrow keys (↑ ↓ → ←) are used to highlight items on the menu and the PAGEUP and PAGEDOWN keys are used to change the entry values for the highlighted item. To select an entry, press the ENTER key. Also, you can press the F1 key to obtain help information or the ESC key to leave an option, close a menu or to quit the program.

Table 19-1 provides more details on how to navigate in the Setup program:

TABLE 19-1: Using AWARD Setup Program

Key	Function
↑	Moves to previous item.
↓	Moves to next item.
←	Moves to the item in the left hand.
→	Moves to the item in the right hand.
ESC	When in the Main Menu: Quits program (Answer 'Y' to save changes into CMOS). When in other screens: Exits and returns to the Main Menu.
PAGEUP or +	Increases the numeric value or changes value.
PAGEDOWN or -	Decreases the numeric value or changes value.
F5	When in the Main Menu: Restores the previous setup values for all the BIOS parameters (except Standard CMOS) which were displayed when you entered the program. When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, Thermal Management Setup, PNP/PCI Setup or Integrated Peripherals Setup: Restores the previous setup values for that setup screen only.
F6	When in the Main Menu: Loads the BIOS Defaults of all the BIOS parameters (except Standard CMOS). The BIOS Defaults are fail safe settings which consist of the safest set of parameters. When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, Thermal Management Setup, PNP/PCI Setup or Integrated Peripherals Setup: Loads the BIOS Defaults for all the BIOS parameters for that setup screen only.
F7	When in the Main Menu: Loads the Setup Defaults for all the BIOS parameters (except Standard CMOS). When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, Thermal Management Setup, PNP/PCI Setup or Integrated Peripherals Setup: Loads the Setup Defaults for all the BIOS parameters for that setup screen only.
F10	When in the Main Menu: Saves all the CMOS changes.

The Main Menu includes the following categories:

Standard CMOS Setup	This Setup page includes all the items in a standard, AT-compatible BIOS (date, time, hard disk type, floppy disk type, video adapter type, memory…).
BIOS Features Setup	This Setup page includes all the items of AWARD's special enhanced features.
Chipset Features Setup	This Setup page includes all the items of the chipset's special features.
Power Management Setup	This Setup page sets power conservation options.
Thermal Management Setup	This Setup page sets thermal management options.
PnP/PCI Configuration	This Setup page sets plug and play and PCI configuration options.
Integrated Peripherals	I/O susbsystems that depend on the integrated peripherals controller in your system.
Load Bios Defaults	The BIOS defaults are fail safe settings which consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.
Load Setup Defaults	The Setup defaults are optimal settings which provide optimum performance for all devices and system features. If CMOS RAM is corrupted, the Setup defaults are loaded automatically.
Supervisor/User Password Setting	Change, set, or disable password. It allows you to limit access to the system and the Setup, or just to the Setup.
IDE HDD Auto Detection	Automatically detect and configure IDE hard disk parameters.

19.3 SAVING CONFIGURATIONS & EXITING AWARD SETUP

Use one of the following options available from the Main Menu:

Save & Exit — After having modified the AWARD Setup, you can save the configuration in CMOS RAM and the Flash BIOS, by selecting this option.

Exit Without Saving — This option is used to exit AWARD Setup without saving the configuration to CMOS RAM.

19.4 STANDARD CMOS SETUP

This part of the setup allows you to set the time, date, hard disk type, types of floppy drives and video type.

Date/Time — The current values for each category are displayed. Enter new values through the keyboard.

Hard Disks — Two IDE controllers are defined on the PCI-941 board. The Primary and Secondary controller can have two disks: Master Disk or Slave Disk. The disks are bootable in this order: 1) Primary Master, 2) Primary Slave, 3) Secondary Master, and 4) Secondary Slave. The W4 jumper configures the CompactFlash disk as Secondary Master or Secondary Slave.

Only three settings are available for the hard disk type: Auto, 47 (user defined) and None. Type 1 to 46 are not predefined in the system: Use auto-detect or enter the parameters for the type in the user-defined type 47.

Drive A / Drive B — Select the type of floppy disk installed for drive A and drive B.

Video — This option specifies the basic type of display adapter card installed in the system.

CRT & LCD — This option allows the user to set the display mode for the video controller: CRT Only (default), LCD Only or Both.

Halt on — This option specifies the type of errors that will stop the system during the BIOS booting procedure. A message asks that you press F1 to continue or press the DELETE key to enter Setup. The settings are: All errors, No errors, All but keyboard, All but diskette, and All but disk/key (default setting).

Memory — This display-only option indicates the amount of Base, Extended and other types of memory installed in the system.

19.5 BIOS FEATURES SETUP

This part of the setup handles options and features such as boot sequence, NUM LOCK, security options, shadowing, …

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP default values provide optimum performance settings for all devices and system features.

TABLE 19-2: BIOS Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Virus Warning	Disabled	Disabled	Enabled, Disabled	When Enabled, you receive a warning message if a program (specifically, a virus) attempts to write to the boot sector or the partition table of the hard disk drive. You should then run an anti-virus program. Keep in mind that this feature protects only the boot sector, not the entire hard drive. **Note: Many disk diagnostic programs and OS setups (e.g., Win95 setup), that access the boot sector table, can trigger the virus warning message. If you plan to run such a program, we recommend that you first disable the virus warning.**
CPU Internal Cache	Disabled	Enabled	Enabled, Disabled	Enables or Disables the CPU Internal Cache (L1 cache).
External Cache	Disabled	Enabled	Enabled, Disabled	Enables or Disables the External Cache (L2 cache).
CPU L2 Cache ECC Checking	Disabled	Enabled	Enabled, Disabled	Enables or Disables ECC Checking for L2 cache.

TABLE 19-2: BIOS Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Quick Power On Self Test	Disabled	Enabled	Enabled, Disabled	Select Enabled to reduce the amount of time required to run the power-on self test (POST). A quick POST skips certain steps. We recommend that you enable quick POST to save time, since most major OS do their own tests
Boot From LAN First	Disabled	Disabled	Enabled, Disabled	If Enabled, the BIOS will first attempt to boot from the LAN. The complete procedure for this function is available on the Boot From LAN utility diskette.
Boot Sequence	A,C,SCSI	C,A,SCSI	A,C,SCSI; C,A,SCSI; C,CDROM,A; CDROM,C,A; D,A,SCSI; E,A,SCSI; F,A,SCSI; SCSI,A,C; SCSI,C,A; C only; LS/ZIP,C.	This option defines the searching order in the BIOS for the boot device(s).
Swap Floppy Drive	Disabled	Disabled	Enabled, Disabled	Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B. If there is only one floppy on the system, it could be assigned to B with this option.
Boot Up Floppy Seek	Enabled	Disabled	Enabled, Disabled	When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360KB floppy drives have 40 tracks; drives with 720KB, 1.2MB, and 1.44MB capacity all have 80 tracks. Because very few modern PCs have 40 track floppy drives, we recommend that you set this field to "Disabled" to save time.
Drive A Boot Permit	Enabled	Enabled	Enabled, Disabled	When Disabled, this option will not permit booting from Drive A.
Floppy Disk Access Control	R/W	R/W	R/W, Read Only	When Read Only, this option will not permit writing to the floppy disk.
Hard Disk Write Protect	Disabled	Disabled	Enabled, Disabled	When Enabled, this option will not permit writing to the hard disk.
HDD S.M.A.R.T. Capability	Disabled	Enabled	Enabled, Disabled	This option allows BIOS to use the S.M.A.R.T. (System Management and Reporting Technologies) protocol for reporting server system information over a network.

TABLE 19-2: BIOS Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Boot Up NumLock Status	On	On	On, Off	Toggle between On or Off to control the state of the NumLock key when the system boots. When toggled On, the numeric keypad generates numbers instead of controlling cursor operations.
Typematic Rate Setting	Disabled	Enabled	Enabled, Disabled	When Disabled, the following two items (Typematic Rate and Typematic Delay) are irrelevant. Keystrokes repeat at a rate determined by the keyboard controller in your system. When Enabled, you can select a typematic rate and a typematic delay.
Typematic Rate (Chars/Sec)	30	30	6, 8, 10, 12, 15, 20, 24, 30 char. per sec.	When the typematic rate setting is Enabled, you can select a typematic rate (the rate at which characters repeat when you hold down a key).
Typematic Delay (Msec)	250	250	250, 500, 750, 1000 ms	When the typematic rate setting is Enabled, you can select a typematic delay (the delay before key strokes begin to repeat).
PCI/VGA Palette Snoop	Disabled	Disabled	Enabled, Disabled	Palette snooping allows multiple VGA devices operating on different buses to handle data from the CPU on each set of palette registers. When set to Enabled, data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA device's palette registers, permitting the palette registers of both to be identical. When set to Disabled, data read and written by the CPU is only directed to the PCI VGA device's palette registers.
OS Select For DRAM > 64MB	Non-OS2	Non-OS2	Non-OS/2, OS/2	Select OS2 only if you are running OS/2 with greater than 64MB of RAM.
Gate A20 Option	Normal	Fast	Normal, Fast	When Fast, enables fast switching of Gate A20 via the 440BX chipset, instead of the keyboard controller.
Security Option	Setup	Setup	Setup, System	If you have set a password, select whether the password is required every time the system boots ("System" option), or only when you enter Setup ("Setup" option).
Save CMOS in Flash	Disabled	Disabled	Enabled, Disabled	When this option is set to "Enabled", the CMOS RAM Setup will be restored from the Flash BIOS at each power up. If the battery fails, only the date and time could be lost.

TABLE 19-2: BIOS Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Video BIOS Shadow	Disabled	Enabled	Enabled, Disabled	Software that resides in a read-only memory (ROM) chip on a device is called *firmware*. Award permits shadowing of firmware such as the system BIOS, video BIOS, and similar operating instructions that come with some expansion peripherals. Shadowing copies from ROM into system RAM, where the CPU can read it through the 64-bit DRAM bus. Firmware not shadowed must be read by the system through the 8-bit or 16-bit X-bus. Shadowing improves the performance of the system BIOS and similar firmware for expansion peripherals. Enable shadowing into each section of memory separately. Many system designers hardwire shadowing of the system BIOS and eliminate a System BIOS Shadow option. Note that on a PCI VGA card (onboard or offboard), the VGA BIOS is always shadowed. Video BIOS shadows into memory area C0000 plus the VGA BIOS size. The remaining areas between C0000 and DFFFF shown on the BIOS Features Setup screen may be occupied by other expansion card firmware. If an expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies to shadow it into the correct area of RAM.
C8000-CBFFF Shadow	Disabled	Disabled	Enabled, Disabled	
CC000-CFFFF Shadow	Disabled	Disabled	Enabled, Disabled	
D0000-D3FFF Shadow	Disabled	Disabled	Enabled, Disabled	
D4000-D7FFF Shadow	Disabled	Disabled	Enabled, Disabled	
D8000-DBFFF Shadow	Disabled	Disabled	Enabled, Disabled	
DC000-DFFFF Shadow	Disabled	Disabled	Enabled, Disabled	
Watchdog Timer	Disabled	Disabled	Enabled, Disabled	Enable this function to toggle the watchdog timer during the BIOS POST sequence (handled Int08h)
Watchdog After POST	Disabled	Disabled	Enabled, Disabled	When the watchdog is set, use this option to continue toggling the watchdog after the BIOS POST sequence (Int08h remains used)

19.6 CHIPSET FEATURES SETUP

This part of the setup allows you to define chipset-specific options and features.

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP default values provide optimum performance settings for all devices and system features.

CAUTION

These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

TABLE 19-3: Chipset Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
SDRAM CAS Latency Time	3	3	2, 3	For 100MHz SDRAM, set this option to 2 (clocks). For 66MHz SDRAM, set this option to 3 (clocks).
DRAM Data Integrity Mode	Non-ECC	Non-ECC	ECC, Non-ECC	When set to ECC, allows auto-correction of the data read from memory. It does not scrub the memory. The ECC error flags' status register and the error pointer are updated if error correction occurs in this mode. When set to Non-Ecc, no error checking or error reporting is done.
System BIOS Cacheable	Disabled	Enabled	Enabled, Disabled	Selecting Enabled allows caching of the system BIOS ROM at F0000h-FFFFFh, resulting in better system performance. However, if any program writes to this memory area, a system error may occur.

TABLE 19-3: Chipset Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Video BIOS Cacheable	Disabled	Enabled	Enabled, Disabled	Selecting Enabled allows caching of the video BIOS ROM at C0000h plus the VGA BIOS size, resulting in better video performance. However, in any program writes to this memory area, a system error may occur.
Video RAM Cacheable	Disabled	Disabled	Enabled, Disabled	When Enabled, video memory region is cacheable. Some offboard video card drivers may behave strangely; in such a case, disable this option.
8 Bit I/O Recovery Time	3	1	1, 2, 3, 4, 5, 6, 7, 8, NA	The I/O recovery mechanism adds bus clock cycles between PCI-originated I/O cycles to the ISA bus. This delay takes place because the PCI bus is so much faster than the ISA bus. These two fields let you add recovery time (in bus clock cycles) for 16-bit and 8-bit I/O.
16 Bit I/O Reccovery Time	2	1	1, 2, 3, 4, NA	
Memory Hole At 15M-16M	Disabled	Disabled	Enabled, Disabled	You can reserve this area of system memory for ISA adapter ROM. When this area is reserved, it cannot be cached. The user information of peripherals that need to use this area of system memory usually discusses their memory requirements.
Passive Release	Enabled	Enabled	Enabled, Disabled	When Enabled, CPU to PCI bus accesses are allowed during passive release otherwise the arbiter only accepts another PCI master access to local DRAM.
Delayed Transaction	Enabled	Enabled	Enabled, Disabled	The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specifications version 2.1.
Supervisor I/O Base Addr.	190h	190h	190h, 290h, 390h	This option determines the base address for the Supervisor I/O Register, which is used for such functions as power fail detection and the watchdog timer.

19.7 POWER MANAGEMENT SETUP

This part of the setup sets power conservation options.

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP default values provide optimum performance settings for all devices and system features.

TABLE 19-4: Power Management Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
ACPI Function	Disabled	Enabled	Enabled, Disabled	When Enabled and the OS supports ACPI or OSPM (e.g., Win98, Window NT 5), power management functionality moves to the OS. **Note: When Enabled, all other options in the Power Management Setup will not be used.**
Power Management	Disable	User Define	Min Saving, Max Saving, User Define, Disable	This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. Max Saving: Maximum power savings. Inactivity period is 1 minute in each mode. Min Saving: Minimum power savings. Inactivity period is the maximum setting in each mode (1 hour for Doze, Standby and Suspend). User Define: Set each mode individually. Select time-out periods in the PM Timers section (see below).
PM Control by APM	Yes	Yes	Yes, No	If Yes, the OS will control the PM by APM calls. If No, the BIOS will control the PM and APM calls from the OS will be ignored.

TABLE 19-4: Power Management Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Video Off Method	V/H SYNC+Blank	V/H SYNC+Blank	V/H SYNC+Blank, DPMS, Blank Screen	Determines the manner in which the monitor is blanked. V/H SYNC + Blank: System turns off vertical and horizontal synchronization ports and writes blanks to the video buffer. DPMS Support: Select this option if your monitor supports the Display Power Management Signaling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsytem to select video power management values. Blank Screen: System only writes blanks to the video buffer.
Video Off After	Standby	Standby	Doze, Standby, Suspend, NA	As the system moves from lesser to greater power-saving modes, select the mode in which you want the monitor to blank.
Modem Use IRQ	3	3	N/A, 3, 4, 5, 7, 9, 10, 11	Name the IRQ line assigned to the modem (if any) on your system. Activity of the selected IRQ always awakens the system.
PM Timers:				The following modes are Green PC power saving functions. They are user-configurable only during User Defined Power Management mode.
Doze Mode	Disable	20 Min	1, 2, 4, 6, 8, 10, 20, 30, 40 Min, 1 Hour, Disable	After the selected period of system inactivity (1 minute to 1 hour), the CPU clock runs at lower speed while all other devices still operate at full speed.
Standby Mode	Disable	40 Min	1, 2, 4, 6, 8, 10, 20, 30, 40 Min, 1 Hour, Disable	After entering Doze mode and the selected period of system inactivity (1 minute to 1 hour) has elapsed, the fixed disk drive and the video shut off while all other devices still operate at full speed.
Suspend Mode	Disable	1 Hour	1, 2, 4, 6, 8, 10, 20, 30, 40 Min, 1 Hour, Disable	After entering Standby mode and the selected period of system inactivity (1 minute to 1 hour) has elapsed, all devices except the CPU shut off.
HDD Power Down	Disable	15 Min	1, 2, 3, (…), 15 Min, Disable	After the selected period of drive inactivity (1 to 15 minutes), the hard disk drive powers down while all other devices remain active. The HDD power down mode is only available if the hard drive has this capability.

TABLE 19-4: Power Management Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Throttle Duty Cycle	75.0%	75.0%	12.5%, 25.0%, 37.5%, 50.0%, 62.5%, 75.0%	When the system enters Doze mode, the CPU clock runs only part of the time. You may select the percentage of time that the clock does not run.
VGA Active Monitor	Enabled	Enabled	Enabled, Disabled	When Enabled, any video activity restarts the global timer for Standby mode.
Resume by Ring	Disabled	Enabled	Enabled, Disabled	When Enabled and a modem is connected to a COM port, allows a modem ring to re-activate the CPU when in Suspend mode.
Resume by Alarm	Disabled	Disabled	Enabled, Disabled	When Enabled, allows setup of a time to re-activate the CPU when in Suspend mode with the options Date (of Month) Alarm and Time (hh:mm:ss) Alarm. **Note: The IRQ 8 Break Suspend option in this setup screen must be Enabled to use the RTC alarm.**
Date (of Month) Alarm	-	-	A number between 0 and 31	This option appears only if Resume by Alarm is enabled. It specifies the date in the month for the RTC alarm.
Time (hh:mm:ss) Alarm	-	-	A time between 0:0:0 and 23:59:59	This option appears only if Resume by Alarm is enabled. It specifies time of day for the RTC alarm.
IRQ 8 Break Suspend	Disabled	Enabled	Enabled, Disabled	When Enabled, the RTC alarm interrupt is monitored to allow an interrupt to awaken the system when in Doze, Standby or Suspend Mode.
Reload Global Timer Events:				When any of the options below is Enabled, monitoring of the interrupt will occur to allow an interrupt to awaken the system when in Doze, Standby or Suspend Mode.
IRQ[3-7,9-15], NMI	Disabled	Enabled	Enabled, Disabled	
Primary IDE 0	Disabled	Disabled	Enabled, Disabled	
Primary IDE 1	Disabled	Disabled	Enabled, Disabled	
Secondary IDE 0	Disabled	Disabled	Enabled, Disabled	
Secondary IDE 1	Disabled	Disabled	Enabled, Disabled	
Floppy Disk	Disabled	Disabled	Enabled, Disabled	
Serial Port	Enabled	Enabled	Enabled, Disabled	
Parallel Port	Disabled	Disabled	Enabled, Disabled	

19.8 THERMAL MANAGEMENT SETUP

This part of the setup sets thermal management options.

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP default values provide optimum performance settings for all devices and system features.

TABLE 19-5: Thermal Management Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Thermal Management	Disabled	Disabled	Enabled, Disabled	When this option is enabled, the CPU temperature is monitored. Whenever the CPU overheats, the CPU slows down to lower the temperature.
Thermal Audio Alarm	Disabled	Disabled	Enabled, Disabled	When the Thermal Management option and this option are enabled, a continuous audible alarm is sounded when the temperature specified in the Overheat Alarm options is reached. Such an alarm may not be supported by the Operating System.
CPU Die Temperature (°C)	-	-	Varies	Displays the current die (internal) CPU temperature, when Thermal Management is enabled.
(CPU Die Temperature) Resume Alarm (°C)	30	30	10 to 70 by increments of 4	The CPU will be slowed down (Doze mode) when it reaches the selected Overheat Alarm (°C) temperature. Full speed (Normal mode) will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 4° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm.
(CPU Die Temperature) Overheat Alarm (°C)	50	50	30 to 90 by increments of 4	

TABLE 19-5: Thermal Management Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
CPU Case Temp. (°C)	-	-	Varies	Displays the current case (external) CPU temperature, when Thermal Management is enabled.
(CPU Case Temperature) Resume Alarm (°C)	34	34	10 to 70 by increments of 4	The CPU will be slowed down (Doze mode) when it reaches the selected Overheat Alarm (°C) temperature. Full speed (Normal mode) will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 4° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm.
(CPU Case Temperature) Overheat Alarm (°C)	50	50	30 to 90 by increments of 4	

19.9 PNP/PCI CONFIGURATION

This part of the setup sets PnP/PCI options.

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP default values provide optimum performance settings for all devices and system features.

TABLE 19-6: PnP/PCI Configuration

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
PNP OS Installed	No	Yes	Yes, No	If the operating system (OS) is Plug and Play (for example Windows 95), select "Yes" if you want the OS to allocate resources according to Plug and Play standards, or "No" if you want the same resource allocations at every system boot-up. Select "No" when the OS is not Plug and Play (for example, DOS).
Resources Controlled By	Auto	Manual	Auto, Manual	The Award Plug and Play BIOS can automatically configure all the boot and Plug and Play-compatible devices. If you select Auto, all the interrupt requests (IRQs) and DMA assignment fields disappear, as the BIOS automatically assigns them.
Reset Configuration Data	Disabled	Disabled	Enabled, Disabled	Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.

TABLE 19-6: PnP/PCI Configuration (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
IRQ *n* Assigned To	PCI/ISA PnP	PCI/ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific interrupt, such as IRQ4 for serial port 1. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for an IRQ line, this resource will not be available for PCI/ISA PnP.
DMA *n* Assigned To	PCI/ISA PnP	PCI/ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system DMA channel as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific DMA channel. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for a DMA channel, this resource will not be available for PCI/ISA PnP.
Used MEM Base Address	N/A	N/A	N/A, C800, CC00, D000, D400, D800, DC00	Select a base address for the memory area used by any peripheral that requires high memory.
Used MEM Length	8K	8K	8K, 16K, 32K, 64K	Select a length for the memory area specified in the previous field. This field does not appear if no base address is specified.
Assign IRQ For USB	Enabled	Enabled	Enabled, Disabled	When Enabled, the USB is assigned an IRQ. When Disabled, the IRQ is freed up for another purpose.
PCI Latency Timer	32	32	0 to 255 (integers)	This option specifies the value of the Latency Timer for the PCI bus master, in units of PCI bus clocks.

19.10 INTEGRATED PERIPHERALS

This part of the setup sets Integrated Peripherals options.

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP default values provide optimum performance settings for all devices and system features.

TABLE 19-7: Integrated Peripherals

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
IDE HDD Block Mode	Disabled	Enabled	Enabled, Disabled	Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.
IDE Primary/Secondary Master/Slave PIO	Auto	Auto	Mode 0, Mode 1, Mode 2, Mode 3, Mode 4, Auto	These options only appear if the On-Chip Primary/Secondary PCI IDE options are enabled. The four IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance and speed. In Auto mode, the system automatically determines the best mode for each device. If you select a mode that the drive does not support, it may not work, so choose a lesser value or Auto to see the best mode for the drive.

TABLE 19-7: Integrated Peripherals (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
IDE Primary/Secondary Master/Slave UDMA	Disabled	Auto	Auto, Disabled	Ultra DMA/33 implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If your hard drive and your system software both support Ultra DMA/33, select Auto to enable BIOS support.
On-Chip Primary/Secondary PCI IDE	Enabled	Enabled	Enabled, Disabled	The integrated peripheral controller contains an IDE interface with support for two IDE channels. Select Enabled to activate each channel separately.
Onboard PCI SCSI Chip	Enabled	Enabled	Enabled, Disabled`	Enables/disables the onboard SCSI controller
Ethernet Controller	Enabled	Enabled	Enabled, Disabled	Enables/disables the onboard Ethernet controller.
USB Keyboard Support	Disabled	Disabled	Enabled, Disabled	Select Enabled, if your system contains an Universal Serial Bus (USB) controller and you have an USB keyboard. **Note: This option is for DOS and BIOS support only (Win95 has its own drivers).**
Onboard FDC Controller	Enabled	Enabled	Enabled, Disabled	Select Enabled if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install an add-in FDC or the system has no floppy drive, select Disabled in this field.
Onboard Serial Port 1/2	Auto	Auto	Disabled, 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3, Auto	Select a COM port address and IRQ# for the first and second serial ports.
Serial Port 2 Mode	RS-232	RS-232	RS-232, RS-422, RS-485	Select the operation mode for Serial Port 2.
VT100 Mode on Serial Port 1 or 2	1	1	1, 2	Selects the communication port for VT100 mode: Serial Port 1 or 2.

TABLE 19-7: Integrated Peripherals (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Onboard Parallel Port	378/IRQ7	378/IRQ7	Disabled, 3BC/IRQ7, 378/IRQ7, 278/IRQ5,	Select a LPT address and IRQ# for the physical parallel (printer) port.
Parallel Port Mode	ECP+EPP1.9	ECP+EPP1.9	SPP, EPP1.9+SPP, ECP, ECP+EPP1.9, Normal, EPP1.7+SPP, ECP+EPP1.7	Select an operating mode for the onboard parallel port. Select ECP or EPP unless you are certain both your hardware and software does not support ECP or EPP mode. Parallel port modes are defined in section 14.2.2.
ECP Mode Use DMA	3	3	1, 3	Select a DMA channel for the port.

20. CONFIGURING SCSI WITH SCSISELECT

The Adaptec SCSISelect Configuration Utility allows you to configure or view the SCSI host adapter settings. It also allows you to run SCSI disk utilities, such as a low-level disk format. The various menus and options of the SCSISelect Configuration Utility program are described in this Section.

The Adaptec SCSISelect Configuration Utility is a DOS program available on the LAN Boot & SCSI Utility 2 diskette (file name 7880cfg.exe).

See Section 11.3 for installing and connecting SCSI devices on the PCI-941. Also, follow the installation instructions provided with your SCSI peripheral device to install it in the host.

NOTE

You should not "install" your SCSI hard disk type in the AWARD Setup (only your IDE hard disk).

NOTE

Each device being installed must be assigned a unique identifier called a SCSI Target ID (this is done by jumper on the device or through the SCSISelect Configuration Utility when supported). SCSI peripherals that support the SCAM protocol can have SCSI IDs automatically assigned to them, if the Plug and Play SCAM Support option in the SCSISelect's Advanced Configuration Options is set to Enabled.

20.1 SCSISELECT FIRST SCREEN

Run the SCSISelect program by typing 7880cfg.exe at the DOS prompt. The first screen appears as follow:

Two options are available from this screen:

- **Configure/View Host Adapter Settings:** This option allows configuring and viewing host adapter settings. The default settings are indicated with an asterisk (*) in the pop-up windows: These settings are appropriate for most systems. This option is described in section 20.2.
- **SCSI Disk Utilities:** This option includes low level formatting of SCSI hard disks and verifying disk media. This option is described in section 20.3.

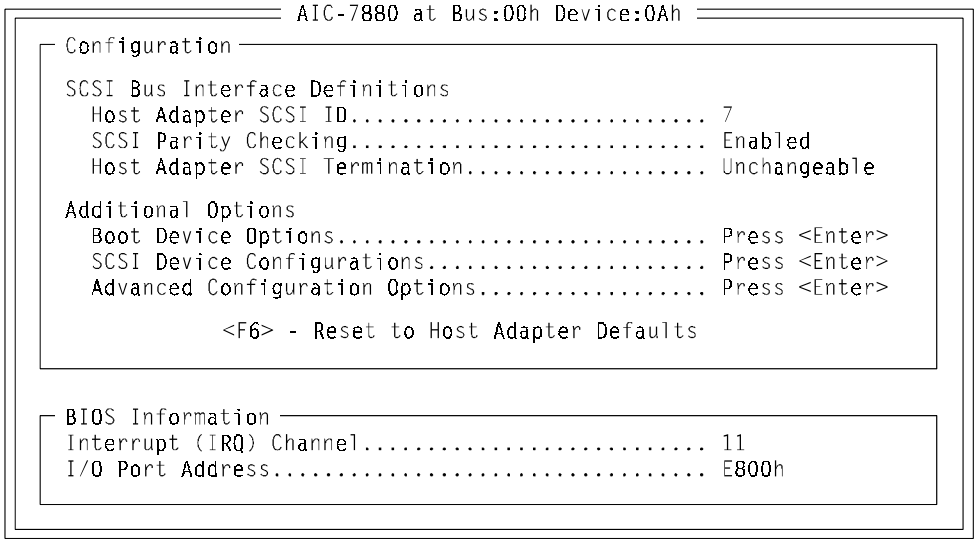
NOTE

Depending on the W18 SCSI Mode jumper (shorted = 16-bit or open = 8-bit), the number of SCSI devices appearing on the screens will vary. The 16-bit mode allows 16 SCSI ID numbers between 0 and 15 (7 is the host adapter, with the highest priority; the priorityof the remaining IDs, in descending order, is 6 to 0, 15 to 8). The 8-bit mode allows 8 SCSI ID numbers between 0 and 7 (7 is the host adapter; the priorityof the remaining IDs, in descending order, is 6 to 0).

Please note that the following sections will show only the 16-bit screens with their default settings. However, in the description of the options, we will indicate any differences with the 8-bit screens.

20.2 CONFIGURE / VIEW HOST ADAPTER SETTINGS

When you select the Configure/View Host Adapter Settings option from the first screen, this window appears:



The window is devided in two boxes, Configuration and BIOS Information. The Configuration box includes options that may be modified. The BIOS Information box include options for viewing only (Interrupt (IRQ) Channel and I/O Port Address).

Configuration options will be described in this section.

SCSI Bus Interface Definitions

- **Host Adapter SCSI ID:** Sets the SCSI ID for the PCI-941 SCSI interface. The SCSI interface is set at 7, which gives it the highest priority on the SCSI bus. We recommend you do not change this setting.
- **SCSI Parity Checking:** When set to Enabled, verifies the accuracy of data transfer on the SCSI bus. Leave this setting enabled unless any SCSI peripheral connected to the PCI-941 SCSI interface does not support SCSI parity.
- **Host Adapter SCSI Termination:** This option cannot be changed when the W2 jumper is installed. See section 11.3 for more information on enabling or disabling SCSI termination for the PCI-941 board.

Additional Options

- **Boot Device Options:** Press the ENTER key for the Boot Device Configuration pop-up window.

```
Boot Device Configuration
Select SCSI peripheral from which to boot.
To view peripheral by ID# select "SCSI Disk Utilities" from previous menu.
Boot SCSI ID..................................................... 0

Option Listed Below Has NO EFFECT if MULTI LUN Support is Disabled
Boot LUN Number.................................................. 0
```

  - **Boot SCSI ID:** Specifies the SCSI ID of your boot device.
  - **Boot LUN number:** Specifies which LUN (Logical Unit Numbers) to boot from on your boot device. Multiple LUN Support must be enabled (see Advanced Configuration Options).

- **SCSI Device Configurations:** Press the ENTER key for the SCSI Device Configuration pop-up window.

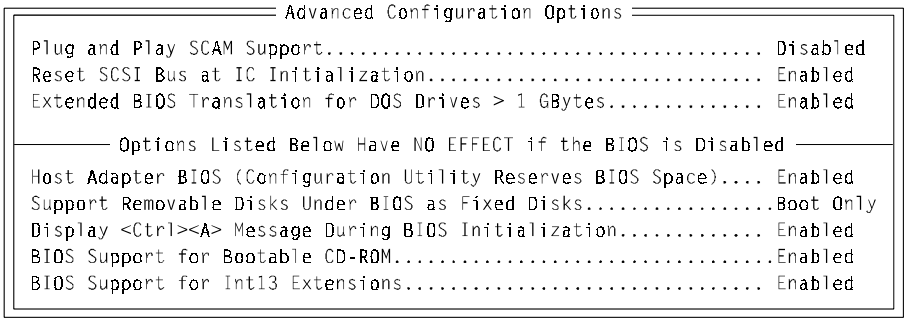
```
SCSI Device Configuration
SCSI Device ID#                  #0   #1   #2   #3   #4   #5   #6   #7
Initiate Sync Negotiation.....   yes  yes  yes  yes  yes  yes  yes  yes
Maximum Sync Transfer Rate....   40.0 40.0 40.0 40.0 40.0 40.0 40.0 40.0
Enable Disconnection..........   yes  yes  yes  yes  yes  yes  yes  yes
Initiate Wide Negotiation.....   yes  yes  yes  yes  yes  yes  yes  yes
Options Listed Below Have NO EFFECT if the BIOS is Disabled
Send Start Unit Command.......   no   no   no   no   no   no   no   no
BIOS Multiple LUN Support.....   no   no   no   no   no   no   no   no
Include in BIOS Scan..........   yes  yes  yes  yes  yes  yes  yes  yes

SCSI Device ID#                  #8   #9   #10  #11  #12  #13  #14  #15
Initiate Sync Negotiation.....   yes  yes  yes  yes  yes  yes  yes  yes
Maximum Sync Transfer Rate....   40.0 40.0 40.0 40.0 40.0 40.0 40.0 40.0
Enable Disconnection..........   yes  yes  yes  yes  yes  yes  yes  yes
Initiate Wide Negotiation.....   yes  yes  yes  yes  yes  yes  yes  yes
Options Listed Below Have NO EFFECT if the BIOS is Disabled
Send Start Unit Command.......   no   no   no   no   no   no   no   no
BIOS Multiple LUN Support.....   no   no   no   no   no   no   no   no
Include in BIOS Scan..........   yes  yes  yes  yes  yes  yes  yes  yes
```

  - **Initiate Sync Negotiation:** When set to Yes, initiates synchronous data transfer negotiation (Sync Negotiation) between the peripheral and SCSI interface. Leave this setting to Yes unless any attached SCSI peripheral connected to the SCSI interface does not support synchronous negotiation.

- **Maximum Sync Transfer Rate:** Determines the maximum synchronous data transfer rate the SCSI interface supports. The default maximum value for Wide-Ultra 16-bit is 40.0 (W18 jumper shorted). If your peripheral is not Wide, select a transfer rate of 20.0 (when W18 jumper is open, 20 is the maximum default).
- **Enable Disconnection:** When set to Yes, allows the SCSI peripheral to disconnect from the SCSI bus. Leave the setting at Yes if two or more SCSI peripherals are connected to the SCSI interface. If only one SCSI peripheral is connected, changing the setting to No results in slightly better performance.
- **Initiate Wide Negotiation:** This option does not appear if the W18 SCSI Mode jumper is set to 8-bit (jumper open). When set to Yes, the SCSI interface attempts 16-bit data transfer (wide negotiation). When set to No, the SCSI interface uses 8-bit data transfer unless the SCSI peripheral requests wide negotiation.
- **Send Start Unit Command:** When set to Yes, sends the Start Unit Command to the SCSI peripheral at bootup.
- **BIOS Multiple LUN Support:** When set to Yes, the SCSI BIOS provides boot support for a SCSI peripheral with multiple LUNs. Leave this setting to No if your boot device does not have multiple LUNs.
- **Include in BIOS Scan:** When set to Yes, the SCSI BIOS includes the peripheral as part of its BIOS scan at bootup.

▪ **Advanced Configuration Options:** Press the ENTER key for the Advanced Configuration Options pop-up window.



- **Plug-and-Play SCAM Support:** When set Enabled, the SCSI interface automatically assigns SCSI IDs to SCSI peripherals that support the SCAM protocol. The default is Disabled, but you can set it to Enabled even if you have a non-SCAM peripheral.
- **Reset SCSI Bus at IC Initialization:** When set to Enabled, the SCSI interface generates a SCSI bus reset during its power-on initialization and after a hard reset.

- **Extended BIOS Translation for DOS Drives > 1 GByte**: When set to Enabled, provides an extended translation scheme for SCSI hard disks with capacities greater than 1 GByte. This setting is necessary only for MS-DOS 5.0 or above; it is not required for other operating systems, such as NetWare or UNIX. The extended translation scheme supports disk drives as large as 8 GBytes.

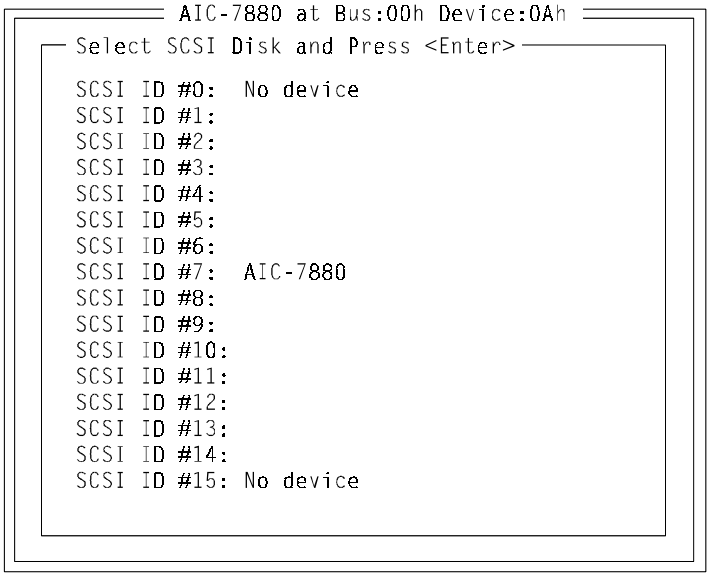
  To partition a disk larger than 1 GByte controlled by the SCSI card BIOS, use the MS-DOS Fdisk command.

  CAUTION: Back up your disk drives before changing the translation scheme.
- **Host Adapter BIOS (Configuration Utility Reserves BIOS Space):** Enables or disables the SCSI interface BIOS. Set to Enabled, if you boot from a SCSI disk drive connected to the SCSI interface. Set to Disabled if the peripherals on the SCSI bus (for example, CD-ROM drives) are controlled by software drivers and do not need the BIOS.
- **Support Removable Disks Under BIOS as Fixed Disks:** Determines which removable-media drives are supported by the SCSI card BIOS. Choices are as follows: **Boot Only** - Only the removable-media drive designated as the boot device is treated as a hard disk drive. **All Disks** - All removable-media drives supported by the BIOS are treated as hard disk drives. **Disabled** - No removable-media drives are treated as hard disk drives. Software drivers are required because the drives are not controlled by the BIOS.

  CAUTION: Do not remove a removable-media cartridge from a SCSI drive controlled by the SCSI card BIOS while the drive is on. You may lose data. To allow removability of the media while the drive is on, install the removable-media software driver and set Support Removable Disks Under BIOS as Fixed Disks to Disabled.
- **Display <Ctrl> <A> Messages during BIOS Initialization:** The settings do nothing on the PCI-941, since the program is not part of the BIOS, but invoked as a DOS utility.
- **BIOS Support for Bootable CD-ROMs:** When set to Enabled, the SCSI BIOS allows booting from a CD-ROM drive.
- **BIOS Support for Int 13 Extensions:** When set to Enabled, the SCSI BIOS supports Int 13h extensions as required by Plug-and-Play. The setting can be either enabled or disabled if your system is not Plug-and-Play.

20.3 SCSI DISK UTILITIES

Once the SCSI Disk Utilities option is selected from the SCSISelect's first screen, the program scans the SCSI bus to determine the devices installed and displays a list of all SCSI IDs and the devices assigned to each ID, as follows:



Use the ↓ and ↑ keys to move the cursor to a specific ID and device, then press ENTER. A small pop-up window appears, displaying these options:

- **Format Disk:** Allows you to perform a low-level format on a hard disk drive. Most SCSI disk devices are preformatted at the factory and do not need to be formatted again. Each hard disk drive must be low-level formatted before you can use your operating system's partitioning and file preparation utilities, such as MS-DOS Fdisk and Format.

  CAUTION: A low-level format destroys all data on the drive. Be sure to back up your data before performing this operation. You cannot abort a low-level format once it is started.

- **Verify Disk Media:** Allows you to scan the media of a hard disk drive for defects. If the utility finds bad blocks on the media, it prompts you to reassign them; if you select yes, those blocks are no longer used. You can press Esc at any time to abort the utility.

21. INSTALLING DRIVERS

21.1 SCSI DRIVERS

The EZ-SCSI software available on the SCSI Utility Disk 1 allows you to install the appropriate driver for your specific operating system.

21.2 VIDEO DRIVERS

The Video Controller has specific video drivers for various operating systems and software. To install these drivers, you must use the Utility Disk containing the video drivers for your operating system. With the Utility Disk in your floppy drive, run the installation program found on the diskette (e.g., SETUP or INSTALL).

21.3 ETHERNET DRIVERS

The Ethernet controller has specific drivers for various operating systems and software. To install these drivers, you must use the Utility Disk containing the Ethernet drivers for your operating system. With the Utility Disk in your floppy drive, run the installation program found on the diskette (e.g., SETUP or INSTALL).

NOTE

To install drivers for Ethernet, you can also follow the procedure given in the README.BAT file on the Ethernet Utility Disk.

The Ethernet controller on the PCI-941 resides on the PCI bus and is therefore Plug and Play by default. No manual configuration is required.

Once the proper Ethernet driver is installed, the onboard Plug and Play BIOS and the driver automatically allocate resources for the Ethernet device.

21.4 CHIPSET DRIVER FOR WINDOWS 95

The required Windows 95 driver for the PIIX4 chipset is on the PIIX4 Driver utility diskette.

21.5 OTHER DRIVERS

NOTE

For other operating system drivers and installation instructions, or for more information, contact TEKNOR's Technical Support department.

22. UPDATING OR RESTORING BIOS IN FLASH

22.1 USING THE UBIOS UTILITY TO UPDATE BIOS

22.1.1 INTRODUCTION

UBIOS 3.0 is a utility that allows you to take BIOS files from a disk and update the Flash BIOS device with them.

It also allows BIOS files in the Flash BIOS device to be saved to disk.

The program can be executed in one of two modes:

- Interactive Mode: In this mode the program is menu-driven. This mode is explained in section 22.1.2.
- Batch Mode: It is also possible to run the program without menus by a command which specifies the selected options and files with parameters. This mode is explained in section 22.1.3.

NOTE

Using UBIOS, will clear the CMOS Setup in ROM. Therefore, it is recommended that you take note of your Setup parameters (especially Hard Disk parameters), so you can reset them afterwards.

NOTE

To update BIOS files, these files must be in the same directory as the UBIOS.EXE program. Therefore, prior to running the program, make sure the files you wish to update and the UBIOS program file are in the same directory.

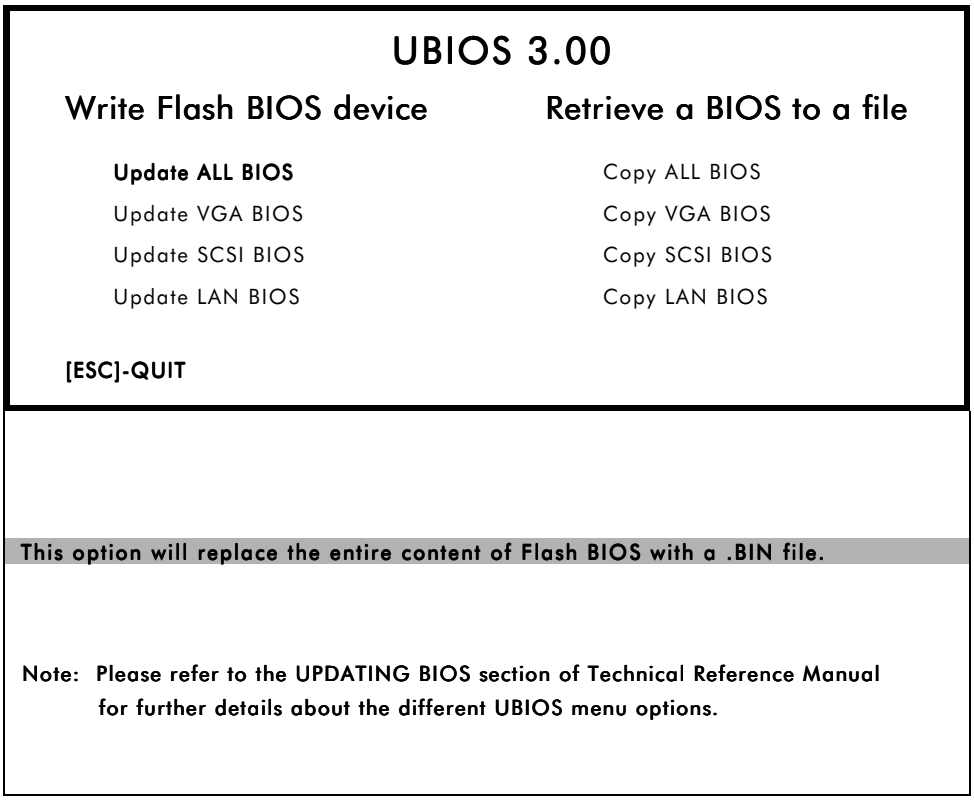
When you enter UBIOS, only the current directories are available. Within the UBIOS program, you can change the drive, but not the directory.

22.1.2 UBIOS - INTERACTIVE MODE

To run the program in interactive mode, type "UBIOS" from the DOS prompt and the UBIOS 3.0 presentation screen will be displayed. To continue, hit any key on the keyboard. This brings you to the main menu.

22.1.2.1 Main Menu

The main menu appears below:



The main menu displays two groups of options: Write Flash BIOS device and Retrieve a BIOS to a file. The first group allows you to update the Flash BIOS device with a BIOS file stored on disk. The second group allows you to copy the contents of the Flash BIOS device to files on disk.

In the above menu, the option **Update ALL BIOS** is highlighted and the option is described in the shaded row below. Move the arrow keys to highlight other options.

To select the highlighted option, press ENTER.

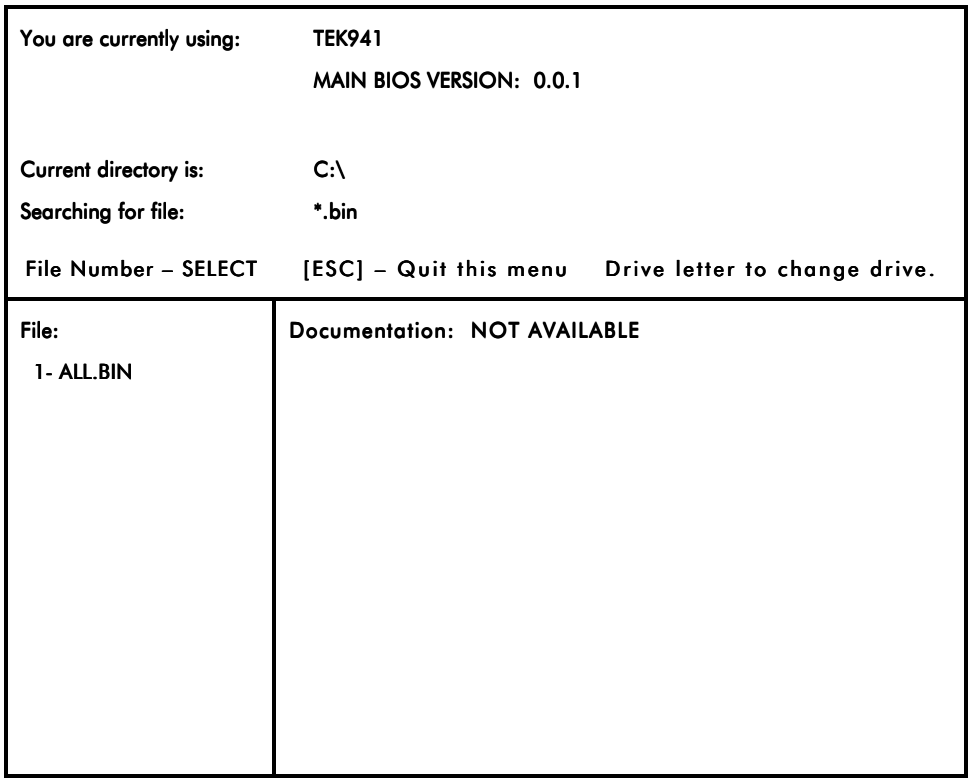
To exit the program, press the ESC key when you are in the main menu.

There are four types of BIOS files which appear on the main menu:

- **ALL BIOS File:** This file combines all BIOS files contained in the Flash BIOS device in a single file. It has the .BIN extension.
- **VGA BIOS File:** This file contains the VGA BIOS section of the Flash BIOS. There are two possible types of VGA BIOS files: files with the .VGA extension (supports CRT displays only) and files with the .BFP extension (supports CRT and Flat Panel displays).
- **SCSI BIOS File:** This file contains the SCSI BIOS section of the Flash BIOS. It has the .BIN extension.
- **LAN BIOS File:** This file contains the LAN BIOS section of the Flash BIOS. It has the .BIN extension.

22.1.2.2 Updating Flash BIOS

If you select one of the **Update** options from the main menu, a screen similar to the following is displayed:



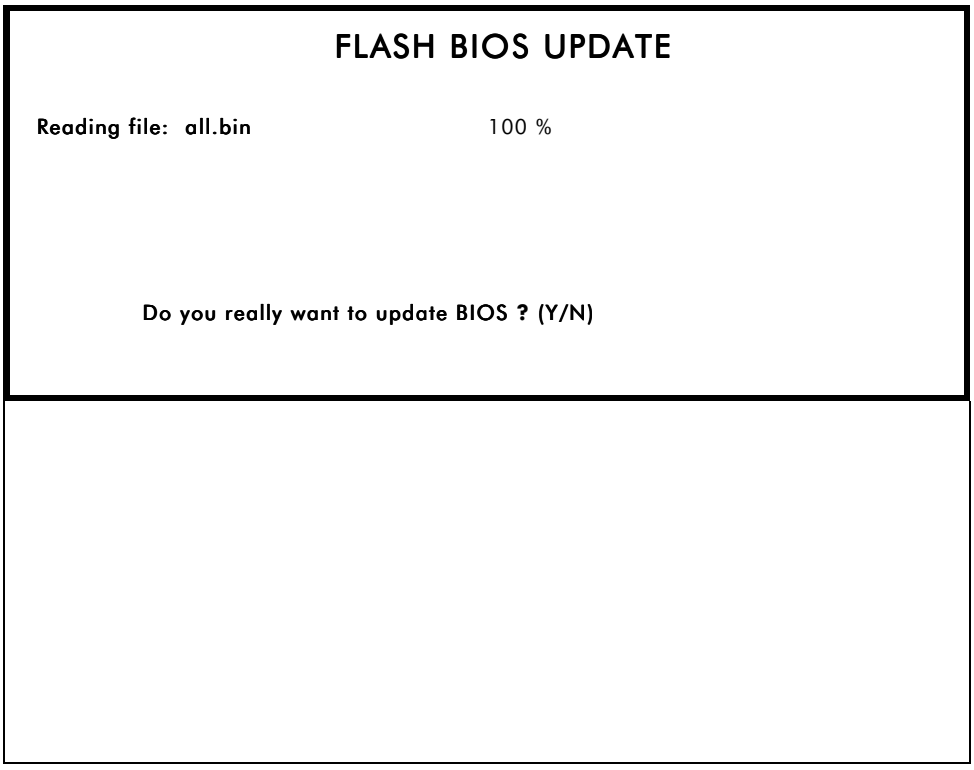
Files of the type you selected in the main menu and which are in the current directory are displayed in the **File** window.

To change directory, type the drive letter. If there are any files of the type you selected in this directory, they will be displayed in the **File** window.

The **Documentation** window displays “NOT AVAILABLE”. It will be used in the future for displaying the contents of a .doc file.

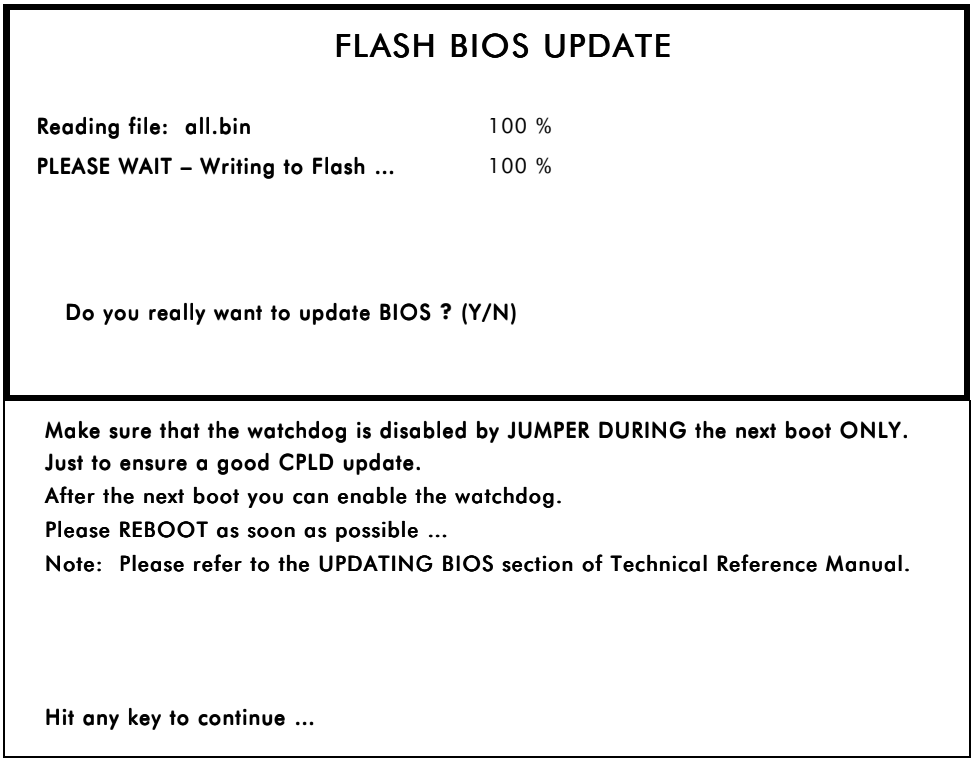
If you want to return to the previous menu, press the ESC key.

To select a file from the **File** window, in order to update the Flash BIOS with this file, type the file number which appears before the filename in the list. A new screen is displayed as shown below. This is the Flash BIOS Update screen. You must first confirm if you want to update the Flash BIOS with the selected file (the filename appears next to **Reading file)**, by typing "Y" for Yes, "N" for No.



If you choose to update the file, by typing "Y", the program will write the file to Flash. The progress of the operation is indicated in percentage completed, next to **PLEASE WAIT – Writing to Flash …**

When the update is over the screen will appear as follow:



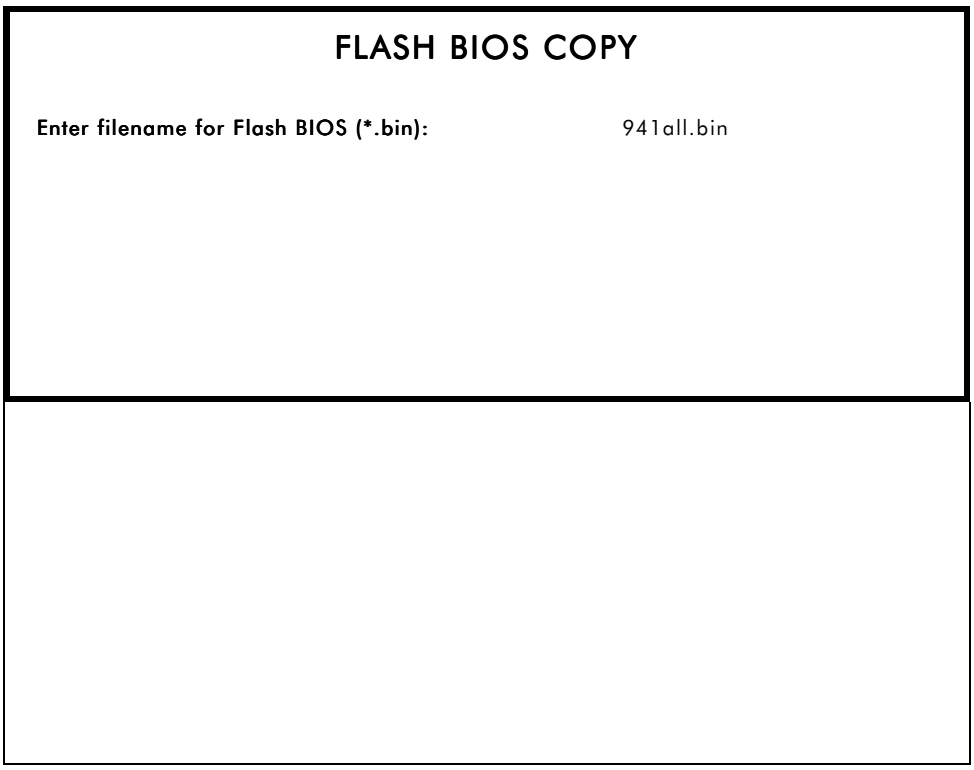
To return to the main menu, hit any key on the keyboard.

NOTE

There may be slight changes to the Flash BIOS Update screen compared to those shown here for an Update ALL BIOS operation. Also, if an error occurs, these will be indicated on the screen.

22.1.2.3 Copying Flash BIOS

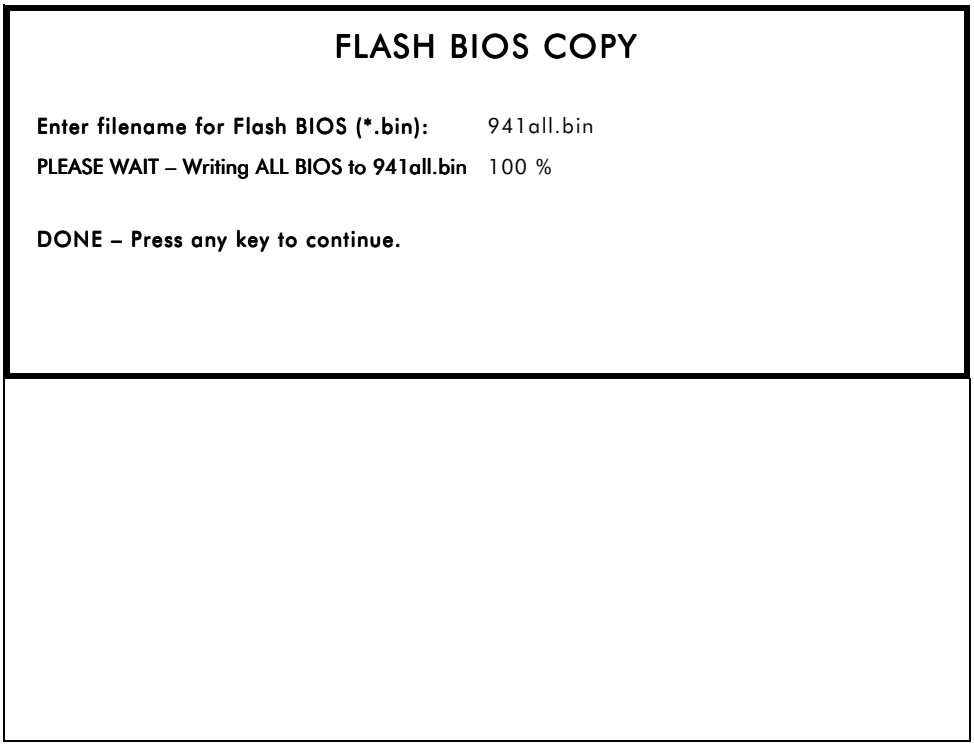
If you select one of the **Copy** options from the main menu, a screen similar to the following is displayed:



You begin a Flash Copy operation, by typing a filename (including the extension) for the file you are creating. You must use the same extension as the one indicated in parentheses on the screen. In the above example, the filename entered was “941all.bin”.

Press ENTER to proceed.

The progress of the operation will display on the screen in percentage completed. The example shown on the following page is for the Copy ALL BIOS option.



If the filename entered for the BIOS file already exists, the following message will appear on the screen:

File already exits! Overwrite? (Y/N)

If you choose to overwrite the existing file, its content will be lost.

To return to the main menu, hit any key on the keyboard.

NOTE

There may be slight changes to the Flash BIOS Copy screen compared to those shown here for an Copy ALL BIOS operation. Also, if an error occurs, these will be indicated on the screen.

22.1.3 UBIOS – BATCH MODE

While files can be manually selected using the Interactive Mode, Flash BIOS Update or Copy can be achieved through Batch Mode.

The command line format is as follows:

UBIOS -B [operation] [filetype] [filename] [options] where:

-B specifies that this is a Batch Mode command.

[operation] is the Flash BIOS operation you wish to perform, and can be replaced with one of three letters:
- U for Update,
- C for Copy, or
- V for Verify (used to compare the contents of the Flash BIOS device and the specified BIOS file).

[filetype] is the filetype of the BIOS file to program (with an update operation) or to create (with a copy operation), and can be replaced with one of the following:

ALL	for All BIOS files in a single file with the .BIN extension,
VGA	for VGA BIOS file with the .VGA or .BFP extension,
SCSI	for SCSI BIOS file with the .BIN extension,
LAN	for LAN BIOS file with the .BIN extension.

[filename] is the name of the BIOS file (including the extension) to program (with an update operation) or to create (with a copy operation), and can be replaced with the filename which corresponds to the filetype. For example, if "VGA" was listed as filetype, then the filename could be "FLAT.BFP".

[options] these are optional parameters that may be added:

/C This option will not clear the CMOS Setup when updating main BIOS (AMIBIOS), however this is not recommended since the CMOS Setup should be updated when the main BIOS is changed.

/R Instructs UBIOS to reset the board upon completion of an operation.

/? To get a summary of the Batch Mode options from UBIOS. It will display a Batch options summary of valid UBIOS command lines. The same help information will also be displayed each time UBIOS detects an error in the command line.

22.2 AUTOMATIC CPLD HARDWARE UPGRADE AFTER A BIOS UPDATE

During the first system bootup after you update the Flash BIOS device with the UBIOS utility, the BIOS may need to upgrade the CPLD devices.

This message appears on the screen when the BIOS writes to the devices:

```
A hardware upgrade will be performed on some CPLDs. Follow the instructions
below with special care. Do not disturb the process.

DO NOT RESET OR POWER DOWN THE BOARD!!!

   □□□ Device 1 □□□   0% □□□□□□□□□□□□□□□□□□□□ 100%
   □□□ Device 2 □□□   0% □□□□□□□□□□□□□□□□□□□□ 100%

Status :
         Please wait...
```

The color of the boxes displayed in the message indicates these functions:

Device OK	Green
Device busy	Blue
Device will be updated	Red

If your device upgrade was successful, the following message is displayed under the "Status:" line prior to rebooting:

```
Update complete successfully, wait for the automatic reboot.
Rebooting in 5 second(s).
```

If the update is not successful, the following message appears under the "Status:" line:

```
ERROR: general failure programming CPLDs!
Please contact Teknor Industrial Computers technical support.
```

You must contact TEKNOR's technical support for further instructions.

WARNING

Whenever the BIOS performs a CPLD hardware upgrade, **disable the watchdog (by removing the W7 jumper) and do not interrupt the system in any way (power down, reset, mouse or keyboard functions). The devices will be damaged and your board rendered inoperational if you disturb the update process!**

23. VT100 MODE

The PCI-941 utilizes a feature known as VT100 mode. This mode enables your single board computer to run without a local keyboard or screen. That is, operation can be controlled via a remote terminal supporting VT100 mode or a computer with a terminal emulation program (for example, Telix, Procomm).

NOTE

With the PCI-941 running in VT100 mode, the user can access the BIOS Setup program on his terminal.

23.1 VT100 REQUIREMENTS

The terminal you are using should emulate a VT100 or ANSI terminal. Although this is not an absolute requirement, strange characters may appear on screen if it does not. This occurs because the VT100 recognizes these control characters, and causes them to perform a specific function, for example, screen erase, cursor position, and so on.

23.2 VT100 SETUP & CONFIGURATION

Follow these steps for setting up VT100 Mode:

- Power on your PCI-941 and run the AWARD Setup program by hitting the DELETE key, before or when you see the message "Press DEL To Enter SETUP" at the top of the screen. On the Integrated Peripherals screen, set the "VT100 Mode Serial Port 1 or 2" option to the desired communication port (1 or 2). VT100 mode runs on Serial Port 1 or Serial Port 2.
- Power off your PCI-941 and install jumper W3 (5-6) to enable VT100 Mode.
- Connect the communications cable as shown in Diagram 23-1. Note: If you do not require a full cable for your terminal, you can set up a partial cable by using only the TXD and RXD lines. The control lines can be ignored by looping them back as shown in Diagram 23-2.
- The BIOS Setup will automatically detect the user terminal speed and set the communication port speed likewise. These speeds are supported: 2400, 9600, 19200, 38400, 57600 and 115200 baud. If the terminal is set at another speed or if it is powered off, the BIOS Setup sets the port at 115200 by default.
- You must respect this protocol:
  8 Bits
  No Parity
  1 Stop Bit
  Echo Off.

  If you are running a terminal emulation program, these parameters must be set in it.

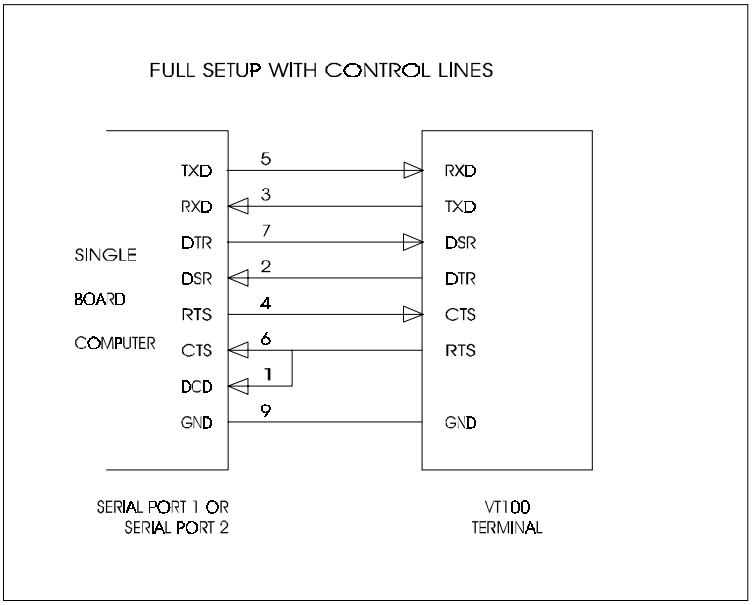
23.3 RUNNING WITHOUT A TERMINAL

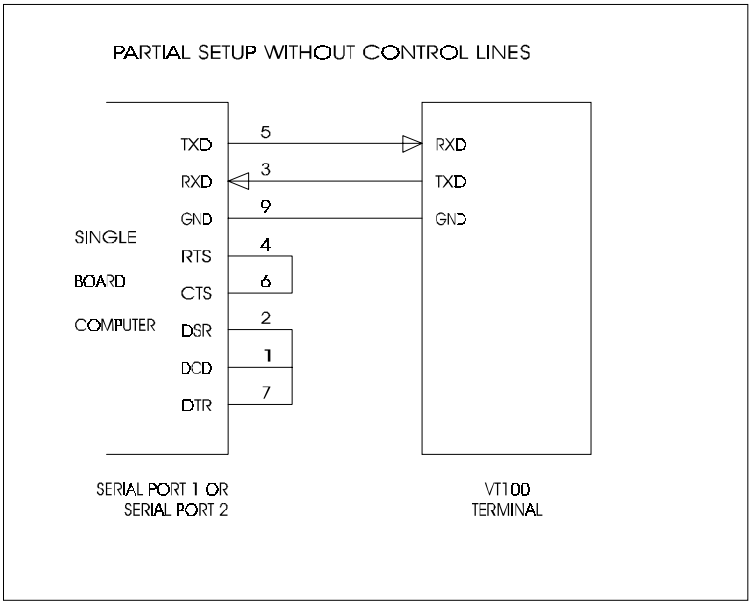
The PCI-941 can boot up without a screen or terminal attached. Wiring the system according to Diagram 23-2 allows the lines to remain active. This does not apply if the VT100 jumper is not set.

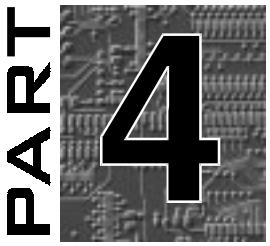
Furthermore, you can run without any console at all by simply not enabling VT100 Mode and by disabling the video interface.

DIAGRAM 23-1: VT100 Full Setup

DIAGRAM 23-2: VT100 Partial Setup







APPENDIXES

A. BOARD SPECIFICATIONS

B. BOARD DIAGRAMS

C. CONNECTOR LOCATION & PINOUTS

D. LIST OF APPROVED VENDORS

E. I/O MAP

F. MEMORY MAP

G. IRQ LINES

H. DMA CHANNELS

I. BIOS SETUP ERROR CODES

J. EMERGENCY PROCEDURE

A. BOARD SPECIFICATIONS

A.1 ELECTRICAL

- Conforms to the electrical specifications in the IEEE P996 Bus Specification (PC/AT) and the PCI Local Bus Specification Revision 2.1.
- Power Requirements*:

Power Management Mode	Mobile Pentium II 233MHz	Mobile Pentium II 266MHz	Mobile Pentium II 300MHz
Normal Mode	3.50A	3.67A	3.72A
Doze Mode	3.36A	3.50A	3.45A
Standby Mode	3.34A	3.48A	3.38A
Suspend Mode	2.28A	2.30A	2.28A

* Measured with 16MB SDRAM, Ethernet, video, SCSI, keyboard, floppy and hard disk.

A.2 MECHANICAL

- Please refer to Mechanical Specifications in Appendix B.3.
- Dimensions: 13.33 in. x 4.80 in. / 338.5 mm x 121.9 mm.

A.3 ENVIRONMENTAL

- Operating Temperature: 0 to 60°C (heatsink and fan), calculated with typical power consumption.
- Storage Temperature: Ambient temperature range of -40°C to +70°C.
- Maximum Noncondensing Relative Humidity: 95%.
- Altitude: 15 000 feet / 4.572 m. (operating); 50 000 feet / 5.240 m (storage, transit).
- Shock: 5G, each axis.
- Vibration: 1.5G, each axis.

A.4 RELIABILITY

- Reliability Prediction PCI-941 (MTBF):

Processor	Configuration Basic Board | Flash Memory Module | Video Option			MTBF (Hours)	Failure Rate ($x10^{-6}$)
Mobile Pentium II 233MHz	✓			102 062	9.7980
	✓	✓		101 828	9.8205
	✓		✓	85 082	11.7534
	✓	✓	✓	84 920	11.7758
Mobile Pentium II 266MHz	✓			102 062	9.7980
	✓	✓		101 828	9.8205
	✓		✓	85 082	11.7534
	✓	✓	✓	84 920	11.7758
Mobile Pentium II 300MHz	✓			102 062	9.7980
	✓	✓		101 828	9.8205
	✓		✓	85 082	11.7534
	✓	✓	✓	84 920	11.7758

- Designed to meet or exceed:

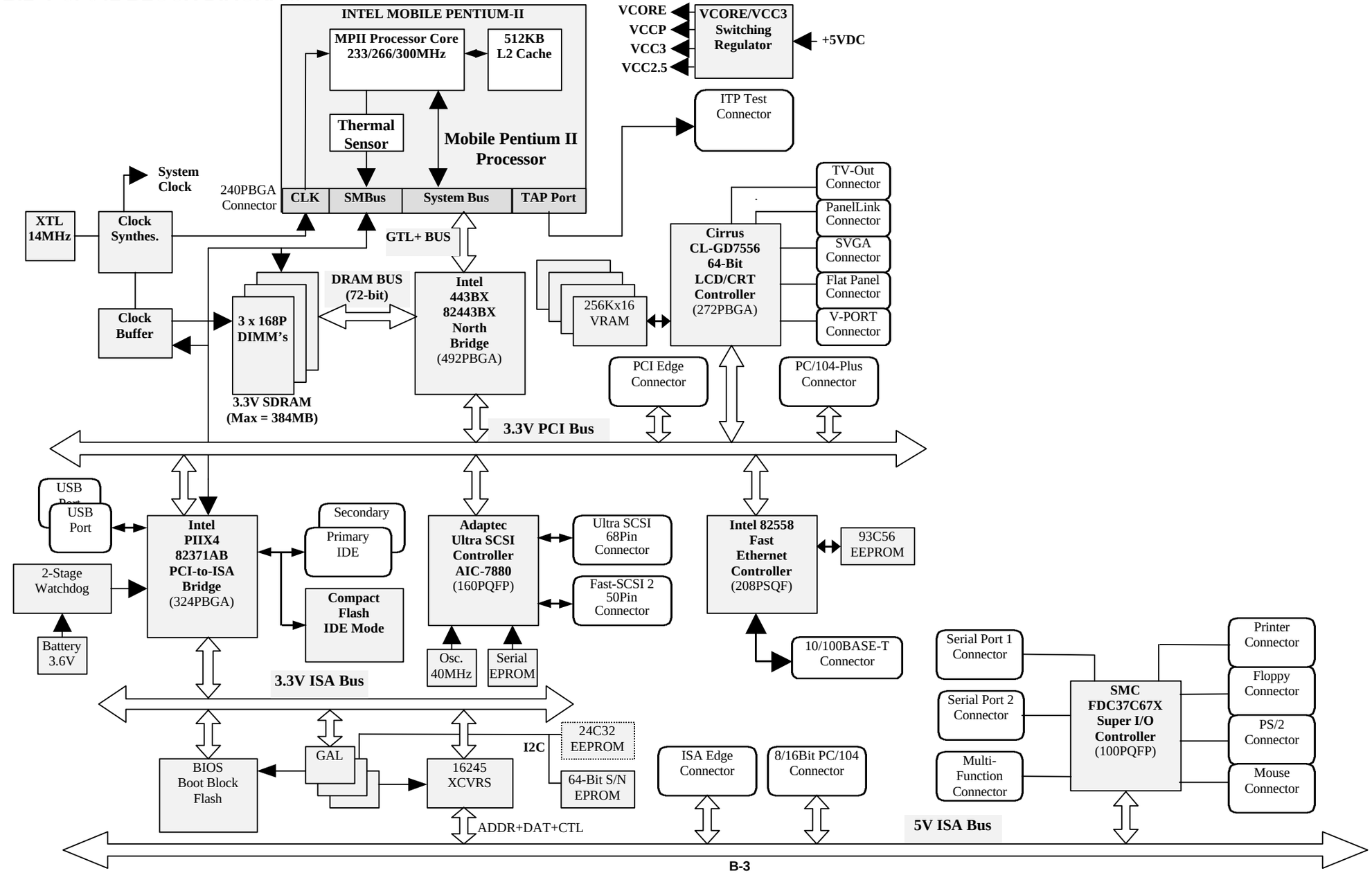
Safety	EMI/EMC
UL 1950	FCC 47 CFR Part 15/CISPR22
CSA C22.2 No 950	CE Mark to EN55022/EN50082
EN 60950	
IEC950	

B. BOARD DIAGRAMS

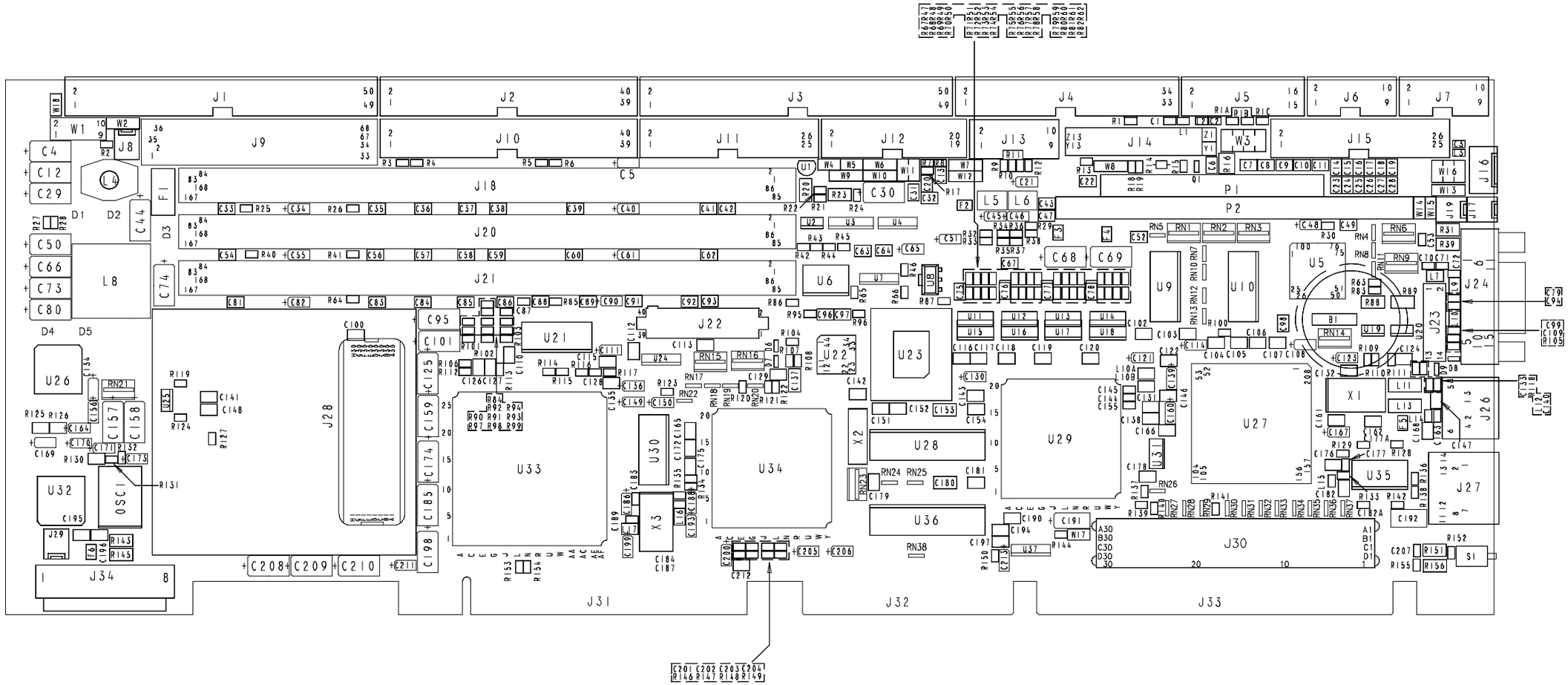
This appendix contains the following board diagrams:

Number	Title
B-1	PCI-941 Block Diagram
B-2	PCI-941 Assembly Diagram (Top)
B-3	PCI-941 Assembly Diagram (Bottom)
B-4	PCI-941 Configuration Diagram
B-5	PCI-941 Mechanical Specifications Diagram

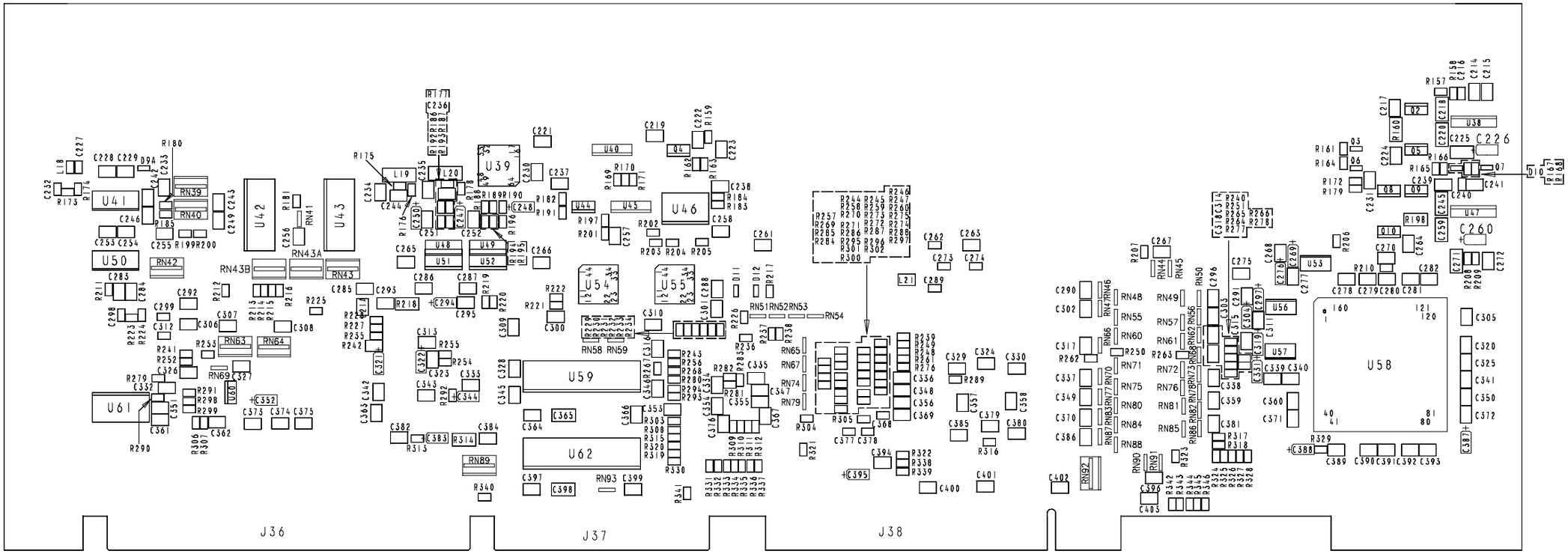
B.1 PCI-941 BLOCK DIAGRAM



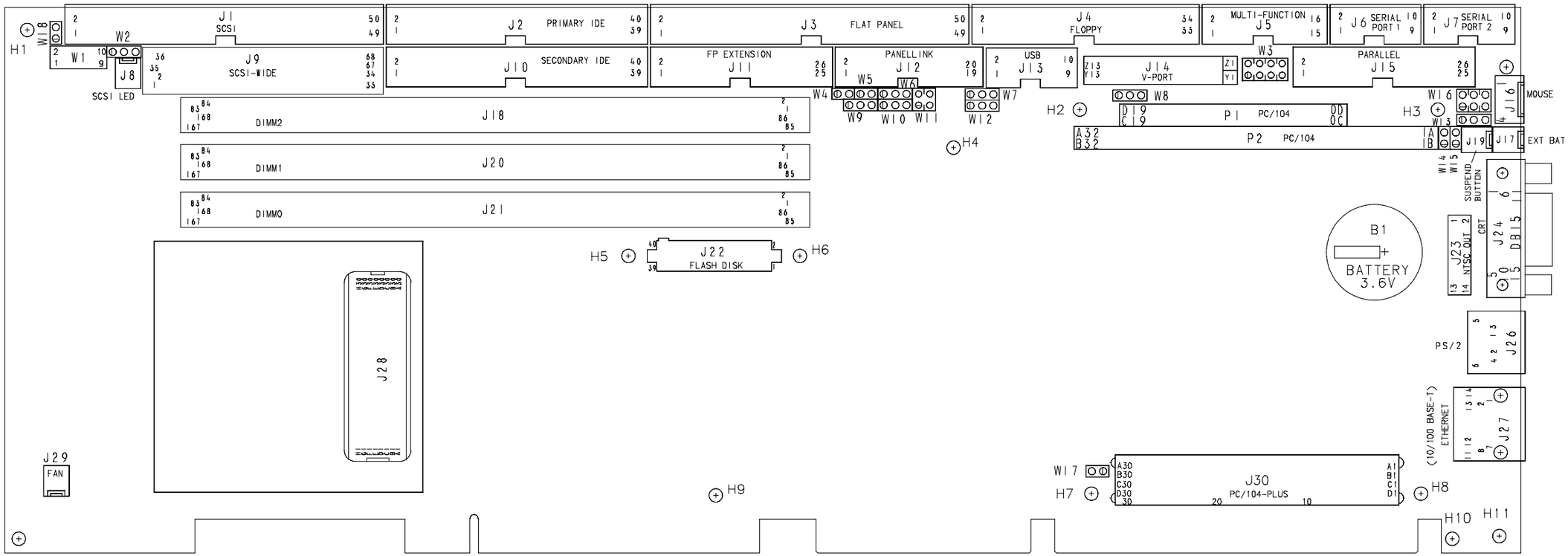
B.2 PCI-941 ASSEMBLY DIAGRAM (TOP)



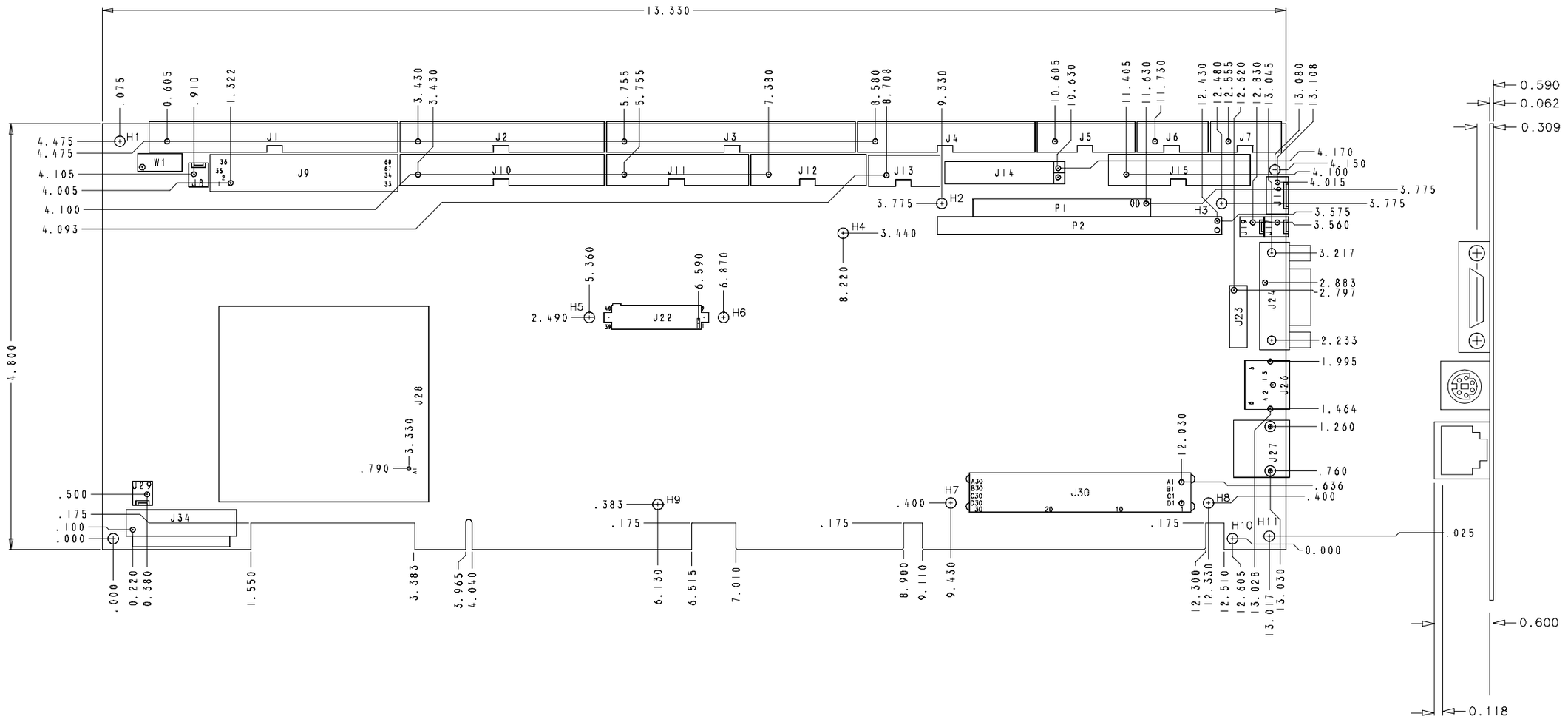
B.3 PCI-941 ASSEMBLY DIAGRAM (BOTTOM)



B.4 PCI-941 CONFIGURATION DIAGRAM



B.5 PCI-941 MECHANICAL SPECIFICATIONS DIAGRAM

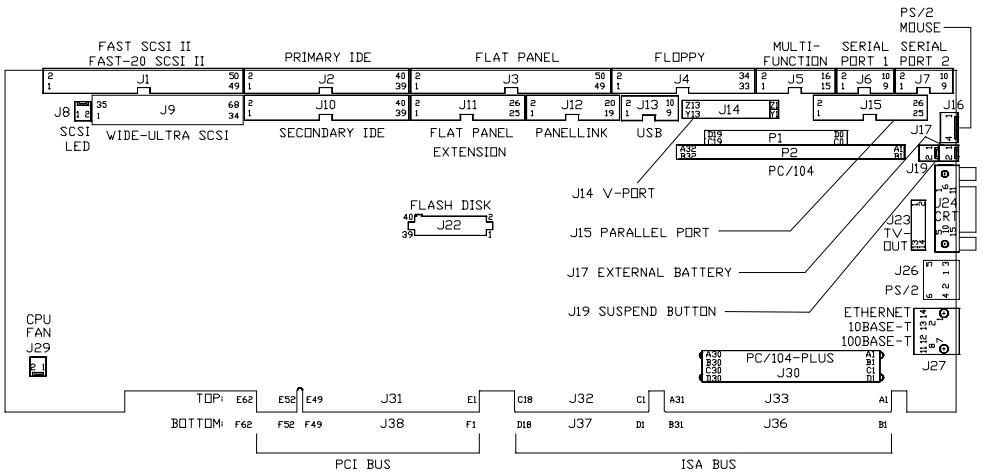


C. CONNECTOR LOCATION & PINOUTS

C.1 LOCATION OF CONNECTORS ON THE PCI-941

Diagram C-1 shows the connector locations on the PCI-941.

DIAGRAM C-1: PCI-941 Connector Locations



C.2 CONNECTOR PINOUTS

TABLE C-1: Fast SCSI Interface Connector (J1) - Pinout

Pin Number	Signal	Pin Number	Signal
1	GND	2	SD0*
3	GND	4	SD1*
5	GND	6	SD2*
7	GND	8	SD3*
9	GND	10	SD4*
11	GND	12	SD5*
13	GND	14	SD6*
15	GND	16	SD7*
17	GND	18	SDP*
19	GND	20	GND
21	GND	22	GND
23	Not Connected	24	GND
25	Not Connected	26	Term Power
27	Not Connected	28	GND
29	GND	30	GND
31	GND	32	SATN*
33	GND	34	GND
35	GND	36	SBSY*
37	GND	38	SACK*
39	GND	40	SRST*
41	GND	42	SMSG*
43	GND	44	SSEL*
45	GND	46	SCD*
47	GND	48	SREQ*
49	GND	50	SIO*

* Active low signal

TABLE C-2: Primary Enhanced IDE Connector (J2) - Pinout

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	RESET*	2	-	GND
3	I/O	DATA 7	4	I/O	DATA 8
5	I/O	DATA 6	6	I/O	DATA 9
7	I/O	DATA 5	8	I/O	DATA 10
9	I/O	DATA 4	10	I/O	DATA 11
11	I/O	DATA 3	12	I/O	DATA 12
13	I/O	DATA 2	14	I/O	DATA 13
15	I/O	DATA 1	16	I/O	DATA 14
17	I/O	DATA 0	18	I/O	DATA 15
19	-	GND	20	-	Not Connected
21	I	DRQ 0	22	-	GND
23	O	IOW*	24	-	GND
25	O	IOR*	26	-	GND
27	I	IORDY	28	O	PRIM. PDI[1]
29	O	DACK 0*	30	-	GND
31	I	IRQ 14	32	-	Not Connected
33	O	ADD 1	34	-	Not Connected
35	O	ADD 0	36	O	ADD 2
37	O	CS 1P*	38	O	CS 3P*
39	I	IDEACTP*	40	-	GND

* Active low signal
[1] 470 ohm pull-down

TABLE C-3: Flat Panel Connector (J3) - Pinout

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	FP2	2	O	FP3
3	O	FP4	4	O	FP5
5	O	FP8	6	O	FP9
7	O	FP10	8	O	FP11
9	O	FP13	10	O	FP12
11	O	FP7	12	O	FP6
13	O	FP17	14	O	FP16
15	O	FP15	16	O	FP14
17	-	GND	18	-	FPVDCK (Shift Clock)
19	-	GND	20	O	FP25
21	-	GND	22	O	LFS (Frame Start)
23	O	FP1	24	O	FP18
25	-	GND	26	O	FPDE (Data Enable)
27	-	GND	28	-	GND
29	O	FP24	30	O	GP0 (Control 0)
31	O	GP1 (Control 1)	32	-	GND
33	O	FPVEE (Enable VEE)	34	-	GND
35	O	LLCLK (Line clock)	36	-	GND
37	O	FPVEE (Enable VEE)	38	-	FPVCC (Enable VCC)
39	O	FP0	40	O	GP2 (Control 2)
41	I	STNDBY*	42	O	FP30
43	O	FP19	44	O	FP31
45	I	ACTI	46	O	FPDECTL
47	-	FPVCC (3.3/5V Select)	48	-	FPVCC (3.3/5V Select)
49	-	+12V	50	-	+12V

* Active low signal

TABLE C-4: Floppy Drive Connector (J4) - Pinout

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	-	GND	2	O	DRV DENS. SEL. 0*
3	-	GND	4	-	Not Connected
5	-	GND	6	-	Not Connected
7	-	GND	8	I	INDEX*
9	-	GND	10	O	MOTOR ON 0,1*
11	-	GND	12	O	DRIVE SELECT B*
13	-	GND	14	O	DRIVE SELECT A*
15	-	GND	16	O	MOTOR ON 2*
17	-	Not Connected	18	O	DIR CONTROL*
19	-	GND	20	O	STEP*
21	-	GND	22	O	WRITE DATA*
23	-	GND	24	O	WRITE ENABLE*
25	-	GND	26	I	TRACK 0*
27	-	Not Connected	28	I	WRITE PROTECT*
29	-	FLOPPY DETECT	30	I	READ DATA*
31	-	GND	32	O	HEAD SELECT*
33	-	Not Connected	34	I	DSKCHG*

* Active low signal

TABLE C-5: Multi-Function Header (J5) - Pinout

Function	Pin Number	Signal Flow			Pin Number	Signal Flow	
	Signal						Signal
AT Keyboard	KBCLK	I/O	1	2	-	GND
	KDATA	I/O	3	4	-	GND
	VCC (+5V)	-	5	6	-	VCC (+5V)
8 Ohm Speaker	SPEAKER	O	7	8	-	VCC (+5V)
	Not Used	-	9	10	-	GND
Suspend Button	PWRBT*	I	11	12	-	GND
Push Button Reset	PBRES*	I	13	14	-	GND
Hard Disk LED	ACTIVE*	O	15	16	-	VCC(+5V)

* Active low signal

TABLE C-6: Serial Port 1 - (J6) RS-232 - Pinout

Pin Number	Signal Flow			Pin Number	Signal Flow	
Signal						Signal
DCD 1*	I	1		2	I	DSR 1*
RXD 1*	I	3		4	O	RTS 1*
TXD 1	O	5		6	I	CTS 1*
DTR 1*	O	7		8	I	RI 1*
GND	-	9		10	-	Not Connected

* Active low signal

TABLE C-7: Serial Port 2 - (J7) RS-232 - Pinout

Pin Number	Signal Flow			Pin Number	Signal Flow	
Signal						Signal
DCD 2*	I	1		2	I	DSR 2*
RXD 2*	I	3		4	O	RTS 2*
TXD 2	O	5		6	I	CTS 2*
DTR 2*	O	7		8	I	RI 2*
GND	-	9		10	-	Not Connected

* Active low signal

TABLE C-8: Serial Port 2 - (J7) RS-422/RS-485 - Pinout

Pin Number				Pin Number		
Signal Flow					Signal Flow	
Signal						Signal
DCD 2*	I	1		2	I	DSR 2*
RX(-)	I/O	3		4	I/O	RX(+)
TX(-)	O	5		6	I	TX(+)
DTR 2*	O	7		8	I	RI 2*
GND	-	9		10	-	Not Connected

* Active low signal

TABLE C-9: SCSI LED Connector (J8) - Pinout

Pin Number	Signal Flow	Signal
1	-	VCC (+5V)
2	O	SCLED*

* Active low signal

TABLE C-10: PCI Wide-Ultra SCSI Interface Connector (J9) - Pinout

Pin Number	Signal	Pin Number	Signal
1	GND	35	SD12*
2	GND	36	SD13*
3	GND	37	SD14*
4	GND	38	SD15*
5	GND	39	SDPH*
6	GND	40	SD0*
7	GND	41	SD1*
8	GND	42	SD2*
9	GND	43	SD3*
10	GND	44	SD4*
11	GND	45	SD5*
12	GND	46	SD6*
13	GND	47	SD7*
14	GND	48	SDP*
15	GND	49	GND
16	GND	50	GND
17	Term Power	51	Term Power
18	Term Power	52	Term Power
19	Not Connected	53	Not Connected
20	GND	54	GND
21	GND	55	SATN*
22	GND	56	GND
23	GND	57	SBSY*
24	GND	58	SACK*
25	GND	59	SRST*
26	GND	60	SMSG*
27	GND	61	SSEL*
28	GND	62	SCD*
29	GND	63	SREQ*
30	GND	64	SIO*
31	GND	65	SD8*
32	GND	66	SD9*
33	GND	67	SD10*
34	GND	68	SD11*

* Active low signal

TABLE C-11: Secondary Enhanced IDE Connector (J10) - Pinout

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	RESET*	2	-	GND
3	I/O	DATA 7	4	I/O	DATA 8
5	I/O	DATA 6	6	I/O	DATA 9
7	I/O	DATA 5	8	I/O	DATA 10
9	I/O	DATA 4	10	I/O	DATA 11
11	I/O	DATA 3	12	I/O	DATA 12
13	I/O	DATA 2	14	I/O	DATA 13
15	I/O	DATA 1	16	I/O	DATA 14
17	I/O	DATA 0	18	I/O	DATA 15
19	-	GND	20	-	Not Connected
21	I	DRQ 1	22	-	GND
23	O	IOW*	24	-	GND
25	O	IOR*	26	-	GND
27	I	IORDY	28	O	SEC. PDI[1]
29	O	DACK 1*	30	-	GND
31	I	IRQ15	32	-	Not Connected
33	O	ADD 1	34	I/O	SDIAG*
35	O	ADD 0	36	O	ADD 2
37	O	CS 1S*	38	O	CS 3S*
39	I	IDEACTS*	40	-	GND

* Active low signal
[1] 470 ohm pull-down

TABLE C-12: Flat Panel Extension Connector (J11) - Pinout

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	FP20	2	-	GND
3	O	FP21	4	-	GND
5	O	FP22	6	-	GND
7	O	FP23	8	-	GND
9	O	FP26	10	-	GND
11	O	FP27	12	-	GND
13	O	FP28	14	-	GND
15	O	FP29	16	-	GND
17	O	FP32	18	-	GND
19	O	FP33	20	-	FPVCC (3.3/5V Select)
21	O	FP34	22	-	FPVCC (3.3/5V Select)
23	O	FP35	24	O	Contrast Ctrl Out (0 - 3.85 V)
25	I/O	Contrast Ctrl Pot. Hi [1]	26	I/O	Contrast Ctrl Pot. Lo [1]

[1] This variable voltage output is used for adjusting contrast. Adjustment of these outputs are performed using the onboard I2C bus. For more information, contact TEKNOR's Technical Support department.

TABLE C-13: PanelLink Connector (J12) - Pinout

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	GP0	2	-	+12V
3	O	GP1	4	-	GND
5	O	GP2	6	-	GND
7	-	VCC	8	-	VCC
9	O	TXC-	10	O	TXC+
11	-	VCC3	12	-	VCC3
13	O	TX0-	14	O	TX0+
15	O	TX1-	16	O	TX1+
17	O	TX2-	18	O	TX2+
19	-	FPVCC (3.3/5V Select)	20	I	PD (Power Down)

TABLE C-14: USB Header (J13) - Pinout

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	-	+5V-USB0	2	-	+5V-USB1
3	I/O	USB0-	4	I/O	USB1-
5	I/O	USB0+	6	I/O	USB1+
7	-	GND-USB0	8	-	GND-USB1
9	-	SHIELD GND	10	-	SHIELD GND

TABLE C-15: V-PORT Connector (J14) - Pinout

I/O Pin	Signal Flow	Signal Name	I/O Pin	Signal Flow	Signal Name
Y1	I	VPC0	Z1	-	GND
Y2	I	VPC1	Z2	-	GND
Y3	I	VPC2	Z3	-	GND
Y4	I	VPC3	Z4	O	I2C_DATA
Y5	I	VPC4	Z5	I	VP_VSYNC
Y6	I	VPC5	Z6	O	EN_CAM*
Y7	I	VPC6	Z7	-	VCC
Y8	I	VPC7	Z8	-	GND
Y9	O	I2C_CLK	Z9	-	GND
Y10	I	VP_HSYNC*	Z10	-	GND
Y11	O	VP_OUT	Z11	-	GND
Y12	I	VP_IN	Z12	O	ZVPCLK
Y13	-	GND	Z13	I	VACTI

* Active low signal

TABLE C-16: Parallel Port Header (J15) - Standard Mode

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	STROBE*	2	O	AUTOFD*
3	I/O	PD0	4	I	ERROR*
5	I/O	PD1	6	O	INIT*
7	I/O	PD2	8	O	SELECTIN*
9	I/O	PD3	10	-	GND
11	I/O	PD4	12	-	GND
13	I/O	PD5	14	-	GND
15	I/O	PD6	16	-	GND
17	I/O	PD7	18	-	GND
19	I	ACK*	20	-	GND
21	I	BUSY	22	-	GND
23	I	PE	24	-	GND
25	I	SELECT	26	-	GND

* Active low signal

TABLE C-17: Parallel Port Connector (J15) - EPP Mode

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	WRITE*	2	O	DATASTB*
3	I/O	PD0	4	-	Not Connected
5	I/O	PD1	6	-	Not Connected
7	I/O	PD2	8	O	ADDRSTRB*
9	I/O	PD3	10	-	GND
11	I/O	PD4	12	-	GND
13	I/O	PD5	14	-	GND
15	I/O	PD6	16	-	GND
17	I/O	PD7	18	-	GND
19	I	INTR	20	-	GND
21	I	WAIT*	22	-	GND
23	-	Not Connected	24	-	GND
25	-	Not Connected	26	-	GND

* Active low signal

TABLE C-18: Parallel Port Connector (J15) - ECP Mode

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	STROBE*	2	O	AUTOFD*, HOSTACK[2]
3	I/O	PD0	4	I	FAULT*[1], PERIPHRQST*[2]
5	I/O	PD1	6	O	INIT*[1], REVERSERQST*[2]
7	I/O	PD2	8	O	SELECTIN*[1,2]
9	I/O	PD3	10	-	GND
11	I/O	PD4	12	-	GND
13	I/O	PD5	14	-	GND
15	I/O	PD6	16	-	GND
17	I/O	PD7	18	-	GND
19	I	ACK*	20	-	GND
21	I	BUSY, PERIPHACK[2]	22	-	GND
23	I	PERROR, ACKREVERSE[2]	24	-	GND
25	I	SELECT	26	-	GND

* Active low signal
[1] Compatible Mode
[2] High Speed Mode

NOTE

For more information on the ECP protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard (available from Microsoft Corporation) or contact our Technical Support department.

TABLE C-19: Mouse Header (J16) - Pinout

Pin Number	Signal Flow	Signal
1	I/O	MCLK
2	-	GND
3	I/O	MDATA
4	-	VCC (+5V)

TABLE C-20: External Battery Connector (J17) - Pinout

Pin Number	Signal Flow	Signal
1	I	EXTBAT
2	-	GND

TABLE C-21: Suspend Button Connector (J19) - Pinout

Pin Number	Signal Flow	Signal
1	I	PWRBT*
2	-	GND

* Active low signal

TABLE C-22: CompactFlash IDE Connector (J22) - Pinout

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	I/O	DD11	2	-	GND
3	I/O	DD12	4	I/O	DD3
5	I/O	DD13	6	I/O	DD4
7	I/O	DD14	8	I/O	DD5
9	I/O	DD15	10	I/O	DD6
11	O	CS3*	12	I/O	DD7
13	-	Not Connected	14	O	CS1*
15	-	Not Connected	16	O	IOR*
17	I/O	SDIAG*	18	O	IOW*
19	I	IRQ15	20	-	VCC (+5V)
21	-	VCC (+5V)	22	-	VCC (+5V)
23	-	GND	24	-	GND
25	O	RESET*	26	-	GND
27	O	W4 Jumper Select	28	O	DA2
29	O	DA1	30	I	ACTIVE*
31	O	DA0	32	-	Not Connected
33	I/O	DD0	34	I/O	DD8
35	I/O	DD1	36	I/O	DD9
37	I/O	DD2	38	I/O	DD10
39	-	Not Connected	40	-	GND

* Active low signal

TABLE C-23: TV-OUT Connector (J23) - Pinout

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	RED	2	-	DAC GND
3	O	GREEN	4	-	DAC GND
5	O	BLUE	6	-	DAC GND
7	O	CSYNC	8	-	GND
9	O	TVON	10	-	GND
11	O	NTSC_PAL	12	-	GND
13	O	HSYNC	14	O	VSYNC

TABLE C-24: CRT VGA Interface Connector (J24) - Pinout

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	RED	6	-	ANALOG GND	11	-	Not Connected
2	O	GREEN	7	-	ANALOG GND	12	O	I2CDATA
3	O	BLUE	8	-	ANALOG GND	13	O	RHSYNC
4	-	Not Connected	9	-	Not Connected	14	O	RVSYNC
5	-	GND	10	-	GND	15	O	I2CCLK

TABLE C-25: PS/2 Connector (J26) - Pinout

Pin Number	Signal Flow	Signal
1	I/O	KDATA when W16 jumper pins 3-5 and 4-6 are shorted, or MDATA when W16 jumper pins 1-3 and 2-4 are shorted.
2	-	Not Connected
3	-	GND
4	-	VCC (+5V)
5	I/O	KBCLK when W16 jumper pins 3-5 and 4-6 are shorted, or MCLK when W16 jumper pins 1-3 and 2-4 are shorted.
6	-	GND

TABLE C-26: Ethernet 10Base-T/100Base-T RJ-45 Connector (J27) - Pinout

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	O	TX+	2	O	TX-
3	I	RX+	4	-	RJ1[1]
5	-	RJ1[1]	6	I	RX-
7	-	RJ2[1]	8	-	RJ2[1]

[1] These lines are terminated with 75 ohm resistors.

TABLE C-27: Fan Connector (J29) - Pinout

Pin Number	Signal
1	+5V
2	GND

TABLE C-28: PC/104-Plus Connector (J30) - Pinout

A Side

I/O Pin	Signal Name	I/O
A1	5V_KEY	-
A2	VI/O	-
A3	AD5	I/O
A4	C/BE0*	I/O
A5	GND	-
A6	AD11	I/O
A7	AD14	I/O
A8	+3.3V	-
A9	SERR*	I/O
A10	GND	-
A11	STOP*	I
A12	+3.3V	-
A13	FRAME*	O
A14	GND	-
A15	AD18	I/O
A16	AD21	I/O
A17	+3.3V	-
A18	IDSEL0	O
A19	AD24	I/O
A20	GND	-
A21	AD29	I/O
A22	+5V	-
A23	REQ0*	I
A24	GND	-
A25	GNT1*	O
A26	+5V	-
A27	CLK2	O
A28	GND	-
A29	+12V	-
A30	-12V	-

B Side

I/O Pin	Signal Name	I/O
B1	Not Connected	-
B2	AD2	I/O
B3	GND	-
B4	AD7	I/O
B5	AD9	I/O
B6	VI/O	-
B7	AD13	I/O
B8	C/BE1*	I/O
B9	GND	-
B10	PERR*	I/O
B11	+3.3V	-
B12	TRDY*	I
B13	GND	-
B14	AD16	I/O
B15	+3.3V	-
B16	AD20	I/O
B17	AD23	I/O
B18	GND	-
B19	C/BE3*	I/O
B20	AD26	I/O
B21	+5V	-
B22	AD30	I/O
B23	GND	-
B24	REQ2*	I
B25	VI/O	-
B26	CLK0	O
B27	+5V	-
B28	INTD*	I
B29	INTA*	I
B30	Not Connected	-

* Active low signal

TABLE C-28: PC/104-Plus Connector (J30) – Pinout (Continued)

C Side

I/O Pin	Signal Name	I/O
C1	+5V	-
C2	AD1	I/O
C3	AD4	I/O
C4	GND	-
C5	AD8	I/O
C6	AD10	I/O
C7	GND	-
C8	AD15	I/O
C9	SB0*	I/O
C10	+3.3V	-
C11	LOCK*	I/O
C12	GND	-
C13	IRDY*	O
C14	+3.3V	-
C15	AD17	I/O
C16	GND	-
C17	AD22	I/O
C18	IDSEL1	O
C19	VI/O	-
C20	AD25	I/O
C21	AD28	I/O
C22	GND	-
C23	REQ1*	I
C24	+5V	-
C25	GNT2*	O
C26	GND	-
C27	CLK3	O
C28	+5V	-
C29	INTB*	I
C30	Not Connected	-

D Side

I/O Pin	Signal Name	I/O
D1	AD0	I/O
D2	+5V	-
D3	AD3	I/O
D4	AD6	I/O
D5	GND	-
D6	Not Connected (MM66EN)	-
D7	AD12	I/O
D8	+3.3V	-
D9	PAR	I/O
D10	SDONE	I/O
D11	GND	-
D12	DEVSEL*	I
D13	+3.3V	-
D14	C/BE2*	I/O
D15	GND	-
D16	AD19	I/O
D17	+3.3V	-
D18	IDSEL2	O
D19	IDSEL3	O
D20	GND	-
D21	AD27	I/O
D22	AD31	I/O
D23	VI/O	-
D24	GNT0*	O
D25	GND	-
D26	CLK1	O
D27	GND	-
D28	RESET*	O
D29	INTC*	I
D30	3.3V_KEY	-

* Active low signal

TABLE C-29: PCI Bus Connector - Pinout

E SIDE (J31) **F SIDE (J38)**

I/O PIN	Signal Name	I/O		I/O PIN	Signal Name	I/O
E1	VCC (+5V)	-		F1	-12V	-
E2	+12V	-		F2	Not Connected	-
E3	Not Connected	-		F3	GND	-
E4	TD	-		F4	TD	-
E5	VCC (+5V)	-		F5	VCC (+5V)	-
E6	INTA*	I		F6	VCC (+5V)	-
E7	INTC*	I		F7	INTB*	I
E8	VCC (+5V)	-		F8	INTD*	I
E9	CLK2	O		F9	REQ3*	I
E10	VCC (+5V)	-		F10	REQ1*	I
E11	CLK3	O		F11	GNT3*	O
E12	GND	-		F12	GND	-
E13	GND	-		F13	GND	-
E14	GNT1*	O		F14	CLK0	O
E15	RESET*	O		F15	GND	-
E16	VCC (+5V)	-		F16	CLK1	O
E17	GNT0*	O		F17	GND	-
E18	GND	-		F18	REQ0*	I
E19	REQ2*	I		F19	VCC (+5V)	-
E20	AD30	I/O		F20	AD31	I/O
E21	Not Connected	-		F21	AD29	I/O
E22	AD28	I/O		F22	GND	-
E23	AD26	I/O		F23	AD27	I/O
E24	GND	-		F24	AD25	I/O
E25	AD24	I/O		F25	Not Connected	-
E26	GNT2*	O		F26	C/BE3*	I/O
E27	Not Connected	-		F27	AD23	I/O
E28	AD22	I/O		F28	GND	-
E29	AD20	I/O		F29	AD21	I/O
E30	GND	-		F30	AD19	I/O

* Active low signal

TABLE C-29: PCI Bus Connector - Pinout (Continued)

E SIDE (J31) **F SIDE (J38)**

I/O PIN	Signal Name	I/O		I/O PIN	Signal Name	I/O
E31	AD18	I/O		F31	Not Connected	-
E32	AD16	I/O		F32	AD17	I/O
E33	Not Connected	-		F33	C/BE2*	I/O
E34	FRAME*	O		F34	GND	-
E35	GND	-		F35	IRDY*	O
E36	TRDY*	I		F36	Not Connected	-
E37	GND	-		F37	DEVSEL*	I
E38	STOP*	I		F38	GND	-
E39	Not Connected	-		F39	PLOCK*	I/O
E40	SDONE	I/O		F40	PERR*	I/O
E41	SBO*	I/O		F41	Not Connected	-
E42	GND	-		F42	SERR*	I/O
E43	PAR	I/O		F43	Not Connected	-
E44	AD15	I/O		F44	C/BE1*	I/O
E45	Not Connected	-		F45	AD14	I/O
E46	AD13	I/O		F46	GND	-
E47	AD11	I/O		F47	AD12	I/O
E48	GND	-		F48	AD10	I/O
E49	AD9	I/O		F49	GND	-
E50	Connector Key	-		F50	Connector Key	-
E51	Connector Key	-		F51	Connector Key	-
E52	C/BE0*	I/O		F52	AD8	I/O
E53	Not Connected	-		F53	AD7	I/O
E54	AD6	I/O		F54	Not Connected	-
E55	AD4	I/O		F55	AD5	I/O
E56	GND	-		F56	AD3	I/O
E57	AD2	I/O		F57	GND	-
E58	AD0	I/O		F58	AD1	I/O
E59	VCC (+5V)	-		F59	VCC (+5V)	-
E60	REQ64*	I/O		F60	ACK64*	I/O
E61	VCC (+5V)	-		F61	VCC (+5V)	-
E62	VCC (+5V)	-		F62	VCC (+5V)	-

* Active low signal

TABLE C-30: ISA Bus Connector - Pinout

A SIDE (J33)

I/O Pin	Signal Name	I/O
A1	IOCHK*	I
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	IOCHRDY	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O
A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

B SIDE (J36)

I/O Pin	Signal Name	I/O
B1	GND	-
B2	RESET DRV	O
B3	VCC (+5V)	-
B4	IRQ9	I
B5	-5V	-
B6	DRQ2	I
B7	-12V	-
B8	NOWS*	I
B9	+12V	-
B10	GND	-
B11	SMEMW*	O
B12	SMEMR*	O
B13	IOW*	I/O
B14	IOR*	I/O
B15	DACK3*	O
B16	DRQ3	I
B17	DACK1*	O
B18	DRQ1	I
B19	REFRESH*	I/O
B20	SYSCLK	O
B21	IRQ7	I
B22	IRQ6	I
B23	IRQ5	I
B24	IRQ4	I
B25	IRQ3	I
B26	DACK2*	O
B27	T/C	O
B28	BALE	O
B29	VCC (+5V)	-
B30	OSC	O
B31	GND	-

* Active low signal

TABLE C-30: ISA Bus Connector - Pinout (Continued)

C SIDE (J32)

I/O Pin	Signal Name	I/O
C1	SBHE*	I/O
C2	LA23	I/O
C3	LA22	I/O
C4	LA21	I/O
C5	LA20	I/O
C6	LA19	I/O
C7	LA18	I/O
C8	LA17	I/O
C9	MEMR*	I/O
C10	MEMW*	I/O
C11	SD8	I/0
C12	SD9	I/O
C13	SD10	I/O
C14	SD11	I/O
C15	SD12	I/O
C16	SD13	I/O
C17	SD14	I/O
C18	SD15	I/O

D SIDE (J37)

I/O Pin	Signal Name	I/O
D1	MEMCS16*	I
D2	IOCS16*	I
D3	IRQ10	I
D4	IRQ11	I
D5	IRQ12	I
D6	IRQ15	I
D7	IRQ14	I
D8	DACK0*	O
D9	DRQ0	I
D10	DACK5*	O
D11	DRQ5	I
D12	DACK6*	O
D13	DRQ6	I
D14	DACK7*	O
D15	DRQ7	I
D16	VCC (+5V)	-
D17	MASTER*	I
D18	GND	-

* Active low signal

TABLE C-31: PC/104 Connector (P2) - Pinout

A Side

I/O Pin	Signal Name	I/O
A1	IOCHK*	I
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	IOCHRDY	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O
A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O
A32	GND	-

B Side

I/O Pin	Signal Name	I/O
B1	GND	-
B2	RESET DRV	O
B3	VCC (+5V)	-
B4	IRQ9	I
B5	-5V	-
B6	DRQ2	I
B7	-12V	-
B8	0WS*	I
B9	+12V	-
B10	Not Connected	-
B11	SMEMW*	O
B12	SMEMR*	O
B13	IOW*	I/O
B14	IOR*	I/O
B15	DACK3*	O
B16	DRQ3	I
B17	DACK1*	O
B18	DRQ1	I
B19	REFRESH*	I/O
B20	SYSCLK	O
B21	IRQ7	I
B22	IRQ6	I
B23	IRQ5	I
B24	IRQ4	I
B25	IRQ3	I
B26	DACK2*	O
B27	T/C	O
B28	BALE	O
B29	VCC (+5V)	-
B30	OSC	O
B31	GND	-
B32	GND	-

*Active low signal

TABLE C-31: PC/104 Connector (P1) – Pinout (Continued)

C Side

I/O Pin	Signal Name	I/O
C0	GND	-
C1	SBHE*	I/O
C2	LA23	I/O
C3	LA22	I/O
C4	LA21	I/O
C5	LA20	I/O
C6	LA19	I/O
C7	LA18	I/O
C8	LA17	I/O
C9	MEMR*	I/O
C10	MEMW*	I/O
C11	SD8	I/O
C12	SD9	I/O
C13	SD10	I/O
C14	SD11	I/O
C15	SD12	I/O
C16	SD13	I/O
C17	SD14	I/O
C18	SD15	I/O
C19	Not Connected	-

D Side

I/O Pin	Signal Name	I/O
D0	GND	-
D1	MEMCS16*	I
D2	IOCS16*	I
D3	IRQ10	I
D4	IRQ11	I
D5	IRQ12	I
D6	IRQ15	I
D7	IRQ14	I
D8	DACK0*	O
D9	DRQ0	I
D10	DACK5*	O
D11	DRQ5	I
D12	DACK6*	O
D13	DRQ6	I
D14	DACK7*	O
D15	DRQ7	I
D16	VCC (+5V)	-
D17	MASTER*	I
D18	GND	-
D19	GND	-

* Active low signal

D. LIST OF APPROVED VENDORS

The following is list of recommended devices and connectors for use on the PCI-941. Many other models are available and function equally well. Users are encouraged to check with their local distributors for comparable substitutes.

D.1 RECOMMENDED DRAM DEVICES

Recommended DRAM devices for the 168-pin sockets have these features:

- 3.3V only, single-sided or double-sided.
- Registered/Unregistered 66MHz modules.
- Serial Presence Detect (SPD) EPROM.
- 64-bit or 72-bit DIMMs.
- Error Checking and Correction (ECC) or parity bit, with 72-bit DIMMs.
- Compliant with Intel's PC SDRAM Unbuffered DIMM Specification (66MHz), Revision 1.0.

Consult the following list to see examples of recommended DRAM devices on the PCI-941.

TABLE D-1: Recommended DRAM Devices on the PCI-941

DIMM	VENDOR	PART NUMBER
2M*72 (SDRAM) 16MB module	CENTON	CFDKG1TTNVU367G
4M*72 (SDRAM) 32MB module	ROCKY MOUNTAIN RAM	4x72CQ2x8S4E
	CENTON	CFEKG1TTNVU367G
8M*72 (SDRAM) 64MB module	CENTON	CKFKJ1TT4VU346G
16M*72 (SDRAM) 128MB module	CENTON	CKGKJ1TT4VU371G
	ROCKY MOUNTAIN RAM	16x72CQ8x8S4E

D.2 INTERFACE CONNECTORS

The following connectors are recommended for interfacing with the I/O devices. The parts shown here do not have a strain relief but one may be added.

Connector	Recommended Mating Part
SCSI Header (J1)	AMP 1-746285-0 [optional strain relief: 499252-4], Robinson Nugent IDS-C50PK-TG, Thomas & Betts 622-5030 [optional strain relief: 622-5041]. (50-pin flat cable connector).
IDE Hard Disks (J2, J10)	AMP 746285-9 [optional strain relief: 499252-1], Robinson Nugent IDS-C40PK-TG, Thomas & Betts 622-4030 [optional strain relief: 622-4041]. (40-pin flat cable connector).
Floppy Disk (J4)	Amp 746285-8 [optional strain relief: 499252-6], Robinson Nugent IDS-C34PK-TG, Thomas & Betts 622-3430 [optional strain relief: 622-3441]. (34-pin flat cable connector).
Multi-Function (J5)	Amp 746285-3 [optional strain relief: 499252-8], Robinson Nugent IDS-C16PK-TG, Thomas & Betts 622-1630 [optional strain relief: 622-1641]. (16-pin flat cable connector).
Serial Ports 1 & 2 (J6, J7)	Amp 746285-1 [optional strain relief: 499252-5], Robinson Nugent IDS-C10PK-TG, Thomas & Betts 622-1030 [optional strain relief: 622-1041]. (10-pin flat cable connector).
SCSI LED (J8)	Leoco 2530 S020013 (housing), Leoco 2533 TCB00A0 (crimp). Molex 22-01-3027 (housing), Molex 08-50-0114 (crimp).
USB (J13)	Teknor 150-316 (Universal Serial Bus Cable Assembly).

Connector	Recommended Mating Part
Parallel Port (J15)	Amp 746285-6 [optional strain relief: 499252-3], Robinson IDS-C26PK-TG, Thomas & Betts 622-2630 [optional strain relief: 622-2641]. (Polarized IDC female socket connector).
PS/2 Mouse (J16)	Molex 22-01-3047 (connector), Molex 20-50-0114 (crimp).

E. I/O MAP

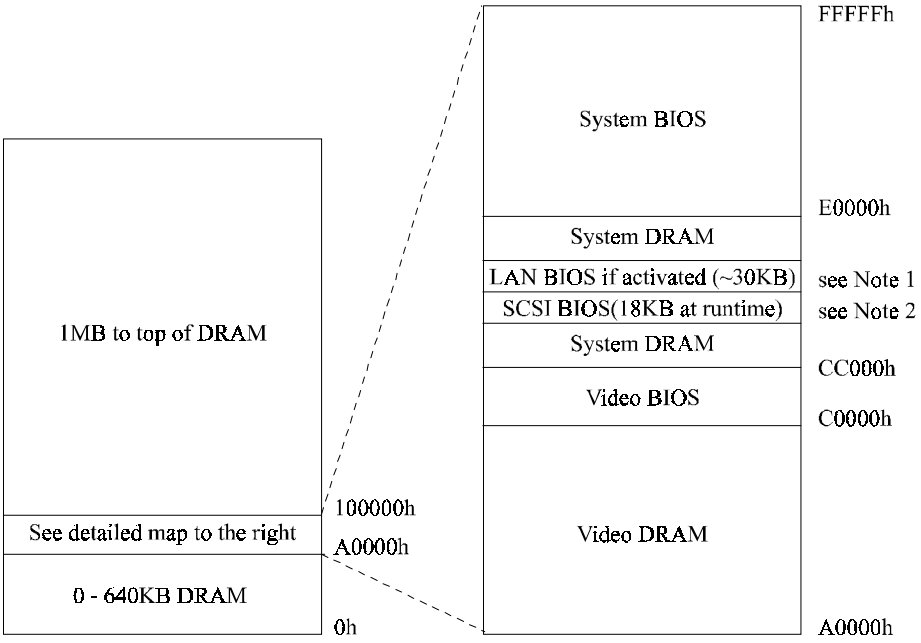
TABLE E-1: I/O Map

Address	Optional Address	Optional Address	Optional Address	Function
000-01F				DMA Controller 1
020-03F				Interrupt Controller 1
040-05F				Timer
060-06F				Keyboard
070-07F				Real-time clock
080-09F				DMA Page Register
0A0-0BF				Interrupt Controller 2
0C0-0DF				DMA Controller 2
0F0-0F1, 0F8-0FF				Math Coprocessor
190-197	290-297	390-397		TEKNOR Control Port
1F0-1F7, 3F6				Primary IDE
170-177, 376				Secondary IDE
3F0-3F7	370-377			Floppy Disk
378-37A	3BC-3BE	278-27A		Parallel Port (LPT1 by default)
3F8-3FF (COM1)	2F8-2FF (COM2)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 2 (COM2 by default)
3C0-3CF, 3D0-3DF, 3B0-3BB				Graphics Controller (I2C Port)

F. MEMORY MAP

Diagram F-1 illustrates the system memory map. It is shown in table format in Table F-1.

DIAGRAM F-1: Memory Map Diagram



Note 1: LAN BIOS address may vary.

Note 2: SCSI BIOS address may vary.
Size only 2KB if no device.

TABLE F-1: Memory Map

Address	Function
00000-9FFFF	0-640 KB DRAM
A0000-BFFFF	Video DRAM
C0000-CBFFF	Video BIOS
D8000-FFFFF	System DRAM
	LAN BIOS around 30KB if activated, address may vary
	SCSI BIOS 18KB at runtime, 2KB if no device, address may vary
100000-Top of DRAM	1 MB - Top of DRAM

G. IRQ LINES

The PCI-941 board is fully PC compatible with interrupt steering for PCI plug and play compatibility.

TABLE G-1: IRQ Lines

Controller # 1		Controller # 2	
IRQ 0	Timer Output 0	IRQ 8	Real-Time Clock
IRQ 1	Keyboard (Output Buffer Full)	IRQ 9	Available [1]
IRQ 2	Cascade Controller # 2	IRQ 10	Available [1]
IRQ 3	Serial Port 2 *	IRQ 11	Available [1]
IRQ 4	Serial Port 1 *	IRQ 12	PS/2 Mouse
IRQ 5	Parallel Port 2 * or Available [1]	IRQ 13	Coprocessor Error
IRQ 6	Floppy Controller *	IRQ 14	Primary IDE * or available [1]
IRQ 7	Parallel Port 1 * or Available [1]	IRQ 15	Secondary IDE * or available [1]

* All functions marked with an asterisk (*) can be disabled or reconfigured.
[1] Available lines service on board and external PCI/ISA PnP devices or a Legacy ISA device.

H. DMA CHANNELS

The PCI-941 integrates the functionality of two 8237 DMA controllers. Eight DMA channels are available.

According to Plug and Play standards, the system BIOS automatically allocates DMA Channel 1 or 3 for the parallel port's ECP mode. Channel 2 is reserved for the floppy controller and Channel 4 is used to cascade Channels 0 through 7 to the microprocessor.

TABLE H-1: DMA Channels

DMA Channel	Function
DMA 0	Available
DMA 1	PnP available (ECP)
DMA 2	Floppy controller
DMA 3	PnP available (ECP)
DMA 4	Cascade controller # 1
DMA 5	PnP available
DMA 6	PnP available
DMA 7	PnP available

I. BIOS SETUP ERROR CODES

I.1 POST MESSAGES

During the Power On Self Test (POST), if the BIOS detects an error requiring your attention, it will either sound a beep code, display a message, or both.

If a message is displayed, it will be accompanied by:
"PRESS F1 TO CONTINUE, DEL TO ENTER SETUP".

I.2 POST BEEP

Currently there is only one beep code in the Main BIOS (more in Emergency Procedure, Appendix J.3). This code indicates that a video error has occurred and BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps.

I.3 ERROR MESSAGES

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

CMOS BATTERY HAS FAILED

CMOS battery is no longer functional and should be replaced, or battery jumper is removed and should be installed.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This can indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace it if necessary. It can also happen if the battery jumper is removed: in such a case, it should be installed.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP

Type of diskette drive installed in the system is different from CMOS definition. Run Setup to reconfigure the drive type correctly.

DISPLAY TYPE HAS CHANGED SINCE LAST BOOT

Since last powering off the system, the display adapter has been changed. You must configure the system for the new display type.

ERROR ENCOUNTERED INITIALIZING HARD DRIVE

Hard drive cannot be initialized. Be sure the adapter is installed correctly and all cables are correctly and firmly attached. Also be sure the correct hard drive type is selected in Setup.

ERROR INITIALIZING HARD DRIVE DISK CONTROLLER

Cannot initialize controller. Make sure the cord is correctly and firmly installed on the CPU board. Be sure the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set on the hard drive.

FLOPPY DISK CNTRLR ERROR OR NO CNTRLR PRESENT

Cannot find or initialize the floppy drive controller. Make sure the controller is installed correctly and firmly. If there are no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause BIOS to ignore the missing keyboard and continue the boot.

MEMORY ADDRESS ERROR AT ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory.

MEMORY PARITY ERROR AT ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory.

MEMORY VERIFY ERROR AT ...

Indicates an error verifying a value already written to memory. You can use this location along with the memory map for your system to find and replace the bad memory.

OFFENDING SEGMENT

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

PRESS A KEY TO REBOOT

This will be displayed at the bottom of the screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a non-maskable interrupt condition during boot, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

RAM PARITY ERROR - CHECKING FOR SEGMENT ...

Indicates a parity error in Random Access Memory.

I.4 POST CODES

NOTE

ISA POST codes are output to port address 80h.

TABLE I-1: POST Codes

POST (hex)	Name	Description	
01	BOOT BLOCK	Boot Block in EMERGENCY : Clear Base Memory Area.	
03	Initialize Chips	1. Clear CMOS shutdown byte. 2. Initialize EISA extended registers. (Not for us since we don't have EISA bus.)	
04	Test Memory Refresh Toggle	RAM must be periodically refreshed in order to keep the memory from decaying.	
05	Blank Video, Initialize Keyboard	1. Clear CMOS reset status byte. 2. Early Keyboard initialization.	Boot Block in EMERGENCY: Initialize Keyboard Controller.
06	EPROM Checksum	1. Test F000h segment shadow readable and writeable for POST access correct. If not, show POST FE and beep continuously… 2. Autodetect Flash EPROM.	
07	Test CMOS Interface and Battery Status	1. Install the TEKNOR segment. 2. Verifies CMOS is working correctly (walking bit test). 3. Restore CMOS from Flash if option is enabled. 4. Check for OVERRIDE KEY (INSERT key).	
08	Program Chipset default	Program Chipset default (show POST BEh).	
09	Early Cache Initialization	1. Check for Intel's and/or Cyrix CPU. 2. Early Cache Initialization when cache is separate from chipset. 3. Turn off Gate A20.	
0A	Setup Interrupt Vector Table	1. Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize int. 00h-1Fh according to INT_TBL. 2. Early Power Management Initialization.	

TABLE I-1: POST Codes (Continued)

POST (hex)	Name	Description	
0B	Test CMOS RAM Checksum	1. Verify time and date for valid values. 2. If Override enabled, check for Override key. If Override key pressed, Kill CMOS checksum. 3. Check CMOS Battery (useless if save CMOS in FLASH enabled since it's already done). 4. Verify Checksum, if bad, load defaults. 5. Copy CMOS in the stack. 6. Clear CMOS Alarm date. 7. Clear HD if Hidden. 8. Clear Floppy "B" if only one drive. 9. Detect for a Math Co-processor. 10. Set Fast Gate A20 Flag in CMOS. 11. If "B" drive only is set the 2 Drive are set… 12. Program Chipset for early Power Management. 13. P6 Bios Update (if applicable). 14. Kill Onboard PnP IO. 15. PnP Early Initialization. 16. PnP System Resource: 1. Get ESCD. 2. Create default SYSTEM_MAP. 3. Decode/Record ISA ESCD resources. 4. Record I/O port for PnP operation. 17. Chipset Early Shadow.	
0C	Initialize Keyboard	1. Open Xilinx I/O Port location to x90h (X=1,2 or 3) inside the chipset (if necessary). 2. Disable (if necessary). Thermal Management. 3. Disable (if necessary) Ethernet Chip.Set IDE Detect counter to 0. 4. Set CD-ROM found variable to 0. 5. Initialize zone 40:0h for the keyboard buffer.	Boot Block 1st : Verify BIOS checksum. Boot Block in EMERGENCY 2nd : Init. vector 00h through 77h.

TABLE I-1: POST Codes (Continued)

POST (hex)	Name	Description	
0D	Initialize Video Interface & Chipset	1. On M1 set the cache for the memory installed. 2. On PCI, do a PCI ROM init. 3. On P6, Init. Apic. 4. Init. Chipset. 5. Turn ON CPU Cache. 6. Set Maximum Speed. 7. Measure CPU Clock Speed. 8. Restore Speed. 9. Turn Off CPU Cache. 10. Early Video Shadow. 11. Read CMOS location 14h to find out type of video to use. Detect and initialize Video Adapter. 12. Init. T380 if necessary.	Boot Block in EMERGENCY: Try to init. Video Card…
0E	Test Video Memory	1. If CGA or MONO, test video memory. 2. Beep the speaker. 3. Show the LOGO. 4. Install VT100 driver if necessary. 5. Write sign-on message to screen. 6. Write Copyright message to screen. 7. Write Evaluation message to screen. 8. Show CPU type and speed.	
0F	Test DMA Controller 0	Test DMA Controller 0.	
10	Test DMA Controller 1	Test DMA Controller 1.	
11	Test DMA Page Registers	Test DMA Page Registers.	
12	Reserved	Reserved for 8254 Counter 0 - Not implemented.	
13	Reserved	Reserved for 8254 Counter 1 - Not implemented.	
14	Test Timer Counter 2	Test 8254 Timer 0 Counter 2.	
15	PIC Test 8259-1 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	
16	PIC Test 8259-2 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	
17	Test Struck 8259's Interrupt Bits	Nothing	
18	Test 8259 Interrupt functionality	Force an interrupt and verify that the interrupt occurred (IRQ 0 - clock int. 8h).	
19	Test Struck NMI Bits (Parity/ IO check)	Nothing.	
1A	Reserved	Reserved	
1B	Reserved	Reserved	
1C	Reserved	Reserved	
1D	Reserved	Reserved	
1E	Reserved	Reserved	

TABLE I-1: POST Codes (Continued)

POST (hex)	Name	Description
1F	Set EISA Mode	If EISA non-volatile memory checksum is good, execute EISA initialization. If no, execute ISA test and clear EISA mode flag. Test EISA Configuration Memory integrity (checksum & communication interface).
20	Enable Slot 0	Initialize slot 0 (System Board).
21	Enable Slot 1	Initialize slot 1.
22	Enable Slot 2	Initialize slot 2.
23	Enable Slot 3	Initialize slot 3.
24	Enable Slot 4	Initialize slot 4.
25	Enable Slot 5	Initialize slot 5.
26	Enable Slot 6	Initialize slot 6.
27	Enable Slot 7	Initialize slot 7.
28	Enable Slot 8	Initialize slot 8.
29	Enable Slot 9	Initialize slot 9.
2A	Enable Slot 10	Initialize slot 10.
2B	Enable Slot 11	Initialize slot 11.
2C	Enable Slot 12	Initialize slot 12.
2D	Enable Slot 13	Initialize slot 13.
2E	Enable Slot 14	Initialize slot 14.
2F	Enable Slot 15	Initialize slot 15.
30	Size Base & Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB.
31	Test Base & Extended Memory	1. Test base memory from 256K to 640K and extended memory above 1MB using various patterns. 2. The last test is filling memory with 0's. 3. On a quick memory test or if user press the ESC key while testing memory, only the last test is performed.
32	Test EISA Extended Memory	If EISA Mode flag is set, then test EISA memory found in slots Initialization. NOTE 1: This will be skipped in ISA mode. NOTE 2: This POST also Detect & Report I/O PORTS and also Init. Super IO.
33	Reserved	Reserved
34	Reserved	Reserved
35	Reserved	Reserved
36	Reserved	Reserved
37	Reserved	Reserved
38	Reserved	Reserved
39	Reserved	Reserved
3A	Reserved	Reserved
3B	Reserved	Reserved

TABLE I-1: POST Codes (Continued)

POST (hex)	Name	Description
3C	Setup Enable	
3D	Initialize & Install PS/2 Mouse	Detect if mouse is present. Initialize mouse. Install interrupt vector.
3E	Setup Cache Controller	Initialize cache controller.
3F	Reserved	Reserved
40	Reserved	Reserved
41	Initialize Floppy Drive & Controller	1. Verify if we should enter setup. If so, enter setup. 2. Initialize floppy disk drive controller and any drive. Boot Block in EMERGENCY: Scan for Floppy for emergency disk…
42	Initialize Hard Drive & Controller	Initialize hard drive controller and any drive. (Call HD_INSTALL).
43	Detect & Initialize Serial/Parallel/Joystick ports	Initialize any serial, parallel and game ports.
44	Reserved	Reserved
45	Detect & Initialize Math Coprocessor	Initialize Math Coprocessor.
46	Reserved	Reserved
47	Set Speed for Boot	Set Speed for Boot.
48	Reserved	Reserved
49	Reserved	Reserved
4A	Reserved	Reserved
4B	Reserved	Reserved
4C	Reserved	Reserved
4D	Init. PC-Speaker to LINE OUT	Enable access to PC-Speaker to LINE OUT and Enable/Disable it. (T934).
4E	Manufacturing POST Loop or display Messages	1. Reboot if Manufacturing POST Loop pin is set. 2. Otherwise display any messages (i.e., any non-fatal errors that were detected during POST). 3. Enter SETUP if needed.
4F	Security Check	Ask password security if needed.
50	Write CMOS	Write all CMOS values back to CMOS-RAM and clear screen.
51	Pre-Boot Enable	1. Enable Parity checker. 2. Enable NMI. 3. Enable cache before boot.
52	Initialize Option (ROM scan)	1. Call POST 81 2. Initialize any ROMs present from C8000h to DBFFFh. Disable POST code from segment E0000h. 3. Initialize any ROMs present from DC000h to E0800h. NOTE: When FSCAN option is enabled, will initialize from C8000h to F7FFFh.
53	Initialize Time Value	Initialize Time value in 40h: BIOS area.
54	Reserved	Reserved
55	Reserved	Reserved
56	Reserved	Reserved

TABLE I-1: POST Codes (Continued)

POST (hex)	Name	Description
57	Reserved	Reserved
58	Reserved	Reserved
59	Reserved	Reserved
5A	Reserved	Reserved
5B	Reserved	Reserved
5C	Reserved	Reserved
5D	Reserved	Reserved
5E	Reserved	Reserved
5F	Reserved	Reserved
60		Store boot partition of head & cylinder.
61	Final Init	For last µs detail before boot.
62	Num Lock ON	Put Num Lock ON and Daylight Saving.
63	Boot Attempt	1. Call POST 82. 2. Set Low stack. 3. Boot via int 19h.
64	Reserved	Reserved
65	Reserved	Reserved
66	Reserved	Reserved
67	Reserved	Reserved
68	Reserved	Reserved
69	Reserved	Reserved
6A	Reserved	Reserved
6B	Reserved	Reserved
6C	Reserved	Reserved
6D	Reserved	Reserved
6E	Reserved	Reserved
6F	Reserved	Reserved
70	Reserved	Reserved
71	Reserved	Reserved
72	Reserved	Reserved
73	Reserved	Reserved
74	Reserved	Reserved
75	Reserved	Reserved
76	Reserved	Reserved
77	Reserved	Reserved
78	Reserved	Reserved
79	Reserved	Reserved
7A	Reserved	Reserved
7B	Reserved	Reserved
7C	Reserved	Reserved
7D	Reserved	Reserved
7E	Reserved	Reserved
7F	Reserved	Reserved
80	Teknor Segment Move 1	Install the Teknor segment from Flash to DC00:0h.
81	Teknor Segment Move 2	Install the Teknor segment from DC00:0h to 7000:0h.
82	Teknor Segment Move 3	Install the Teknor segment from 7000:0h to EC00:0h.

TABLE I-1: POST Codes (Continued)

POST (hex)	Name	Description
83	Check & Program CPLD	Check & Program CPLD for valid UserCode & IDCode.
84	Teknor CRC Check	Check if Teknor block have a valid CRC. If not, the Emergency procedure is launched.
85	Reserved	Reserved
86	Reserved	Reserved
87	Reserved	Reserved
88	Reserved	Reserved
89	Reserved	Reserved
8A	Reserved	Reserved
8B	Reserved	Reserved
8C	Reserved	Reserved
8D	Reserved	Reserved
8E	Reserved	Reserved
8F	Reserved	Reserved
90	Reserved	Reserved
91	Reserved	Reserved
92	Reserved	Reserved
93	Reserved	Reserved
94	Reserved	Reserved
95	Reserved	Reserved
96	Reserved	Reserved
97	Reserved	Reserved
98	Reserved	Reserved
99	Reserved	Reserved
9A	Reserved	Reserved
9B	Reserved	Reserved
9C	Reserved	Reserved
9D	Reserved	Reserved
9E	Reserved	Reserved
9F	Reserved	Reserved
A0	Reserved	Reserved
A1	Reserved	Reserved
A2	Reserved	Reserved
A3	Reserved	Reserved
A4	Reserved	Reserved
A5	Reserved	Reserved
A6	Reserved	Reserved
A7	Reserved	Reserved
A8	Reserved	Reserved
A9	Reserved	Reserved
AA	Reserved	Reserved
AB	Reserved	Reserved
AC	Reserved	Reserved
AD	Reserved	Reserved
AE	Reserved	Reserved
AF	Reserved	Reserved
B0	Spurious	If interrupt occurs in protected mode.

TABLE I-1: POST Codes (Continued)

POST (hex)	Name	Description	
B1	Unclaimed NMI	If unmasked NMI occurs, display: Press F1 to disable NMI, F2 reboot.	
B2	Reserved	Reserved	
B3	Reserved	Reserved	
B4	Reserved	Reserved	
B5	Reserved	Reserved	
B6	Reserved	Reserved	
B7	Reserved	Reserved	
B8	Reserved	Reserved	
B9	Reserved	Reserved	
BA	Reserved	Reserved	
BB	Reserved	Reserved	
BC	Reserved	Reserved	
BD	Reserved	Reserved	
BE	Early Prog Chipset Def.	Going to early program chipset to default values (called from POST_8s).	
BF	Program Chip Set	Called early at POST 0Dh to program chipset from CT-TABLE.	
C0	Turn ON/OFF Cache	OEM Specific - Cache control.	Boot Block: First POST.
C1	Memory presence	OEM Specific - Test to size on-board memory test.	Boot Block: Search for Boot Block Signature "*BBSS*".
C2	Early Memory Initialization	OEM Specific - Board Initialization.	
C3	Extended Memory Initialization	OEM Specific - Turn ON extended memory DRAM select.	Boot Block: Expand compressed BIOS
C4	Special Display Switch Handling	OEM Specific - Display/Video switch handling so that display switch errors never occur.	
C5	Early Shadow	OEM Specific - Early Shadow enable for fast boot.	Boot Block: Early Shadow System BIOS.
C6	Cache Programming	OEM Specific - Routine for programming which region are cacheable.	Boot Block: Cache Sizing
C7	Reserved	Reserved	
C8	Special Speed Switching	OEM Specific - Routine to handle speed switching.	
C9	Special Shadow Handling	OEM Specific - Normal Shadow routine.	
CA	Very Early Initialization	OEM Specific – Initialize hardware before any other hardware initialization.	
CB	Reserved	Reserved	
CC	Reserved	Reserved	
CD	Reserved	Reserved	
CE	Reserved	Reserved	
CF	Reserved	Reserved	
D0	Power Management Full speed	Trying to go back or into full speed mode.	
D1	Power Management -- Doze mode	Trying to go or in Doze mode.	
D2	Power Management --Sleep mode	Trying to go or in Sleep mode.	

TABLE I-1: POST Codes (Continued)

POST (hex)	Name	Description
D3	Power Management – Suspend mode	Trying to go or in Suspend mode.
D4	Debug	Available POST codes for use by source code customers during development.
D5	Debug	Available POST codes for use by source code customers during development.
D6	Debug	Available POST codes for use by source code customers during development.
D7	Debug	Available POST codes for use by source code customers during development.
D8	Debug	Available POST codes for use by source code customers during development.
D9	Debug	Available POST codes for use by source code customers during development.
DA	Debug	Available POST codes for use by source code customers during development.
DB	Debug	Available POST codes for use by source code customers during development.
DC	Debug	Available POST codes for use by source code customers during development.
DD	Debug	Available POST codes for use by source code customers during development.
DE	Debug	Available POST codes for use by source code customers during development.
DF	Debug	Available POST codes for use by source code customers during development.
E0	Reserved	Reserved
E1	Setup Page	Page 1
E2	Setup Page	Page 2
E3	Setup Page	Page 3
E4	Setup Page	Page 4
E5	Setup Page	Page 5
E6	Setup Page	Page 6
E7	Setup Page	Page 7
E8	Setup Page	Page 8
E9	Setup Page	Page 9
EA	Setup Page	Page 10
EB	Setup Page	Page 11
EC	Setup Page	Page 12
ED	Setup Page	Page 13
EE	Setup Page	Page 14
EF	Shadow Error	In POST 6 to signal a Shadow Error.
F0	Reserved	Reserved
F1	Reserved	Reserved
F2	Reserved	Reserved
F3	Reserved	Reserved
F4	Reserved	Reserved

TABLE I-1: POST Codes (Continued)

POST (hex)	Name	Description
F5	Reserved	Reserved
F6	Reserved	Reserved
F7	Reserved	Reserved
F8	Reserved	Reserved
F9	Reserved	Reserved
FA	Reserved	Reserved
FB	Reserved	Reserved
FC	Reserved	Reserved
FD	Reserved	Reserved
FE	Reserved	Reserved
FF	Boot	The system is now booted or waiting for an OS.

J. EMERGENCY PROCEDURE

Follow this procedure only in case of emergency such as a critical error during the boot block flash BIOS update (when using UBIOS utility program or saving AWARD parameters in flash) or if you meet one of the following symptoms at anytime.

J.1 SYMPTOMS

- No POST code on a power up (when using a POST code card).
- System stops at POST 41h (when using a POST code card; see Table I-1 in previous section), associated beep code is generated (see Table J-2) and the system tries to read from the floppy drive.
- Board does not boot, even after following all the steps indicated in Section 18.3.

J.2 GENERATE AN EMERGENCY FLOPPY DISKETTE

Use a system that has a 1.44 MB floppy drive A.

1. Insert the TEKNOR EMERGENCY diskette in drive A:
2. Copy the two files WDISK.COM and EMERDISK.TEK from drive A: to your hard drive (those files are available in your TEKNOR diskette package).
3. Remove the TEKNOR EMERGENCY diskette
4. Format a diskette in drive A:.
5. At the DOS prompt of your hard drive (the same directory as the two files WDISK.COM and EMERDISK.TEK), type WDISK and then press Enter.

The program may display one of the following messages:

"Emergency Code transferred"
The emergency diskette has been successfully created.

Take the appropriate actions and restart from step 4 if you see the following messages:

"Write to disk failure!"
Verify if your floppy diskette is write-protected.

"The file to program in flash was not found"
Be sure that EMERDISK.TEK file is in your current directory.

"Unable to read the binary file" or **"Unable to close the opened file"**
Possible floppy diskette corruption or bad data transfer between floppy disk and host system.

"Unable to allocate a memory block of 256 Kbytes"
Not enough memory to run the WDISK program.

J.3 EMERGENCY PROCEDURE

Running an EMERGENCY PROCEDURE.

1. Remove battery jumper W13 even if it is set to onboard or offboard.
2. Install the EMERGENCY diskette in the floppy drive A (1.44 MB) connected to the PCI-941 board.
3. Power on the board. (Nothing appears on the screen.)
4. Boot block flash update will be completed when you see POST code 55 (when using a POST code card; see Table J-1) or hear the associated beep code (see Table J-2) or when the floppy drive stops. If you see POST code 22, 33 or 44, an error has occured. You should repeat the emergency procedure. If repeated attempts at updating the boot block flash fail, that is, you are unable to generate POST code 55, contact the TEKNOR Technical Support department.
5. After the procedure is successfully completed, power down the board, set your battery jumper as it was previously and power up the board. Your PCI-941 boot block flash BIOS should be correctly programmed and the system should run properly.

NOTE

If the emergency disk has been lost, see section J.2: Generate an Emergency Floppy Diskette.

TABLE J-1: Emergency Procedure POST Codes

Post Code	Description
xx	Post code counter displaying emergency file block number loaded from floppy.
11	Begin the flash reprogramming process.
22	Error when getting the boot block flash ID code.
33	Error when erasing the boot block flash.
44	Error when programming the boot block flash.
55	Success of the boot block recovery code .

TABLE J-2: Emergency Procedure Beep Codes

Post Code	Beepcode	Description
41	**-*	Enterring the boot block recovery code (i.e. Main BIOS checksum error).
22	*-*-*	Error when getting the boot block flash ID code.
33	*-*-*-*	Error when erasing the boot block flash.
44	*-*-*-*-*	Error when programming the boot block flash.
55	*-*	Success of the boot block recovery code. The board is ready to be manually reset.

* 1 Beep code
\- Silence

GETTING HELP

At TEKNOR we take great pride in our customer's successes. We strongly believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, you may contact our Technical Support department at:

CANADIAN HEADQUARTERS	EUROPEAN REGIONAL OFFICE
Tel.: (450) 437-5682	Tel.: +49 811 / 600 15-0
Fax: (450) 437-8053	Fax: +49 811 / 600 15-33

If you have any questions about TEKNOR, our products or services, you may reach us at the above numbers or by writing to:

TEKNOR INDUSTRIAL COMPUTERS INC.	TEKNOR INDUSTRIAL COMPUTERS INC.
616 Cure Boivin	**Zeppellin Str. 4**
Boisbriand, Quebec	**D-85399 Hallbergmoos**
J7G 2A7 CANADA	**GERMANY**

LIMITED WARRANTY

TEKNOR INDUSTRIAL COMPUTERS INC. ("the seller") warrants its boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

Returning Defective Merchandise

If your TEKNOR product malfunctions, please do the following before returning any merchandise:

1) Call our Technical Support department in Canada at (450) 437-5682 or in Germany at +49 811 / 600 15-0. Make certain you have the following at hand: the TEKNOR Invoice #, your Purchase Order #, and the Serial Number of the defective board.

2) Give the serial number found on the back of the board and explain the nature of your problem to a service technician.

3) If the problem cannot be solved over the telephone, the technician will further instruct you on the return procedure.

4) Prior to returning any merchandise, make certain you receive an RMA # from TEKNOR's Technical Support and clearly mark this number on the outside of the package you are returning. To request a number, follow these steps: make a copy of the request form on the following page, fill it out and fax it to us.

5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. **Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.**

6) When returning a TEKNOR board:

   i) Make certain that the board is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.

   ii) Ship prepaid to (but not insured, since incoming units are insured by TEKNOR):

TEKNOR INDUSTRIAL COMPUTERS INC.	**TEKNOR INDUSTRIAL COMPUTERS INC.**
616 Cure Boivin	**Zeppellin Str. 4**
Boisbriand, Quebec	**D-85399 Hallbergmoos**
J7G 2A7 CANADA	**GERMANY**

TEKNOR
INDUSTRIAL COMPUTERS INC.

RETURN TO MANUFACTURER AUTORIZATION REQUEST

Contact Name: _____

Company Name: _____

Street Address: _____

City: _____ **Province / State:** _____

Country: _____ **Postal / Zip Code:** _____

Phone Number: _____ **Fax Number:** _____

Extension: _____

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

ref.: RMA-02

Fax this form to TEKNOR's Technical Support department in Canada at (450) 437-8053 or in Germany at +49 811 / 600 15-33