

ROCKY-3706EV/EVG
Socket-370 Base CPU Board with
10/100Mb LAN, VGA & Gigabit LAN(EVG)
Ver1.1

Manual Revision 1.1
Jul 5, 2002

@Copyright 2001

All Rights Reserved.

Manual first edition Jan 14, 2001

The information in this document is subject to change without prior notice in order to improve reliability, design and function and does not represent a commitment on the part of the manufacturer.

In no event will the manufacturer be liable for direct, indirect, special, incidental, or consequential damages arising out of the use or inability to use the product or documentation, even if advised of the possibility of such damages.

This document contains proprietary information protected by copyright. All rights are reserved. No part of this manual may be reproduced by any mechanical, electronic, or other means in any form without prior written permission of the manufacturer.

Trademarks

ROCKY-3706EV/EVG is registered trademarks of ICP Electronics Inc., IBM PC is a registered trademark of International Business Machines Corporation. Intel is a registered trademark of Intel Corporation. AMI is registered trademarks of American Megatrends Inc. , Other product names mentioned herein are used for identification purposes only and may be trademarks and/or registered trademarks of their respective companies.

Contents

1. Introduction	5
1.1 Specifications.....	6
1.2 What You Have.....	7
2. Installation	8
2.1 ROCKY-3706EV/EVG Layout.....	9
2.2 Clear CMOS Setup	10
2.3 On Board VGA Setup.....	10
3. Connection.....	11
3.1 Floppy Disk Drive Connector	11
3.2 PCI E-IDE Disk Drive Connector	12
3.3 Parallel Port	13
3.4 USB Port Connector	14
3.5 Power Button Switch.....	14
3.6 Serial Ports	15
3.7 Keyboard/Mouse Connector	15
3.8 Fan Connector	17
3.9 VGA Connector.....	17
3.10 ATX Connector	18
3.11 External Switches and Indicators	19
3.12 PS-ON Connector	19
3.13 LAN RJ45 Connectors	20

3.14	External LED Connector	21
------	------------------------------	----

4. BIOS Setup..... 22

4.1	Introduction	22
4.2	Starting Setup	22
4.3	Setup Summary	23
4.4	Main Menu	23
4.5	Advanced Menu	24
4.6	Chipset Menu.....	30
4.7	PCIPnP Menu	32
4.8	Power Menu	34
4.9	Boot Menu	35
4.10	Security Menu	37
4.11	Exit Menu	38

Appendix A. Watch Dog Timer.....	39
Appendix B. E ² Key™ Function	41
Appendix C. Address Mapping.....	42
Appendix D. ATX Power Supply	44



Introduction

The ROCKY-3706EV/EVG ATX/AT main board is a high-performance computer mainboard based on RCC[®] LE-T / LC-T chipset. The ROCKY-3706EV/EVG is designed for Socket370 base processor for high-performance server markets.

The Champion's North Bridge "CNB30" provide an integrated high-performance main memory subsystem, a dual PCI bus bridge that provides a high-performance data flow path between the Processor bus and 64-bit PCI Bus, and a 32-bit PCI Bus.

The LE-T / LC-T is a Socket-370 system logic north bridge with the addition of 133 MHz capability for both the CPU and registered SDRAM interfaces. LE-T / LC-T may be used to implement desktop personal computer systems from 100MHz to 133MHz based on Socket-370 (Pentium[®] III processor). The primary features of the CNB30-North Bridge are: Socket-370 CPU (Front Side Bus) Interface (100 / 133MHz), registered SDRAM Memory Interface (100 / 133MHz), 64bitPCI Bus Interface (33/66MHz), 32bitPCI Bus Interface (33MHz).

***** If PCI BUS run in 66MHz*****

The ROCKY-3706EV/EVG V1.0 only one PCI card support, ROCKY-3706EV V1.1 is support two PCI card.

1.1 Specifications :

- Intel® Pentium® III (FC-PGA), Pentium® III Tualatin(FC-PGA2), & Celeron (FSB: **Support 100/133MHz**)
- **Bus:** PICMG Bus(Support PCI Master x 4)
- **DMA channels:** 7
- **Interrupt levels:** 15
- **Chipset:** RCC LE-T+CSB4
- **RAM memory:** Two 168-pin DIMM sockets support REGISTERED SDRAM only. The max memory is up to 2GB. Support ECC(Error Code Correct) function
- **Ultra ATA33 IDE Interface :** Two PCI Enhance IDE hard drives. The south bridge CSB4 supports Ultra ATA33 IDE interface.
- **Floppy disk drive interface :** Supports 2.88 MB, 1.44MB, 1.2MB, 720KB, or 360KB floppy disk drive.
- **Two high speed Series ports :** NS16C550 compatible UARTs
- **Bi-directional Parallel Port :** IEEE1284 compatible
- **IrDA port :** Support Serial Infrared(SIR) and Amplitude Shift Keyed IR(ASKIR) interface.
- **USB port :** Support two USB ports for future expansion.
- **VGA Controller :** ATi RageXL VGA controller, 8MB main memory . Screen Resolution : up to 1600x1200 in 8-bit Color at 85Hz refresh.
- **Intel 82559 Fast Ethernet Multifunction PCI Controller :** IEEE 802.3u Auto-Negotiation support for 10BASE-T/100BASE-TX standard. Fast back-to-back transmission support with minimum interframe spacing. Connected to your LAN through RJ45 connector.
- **Broadcom Gigabit LAN 64bit PCI Controller :** BCM5701 is an up to gigabit of Ethernet Controller for the PCI bus. Can support full duplex 10/100/1000Mb/s transmission and reception. Connected to your LAN through RJ45 connector.
- **Keyboard connector & PS/2 Mouse** Port on-board
- **Operating Temperature :** 0° ~ 55° C (CPU needs Cooler)

1.2 What You Have

In addition to this *User's Manual*, the ROCKY-3706EV/EVG package includes the following items:

- ROCKY-3706EV/EVG Single Board Computer x1
- RS-232/Print Cable x 1
- FDD Cable x 1
- IDE HDD Cable x 1
- CD-ROM Driver x 1
- Y Cable x 1

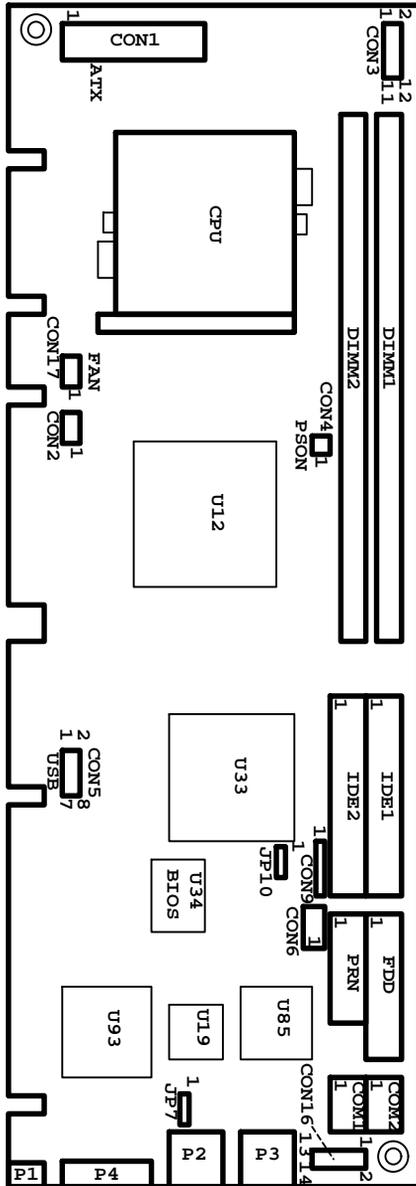
If any of these items is missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.

2

Installation

This chapter describes how to install the ROCKY-3706EV/EVG. At first, the layout of ROCKY-3706EV/EVG is shown, and the unpacking information that you should be careful is described. The jumpers and switches setting for the ROCKY-3706EV/EVG configuration, such as CPU type selection, system clock setting, and watchdog timer, are also included.

2.1 ROCKY-3706EV/EVG Layout



2.2 Clear CMOS Setup

If want to clear the CMOS Setup(for example forgot the password, you should clear the CMOS and then set the password again.), you should close the JP10 (2-3) for about 3 seconds, then open again. This will set back to normal operation mode.

- **JP10 : Clear CMOS Setup**



1 2 3

JP10	DESCRIPTION
1-2 (default)*	Keep CMOS Setup (Normal Operation)
Short 2-3	Clear CMOS Setup

2.3 On Board VGA Setup

If want to disabled the on board VGA chipset, you should close the JP7 (2-3).

- **JP7 : VGA Setup**



1 2 3

JP7	DESCRIPTION
1-2 (default)*	On Board VGA is Enabled (Normal Operation)
Short 2-3	On Board VGA is Disabled

3

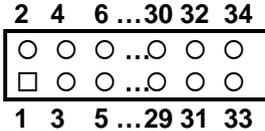
Connection

This chapter describes how to connect peripherals, switches and indicators to the ROCKY-3706EV/EVG board.

3.1 Floppy Disk Drive Connector

ROCKY-3706EV/EVG board is equipped with a 34-pin daisy-chain driver connector cable.

- **CON7 : FDC CONNECTOR**



PIN	DESCRIPTION	PIN	DESCRIPTION
1	GROUND	2	REDUCE WRITE
3	GROUND	4	N/C
5	GROUND	6	N/C
7	GROUND	8	INDEX#
9	GROUND	10	MOTOR ENABLE A#
11	GROUND	12	DRIVE SELECT B#
13	GROUND	14	DRIVE SELECT A#
15	GROUND	16	MOTOR ENABLE B#
17	GROUND	18	DIRECTION#
19	GROUND	20	STEP#
21	GROUND	22	WRITE DATA#
23	GROUND	24	WRITE GATE#
25	GROUND	26	TRACK 0#
27	GROUND	28	WRITE PROTECT#
29	N/C	30	READ DATA#
31	GROUND	32	SIDE 1 SELECT#
33	N/C	34	DISK CHANGE#

3.2 PCI E-IDE Disk Drive Connector

You can attach four IDE(Integrated Device Electronics) device.

CON13 (IDE1) : Primary IDE Connector

CON14 (IDE2) : Secondary IDE Connector

- **CON13/CON14 : IDE Interface Connector**

2 4 6 ..36 38 40



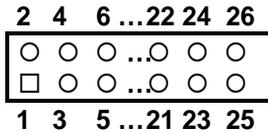
1 3 5 ..35 37 39

PIN	DESCRIPTION	PIN	DESCRIPTION
1	RESET#	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	N/C
21	DRQ	22	GROUND
23	IOW#	24	GROUND
25	IOR#	26	GROUND
27	CHRDY	28	REV. PULL LOW
29	DACK	30	GROUND-DEFAULT
31	INTERRUPT	32	N/C
33	SA1	34	N/C
35	SA0	36	SA2
37	HDC CS0#	38	HDC CS1#
39	HDD ACTIVE#	40	GROUND

3.3 Parallel Port

This port is usually connected to a printer, The ROCKY-3706EV/EVG includes an on-board parallel port, accessed through a 26-pin flat-cable connector CON8.

• **CON8 : Parallel Port Connector**



PIN	DESCRIPTION	PIN	DESCRIPTION
1	STROBE#	2	DATA 0
3	DATA 1	4	DATA 2
5	DATA 3	6	DATA 4
7	DATA 5	8	DATA 6
9	DATA 7	10	ACKNOWLEDGE
11	BUSY	12	PAPER EMPTY
13	PRINTER SELECT	14	AUTO FORM FEED #
15	ERROR#	16	INITIALIZE
17	PRINTER SELECT LN#	18	GROUND
19	GROUND	20	GROUND
21	GROUND	22	GROUND
23	GROUND	24	GROUND
25	GROUND	26	NC

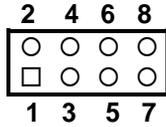
3.4 USB Port Connector

The ROCKY-3706EV/EVG built in two USB(Spec. 1.1) ports for the future new I/O bus expansion.

CON5 : 2 ports USB Connector

Pin 1,3,5,7 for USB 1

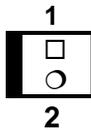
Pin 2,4,6,8 for USB 0



PIN	DESCRIPTION	PIN	DESCRIPTION
1.	VCC	2.	GROUND
3.	DATA1-	4.	DATA0+
5.	DATA1+	6.	DATA0-
7.	GROUND	8.	VCC

3.5 Power Button Switch

CON4 : 2 Pin Power Button Switch



PIN	DESCRIPTION
1	ATX SW PIN 1
2	ATX SW PIN 2

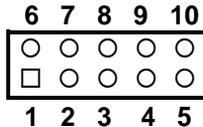
3.6 Serial Ports

The ROCKY-3706EV/EVG offers two high speed NS16C550 compatible UARTs with 16 byte Read/Receive FIFO serial ports.

CON12 : COM1

CON10 : COM2

- **CON12/CON10 : Serial Port 10-pin Connector**



PIN	DESCRIPTION
1	DATA CARRIER DETECT (DCD)
2	RECEIVE DATA (RXD)
3	TRANSMIT DATA (TXD)
4	DATA TERMINAL READY (DTR)
5	GROUND (GND)
6	DATA SET READY (DSR)
7	REQUEST TO SEND (RTS)
8	CLEAR TO SEND (CTS)
9	RING INDICATOR (RI)
10	N/C

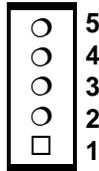
3.7 Keyboard/Mouse Connector

The ROCKY-3706EV/EVG provide 6-pin DIN keyboard/mouse connector and 5-pin keyboard connector..

- **P1 : 6-pin DIN Keyboard/Mouse Connector**

PIN	DESCRIPTION
1	KEYBOARD DATA
2	MOUSE DATA
3	GROUND
4	+5V
5	KEYBOARD CLOCK
6	MOUSE CLOCK

CON6 : 5-pin External Keyboard Connector

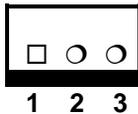


PIN	DESCRIPTION
1	KEYBOARD CLOCK
2	KEYBOARD DATA
3	NC
4	GROUND
5	+5V

3.8 Fan Connector

The ROCKY-3706EV/EVG provides CPU with cooling fan connector. The connectors can supply 12V/500mA to the cooling fan. There is a “rotation” pin in fan connector. This rotation pin is to get the fan’s rotation signal to system. So the system BIOS could recognize the fan speed. Please be noted that only specific fan offers the rotation signal.

- **CON17 : CPU Fan Connector**



PIN NO.	CPU FAN
1	Ground
2	12V
3	Rotation Signal

3.9 VGA Connector

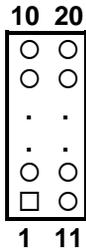
- **P4 : 15-pin Female Connector**

PIN	DESCRIPTION	PIN	DESCRIPTION
1	RED	2	GREEN
3	BLUE	4	NC
5	GROUND	6	GROUND
7	GROUND	8	GROUND
9	VCC / NC	10	GROUND
11	NC	12	DDC DAT
13	HSYNC	14	VSYNC
15	DDCCLK		

3.10 ATX Connector

The ROCKY-3706EV/EVG/EVF/EV offers one standard ATX power connector

- **CON1: 20-pin Connector**

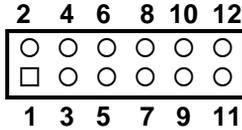


PIN	DESCRIPTION
1	NC
2	NC
3	GND
4	+5V
5	GND
6	+5V
7	GND
8	Power Good
9	+5V SB
10	+12V
11	NC
12	-12V
13	GND
14	PSON#
15	GND
16	GND
17	GND
18	-5V
19	+5V
20	+5V

3.11 External Switches and Indicators

There are several external switches and indicators for monitoring and controlling your CPU board. All the functions are in the CN23 connector.

CON3 Pin Assignment and Functions :

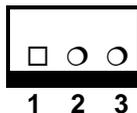


FUNCTION	PIN	DESCRIPTION	
SPEAKER	2	SPK SIGNAL	Jump for Buzzer
	4	N/C	
	6	N/C	
	8	VCC	
RESET	10	RESET	
	12	GROUND	
HDD LED	9	LED+	
	11	LED-	
POWER LED	1	LED+	
	3	LED-(GROUND)	
Reserved	5	Reserved	
	7	GROUND	

3.12 PS-ON Connector

This connector is used to control the ATX power supply.

- **CON2 : PS-ON Connector (refer to Appendix D for detail)**



PIN	DESCRIPTION
1	Ground
2	PS-ON
3	+5V Standby

3.13 LAN RJ45 Connector

ROCKY-3706EV/EVG is equipped with Ethernet Controllers (Intel 82559 10/100Mbps and Broadcom BCM5701 Gigabit for ROCKY-3706EVG only). You can connect it to your LAN through RJ45 LAN connector. The pin assignments are as follows:

- **P2 LAN1 RJ45 Connector (10/100)**

PIN	DESCRIPTION	PIN	DESCRIPTION
1	TX+	7	N/C
2	TX-	8	N/C
3	RX+	9	Speed +
4	N/C	10	Speed -
5	N/C	11	Active/LINK +
6	RX-	12	Active/LINK -

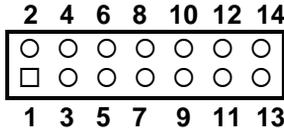
- **P3 LAN2 RJ45 Connector (Giga LAN ROCKY-3706EVG only)**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	TA+	7	TD+
2	TA-	8	TD-
3	TB+	9	Speed 1000M+
4	TC+	10	Speed 1000M-
5	TC-	11	Active +
6	TB-	12	Active -

3.14 External LED Connector

The LED connector includes Ethernet Link/Active LED, Ethernet speed LED.

CON16 External LED Connector



LED +	LED -	LED Function
2	1	LAN 2 Speed LED (1000M)
4	3	LAN 2 Speed LED (100M)
6	5	LAN 2 Speed LED (10M)
8	7	LAN 2 Active LED
10	9	LAN 1 Speed LED
12	11	LAN 1 Link LED
14	13	LAN 1 Active LED

4

BIOS Setup

4.1 Introduction

This chapter discusses the Setup program built into the BIOS. The Setup program allows users to configure the system. This configuration is then stored in battery-backed CMOS RAM so that it retains the Setup information while the power is off.

4.2 Starting Setup

The BIOS is immediately active when you turn on the computer. While the BIOS is in control, the Setup program can be activated in one of two ways:

1. By pressing immediately after switching the system on, or
2. by pressing the key when the following message appears briefly at the bottom of the screen during the POST (Power On Self-Test).

Press DEL to run SETUP.

4.3 Setup Summary

Main

Set the Time & Date.

Advanced

SuperIO, IDE, Floppy, Boot configuration & System Health

Chipset

No setting needed or don't change is recommended.

Power

Change power management.

Boot

Reconfigure default boot order settings.

Security

Set Supervisor & User passwords.

Exit

Save, exit & load default setting.

4.4 Main Menu Selections

BIOS SETUP UTILITY	
Main	Advance Chipset PCIPnP Power Boot Security Exit
AMIBIOS Version :	07.00.xx
BIOS Build Date :	11/02/01
BIOS ID :	0AAXG011
Processor Type :	Pentium III (tm)
Processor Speed :	1000MHz
System Memory :	1024MB
System Time	[20:32:40]
System Date	[Mon 12/10/2001]
	→ ® Select Screen - - Select Item +- Change Field Tab Select Field F1 General Help F10 Save and Exit ESC Exit
v02.03 (C)Copyright 1985-2000, American Megatrends Inc.	

Figure 1: The Main Menu

4.5 Advanced Menu Selections

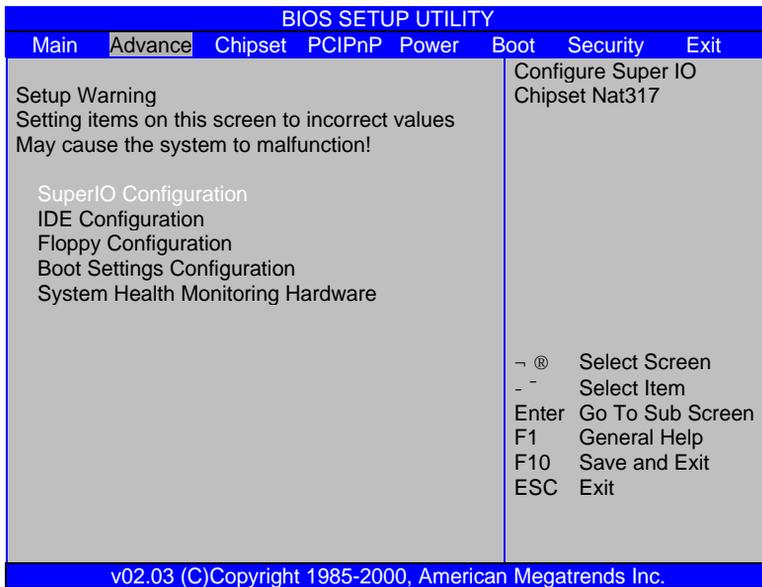


Figure 2.1: The Advance Menu

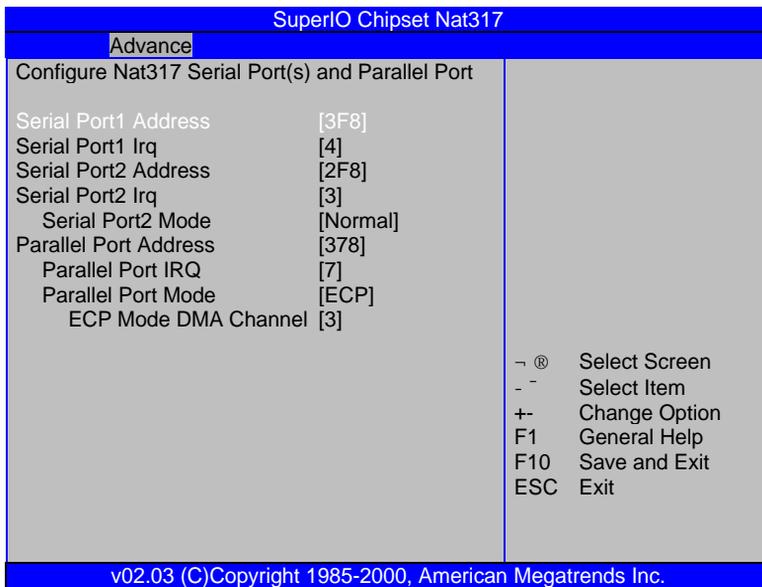


Figure 2.2: The Advance/SuperIO Menu

OnBoard Parallel Port

This option specifies the base I/O port address of parallel port on the motherboard. The settings are Disabled, 378h, 278h, or 3BCh.

Parallel Port Mode

This option specifies the parallel port mode. The settings are Normal, Bi-Dir, EPP, ECP.

Normal

The normal parallel port mode is used.

Bi-Dir

Use this setting to support bidirectional transfers on the parallel port.

EPP

The parallel port can be used with devices that adhere to the Enhanced Parallel Port(EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.

ECP

The parallel port can be used with devices that adhere to the Entended Capabilities Port(ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits per second. ECP provides symmetric bidirectional communication.

Parallel Port IRQ

This option specifies the IRQ used by the parallel port. The settings are (IRQ)5, (IRQ)7.

Parallel Port DMA Channel

This option is only available if the setting for the Parallel Port Mode option is ECP. This option sets the DMA channel used by the parallel port. The settings are DMA Channel 0, 1,2, or 3.

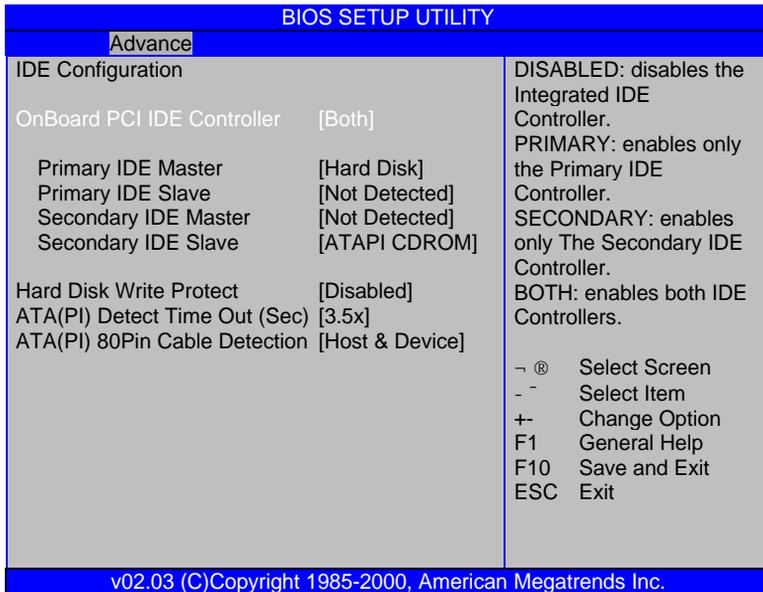


Figure 2.3: The Advance/IDE Menu

Primary/Secondary Master/Slave IDE

Select these options to configure the drive named in the option. Select Auto Detect IDE to let AMIBIOS automatically configure the drive. A screen with a list of drive parameters appears. Click on OK to configure the drive.

Primary/Secondary Master/Slave LBA Mode

LBA(Logical Block Addressing) is a new IDE HDD accessing method to overcome the 528 megabyte capacity bottle neck. If your IDE hard disk over 528MB, AMIBIOS can enable this LBA mode feature. The option only for Primary Master IDE LBA mode.

Primary/Secondary Master/Slave Block Mode

If your hard disk drive supports IDE block transfer mode, enable this option for faster IDE hard disk drive transfer rate. The option only for Primary Master Block mode.

Primary/Secondary Master/Slave 32Bit Mode

This option enables Primary Master IDE 32-bit data transfers on the IDE data port. If disabled,16-bit data transfer is used by the BIOS.32-bit data transfers can only be enabled if IDE prefetch mode is also enabled.

Primary/Secondary Master/Slave PIO Mode

This option enables Primary Master IDE PIO mode on the IDE may have to set to proper cycle timings. Cycle timing relation between the IDE PIO mode value and IDE cycle timing is shown below

Mode 0 -> Timing (600ns)

Mode 1 -> Timing (383ns)

Mode 2 -> Timing (240ns)

Mode 3 -> Timing (180ns)

Mode 4 -> Timing (120ns)

Mode 5 -> Timing (60ns)

Primary/Secondary Master/Slave ARMD Emulated Type

If set to Auto, the default emulation type depends on ARMD drive. The default emulation type is Floppy for LS120, Hard Disk for MO, Hard Disk for IOMEGA Zip.

The settings are Auto, Floppy, Hard Disk.

S.M.A.R.T. for Hard Disks

Self-Monitoring, Analysis and Reporting Technology. This option can help BIOS to warn the user of the possible device failure and give user a chance to back up the device before actual failure happens.

The settings are Auto, Disabled, Enabled.

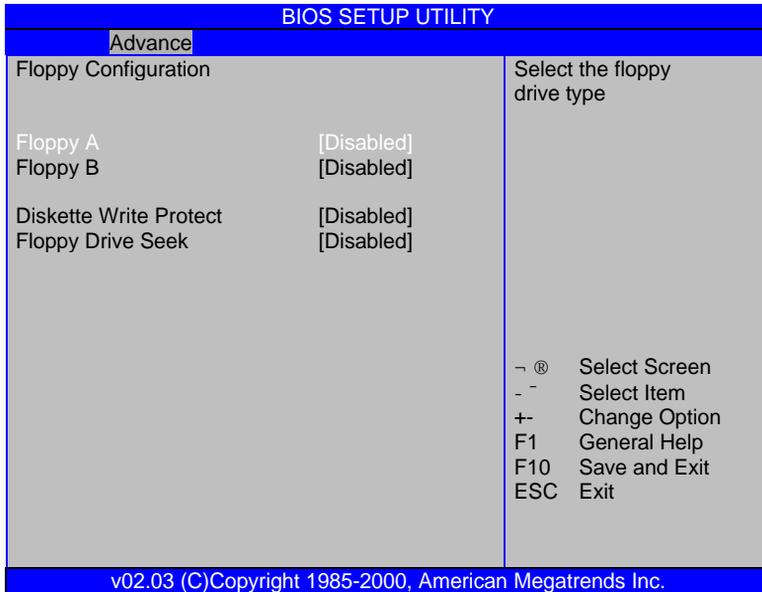


Figure 2.4: The Advance/Floppy Menu

Floppy A, B

Move the cursor to these fields via and select the floppy type.

Floppy Write Protect

This option specifies the read/write access that is set when booting from a floppy drive.

The settings are Enable or Disabled.

Floppy Drive Seek

Set this option to Enabled to specify that floppy drives A: will perform a Seek operation at system boot. The settings are Enabled or Disabled.

BIOS SETUP UTILITY		
Advance		
Boot Settings Configuration		Allows BIOS to skip certain tests while booting. This will decrease the time needed to boot the system.
Quick Boot	[Enabled]	
Quiet Boot	[Disabled]	
AddOn ROM Display Mode	[Force BIOS]	
Bootup Num-Lock	[On]	
BootUp CPU Speed	[High]	
PS/2 Mouse Support	[Enabled]	
Typematic Rate	[Fast]	
System Keyboard	[Present]	
Primary Display	[VGA/EGA]	
Parity Check	[Disabled]	
Boot To OS/2	[No]	
Wait For ' F1' If Error	[Enabled]	
Hit ' DEL' Message Display	[Enabled]	
Processor Serial Number	[Disabled]	
Internal Cache	[Write-Back]	
System BIOS Cacheable	[Enabled]	
		↵ ® Select Screen - - Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit
v02.03 (C)Copyright 1985-2000, American Megatrends Inc.		

Figure 2.5: The Advance/Boot Menu

Quick Boot

When set to enable, DRAM testing function will disable.

BootUp Num-Lock

When On, this option turns off Num Lock when the system is powered on so the end user can use the arrow keys on both the numeric keypad and the keyboard.

BootUp CPU Speed

This option sets the speed of the CPU at system boot time. options. The settings are Low or High.

PS/2 Mouse Support

When this option is enabled, BIOS support a PS/2- type mouse.

Typematic Rate

Typematic Rate sets the rate at which characters on the screen repeat when a key is pressed and held down. The settings are Slow, Fast.

System Keyboard

This option does not specify if a keyboard is attached to the computer. Rather, it specifies if error messages are displayed if a keyboard is not attached. This option permits you to configure workstation with no keyboard. The settings are Absent, Present.

Primary Display

Select this option to configure the type of monitor attached to the computer. The settings are Monochrome, Color 40x25, Color 80x25, VGA/PGA/EGA, or Not Install.

Parity Check

Set this option to Enabled to check the parity of all system memory. The settings are Disabled or Enabled.

Boot To OS/2

Set this option to Enabled if running OS/2 operating system and using more than 64MB of system memory on the motherboard. The settings are Disabled or Enabled.

Wait For 'F1' If Error

If this option is enabled, AMIBIOS waits for the end user to press <F1> before continuing. If this option is disabled, AMIBIOS continues the boot process without waiting for <F1> to be pressed. The settings are Disabled or Enabled.

Hit 'DEL' Message Display

Disabling this option prevents "Hit if you want to run Setup" from appearing when the system boots. The settings are Disabled or Enabled.

Internal Cache

The option enabled or disabled the internal cache memory in the processor.

System BIOS Cacheable

When this option is set to enabled, the System ROM area from F0000-FFFFFF is copied (shadowed) to RAM for faster execution.

BIOS SETUP UTILITY	
Advance	
System Health Monitoring	
Current CPU Temp.	0° C/32° F
Current CPU Fan Speed	0MPR
CPU VID	1.70V
3.3VSTBY	3.300 V
3.3V Vcc	3.300 V
+5V	5.000 V
Vcore	1.720 V
+12V	12.000 V
Vtt	1.500 V
2.5V	2.500 V
-12V	-12.00 V
	→ ® Select Screen
	- - Select Item
	F1 General Help
	F10 Save and Exit
	ESC Exit
v02.03 (C)Copyright 1985-2000, American Megatrends Inc.	

Figure 2.6: The Advance/Health Menu

4.6 Chipset Menu Selections

BIOS SETUP UTILITY							
Main	Advance	Chipset	PCIPnP	Power	Boot	Security	Exit
C000,16K Shadow			[Cached]				
C400,16K Shadow			[Cached]				
C800,16K Shadow			[Disabled]				
CC00,16K Shadow			[Disabled]				
D000,16K Shadow			[Disabled]				
D400,16K Shadow			[Disabled]				
D800,16K Shadow			[Disabled]				
DC00,16K Shadow			[Disabled]				
Memory Scrubbing			[Disabled]				
Memory Timing Control			[Auto]				
ISA IO Cycle Delay			[FULL Delay]				
MSP 1.4 Support			[Enabled]				
CPU Clock to FSB Ratio			[4.0x]				
					↵	®	Select Screen
					-	-	Select Item
					+-		Change Field
					F1		General Help
					F10		Save and Exit
					ESC		Exit
v02.03 (C)Copyright 1985-2000, American Megatrends Inc.							

Figure 3: The Chipset Menu

C000,16k Shadow

When this option is set to enabled, the Video ROM area from C0000-C7FFF is copied (shadowed) to RAM for faster execution.

Disabled :The contents of the video ROM are not copied to RAM.

Cached :The contents of the video ROM area from C0000h - C7FFFh are copied from ROM to RAM and can be written to or read from cache memory.

Enabled :The contents of the video ROM area from C0000h - C7FFFh are copied (shadowed) from ROM to RAM for faster execution.

C400,16k Shadow

These options enable shadowing of the contents of the ROM area named in the option title. The settings are Enable Disable, Cached.

The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards.

C800,16k Shadow

These options enable shadowing of the contents of the ROM area named in the option title. The settings are Enable Disable, Cached.

The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards.

CC00,16k Shadow

These options enable shadowing of the contents of the ROM area named in the option title. The settings are Enable Disable, Cached.

The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards.

D000,16k Shadow

These options enable shadowing of the contents of the ROM area named in the option title. The

settings are Enable Disable, Cached.

The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards.

D400,16k Shadow

These options enable shadowing of the contents of the ROM area named in the option title. The settings are Enable Disable, Cached.

The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards.

D800,16k Shadow

These options enable shadowing of the contents of the ROM area named in the option title. The settings are Enable Disable, Cached.

The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards.

DC00,16k Shadow

These options enable shadowing of the contents of the ROM area named in the option title. The settings are Enable Disable, Cached.

The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards.

4.7 PCIPnP Menu Selections

BIOS SETUP UTILITY							
Main	Advance	Chipset	PCIPnP	Power	Boot	Security	Exit
Plug & Play O/S			[No]				No: lets the BIOS Configure all the devices in the system.
Reset Config Data			[No]				YES: lets the operating system configure Plug and Play (PnP) devices not Required for boot if Your system has a Plug And Play operating system.
PCI Latency			[64]				
Allocate IRQ to PCI VGA			[Yes]				
Palette Snooping			[Disabled]				
OffBoard PCI/ISA IDE Card			[Auto]				
IRQ3			[Available]				
IRQ4			[Available]				
IRQ5			[Available]				
IRQ7			[Available]				
IRQ9			[Available]				→ ® Select Screen
IRQ10			[Available]				- - Select Item
IRQ11			[Available]				+ - Change Option
IRQ14			[Available]				F1 General Help
IRQ15			[Available]				F10 Save and Exit
DMA Channel 0			[Available]				ESC Exit
DMA Channel 1			[Available]				
v02.03 (C)Copyright 1985-2000, American Megatrends Inc.							

Figure 4.1: The PCIPnP Menu

BIOS SETUP UTILITY							
Main	Advance	Chipset	PCIPnP	Power	Boot	Security	Exit
DMA Channel 3			[Available]				Available: Specified DMA is Available to be used by PCI/PnP devices.
DMA Channel 5			[Available]				Reserved: Specified DMA is reserved for Use by Legacy ISA devices.
DMA Channel 6			[Available]				
DMA Channel 7			[Available]				
Reserved Memory Size			[Disabled]				
							→ ® Select Screen
							- - Select Item
							+ - Change Option
							F1 General Help
							F10 Save and Exit
							ESC Exit
v02.03 (C)Copyright 1985-2000, American Megatrends Inc.							

Figure 4.2: The PCIPnP Menu

Plug and Play O/S

If enable, BIOS will configure only PnP ISA boot devices(i.e. all PnP ISA cards which has boot flag set). And PnP aware OS will configure all other devices. If disable, BIOS will configure all devices.

DMA Channel 0, 1, 3, 5, 6, 7

The option allow you to specify the bus type used by each DMA channel. The settings are PnP or ISA

IRQ3, 4, 5, 7, 9, 10, 11, 14, 15

The option specify the bus that the specified IRQ line is used on. The option allow you to reserve IRQs for legacy ISA adapter cards. The option determine if AMIBIOS should remove an IRQ from the pool of available IRQs passed to devices that are configurable by the system BIOS. The available IRQ pool is determined by reading the ESCD NVRAM. If more IRQs must be removed from the pool, the end user can use the option to reserve the IRQ by assigning an ISA setting to it. Onboard I/O is configured by AMIBIOS. All IRQs used by onboard I/O are confogured as PCI/PnP.

4.8 Power Menu Selections

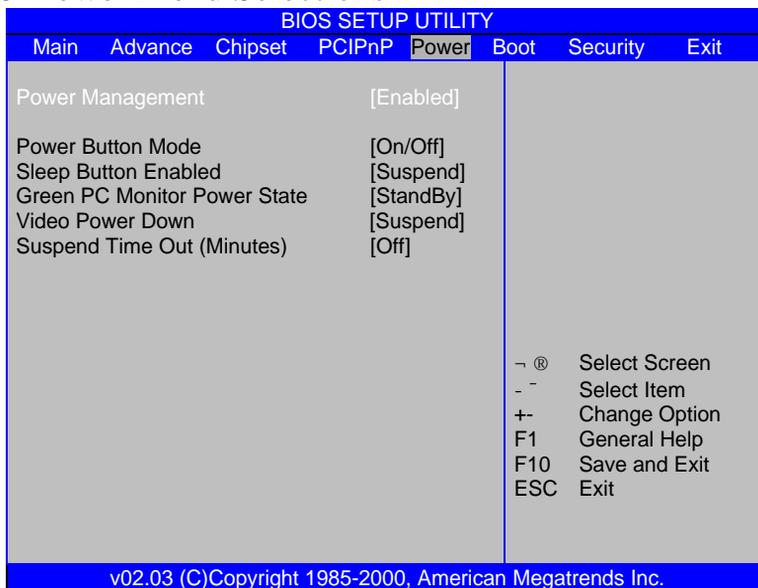


Figure 5: The Power Menu

Power Management

Set this option to Enabled to enable APM (Advanced Power Management).

Green PC Monitor Power State

This option specifies the power state that the green PC-compliant video monitor enters when AMIBIOS places it in a power saving state after the specified period of display inactivity has expired. The settings are Stand By, Suspend, Off.

Video Power Down Mode

Set this option to Enabled to allow the Video adapter and Monitor to be powered down by BIOS.

Suspend Time Out (Minutes)

This option specifies the length of a period of system inactivity while in Standby state. When this length of time expires, the computer enters Suspend power state.

4.9 Boot Menu Selections

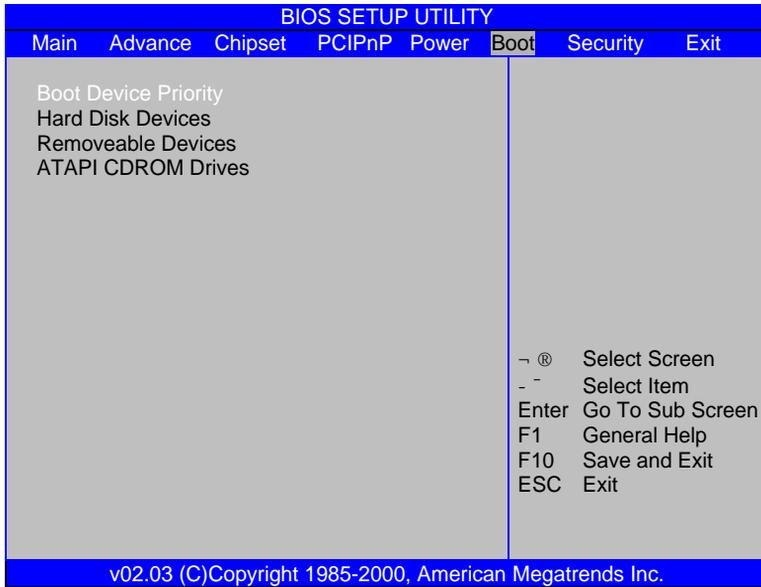


Figure 6.1: The Boot Menu

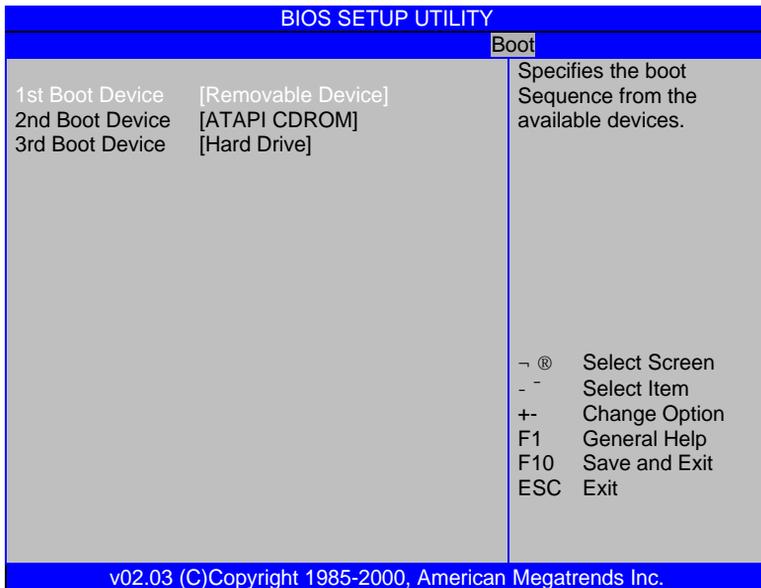


Figure 6.2: The Boot Menu

1st Boot Device

This option sets the type of device for the first boot drives that the AMIBIOS attempts to boot from after AMIBIOS POST completes. The settings are Disabled, IDE-0, IDE-1, IDE-2, IDE-3, Floppy, ARMD-FDD, ARMD-HDD, CDROM, SCSI.

2nd Boot Device

This option sets the type of device for the second boot drives that the AMIBIOS attempts to boot from after AMIBIOS POST completes.

The settings are Disabled, IDE-0, IDE-1, IDE-2, IDE-3, Floppy, ARMD-FDD, ARMD-HDD, CDROM.

3rd Boot Device

This option sets the type of device for the third boot drives that the AMIBIOS attempts to boot from after AMIBIOS POST completes.

The settings are Disabled, IDE-0, IDE-1, IDE-2, IDE-3, Floppy, ARMD-FDD, ARMD-HDD, CDROM.

4th Boot Device

This option sets the type of device for the fourth boot drives that the AMIBIOS attempts to boot from after AMIBIOS POST completes.

The settings are Disabled, IDE-0, IDE-1, IDE-2, IDE-3, Floppy, ARMD-FDD, ARMD-HDD, CDROM.

Try Other Boot Devices

Set this option to Yes to instruct AMIBIOS to attempt to boot from any other drive in the system if it cannot find a boot drive among the drives specified in the 1st Boot Device, 2nd Boot Device, 3rd Boot Device, 4th Boot Device options. The settings are Yes or No.

4.10 Security Menu Selections

BIOS SETUP UTILITY			
Main	Advance	Chipset	PCIPnP Power Boot Security Exit
Supervisor Password :		Not Installed	Install or Change the password.
User Password :		Not Installed	
Change Supervisor Password			
Change User Password			
Clear User Password			
Boot Sector Virus Protection		[Disabled]	
			→ ® Select Screen - - Select Item Enter Go To Sub Screen F1 General Help F10 Save and Exit ESC Exit
v02.03 (C)Copyright 1985-2000, American Megatrends Inc.			

Figure 7: The Security Menu

Boot Sector Virus Protection

When this option is enabled, AMIBIOS issues a warning when any program or virus issues a Disk Format command or attempts to write to the boot sector of the hard disk drive. The settings are Disabled, Enabled.

4.11 Exit Menu Selections

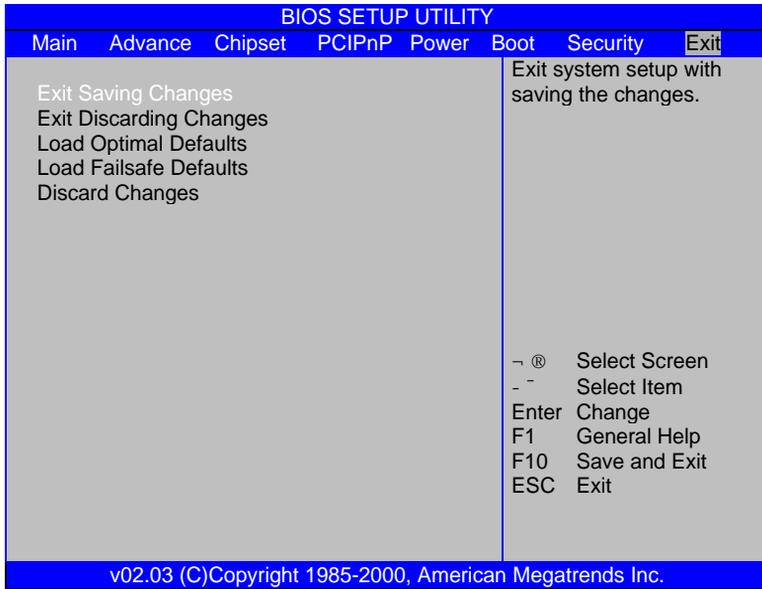


Figure 8: The Exit Menu

Appendix A. Watch-Dog Timer

The WatchDog Timer is a device to ensure that standalone systems can always recover from abnormal conditions that cause the system to crash. These conditions may result from an external EMI or a software bug. When the system stops working, hardware on the board will perform hardware reset (cold boot) to bring the system back to a known state.

Three I/O ports control the operation of WatchDog Timer.

443 (hex)	Write	Set WatchDog Time period
443 (hex)	Read	Enable the refresh the Watchdog Timer.
043/843 (hex)	Read	Disable the Watchdog Timer.

Prior to enable the Watchdog Timer, user has to set the time-out period. The resolution of the timer is 1 second and the range of the timer is from 1 sec to 255 sec. You need to send the time-out value to the I/O port – 443H, and then enable it by reading data from the same I/O port – 443H. This will activate the timer that will eventually time out and reset the CPU board. To ensure that this reset condition won' t occur, the Watchdog Timer must be periodically refreshed by reading the same I/O port 443H. This must be done within the time-out period that is set by the software, please refer to the example program. Finally, we have to disable the Watchdog timer by reading the I/O port -- 843H or 043H. Otherwise the system could reset unconditionally.

A tolerance of at least 5% must be maintained to avoid unknown routines in the operating system (DOS), such as disk I/O that can be very time-consuming. Therefore if the time-out period has been set to 10 seconds, the I/O port 443H must be read within 7 seconds.

Example assembly program:

```
TIMER_PORT = 443H
TIMER_START = 443H
TIMER_STOP = 843H
;;Initial Timer Counter
MOV DX, TIMER_PORT
MOV AL, 8 ;;8 seconds
OUT DX, AL
MOV DX, TIMER_START
IN AL, DX. ;;Start counter
```

```
W_LOOP:
MOV DX, TIMER_STOP
IN AL, DX
MOV DX, TIMER_START
IN AL, DX ;;Restart counter
;;Add Your Appliaction Here
CMP EXIT_AP, 0
JNE W_LOOP
MOV DX, TIMER_STOP
IN AL, DX
;;Exit AP
```

Appendix B. E² Key™ Function

The ROCKY-3706EV/EVG provides an outstanding E²KEY™ function for system integrator. Based on the E²KEY™, you can free to store the ID Code, Password or Critical Data in the 1Kbit EEPROM. Because the EEPROM is nonvolatile memory, you don't have to worry for losing very important data.

Basically the E²KEY™ is based on a 1Kbit EEPROM which is configured to 64 words (from 0 to 63). You could access (read or write) each word at any time.

When you start to use the E²KEY™, you should have the utility in the package. The software utility will include four files as follows,

```
README.DOC  
E2KEY.OBJ  
EKEYDEMO.C  
EKEYDEMO.EXE.
```

The E2KEY.OBJ provides two library functions for user to integrate their application with E²KEY™ function. These library (**read_e2key** and **write_e2key**) are written and compiled in C language. Please check the following statement, then you will know how to implement it easily.

```
unsigned int read_e2key(unsigned int address)
```

```
/* This function will return the E2KEY™s data at address. The address range is from 0 to 63. Return data is one word, 16 bits
```

```
*/void write_e2key(unsigned int address, unsigned data)
```

```
/* This function will write the given data to E2KEY™ at certain address. The address range is from 0 to 63. The data value is from 0 to 0xffff. */
```

To easily start to use the function, please refer to the included EKEYDEMO.C code at first.

Appendix C. Address Mapping

IO Address Map

I/O address Range	Description
000-01F	DMA Controller #1
020-021	Interrupt Controller #1, Master
040-05F	8254 timer
060-06F	8042 (Keyboard Controller)
070-07F	Real time Clock, NMI Mask
080-09F	DMA Page Register
0A0-0BF	Interrupt Controller #2
0C0-0DF	DMA Controller #2
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F2	Core logic programming configuration
0F8-0FF	Math Coprocessor
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2 (LPT3)
2E8-2EF	Serial Port 4
2F8-2FF	Serial Port 2
300-31F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1 (LPT2)
3B0-3BF	Monochrome Display and Printer Adapter (LPT1)
3C0-3CF	Reserved
3D0-3DF	Color/Graphics Monitor Adapter
3E8-3EF	Serial Port 3
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1

1st MB Memory Address Map

Memory address	Description
00000-9FFFF	System memory
A0000-BFFFF	VGA buffer
C0000-C7FFF	VGA BIOS
F0000-FFFFF	System BIOS
1000000-	Extend BIOS

*Default setting

IRQ Mapping Table

IRQ0	System Timer	IRQ8	RTC clock
IRQ1	Keyboard	IRQ9	Available
IRQ2	Cascade to IRQ Controller	IRQ10	Available
IRQ3	COM2	IRQ11	Available
IRQ4	COM1	IRQ12	PS2 mouse
IRQ5	Available	IRQ13	FPU
IRQ6	FDC	IRQ14	Primary IDE
IRQ7	Printer	IRQ15	Secondary IDE

DMA Channel Assignments

Channel	Function
0	Available
1	Available
2	Floppy disk (8-bit transfer)
3	Available
4	Cascade for DMA controller 1
5	Available
6	Available
7	Available

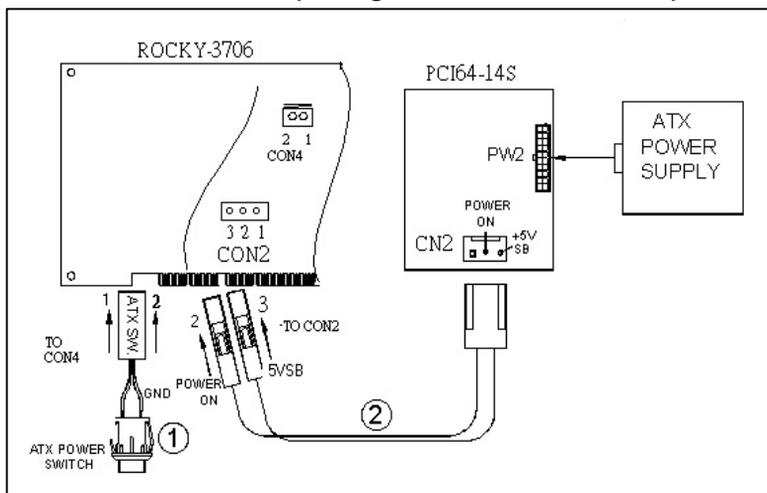
Appendix D. ATX Power Supply

The following notes show how to connect ATX Power Supply to the backplanes and / or the ISBC card.

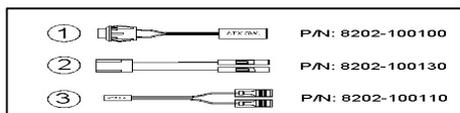
A. For backplanes with ATX Connector

1. Please, disconnect the AC cord of the Power Supply from the AC source to prevent sudden electric surge to the board.
2. Please, check the type of your CPU board. All CPU board listed on the next page support ATX power supply but has two types of power switch connection:

2.1. ROCKY-3706EV/EVG (through Power Button & GND):



Connect the ATX power button switch to the pin 1 (power button) and pin 2 (+5VSB) of CON2 on the board. And connect the power cable from CN2 of backplane to CON2 of CPU card. If you want to turn ON the system, just press the button once. And If you want to turn off the power supply, please press the ATX power switch button for about 4 seconds.



B. For the backplanes with ATX power supply connector

For some SBC without ATX power ON/OFF function, then you can control the ATX power supply through backplane's PS ON connector. Refer to the figure below: for the backplanes with ATX connector, the connection can be made simply as following:

1. Connect the ON/OFF (ordinary one) switch to Pin 2 (PS ON) and Pin 3 (GND) of connector CN2
2. You may now turn the power ON/OFF by the power switch

