

# CP 8xxx Series Quick Reference Guide

## Jumper & Switch Settings

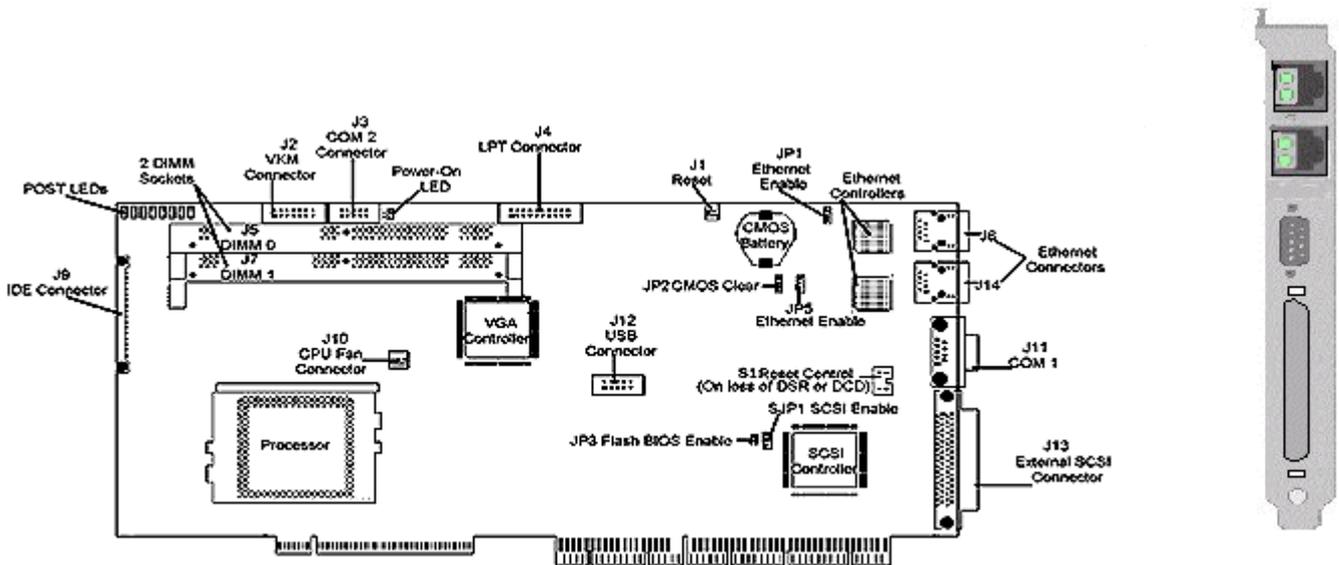


Figure 5  
CP8xxx  
End Bracket

CP 8xxx Series Board Layout & End Bracket  
(Shown with optional External SCSI)

### Switch 1 (S1) Settings

#### S1 - Position 1

The CP8xxx board comes equipped with a 2 position dip switch for reset control. Position 1 is for data set ready (DSR). If position 1 is set in the "on" position (the on and "off" positions are designated by an arrow clearly marked on the switch), the CP8xxx board will reset the CPU on loss of data set ready. The factory default setting for S1, position 1 is in the "off" position.

#### S1 - Position 2

S1, position 2 is for data carrier detect (DCD). If position 2 is set in the "on" position, the CP8xxx board will reset the CPU when there is a loss of carrier. The factory default setting for S1, position 2 is in the "off" position.

Table 1, S1 Switch Settings

Function	1	2

Reset on Loss of DSR	on	
Do Not Reset on Loss of DSR	off	
Reset on Loss of DCD		on
Do Not Reset on Loss of DCD		off
<b>Factory Default</b>	off	off

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## Jumper Settings

The figure above shows the connector, switch and jumper locations on the board.

### JP1 and JP5 - Ethernet

The board is equipped with two integrated Intel 82559 PCI fast Ethernet controllers with two RJ-45 10/100 BASE TX connectors on the mounting bracket at the rear of the board. The I/O addresses and interrupts are set by the PCI plug and play BIOS at boot time. The controllers are enabled or disabled via jumpers JP1 and JP5 (see Figure above for jumper locations).

Jumper	Function	Jumper On Pins 1-2	Jumper On Pins 2-3
JP1	Ethernet	Enabled	Disabled
JP5	Ethernet	Enabled	Disabled

### JP2 - CMOS Clear

The CMOS battery can be cleared by using JP2 (see Figure above for JP2 location). This battery controls the maintenance and storage of three sets of information: (1) the date and time generated and displayed on the computer screen; (2) the peripheral setup, i.e. programming base register for the chip sets; and (3) the password necessary for entry.

The first two sets of information can be changed during boot-up by following specific directions displayed on the computer screen at the time the computer is booting-up. The CMOS battery will automatically update and store the new information input. However, if setup cannot be entered the normal way, CMOS clear is the recovery mechanism which can be used. Or, if password information has been lost, the CMOS will need to be cleared so the information can be updated, before program entry is possible.

To clear CMOS, the jumper must be removed from pins 1 and 2, and placed on pins 2 and 3. After clearing, the jumper must be reinstalled on jumper pins 1 and 2 before updates can be made.

Jumper	Function	Jumper On Pins 1-2	Jumper On Pins 2-3
JP2	CMOS Clear	Normal	CMOS Clear

### JP3 - Flash Bios

If the Flash Bios is to be upgraded, a shunt must be installed on the 2-pin jumper JP3 (see figure above for JP3 location). Upgrades typically come on a floppy disc and are accompanied by upgrade instructions. When the upgrade is complete, the shunt should be removed to protect the system from accidental erasure.

Jumper	Function	Jumper On	Jumper Off

JP3	Flash Write Enable	Enabled	Disabled
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## JP4 - IES Interrupt (IRQ 10)

The IES module communicates with the CP8xxx processors in the subsystem via a hardware interrupt which is IRQ 10. The supervisory interrupt is enabled with JP5. If the CP8xxx board is part of the GlobalVision network, supervisory interrupt is necessary and IES Interrupt must be enabled. If this board is not part of the GlobalVision network, IES Interrupt can be disabled with JP4.

Jumper	Function	Jumper On Pins 1-2	Jumper On Pins 2-3
JP4	IES Interrupt on IRQ 10	Disabled	Enabled

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## Symbios SCSI Controller Jumper Settings

The CP8xxxx board comes equipped to support an internal IDE drive. However, for applications that require external SCSI devices, an integrated Wide Ultra2 SCSI controller (Symbios 53C895) and an external SCSI cable connector (68-pin) can be ordered as an option. This SCSI controller supports both LVD and Single-Ended SCSI devices. The controller is enabled or disabled via a hardware jumper SJP1. (The "S" preceding the "JP" designates the jumper is specific to SCSI functions.)

The SCSI controller is a bus master device which gains control of the PCI bus to transfer data between the CPU memory and the SCSI devices. The I/O base address and interrupts are set by the PCI plug and play BIOS at boot time.

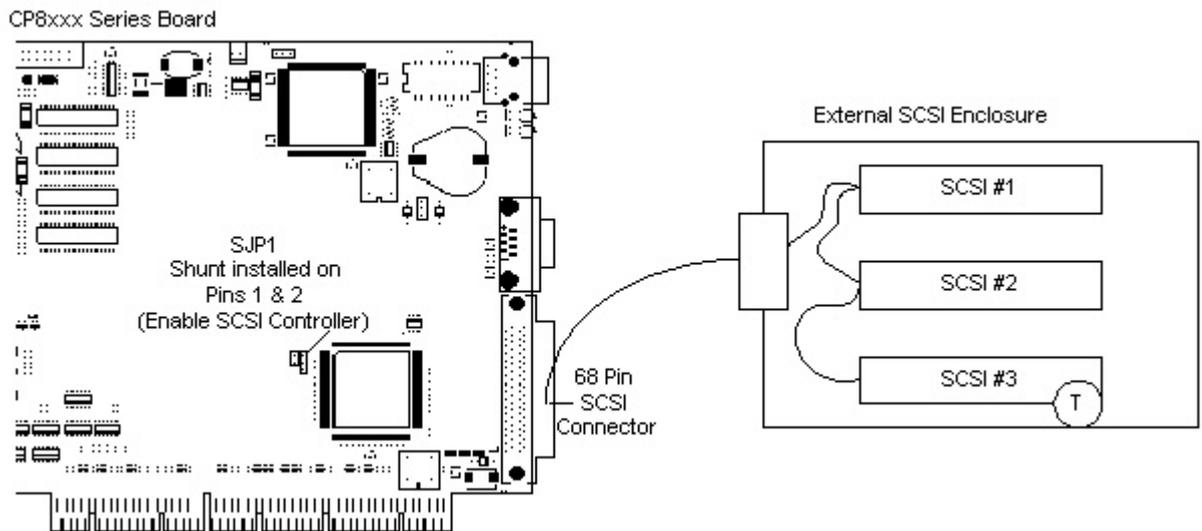
If the SCSI controller is ordered, a SCSI configuration utility is available on boot-up of the board. Shortly after the SCSI BIOS information displays, the configuration program can be accessed by pressing "Control C". The configuration utility will allow you to scan the SCSI bus, change configuration options and view a list of SCSI devices connected to the board.

### SJP1 - Enable/Disable SCSI Controller

As stated above, the on-board Symbios Wide Ultra2 SCSI controller can be enabled or disabled with SJP1 (see Figure above for SJP1 location).

Jumper	Function	Jumper On Pins 1-2	Jumper On Pins 2-3
SJP1	SCSI	Enabled	Disabled

The SCSI controller supports up to 15 external devices, either Ultra2 LVD or Single Ended Wide. The end of the SCSI chain Must be terminated independent of whether devices are Single Ended or LVD. Consult the owners manual pertaining to the external SCSI device for instructions on how to terminate. The end of the SCSI chan **must be terminated** independent of whether drives are Single Ended or LVD.




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## LED Status Indicators

### Ethernet Adapter LEDs

On each RJ-45 connector and visible on the mounting bracket is a pair of LEDs

**On the upper LED:** When the LED is green it indicates a link to an Ethernet hub and when blinking it is showing network activity

**On the lower LED:** When it is green it indicates the interface is set to 100Mbit/s.

### POST Display LEDs

The CP8xxx board has a group of 8 LEDs arranged above the IDE connector (J9). As the system proceeds through its Power On Self Test (POST) these LEDs display binary codes which can be used to diagnose board failures.

### Board Power LED

There is a Board Power LED located on the CP8xxx board between COM2 (J3) and the LPT connector (J4) (see Figure 2 for Board Power LED location). This LED will be green when there is power to the board. This LED is only visible when the cover is off the Density System.

### SCSI Activity LED

There is a SCSI Activity LED on the back side of the CP8xxx board. This LED will be amber when the SCSI is busy. The SCSI Activity LED is located at the rear of the board, close to the Ethernet Enable jumper (JP1) and is only visible when the cover is off the Density System.

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## Memory Configuration & Management

- All memory is provided in 168 pin, 72 bit 100MHZ (PC100) ECC SDRAM DIMMs.
- DIMMs do not need to be installed in pairs, and different sizes may be mixed.
- DIMMs may be either registered or unbuffered. Registered and unbuffered DIMMs may not be mixed.

- DIMMs must have gold contacts (edge connectors)

**Table 4-1, Memory Map**

Memory Range	Size	Use
00000-9FFFF	640KB	Conventional Memory
A0000-AFFFF	64KB	VGA Graphics Buffer
B0000-B7FFF	32KB	MDA Text Buffer
B8000-BFFFF	32KB	VGA/CGA Text Buffer
C0000-C7FFF	32KB	VGA Bios
C8000-DFFFF	96KB	Available
E0000-FFFFFF	127KB	System & PCI BIOS

**Table 4-2, I/O Map**

ISA Ports	Description
0000-00FF	Various "AT" functions in ISP chip and keyboard controller
01F0-01F7	IDE hard drive interface
02F8-02FF	COM2
03A0	Cubix supervisory interface
03A8-03AF	IES serial port
03B4-03B5	VGA
03BC-03BF	LPT1
03C0-03CF	VGA
03D4-03D5	VGA
03F0-03F7	Floppy / IDE
03F8-03FF	COM1

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## **System Interrupts**

The 16 system hardware interrupts on the SP are represented in Table 4 - 4. Interrupts are managed by two standard 8259A Programmable Interrupt Controllers (PICs). Interrupts at IRQ 0 through 7 are located on the main PIC; IRQ 8 through 15 are on the SLAVE PIC.

**Table 4-3, System Interrupts**

<b>IRQ</b>	<b>Description</b>	<b>IRQ</b>	<b>Description</b>
<b>0</b>	Timer clock	<b>8</b>	Real Time Clock
<b>1</b>	Keyboard	<b>9</b>	Redirected IRQ 2, Set By PCI Plug & Play at Boot Time
<b>2</b>	Second PIC controller	<b>10</b>	Reserved for IES (Factory Default, see JP4)
<b>3</b>	COM2	<b>11</b>	Set By PCI Plug & Play at boot time
<b>4</b>	COM1	<b>12</b>	Available (or PS/2 Mouse)
<b>5</b>	Set By PCI Plug & Play at boot time	<b>13</b>	Math Coprocessor
<b>6</b>	Floppy Disk Controller	<b>14</b>	Primary IDE
<b>7</b>	LPT1	<b>15</b>	Secondary IDE Controller (CD-ROM)

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