PCI54IT

Version 0.10A

User's Manual

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User's Manual
PCI54IT Motherboard
1st Edition
TMC

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Chapter 1 Specifications

The PCI54IT is a high performance PCI system board. It's highly flexible in CPU frequency, L2 cache type and size, and main memory type and size. The main features are listed as follows:

Main Processor

Intel Pentium 75/90/100/120/133/150/166/180/200

Processor Upgrade

Intel P6 based Over Drive

L2 Cache

Size: 256K or 512K
Type: Pipelined Burst Synchronous module, Asynchronous module, or Discrete Asynchronous on board.

Main Memory

Up to 128MB of total main memory
SIMM Size: 4, 8, 16 or 32 MB SIMMs
SIMM Type: Fast page mode or Extended Data Out (EDO)

Chipset

Intel Triton chipset with built- in PCI-IDE

BIOS

Licensed BIOS with additional features:

- ISA Plug and Play (PnP) extension
- Power management
- NCR 53C810 SCSI BIOS

Expansion Slots

Four PCI slots
Three ISA slots

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Chapter 2 Hardware Description

This chapter briefly describes each of the major features of the PCI54IT system board. The layout of the board is shown in *Figure 1* which shows the locations of key components. The topics covered in this chapter are as follows:

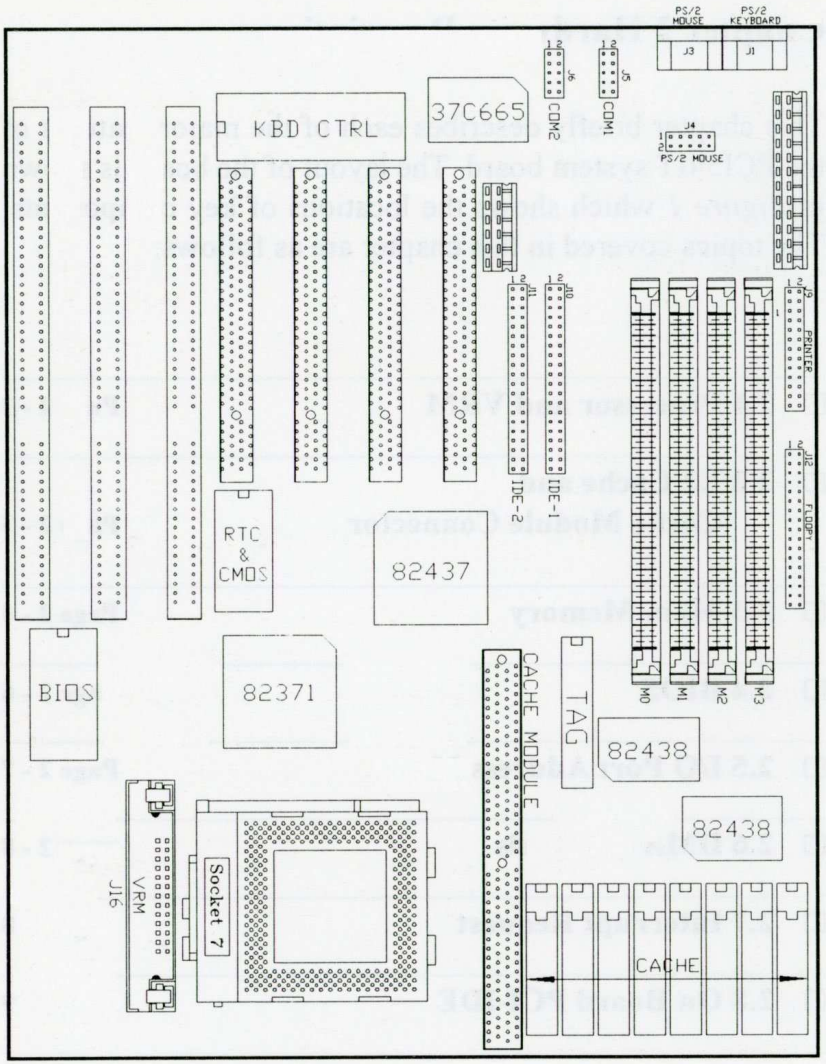

Figure 1: Layout of the PCI54IT

2.1 Processor and VRM

The PCI54IT is designed to take a PENTIUM Processor with a bus speed of 50, 60 and 66 MHz. Since the internal clock of the CPU can be multiples of 1.5 or 2 of the bus clock, the CPU frequency can be 75, 90, 100, 120 or 133. The VRM (Voltage Regulator Module) socket provides support for CPUs which requires voltage other than 3.3V, such as 2.5V, and/or power consumption higher than 10 watts. One example is a P6 based Over Drive.

2.2 L2 Cache and Cache Module Connector

The PCI54IT supports both P.B. (Pipelined Burst) Synchronous Cache and Asynchronous Cache. The P.B. Synchronous Cache boost the system performance 10% higher than regular Asynchronous Cache. There are four Cache configurations available and are shown on the following table:

	On Board Discrete	Cache Module
256K Asynchrous	Yes	Yes
512K Asynchrous	Yes	Yes
256K P.B. Synchrous	No	Yes
512K P.B. Synchrous	No	Yes

Note: The on board discrete and cache module can not co-exist.

2.3 Main Memory

The PCI54IT provides two 64bit memory banks. Each bank consist of two SIMMs, M0/M1 and M2/M3. Both EDO and page mode DRAM are supported. The size of SIMM can be 1Mx32, 2Mx32, 4Mx32, and 8Mx32.

The following are the important factors for populating the SIMM sockets:

1. Either M0/M1 or M2/M3 bank can be populated first

2. Each bank should consist of the same size SIMMs

3. Each bank should consist of the same type SIMMs.
   ex: M0 and M1 should both be EDO or page mode.

4. SIMMs can be mixed by the bank.
   ex: M0/M1 are page mode and M2/M3 are EDO

5. SIMMs can be with or without parity.

Available memory configurations are shown in the following table:

Bank0 (M0, M1)	Bank1 (M2, M3)	Total Memory
4	-----	8MB
8	-----	16MB
16	-----	32MB
32	-----	64MB
4	4	16MB
4	8	24MB
4	16	40MB
4	32	72MB
8	8	32MB
8	16	48MB
8	32	80MB
16	16	64MB
16	32	96MB
32	32	128MB

Note: The Bank0 designate the memory bank populated first which can be M0/M1 or M2/M3.

2.4 BIOS

The BIOS on the PCI54IT system board provides the standard BIOS functions plus the following additional features:

1. ISA Plug and Play (PnP) extension

Unlike PCI cards which are plug and play, ISA cards require setting jumpers to resolve hardware conflict. To make a computer system PnP, an ISA PnP standard is established and supported by new OSes, such as Windows 95. Under Windows 95, the system board BIOS must have ISA PnP extension to support the new ISA PnP cards.

2. Power management

The power management feature provides power saving by slowing down the CPU clock, turning off the monitor screen, and stopping the HDD spindle motor.

3. NCR 53C810 SCSI BIOS

NCR 53C810 is a PCI SCSI shippped from NCR. The BIOS required to run cards with the 53C810 chip is built-in the system BIOS. The BIOS will automatically detect the existence of an 53C810 chip and configure it accordingly.

2.5 I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port address which also becomes the identity of the device. There are a total of 1K port address space available. The following table list the I/O port address used on the system board.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
2F8h - 2FFh	Serial Port #2(COM2)
378h - 3FFh	Parallel Port #1(LPT1)
3F0h - 3F7h	Floppy Disk Controller
3F8h - 3FFh	Serial Port #1(COM1)

2.6 DMA Channels

There are seven DMA Channels available on the system board. Only DRQ2 is used by the floppy controller. In the case that ECP mode on parallel port is used, DRQ1 or DRQ3 will be used.

2.7 Interrupt Request (IRQ)

There are a total of 15 IRQs available on the system board. Peripheral devices use interrupt request to notify CPU for the service required. The following table shows the IRQ used by the devices on the system board:

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ8	Real Time Clock
IRQ9	Software Redirected to Int 0Ah
IRQ10	Reserved
IRQ11	Reserved
IRQ12	Reserved
IRQ13	80287
IRQ14	Primary IDE
IRQ15	Secondary IDE
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Parallel Port #2
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1

2.8 On board PCI-IDE

The PCI-IDE controller is part of the Triton chip set. It supports PI0 mode 3/4 and bus mastering. The peak Transfer rate of PI0 mode 3/4 can be as high as 17MB/sec. Using HDDs that support bus mastering, the peak transfer rate can reach 22MB/sec. There are two IDE connectors, primary IDE and secondary IDE. With two devices per connector, up to four IDE drives are supported.

2.9 On Board Multi-I/O

The on board multi-I/O chip, SMC37C665, provides two serial ports, one parallel port, and one floppy controller. The serial ports are 16550 UART compatible. The parallel port supports high speed ECP mode. The floppy controller supports up to 2.88 MB format. The I/O port addresses of the serial and parallel ports are programmable via BIOS set-up. Each I/O can be individually disabled as well.

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Chapter 3 Configuring the PCI54IT

The following sections describe the necessary procedures and proper jumper settings to configure the PCI54IT system board. For the locations of the jumpers and Resistor Arrays, refer to *Figure 3.*

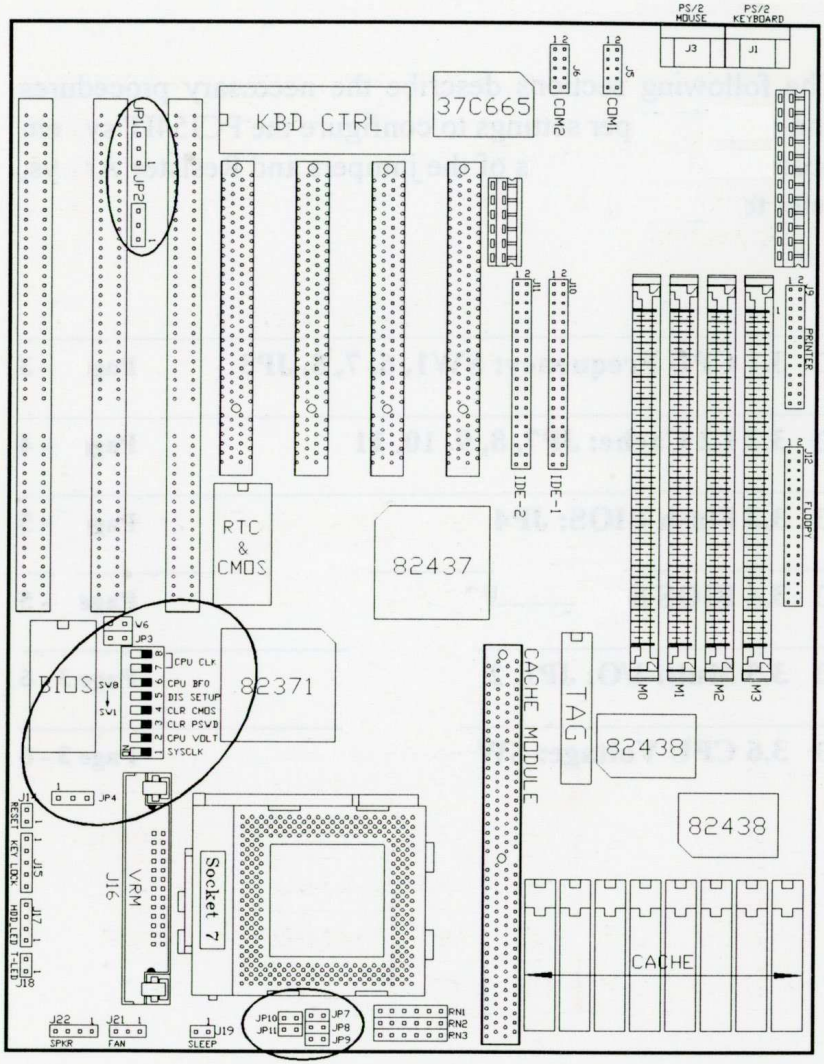


Figure 2: Jumper locations of the PCI54IT

3.1 CPU Frequency: SW1, 6, 7, 8, JP3

SW7 and SW8 set the clock generator frequency to be 50, 60, or 66MHz. SW6 sets the ratio of CPU internal clock, which is the frequency of the CPU, to the bus clock. SW1 sets the ratio of bus clock to AT clock. SW1 should always be kept at ON position.

Refer to the following table for the correct setting to match the CPU frequency.

SW1	JP3	SW6	SW7	SW8	Bus Clock	CPU FREQ.
ON	OFF	OFF	OFF	OFF	50MHz	75MHz
ON	OFF	OFF	ON	OFF	60MHz	90MHz
ON	OFF	OFF	ON	ON	66MHz	100MHz
ON	OFF	ON	ON	OFF	60MHz	120MHz
ON	OFF	ON	ON	ON	66MHz	133MHz
ON	ON	ON	ON	OFF	60MHz	150MHz
ON	ON	ON	ON	ON	66MHz	166MHz
ON	ON	OFF	ON	OFF	60MHz	180MHz
ON	ON	OFF	ON	ON	66MHz	200MHz

3.2 L2 Cache: JP7, 8, 9, 10, 11

The PCI54IT provides great flexibility in L2 cache configuration. The on board discrete sockets accommodate 256KB or 512KB Asynchronous cache. The cache module connector supports P.B. Synchronous or Asynchronous cache module. The JP7, 8, 9, 10 and 11 should be set according to the following table to ensure proper L2 cache operation.

JP7	JP8	JP9	JP10	JP11	Cache Type
IN	out	out	out	IN	256KB Asynchronous
out	IN	IN	out	IN	512KB Asynchronous
IN	out	out	out	out	256KB P.B. Synchronous
out	IN	IN	out	out	512KB P.B. Synchronous
out	out	out			No Cache

To install discrete SRAM on board, refer to the following tables for the type and speed of the SRAM required.

TAG	Cache	Cache Size
8Kx8	32Kx8	256KB Asynchronous
32Kx8	64Kx8	512KB Asynchronous

Bus Clock	TAG	Cache
50MHz	20NS	20NS
60, 66MHz	15NS	15NS

Note: The speed of SRAM shown is recommended value

3.3 Flash BIOS: JP4

Depending on the manufacture and model, the programming voltage of the flash ROM can be 5V or 12V. This jumper should ***not*** be altered unless the flash BIOS is being replaced with a different type of flash ROM.

JP4	Flash Type
1 - 2	12V Programming
2 - 3	5V Programming

Note: SST Flash ROM JP4 is Don't Care.

3.4 BIOS Set-up: SW3, 4, 5

SW3, 4 and 5 control BIOS set-up related options. The function of each SW is listed in the following table:

	OFF	ON
SW3	Normal	Clear BIOS password
SW4	Normal	Clear BIOS CMOS content
SW5	Normal	Aceess to BIOS set-up prevented

3.5 Multi-I/O: JP1, 2

JP1 and JP2 select the DMA channel for the parallel port when ECP mode is enabled.

JP1, 2	DMA Channel
1 - 2	DMA1
2 - 3	DMA3

3.6 CPU Voltage: SW2

The output voltage of the on board regulator is normally set to support all the existing CPU models. In the case that a new CPU model requires higher working voltage, SW2 setting will adjust the regulator output voltage.

SW2	CPU Voltage
ON	Normal
OFF	Higher

Chapter 4 Installation

This chapter describes the interface that the PCI54IT provides for creating a working system. Refer to Figure 3 for the location of the connectors.

The following items are covered in this chapter:

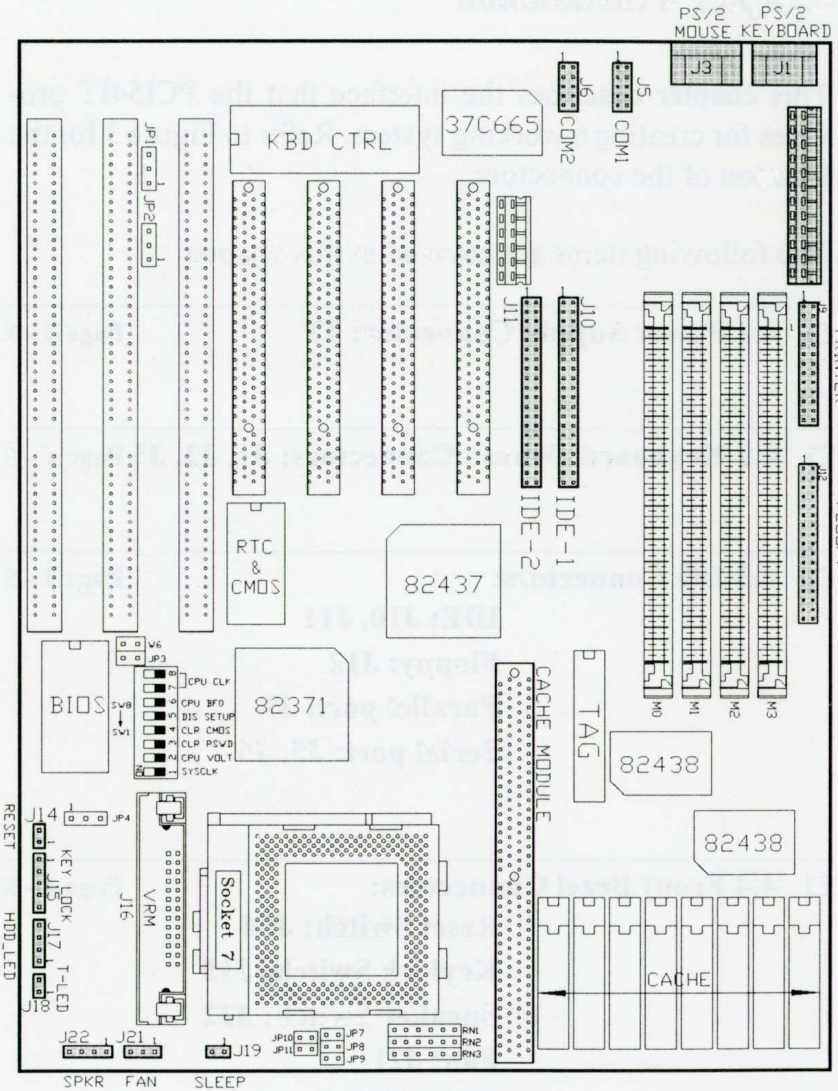


Figure 3: Connector locations and orientation

4.1 Power Supply Connector: J7

When using an AT compatible power supply, plug both of the power supply connectors into J7.

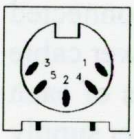
Make sure the power supply connectors are connected in the right orientation. The power supply connectors are connected in the right orientation if the black wires of each power cable are ADJACENT to each other. That is, black wires of each connector should be aligned in the center of the power supply connectors, J7, of the PCI54IT.

The following table indicates the pin-out assignments of the power supply connectors.

J7 Pin #		Description	Wire Color
1		Power Good	Orange
2		-5V	Red
3		+12V	Yellow
4		-12V	Blue
5		Ground	Black
6		Ground	Black
7		Ground	Black
8		Ground	Black
9		-5V	White
10		+5V	Red
11		+5V	Red
12		+5V	Red

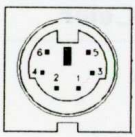
4.2 Keyboard/Mouse Connector: J1, J2, J3

There are two configuration available on PCI54IT, an AT keyboard or PS/2 keyboard and mouse.



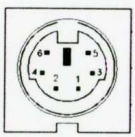
J2: AT Keyboard

J2 Pin#	Function
1	Keyboard Clock
2	Keyboard Data
3	N.C.
4	Ground
5	VCC



J1: PS/2 Keyboard

J1 Pin#	Function
1	Data
2	N.C.
3	GND
4	5V
5	Clock
6	N.C.

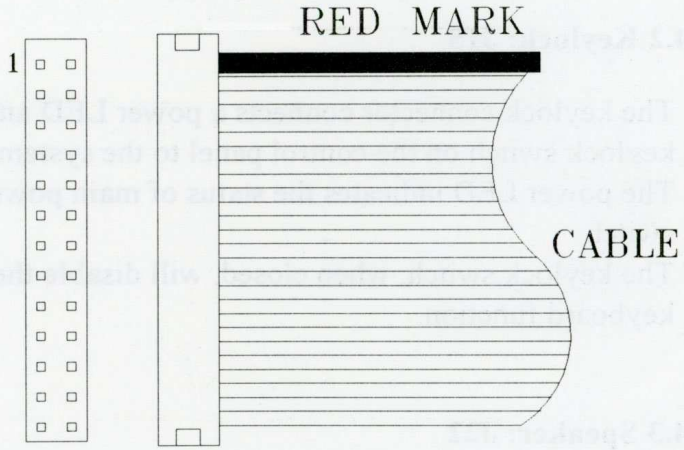


J3: PS/2 Mouse

J3 Pin#	Function
1	Data
2	N.C.
3	GND
4	5V
5	Clock
6	GND

4.3 I/O Connector

The I/O connectors connect the PCI54IT to the most common peripherals. To connect cables to these connectors, align carefully the Pin 1 of the cables to that of connectors. Refer to Figure 3 for the location and orientation of the connectors.



4.4 Front Bezel Connectors

The front bezel of the case has a control panel which provides light indication of the computer activities and switches to change the computer status.

4.4.1 Reset Switch: J14

The reset switch allows the user to reset the system without turning the main power switch off and then on.

4.4.2 Keylock: J15

The keylock connector connects a power LED and keylock switch on the control panel to the system board. The power LED indicates the status of main power switch.
The keylock switch, when closed, will disable the keyboard function.

4.4.3 Speaker: J22

This connector provides an interface to a speaker for audio tone generation. An 8-ohm speaker is recommended.

4.4.4 FAN: J21

This J21 is an easy access connector for CPU fan power. The fan must be a 12V fan.

4.4.5 Sleep: J19

This connector is for "Green Switch" on the control panel, which, when pressed, will force the system board into power saving mode immediately.

4.4.6 HDD LED: J17

This connector connects to the hard drive activity LED on control panel. This LED will flash to when the HDD is being accessed.

4.4.7 Turbo LED: J18

There is no turbo/deturbo function. The Turbo LED on control panel will always be on when attached to this connector.

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