



# PCI-949

CELERON PENTIUM III SBC

Technical Reference Manual  
Version 1.3, February 2003

**Note: The latest releases of the Technical Reference Manuals are available at:**

[ftp://ftp.kontron.ca/Support/Product\\_Manuals/](ftp://ftp.kontron.ca/Support/Product_Manuals/)



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# DOCUMENTATION SURVEY

## PCI-949 – Technical Reference Manual

Your comments are valuable for us and will contribute to improve the quality of this product by complementing and returning this form.

1. Overall rating of the Technical Reference Manual:  Excellent  Satisfactory  Fair  Poor

2. Was the information you were seeking easy to find?  Yes  No

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In terms of clarity of information:  Excellent  Satisfactory  Fair  Poor

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\_\_\_\_\_

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5. Is there any missing information?  Yes  No

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Name \_\_\_\_\_

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Address \_\_\_\_\_

\_\_\_\_\_ **Optional** \_\_\_\_\_



# **FCC COMPLIANCE STATEMENT**

## **Warning**

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generated, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

## **European Statement**

### **Warning**

This is a Class B product. If not installed in a properly shielded enclosure and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his own expense.

### **Safety Standard**

UL Recognized Component, File # E186339 vol. 1 section 2

### **Care and handling precautions for Lithium batteries**

- Do not short circuit
- Do not heat or incinerate
- Do not charge
- Do not deform or disassemble
- Do not apply solder directly
- Do not mix different types or partially used batteries together
- Always observe proper polarities

# READ ME FIRST

Your computer board has a standard non-rechargeable lithium battery. To preserve the battery lifetime, **the battery enable jumper is removed when you receive the board**. If you do not have any jumper cap, we suggest you to use the Watchdog Timer jumper cap.

## EXERCISE CAUTION WHILE REPLACING LITHIUM BATTERY



### WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.



### ATTENTION

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie.

Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le fabricant. Mettre au rebut les batteries usagées conformément aux instructions du fabricant.



### ACHTUNG

Explosionsgefahr bei falschem Batteriewechsel. Verwenden Sie nur die empfohlenen Batterietypen des Herstellers. Entsorgen Sie die verbrauchten Batterien laut Gebrauchsanweisung des Herstellers.



### ATENCION

Puede explotar si la pila no este bien reemplazada.

Solo reemplazca la pila con tipas equivalentes segun las instrucciones del manufacturo. Vote las pilas usadas segun las instrucciones del manufacturo.



## **POWERING-UP THE BOARD**

**If you should encounter a problem, verify the following items:**

Make sure that all connectors are properly connected.

Check your boot diskette.

If the board still does not start up properly, you should try booting your system with the PCI-949 installed in the system, a monitor and a mouse connected to the board. This is the minimum required to verify the board's operation.

If you still are not able to verify your board, please refer to the emergency Procedure in the Appendix Section.

If you still are not able to get your board up and running, contact our Technical Support department for assistance (see appendix G, Getting Help).



## **ADAPTER CABLES**

While adapter cables are provided from various sources, the pinout is often different. The direct crimp design offered by Kontron allows the simplest cable assembly. All cables are available from Kontron Sales Department.

# **UNPACKING AND SAFETY PRECAUTIONS**

## **Static Electricity**

Since static electricity can cause damage to electronic devices, the following precautions should be taken:

1. Keep the board in its anti-static package, until you are ready to install it.
2. Always touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
3. Handle the board by the edges.

## **Storage Environment**

Electronic boards are sensitive devices. Do not handle or store devices near strong electrostatic, electromagnetic, magnetic or radioactive fields.

## **Power Supply**

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

## **Unpacking**

Follow these recommendations while unpacking:

1. After opening the box, save it and the packing material for possible future shipment.
2. Remove the board from its anti-static wrapping and place it on a grounded surface.
3. Inspect the board for damage. If there is any damage or missing items, notify Kontron immediately.

When unpacking you will find:

1. One PCI-949 SBC.
2. One Quick Reference sheet.
3. One CDROM containing drivers.

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# **1 PRODUCT OVERVIEW**

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**PART**

**1**

- 1. INTRODUCTION**
- 2. PCI-949 SBC TECHNICAL SPECIFICATIONS**
- 3. POWER REQUIREMENTS**



## **1.1 Introduction**

The PCI-949 is a solid, general purpose single board computer geared to satisfy the needs of various industrial and medical PCI/ISA applications that require flat panel support.

Additional value is provided with an Ultra-2 SCSI LVD/SE (80MB/s) for increased storage support, ideal for most mission-critical CTI applications.

As bandwidth-intensive applications continue to increase, Kontron's PCI-949 offers the latest in processing power with an Intel® Pentium® III processor at 850MHz clock speeds which is integrated into a single slot, low profile SBC to meet the critical requirements for more power in less space. Other essential features include up to 1GB of SDRAM, two 10Base-T/100BaseTx Ethernet interface, two USB ports, ATX support, and CPU/Board monitoring.

Compatible with Kontron's backplanes and enclosures, the PCI-949 is capable of supporting a comprehensive range of OSs, including Windows NT 4.0/2000, QNX and Linux.

## 1.2 PCI-949 SBC Technical Specifications

FEATURES	DESCRIPTIONS
<b>CPU</b>	<ul style="list-style-type: none"> <li>• Celeron® processor 433, 566 and 733 MHz</li> <li>• Pentium III processor - 600MHz, 700 and 850MHz</li> </ul> <p>Note : Will feature higher speeds when CPU available.</p>
<b>Chipset</b>	<ul style="list-style-type: none"> <li>• Intel 440BX AGPset.</li> </ul>
<b>Cache</b>	<ul style="list-style-type: none"> <li>• 16K/16K Instruction / Data CPU-internal Level 1</li> <li>• 256KB Advanced Transfer Cache (64-bit wide on-die full speed Level 2 pipelined burst with ECC)</li> </ul>
<b>Memory</b>	<ul style="list-style-type: none"> <li>• Four 168-pin latching DIMM sockets, 64/72-bit</li> <li>• Up to 1GB of SDRAM with parity or ECC (for single bit error correction and double bit error detection)</li> </ul>
<b>Data Path</b>	<ul style="list-style-type: none"> <li>• 64-bit between CPU and memory</li> <li>• 32-bit on local PCI and AGP bus.</li> <li>• 16-bit on the ISA bus</li> </ul>
<b>Bus Interfaces</b>	<ul style="list-style-type: none"> <li>• Front Side Bus 66MHz/100MHz determined by CPU</li> <li>• AGP Bus, 32-bit 66MHz</li> <li>• PCI Bus, 32-bit 33MHz</li> <li>• ISA Bus, 16-bit 8MHz</li> <li>• PCI-to-ISA non-transparent bridge; Intel's 82371EB</li> <li>• SMBus (for system management of CPU temperature monitoring, DRAM control, Clock buffers and power control)</li> </ul>
<b>Interrupts</b>	<ul style="list-style-type: none"> <li>• 11 edge/level sensitive and configurable</li> <li>• 4 PCI level sensitive, configurable to any interrupt vector for PnP compatibility</li> <li>• All ISA onboard interrupts are PnP compliant</li> </ul>
<b>DMA Channels (ISA)</b>	<ul style="list-style-type: none"> <li>▪ Four 8-bit, three 16-bit</li> <li>▪ Supports scatter / gather, Fast Type-F DMA</li> </ul>

## PCI-949 SBC Technical Specifications (continued)

FEATURES	DESCRIPTIONS
<b>Flash Memory</b>	<ul style="list-style-type: none"> <li>• 256KB for BIOS field upgrade</li> <li>• 4KB Serial EEPROM for user configuration</li> <li>• Silicon Serial ID TAG for unique board identification accessible via software</li> </ul>
<b>Video</b>	<ul style="list-style-type: none"> <li>• 32-bit AGP video controller (C&amp;T 69000) with 2MB on die 83MHz SDRAM video memory</li> <li>• CRT resolutions up to 1280x1024x256 colors, non-interlaced</li> </ul>
<b>Clock/Calendar</b>	<ul style="list-style-type: none"> <li>• Real-time clock with (replaceable) battery backup</li> <li>• 256-byte CMOS RAM</li> </ul>
<b>I/O</b>	<ul style="list-style-type: none"> <li>• <b>Super I/O Controller</b> : SMC FDC37C672</li> <li>• <b>USB Ports</b> : Two</li> <li>• <b>Serial Ports</b> : Two (COM1: RS-232, COM2: Configurable as RS-232/422/485)</li> <li>• <b>Parallel port</b> : One bi-directional with all IEEE 1284 protocols supported, BIOS selectable IRQs and addressing</li> <li>• <b>Floppy Disk</b> : Support for two drives (360KB to 1.44MB)</li> <li>• <b>EIDE</b> : Two channels Bus Master PCI EIDE; support for two IDE drives (master/slave configuration); LBA, PIO Mode 0-4 and Ultra DMA/33</li> <li>• <b>Ethernet</b> : Two Intel 82559 Fast Ethernet controllers, PCI 10/100Base-TX ports</li> <li>• <b>Multifunction</b> : PS/2 mouse, AT and PS/2 standard keyboard, speaker, reset switch and hard disk LED</li> <li>• <b>CompactFlash™ Module</b>: Optional bootable CompactFlash™ disk interfaces to secondary EIDE channel, master/slave.</li> <li>• <b>Ultra2 SCSI LVD/SE</b> : Up to 80MB/sec</li> </ul>

## PCI-949 SBC Technical Specifications (continued)

FEATURES	DESCRIPTIONS
<b>BIOS Features</b>	<ul style="list-style-type: none"> <li>• Award Elite BIOS in Boot Block Flash with emergency recovery code; save CMOS in Flash option, and boot from LAN capability.</li> <li>• Auto configuration, extended setup.</li> <li>• CC000-E0000 address blocking; PnP tables.</li> <li>• Setup console redirection to serial port (VT100 mode) with CMOS setup access.</li> <li>• Software enable/disable of onboard Ethernets; hardware enable/disable of onboard video.</li> <li>• Diskless, keyboardless, and videoless operation extensions.</li> <li>• Batteryless operation with CMOS copy in flash BIOS.</li> <li>• System, video, and LAN BIOS shadowing system, video, and option BIOS shadowing.</li> <li>• Programmable bus and I/O speeds and memory wait states.</li> <li>• Advanced Configuration and Power Interface (ACPI 1.0), Advanced Power Management (APM 1.2), advanced thermal management (resume, overheat alarm and auto slow down), and Green support.</li> </ul>
<b>Supervisory</b>	<ul style="list-style-type: none"> <li>• Two-stage software programmable Watchdog timer drives NMI on first stage and system reset on second stage</li> <li>• Time out from 16ms to 4.25min</li> <li>• Programmable CPU temperature monitor alarm</li> <li>• Board temperature sensor</li> <li>• Power failure and voltage monitoring/low battery detector</li> <li>• Two end-user defined open-drain general purpose I/Os; SMBus, I2C Bus</li> <li>• LEDs: IDE activity, Ethernet activity and link status.</li> </ul>
<b>OS Compatibility</b>	<ul style="list-style-type: none"> <li>• Windows® 95/98/2000, Windows® NT 4.0, QNX™, Linux, and FreeBSD</li> </ul>
<b>PICMG compliance</b>	<ul style="list-style-type: none"> <li>• Mechanical : compliant to IEEE P996 PC-AT Bus, PCI Rev 2.1, and PICMG Rev. 2.0 standards</li> </ul>
<b>Form Factor</b>	<ul style="list-style-type: none"> <li>• 338 x 122 x 36 mm (13.32" x 4.80" x 1.40") at CPU fan.</li> </ul>

## PCI-949 SBC Technical Specifications (continued)

FEATURES	DESCRIPTIONS																					
<b>Power Requirements</b>	<ul style="list-style-type: none"> <li>• Supply Voltages:     +5V ± 5%     +12V ± 5%</li> <li>• Supply Current * :    5V   8.1A max.                                   12V  0.1A max.</li> <li>• Power Dissipation: ≈ 40W max.</li> </ul> <p><i>* Pentium III processor 850MHz with 1GB SDRAM (no hard drive).</i></p>																					
<b>Environmental</b>	<table border="0" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;"></th> <th style="width: 45%; text-align: center;"><b>Operating</b></th> <th style="width: 40%; text-align: center;"><b>Storage and Transit</b></th> </tr> </thead> <tbody> <tr> <td>Temp.</td> <td style="text-align: center;">0-55°/32-131°F (w/ 150LFM airflow)</td> <td style="text-align: center;">-40° to +70° / -40° to 158°F</td> </tr> <tr> <td></td> <td colspan="2" style="text-align: center;"><b>When using a CompactFlash disk, must not exceed 50°C (0-50°C/32-122°F)</b></td> </tr> <tr> <td>Humidity</td> <td style="text-align: center;">5% to 95% @ 40°C/104°F non-condensing</td> <td style="text-align: center;">5% to 95% @ 40°C/104°F non-condensing</td> </tr> <tr> <td>Altitude</td> <td style="text-align: center;">4,572m / 15,000ft</td> <td style="text-align: center;">15,240m / 50,000ft</td> </tr> <tr> <td>Shock</td> <td colspan="2" style="text-align: center;">5G, each axis</td> </tr> <tr> <td>Vibration</td> <td colspan="2" style="text-align: center;">1.5G, each axis</td> </tr> </tbody> </table>		<b>Operating</b>	<b>Storage and Transit</b>	Temp.	0-55°/32-131°F (w/ 150LFM airflow)	-40° to +70° / -40° to 158°F		<b>When using a CompactFlash disk, must not exceed 50°C (0-50°C/32-122°F)</b>		Humidity	5% to 95% @ 40°C/104°F non-condensing	5% to 95% @ 40°C/104°F non-condensing	Altitude	4,572m / 15,000ft	15,240m / 50,000ft	Shock	5G, each axis		Vibration	1.5G, each axis	
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Shock	5G, each axis																					
Vibration	1.5G, each axis																					
<b>Reliability</b>	<ul style="list-style-type: none"> <li>• MTBF: &gt; 85,000 hours 55°C/131°F (MIL-HDBK-217F)</li> <li>• Unique silicon serial number accessible via software</li> <li>• SCSI termination, USB, keyboard and mouse voltage protected by self-resetting fuses</li> <li>• 2 year limited warranty</li> </ul>																					
<b>Safety</b>	<ul style="list-style-type: none"> <li>• Designed to meet or exceed UL 1950; CSA C22.2 No 950; EN 60950; IEC950</li> </ul>																					
<b>EMI/EMC</b>	<ul style="list-style-type: none"> <li>• FCC 47 CFR Part 15/CISPR22, Class B; CE Mark to EN55022/EN50082</li> </ul>																					

FEATURES	DESCRIPTIONS
<p><b>Connectors</b></p>	<ul style="list-style-type: none"> <li>• <b>Faceplate :</b> <ul style="list-style-type: none"> <li>Ethernet : Two RJ45 with link/activity indicators</li> <li>USB : Two USB connector</li> <li>Video : One 15-pin DB connector</li> </ul> </li>   <li>• <b>Headers :</b> <ul style="list-style-type: none"> <li>Serial ports : Two 10-pin shrouded</li> <li>Parallel port : 26-pin shrouded</li> <li>Floppy : 34-pin shrouded</li> <li>EIDE : Two 40-pin shrouded</li> <li>PS/2 mouse : 4-pin locking</li> <li>Power-down : 2-pin locking</li> <li>External power: 8-pin locking</li> <li>SCSI : D-Sub 68-pin connector</li> <li>Multifunction : 16-pin shrouded (keyboard, speaker and EIDE disk LED)</li> <li>CPU fan : Two 3-pin locking</li> <li>Battery : 4-pin non-locking</li> <li>Ext. Battery : 2-pin locking</li> <li>SCSI LED : 2-pin locking</li> <li>Hardware Monitor : 20-pin shrouded</li> <li>CompactFlash™ Module header (40-pin)</li> </ul> </li> </ul>

### 1.3 Power requirements

The power requirements for the PCI-949 are specified as follows:

CPU	Celeron 433	Pentium III 600	Pentium III 850
<b>VCORE</b>	2.00 V	1.65V	1.65V
<b>Frequency (Int / Ext)</b>	433 / 66	600 / 100	850 / 100
<b>Power MAX 5V/12V</b>	33.75 / 1W	33.1 / 1W	40.3 / 1 W
<b>Power TYP 5V/12V</b>	25.5 / 1W	27.8 / 1W	31.8 / 1W
<b>Power SUS 5V/12V</b>	11.9 / 1W	14.9 / 1W	14.85 / 1W
<b>Ambient temp MAX</b>	55°C	40°C	40°C
<b>TEST CONDITIONS</b>			
<b>Power MAX</b>	Running KPower in Windows		
<b>Power TYP</b>	Idle in Windows		
<b>Power SUS</b>	Suspend mode in Windows		
<b>Test setup</b>	1GB SDRAM, running Windows 98 with 3.2GB hard disk.		

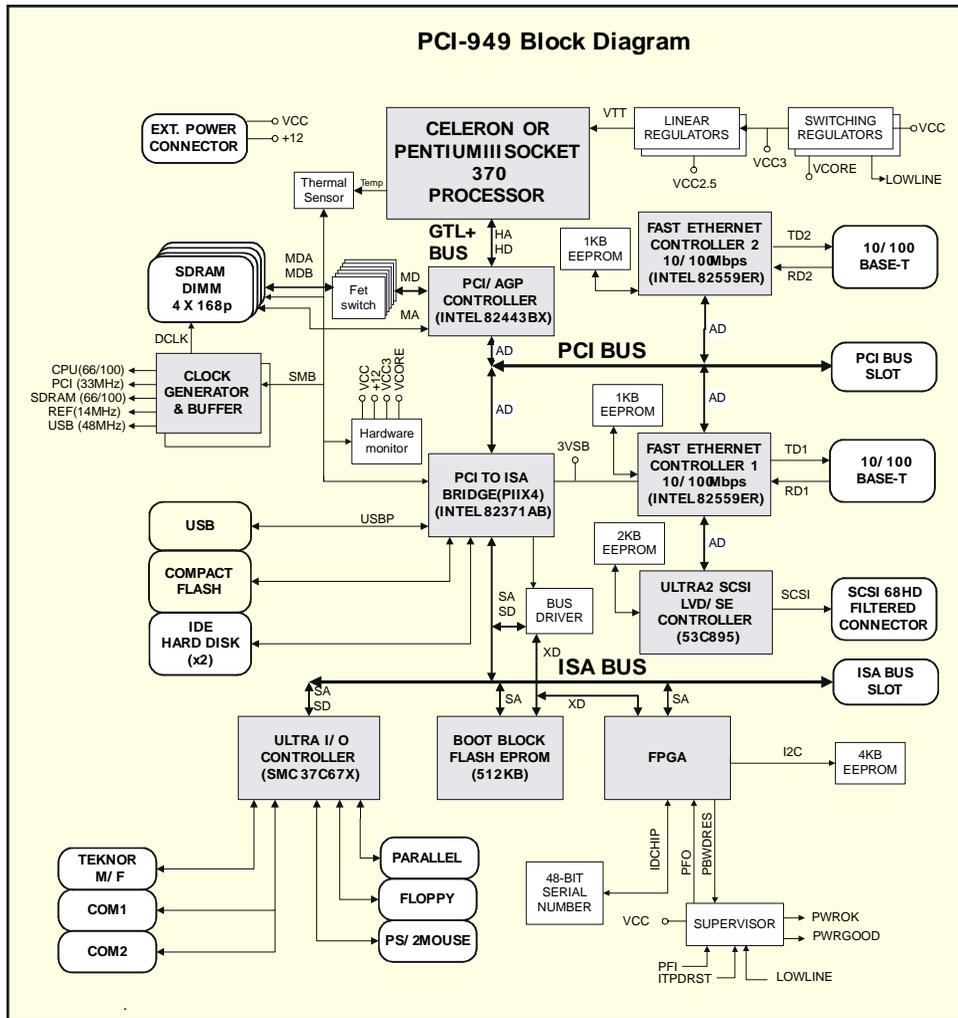
Note: The 3.3V is generated from +5V.

## 2 ONBOARD FEATURES

---

1. BLOCK DIAGRAM
  2. SYSTEM CORE
  3. BATTERY
  4. THERMAL MANAGEMENT
  5. POWER SUPPLY
  6. I/O DEVICES
  7. STORAGE DEVICES
-

## 2.1 Block Diagram



## 2.2 System Core

### 2.2.1 Processors

#### Celeron® and Pentium® III Processors

Peripheral processor supports the Intel's Celeron® 433, 566 and 733MHz, as well as the Pentium III® 600, 700 and 850MHz. Higher clock speeds will be available when Intel releases the corresponding parts.

It consists of a Pentium® II / III processor core with an integrated second level cache of 256KB (on-die, full CPU speed, ECC capable) and a 64-bit high-performance 66/100MHz front side bus.

The processor interfaces to the 440BX AGPset through the 64-bit low-power GTL + data bus interface.

The PCI-949 SBC is shipped with the Celeron® or the Pentium® III processor equipped with a heat sink with fan that provides adequate cooling in a 150LFM airflow environment.

---

#### Related Jumpers

None

#### BIOS Settings

None

---



#### CAUTION

Since CPUs are very sensitive components, particular attention should be given while installing a processor on the board.

Improper installation may damage the board and/or the CPU.

Before installing a processor on your board, **you must contact our Technical Support** for the installation procedure (see Appendix G, Getting Help).

## 2.2.2 Chipset

### 2.2.2.1 North Bridge Chipset

This chipset consist of 443BX AGPset, 64/72-bit SDRAM data interface with ECC support, Low-Power GTL Bus, five PCI arbitration channels, PCI bus rev. 2.1, Accelerated Graphics Port Interface (AGP). The bus is optimised for 100MHz operation.

### 2.2.2.2 82371AB PCI-to-ISA Bridge / IDE Xcelerator (PIIX4E)

This Multifunction PCI-to-ISA bridge supports PCI 2.1, full ISA (EIO) Bus, 3.3V operation with 5V tolerant buffers. It provides the PCI-949 SBC with an IDE interface for up to four drives with Bus Mastering IDE, Transfer, each with independent timing and UDMA/33 capabilities.

The 82371AB (PIIX4E) also supports ACPI Power Management functions and OS Directed Power Management. In addition it provides two 82C37 DMA Controllers, a 15 Interrupt Controller (two 82C59), two USB 1.1 Ports, a System Management Bus (SMB) and support for other peripherals like standard Serial and Parallel Ports, Floppy Drives, Mouse and Keyboard through the FDC37C627 super I/O controller.

## 2.2.3 Memory

### 2.2.3.1 SDRAM System Memory

The PCI-949 SBC supports four industry standard 168-pin DIMMs (Dual In-Line Memory Module) sockets for memory configuration from 8MB to 1GB of Synchronous DRAM.

The memory characteristics must conform to the following:

- 1.15 inch height, 168-pin DIMM
- Standard 3.3V only,
- 64-bit and 72-bit modules, single-sided or double-sided
- Unbuffered 100MHz (SDRAM),
- Serial Presence Detect (SPD) EEPROM,
- Errors Checking and Correction (ECC) capabilities or parity bit with 72-bit modules,
- Compliant with Intel's PC SDRAM Unbuffered DIMM Specification (100MHz) Rev. 1.0.

At least 8MB of memory must be installed on the board for proper operation. Modules can be installed in any socket and order. The total system memory is equal to the sum of the memory module size installed in the four DIMM sockets.



**NOTE**

When populating with more than one memory module, each socket must be installed with the same memory type (64/72-bit), however the capacity of each module may be different from the other. The BIOS will take the less common denominator.

To get the latest list of approved DIMMs, please visit our FTP site at location:

[ftp://ftp.kontron.ca/Support/Product\\_Memory\\_AVL\\_Approved\\_Vendor\\_List/](ftp://ftp.kontron.ca/Support/Product_Memory_AVL_Approved_Vendor_List/)

### 2.2.3.2 DIMM Installation

To install the DIMMs in the sockets, proceed as follows:

1. With the board flat on a static-free surface, turn it so that the faceplate is facing right.
2. Hold the module vertically so that the bottom connector key is at right. Install the DIMM straight down into the DIMM socket. The socket's keys will ensure a correct mating.
3. Press firmly on the top edge of the memory module to engage it into the socket. The module is fully inserted when the retaining clips snap into notches located at each end of the module.

If necessary, work your way by inserting the other modules, one by one.

To remove the DIMMs from the sockets, pull simultaneously on the retaining clips located on each side of the socket. Once the module has snapped out, pull gently on it.



#### **WARNING**

Since static electricity can cause damage to electronic devices, the following precautions should be taken:

1. Keep the board in its anti-static package, until you are ready to install it.
2. Touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
3. Handle the board by the edges.

## 2.3 Battery

The battery is required to keep the BIOS settings and the real-time clock stored into the CMOS RAM. The board is shipped from factory with the battery electrically disconnected from the board.

**Prior to first powering the board, the battery must be connected using the W8 Battery jumper.**

The battery specifications are as follows: 3.6V Lithium battery, 0.37A/h

### Related Jumpers

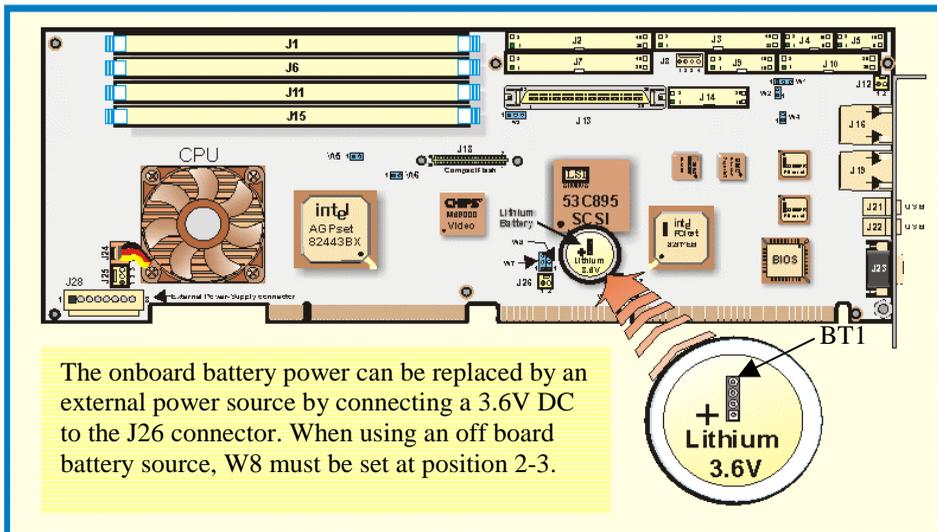
- W 7** Power failed detection
- W 8** Battery source (on board, external or disconnected)

### Related Connectors

- BT1** Polarized battery holder
- J26** External battery connector

### 2.3.1 Installation

Connect the battery to the BT1 header. The positive terminal of the battery holder is located at the bottom center.



**WARNING**

***Danger of explosion if battery is incorrectly replaced.***

Replace only with the same or equivalent type recommended by the manufacturer.  
Dispose of used batteries according to the manufacturer's instructions.

### 2.3.2 Backup Battery

An onboard 3.6V lithium battery is provided to backup BIOS setup values and the real time clock (RTC).

When replacing the battery, it must be connected as follows:

Connect the battery to the BT1 header. The positive terminal of the battery holder is located near the ISA edge connector.

### 2.3.3 Supervisory Features

The PCI-949 SBC provides a set of programmable I/O registers to setup the Intel PIIX4E (I/O addresses 4030h to 4037h) and the XILINX FPGA (I/O addresses programmable at 190h-197h, 290h-297h or 390h-397h using the AWARD Chipset Features Setup).

Only register bits needed to program the power fail detection and watchdog functions are described below (for more details, see section 3.2).

### 2.3.4 Power Fail Monitoring

The status of the power failure detector can be read from one bit of the system register located at the address n91h (n=1, 2, or 3) Bit 0. The detection conforms to the following conditions (\* = active low signal):

The board always monitors the +5V power supply. When it drops below 4.65V (typical), the system is reset.

The board monitors the onboard battery. When the battery is in a low condition (below 2.9V typical), the PFO\* (power fail output) signal goes low. The status of the PFO\* signal can be read at I/O address 4031h, bit 1 (0 = failed, 1 = good). An interrupt handler can then service the interrupt. If you choose not to generate a NMI, you can use an algorithm to detect a low-battery condition and respond accordingly.

**For more information, contact the Technical Support department (see Appendix G)**

## 2.4 Watchdog

The function of a watchdog is to reset the CPU board if the processor is not able to generate a trigger for longer than the watchdog time-out period. This feature is useful in embedded systems where human supervision is not required or impossible.

The PCI-949 SBC provides a two-stage digital watchdog with software programmable time-out period.

Following a reset of any source, the watchdog is disabled. The watchdog can be enabled by software.

### 2.4.1 Dual Stage Watchdog

#### Enabling the Programmable Watchdog

To enable the programmable watchdog, first unlock the enable bit by clearing the lock bit in register \*n92h (bit 2), then set the bit WDEN (bit 7) in register n96h and re-lock it by setting the lock bit in register n92h (bit 2). The following is an example in C language:

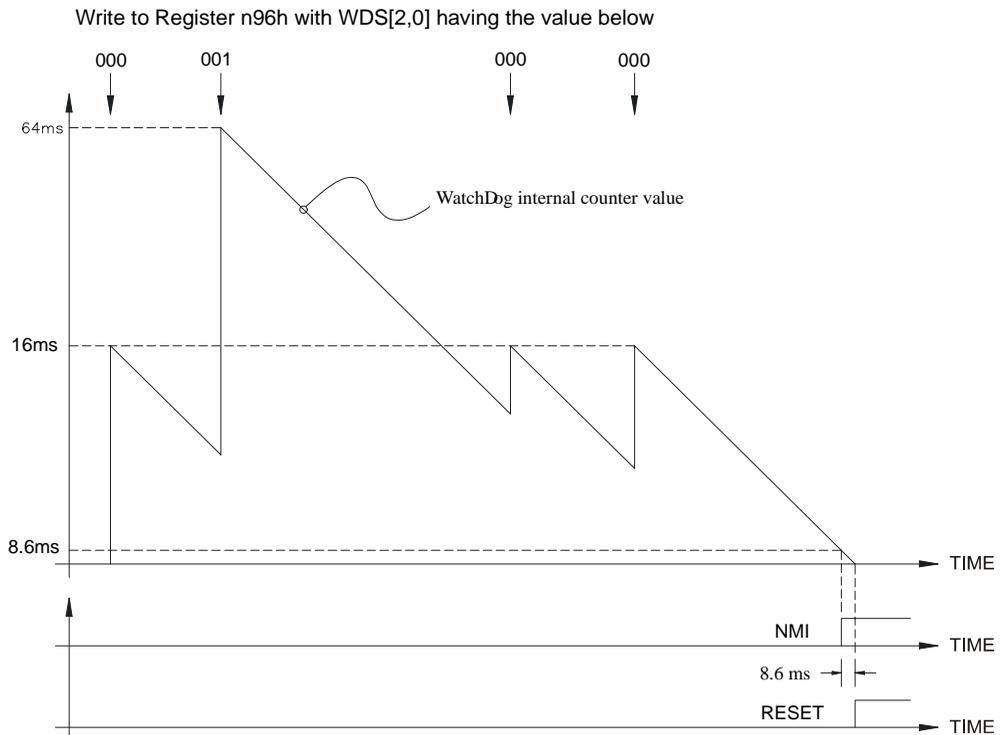
```
#define TekReg 0x190           // define base address (0x190, 0x290 or 0x390)
void ArmWatchdog(void)
{
    outp(TekReg+2, inp(TekReg+2) & 0xFB);    // unlock watchdog enable bit
    outp(TekReg+6, inp(TekReg+6) | 0xF0);    // enable and trigger at max time-out
    outp(TekReg+2, inp(TekReg+2) | 0x04);    // lock watchdog enable bit
}
```

\* Note : n = 1, 2 or 3

#### Triggering the Programmable Watchdog

To trigger the programmable watchdog, the processor writes to register n96h (n=1, 2 or 3). The action of writing to the register is the trigger and the value written to the register tells the watchdog the current time-out to use (see register n96h description, section 3.2.6). For a fixed time-out, the software simply writes a constant in register n96h.

A variable refresh is possible as shown below:



The programmable watchdog can be viewed as a decrementing counter that is initialised by a write to register n96h (n = 1, 2 or 3). The processor must initialise the counter to prevent it from reaching count 0 (timeout).

The following C language procedure can be used to trigger the programmable watchdog.

```
#define TekReg 0x190          // define base address (0x190, 0x290 or 0x390)
void TrigWatchdog(timeout) // select timeout at runtime: 0x80 = 0.016s,
                          // 0x90 = 0.065s, 0xA0 = 0.261s, ...
{
    outp(TekReg+6,(inp(TekReg+6) & 0x0F) | (timeout & 0xF0));
}
```

## Time-out

The programmable watchdog has two stages: the first stage has a variable time-out while the second stage has a fixed one.

The first stage time-out is chosen at runtime from eight preset values (see table below). The first stage time-out generates a NMI interrupt (if enabled in register n96h, bit 7). An appropriate NMI handler must be written, otherwise this will be treated as a parity error by the default BIOS NMI handler; see register n96h description for a suggestion on how to do this.

The second stage times-out  $8.6\text{ms} \pm 10\%$  (depending on the temperature) after the first one and generates a master reset.

WDD[2..0]	NMI(T)	RESET(T)
000	16T	NMI(T)+8T
001	64T	NMI(T)+8T
010	256T	NMI(T)+8T
011	1024T	NMI(T)+8T
100	4096T	NMI(T)+8T
101	16384T	NMI(T)+8T
110	65536T	NMI(T)+8T
111	262144T	NMI(T)+8T

Time-out selection with  $T = 1.08\text{ms}$  (TBC)

A reset from the programmable watchdog is latched for reset source identification.

## 2.5 Thermal Management

Two temperature sensors are provided to supervise the thermal environment. One is used to monitor the CPU die temperature, while the second one, located on the CPU casing, allows the monitoring of the ambient temperature around the CPU.

The temperature is controlled according to two temperature levels, the Low-temperature limit, which indicates normal operating conditions, and the High-temperature limit, which indicates an overheat condition.

The temperature management consists in reducing the CPU clock speed (throttling) when the temperature goes over the high limit (overheat condition) and suspending the throttling operation as soon as the temperature returns under the low-temperature limit (normal condition).

The clock speed may be throttled due to CPU overheating, maybe caused by the system cooling failure. In such a case, the temperature control is triggered as soon as the temperature reaches a high-temperature limit.

The ambient temperature of the CPU generally raises up due to an augmentation of the temperature in the casing. In that case, the clock speed will be slowed down as soon as the ambient temperature reaches the high-ambient temperature value.

Thermal management operations are controlled by the BX chipset, and settings are provided through the BIOS setup program interface, (See Section 4.1.8 *CPU/Board Feature Setup*).

## 2.6 Power Supply

When used as a stand-alone system, the PCI-949 must be powered through the J28 Power connector. When installed on a backplane, the power is drawn to the power lines connected to the ISA and PCI fingers of the edge connectors.

---

### Related Jumpers

None

### BIOS Settings

See Power Management options described in Section 4.1.6 *Power Management Setup*.

---

### 2.6.1 Power Management

The PCI-949 SBC, when powered by an ATX power supply, offers the benefit of Operating System Directed Power Management (OSPM) supported by the hardware and BIOS implementation of Advanced Configuration and Power Interface (ACPI) specification.

ACPI defines the interfaces between the SBC BIOS, Chipset (PIIX4E), SMBus, peripheral devices and OSPM. It provides the BIOS with various hardware interface description Tables, a Firmware Control Structure and pseudo-code Control Methods written in ACPI Source Language (ASL) and ACPI Machine Language (AML) to empower the OSPM and device drivers.

The PIIX4E Chipset supports:

- Clock Control and Processor Complex Management
- Peripheral Device Management
- Event System Management: System Management and System Control Interrupts (SMI) and (SCI) generation and SMBus message handling
- Global System States (Working, Doze, Standby, Suspend, Hibernation, Soft Off) transition
- Device Power States (various, device specific) transition

The utilisation of an OSPM pushes the limits of previous Advanced Power Management (APM) strategies to the critical requirement of the application actually running on the PCI-949 hardware. For instance, the spindle of a hard disk drive could be shut-off immediately after a save to disk operation if it is determined that an application requires little more than its timed AutoSave to disk function; a CPU speed could be reduced for an application phase requiring less computing power.

Wake-up event can be keyboard activity, mouse movement, Wake-on Timer, Wake-on-Ring, or Wake-on-LAN feature.

---

---

### **Signal Path**

The ACPI Power Management supporting PS-OK, PS-ON signals and 5VSB voltage extension to the external Power Supply are available on the J28 connector.

### **Related Jumpers**

None

### **BIOS Settings**

Section 4.1.6 *Power Management Setup*

---

---

## 2.7 I/O DEVICES

### 2.7.1 Ethernet Interface

The Ethernet controller is electrically connected to the Primary PCI bus. It supports 10Base-T and 100Base-TX operations: 10Mbps and 100Mbps network speeds are automatically detected and switched.

---

#### Signal Path

The Ethernet interfaces are available through the J16 and J19 (RJ-45) connector located on the edge bracket. They support the Wake-on-LAN.

#### Related Jumpers

None.

#### BIOS Settings

Section 4.1.4 BIOS Features Setup: Boot from LAN First.  
Section 4.1.9 Integrated Peripherals, Ethernet Controller

---

#### 2.7.1.1 Boot from LAN

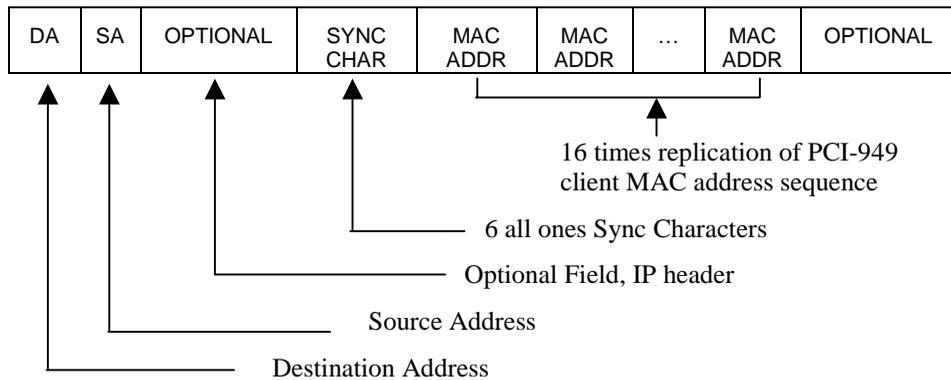
The Boot from LAN capability is supported. To enable the option, use the BIOS Setup program. Please refer to Section 4.1 *BIOS Setup Program*.

#### 2.7.1.2 Drivers

Network Drivers for Intel 82559 are available on the CD-ROM included with the PCI-949. It contains network drivers for most common operating systems.

### 2.7.1.3 Wake-on-LAN Feature

The Wake-on-LAN feature is available with the PCI-949 SBC when it is connected as a client on a LAN. In this case the wake-up event takes the form of an Ethernet packet of a unique format also called Magic Packet™ by AMD. Even in PCI-949 Sleep State, ETHERNET LAN stays powered-on to monitor all incoming packets. Upon detection of its own Magic Packet, characterised by the inclusion of a 16 continuous duplication sequence of its own Media Access Control (MAC) address, the 82559 Fast Ethernet Controller issues a WOL signal which initiates the PCI-949 into a Working State. Wake-on-LAN is neither an APM or ACPI strategy.



Users already familiar with a remote wake-up from Suspend state by a modem ring (Wake-on-Ring) on a designated COM Port (Ring Indicator) can use this option on the PCI-949 SBC.

Wake-on-Event (LAN, Ring, and Timer) and Soft-Off functions are enabled in the *Power Management Setup* option of the *AWARD CMOS Setup Utility* (see Section 4.1.6). The PCI-949 SBC also supports SMI/SMM Power Management. It also supports APM, but its utilisation is mutually exclusive with ACPI.

## 2.7.2 PS/2 Mouse Interface

The onboard keyboard controller is Intel 8042 microcode compatible. PS/2 Keyboard and mouse signals are available through an output that supports direct connection to the interface. Since signals of both devices are combined on the same J20 connector, a Y-cable is required to split the signals and feed a standard PS/2 keyboard and a PS/2 mouse.

---

### Signal Path

PS/2 mouse signals are available through J8 connector and the standard PS/2 keyboard signals are available through J9.

### Related Jumpers

None.

### BIOS Settings

Section 4.1.9 *Integrated Peripherals : USB Keyboard Support, and PS/2 Mouse Function Control.*

---

### 2.7.2.1 I/O Connections

Standard AT keyboard, speaker port, reset and power buttons, and hard disk LED signals are available on the J9 multifunction header.

## 2.7.3 Parallel Port

The PCI-949 features one IEEE-1854 multi-mode parallel port. It is compatible with Standard Mode IBM PC/XT, PC/AT, and PS/2 compatible bi-directional parallel port, Enhanced Parallel Port (EPP), and Enhanced Capabilities Port (ECP).

---

### Signal Path

The Parallel Port interface is only available through J10 connector.

### Related Jumpers

None

### BIOS Settings

Section 4.1.9 *Integrated Peripherals: Onboard Parallel Port, and Parallel Port Mode*

---

The differences between Standard, EPP, and ECP modes appear in the signal assignation of the pins on the connector. Differences are described as follows:

Pin Number (J10)	Standard Mode	EPP Mode	ECP Mode
A15	SLCT	-	SLCT
B15	PE	-	PERROR <sup>1</sup> , ACKREVERS <sup>2</sup>
C15	BUSY	WAIT	BUSY <sup>1</sup> , PERIPHACK <sup>2</sup>
D15	ACK#	INTR#	ACK#
E16	SLCTIN#	ADDRSTRB#	SLCTIN#
B17	INIT#	-	INIT <sup>1</sup> #, REVERSERQST <sup>2</sup> #
D17	ERR#	-	FAULT <sup>1</sup> #, PERIPHROST <sup>2</sup> #
A18	ALF	DATAS <sup>T</sup> B	ALF <sup>1</sup> , HOSTACK <sup>2</sup>
E17	D0	D0	D0
C17	D1	D1	D1
A17	D2	D2	D2
D16	D3	D3	D3
C16	D4	D4	D4
B16	D5	D5	D5
A16	D6	D6	D6
E15	D7	D7	D7

<sup>1</sup> Compatible mode - <sup>2</sup> High-speed Mode



**NOTE**

To operate in EPP or ECP mode, make sure and verify that the peripheral is designed to work in this mode and the BIOS setup is configured to support it.

### 2.7.3.1 Standard Mode

The Standard mode is unidirectional. It is supported to maintain the compatibility with the IBM PC standard.

### 2.7.3.2 EPP Mode

The EPP (Enhanced Parallel Port) mode consists of a hardware independent method of accessing a parallel port configured as EPP. It provides support for single I/O cycle as well as the high-performance block I/O transfers. The EPP mode always uses the optimum method for I/O transfers. For example, if the hardware supports it, EPP mode will perform 32-bit I/O block transfers.

EPP mode assumes that the parallel port can be used to connect more than one peripheral device using multiplexor or daisy chain configurations.

A multiplexor is an external device that permits up to eight parallel port devices to share a single parallel port.

A daisy chain device has two ports: input and output. The input port is connected either to the host parallel port or to the daisy chain device in front of it. The output is used to connect the next peripheral device to the daisy chain. The last device, however, can be one without daisy chain support.

### 2.7.3.3 ECP Mode

ECP (Extended Capabilities Port) works the same as EPP mode, but it will take precedence over the EPP mode when addressing multiple logical devices in a single physical product. While the EPP mode may intermix read and write operations without any overhead or protocol handshaking, the ECP mode negotiates data transfers using a request from the host and an acknowledgement from the peripheral.



#### NOTE

For more information on the ECP protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard (available from Microsoft Corporation) or contact our Technical Support department (See appendix G).

## 2.7.4 Serial Ports

Two fully functional serial ports are provided on the board for asynchronous serial communications. They are 16C550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 50bps to 115Kbaud.

Each serial port is specified as follows:

Designation	Communication Mode	Output Path
Serial Port 1	RS-232	J4
Serial Port 2	RS-232, RS-422 or RS-485	J5

UART registers are individually addressable and fully programmable.

### 2.7.4.1 Serial Port 1

Serial Port 1 is buffered directly for RS-232 operation. Signals include the complete signal set for handshaking, modem control, interrupt generation, and data transfer. When assigned as COM1, the port is 100% compatible with the IBM-AT serial port in RS-232 mode.

---

---

#### Signal Path

Serial Port 1 or COM1 signals are available on J4 connector.

#### Related Jumpers

None

#### BIOS Settings

Section 4.1.9 *Integrated Peripherals : Onboard Serial Port 1\2 Port Address of COM1*

---

### 2.7.4.2 Serial Port 2

The serial port 2 is buffered directly for RS-232, RS-422 or RS-485 operations and is 16C550 PC-Compatible. The interface includes the complete signal set for handshaking, modem control, interrupt generation, and data transfer.

When configured for RS-232 operation mode, the serial port 2 is 100% compatible with the IBM-AT serial port.

---

---

#### Signal Path

Serial Port 2 signals are available on the J5 connector

#### Related Jumpers

W2 and W4 to connect or disconnect Serial Port 2 line termination resistors in RS-485 operating mode. See Section 2.1– *Setting Jumpers*

#### BIOS Settings

Section 4.1.9 *Integrated Peripherals Setup: Onboard Serial Port 2, and Serial Port 2 Mode.*

---

Upon a power-up or reset, the Serial Port 2 interface circuits are automatically configured for the operation mode setup in the BIOS. The Serial Port 2 signal assignment on the J5 connector depends on the operational mode (RS-232, RS-422, or RS-485) it has been set.

#### **2.7.4.2.1 RS-232 Protocol**

When configured for RS-232 operation mode, the Serial Port 2 is 100% compatible with the IBM-AT serial port signal configuration.

#### **2.7.4.2.2 RS-422 Protocol**

The RS-422 protocol (Full Duplex) uses both RX and TX lines simultaneously during a communication session.



#### **CAUTION**

In RS-485 mode, W2 and W3 jumpers must be installed to connect the 120 ohms line termination resistors (See Section 3.1 *Jumper Settings*).

#### **2.7.4.2.3 RS-485 Protocol**

The RS-485 protocol (Full Duplex) also uses differential signals during a communication session. It differs from the RS-422 mode as it offers the ability to transmit and receive over the same pair of wires, and allows the sharing of the communication line by multiple stations. This configuration (also known as Party Line) allows only one system to take control of the communication line at the time.

In RS-485 mode, the RX lines are used as the transceiver lines, and the RTS signal is used to control the direction of the RS-485 buffer.

When set for RS-485 mode in the BIOS, upon power-up or reset, the transceiver is by default in receiver mode to prevent unwanted perturbation on the line. Party line operation mode requires termination resistors to be installed at both ends of the network.

## 2.7.5 USB Interfaces

Signals for two USB ports are available on Connectors J21 and J22.

USB is rapidly becoming the new peripheral interface standard. The USB advantages are: capability to daisy chain as many as 127 devices per single interface, bi-directional, isochronous/asynchronous protocol, fast 12Mbps transfer rate, and standardisation of peripheral interface hardware and protocol into a single format signal paths USB interface signals are available on connectors J21 and J22.

---

### Related Jumpers

None

### BIOS Settings

4.1.7 *PnP/PCI Configuration: Assign IRQ For USB.*

---

The USB interface supports Plug and Play and hot swapping operations (OS level). These user-friendly features allow USB devices to be automatically attached, configured and detached, without powering down, reboot or running setup.

The PCI-949 board fully supports the standard Universal Host Controller Interface (UHCI) and uses standard software drivers that are UHCI-compatible.

## 2.7.6 Video Interface

The high-performance video capability of the board is based on Accelerated Graphics Port (AGP) technology. The video controller, a 69000 (Chips and Technologies), with its integrated 2MegaBytes of high-performance SDRAM is capable of CRT resolutions up to 1280 x 1024 x 256 colors.

The video interface features 32-bit AGP 2D GUI engine supporting CGA, EGA, Hercules, MDA, VGA, SVGA, XGA, and SXGA video display formats.

**Signal Path**

The video signals are available on J23 VGA connector located on the PCI-949 SBC edge bracket allowing direct CRT display connection.

**Related Jumpers**

None

**BIOS Settings**

4.1.7 *PnP/PCI Configuration: Init Display First, and Assign IRQ for VGA*

**2.7.6.1 Supported Display Resolution and Colors**

The maximum video resolution, colors displayed and performance depend directly on the Video drivers running with your application. The PCI-949 SBC Video Interface supports both Frame AGP 1x and PCI bus which enables wide range of system platforms and enables true dual display support. Resolution Refresh Rate and Number of Colors specification for the Intel HiQVideo™ Accelerator are listed below:

Resolution	Number of Colors (bpp)
1280x1024	256 (8 bits)
1024x768	64K (16 bits)
800x600	16M (24 bits)
640x480	16M (24 bits)

**2.7.6.2 2D Graphics Engine**

The 2D graphics engine is an advanced 64-bit three-operand engine that accelerates BitBLTs as line draws, polygon draw, and polygon fill. The 2D graphics engine also performs video and bitmap scaling, and data overlay.

## 2.8 Storage

### 2.8.1 CompactFlash Interface

The PCI-949 board supports an IDE compatible flash disk by using a CompactFlash carrier module. CompactFlash (C-Flash) disks are the resident industry-standard ATA/IDE subsystem for application, data, image, and audio storage. They have the same functionality and capabilities as intelligent disk drives, but with the advantages of being very compact, rugged (typical M.T.B.F. is 1,000,000 hours) and low power. The PCI-949 supports all CompactFlash sizes presently available and future sizes when available. The C-Flash disk connects on the PCI-949 via the onboard Flash Disk adapter T069.

---

---

#### Related Jumpers

W6 to set the CompactFlash disk as master (ON) or slave (OFF).

#### BIOS Settings

Section 4.1.1 *Main Menu: IDE HDD Auto Detection* to set the type of hard disk.

---

The CompactFlash disk connects directly to the SECONDARY EIDE interface. It must be configured the same way as a standard hard disk using the BIOS setup program (Autodetect function).

To setup the CompactFlash disk for Master or Slave configuration, use the CompactFlash jumper W6. To locate and install this jumper, please refer to Section 3.1, *Setting Jumpers*.



#### NOTES

1. Since CompactFlash devices use the ATA/IDE interface, no specific flash disk driver is required for various operating systems.
2. When using a CompactFlash disk, the operating temperature must not exceed 50°C (0-50°C/32-122°F).

## 2.8.2 Enhanced IDE Interfaces

Two IDE interfaces are provided to support up to four IDE devices, such as hard disks, CD-ROM, and CompactFlash. Connections are supported through a 40-pin dual row header.

---

### Signal Paths

The IDE interface is available on the Primary (J2) and Secondary (J7) connectors, and on the Compact Flash J18 connector.

### Related Jumpers

None

### BIOS Settings

Section 4.1.9 *Integrated Peripherals*.

---

The IDE interface supports PIO mode 4 transfers up to 14MB/sec and Bus Master IDE transfer up to 33MB/sec (Ultra-DMA 33). It does not consume any ISA DMA resources and integrates 16x32-bit buffers for optimal transfers.



### CAUTION

When connecting IDE devices to the Primary IDE interface, Master and Slave devices must be shared in respect of the device allocation on both the CompactFlash and hard disk drives.

### 2.8.3 Floppy Disk Interface

The onboard floppy disk controller is IBM PC XT/AT compatible. It handles 3.5" and 5.25", low and high-density disks. Up to two drives are supported in any combination.

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#### Signal Paths

The Floppy Disk Controller interface is available through J3 connector.

#### Related Jumpers

None.

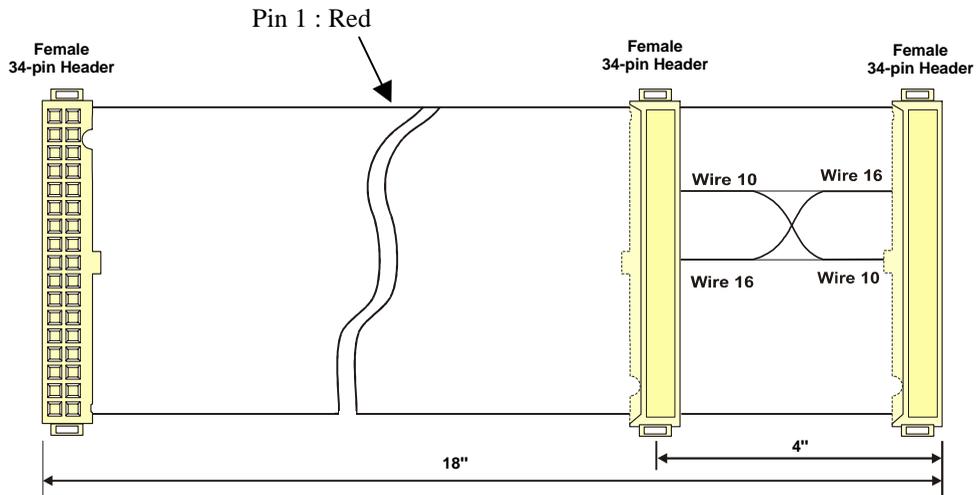
#### BIOS Settings

Section 4.1.4 *Standard CMOS Setup: Select type of floppy.*

Section 4.1.10 *Integrated Peripherals: Enable/Disable Onboard FDC Controller.*

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Two floppy disk drive units can be connected to the board through the J3 Floppy Disk connector using a standard IBM 34-pin flat ribbon cable. As illustrated below an 18" floppy disk cable is available from Kontron Part number 150-051. One cable is provided with your board.



## **3 INSTALLING THE BOARD**

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- 1. SETTING JUMPERS**
- 2. REGISTER'S DESCRIPTION**

### 3.1 Setting Jumpers

Nine jumpers are provided to setup the board. Their functions are summarised below:

<b>JUMPER SETTINGS (* : Default Setting)</b>			
<b>● W1 - VT-100 Reset</b>			
COM2		1-2	
COM1		2-3	
<b>● W3- SCSI Termination</b>			
No termination		Off	
Controlled by software		1-2	
Hardware terminated		2-3	
<b>● W5 - Onboard video</b>			
* Enabled		Off	
Disabled		On	
<b>● W6 - Compact Flash Disk</b>			
* Slave		Off	
Master		On	
<b>● W10 - VT-100 Enable</b>			
* Disabled		Off	
Enabled		On	
<b>● W2, W4 - COM2 RS485 Termination</b>			
RS-422/485 modes only	W2	W4	
With termination resistors	On	On	
* Without termination resistors	Off	Off	
<b>● W7 - Power Fail : Source Detection</b>			
* Offboard Battery		1-2	
Onboard Battery		2-3	
<b>NOTE 1</b>			
To prevent the board from spurious PFI (Power Fail Interrupt), the jumper cap W7 must always be installed at either 1-2 or 2-3 position.			
<b>● W8 - Battery Source</b>			
On Board		1-2	
* External		2-3	
Battery disconnected		Off	
<b>● W9 - Reserved</b>			

### 3.2 Register's Description

Although base address of Supervisor I/O register is shown here at 0x190, it can be programmed at 0x290 or 0x390.

### 3.2.1 Serial Port 2 Configuration

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x190*	NU	NU	NU	RS485	RS232	ST1	NU	NU
WRITE	0x190*	NU	NU	NU	RS485	RS232	ST1	NU	NU
<b>ST1</b>	Enable RTS2 to be used as 485TX ENABLE when in 485 mode.								
<b>RS232</b>	Enable uart2 RS232 operation.								
<b>RS485</b>	Enable uart2 RS422 & 485 operation.								
<b>NU</b>	Reserved.								

The serial port 2 mode can be controlled by setting three bits. Here are the possibilities.

Mode	Bit RS485	Bit RS232	Bit ST1
RS-232	1	0	X*
RS-422	0	1	0
RS-485	0	1	1

\* Do not care.

### 3.2.2 History and Monitor Status

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x191*	PBRST	NU	WDO	CPUFLT	NU	NU	NU	NU
WRITE	0x191*	NU	NU	NU	CPUFLT	NU	NU	NU	NU
<b>PBRST</b>	When high, indicates that a system reset was caused by push button reset switch.								
<b>WDO</b>	When high, indicates that the last system reset was caused by watchdog time out.								
<b>CPUFLT</b>	When low, signals a CPU thermal alarm to the outside world on the system monitor connector.								
<b>NU</b>	Reserved.								

### 3.2.3 History Status

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x192*	NU	NU	NU	NU	NU	WD_LOCK	NU	CLRHS
WRITE	0x192*	NU	NU	NU	NU	NU	WD_LOCK	NU	CLRHS
<b>CLRHS</b>	When low, clears all history bits and disables logging of history for WD and PBreset. When high, enables logging.								
<b>WD_LOCK</b>	When high, locks the state of the enable bit for the digital watchdog.								
<b>NU</b>	Reserved								

### 3.2.4 Monitoring Status and I/O Access

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x193*	APPFLT	GPIO2	GPIO1	NU	IDCHIP	VGA_INT	I2C_CLK	I2C_DATA
WRITE	0x193*	APPFLT	GPIO2	GPIO1	NU	IDCHIP	VGA_INT	I2C_CLK	I2C_DATA
<b>I2C_DATA</b> I2C data. <b>I2C_CLK</b> I2C Clock. <b>IDCHIP</b> One-wire clock/data for silicon ID chip. <b>GPIO_1</b> General purpose I/O. <b>GPIO_2</b> General purpose I/O. <b>APPFLT</b> When low, signals an application fault to the outside world on the system monitor connector. <b>VGA_INT</b> Enable/Disable Video refresh interrupt. <b>NU</b> Reserved.									

### 3.2.5 Registers 0x194 and 0x195

These registers are reserved.

### 3.2.6 Digital Watchdog

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x196*	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
WRITE	0x196*	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
<b>WDEN</b> Enable/disable digital watchdog. <b>WDD[2..0]</b> Duration of digital watchdog. <b>NU</b> Reserved.									

### 3.2.7 NMI Control

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x197*	BATFEN	BATFLT	FANFEN	FANFLT	EXTFEN	EXTFLT	WDNMIEN	WDNMI
WRITE	0x197*	BATFEN	NU	FANFEN	NU	EXTFEN	NU	WDNMIEN	NU
<b>WDNMI</b> When low, signal NMI from watchdog timeout. <b>WDNMIEN</b> Enable NMI generation from digital watchdog. <b>EXTFLT</b> When high, signal NMI from external source on monitor connector. <b>EXTFEN</b> Enable NMI generation from external source. <b>FANFLT</b> When high, signal NMI from external fan motion detector on monitor connector. <b>FANFEN</b> Enable NMI generation from fan fault on monitor connector. <b>BATFLT</b> When high, signal NMI from local RTC battery monitor. <b>BATFEN</b> Enable NMI generation for bat fault. <b>NU</b> Reserved.									

### 3.2.8 Register Bits Position (Summary)

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x190*	NU	NU	NU	RS485	RS232	ST1	NU	NU
WRITE	0x190*	NU	NU	NU	RS485	RS232	ST1	NU	NU
READ	0x191*	PBRST	NU	WDO	CPU_FLT	NU	NU	NU	NU
WRITE	0x191*	NU	NU	NU	CPU_FLT	NU	NU	NU	NU
READ	0x192*	NU	NU	NU	NU	NU	WD_LOCK	NU	CLRHis
WRITE	0x192*	NU	NU	NU	NU	NU	WD_LOCK	NU	CLRHis
READ	0x193*	APP_FLT	GPIO_2	GPIO_1	NU	IDCHIP	VGA_INT	I2C_CLK	I2C_DATA
WRITE	0x193*	APP_FLT	GPIO_2	GPIO_1	NU	IDCHIP	VGA_INT	I2C_CLK	I2C_DATA
READ	0x194*	NU	NU	NU	NU	NU	NU	NU	NU
WRITE	0x194*	NU	NU	NU	NU	NU	NU	NU	NU
READ	0x195*	NU	NU	NU	NU	NU	NU	NU	NU
WRITE	0x195*	NU	NU	NU	NU	NU	NU	NU	NU
READ	0x196*	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
WRITE	0x196*	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
READ	0x197*	BAT_FLT_EN	BAT_FLT_STATUS	FAN_FLT_EN	FAN_FLT_STATUS	EXT_FLT_EN	EXT_FLT_STATUS	WDMNMIEN	WDMNMI
WRITE	0x197*	BAT_FLT_EN	NU	FAN_FLT_EN	NU	EXT_FLT_EN	NU	WDMNMIEN	NU

\* The base address for the Supervisor I/O Register, which is used for such functions as power fail detection and the watchdog timer can be set to 190h, 290h, and 390h (see *Chipset Features Setup*).

## **4 SOFTWARE SETUPS**

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**PART**

**4**

- 1. BIOS SETUP PROGRAM**
- 2. UPDATING OR RESTORING THE BIOS IN FLASH**
- 3. VT100 MODE**

## 4.1 BIOS Setup Program

All relevant information for operating the board and connected peripherals is stored in the CMOS memory (a battery-backed up memory holds this information when the board is powered off). The BIOS Setup program is required to make changes to the setup.



### NOTES

1. Make sure you setup the BIOS Setup program prior to installing your operating system and your drivers.
2. For systems that need the BIOS to first attempt to boot from LAN, follow these steps:
  - a. Set the *Boot from LAN first* option to "Enabled" in the BIOS Setup's *BIOS Features Setup*.
  - b. Follow the complete procedure in the Boot from LAN utility CDROM.

## Accessing the BIOS setup program

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the PCI-949 peripheral processor. The PCI-949 uses the AWARD Setup program, a setup utility in flash memory that is accessed by pressing the DELETE key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.



### CAUTION

Before modifying CMOS setup parameters, ensure that the W7 battery selection jumper is installed to enable the CMOS battery back up (please refer to Section 3.1).

To run the AWARD Setup program incorporated in the ROM BIOS:

- Turn on or reboot the system.
- Hit the DELETE key when the message - "Press DEL to Enter SETUP" appears near the bottom of the screen.

The main menu of the AWARD BIOS CMOS Setup Utility appears on the screen.

KONTRON APPPLICOM T9004 BIOS VERSION 2.0 CMOS SETUP UTILITY AWARD SOFTWARE, INC. (2A69TU00)			
STANDARD CMOS SETUP		LOAD BIOS DEFAULTS (safe)	
BIOS FEATURES SETUP		LOAD SETUP DEFAULTS (optimal)	
CHIPSET FEATURES SETUP		SUPERVISOR PASSWORD	
POWER MANAGEMENT SETUP		USER PASSWORD	
PNP/PCI CONFIGURATION		IDE HDD AUTO DETECTION	
CPU/BOARD FEATURES SETUP		SAVE & EXIT SETUP	
INTEGRATED PERIPHERALS		EXIT WITHOUT SAVING	
Esc	:	Quit	↑ ↓ → ← : Select Item
F10	:	Save & Exit Setup	(Shift)F2 : Change Color
Time, Date, Hard Disk Type . . .			

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters, except those in “standard CMOS setup”, if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS Default settings consist of the **safest** set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP Default values provide **optimum performance** settings for all devices and system features.



**CAUTION**

These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

## 4.1.1 Main Menu

The Main Menu includes the following categories:

Category	Description
Standard CMOS Setup	This Setup page includes all the items in a standard, AT-compatible BIOS (date, time, hard disk type, floppy disk type, video adapter type, memory, etc.).
BIOS Features Setup	This Setup page includes all the items of AWARD's special enhanced features.
Chipset Features Setup	This Setup page includes all the items of the chipset's special features.
Power Management Setup	This Setup page sets power conservation options.
PnP/PCI Configuration	This Setup page sets Plug and Play and PCI configuration options.
CPU/Board Features Setup	This Setup page sets processor speed, thermal management and board monitoring options.
Integrated Peripherals	I/O subsystems that depend on the integrated peripherals controller in your system.
Load Bios Defaults	The BIOS defaults are <b>fail safe</b> settings, which consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.
Load Setup Defaults	The Setup defaults are the <b>optimal</b> settings that provide the optimum performance for all devices and system features. <b>If the CMOS RAM is corrupted, the Setup defaults are loaded automatically.</b>
Supervisor/User Password Setting	Change, set or disable the password. It allows you to limit the access to the system and the Setup, or only to the Setup.
IDE HDD Auto Detection	Forces the detection of the IDE hard disk drives parameters and puts them in the Standard CMOS Setup page.
Save & Exit	After having modified the BIOS Setup, you can save the configuration in CMOS RAM and the Flash BIOS, by selecting this option.
Exit Without Saving	This option is used to exit AWARD Setup without saving the configuration to CMOS RAM or Flash BIOS.

## 4.1.2 Setups

The arrow keys (↑ ↓ → ←) are used to highlight items on the menu and the PAGEUP and PAGEDOWN keys are used to change the entry values for the highlighted item. To enter in a submenu, press the ENTER key. Also, you can press the F1 key to obtain help information or the ESC key to close a menu or to quit the program.

Key	Function
↑	Moves to previous item.
↓	Moves to next item.
←	Moves to the item at the left.
→	Moves to the item at the right.
<b>ESC</b>	When in the Main Menu: Quits program without saving modifications. When in other screens: Exits and returns to the Main Menu.
<b>PAGEUP or +</b>	Increases the numeric value or changes value.
<b>PAGEDOWN or -</b>	Decreases the numeric value or changes value.
<b>F1</b>	Help Menu
<b>F2 / &lt;Shift&gt;F2</b>	At the main menu, change the color of the menu.
<b>F5</b>	When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup, Integrated Peripherals Setup or CPU Board Features: Restores the previous setup values for that setup screen only.
<b>F6</b>	When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup, Integrated Peripherals Setup or CPU Board Features: Loads the BIOS Defaults for all the BIOS parameters for that setup screen only.
<b>F7</b>	When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup, Integrated Peripherals Setup or CPU Board Features: Loads the Setup Defaults for the BIOS parameters for that setup screen only. If the CMOS RAM is corrupted, the Setup defaults are loaded automatically.
<b>F10</b>	When in the Main Menu: Saves all the CMOS changes and exit.

### 4.1.3 Standard CMOS Setups

Function	Description
<b>Date/Time</b>	The current values for each category are displayed. Enter new values through the keyboard.
<b>Hard Disks</b>	Two IDE controllers are defined on the board. The Primary and Secondary controllers can both have two disks: Master Disk or Slave Disk. Three settings are available for the hard disk type: Auto, User and None. Types 1 to 46 are not predefined in the system: Use auto or enter the parameters for the type in the user-defined.
<b>Drive A / Drive B</b>	Select the type of floppy disk installed for drive A and drive B.
<b>Video</b>	This option specifies the basic type of display adapter card installed in the system.
<b>CRT &amp; LCD</b>	Indicates whether the CRT only, LCD only or Both display mode is selected.
<b>Halt on</b>	This option specifies the type of errors that will stop the system during the BIOS booting procedure. A message asks that you " <b>press F1 to continue or press the DELETE key to enter Setup</b> ". The settings are: All errors, No errors, All but keyboard, All but diskette, and All but disk/key (default setting).
<b>Memory</b>	This display-only option indicates the amount of Base, Extended and other types of memory installed in the system.

## 4.1.4 BIOS Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Virus Warning	Dis.	Dis.	En. / Dis.	When Enabled, you receive a warning message if a program (specifically, a virus) attempts to write to the boot sector or the partition table of the hard disk drive. You should then run an anti-virus program. Keep in mind that this feature protects only the boot sector, not the entire hard drive. <b>Note: Many disk diagnostic programs and OS setups (e.g., Win95 setup), that access the boot sector table, can trigger the virus-warning message. If you plan to run such a program, we recommend that you first disable the virus warning.</b>
Quiet POST	Dis.	Dis.	En./Dis.	At the power on self-test (POST), only the AWARD logo and the "Press DEL to enter SETUP" message appears when Enabled.
Quick Power On Self Test	Dis.	En.	En./Dis.	Select Enabled to reduce the amount of time required running the POST. A quick POST skips certain steps. We recommend that you enable quick POST to save time, since most major OS do their own tests
Full Screen Logo Show	Dis.	Dis.	En./Dis.	When enabled, a full screen bitmap (BMP) picture will appear during the POST or you can have your logo being displayed. Contact the technical Support (see Appendix G).
Boot from LAN First	Dis.	Dis.	LAN1 LAN2 LAN1-2 LAN2-1 None	If Enabled, the BIOS will first attempt to boot from the LAN. The complete procedure for this function is available on the "Boot from LAN" utility CDROM.
Raid Card Boot First	Dis.	Dis.	En./Dis.	If Enabled, the BIOS will first attempt to boot from the RAID disk card.
Boot Sequence	A,C, SCSI	C,A, SCSI	A,C,SCSI; C,A,SCSI; C,CDROM,A; CDROM,C,A; D,A,SCSI; E,A,SCSI; F,A,SCSI; SCSI,A,C; SCSI,C,A; C only; LS/ZIP,C.	This option defines the searching order in the BIOS for the boot device(s). <b>Note: The Boot from LAN First and Raid Card Boot First options take precedence over this option.</b>
Swap Floppy Drive	Dis.	Dis.	En./Dis.	Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B.
Boot Up Floppy Seek	En.	Dis.	En./Dis.	When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360KB floppy drives have 40 tracks; drives with 720KB, 1.2MB, and 1.44MB capacity all have 80 tracks. Because very few modern PCs have 40 track floppy drives, we recommend that you set this field to "Disabled" to save time.
Drive A Boot Permit	En.	En.	En./Dis.	When Disabled, this option will not permit booting from Drive A.
Floppy Disk Access Control	R/W	R/W	R/W, Read Only	When Read Only, this option will not permit writing to the floppy disk.

## BIOS Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Report No FDD For Win 95	No	No	Yes, No	Select Yes to release IRQ6 when the system contains no floppy drive, for compatibility with Windows 95 logo certification. In the Integrated Peripherals screen, select NO on the Onboard FDC Controller option.
Hard Disk Write Protect	Dis.	Dis.	En./Dis.	When Enabled, this option will not permit writing to the hard disk.
HDD S.M.A.R.T. Capability	Dis.	En.	En./Dis.	When Enabled, the Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.) features of the HDD are supported. S.M.A.R.T is used for prediction of device degradation and/or faults.
Delay For HDD (Secs)	0	0	0-15	This number of seconds inserted prior to HDD initialisation. 0 is disabled.
OS Select For DRAM > 64MB	Non-OS/2	Non-OS/2	Non-OS/2, OS/2	Select OS2 only if you are running OS/2 with greater than 64MB of RAM.
Gate A20 Option	Norm.	Fast	Normal, Fast	When Fast, enables fast switching of Gate A20 via the 440BX chipset, instead of the keyboard controller.
Security Option	Setup	Setup	Setup, System	If you have set a password, select whether the password is required every time the system boots ("System" option), or only when you enter Setup ("Setup" option).
Diskette Access For	All	All	All, Supervisor	When this option is set to Supervisor and the Security option to System, all floppy disk accesses (read/write) are limited to the Supervisor (supervisor password required).
Boot Up NumLock Status	On	On	On, Off	Controls the state of the NumLock key when the system boots. When set to "On", the numeric keypad generates numbers instead of controlling cursor operations.
Typematic Rate Setting	Dis.	En.	En./Dis.	When Disabled, the following two items (Typematic Rate and Typematic Delay) are irrelevant. Keystrokes repeat at a rate determined by the keyboard controller in your system. When Enabled, you can select a typematic rate and a typematic delay.
Typematic Rate (Chars/s)	30	30	6, 8, 10, 12, 15, 20, 24, 30 char/sec.	When the typematic rate setting is Enabled, you can select a typematic rate (the rate at which characters repeat when you hold down a key).
Typematic Delay (msec)	250	250	250, 500, 750, 1000 ms	When the typematic rate setting is Enabled, you can select a typematic delay (the delay before keystrokes begin to repeat when you hold down a key).
<b>VT100 Settings</b>				
Comport	1	1	1,2	Use this option to select which COM port will be used for VT100
Speed	Auto	Auto	Auto, 2400, 9600, 19200, 38400, 57600, 115200	Select the baud rate off the COM port. used in VT100 mode.
Parity	None	None	None, Odd, Mark, Even, Space	Use this option to select the parity.
Data	8	8	7, 8	Use this option to specify the number of data bits being used.
Stop	1	1	1, 2	Use this option to specify the number of stop bits being used.

## 4.1.5 Chipset Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
CPU Internal Cache	Dis.	En.	En./Dis.	Enables or Disables the CPU Internal Cache (L1 cache).
External Cache	Dis.	En.	En./Dis.	Enables or Disables the External Cache (L2 cache).
CPU L2 Cache ECC Checking (on CuMine PIII processor, you cannot disable ECC)	Dis.	En.	En./Dis.	Enables or Disables ECC Checking for L2 cache. <b>Note: processors provided by Kontron support ECC. However, not all Pentium® II processors support ECC. Check Intel's website to know if your processor supports ECC:</b> <a href="http://developer.intel.com/support/processors/pentiumII/Identify.htm">http://developer.intel.com/support/processors/pentiumII/Identify.htm</a> .
SDRAM RAS-to-CAS Delay	3	3	2, 3	<b>Note: Upon boot-up, the BIOS will detect and display the optimal value for the SDRAM options (three options in this menu), if it is different from the Setup value. You must enter the AWARD Setup, and set the options at the suggested value if you want the best performance.</b> This option inserts a timing delay between the CAS and RAS strobe signals, used when SDRAM is written to, read from, or refreshed. The number selected is the number of clocks to be inserted between a row activates command and either a read or write command.
SDRAM RAS Precharge Time	3	3	2, 3	Selects the number of CPU clocks for the RAS precharge. If an insufficient number of cycles are allowed for the RAS to accumulate its charge before SDRAM refresh, the refresh may be incomplete and the DRAM may fail to retain data.
SDRAM CAS Latency Time	3	3	2, 3	This option controls the number of clocks between when a read command is sampled by the SDRAMs and when the chipset samples read data from the SDRAMs. Select 3 for 3 DCLKs and 2 for 2 DCLKs. If a given row is populated with a registered SDRAM DIMM, an extra clock is inserted between the read command and when the chipset samples read data.
SDRAM Precharge Control	Dis.	Dis.	En./Dis.	When Enabled, all CPU cycles to SDRAM result in an All Banks Precharge Command on the SDRAM interface.
DRAM Data Integrity Mode	Non-ECC	ECC	ECC, Non-ECC	When set to ECC, allows auto-correction of the data read from memory. The ECC error flags' status register and the error pointer are updated if error correction occurs in this mode. When set to Non-Ecc, no error checking or error reporting is done.
Memory Hole At 15M-16M	Dis.	Dis.	En./Dis.	You can reserve this area of system memory for ISA adapter ROM. When this area is reserved, it cannot be cached. The user information of peripherals that need to use this area of system memory usually discusses their memory requirements.
Video BIOS Cacheable	Dis.	En.	En./Dis.	Selecting Enabled allows caching of the video BIOS ROM at C0000h plus the VGA BIOS size, resulting in better video performance. However, in any program writes to this memory area, a system error may occur.
Video RAM Cacheable	Dis.	En.	En./Dis.	When Enabled, video memory region is cacheable. Some off-board video card drivers may behave strangely; in such a case, disable this option.
8 Bit I/O Recovery Time	3	1	1-8, NA	The I/O recovery mechanism adds bus clock cycles between PCI-originated I/O cycles to the ISA bus. This delay takes place because the PCI bus is much faster than the ISA bus. These two fields let you add recovery time (in bus clock cycles) for 8-bit and 16-bit I/O.
16 Bit I/O Recovery Time	2	1	1-4, NA	

## Chipset Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
PCI/VGA Palette Snoop	Dis.	Dis.	En./Dis.	<p>Palette snooping allows multiple VGA devices operating on different buses to handle data from the CPU on each set of palette registers.</p> <p>When set to Enabled, data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA device's palette registers, permitting the palette registers of both to be identical.</p> <p>When set to Disabled, data read and written by the CPU is only directed to the PCI VGA device's palette registers.</p>
Passive Release	En.	En.	En./Dis.	When Enabled, CPU to PCI bus accesses are allowed during passive release otherwise the arbiter only accepts another PCI master access to local SDRAM.
Delayed Transaction	Dis.	Dis.	En./Dis.	The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specifications version 2.1.
Supervisor I/O Base Address	190h	190h	190h, 290h, 390h	This option determines the base address for the Supervisor I/O Register, which is used for such functions as power fail detection and the watchdog timer.
Power-Supply Type Note: This option is not available on T9004 rev0 and rev 1	AT	ATX	AT, ATX	This option selects the type of power supply.
AGP Aperture Size (MB)	64	64	4 to 256	This option selects the size in MB of the AGP Aperture.
Video BIOS Shadow	Dis.	En.	En./Dis.	Software that resides in a read-only memory (ROM) chip on a device is called <i>firmware</i> . Award permits shadowing of firmware such as the system BIOS, video BIOS, and similar operating instructions that come with some expansion peripherals.
C8000-CBFFF	Dis.	Auto	Auto/Dis.	<p>Shadowing copies from ROM into system RAM, where the CPU can read it through the 64-bit DRAM bus. Firmware not shadowed must be read by the system through the 8 or 16-bit ISA bus. Shadowing improves the performance of the system BIOS and similar firmware for expansion peripherals.</p> <p>Auto shadowing into each section of memory separately. Many system designers hardwire shadowing of the system BIOS and eliminate a System BIOS Shadow option. Note that on a PCI card (on board or off-board), the BIOS is always shadowed.</p> <p>Video BIOS shadows into memory area C0000 plus the VGA BIOS size. The remaining areas between C0000 and DFFFF shown on the BIOS Features Setup screen may be occupied by other expansion card firmware. If an expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies to shadow it into the correct area of RAM.</p>
CC000-CFFFF	Dis.	Auto	Auto/Dis.	
D0000-D3FFF	Dis.	Auto	Auto/Dis.	
D4000-D7FFF	Dis.	Auto	Auto/Dis.	
D8000-DBFFF	Dis.	Auto	Auto/Dis.	
DC000-DFFFF	Dis.	Auto	Auto/Dis.	

## 4.1.6 Power Management Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
ACPI Function	Dis.	Dis.	En./Dis.	The Advanced Configuration and Power Interface (ACPI) allows Operating System Direct Power Management (OSPM) and make advanced configuration architectures possible. When Enabled, the OS supports ACPI or OSPM (e.g., Win98, Window 2000). <b>Note: When Enabled, no other option in the Power Management Setup will be used.</b>
Power Management	User Def.	User Def.	User Define, Min Saving, Max Saving	This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. <b>Max Saving:</b> Maximum power savings. Inactivity period is 1 minute in each mode. <b>Min Saving:</b> Minimum power savings. Inactivity period is the maximum setting in each mode (1 hour for Doze, Standby and Suspend). <b>User Define:</b> Set each mode individually. Select time-out periods in the PM Timers section (see below).
PM Control by APM	Yes	Yes	Yes, No	If Yes, the OS will control the PM by APM calls. If No, the BIOS will control the PM and APM calls from the OS will be ignored.
Video Off Method	V/H SYNC + Blank	V/H SYNC + Blank	Blank Screen V/H SYNC+Blank, DPMS,	Determines the manner in which the monitor is blanked. <b>V/H SYNC + Blank:</b> System turns off vertical and horizontal synchronization ports and writes blanks to the video buffer. <b>DPMS Support:</b> Select this option if your monitor supports the Display Power Management Signalling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsystem to select video power management values. <b>Blank Screen:</b> System only writes blanks to the video buffer.
Video Off After	Stand by	Stand by	NA, Suspend, Standby, Doze,	As the system moves from lesser to greater power-saving modes, select the mode in which you want the monitor to blank.
Doze Mode	Dis.	Dis	Disable 1min to 1h	After the selected period of system inactivity (1 minute to 1 hour), the CPU clock runs at lower speed while all other devices still operate at full speed.
Standby Mode	Dis.	Dis.	Disable 1min to 1h	After entering Doze mode and the selected period of system inactivity (1 minute to 1 hour) has elapsed, some devices shuts off while all other devices still operate at full speed.
Suspend Mode	Dis.	Dis.	Disable 1min to 1h	After entering Standby mode and the selected period of system inactivity (1 minute to 1 hour) has elapsed, all devices including the CPU shut off and the system waits for an event to wake them up again.
HDD Power Down	Dis.	Dis.	Disable 1-15min	After the selected period of drive inactivity (1 to 15 minutes), the hard disk drive powers down while all other devices remain active. The HDD power down mode is only available if the hard drive has this capability.
HDD Down When Suspend	En.	En.	En./Dis.	When Enabled and the system goes in Suspend Mode, the hard disk is shut down.
Throttle Duty Cycle	75.0%	75.0%	12.5%-75.0%	When the system enters Doze mode, the CPU clock runs only part of the time. You may select the percentage of time that the clock does not run.
PCI/VGA Act-Monitor	Dis.	Dis.	En./Dis.	When Enabled, continuous video activity restarts the global timer for Standby mode.
Soft-OFF by PWR-BTTN  Note: This option is not available on T9003 rev0 and rev 1	Delay 4 sec	Delay 4 sec	Delay 4 sec. Instant-off,	This option only works with an ATX power supply. It allows two configurations for the power button: Instant-off for power supply on/off switch, or Delay 4 sec. for entering Suspend Mode after pressing the button at least 4 seconds.
PWRON After PWR-Fail  Note: This option is not available on T9003 rev0 and rev 1	Last-State	Last-State	Last-State On Off	Select the power-on status desired after power fail: Last-State – the board will power on or off according to the last power Status when power fail. On – Always power-on after power fail Off – Always power-off after power fail Note: if Last-State is selected, make a save cmos and then shutdown the board (AC-OFF for about 5sec-30sec depending on the power supply type to make sure the V-Standby is off for proper activating of this option). Depending on the power supply, Last State functionality might be affected by a short power failure.

## Power Management Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Resume by Ring	Dis.	En.	En./Dis.	When Enabled and a modem is connected to a COM port, allows a modem ring to re-activate the CPU when in Suspend mode.
IRQ 8 Break Suspend	Dis.	En.	En./Dis.	When Enabled, the RTC alarm interrupt is monitored to allow an interrupt to awaken the system when in Doze, Standby or Suspend Mode.
Resume by Alarm	Dis.	Dis.	En./Dis.	When Enabled, allows setup of a time to re-activate the CPU when in Suspend mode with the options Date (of Month) Alarm and Time (hh:mm:ss) Alarm. <b>Note: The IRQ 8 Break Suspend option in this setup screen must be Enabled to use the RTC alarm.</b>
Reload Global Timer Events:				
IRQ[3-7,9-15], NMI	Dis.	En.	En./Dis.	When any of the options below is Enabled, monitoring of the interrupt will occur to allow an interrupt to awaken the system when in Doze, Standby or Suspend Mode.
Primary IDE 0	Dis.	En.	En./Dis.	
Primary IDE 1	Dis.	En.	En./Dis.	
Secondary IDE 0	Dis.	En.	En./Dis.	
Secondary IDE 1	Dis.	En.	En./Dis.	
Floppy Disk	Dis.	En.	En./Dis.	
Serial Port	En.	En.	En./Dis.	
Parallel Port	Dis.	En.	En./Dis.	

## 4.1.7 PnP/PCI Configuration

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
PnP OS Installed	Yes	No	Yes, No	If the operating system (OS) is Plug and Play (for example Windows 95), select "Yes" if you want the OS to allocate resources according to Plug and Play standards, or "No" if you want the same resource allocations at every system boot-up. Select "No" when the OS is not Plug and Play (for example, DOS). <b>Note: When set to "Yes", only the boot devices will get an IRQ.</b>
Resources Controlled By	Auto	Man.	Auto, Man.	The Award Plug and Play BIOS can automatically configure all the boot and Plug and Play-compatible devices. If you select Auto, all the interrupt requests (IRQs) and DMA assignment fields disappear, as the BIOS automatically assigns them.
Reset Configuration Data	Dis.	Dis.	En./Dis.	Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.
IRQ <i>n</i> Assigned To	PCI/ISA PnP	PCI/ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific interrupt, such as IRQ4 for serial port 1. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for an IRQ line, this resource will not be available for PCI/ISA PnP.
DMA <i>n</i> Assigned To	PCI/ISA PnP	PCI/ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system DMA channel as one of the following types, depending on the type of device using the DMA: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific DMA channel. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for a DMA channel, this resource will not be available for PCI/ISA PnP.
Init Display First	Onboard	Onboard	PCI Slot, Onboard, AGP (not supported)	Initializes the specified video display. The chosen display becomes the primary display. Other display devices are ignored by the BIOS and configured by the OS.
Assign IRQ For VGA	Dis.	Dis.	En./Dis.	When Enabled, the video card is assigned an IRQ.
Assign IRQ For USB	En.	En.	En./Dis.	When Enabled, the USB is assigned an IRQ. When Disabled, the IRQ is freed up for another purpose.
PCI Latency Timer	32	32	0-255 (integers)	This option specifies the value of the Latency Timer for the PCI bus master, in units of PCI bus clocks. Value must be a power of 2 (1, 2, 4, 8, 16, 32, 64, or 128).
Special PCI Routing	En.	En.	En./Dis.	Disable this option if the backplane into which the board is installed conforms to the PICMG specifications. When enabled the board will attempt to detect a special PCI routing configuration.
Bridge init. delay	150 ms	150 ms	150, 300, 600, 1200 ms	Extra delay to ensure proper PCI device reset.
Bridge cache size	16	16	0, 2, 8, 16	Set PCI burst buffer size. 16 means full cache line size.
Used MEM Base Address	N/A	N/A	N/A, C800, CC00, D000, D400, D800	Select a base address for the memory area used by any peripheral that requires high memory. This option is only available when resources are manually controlled.
Used MEM Length	16K	16K	16K, 32K, 48K, 64K	This option is available when <b>Used MEM Base Address</b> is not set at N/A. Select memory size used by peripheral at Used MEM Base Address

## 4.1.8 CPU/Board Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Current Processor(s) Speed	Various, depending on the installed CPU			This option displays the current processor speed.
Front Side Bus Speed				This option displays the current FSB speed.
Thermal Management Options				
Thermal Management	Dis.	Dis.	En./Dis.	When this option is enabled, the CPU temperature is monitored. Whenever the CPU overheats, the CPU slows down to lower the temperature.
Thermal Audio Alarm	Dis.	Dis.	En./Dis.	When the Thermal Management option and this option are enabled, a continuous audible alarm is sounded when the temperature specified in the Overheat Alarm options is reached. Such an alarm may not be supported by the Operating System.
CPU 1 Die Temp °C	-	-	Varies	Displays the current die (internal) CPU temperature, when Thermal Management is enabled.
Resume Alarm (°C)	70	70	50-80	The CPU will be slowed down (Doze mode) when it reaches the selected Overheat Alarm (°C) temperature.
Overheat Alarm (°C)	80	80	60-90	Full speed (Normal mode) will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 2° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm.
CPU Local Temp °C	-	-	Varies	Displays the current case (external) CPU temperature, when Thermal Management is enabled.
Resume Alarm (°C)	60	60	50-80	The CPU will be slowed down (Doze mode) when the selected Overheat Alarm (°C) temperature is reached.
Overheat Alarm (°C)	70	70	60-90	Full speed (Normal mode) will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 2° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm.
Save CMOS in Flash	Dis.	Dis.	En./Dis.	Saving CMOS memory content into Flash Memory will prevent to loose CMOS options when battery fails.
Watchdog Timer	Dis	Dis	En./Dis.	
Watchdog After POST	Dis.	Dis.	En./Dis.	This option enables Watchdog circuit after the POST sequence
Watchdog Duration (ms)	262144	262144	64 to 262144	Use this option to setup duration time (in ms) of the Watchdog timing circuitry.

## 4.1.9 Integrated Peripherals

Option	BIOS defaults	Setup Defaults	Possible Settings	Description
On-Chip Primary PCI IDE	En.	En.	En./Dis.	Select Enabled to activate the Primary/Secondary IDE channel. The four options below appear only if the On-Chip Primary option is enabled.
IDE Primary Master PIO IDE Primary Slave PIO IDE Secondary Master PIO IDE Secondary Slave PIO	Auto	Auto	Auto, Modes 0-4	Use this option to set a PIO mode (0-4) for each of the onboard IDE devices. Modes 0 through 4 provide successively increased performance and speed. In Auto mode, the system automatically determines the best mode for each device. If you select a mode that the drive does not support, it may not work, so choose a lesser value or Auto to see the best mode for the drive.
IDE Primary Master UDMA IDE Secondary Master UDMA IDE Primary Slave UDMA IDE Secondary Slave UDMA	Dis.	Auto	Auto, Disabled.	Ultra DMA/33 implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If your hard drive and your system software both support Ultra DMA/33, select Auto to enable BIOS support.
On-Chip Secondary PCI IDE:	En.	En.	En./Dis.	Select Enabled to activate the Secondary IDE channel. The four options below appear only if the On-Chip Secondary option is enabled.
IDE HDD Block Mode	Dis.	En.	En./Dis.	Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.
Onboard PCI SCSI BIOS	En.	En.	En./Dis.	Enables/disables the onboard SCSI controller BIOS without disabling the SCSI controller.
Onboard PCI SCSI Chip	En.	En.	En./Dis.	Enables/disables the onboard SCSI controller. This option is available only if <b>Onboard PCI SCSI BIOS</b> is disabled.
Ethernet Controller	En.	En.	En./Dis.	Enables/disables the onboard Ethernet controller.
USB Keyboard Support	OS	OS	OS/BIOS	Select OS when support is provided by the operating system (WIN95 or later). Select BIOS to use USB keyboard without driver (DOS and BIOS support). <b>It does not enable or disable the USB controller.</b>
PS/2 Mouse Function Control	Auto	Auto	Auto/Dis.	When set to Auto, the PS/2 mouse is automatically enabled, if it is present.
Onboard FDC Controller	En.	En.	En./Dis.	Select Disabled to disable the onboard floppy disk controller (FDC).
Onboard Serial Port 1/2	Auto	Auto	Dis., 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3, Auto	Select a COM port address and IRQ# for the first and second serial ports.
Serial Port 2 Mode	RS-232	RS-232	RS-232,RS-422, and RS-485	Select the operation mode for Serial Port 2.
Onboard Parallel Port	378/IRQ7	378/IRQ7	Disabled, 3BC/IRQ7, 378/IRQ7, 278/IRQ5,	Select a LPT address and IRQ# for the physical parallel (printer) port.
Parallel Port Mode	ECP + EPP1.9	ECP + EPP1.9	SPP, EPP1.9+SPP, ECP, ECP+EPP1.9, Normal, EPP1.7+SPP, ECP+EPP1.7	Select an operating mode for the onboard parallel port. Select ECP or EPP unless you are certain both your hardware and software does not support ECP or EPP mode.
ECP Mode Use DMA	3	3	1, 3	Select a DMA channel for the port.

## 4.2 Updating or Restoring the BIOS in Flash

The BIOS update procedure can be found with the Emergency Recovery procedure on our ftp site: <ftp://ftp.kontron.ca/Support> in the FAQ section:

Download the FAQ# KC\_0028 at location:

[ftp://ftp.kontron.ca/Support/Support\\_FAQ - Questions & Answers/](ftp://ftp.kontron.ca/Support/Support_FAQ_-_Questions_&_Answers/)

## 4.3 VT100 Mode

The VT100 operating mode allows remote setups of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

### 4.3.1 Requirements

The terminal should emulate a VT100 or ANSI terminal. Terminal emulation programs such as Telix<sup>®</sup> or Procom<sup>®</sup> can also be used.

### 4.3.2 Setup & Configuration

Follow these steps to set up the VT100 mode:

1. Connect a monitor and a keyboard to your board and turn on the power.
2. Enter into the CMOS Setup program in the “BIOS Feature Setup”
3. Set the jumper W9 to “ON” position
4. Select the VT100 mode and the appropriate COM port and save your setup.
5. Connect the communications cable as shown in the next page.

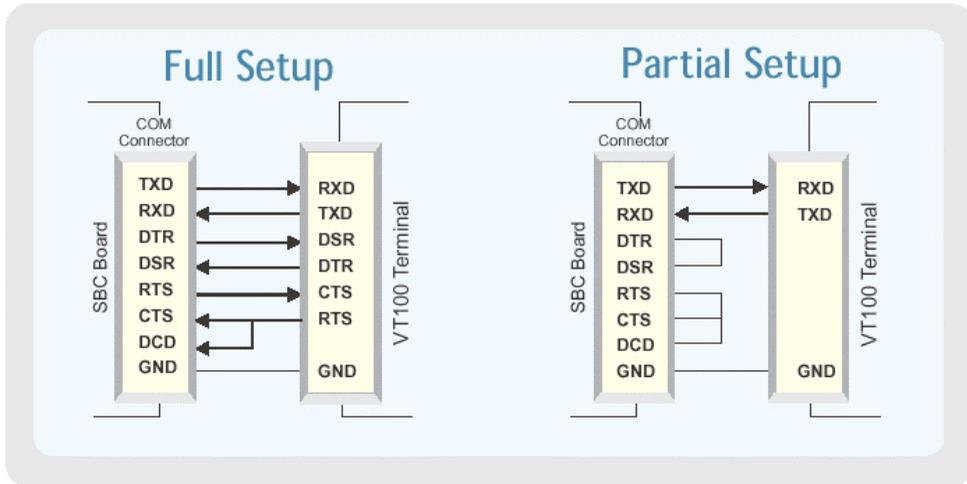


#### **NOTE**

If you do not require a full cable for your terminal, you can set up a partial cable by using only the TXD and RXD lines. To ignore control lines simply loop them back as shown in VT100 Partial Setup cable diagram.

- 6 Configure your terminal to communicate using the same parameters as in CMOS Setup.
- 7 Reboot the board.
- 8 Use the remote keyboard and display to setup the BIOS.

Save the setup, exit, and disconnect the remote computer from the board to operate in stand-alone configuration.



### 4.3.3 Running Without a Terminal

The board can boot up without a screen or terminal attached. If the speed is set to Auto and no terminal is connected, the speed is set to 115,200 bauds.

Furthermore, you can run without any console at all by simply not enabling VT100 Mode and by disabling the onboard video.

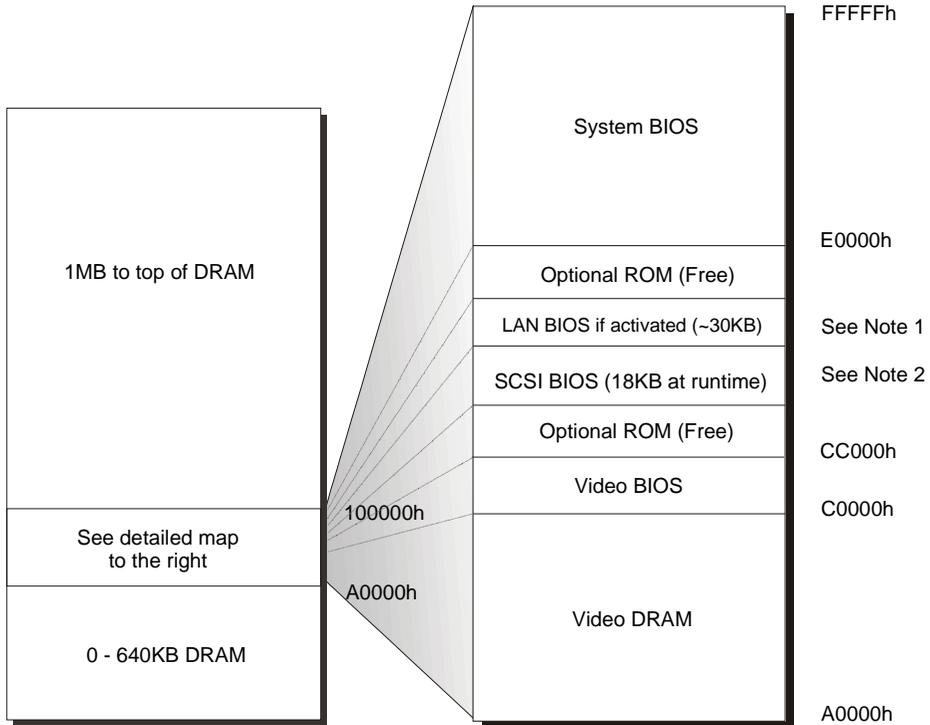
## APPENDICES

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- A. MEMORY & I/O MAPS
  - B. IRQ AND DMA LINES
  - C. BOARD DIAGRAMS
  - D. CONNECTOR PINOUTS
  - E. BIOS SETUP ERROR CODES
  - F. EMERGENCY PROCEDURE
  - G. GETTING HELP & RMA
-

# A. MEMORY & I/O MAPS

## A.1 Memory Mapping



Note 1 : LAN BIOS address may vary

Note 2 : SCSI BIOS address may vary.  
Size is only 2KB if no device.

Address	Function
00000-9FFFF	0-640 KB DRAM
A0000-BFFFF	Video DRAM
C0000-CBFFF	Video BIOS
CC000-DFFFF	Optional ROM (Free)
	LAN BIOS around 30KB if activated, address may vary
	SCSI BIOS 18KB at runtime, 2KB if no device, address may vary
E0000-FFFFF	System BIOS
100000-Top of DRAM	1 MB - Top of DRAM

## A.2 I/O Mapping

Address	Optional Address	Optional Address	Optional Address	Function
000-01F				DMA Controller 1
020-03F				Interrupt Controller 1
040-05F				Timer
060-06F				Keyboard
070-07F				Real-time clock
080-09F				DMA Page Register
0A0-0BF				Interrupt Controller 2
0C0-0DF				DMA Controller 2
0F0-0F1, 0F8-0FF				Math Coprocessor
190-19F	290-29F	390-39F		Kontron Control Port
1F0-1F7, 3F6				Primary IDE
3F0-3F7	370-377			Floppy Disk
378-37A	3BC-3BE	2787-27A		Parallel Port (LPT1 by default)
3F8-3FF (COM1)	2F8-2FF (COM2)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 2 (COM2 by default)
3C0-3CF, 3D0-3DF, 3B0-3BB				Graphics Controller (I2C Port)

## B. IRQ AND DMA LINES

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### B.1 IRQ Lines

The board is fully PC compatible with interrupt steering for PCI plug and play compatibility.

Controller # 1		Controller # 2	
IRQ 0	Timer Output 0	IRQ 8	Real-Time Clock
IRQ 1	Keyboard	IRQ 9	Available <sup>1</sup>
IRQ 2	Cascade Controller # 2	IRQ 10	Available <sup>1</sup>
IRQ 3*	Serial Port 2	IRQ 11	Available <sup>1</sup>
IRQ 4*	Serial Port 1	IRQ 12	PS/2 Mouse
IRQ 5*	Available <sup>1</sup>	IRQ 13	Coprocessor Error
IRQ 6*	Floppy Controller	IRQ 14	Primary IDE or available <sup>1</sup>
IRQ 7*	Parallel Port 1 or Available <sup>1</sup>	IRQ 15	N/C

\*: All functions marked with an asterisk (\*) can be disabled or reconfigured.

<sup>1</sup> Available lines service on board and external PCI/ISA PnP devices or a Legacy ISA device.

### B.2 DMA Channels

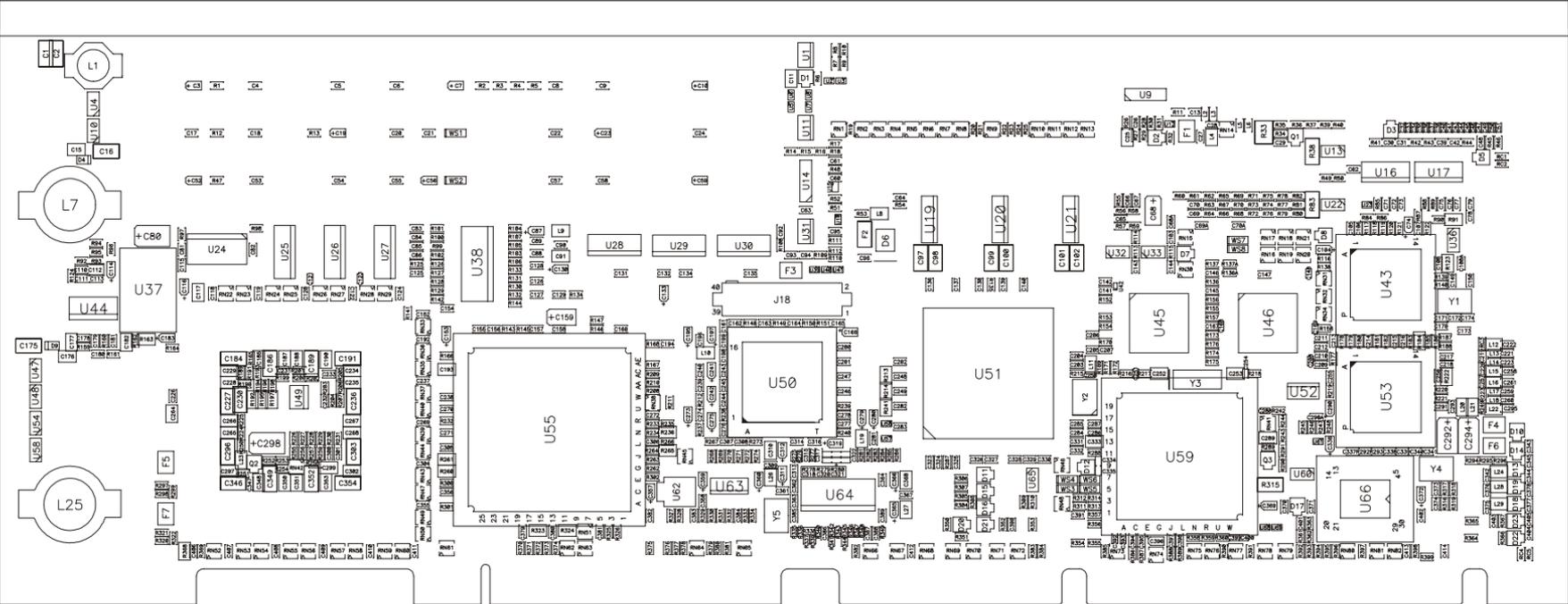
The PCI-949 integrates the functionality of two 8237 DMA controllers. Seven DMA channels are available (channel #4 unavailable).

According to Plug and Play standards, the system BIOS automatically allocates DMA Channel 1 or 3 for the parallel port's ECP mode. Channel 2 is reserved for the floppy controller and Channel 4 is used to cascade Channels 5 through 7 to the microprocessor.

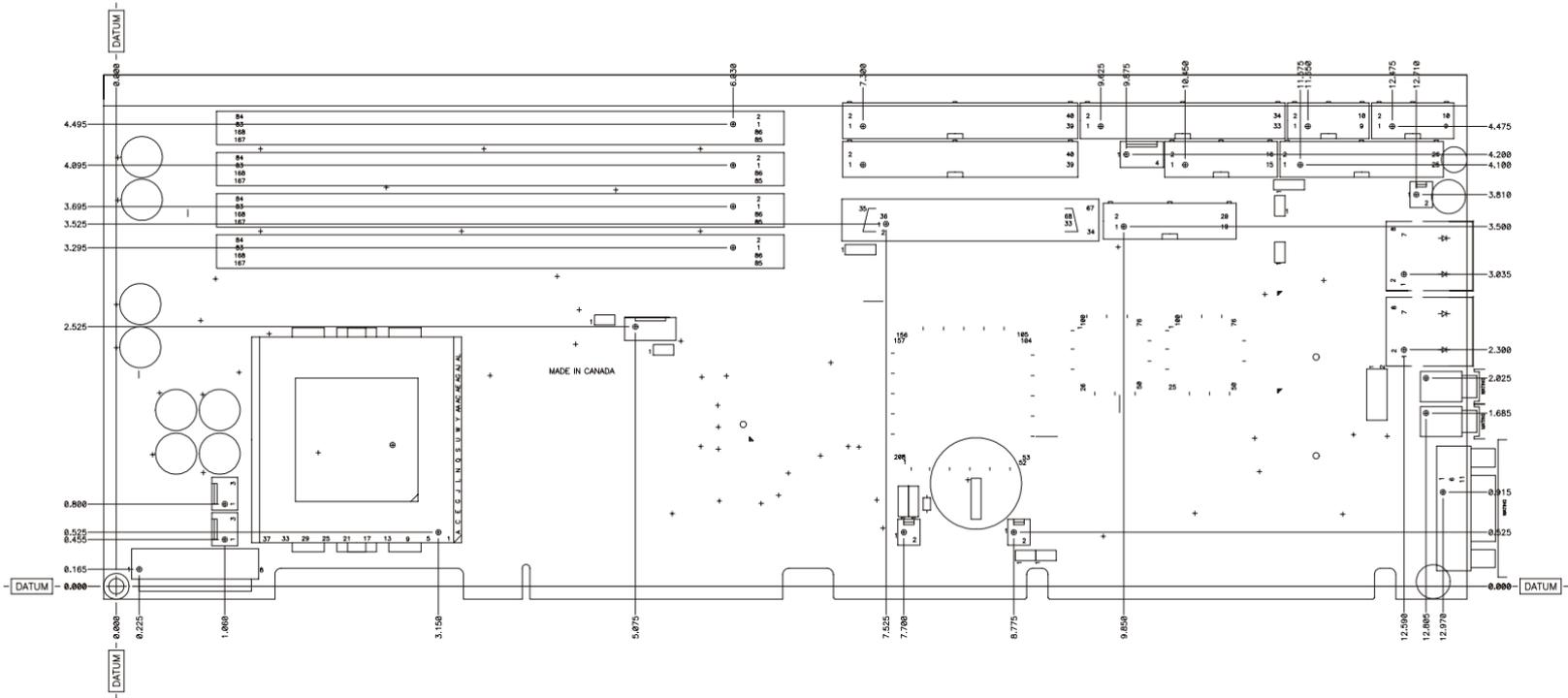
DMA Channel	Function
DMA 0	Available
DMA 1	PnP available (ECP)
DMA 2	Floppy controller
DMA 3	PnP available (ECP)
DMA 4	Cascade controller # 1
DMA 5	PnP available
DMA 6	PnP available
DMA 7	PnP available

# C. BOARD DIAGRAMS

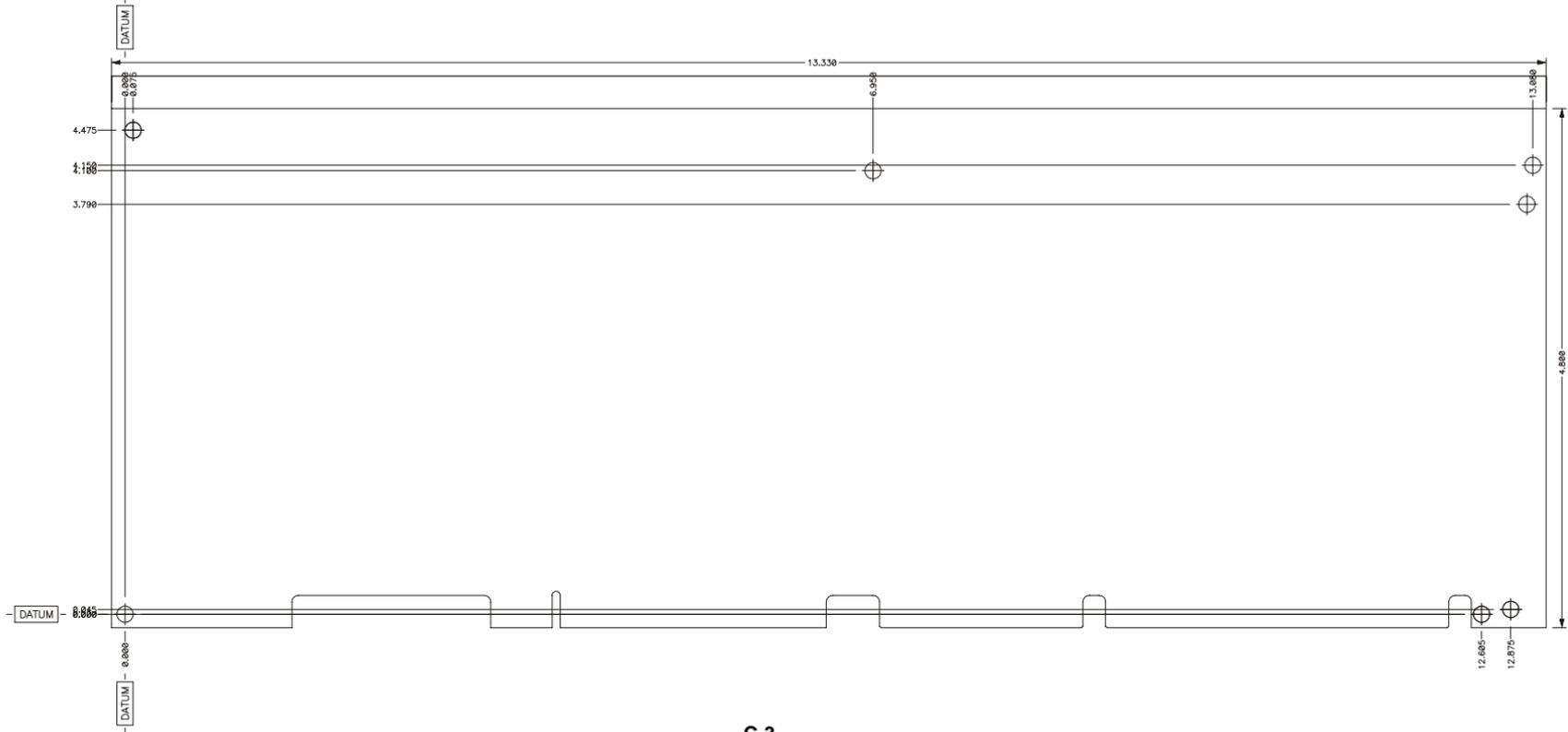
## C.1 Assembly Top - PCI-949



### C.2 Connector Configuration C.S. - PCI-949



### C.3 Mounting Holes - PCI-949



## D. CONNECTOR PINOUTS

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### D.1 PCI-949 Connectors and Headers

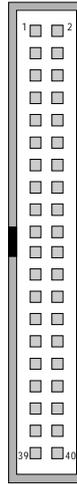
Connectors and Headers on the PCI-949	
J1, J6, J11, J15	DIMM Memory
J2	Primary IDE Connector
J3	Floppy Disk Connector
J4	Serial Port 1 – RS232
J5	Serial Port 2 – RS232 / RS485/RS422
J7	Secondary IDE
J8	Mouse Port
J9	Multifunction Header (keyboard, speaker, etc.)
J10	Parallel Port
J12	Power Button
J13	SCSI
J14	Hardware Monitor Header
J16	Ethernet 0
J18	CompactFlash Disk
J19	Ethernet 1
J21	USB 0
J22	USB 1
J23	Video (SVGA)
J24	CPU Fan 2
J25	CPU Fan 1
J26	External Battery Connector
J27	SCSI LED
J28	External Power

## D.2 J2/J7 - Primary/Secondary IDE Connectors

Pin Number	
Signal	
RST#	1
D7	3
D6	5
D5	7
D4	9
D3	11
D2	13
D1	15
D0	17
GND	19
REQ	21
IOW#	23
IOR#	25
IORDY	27
DACK#	29
IRQ	31
A1	33
A0	35
CS0#	37
ACT#	39

# Active Low Signal

Top View



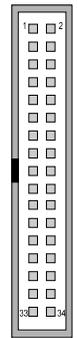
Pin Number	
Signal	
2	GND
4	D8
6	D9
8	D10
10	D11
12	D12
14	D13
16	D14
18	D15
20	N.C.
22	GND
24	GND
26	GND
28	PRIMPDI
30	GND
32	N.C.
34	DIAG#
36	A2
38	CS1#
40	GND

## D.3 J3 – Floppy Disk

Pin Number	
Signal	
GND	1
GND	3
GND	5
GND	7
GND	9
GND	11
GND	13
GND	15
N.C.	17
GND	19
GND	21
GND	23
GND	25
N.C.	27
FDetect	29
GND	31
N.C.	33

# Active Low Signal

Top View

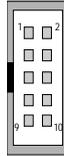


Pin Number	
Signal	
2	DENSEL#
4	N.C.
6	N.C.
8	INDEX#
10	MTR0#
12	DSEL1#
14	DSEL0#
16	MTR1#
18	DIR#
20	STEP#
22	WDATA#
24	WGATE#
26	TRK0#
28	WRPROT#
30	RDATA#
32	HSEL#
34	DSKCHG#

### D.4 J4, J5 – Serial 1, 2 – RS232

Pin Number	
Signal	
DCD	1
RXD	3
TXD	5
DTR	7
GND	9

Top View

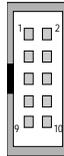


Pin Number	
Signal	
DSR	2
RTS	4
CTS	6
RI	8
N.C.	10

### D.5 J5– Serial Port 2 - RS-485

Pin Number	
Signal	
RSV	1
RX(-)	3
TX(-)	5
RSV	7
GND	9

Top View



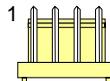
Pin Number	
Signal	
RSV	2
RX(+)	4
TX(+)	6
RSV	8
N.C.	10

# Active Low Signal

### D.6 J8 – PS/2 Mouse Header

Signal	Pin
MOUSE:CLK	1
GND	2
MOUSE:DATA	3
VCC	4

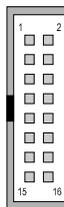
Front View



### D.7 J9 – Multifunction Header

Pin Number	
Signal	
KB:CLK	1
KB:DATA	3
VCC	5
N.C.	7
DOWNLD#	9
PBRES#	11
IDE :ACT#	13
	15

Top View



Pin Number	
Signal	
GND	2
GND	4
VCC	6
VCC	8
GND	10
GND	12
GND	14
VCC	16

#Active Low Signal

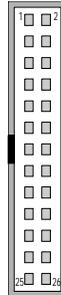
## D.8 J10 – Parallel Port

### D.8.1 Standard Mode

Pin Number	
Signal	
STB#	1
D0	3
D1	5
D2	7
D3	9
D4	11
D5	13
D6	15
D7	17
ACK#	19
BUSY	21
PE	23
SLCT	25

# Active Low Signal

Top View



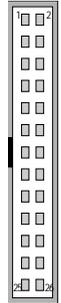
Pin Number	
Signal	
2	ALF#
4	ERR#
6	INIT#
8	SLCTIN#
10	GND
12	GND
14	GND
16	GND
18	GND
20	GND
22	GND
24	GND
26	GND

### D.8.2 EPP Mode

Pin Number	
Signal	
WRITE#	1
D0	3
D1	5
D2	7
D3	9
D4	11
D5	13
D6	15
D7	17
INTR	19
WAIT#	21
N.C.	23
N.C.	25

# Active Low Signal

Top View

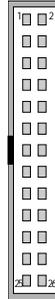


Pin Number	
Signal	
2	DATASTB#
4	N.C.
6	N.C.
8	ADDRSTRB#
10	GND
12	GND
14	GND
16	GND
18	GND
20	GND
22	GND
24	GND
26	GND

### D.8.3 ECP Mode

Pin Number	
Signal	
STROBE#	1
D0	3
D1	5
D2	7
D3	9
D4	11
D5	13
D6	15
D7	17
ACK#	19
BUSY, PERIPHACK <sup>2</sup>	21
PERROR, ACKREVERSE <sup>2</sup>	23
SELECT	25

Top View



Pin Number	
Signal	
AUTOFD#, HOSTACK <sup>2</sup>	2
FAULT# <sup>1</sup> , PERIPHRQST# <sup>2</sup>	4
INIT# <sup>1</sup> , REVERSERQST# <sup>2</sup>	6
SELECTIN# <sup>1,2</sup>	8
GND	10
GND	12
GND	14
GND	16
GND	18
GND	20
GND	22
GND	24
GND	26

# Active Low Signal, <sup>1</sup> Compatible Mode, <sup>2</sup> High Speed Mode

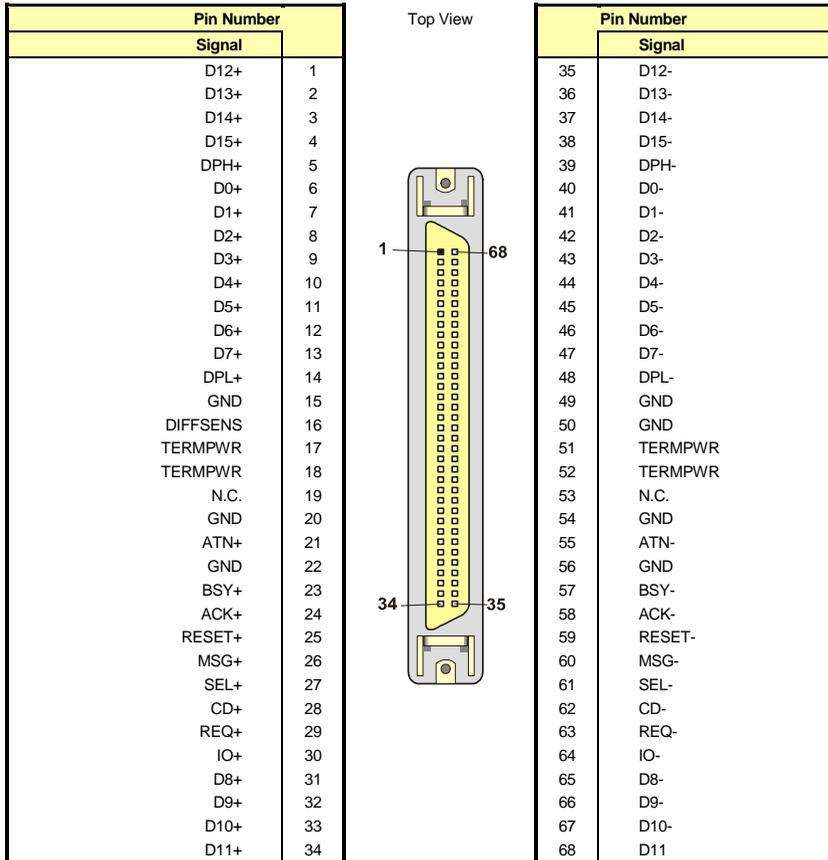
### D.9 J12 – Power Button Connector

Signal	Pin
PWRBTN	1
GND	2

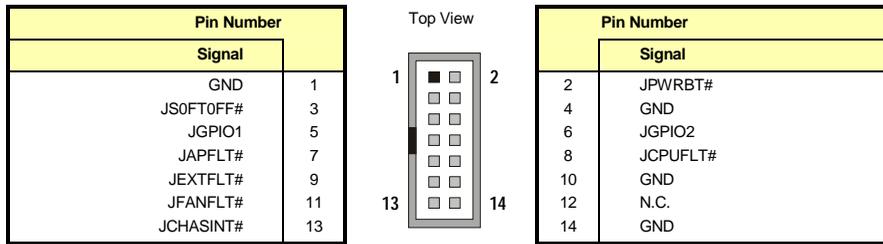
Top View



## D.10 J13 - SCSI Connector



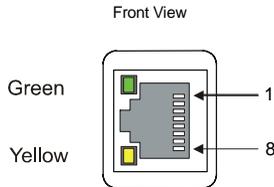
## D.11 J14 – Hardware Monitor Header



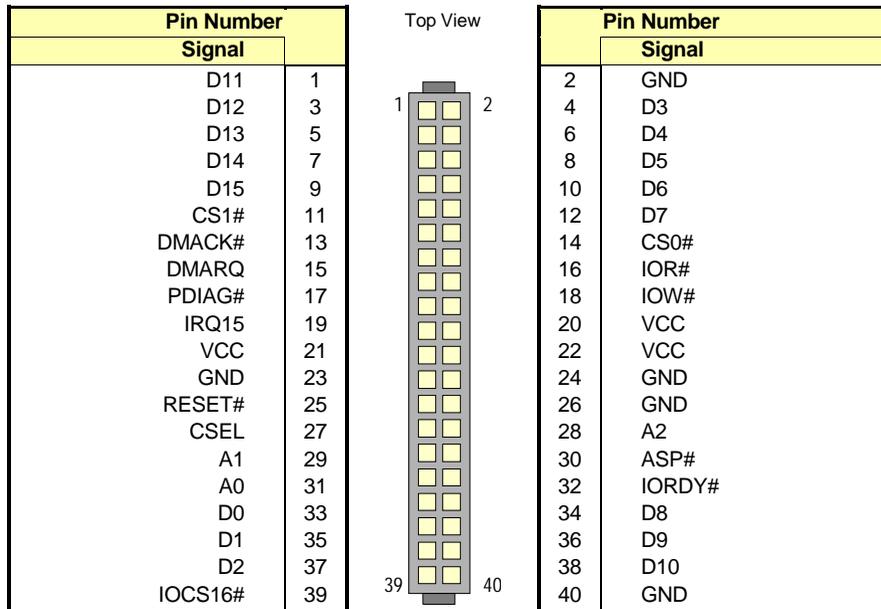
#Active Low Signal

## D.12 J16, J19 – Ethernet 0 and 1, RJ45 Connector (Face Plate)

Signal	Pin
TX+	1
TX-	2
RX+	3
75 ohm line termination	4
75 ohm line termination	5
RX-	6
75 ohm line termination	7
75 ohm line termination	8

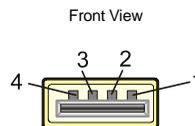


### D.13 J18 – CompactFlash™



### D.14 J21, J22 – USB 1 and 2 Connectors (Face Plate)

Signal	Pin
VCC	1
DATA-	2
DATA+	3
GND	4

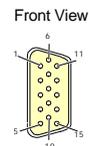


### D.15 J23 - CRT VGA Connector (Face Plate)

Signal	Pin
RED	1
GREEN	2
BLUE	3
N.C.	4
GND	5

Signal	Pin
Analog GND	6
Analog GND	7
Analog GND	8
N.C.	9
GND	10

Signal	Pin
N.C.	11
SDATA	12
HSYNC	13
VSYNC	14
SCLK	15

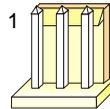


## D.16 J24, J25 – CPU Fan 2 and 1

Note : J24 initiates an NMI if the CPU fan stops. This option is not available on J25.

Signal	Pin
SENSE	1
+5V	2
GND	3

Front View



## D.17 J26 – External Battery Connector

Signal	Pin
Battery (+)	1
Battery (-)	2

Front View



## D.18 J27 – SCSI LED Connector

Signal	Pin
Anode (+)	1
Cathode (-)	2

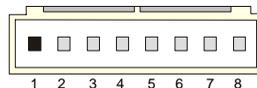
Front View



## D.19 J28 – External Power Supply Connector

Signal	Pin
VCC	1
VCC	2
-5V	3
GND	4

Top View



Pin	Signal
5	GND
6	GND
7	-12V
8	+12V

## E. BIOS SETUP ERROR CODES

---

### E.1 POST Beep

POST beep codes are defined in the BIOS to provide low level tone indication when an error occurs during the BIOS initialization.

Beep codes consist of a combination of long and short beeps. They are described as follows:

#### E.1.1 Beep Codes

Post code	Beep Code	Description
41	**_*	Entering the boot block recovery code (i.e. Main BIOS checksum error)

**Legend**      \* = 1 Short beep code, \*\* = 1 Long beep code, - = Silence

### E.2 POST Messages

During the Power-On Self-Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

**"PRESS F1 TO CONTINUE, DEL TO ENTER SETUP".**

## **E.3 Error Messages**

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

### **CMOS BATTERY HAS FAILED**

CMOS battery is no longer functional. It should be replaced.

### **CMOS CHECKSUM ERROR**

Checksum of CMOS is incorrect. This indicates that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

### **DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER**

No boot device was found. This could mean either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Floppy Drive A and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

### **KEYBOARD ERROR OR NO KEYBOARD PRESENT**

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to **HALT ON ALL, BUT KEYBOARD**. This will cause BIOS to ignore the missing keyboard and continue the boot.

### **OFFENDING SEGMENT**

This message is used in conjunction with the **I/O CHANNEL CHECK** and **RAM PARITY ERROR** messages when the segment that has caused the problem cannot be isolated.

### **PRESS F1 TO DISABLE NMI, F2 TO REBOOT**

When BIOS detects a Non-Maskable Interrupt condition, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

## E.4 POST Codes

POST #	Designation	Description		
01	BOOT BLOCK	Boot Block in <b>EMERGENCY</b> : Clear Base Memory Area.		
03	Initialize Chips	<ol style="list-style-type: none"> <li>1. Clear CMOS shutdown byte.</li> <li>2. Initialize EISA extended registers. (Not for us since we don't have EISA bus.)</li> </ol>		
04	Test Memory Refresh Toggle	RAM must be periodically refreshed in order to keep the memory from decaying.		
05	Blank Video, Initialize Keyboard	<table border="1"> <tr> <td> <ol style="list-style-type: none"> <li>1. Clear CMOS reset status byte.</li> <li>2. Early Keyboard initialization.</li> </ol> </td> <td>           Boot Block in <b>EMERGENCY</b>:            Initialize Keyboard Controller.         </td> </tr> </table>	<ol style="list-style-type: none"> <li>1. Clear CMOS reset status byte.</li> <li>2. Early Keyboard initialization.</li> </ol>	Boot Block in <b>EMERGENCY</b> : Initialize Keyboard Controller.
<ol style="list-style-type: none"> <li>1. Clear CMOS reset status byte.</li> <li>2. Early Keyboard initialization.</li> </ol>	Boot Block in <b>EMERGENCY</b> : Initialize Keyboard Controller.			
06	EPROM Checksum	<ol style="list-style-type: none"> <li>1. Test F000h segment shadow readable and writeable for POST access correct. If not, show POST FE and beep continuously...</li> <li>2. Autodetect Flash EPROM.</li> </ol>		
07	Test CMOS Interface and Battery Status	<ol style="list-style-type: none"> <li>1. Install the Kontron segment.</li> <li>2. Verifies CMOS is working correctly (walking bit test).</li> <li>3. Restore CMOS from Flash if option is enabled.</li> <li>4. Check for OVERRIDE KEY (INSERT key).</li> </ol>		
08	Program Chipset default	Program Chipset default (show POST BEh).		
09	Early Cache Initialization	<ol style="list-style-type: none"> <li>1. Check for Intel's and/or Cyrix CPU.</li> <li>2. Early Cache Initialization when cache is separate from chipset.</li> <li>3. Turn off Gate A20.</li> </ol>		
0A	Setup Interrupt Vector Table	<ol style="list-style-type: none"> <li>1. Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize int. 00h-1Fh according to INT_TBL.</li> <li>2. Early Power Management Initialization.</li> </ol>		
0B	Test CMOS RAM Checksum	<ol style="list-style-type: none"> <li>1. Verify time and date for valid values.</li> <li>2. If Override enabled, check for Override key. If Override key pressed, Kill CMOS checksum.</li> <li>3. Check CMOS Battery (useless if save CMOS in FLASH enabled since it's already done).</li> <li>4. Verify Checksum, if bad, load defaults.</li> <li>5. Copy CMOS in the stack.</li> <li>6. Clear CMOS Alarm date.</li> <li>7. Clear HD if Hidden.</li> <li>8. Clear Floppy "B" if only one drive.</li> <li>9. Detect for a Math Co-processor.</li> <li>10. Set Fast Gate A20 Flag in CMOS.</li> <li>11. If "B" drive only is set the 2 Drive are set...</li> <li>12. Program Chipset for early Power Management.</li> <li>13. P6 Bios Update (if applicable).</li> <li>14. Kill Onboard PnP IO.</li> <li>15. PnP Early Initialization.</li> <li>16. PnP System Resource:             <ol style="list-style-type: none"> <li>1. Get ESCD.</li> <li>2. Create default SYSTEM_MAP.</li> <li>3. Decode/Record ISA ESCD resources.</li> <li>4. Record I/O port for PnP operation.</li> </ol> </li> <li>17. Chipset Early Shadow.</li> </ol>		

## E.4 POST Codes (continued)

POST #	Designation	Description	
0C	Initialize Keyboard	1. Open Xilinx I/O Port location to x90h (X=1,2 or 3) inside the chipset (if necessary).	Boot Block 1 <sup>st</sup> : Verify BIOS checksum.
		2. Disable (if necessary). Thermal Management. 3. Disable (if necessary) Ethernet Chip.Set IDE Detect counter to 0. 4. Set CD-ROM found variable to 0. 5. Initialize zone 40:0h for the keyboard buffer.	Boot Block in EMERGENCY 2 <sup>nd</sup> : Init. vector 00h through 77h.
0D	Initialize Video Interface & Chipset	1. On M1 set the cache for the memory installed. 2. On PCI, do a PCI ROM init. 3. On P6, Init. Apic. 4. Init. Chipset. 5. Turn ON CPU Cache. 6. Set Maximum Speed. 7. Measure CPU Clock Speed. 8. Restore Speed. 9. Turn Off CPU Cache. 10. Early Video Shadow. 11. Read CMOS location 14h to find out type of video to use. Detect and initialize Video Adapter. 12. Init. T380 if necessary.	Boot Block in EMERGENCY: Try to init. Video Card...
0E	Test Video Memory	1. If CGA or MONO, test video memory. 2. Beep the speaker. 3. Show the LOGO. 4. Install VT100 driver if necessary. 5. Write sign-on message to screen. 6. Write Copyright message to screen. 7. Write Evaluation message to screen. 8. Show CPU type and speed.	
0F	Test DMA Controller 0	Test DMA Controller 0.	
10	Test DMA Controller 1	Test DMA Controller 1.	
11	Test DMA Page Registers	Test DMA Page Registers.	
12	Reserved	Reserved for 8254 Counter 0 - Not implemented.	
13	Reserved	Reserved for 8254 Counter 1 - Not implemented.	
14	Test Timer Counter 2	Test 8254 Timer 0 Counter 2.	
15	PIC Test 8259-1 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	
16	PIC Test 8259-2 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	

## E.4 POST Codes (continued)

POST #	Designation	Description	
17	Test Struck 8259's Interrupt Bits	Nothing	
18	Test 8259 Interrupt functionality	Force an interrupt and verify that the interrupt occurred (IRQ 0 - clock int. 8h).	
19	Test Struck NMI Bits (Parity/ IO check)	Nothing.	
1A-1E	Reserved	Reserved	
1F	Set EISA Mode	If EISA non-volatile memory checksum is good, execute EISA initialization. If no, execute ISA test and clear EISA mode flag. Test EISA Configuration Memory integrity (checksum & communication interface).	
20-2F	Enable Slots 0-15	Initialize slot 0 (System Board) to slot 15.	
30	Size Base & Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB.	
31	Test Base & Extended Memory	<ol style="list-style-type: none"> <li>Test base memory from 256K to 640K and extended memory above 1MB using various patterns.</li> <li>The last test is filling memory with 0's.</li> <li>On a quick memory test or if user press the ESC key while testing memory, only the last test is performed.</li> </ol>	
32	Test EISA Extended Memory	<p>If EISA Mode flag is set, then test EISA memory found in slots Initialization.</p> <p>NOTE 1: This will be skipped in ISA mode.</p> <p>NOTE 2: This POST also Detect &amp; Report I/O PORTS and also Init. Super IO.</p>	
33-3C	Reserved	Reserved	
3C	Setup Enable		
3D	Initialize & Install PS/2 Mouse	Detect if mouse is present. Initialize mouse. Install interrupt vector.	
3E	Setup Cache Controller	Initialize cache controller.	
3F-40	Reserved	Reserved	
41	Initialize Floppy Drive & Controller	<ol style="list-style-type: none"> <li>Verify if we should enter setup. If so, enter setup.</li> <li>Initialize floppy disk drive controller and any drive.</li> </ol>	Boot Block <b>in EMERGENCY</b> : Scan for Floppy for emergency disk...
42	Initialize Hard Drive & Controller	Initialize hard drive controller and any drive. (Call HD_INSTALL).	
43	Detect & Initialize Serial/Parallel/Joystick ports	Initialize any serial, parallel and game ports.	
44	Reserved	Reserved	
45	Detect & Initialize Math Coprocessor	Initialize Math Coprocessor.	
46	Reserved	Reserved	
47	Set Speed for Boot	Set Speed for Boot.	
48-4C	Reserved	Reserved	
4D	Init. PC-Speaker to LINE OUT	Enable access to PC-Speaker to LINE OUT and Enable/Disable it. (T934).	
4E	Manufacturing POST Loop or display Messages	<ol style="list-style-type: none"> <li>Reboot if Manufacturing POST Loop pin is set.</li> <li>Otherwise display any messages (i.e., any non-fatal errors that were detected during POST).</li> <li>Enter SETUP if needed.</li> </ol>	
4F	Security Check	Ask password security if needed.	
50	Write CMOS	Write all CMOS values back to CMOS-RAM and clear screen.	

## E.4 POST Codes (continued)

POST #	Designation	Description
51	Pre-Boot Enable	<ol style="list-style-type: none"> <li>1. Enable Parity checker.</li> <li>2. Enable NMI.</li> <li>3. Enable cache before boot.</li> </ol>
52	Initialize Option (ROM scan)	<ol style="list-style-type: none"> <li>1. Call POST 81</li> <li>2. Initialize any ROMs present from C8000h to DBFFFh. Disable POST code from segment E0000h.</li> <li>3. Initialize any ROMs present from DC000h to E0800h.</li> </ol> <p>NOTE: When FSCAN option is enabled, will initialize from C8000h to F7FFFh.</p>
53	Initialize Time Value	Initialize Time value in 40h: BIOS area.
54-5F	Reserved	Reserved
60		Store boot partition of head & cylinder.
61	Final Init	For last $\mu$ s detail before boot.
62	Num Lock ON	Put Num Lock ON and Daylight Saving.
63	Boot Attempt	<ol style="list-style-type: none"> <li>1. Call POST 82.</li> <li>2. Set Low stack.</li> <li>3. Boot via int 19h.</li> </ol>
64-7F	Reserved	Reserved
80	Kontron Segment Move 1	Install the Kontron segment from Flash to DC00:0h.
81	Kontron Segment Move 2	Install the Kontron segment from DC00:0h to 7000:0h.
82	Kontron Segment Move 3	Install the Kontron segment from 7000:0h to EC00:0h.
83	Check & Program CPLD	Check & Program CPLD for valid UserCode & IDCode.
84	Kontron CRC Check	Check if Kontron block has a valid CRC. If not, the Emergency procedure is launched.
85-AF	Reserved	Reserved
B0	Spurious	If interrupt occurs in protected mode.
B1	Unclaimed NMI	If unmasked NMI occurs, display: Press F1 to disable NMI, F2 reboot.
B2-BD	Reserved	Reserved
BE	Early Prog Chipset Def.	Going to early program chipset to default values (called from POST_8s).
BF	Program Chip Set	Called early at POST 0Dh to program chipset from CT-TABLE.
C0	Turn ON/OFF Cache	OEM Specific - Cache control.
C1	Memory presence	OEM Specific - Test to size on-board memory test.
C2	Early Memory Initialization	OEM Specific - Board Initialization.
C3	Extended Memory Initialization	OEM Specific - Turn ON extended memory DRAM select.
C4	Special Display Switch Handling	OEM Specific - Display/Video switch handling so that display switch errors never occur.
C5	Early Shadow	OEM Specific - Early Shadow enable for fast boot.
C6	Cache Programming	OEM Specific - Routine for programming which region are cacheable.
C7	Reserved	Reserved
C8	Special Speed Switching	OEM Specific - Routine to handle speed switching.
C9	Special Shadow Handling	OEM Specific - Normal Shadow routine.

## E.4 POST Codes (continued)

POST #	Designation	Description
CA	Very Early Initialization	OEM Specific – Initialize hardware before any other hardware initialization.
CB-CF	Reserved	Reserved
D0	Power Management Full speed	Trying to go back or into full speed mode.
D1	Power Management -- Doze mode	Trying to go or in Doze mode.
D2	Power Management --Sleep mode	Trying to go or in Sleep mode.
D3	Power Management – Suspend mode	Trying to go or in Suspend mode.
D4-DF	Debug	Available POST codes for use by source code customers during development.
E0	Reserved	Reserved
E1-EE	Setup Page	Page 1 to Page 14
EF	Shadow Error	In POST 6 to signal a Shadow Error.
F0-FE	Reserved	Reserved
FF	Boot	The system is now booted or waiting for an OS.

## F. EMERGENCY PROCEDURE

---

Follow this procedure only in case of emergency such as a critical error occurred during the Boot Block Flash BIOS update (when using UBIOS utility program or if you meet one of the following symptoms at anytime:

1. No POST code on a power up (when using a POST card).
2. System stops at POST 41(when using a POST card) and associated beep code is generated (Refer to Section E.1).
3. Board does not boot, even after usual hardware and connection verifications.

Post code	Beep Code	Description
22	*-*	Error when getting the boot block flash ID code
33	*-*	Error when erasing the boot block flash
44	*-*	Error when programming the boot block flash
55	*-	<b>Success</b> of the boot block recovery code. The board is ready to be manually reset.

### F.1 How to run Emergency Procedure

To run an EMERGENCY PROCEDURE, proceed as follows:

1. Remove battery jumper.
2. Disable the Power Fail Detection function.
3. Connected a 1.44MB floppy drive (drive A) to the board, and insert the EMERGENCY diskette, that you previously created, in it.
4. Power on the board. (Note that no VGA is present during this procedure.)
5. Boot block flash update will be completed when the POST code 55 is displayed (when using a POST card) or the associated beep code sounds.
6. After the procedure is successfully completed, power down the board, install your battery and Power Fail Detection jumpers.

The boot block flash BIOS should be correctly programmed and the system should run properly.

 **NOTE** See Section F.2 Generate an Emergency Floppy Diskette.

## F.2 Generate an Emergency Floppy Disk :

Use a system that has a 1.44 Mbytes floppy drive A.

1. Insert the Kontron Emergency Diskette in drive A:
2. Copy the two files WDISK.COM and EMERDISK.TEK from drive A: to your hard drive (those files are available on Kontron's CDROM).
3. Insert a DOS formatted floppy disk in drive A.
4. At the DOS prompt of your hard drive (same path of the two files WDISK.COM and EMERDISK.TEK), type WDISK EMERDISK.TEK then press Enter key.
5. The program may display one of the following messages:

**"Emergency Code transferred"**

The emergency diskette has been successfully created. Take the appropriate actions and restart from the step 4) when you see the following messages.

**"Write to disk failure!"**

Verify if your floppy diskette is write-protected.

**"The file to program in flash was not found"**

Be sure that EMERDISK.TEK file is in your current path.

**"Unable to read the binary file" "Unable to close the opened file"**

Possible floppy diskette corruption or bad data transfer between floppy disk and host system.

**"Unable to allocate a memory block of 256 Kbytes"**

Not enough memory to run the WDISK program.

## **G. GETTING HELP**

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At Kontron, we take great pride in our customer's successes. We strongly believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, you may contact our Technical Support department at:

### **CANADIAN HEADQUARTERS**

Tel. (450) 437-5682

Fax: (450) 437-8053

If you have any questions about Kontron, our products or services, you may reach us at the above numbers or by writing to:

Kontron inc.  
616 Curé Boivin  
Boisbriand, Québec  
J7G 2A7 Canada

You can access our WEB site at : [www.kontron.com](http://www.kontron.com)

### **LIMITED WARRANTY**

KONTRON INC, ("The seller") warrants its boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts, which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

## RETURNING DEFECTIVE MERCHANDISE

If your Kontron product malfunctions, please do the following before returning any merchandise:

- 1) Call our Technical Support department in Canada at (450) 437-5682. Make certain you have the following at hand:
  - The Kontron Invoice number
  - Your purchase order number
  - The serial number of the defective board.
- 2) Give the serial number found on the back of the board and explain the nature of your problem to a service technician.
- 3) If the problem cannot be solved over the telephone, the technician will further instruct you on the return procedure.
- 4) Prior to returning any merchandise, make certain you receive an RMA number from Kontron's Technical Support and clearly mark this number on the outside of the package you are returning. To request a number, follow these steps:
  - Make a copy of the request form on the following page.
  - Fill out the form and be as specific as you can about the board's problem.
  - Fax it to us.
- 5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.
- 6) When returning a Kontron board:
  - i) Make certain that the board is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.
  - ii) Ship prepaid to (but not insured, since incoming units are insured by Kontron):

Kontron inc.  
616 Curé Boivin  
Boisbriand, Québec  
J7G 2A7 Canada



RETURN TO MANUFACTURER  
AUTHORIZATION REQUEST

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Contact Name	:	_____			
Company name	:	_____			
Street Address	:	_____			
City	:	_____	Province/State	:	_____
Country	:	_____	Postal/Zip Code	:	_____
Phone Number	:	_____	Extension	:	_____
Fax Number	:	_____			

Serial Number	Failure or Problem Description	P.O.# (if not under warranty)

**Fax this form to Kontron's Technical department in Canada at (450) 437-8053**