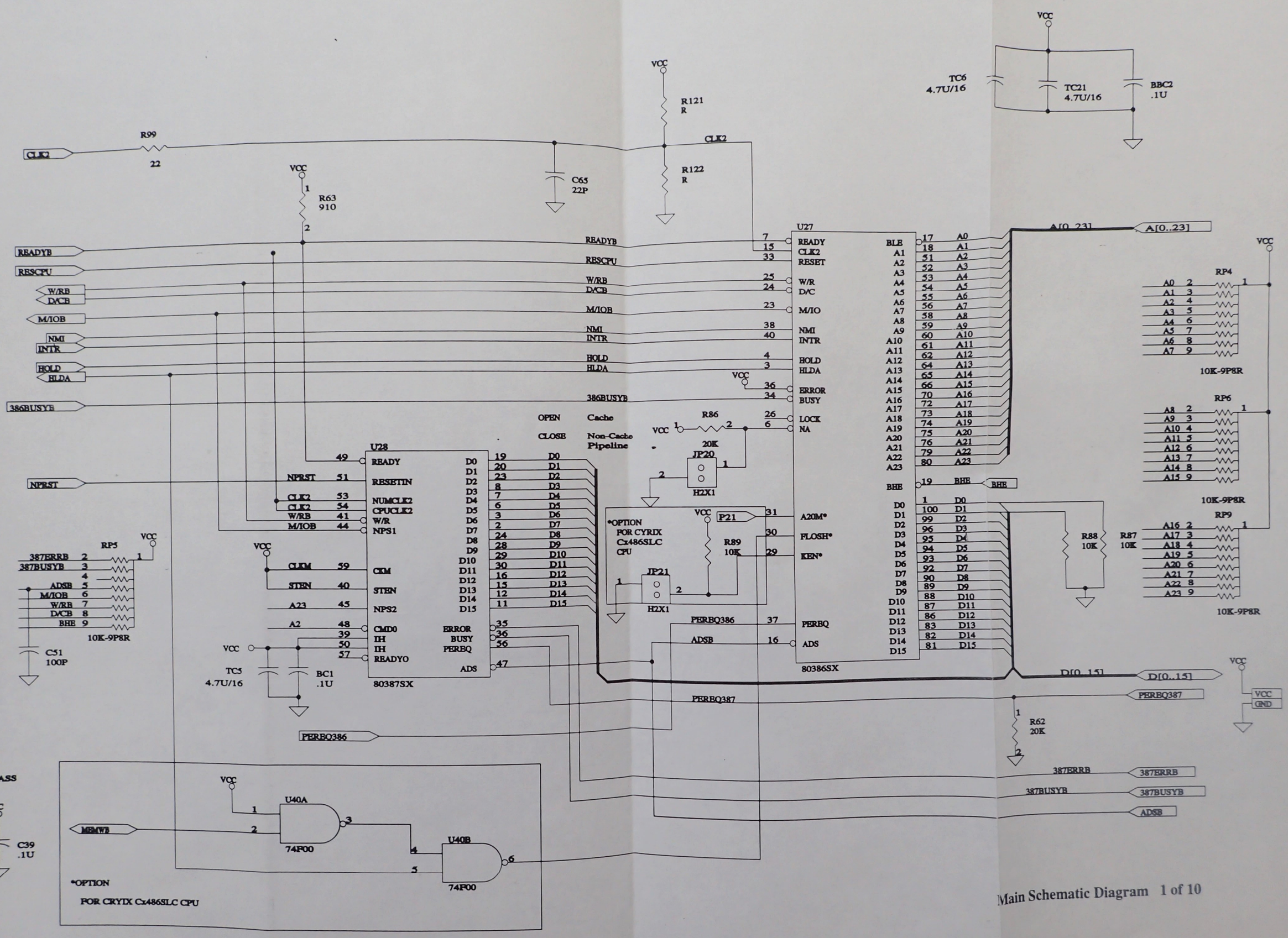

Main Schematic Diagram 1 of 10

RAS0
CASL0
CASH0
RAS1
R105 22 RAS0#
R104 22 CASL0#
R107 22 CASH0#
R106 22 RAS1#
CASL1
CASH1
R102 22 CASL1#
R103 22 CASH1#
LIOR#
LIOW#
MDWRB
MDRDB
MA[0..10]
OSC1
MDGATE
INTA/HLDA1
MBMWB
MBMRB
SMEMWB
SMEMRB
IOCHRDY
MCS16B
IOCS16B
SMEMWB
SMEMRB
NOWSB
IOCHRDY
U32
RC
ADSB
M/IOB
W/RB
D/CB
READYB
RESCPU
RESET
NPRST
RESB
RESET
LMW#
FS1
LMR#
CLK2IN
CLK2
W83C311
IOW#
IOR#
SYSCLK
BALE
XDDIR
D7
D6
D5
D4
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
D3
D2
D1
D0
MDPL
MDPH
PCK
SD15
SD14
SD13
SD12
SD11
SD10
SD9
SD8
D15
D14
D13
A[0..23]
TA[16..23]
BHE
P21
ROMOEB
SBHE
SA0
DOEB
C46
270P
REFRESH
HLDA
HOLD
TOEB
TWEB
ADL
DWE1B
DWE0B
REFRESHB
386BUSYB
PEREQ386
387BUSYB
PEREQ387
387ERRB
MDP[0..1]
SD[0..15]
D[0..15]
VCC
TC22
4.7U/16
TC23
4.7U/16
TC10
4.7U/16
BC2
.1U
ABALE
XDDIR
A7
A8
A9
A10
A11
A12
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
SA16
SA17
SA18
SA19
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
A23
U26
W83C312
IALE/AEN1
EALE/AEN2
INTA/HLDA1
BHLDA
RTCAS
RTCDS
RTCRW
8042CS
MEMR#
MEMW#
IOR#
IOW#
MASTER#
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
SYSCLK
IOCHCK
PCK
NMI
LOUT1
LHRQ1
IOCHRDY
REFRESH#
KBCLK
DRQ[0..3]
DRQ[5..7]
DACK[0..3]
DACK[5..7]
SA[0..19]
T/C
AEN
RTCAS
RTCDS
RTCRW
8042CS
MEMRB
MEMWB
IORB
IOWB
MASTERB
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
SYSCLK
IOCHCK
PU22A
NMI
LOUT1
LHRQ1
IOCHRDY
REFRESH
KBCLK
VDD
VCC
VSS
RESET
SPK
IRQ[3..7]
IRQ1
IRQ8B
IRQ[9..12]
IRQ[14..15]
INTR
LA[17..23]
JP22
PU22
PU22A
H3X1
R90
4.7K
OSC1
C44
100P

Main Schematic Diagram 2 of 10

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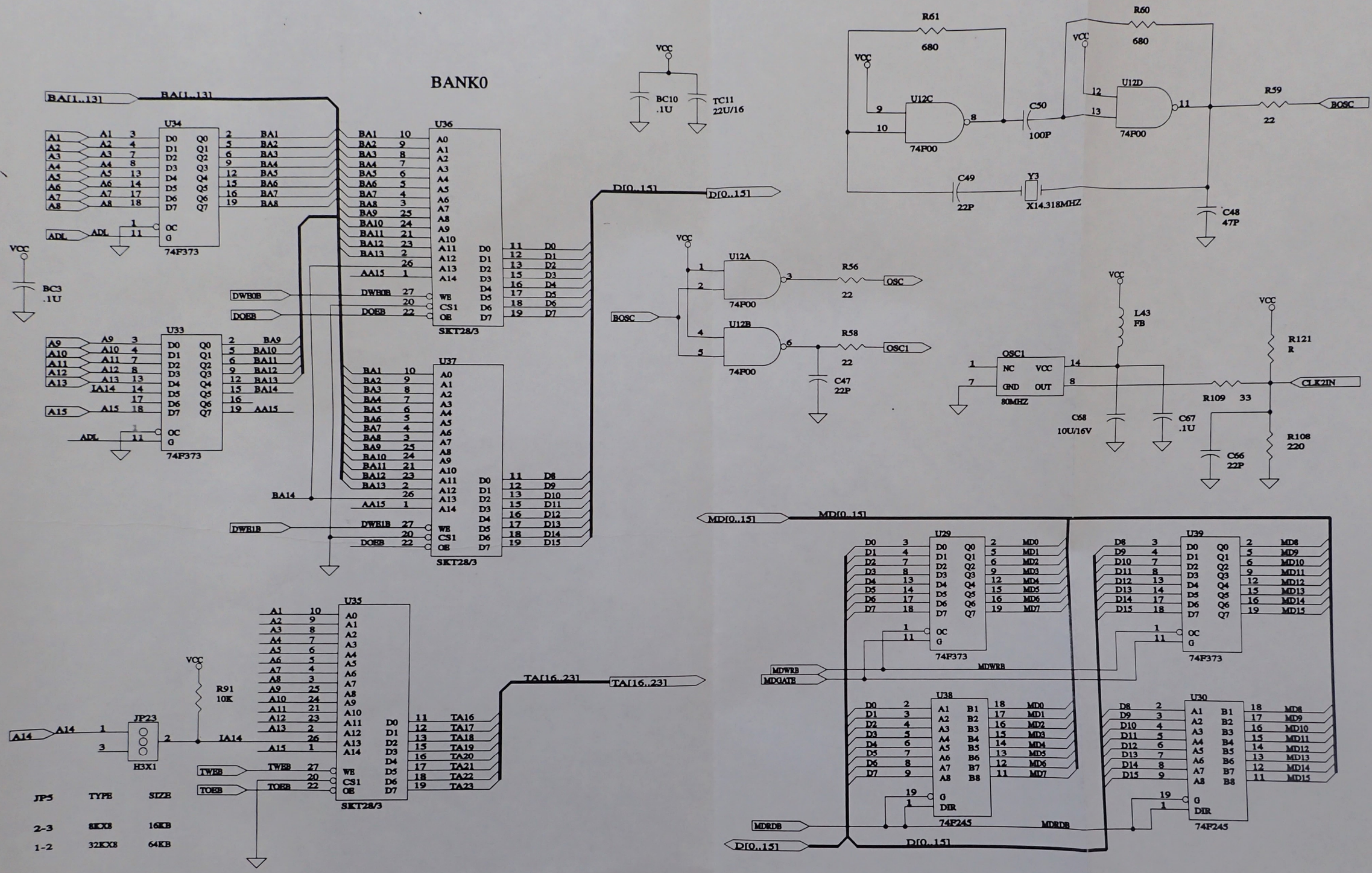
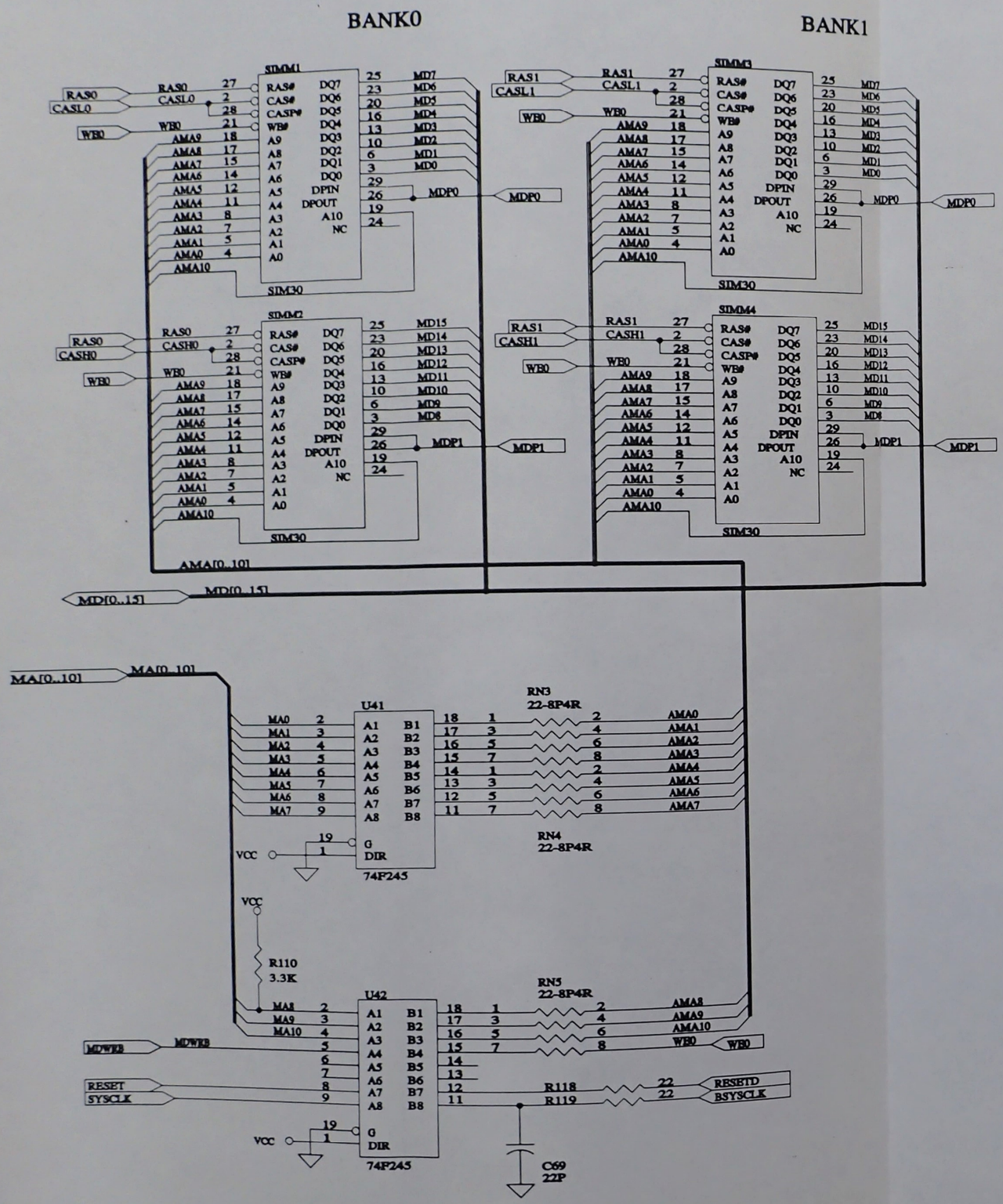
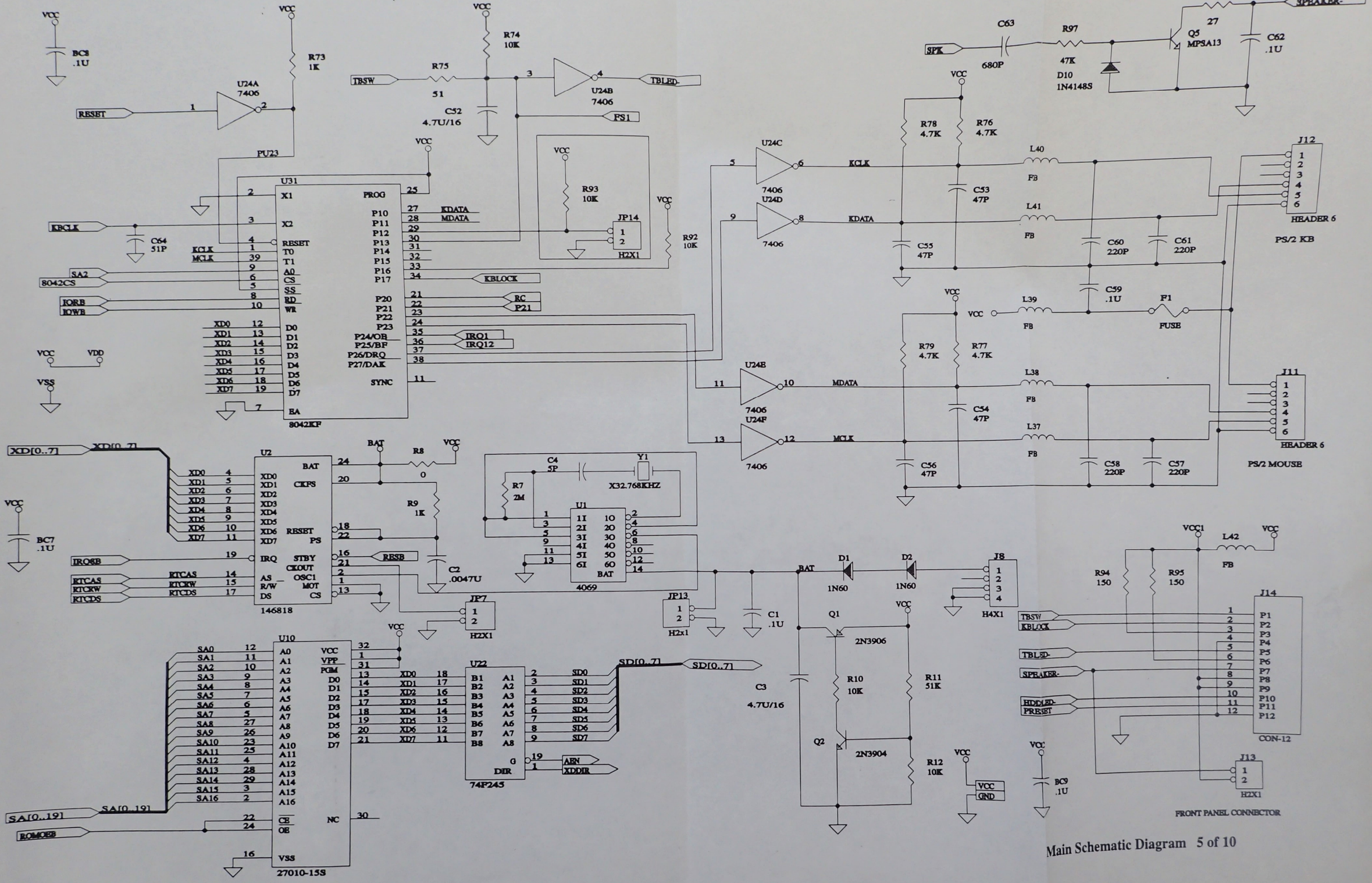


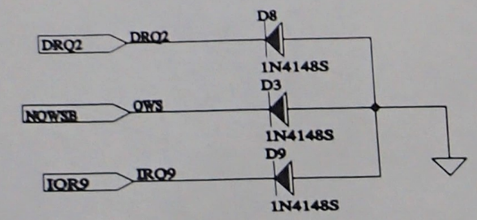
Main Schematic Diagram 3 of 10

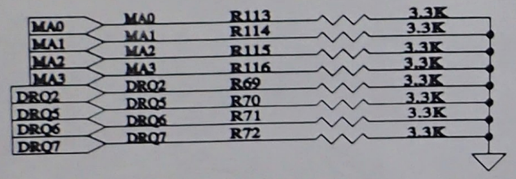


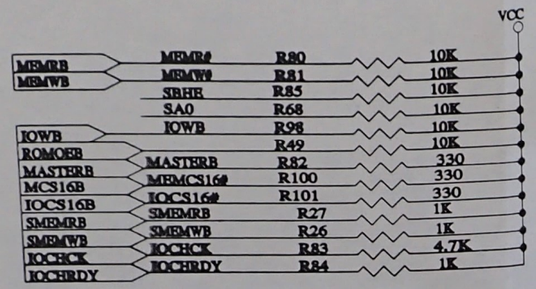
Main Schematic Diagram 4 of 10

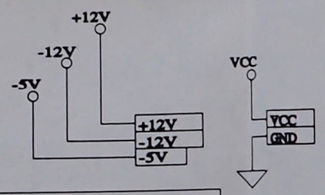


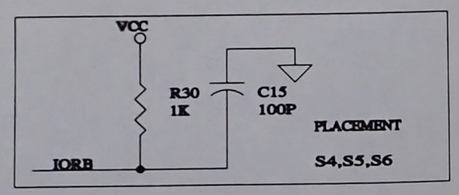
Main Schematic Diagram 5 of 10

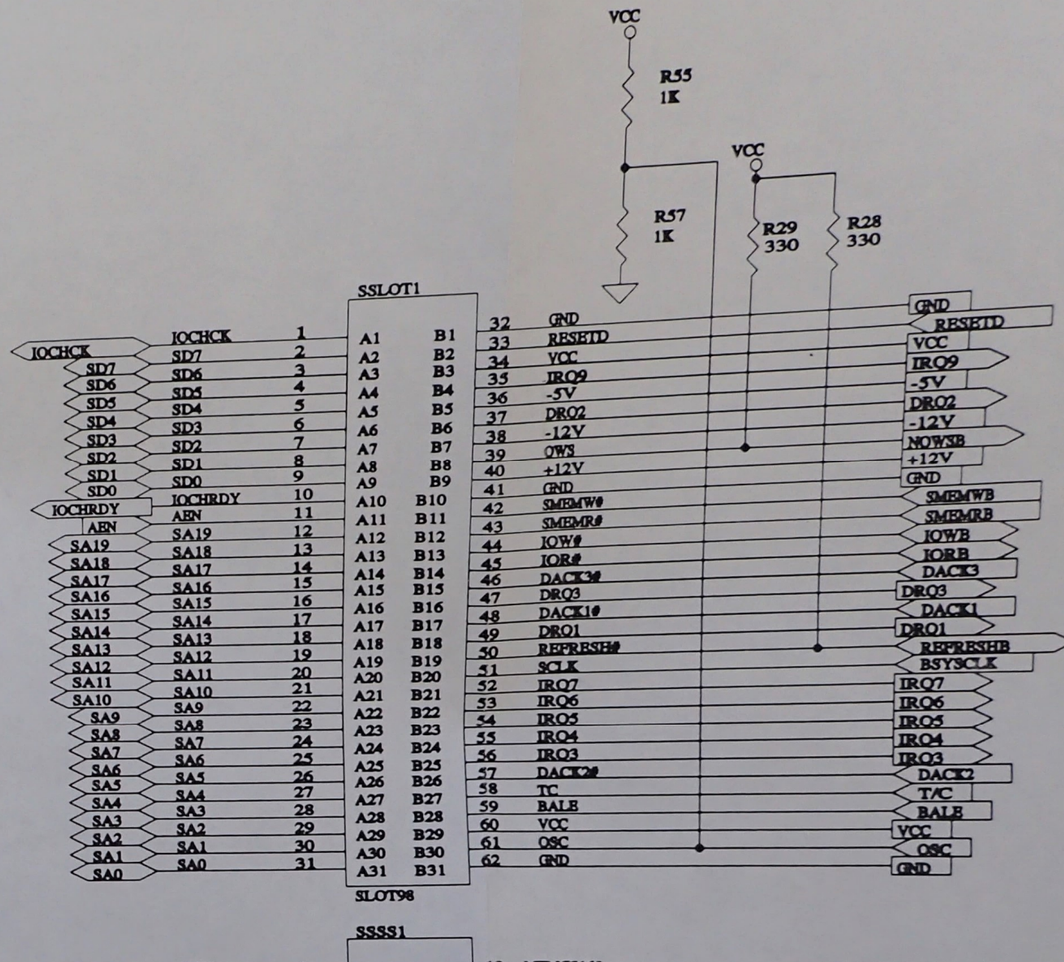


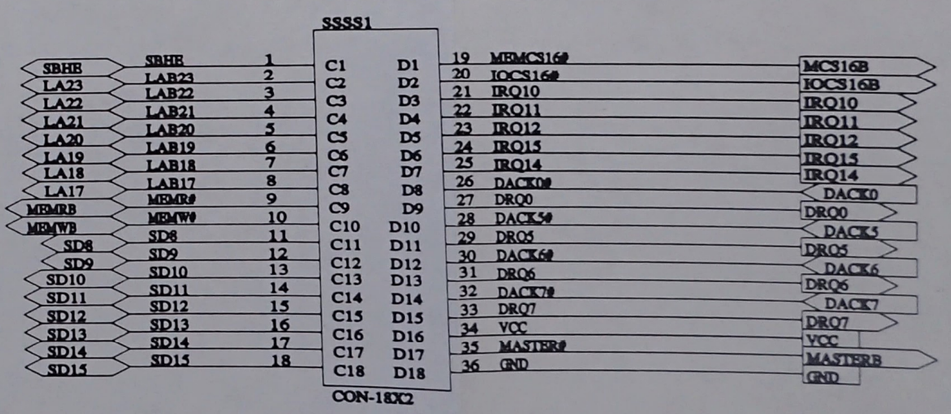


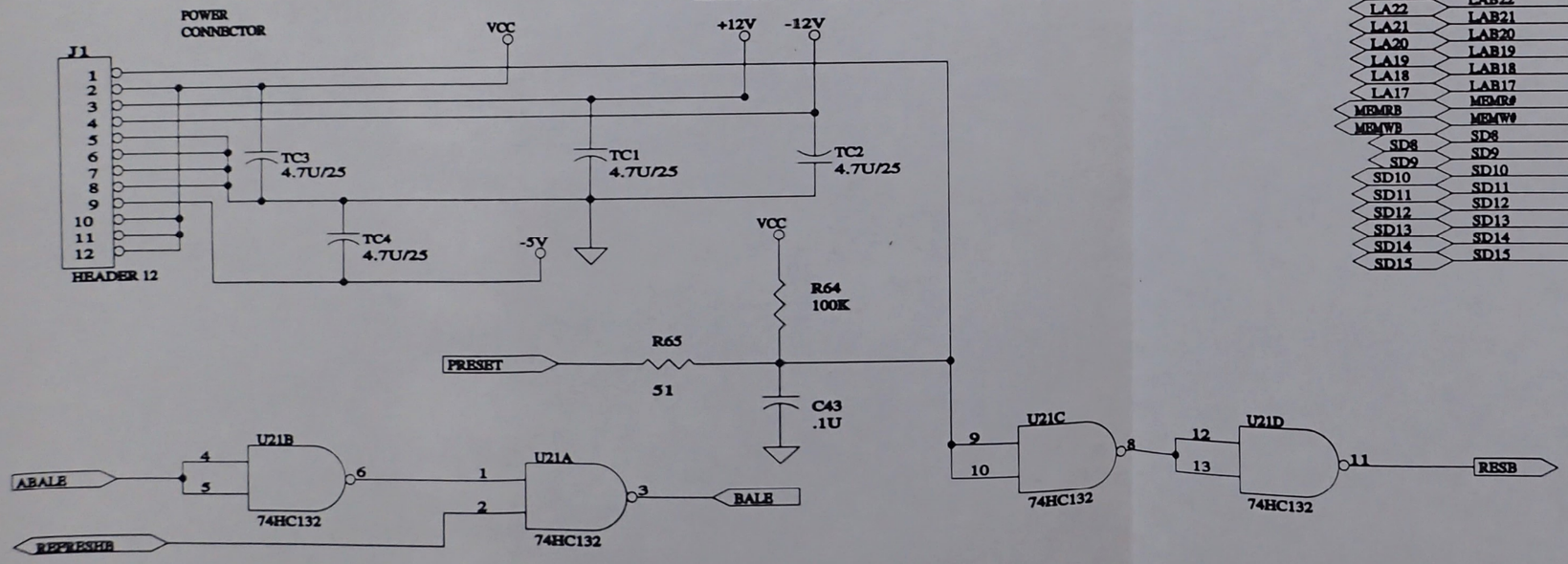




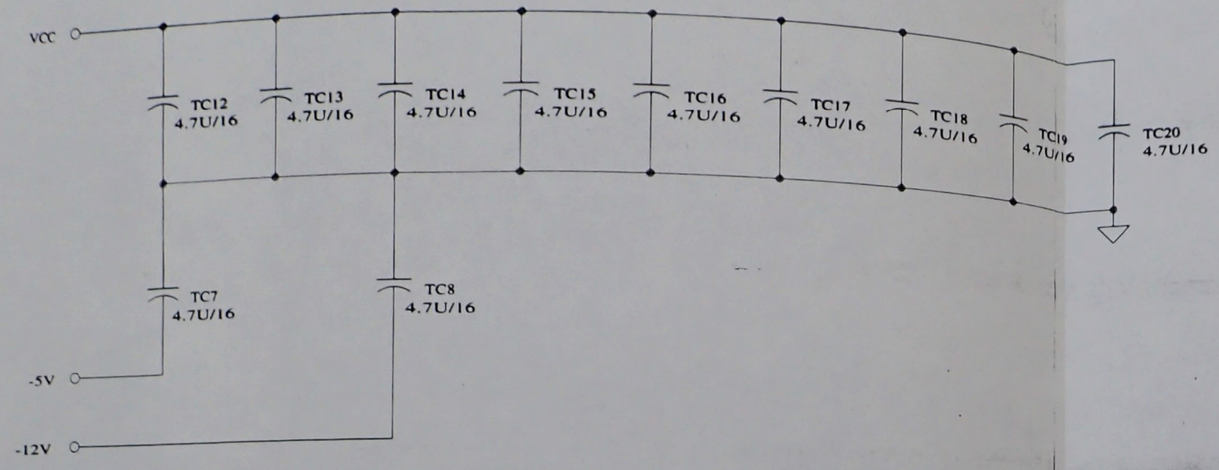


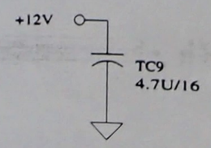


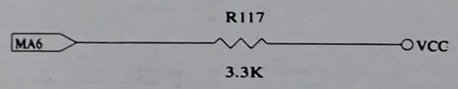


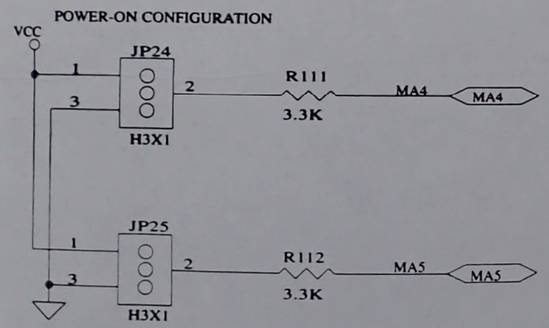


Main Schematic Diagram 6 of 10

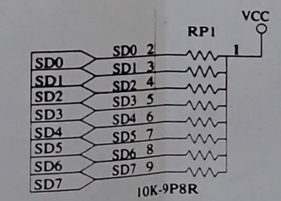


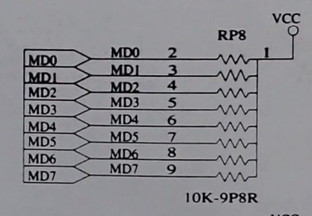


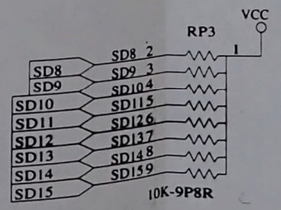


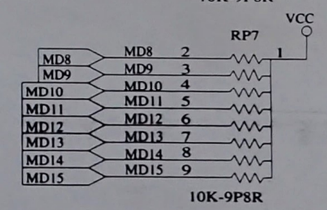


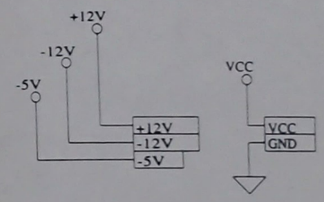
JP6	JP4	SYSCLK SELECTION
1-2	1-2	CLK2IN / 4
1-2	2-3	CLK2IN / 6
2-3	1-2	CLK2IN / 8
2-3	2-3	CLK2IN / 5



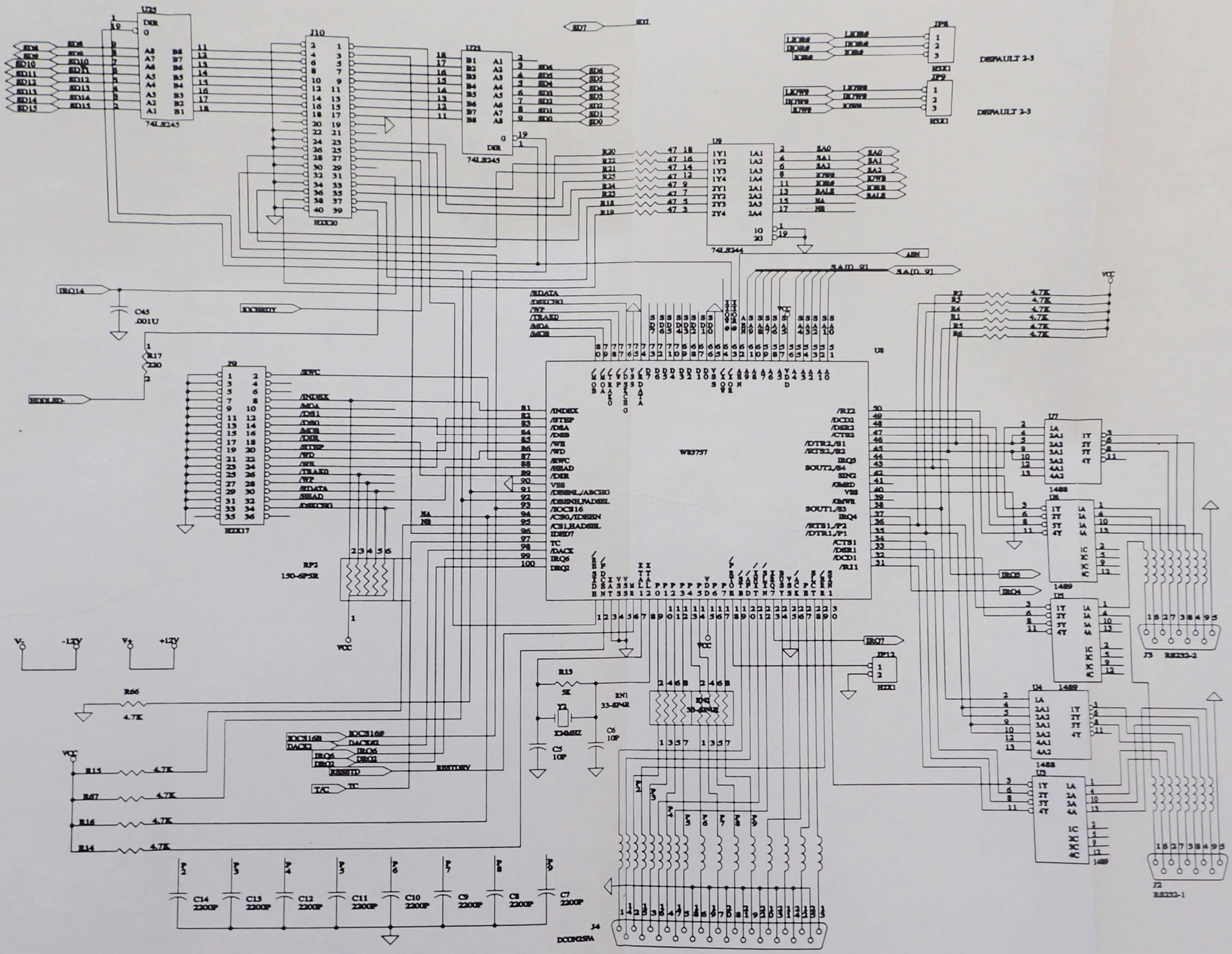




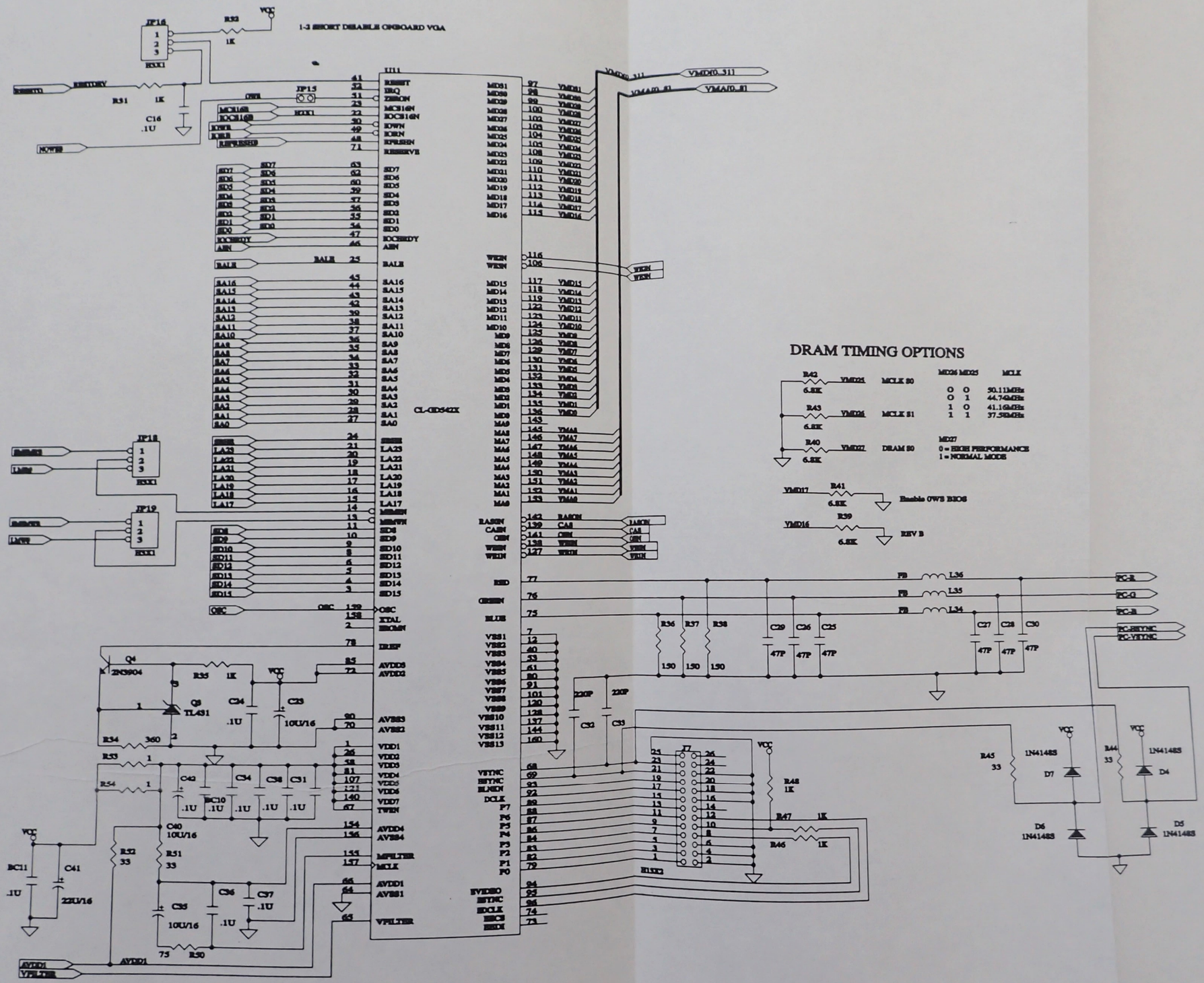




Main Schematic Diagram 7 of 10



Main Schematic Diagram 8 of 10



DRAM TIMING OPTIONS

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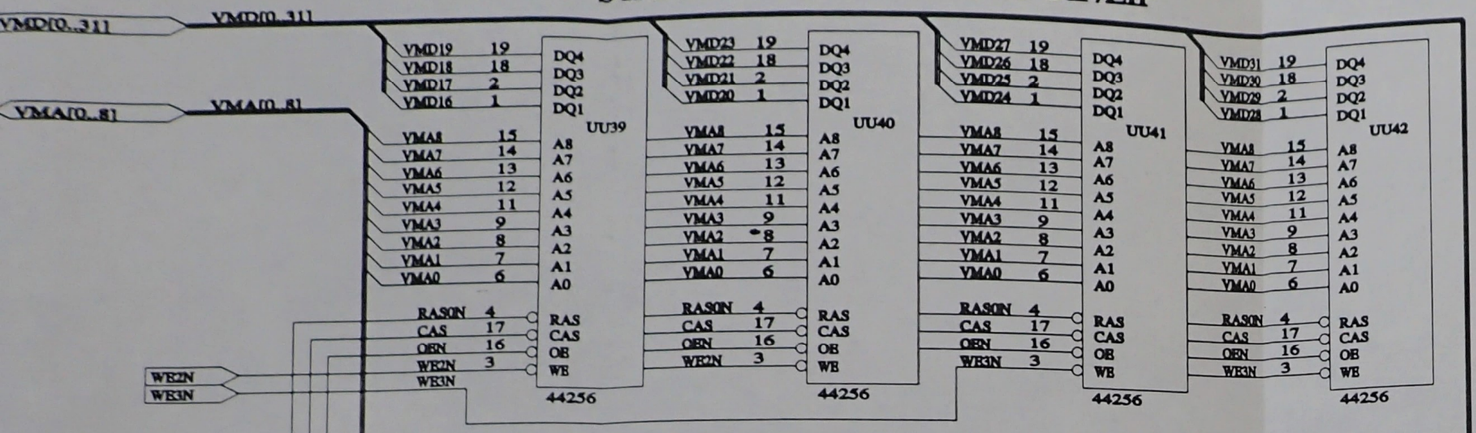
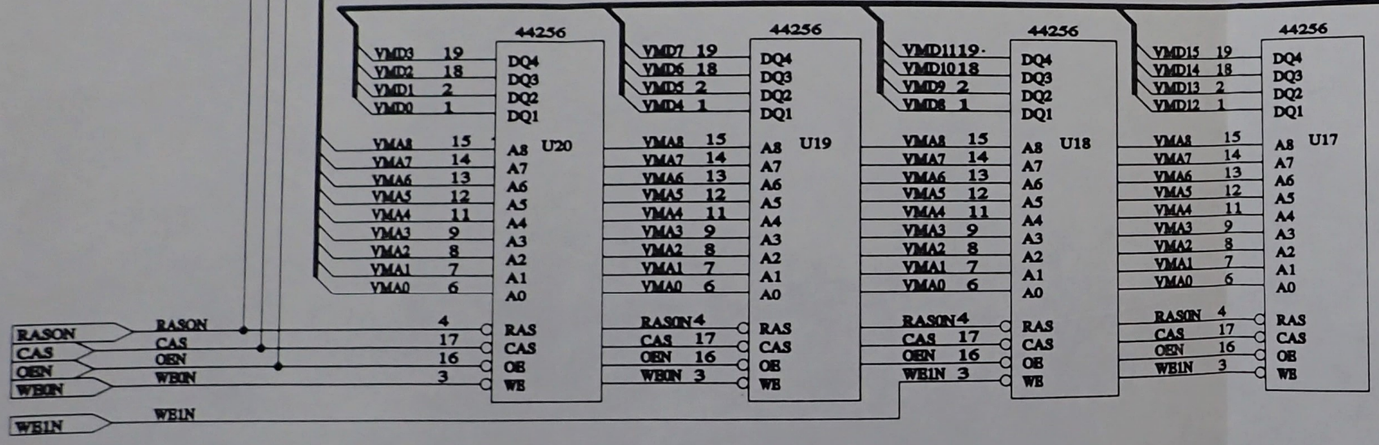
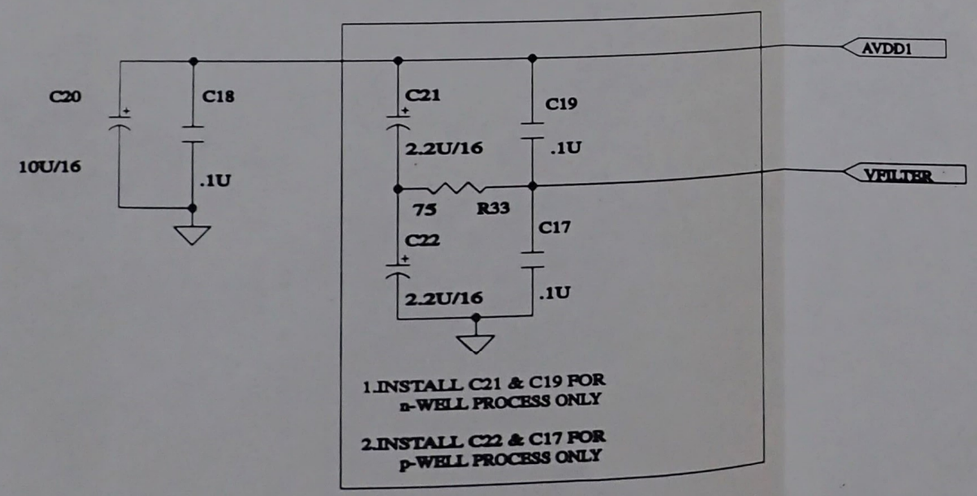
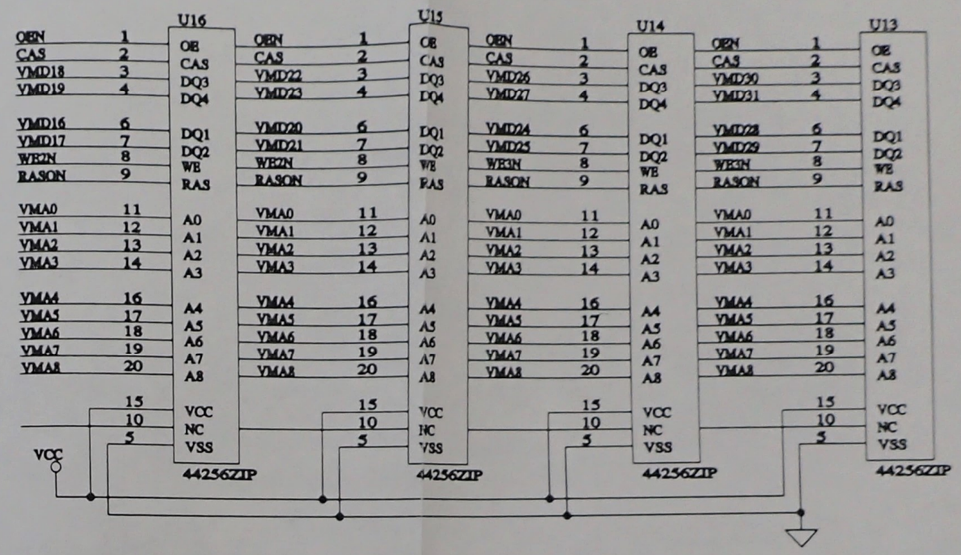
STANDARD 512K MEMORY DIP/ZIP

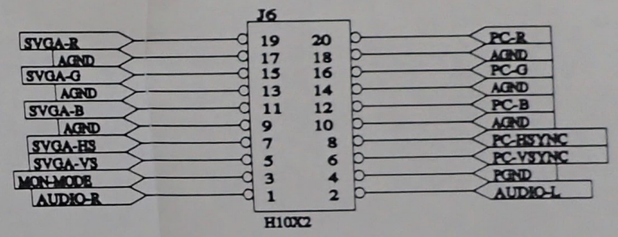


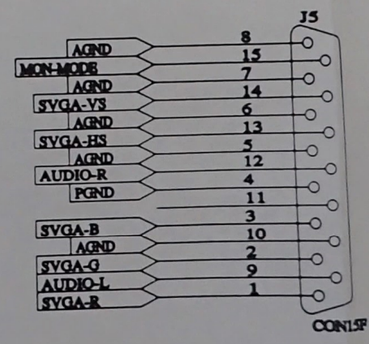
1 MEG DRAM OPTION

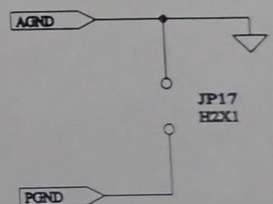






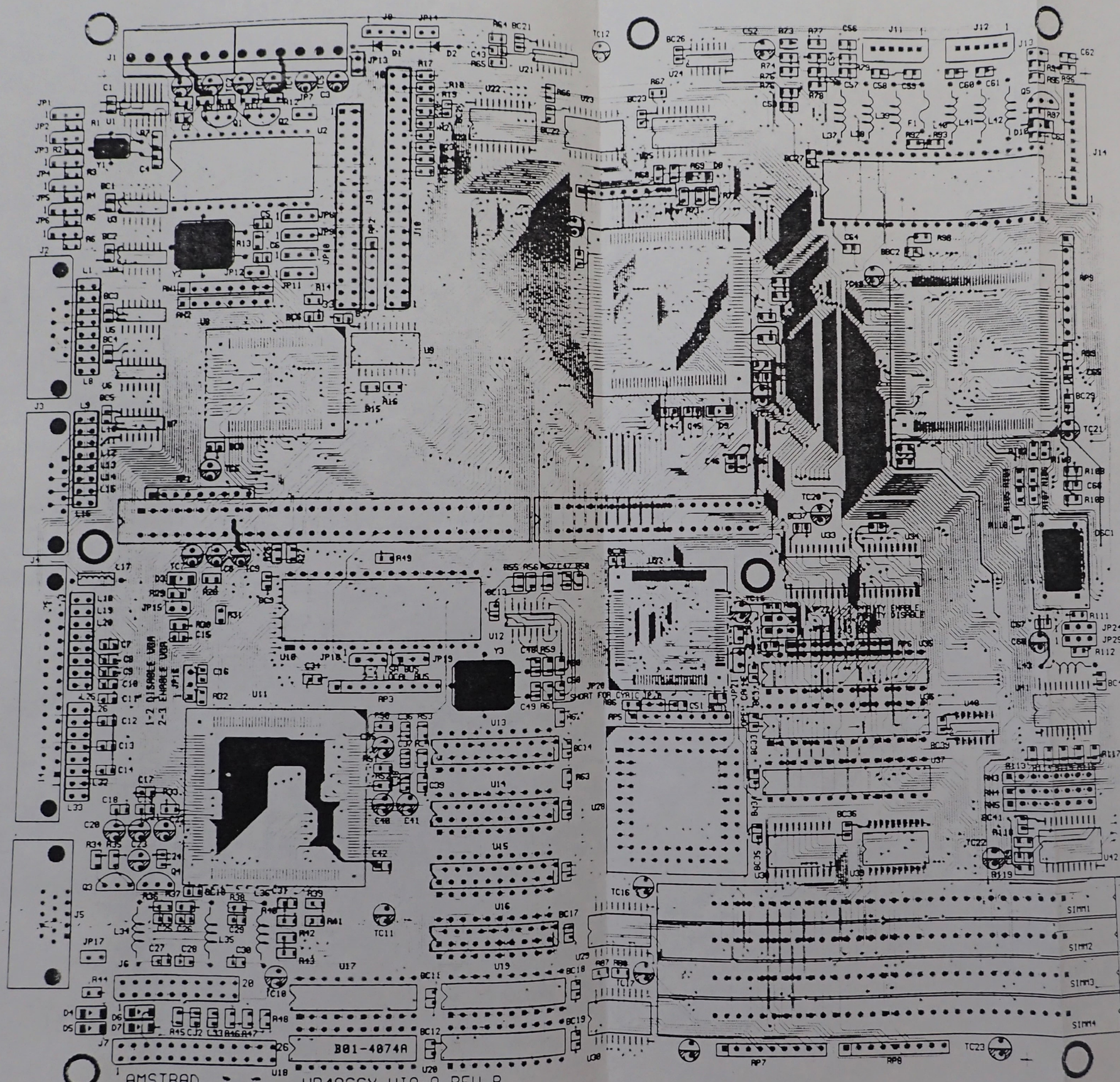






Main Schematic Diagram 10 of 10

Main PCB Top View



Main PCB Bottom View

