PAT54PV

Version 1.1A

User's Manual

PAT54PV
P54C/CT Motherboard
User's Manual

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User's Manual
PAT54PV Motherboard
1st Edition
TMC

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About This Manual

This manual is organized as follows:

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Chapter 2 Specifications - Lists and explains the specifications of the PAT54PV motherboard.

Chapter 3 Hardware Description - Describes each of the major features of the PAT54PV motherboard. Also describes the main memory configurations of the board.

Chapter 4 Configuring the PAT54PV - Describes the necessary procedures and jumper settings to configure the PAT54PV motherboard.

Chapter 5 Installation - Describes the interfaces and connectors the PAT54PV provides for creating a working system.

Chapter 1 Introduction

The PAT54PV is a high performance, P54C/CT microprocessor powered, ISA/VESA Local(VL) Bus motherboard. The P54C/CT processor is designed for high-end desktop and server computers .

The PAT54PV contains a total of eight ISA expansion slots. Three of these slots have VESA Local(VL)-Bus connectors, allowing users to install VL-Bus peripheral cards such as a high resolution graphics card and a high performance storage controller. Two VL-Bus slots of the PAT54PV support bus mastering further enhancing system .

The P54C/CT processor includes separate code and data caches to provide high performance. Each cache is 8KB in size and the data cache can be configured to be write-through or write-back on a line by line basis. In addition to 16KB of on-chip cache memory, the PAT54PV can be configured with up to 512KB of write-back secondary cache memory, further improving system performance.

The on board SIMM sockets are designed to accommodate 256K x 36, 1M x 36, or 4M x 36 modules as well as dual density modules including 512K x 36, 2M x 36 or 8M x 36, providing the user with up to 128MB of system memory.

The performance, speed and expandability of the PAT54PV make it the perfect choice for building a LAN server, a high-end workstation or a multi-user system.

Chapter 2 Specifications

Main Processor

Intel P54C/CT 75MHz, 90MHz or 100MHz processor

Cache Memory

256KB or 512KB of write-back secondary cache memory

Main Memory

Up to *128MB* of on board main memory
Two memory banks
Four 36-bit SIMM sockets for ***256K x 36, 1M x 36 or 4M x 36*** modules
The SIMM sockets also support dual density modules: ***512K x 36, 2M x 36 or 8M x 36***

Chipset

OPTi 82C596/82C597

BIOS

Licensed BIOS

Clock/Calendar

Battery Backed Real Time Clock(146818 compatible) and 128 bytes of CMOS RAM
On board rechargeable battery

DMA Channels

Seven DMA channels(8237 compatible)

Interrupts

Sixteen levels of hardware interrupts (dual 8259 compatible)

System Timer

Three channels of programmable system timer (8254 compatible)

Expansion

Three VL-Bus slots: two master slots
Eight ISA slots

Connectors

Connectors for: power supply, keyboard, reset switch, Power LED, keylock, speaker, turbo switch, turbo LED, external battery and hard disk access LED

Form Factor

Baby AT size

Power Requirement(typical)

+5V @ 3.5 AMPs

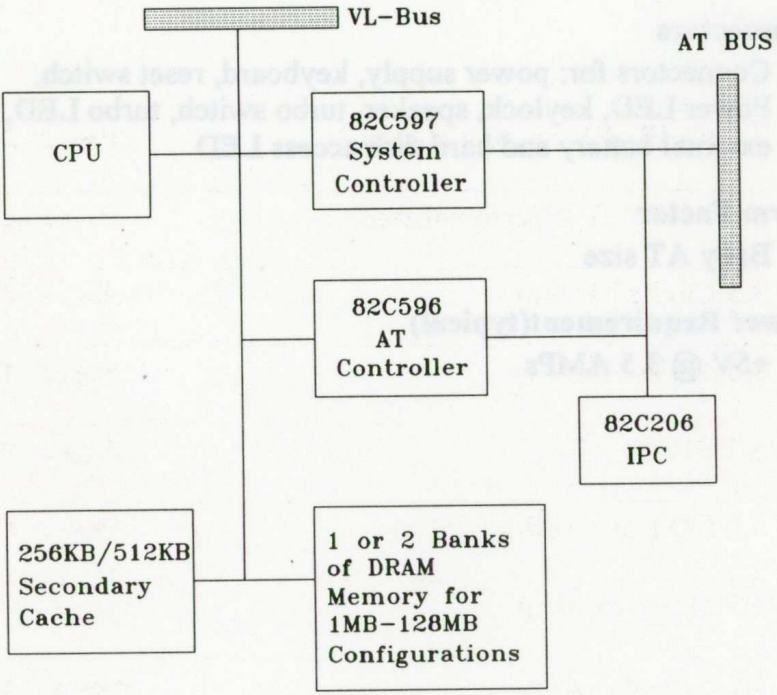


Figure 1: Function block of the PAT54PV

Chapter 3 Hardware Description

This chapter briefly describes each of the major features of the PAT54PV system board. The function block of the board is shown in *Figure 1.* The layout of the board is shown in *Figure 2* to show the locations of key components. The topics covered in this chapter are as follows:

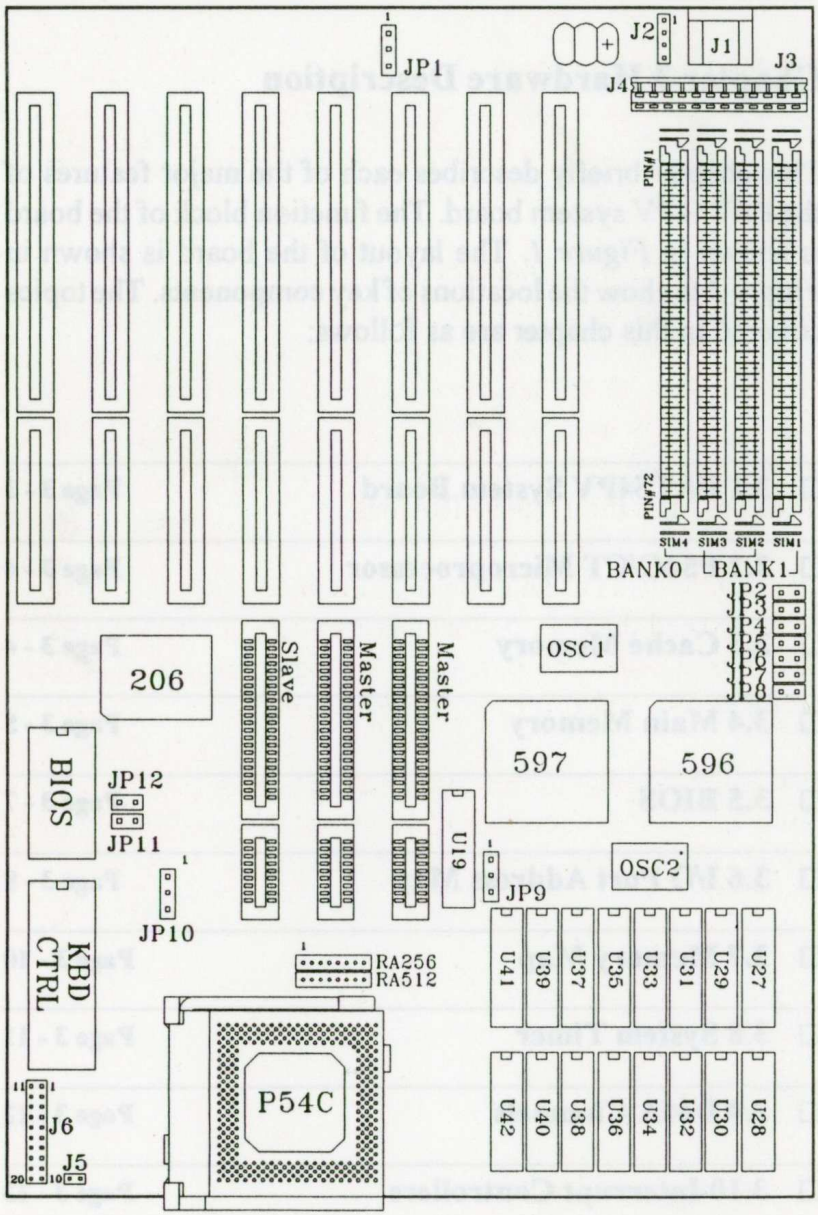


Figure 2: Layout and connector locations of the PAT54PV

3.1 PAT54PV System Board

The PAT54PV is designed by implementing a P54C/CT microprocessor and a highly integrated chipset.

The chipset is comprised of two chips, the 82C597 SYSC controller and 82C596 ATC controller. The SYSC (System Controller) provides the control functions for the host CPU interface, the 32-bit local bus interface, the 64-bit secondary cache memory and 64-bit DRAM bus. The SYSC also controls the data flow between the CPU bus, the DRAM bus, the local bus, and the 16/8-by ISA bus.

The 82C596 ATC (AT Controller) integrates the AT bus interface and the data buffers for transfers between the CPU data bus, Local data bus and the DRAM data bus. It also provides ISA to local bus command translation.

The 82C206 Integrated Peripherals Controller (IPC) incorporates the DMA Controller, Interrupt Controller, System Timer, and Clock/Calendar functions.

3.2 P54C/CT Microprocessor

The P54C/CT processor is designed for high performance desktops and servers and is binary compatible with both the 486DX and 386DX.

The application instruction set of the P54C/CT processor includes the complete 486 CPU instruction set with extensions to accommodate some of the additional functionality of the P54C/CT processor. All application software written for the 386 and 486 microprocessors will run on the P54C/CT processor without modification.

The P54C/CT processor implements several enhancements to increase performance. The P54C/CT processor has increased the data bus to 64-bits and contains separate code and data cache of 8KB each with a cache line size of 32-bytes. The P54C/CT processor also contains a pipelined floating point unit that provides a significant floating point performance advantage over previous generations of the P54C/CT processor

3.3 Cache Memory

The P54C/CT processor includes separate code and data caches integrated on chip to provide high performance. Each cache is 8KB in size, with 32-byte line size and is 2-way set associative. The data cache is configurable to be write-back or write-through on a line by line basis.

For the secondary cache, the PAT54PV supports write-back cache memory sizes of 256KB or 512KB.

3.4 Main Memory

The PAT54PV has two(2) memory banks for up to ***128MB*** of main memory. Each memory bank of the PAT54PV consists of **two***(2)* 36-bit SIMM(Single In-Line Memory Module) sockets that can accept ***256K x 36, 1M x 36 or 4M x 36*** modules.

The SIMM sockets can also accommodate dual density modules such as ***512K x 36, 2M x 36 or 8M x 36*** SIMMs.

Refer to the following figure for the locations of the PAT54PV's memory banks.

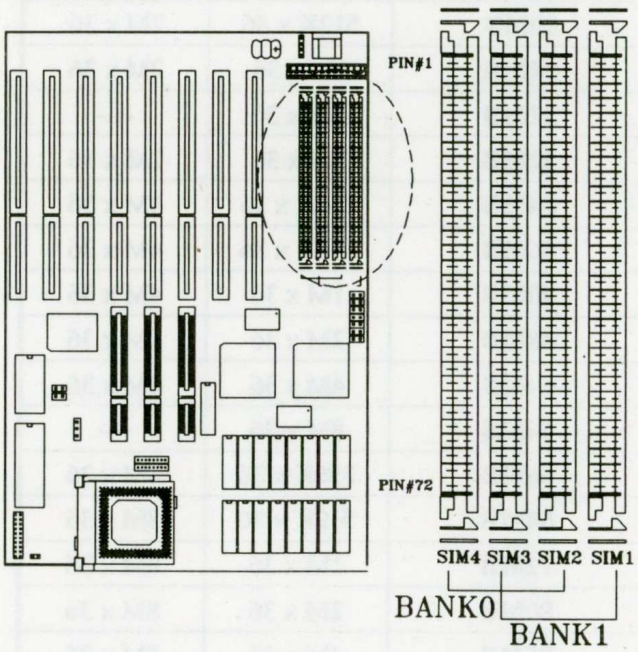


Figure 3: Memory bank locations of the PAT54PV

Table 1: Memory configurations of the PAT54PV

Total Memory	Bank 0	Bank 1
2MB	256K x 36	----
4MB	512K x 36	----
6MB	256K x 36	512K x 36
8MB	1M x 36	----
8MB	512K x 36	512K x 36
10MB	256K x 36	1M x 36
12MB	512K x 36	1M x 36
16MB	1M x 36	1M x 36
16MB	2M x 36	----
18MB	256K x 36	2M x 36
20MB	512K x 36	2M x 36
24MB	1M x 36	2M x 36
32MB	4M x 36	----
32MB	2M x 36	2M x 36
34MB	256K x 36	4M x 36
36MB	512K x 36	4M x 36
40MB	1M x 36	4M x 36
48MB	2M x 36	4M x 36
64MB	4M x 36	4M x 36
64MB	8M x 36	----
66MB	256K x 36	8M x 36
68MB	512K x 36	8M x 36
72MB	1M x 36	8M x 36
80MB	2M x 36	8M x 36
96MB	4M x 36	8M x 36
128MB	8M x 36	8M x 36

3.5 BIOS

The PAT54PV contains a 128Kx8 Flash ROM that contains the system BIOS. The BIOS resides at the upper 64KB of address space in the first megabyte.

In protected mode, the BIOS is also mapped to the upper 64KB of the 128MB space and can be accessed at either location.

The BIOS on the PAT54PV is compatible with the BIOS in the IBM AT with the exception that it does not contain the BASIC interpreter. The BASIC and BASICA on IBM PC-DOS will not run on the PAT54PV.

To run BASIC in systems based on the PAT54PV, the user should use the GW-BASIC interpreter provided with the Microsoft DOS diskette.

3.6 I/O Port Address Map

The CPU of the PAT54PV communicates via I/O ports. There are a total of 1K port address space defined. The following tables list the I/O port addresses used in the PAT54PV and those assigned to other devices that can be used by the add-on cards.

Table 2: I/O port addresses of the devices on the PAT54PV

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor

Table 3: I/O port addresses of devices on the I/O slots

Address	Description
1F0h - 1F7h	Primary IDE Interface
200h - 207h	Game Port
278h - 27Fh	Parallel Port #2(LPT2)
2F8h - 2FFh	Serial Port #2(COM2)
300h - 31Fh	Prototype Card
360h - 36Fh	Reserved
378h - 3FFh	Parallel Port #1(LPT1)
380h - 38Fh	SDLC #2
3A0h - 3AFh	SDLC #1
3B0h - 3BFh	MDA Video Card(including LPT0)
3C0h - 3CFh	Reserved
3D0h - 3DFh	CGA Video Card
3F0h - 3F7h	Floppy Disk Controller
3F8h - 3FFh	Serial Port #1(COM1)

3.7 Memory Map

The PAT54PV has a maximum memory capacity of 128MB. The first megabyte is divided into four blocks with each block dedicated to a fixed function. The following table illustrates the memory map for the PAT54PV.

Table 4: Memory map of the PAT54PV

Memory	Address	Description
0KB	000000h 09FFFFh	Conventional RAM
640KB	0A0000h 0BFFFFh	128 KB of Video RAM
768KB	0C0000h 0EFFFFh	192KB of I/O Expansion ROM
960KB	0F0000h 0FFFFFh	64KB of System BIOS ROM
1MB	100000h 7FEFFFFh	127MB of User RAM
128MB	7FF0000h 7FFFFFFh	Duplicated 64KB of System BIOS ROM at 0F0000h

3.8 System Timer

The PAT54PV has three channels of timer/counter in the 82C206 chip, which is Intel 8254 compatible. The function of each channel is listed as follows:

Table 5: System timer of the PAT54PV

Channel	Function
0	**System Timer** - This timer generates the time base for the system timer. Its output is tied to IRQ0.
1	**Memory Refresh Request** - This timer is used to generate memory refresh requests. It triggers the memory refresh cycle.
2	**Tone Generator for Speaker** - This timer provides the speaker tone. Various sounds can be generated by programming the timer.

3.9 DMA Channels

The PAT54PV contains the equivalent of two 8237A DMA controllers in the 82C206.

The 82C206 provides the user with two DMA controllers, four channels of DMA*(DMA #1)* for 8-bit transfers, and three channels of DMA*(DMA #2)* for 16 bit transfers.(The first 16-bit DMA channel is used for cascading.)

Channel		Function
Controller #1	**Controller #2**	
0		DRQ0, Spare
1		DRQ1, Spare
2		DRQ2, Floppy Disk Controller
3		DRQ3, Spare
	4	DRQ4, Cascade for DMA
	5	DRQ5, Spare
	6	DRQ6, Spare
	7	DRQ7, Spare

3.10 Interrupt Controllers

The PAT54PV contains two Intel 8259A compatible interrupt controllers in the 82C206. Sixteen channels are partitioned into the cascaded controllers (INTC1, INTC2) with 8 inputs each. Of these 16 channels, three are connected internally to various devices, allowing 13 user definable channels of interrupt. Any or all of these interrupts can be masked.

Level	Function
NMI	RAM Parity Check
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ8	Real Time Clock
IRQ9	Software Redirected to Int 0Ah
IRQ10	Reserved
IRQ11	Reserved
IRQ12	Reserved
IRQ13	80287
IRQ14	Fixed Disk Controller
IRQ15	Reserved
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Parallel Port #2
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1

3.11 Real Time Clock and CMOS RAM

The PAT54PV contains an MC146818 compatible Real Time Clock (RTC) and 128 bytes of CMOS RAM in the 82C206.

The CMOS RAM stores the system's configuration information entered via the Setup program. The RTC and the CMOS RAM are kept active by a battery when the system power is turned off.

Note

The Real Time Clock and the CMOS RAM are kept active by an on board rechargeable battery. The PAT54PV also provides an interface for an external battery. Refer to **Section 5.2, "External Battery connector", for details.**

Chapter 4 Configuring the PAT54PV

The following sections describe the necessary procedures and proper jumper settings to configure the PAT54PV system board. For the locations of the jumpers and Resistor Arrays, refer to *Figure 2* on *page 3 - 2*.

The following configuration options can be selected:

4.1 AT Bus Clock Selection Jumpers: JP2 & JP3

The PAT54PV generates the AT Bus clock ***(ATCLK)*** from an internal division of the ***Local Bus(VL-Bus) Clock (VLCLK).***

Refer to the following table for the necessary settings.

Table 7: VLCLK to ATCLK relationship

JP2	JP3	ATCLK Frequency	VLCLK Frequency
		10MHz	50MHz
		8MHz	40MHz
		8MHz	33MHz

Note

VLCLK can be derived from a clock synthesizer in U53 Refer to Section 4.7, "VL-Bus Frequency Selection" for details.

4.2 VL-Bus Signal Sample Selection Jumper: JP4

A VL-Bus device, to indicate that the current cycle is a VL-Bus cycle, generates a signal called ***LDEV#***. This signal, depending on how JP4 is set, can be sampled by the P54C/CT CPU at two different time intervals.

Refer to the following table for the recommended settings.

Table 8: Local bus signal sample selection

JP4	Condition
	Recommended for 33MHz VLCLK
	Recommended for 40/50MHz VLCLK

4.3-1 VL-Bus Wait State Selection Jumper: JP5

This *2-pin* header, **JP5**, determines whether or not an additional local bus clock cycle is necessary to perform a write to a VL-Bus peripheral device. Read cycles are unaffected by this setting.

Refer to the following table for the necessary settings.

Table 9-1: VL-Bus write wait state selection settings

JP5	Condition
	0 wait state writes *(Recommended for 33MHz VLCLK)*
	1 wait state writes *(Recommended for 40MHz/50MHz VLCLK)*

4.3-2 VL-Bus Speed Indication Jumper: JP6

This *2-pin* header, **JP6**, is used to indicate the VL-Bus clock speed (VLCLK) of the PAT54PV

Refer to the following table for the necessary setting

Table 9-2: VL-Bus speed indication settings

JP6	Condition
	33MHz VLCLK
	40/50MHz VLCLK

4.4 Video Adapter Selection Jumper: JP7

This jumper setting is checked by the system BIOS during system boot-up to decide what type of video card is primary card in the system board. This jumper setting is also checked against the configuration information stored in the CMOS RAM by the Setup program.

If there is only one video card installed in the PAT54PV system, set this jumper to reflect its type.

If more than one video card is installed in the PAT54PV system, set this jumper to indicate which card is the primary one.

Table 10: Video adapter selection jumper settings

JP7	Function
	Monochrome
	Color

Note

If this jumper is set to indicate the type of primary display present in the PAT54PV, an error message will appear during boot-up. Also, note that for a videoless application, such as a dedicated file server, it is not necessary to set JP7. You may specify videoless application during the system setup program.

4.5 Back-to-Back I/O Delay Selection: JP8

This 2-pin header must be set according to the following table.

Table 11: Back-to-back I/O delay selection setting

JP8	Function
	Enable back-to-back I/O delay *(default)*
	Disable back-to-back I/O delay

4.6 Local Device Indication Jumper: JP9

Set this 3-pin header, JP9, according to the following table.

Table 12: Local device indication settings

JP9	Function
	33MHz or 40MHz VLCLK
	50MHz VLCLK

4.7 VL-Bus Frequency Selection : JP10 - JP12

The VESA Local(VL) Bus Clock***(VLCLK)*** of the PAT54PV can be derived from ***a clock synthesizer installed in U53.***

JP10 - JP12 are used to determine the VLCLK frequency of the PAT54PV.

Table 13: VLCLK frequency

VLCLK Frequency	JP10	JP11	JP12
33MHz			
40MHz			
50MHz			

4.8 Secondary Cache Memory Size Selection Resistor Arrays: RA256, RA512

These ***TWO(2)*** 8-pin **RA***(Resistor Array)* sockets, **RA256, RA512**, allow the user to indicate the amount of secondary cache memory present on the PAT54PV.

The secondary cache RAM improves the system performance by providing the P54C/CT CPU with data in the event of on-chip cache misses. The secondary cache RAM of the PAT54PV implements the write-back design, further improving system performance.

The PAT54PV supports TWO cache memory sizes: ***256KB or 512KB***. Refer to the following pages for the necessary procedures on installing or changing the cache memory size of the PAT54PV.

Note

Depending on the user's specified cache memory size, these RAs(RA256, RA512) will be preconfigured by the manufacturer. Therefore, unless the user changes the cache size of the PAT54PV, reconfiguration of these RNs WILL NOT be necessary.

To configure the PAT54PV with **256KB** of secondary cache memory, install ***eight(8)*** *32K x 8* SRAM in sockets **U27, U29, U31, U33, U35, U37, U39 and U41** for the cache data RAM and ***one(1)*** *32K x 8* SRAM in **U19** for the tag RAM.

Also, install the RAs in **RA256**. Refer to the following figure for the locations of the SRAM and the Resistor Arrays.

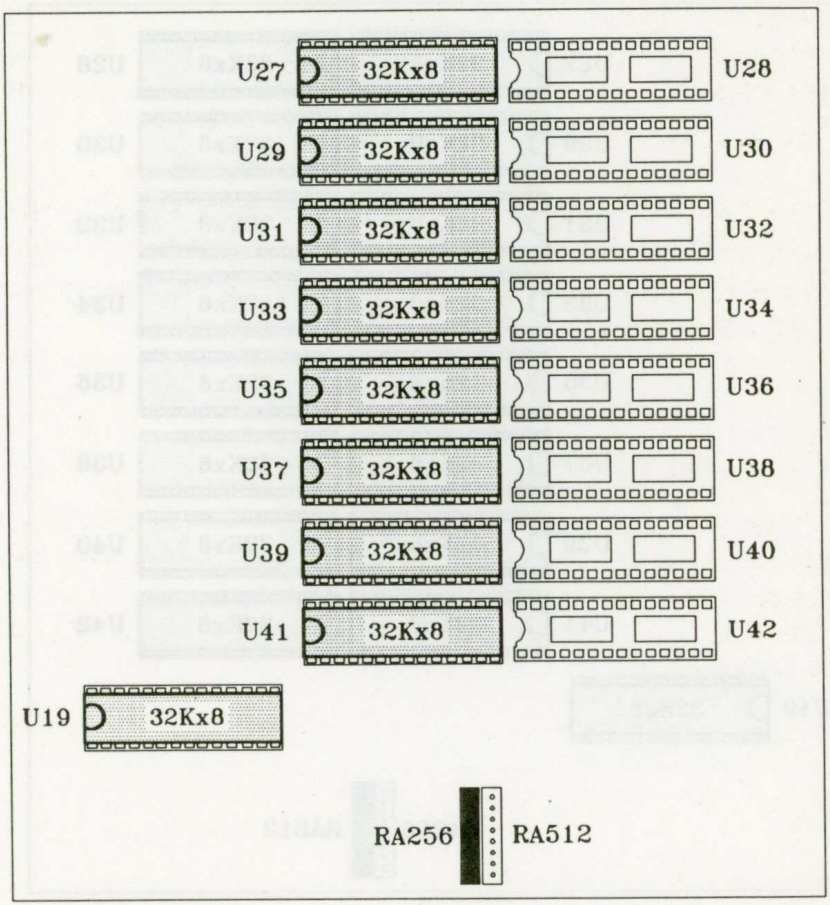


Figure 4: PAT54PV with 256KB of cache memory

512KB of secondary cache memory is achieved by installing ***sixteen(16) 32K x 8*** SRAM in **U27 - U42** for the cache data RAM and ***one(1) 32K x 8*** SRAM in **U19** for the tag RAM.

Also, install the RAs in **RA512** . Refer to the following figure for the locations of the SRAM and the RAs.

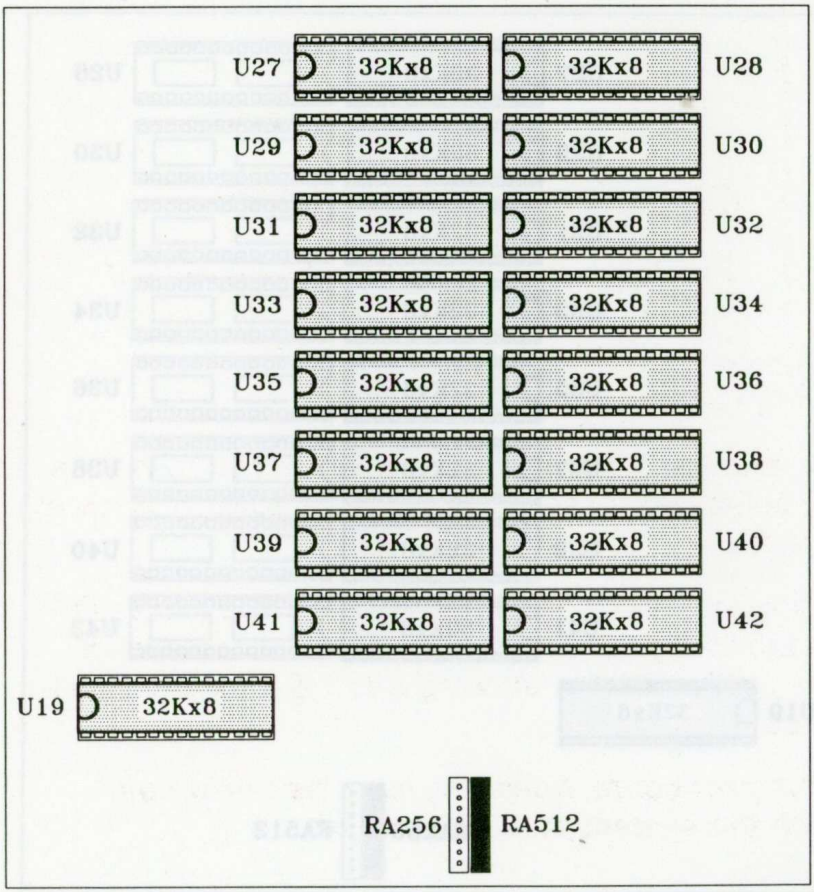


Figure 5: PAT54PV with 512KB of cache memory

4.9 Battery Selection Jumper: JP1

This *3-pin* header allows the user to select whether the on board battery or an external battery for the CMOS RAM and the Real Time Clock is being used.

JP1	Function
	Use the on board battery
	Clear CMOS RAM
	Use an external battery connected to J2

Note

No external battery can be connected to J2 when the on board battery setting is chosen. Doing so will damage the on board battery.

If you are having difficulty booting up due to invalid Setup configuration, you may clear the contents of the CMOS RAM by shorting pins 1 & 2 for a few seconds.

This procedure, however, must be performed with the system power turned off.

4.10 P54C CPU Core/Bus Frequency Selection

CPU	JP18
P54C 100/66	
P54C 90/60	
P54C 75/50	

Chapter 5 Installation

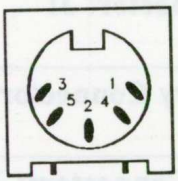
This chapter describes the interface that the PAT54PV provides for creating a working system. Refer to Figure 2 for the locations of the connectors.

The following items are covered in this chapter.

5.1 Keyboard Connector: J1

The keyboard connector, **J1**, is a *5-pin DIN* connector for attaching an IBM AT or an IBM Enhanced 101-key compatible keyboard.

The following describes the pin-out assignment of this connector.



J1 Pin #	Description
1	Keyboard Clock
2	Keyboard Data
3	N.C.
4	Ground
5	V_{cc}

5.2 External Battery Connector: J2

This *4-pin* connector, **J2**, allows the user to connect an external battery to maintain the information stored in the CMOS RAM.

J2 Pin #	Description
1	Vcc
2	N. C.
3	Ground
4	Ground

Note

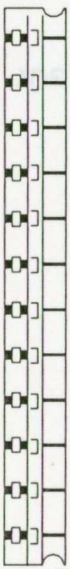
The external battery should be a 6V battery.

5.3 Power Supply Connector: J3 and J4

When using an AT compatible power supply, plug both of the power supply connectors into **J3 and J4.**

Make sure the power supply connectors are connected in the right orientation. The power supply connectors are connected in the right orientation if the black wires of each power cable are *ADJACENT* to each other. That is, the black wires of each connector should be aligned in the center of the power supply connectors, J3 and J4, of the PAT54PV

The following table indicates the pin-out assignments of the power supply connector.

Pin #		Description	Wire Color
1		Power Good	Orange
2		+5V	Red
3		+12V	Yellow
4		-12V	Blue
5		Ground	Black
6		Ground	Black
7		Ground	Black
8		Ground	Black
9		-5V	White
10		+5V	Red
11		+5V	Red
12		+5V	Red

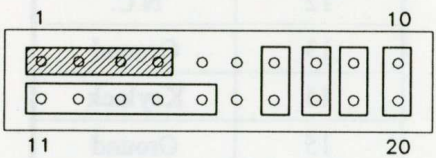
5.4 Speaker Connector: J6(Pins 1 - 4)

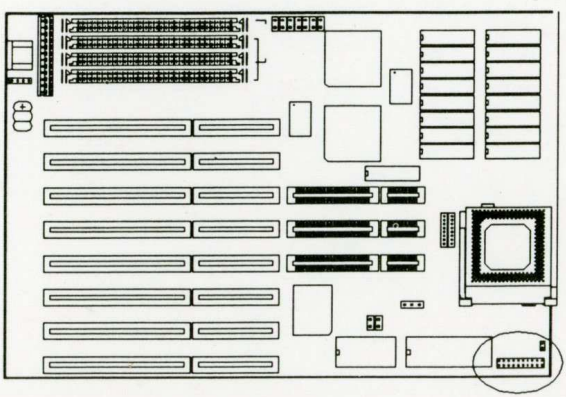
Pins 1 - 4 of the 20-pin connector, **J6**, provide an interface to a speaker for audio tone generation. This connector provides four pins but only two pins are used. A speaker with 8-Ohm or higher impedence is recommended.

Note

Orientation is not required when connecting a speaker to pins 1 - 4 of J6.

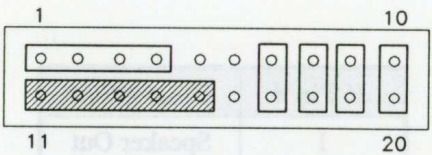
J6 Pin #	Description
1	Speaker Out
2	N.C.
3	Ground
4	+ 5V





5.5 Power LED and Keylock Connector: J6(Pins 11 - 15)

Pins 11 - 15 of the 20-pin connector, **J6**, allow the user to connect the power LED and keylock switch of the system's front panel. The power LED indicates the *ON/OFF* status of the system. The keylock switch, when *CLOSED*, will disable the keyboard function.

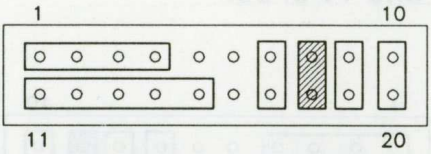


J6 Pin #	Description
11	Power LED
12	N.C.
13	Ground
14	Keylock
15	Ground

5.6 Turbo LED Connector: J6(Pins 8 & 18)

Pins 8 & 18 of the 20-pin connector, **J6**, provide the user with an interface for connecting a turbo LED indicator in the system's front panel.

This LED, when on, indicates the **TURBO**(*FULL*) speed mode of the PAT54PV system.



J6 Pin #	Description
8	Anode
18	Cathode

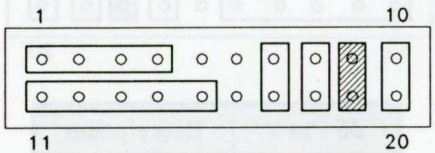
5.7 Reset Switch Connector: J6(Pins 9 & 19)

Pins 9 & 19 of the 20-pin connector, **J6,** provide an interface for a reset switch. The reset switch allows the user to reset the system without turning the power switch off and on.

To reset the PAT54PV based system, *SHORT* pins 9 and 19 of J6 by pressing the reset switch of the system chassis.

Note

Orientation is not required when connecting a reset switch pins 9 and 19 of J6.



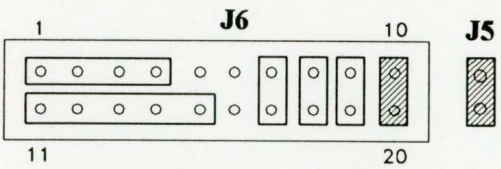
5.8 Hard Disk LED Connector: J6(Pins 10 & 20), J5

These connectors allow the user to connect the hard disk access LED on the system's front panel. The LED will be on whenever the system is accessing the hard drive.

Connect the 2-pin connector from the system chassis to *pins 10 & 20* of **J6**. Also, make a connection from **J5** to the hard disk controller's LED interface.

Note

You may also connect HDD LED on the system's front panel directly to the hard disk controller's LED interface without using these connectors.



Pin #	Description
J6(Pins 10 & 20)	LED In
J5	LED Out

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