# PAT38PC

Version 1.0

# User's Manual

# PAT38PC
# System Board
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(ver 1.0)

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User's Manual
PAT38PC System Board
1st Edition (January 1990)
TMC Research Corporation

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# Organization

This manual is organized as follows:

**Chapter 1 Introduction** - Introduces the PAT38PC system board and the memory cards.

**Chapter 2 Specifications** - Lists and explains the specifications of the PAT38PC system board.

**Chapter 3 Hardware Description** - Describes each of the major features of the PAT38PC system board.

**Chapter 4 Configuring the PAT38PC** - Describes the necessary procedures and jumper settings to configure the PAT38PC system board.

**Chapter 5 Installation** - Describes the interfaces the PAT38PC provides for creating a working system.

**Chapter 6 Options** - Describes the installation and configuration procedures for the options of the PAT38PC.

## 1. Introduction

The PAT38PC is a high performance system board that is functionally compatible with the system board in the IBM AT. The brain of the PAT38PC system board is the powerful Intel 32-bit 80386. The PAT38PC is designed with a highly integrated chipset using VLSI technology to achieve high reliability, small footprint, and low power consumption.

The built in cache controller provides the user with the following features: the user can select the cache RAM size and the cache line size. This provides better cache hit rates in real life applications. The cache design of the PAT38PC ensures the user zero wait state access without the use of high speed DRAMs.

Main memory expansion on the PAT38PC is easy as the system board accepts up to 8MB of SIMM memory. And for your memory hungry applications, the PAT38PC's Page Interleave memory can be increased to 16MB by using an optional high-speed memory card. There are two 32-bit memory cards available for the PAT38PC: DIP8P and SIM16P. The DIP8P accepts 1M x 1 DIP chips and the SIM16P accommodates 256KB or 1MB SIM modules.

The PAT38PC has a coprocessor socket which can accommodate either an Intel 80387 or a Weitek 3167 numeric coprocessor.

With its high performance and reliability, the PAT38PC is the solution to your computing needs.

## 2. Specifications

**Main Processor**
Intel 80386 CPU

**Coprocessor Support**
A socket to accommodate Intel 80387 or Weitek 3167

**Cache Controller**
Built-in direct mapped cache controller

**Cache RAM**
32KB, expandable to 64KB
Selectable 4, 8, or 16 byte line size

**System Memory(on board)**
Eight SIMM sockets for 256K x 9 or 1M x 9 SIMMs

**System Memory(on memory card)**
One 32-bit memory slot
Optional 8MB or 16MB 32-bit memory card

**BIOS**
Licensed BIOS in a single 27C512 EPROM

**Clock Calendar**
Battery backed RTC and CMOS RAM

**Interrupts**
Sixteen levels of hardware interrupts

**Timers**
Three programmable timers

**Expansion Slots**
One 32-bit slot, can be used as a 16-bit slot when not used by a 32-bit memory card
Six 16-bit slots
One 8-bit slot

**Connectors**

Connectors for: power supply, keyboard, reset switch, keylock and power LED, speaker, turbo switch, and turbo LED

**Physical Dimensions**

8.5"(Width) x 13"(Length)

**Power Requirement**

+ 5V 2.5 AMP

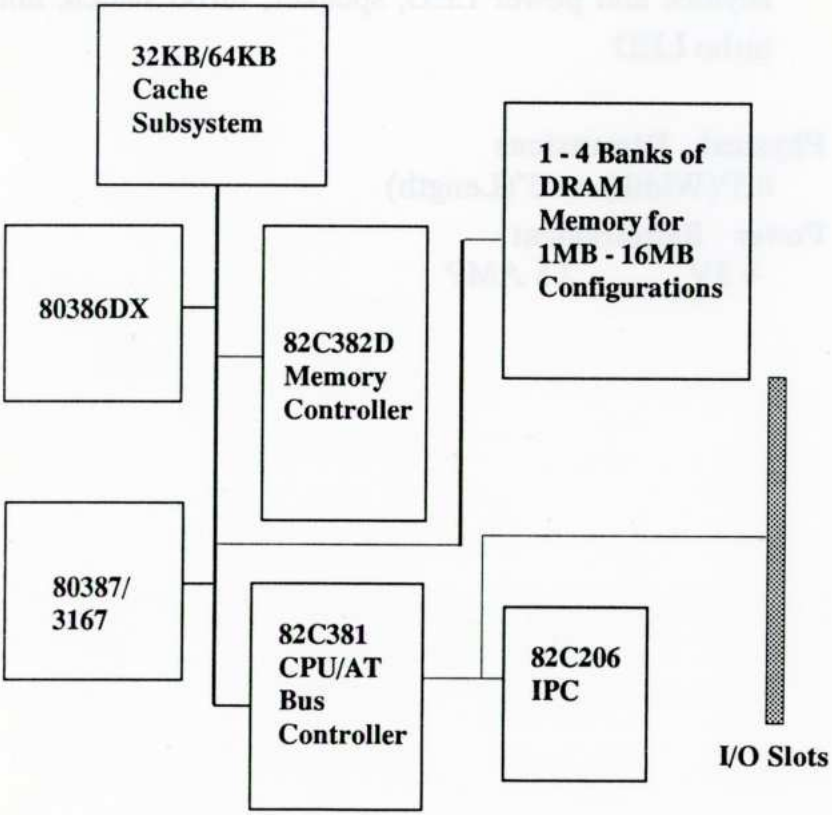



Figure 1: PAT38PC function block

## 3. Hardware Description

This section briefly describes each of the major features of the PAT38PC system board. A layout of the board is shown in Figure 2 to show the locations of the key components. The topics covered in this section are as follows:

Main Processor - Intel 80386

Math Coprocessor - Intel 80387 or Weitek 3167

Cache Controller and Cache Memory

System Memory

I/O Port Address Map

Memory Mapping

BIOS ROM

Timer

DMA Channels

Interrupt Controllers

Real Time Clock and CMOS RAM

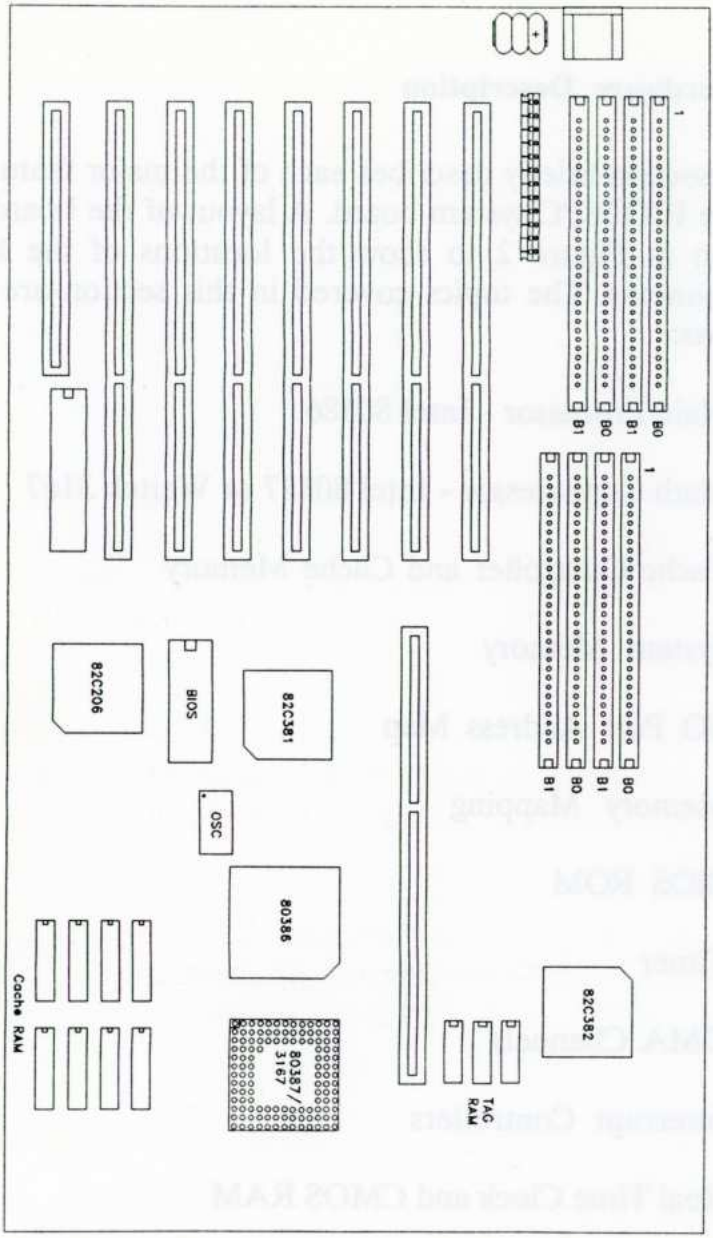



Figure 2: Layout of the PAT38PC

## 3.1 System Board

The PAT38PC is designed by implementing an 80386 CPU and a highly integrated chipset. The chipset consists of the **82C381** CPU/BUS controller and the **82C382D** memory controller. Combined with the **82C206,** Integrated Peripherals Controller, the chipset integrates the 386/AT system board with under 20 devices, plus memory.

The **82C381** provides system logic and data bus conversion logic. The control logic consists of 386 CPU control logic, AT bus cycle control, 387 Numeric coprocessor control logic, synchronous clock divide logic and control of the local peripheral bus.

The **82C382D** performs the Memory Management functions. It supports 32KB or 64KB Direct Mapped Cache Memory along with page interleave for the main memory.

The **82C206** Integrated Peripheral Controller (IPC) incorporates the DMA controller, Interrupt controller, Timer, and Clock/Calendar functions.

## 3.2 80386 CPU

The Central Processing Unit of the PAT38PC system board is Intel's 80386 microprocessor. It provides unprecedented performance, and is upward compatible with Intel's 8088, 8086, and 80286 microprocessor. The 80386 CPU has 32-bit wide internal and external data paths. The 32-bit address lines provide a physical memory capacity of four gigabytes. The design of the PAT38PC implements 24 address lines, limiting the actual physical address space to 16 Mbytes. The virtual 8086 mode permits concurrent execution of multiple software to support the multi-tasking operating system.

## 3.3 Math Coprocessor (Optional)

The PAT38PC has a 121-pin PGA socket to accommodate either the Intel 80387 or the Weitek 3167 coprocessor. The Intel 80387 or the Weitek 3167 will be running in synchronous mode with respect to the CPU. For details on the installation of the 80387 or the 3167, refer to **Section 6.3 Math Coprocessor.**

## 3.4 Cache Controller and Cache Memory

The PAT38PC is designed by implementing an 82C382D cache memory controller with user selectable cache size of 64KB or 32KB of SRAM. It will achieve zero wait state without the use of high speed DRAMs for the system memory. The memory controller also provides a page interleave backend for main DRAM memory, in order to improve performance during cache miss cycles.

The 82C382D provides flexible implementation of paging for the main DRAM memory. For even bank configurations it provides 2 or 4-way page-interleaving; for odd banks it provides page mode accesses.

## 3.5 System Memory

The memory controller, 82C382D, of the PAT38PC can control up to four 32-bit memory banks. To maximize the on board memory capacity and still provide flexibility in expanding the system memory, the PAT38PC provides 2 banks of SIMM memory and a 32-bit memory expansion slot to accommodate an optional 32-bit memory card. Together they provide upto 16MB of Page Interleave memory. The on board memory consists of two 32-bit banks with four memory sockets for each bank. The SIMM sockets are designed to accept either 256KB or 1MB modules, giving the user great flexibility in memory configurations. An optional 32-bit memory card can be installed in the system to increase the memory capacity of the PAT38PC upto 16 MB.

Refer to the following subsections for details on the possible memory configurations of the PAT38PC with the DIP8P and SIM16P.

The following table illustrates the possible on board memory configurations of the PAT38PC.

| Total Memory | PAT38PC | |
|---|---|---|
| | Bank 0 | Bank 1 |
| 1MB | 256K x 9 | --- |
| 2MB | 256K x 9 | 256K x 9 |
| 4MB | 1M x 9 | --- |
| 8MB | 1M x 9 | 1M x 9 |

### 3.5.1 Memory Expansion

There are two 32-bit memory cards available for the PAT38PC, the DIP8P and the SIM16P. The DIP8P consists of two 32-bit banks, with each bank consisting of 36 1M x 1 bit DRAMs. The SIM16P has four 32-bit memory banks, Banks 0 through 3. Each bank consists of four SIMM sockets which are designed to accept 256K x 9 or 1M x 1 SIMMs.

The following table summarizes the memory bank assignments of the PAT38PC, DIP8P, and SIM16P.

| PAT38PC memory banks | On board SIMM memory | DIP8P | | SIM16P |
|---|---|---|---|---|
| | | JP1 - JP10 1, 2 Short | JP1 - JP10 2, 3 Short | |
| Bank 0 | X | X | | X |
| Bank 1 | X | X | | X |
| Bank 2 | | | X | X |
| Bank 3 | | | X | X |

## General Rules for PAT38PC's Memory Expansion

**1. No Partial Banks**

For example, when installing SIMMs on bank 0 of the PAT38PC, all four SIMM sockets must be populated.

**2. No Bank Overlap**

For example, you cannot install SIMMs on bank 0 on the PAT38PC system board and at the same time install DIP chips on bank 0 of the DIP8P.

**3. No Mix of Memory Sizes in the Same Bank**

For example, you cannot mix 256K SIMMs with 1M SIMMs in the same bank.

**4. No Bank Gap**

For example, you cannot populate Banks 0 and 2 and leave bank 1 unpopulated.

For details on possible memory configurations with the SIM16P or the DIP8P, refer to **Sections 6.1 and 6.2.**

## 3.6 I/O Port Address Map

The 80386 CPU communicates via I/O ports. There are a total of 1K port address space defined. The following table lists the I/O port addresses used in the PAT38PC and those assigned to other devices that can be used by I/O expansion cards.

### Devices on the System Board

| Address | Device |
|---|---|
| 000 - 01F | DMA Controller #1 |
| 020 - 03F | Interrupt Controller #1 |
| 040 - 05F | Timer |
| 060 - 06F | Keyboard Controller |
| 070 - 07F | Real Time Clock, NMI |
| 080 - 09F | DMA Page Register |
| 0A0 - 0BF | Interrupt Controller #2 |
| 0C0 - 0DF | DMA Controller #2 |
| 0F0 | Clear Math Coprocessor Busy Signal |
| 0F1 | Reset Math Coprocessor |

## Devices on the I/O slots

| Address | Description |
|---|---|
| 1F0 - 1F8 | Fixed Disk Controller |
| 200 - 207 | Game Port |
| 278 - 27F | Parallel Port #2 (LPT2) |
| 2F8 - 2FF | Serial Port #2 (COM2) |
| 300 - 31F | Prototype Card |
| 360 - 36F | Reserved |
| 378 - 3FF | Parallel Port #1 (LPT1) |
| 380 - 38F | SDLC#2 |
| 3A0 - 3AF | SDLC#1 |
| 3B0 - 3BF | MDA Video Card (including LPTO) |
| 3C0 - 3CF | Reserved |
| 3D0 - 3DF | CGA Video Card |
| 3F0 - 3F7 | Floppy Disk Controller |
| 3F8 - 3FF | Serial Port #1 (COM1) |

## 3.7 Memory Map

The PAT38PC has a maximum memory capacity of 16MB. The first megabyte is divided into four blocks with each block dedicated to a fixed function. The following table illustrates the memory map for the PAT38PC.

| Address | | Description |
|---|---|---|
| 0KB | 000000H | Conventional RAM |
| | 09FFFFH | |
| 640KB | 0A0000H | 128 KB Video RAM |
| | 0BFFFFH | |
| 768KB | 0C0000H | 192KB I/O Expansion ROM |
| | 0EFFFFH | |
| 960KB | 0F0000H | 64KB System BIOS ROM |
| | 0FFFFFH | |
| 1 MB | 100000H | 15 MB User RAM |
| | FEFFFFH | |
| | FF0000H | Duplicated 64KB System BIOS ROM at 0F0000H |
| 16MB | FFFFFFH | |

## 3.8 BIOS

The PAT38PC contains a single 27C512 EPROM that contains the system BIOS. The BIOS resides at the upper 64KB of address space in the first megabyte. In protected mode, the BIOS is also mapped to the upper 64KB of the 16MB space and can be accessed at either location.

The BIOS on the PAT38PC is compatible with the BIOS in the IBM AT with the exception that it does not contain the BASIC interpreter. The BASIC and BASICA on IBM PC-DOS will not run on the PAT38PC. To run BASIC in systems based on the PAT38PC, the user should use the GW-BASIC interpreter provided with the Microsoft DOS diskette.

## 3.9 Timer

The PAT38PC has three channels of timer/counter in the 82C206, which is Intel 8254 compatible. The function of each channel is listed as follows:

| Channel | Function |
|---|---|
| 0 | System timer - This timer generates the time base for the system timer. Its output is tied to IRQ0. |
| 1 | Memory Refresh Request - This timer is used to generate memory refresh requests. It triggers the memory refresh cycle. |
| 2 | Tone Generator for speaker - This timer provides the speaker tone. Various sounds can be generated by programming the timer. |

## 3.10 DMA Channels

The PAT38PC contains the equivalent of two 8237A DMA controllers in the 82C206. The 82C206 provides the user with two DMA controllers and four channels of DMA (DMA #1) for 8-bit transfers and three channels of DMA (DMA #2) for 16 bit transfers.(The first 16-bit DMA channel is used for cascading.)

| Channel | | Function |
|---|---|---|
| Controller #1 | Controller #2 | |
| 0 | | DRQ0, Reserved |
| 1 | | DRQ1, SDLC |
| 2 | | DRQ2, Floppy Disk Controller |
| 3 | | DRQ3, Reserved |
| | 4 | DRQ4, Cascade for DMA |
| | 5 | DRQ5, Reserved |
| | 6 | DRQ6, Reserved |
| | 7 | DRQ7, Reserved |

## 3.11 Interrupt Controller

The PAT38PC contains two Intel 8259A compatible interrupt controllers in the 82C206. Sixteen channels are partitioned into the cascaded controllers (INTC1, INTC2) with 8 inputs each. Of these 16 channels, three are connected internally to various devices, allowing 13 user definable channels of interrupt. Any or all of these interrupts can be masked.

| Level | Function |
|---|---|
| NMI | RAM Parity Check |
| IRQ0 | System Timer Output |
| IRQ1 | Keyboard |
| IRQ2 | Interrupt Cascade |
| IRQ8 | Real Time Clock |
| IRQ9 | Software Redirected to Int 0AH |
| IRQ10 | Reserved |
| IRQ11 | Reserved |
| IRQ12 | Reserved |
| IRQ13 | 80287 |
| IRQ14 | Fixed Disk Controller |
| IRQ15 | Reserved |
| IRQ3 | Serial Port #2 |
| IRQ4 | Serial Port #1 |
| IRQ5 | Parallel Port #2 |
| IRQ6 | Floppy Disk Controller |
| IRQ7 | Parallel Port #1 |

## 3.12 Real Time Clock and CMOS RAM

The PAT38PC contains an MC146818 compatible Real Time Clock (RTC) and 128 bytes of CMOS RAM in the 82C206. The CMOS RAM stores the system's configuration information entered via the Setup program. The RTC and the CMOS RAM are kept active by a battery when the system power is turned off.

## 4. Configuring the PAT38PC

The following sections describe the necessary procedures and proper jumper settings to configure the PAT38PC system board. The following configuration options can be selected:

Video adapter card selection: JP2

Cache RAM size selection: JP4, JP5, JP6, & JP11

Cache line size selection: JP7, JP8

Pipelined mode selection: JP9

Weitek 3167 presence indication: JP10

Math Coprocessor Presence Indication : JP12

Battery selection: JP15

For locations of the jumpers, refer to Figure 3.

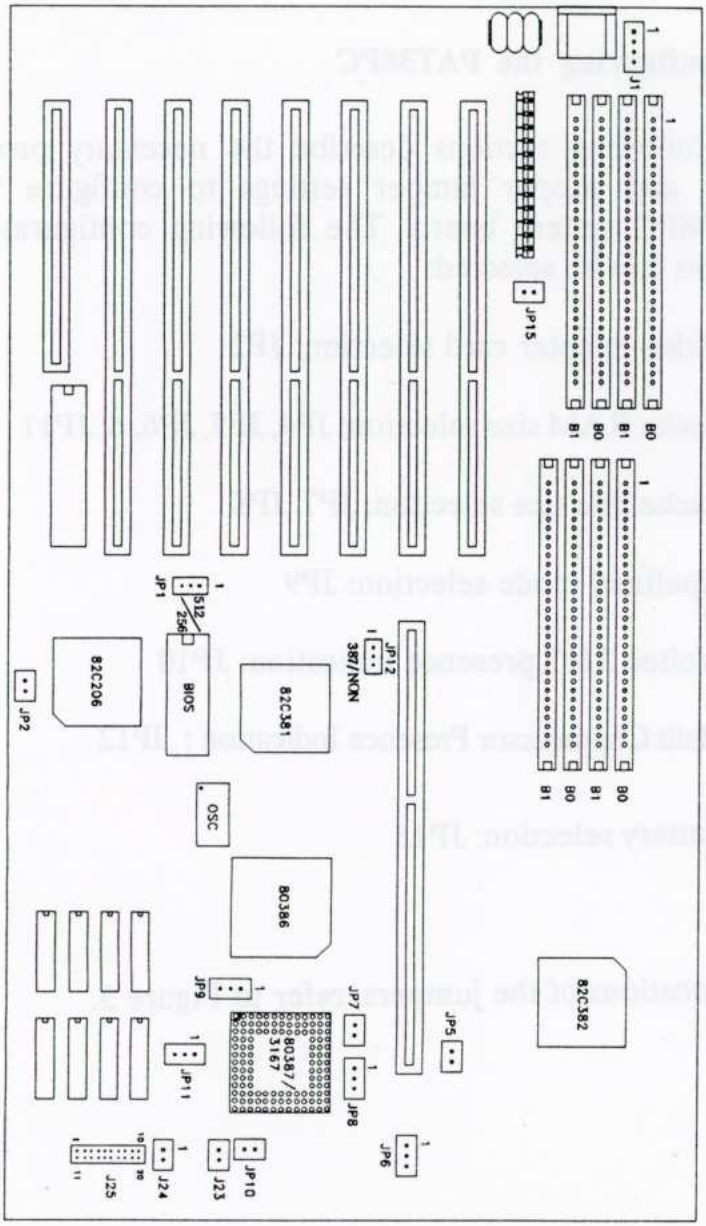



Figure 3: Layout & connector locations of the PAT38PC

## 4.1 Video Adapter Card Selection: JP2

This jumper setting is checked by the system BIOS during system boot-up to decide what type of video card is the primary card on the system board. This jumper setting is also checked against the configuration information stored in the CMOS RAM by the Setup program. If you have only one video card in your system, set the jumper to reflect its type. If more than one video card is installed in your system, set the jumper to indicate which video card is the primary one.

Color Graphics(CGA, EGA, VGA)

Monochrome(MDA, HGC)

## 4.2 Cache RAM Size Selection: JP4 - JP6, & JP11

These jumpers allow the user to select the cache RAM size as 32KB or 64KB. **For total system memory size of less than or equal to 8MB, the cache RAM size can be either 32KB or 64KB. If the system memory size is larger than 8MB, 64KB of cache RAM must be installed.**

The following table illustrates the necessary jumper settings. For the locations of these jumpers and cache RAMs, refer to figures 4 and 5.

| Cache | JP4 | JP5 | JP6 | JP11 |
|---|---|---|---|---|
| **32KB** | 2, 3 Short | Open | 1, 2 Short | 1, 2 Short |
| **64KB** | 2, 3 Short | Close | 2, 3 Short | 2, 3 Short |

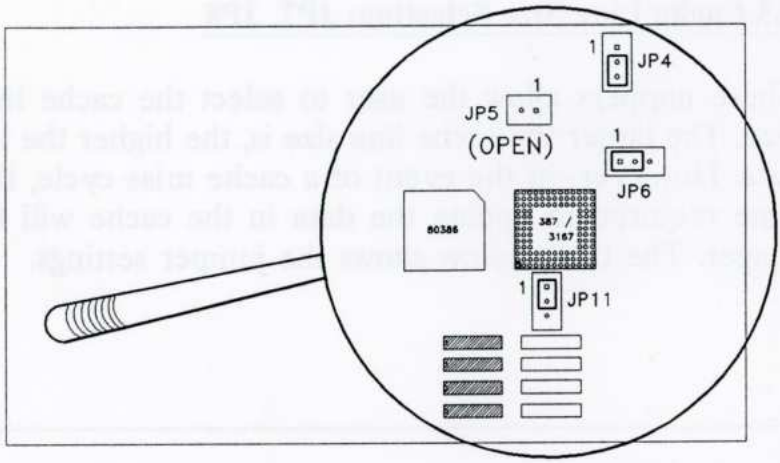



Figure 4: 32KB of cache RAM

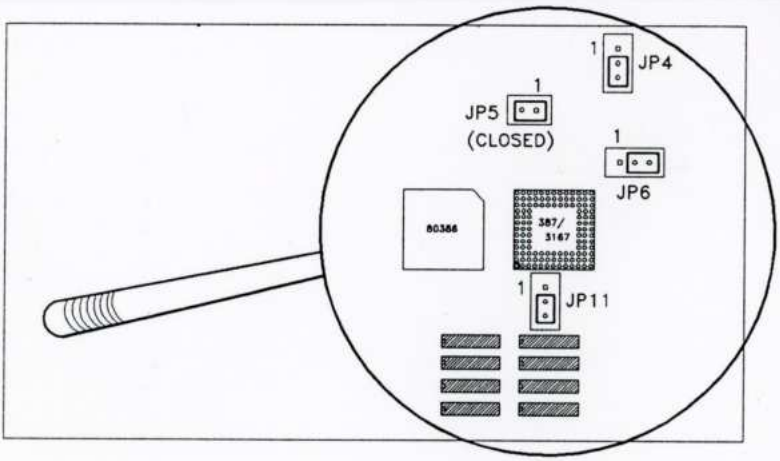



Figure 5: 64KB of cache RAM

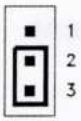
## 4.3 Cache Line Size Selection: JP7, JP8

These jumpers allow the user to select the cache line size. The larger the cache line size is, the higher the hit rate. However, in the event of a cache miss cycle, the time required to update the data in the cache will be longer. The table below shows the jumper settings.

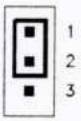
| Line Size | JP7 | JP8 |
|---|---|---|
| **4 bytes** | Close | 1, 2 Short |
| **8 bytes** | Close | 2, 3 Short |
| **16 bytes(Default)** | Open | 2, 3 Short |

## 4.4 Pipelined Mode Selection: JP9

This jumper setting allows the user to select between two choices of address timing: non-pipelined and pipelined. To maximize the performance, enable the pipelined mode for page-interleave(non-cache) operations. **For cache operations, always disable pipelined mode.**




Pipelined Mode Enabled




Pipelined Mode Disabled
**(Required when the cache RAMs are installed.)**

*Note: Depending on your specifications, cache or non-cache, this jumper is configured at the factory.*

## 4.5 Weitek 3167 Presence Indication: JP10

This jumper must be set to indicate whether the Weitek 3167 is present or not present.

*Note: The presence of an 80387 will be automatically detected by the CPU.*

Weitek 3167 Present

No Weitek 3167

## 4.6 Battery Selection: JP15

This jumper setting allows the user to select whether the on board battery or an external battery for the CMOS RAM and the RTC is being used.

Use the on board battery

Use an external battery connected to J1

*Note:*

1. *No external battery can be connected to J1 when the on board is chosen. Doing so will damage the on board battery.*
2. *The on board battery is a rechargeable battery. It will always be charged whenever the system is running. The on board battery is fully charged at the factory as a part of the burn in process. The on board battery should be able to hold the contents of the CMOS RAM and keep the RTC running for 3 months without recharge.*

## 4.7 Math Coprocessor Presence Indication: JP12

This jumper must be set to indicate whether the math coprocessor is present or not present. **Not setting this jumper properly will cause differently during system bootup.**


80387 Installed


NO 80387

## 5. Installation

This section describes the interface that the PAT38PC provides for creating a working system. Please refer to Figure 3 for location of the connectors.

The following items are covered in this section.

External Battery Connector: J1

Keyboard Connector: J2

Power Supply Connectors: J3, J4

Turbo LED Connector: J25

Power LED and Keylock Connector: J25

Speaker Interface: J25

Turbo Switch: J25

Reset Switch: J25

Hard Disk Drive Access Indicator LED: J24, J25

## 5.1 External Battery Connector: J1

This four pin connector, J1, allows the user to connect an external battery to maintain the information stored in the CMOS RAM.

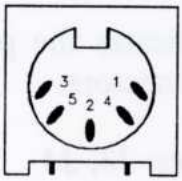
| Pin # | Description |
|---|---|
| 1 | Vcc |
| 2 | N.C. |
| 3 | N.C. |
| 4 | Ground |

*Note: The external battery should be a 6V battery.*

## 5.2 Keyboard Connector: J2

The keyboard connector, J2, is a 5-pin DIN connector for connecting an IBM AT or an IBM Enhanced 101-key compatible keyboard.

The following table describes the pin-out assignments of this connector.




| Pin # | Function |
|---|---|
| 1 | Clock |
| 2 | Data |
| 3 | N.C. |
| 4 | Ground |
| 5 | Vcc |

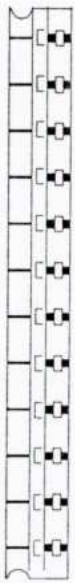
## 5.3 Power Supply Connectors: J3, J4

When using an AT compatible power supply, plug both of the power supply connectors into J3 and J4.

*Caution: Extreme care must be taken when plugging in the power supply connectors. If the connectors are not connected in the right orientation, both the system board and the power supply will be damaged.*

The following figure indicates the pin-out assignments of the power supply connectors:

**Power Supply Connectors: J3, J4**

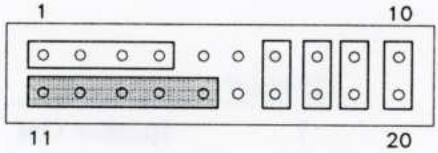


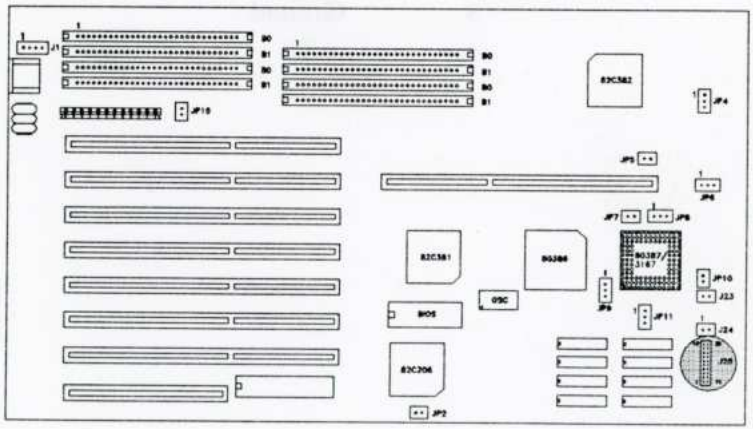
| Pin # | Description | Wire Color |
|---|---|---|
| 1 | Power Good | Orange |
| 2 | +5V | Red |
| 3 | +12V | Yellow |
| 4 | -12 V | Blue |
| 5 | Ground | Black |
| 6 | Ground | Black |
| 7 | Ground | Black |
| 8 | Ground | Black |
| 9 | -5 V | White |
| 10 | +5V | Red |
| 11 | +5V | Red |
| 12 | +5V | Red |

## 5.4 Power LED and Keylock Connector: J25(Pins 11-15)

Pins 11-15 of the 20-pin connector, J25, allow the user to connect the power LED and keylock switch of the system's front panel. The power LED indicates the on/off status of the system. The keylock switch, when closed, will disable the keyboard function.

| J25 Pin # | Function |
|---|---|
| 11 | Power LED |
| 12 | N.C. |
| 13 | Ground |
| 14 | Keylock |
| 15 | Ground |

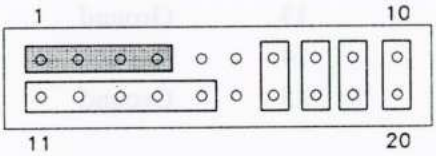


## 5.5 Speaker Interface: J25(Pins 1-4)

Pins 1-4 of the 20-pin connector, J25, provide an interface to a speaker for audio tone generation. This connector provides four pins but only two pins are used. A speaker with 8-Ohm or higher impedence is recommended.

*Note: Orientation is not required when connecting a speaker to pins 1-4.*

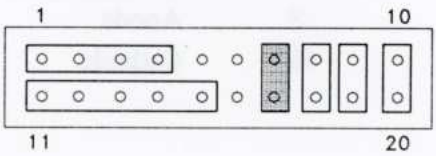



| J25 Pin # | Function |
|---|---|
| 1 | Speaker Out |
| 2 | N. C. |
| 3 | Ground |
| 4 | +5V |

## 5.6 Turbo Switch: J25(Pins 7, 17)

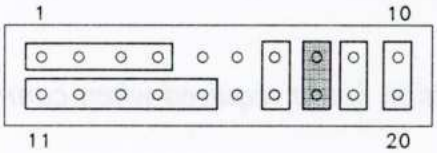
Pins 7 and 17 of the 20-pin connector, J25, allow the user to connect a turbo switch on the front panel of the system chassis. A turbo switch is usually a push-on switch. When the switch is **on**, Pins 7 & 17 is shorted and the CPU will be running at **full** speed. To switch to **low(non-turbo)** speed, simply depress the switch. To return to **high(turbo)** speed mode, press the switch again.

*Note: Orientation is not required when connecting a turbo switch.*



## 5.7 Turbo LED Connector: J25(Pins 8 and 18)

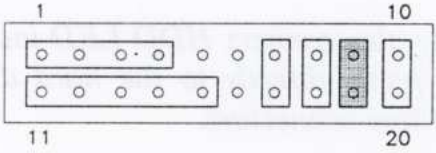
Pins 8 and 18 of the 20-pin connector, J25, provide the user with an interface for connecting a turbo LED indicator in the system's front panel. This LED, when on, indicates the turbo(high) speed mode of the PAT38PC.




| Pin # | Function |
|---|---|
| 8 | Anode |
| 18 | Cathode |

## 5.8 Reset Switch: J25(Pins 9 and 19)

Pins 9 and 19 of the 20-pin connector, J25, provide an interface for a reset switch. The reset switch allows the user to reset the system without turning the power switch off and on.

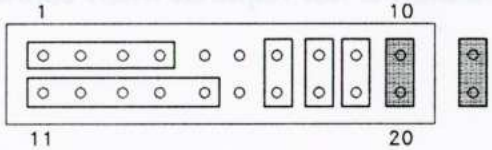



*Note: Orientation is not required when connecting a reset switch.*

## 5.9 Hard Disk Drive Access LED: J24, J25(Pins 10 and 20)

These connectors allow the user to connect the hard disk access LED indicator on the system's front panel. The LED will be on whenever the system is accessing the hard drive. Connect the 2-pin connector from the system chassis to pins 10 and 20 of J25. Also, make a connection from J24 to the hard disk controller's LED interface.

*Note: You may also connect HDD LED indicator on the system's front panel directly to the hard disk controller without using these connectors.*




| J25 (Pins 10 & 20) | J24 |
|---|---|
| LED in | LED out |

## 6. Options

This section describes the installation and configuration of the options for the PAT38PC. The optional boards and equipment include the following:

DIP8P

SIM16P

Math Coprocessors - Weitek 3167 and Intel 80387

## 6.1 DIP8P

The DIP8P is a high-speed 32-bit memory card designed for the PAT38PC. The DIP8P consists of two memory banks with each bank containing 36 DIP chip sockets. The DIP sockets of the DIP8P accept 1M x 1 DRAMs, and when fully populated, will extend the PAT38PC's Page Interleave memory by an additional 8MB.

### Jumper Settings

The DIP8P can be used in two ways, depending on how its memory banks are assigned. There are ten jumpers, JP1 through JP10, on the DIP8P which allow the user to configure the memory banks on the DIP8P as Banks 0 and 1 or as Banks 2 and 3.

Assigning the memory banks on the DIP8P as Banks 0 and 1 will allow the user to utilize DIP memory chips for Banks 0 and 1 instead of SIMMs.

Assigning the memory banks on the DIP8P as Banks 2 and 3 will allow the user to add additional 8MB to the system.

Figures 6 and 7 show the necessary jumper settings.

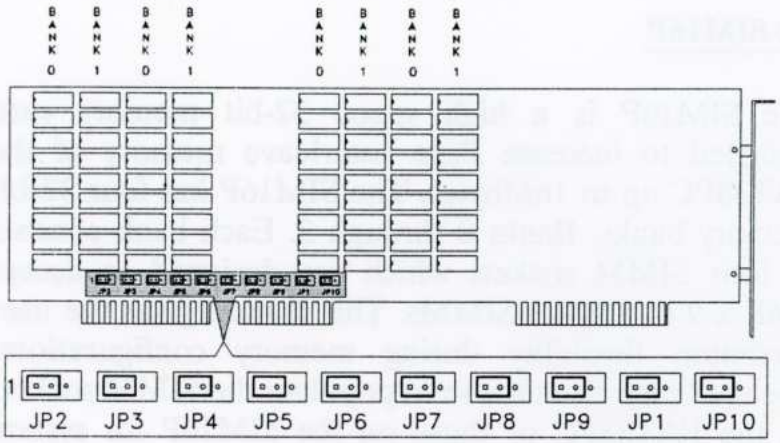



Figure 6: DIP8P configured as Banks 0 & 1 of the PAT38PC

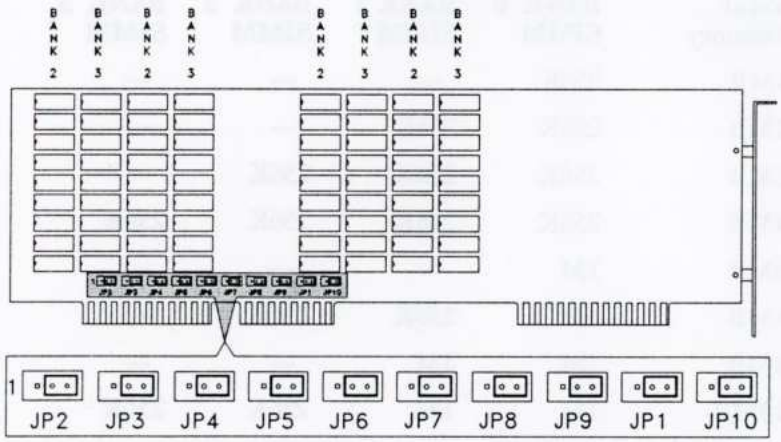



Figure 7: DIP8P configured as Banks 2 & 3 of the PAT38PC

## 6.2 SIM16P

The SIM16P is a high speed 32-bit memory card designed to increase Page Interleave memory of the PAT38PC up to 16Mbytes. The SIM16P has four 32-bit memory banks, Banks 0 through 3. Each bank consists of four SIMM sockets which are designed to accept 256K x 9 or 1M x 9 SIMMs. This feature gives the user maximum flexibility during memory configurations. The user may also choose to populate the SIMM sockets on the PAT38PC or those on the SIM16P for system memory Banks 0 and 1. The following table illustrates the possible memory configurations of the SIM16P.

| Total Memory | BANK 0 SIMM | BANK 1 SIMM | BANK 2 SIMM | BANK 3 SIMM |
|---|---|---|---|---|
| 1MB | 256K | --- | --- | --- |
| 2MB | 256K | 256K | --- | --- |
| 3MB | 256K | 256K | 256K | --- |
| 4MB | 256K | 256K | 256K | 256K |
| 4MB | 1M | --- | --- | --- |
| 6MB | 1M | 256K | 256K | --- |
| 8MB | 1M | 1M | --- | --- |
| 10MB | 1M | 1M | 256K | 256K |
| 12MB | 1M | 1M | 1M | --- |
| 16MB | 1M | 1M | 1M | 1M |

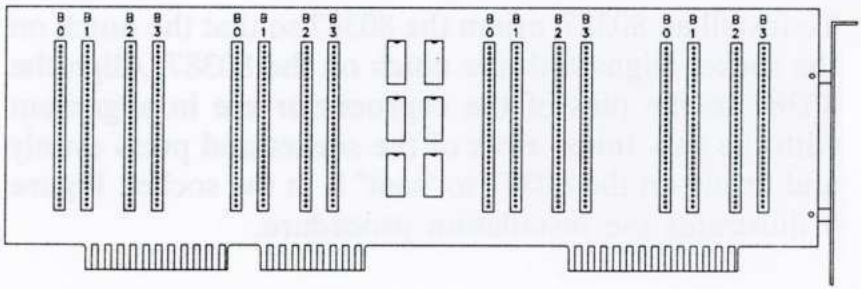



Figure 8: Layout & bank identification of the SIM16P

*Note:*

1. *A memory bank on the SIM16P consists of 4 SIMMs.*
2. *The SIM16P contains four 32-bit memory banks. Therefore if you populate Banks 0 and 1, the SIMM sockets on the PAT38PC must remain empty to avoid bank overlap. The reverse is also true. For details on memory banks, refer to Section 3.5.1 "Memory Expansion."*

## 6.3 Math Coprocessors

The PAT38PC provides a PGA socket to accommodate an Intel 80387 or a Weitek 3167 math coprocessor.

To install an 80387, orient the 80387 so that the notch on the socket aligns with the notch on the 80387. Align the 80387 so the pins of the coprocessor are in alignment with the **two inner rows** of the socket and press evenly and firmly on the 80387 to "seat" it in the socket. Figure 9 illustrates the installation procedure.

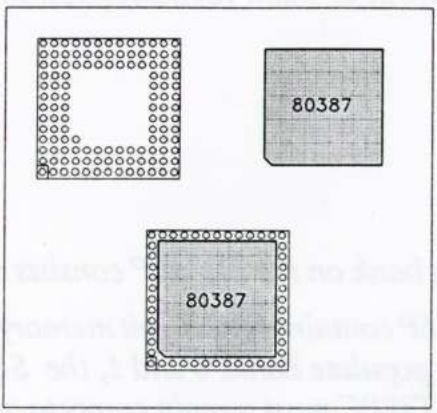



Figure 9: Installation of an 80387

*Note: The 80387 has a total of 68 pins. Therefore, you must align the 80387 with the two inner rows of the PGA socket. Also note that the CPU will automatically recognize the presence of an.80387 and no jumper change is required.*

To install a Weitek 3167, align the notch of the Weitek 3167 with the notch on the socket and press firmly and evenly on the 3167 coprocessor. Figure 10 illustrates the installation procedure.

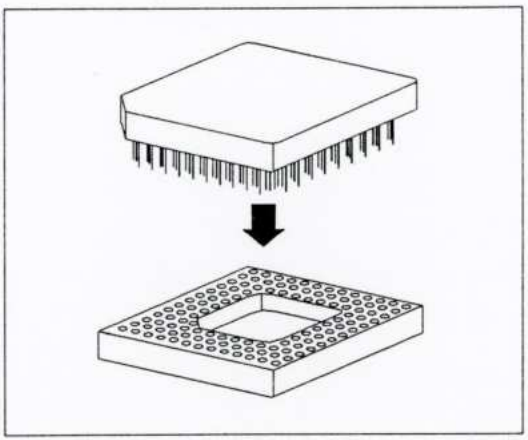


Figure 10: Installation of a Weitek 3167

*Note: Refer to Section 4.5, " Weitek 3167 Presence Indication" and properly set the jumper to indicate the presence of a Weitek 3167.*

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