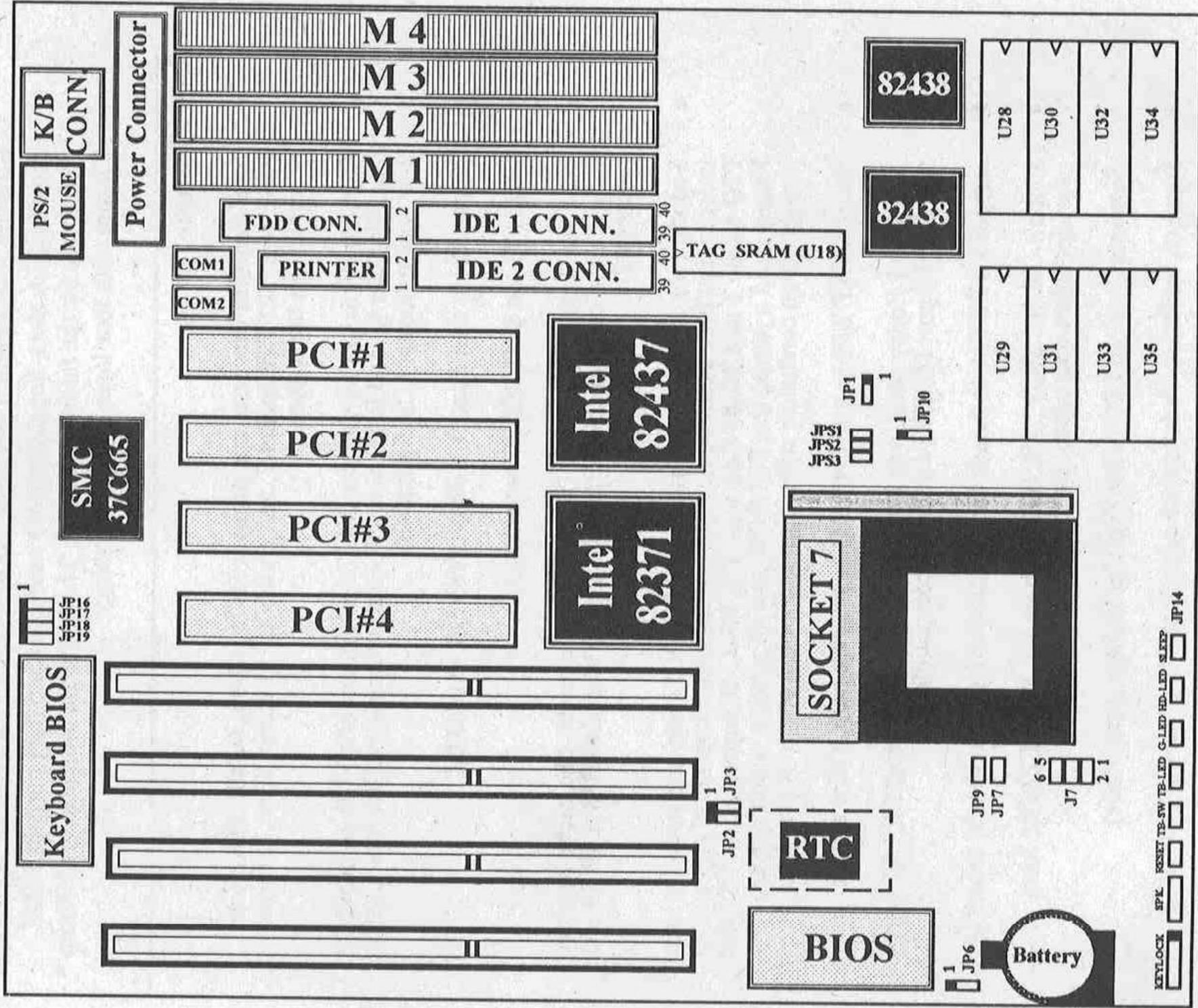
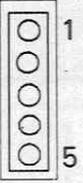


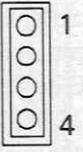
P54C-IP Layout



2-2 Connectors and Jumpers

This section describes all of the connectors and jumpers equipped in the motherboard. Please refer to **Figure 1-1** for actual location of each connector and jumper.

J1  **KeyLock - Keyboard lock switch & Power LED connector.**
 1. Power LED(+)
 2. N/C
 3. GND
 4. Keylock
 5. GND

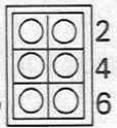
J2  **Speaker - connect to the system's speaker for beeping.**
 1. Speaker
 2. N/C
 3. GND
 4. GND

J3  **Reset - Close to restart system.**

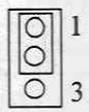
J4  **Turbo Switch : Open for higher speed while Close for slower speed. A BIOS hot key <CTRL><ALT><+> also brings system to a higher speed while <CTRL><ALT><-> set system to a slower speed.**

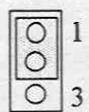
J5  **Turbo LED indicator - LED ON when higher speed is selected.**

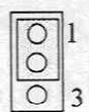
J6  **Power Saving LED indicator - LED ON when system is in any Saving mode.**

J7  **The Power supply of the CPU cooling fan**
 1,2 GND
 3,4 +12V
 5,6 GND

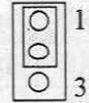
JP5  **IDE LED indicator - LED ON when Onboard PCI IDE Harddisks activites.**

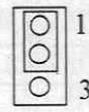
JP1  **CPU Install : 1-2 for Intel Pentium P54C, P54CS CPU (Default). 3-4 for Intel Pentium P55C CPU.**

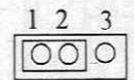
JP2  **Onboard IDE 1: 1-2 for Primary IDE 1 Interrupt IRQ14. 2-3 for None**

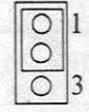
JP3  **Onboard IDE 2 : 1-2 for Secondary IDE 2 Interrupt IRQ15. 2-3 for None**

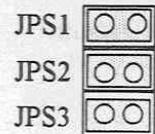
JP14  **Sleep/Resume switch : Close to enter sleep mode. A keystrote or mouse movement (mouse driver exists). The system will instantly "wake up".**

J16  **Serial port (COM 2) : 1-2 for the 2st. serial port IRQ3.(Default) 2-3 for the 2st. serial port IRQ10.**

J17  **Serial port (COM 1) : 1-2 for the 1st. serial port IRQ4.(Default) 2-3 for the 1st. serial port IRQ11.**

J18  **Parallel Mode : 1-2 for the ECP mode at DMA3.(Default)**
J19  **2-3 for the ECP mode at DMA1.**

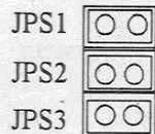
JP6  **EPROM BIOS Select : 1-2 for 5V Flash EPROM while 2-3 for 12V Flash EPROM.**



| Clock chip is IMI SC464 * | | | | | |
|---------------------------|-------|-------|-------|-------|-------|
| Clock/CPU Op. | JPS1 | JPS2 | JPS3 | JP7 | JP9 |
| 50/75 MHz | CLOSE | OPEN | OPEN | OPEN | OPEN |
| 60/90 MHz | CLOSE | OPEN | CLOSE | OPEN | OPEN |
| 66/100 MHz | CLOSE | CLOSE | CLOSE | OPEN | OPEN |
| 60/120 MHz | CLOSE | OPEN | CLOSE | CLOSE | OPEN |
| 66/133 MHz | CLOSE | CLOSE | CLOSE | CLOSE | OPEN |
| 60/150 MHz | CLOSE | OPEN | CLOSE | CLOSE | CLOSE |

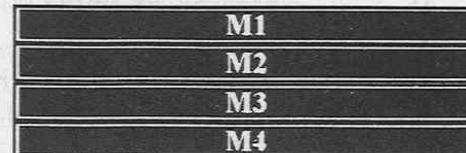
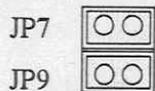
* Note: IMISC464 can't run 50/75 MHz at deturbo (When J4 is OPEN).

* CPU OP. is CPU operation at 75, 90, 100 MHz, etc.



| Clock chip is IMI SC484 | | | | | |
|-------------------------|-------|-------|-------|-------|-------|
| Clock/CPU Op. | JPS1 | JPS2 | JPS3 | JP7 | JP9 |
| 50/75 MHz | OPEN | OPEN | CLOSE | OPEN | OPEN |
| 60/90 MHz | CLOSE | OPEN | CLOSE | OPEN | OPEN |
| 66/100 MHz | CLOSE | CLOSE | CLOSE | OPEN | OPEN |
| 60/120 MHz | CLOSE | OPEN | CLOSE | CLOSE | OPEN |
| 66/133 MHz | CLOSE | CLOSE | CLOSE | CLOSE | OPEN |
| 60/150 MHz | CLOSE | OPEN | CLOSE | CLOSE | CLOSE |

| JP7 | JP9 | CLOCK Chip Frequency. |
|-------|-------|-----------------------|
| OPEN | OPEN | x (3/2) (Default) |
| CLOSE | OPEN | x (2) |
| OPEN | CLOSE | x (3) |
| CLOSE | CLOSE | x (5/2) |



BANK0 Single Side DRAM
BANK0,1 Dual Side DRAM
BANK1 Single Side DRAM
BANK2,3 Dual Side DRAM

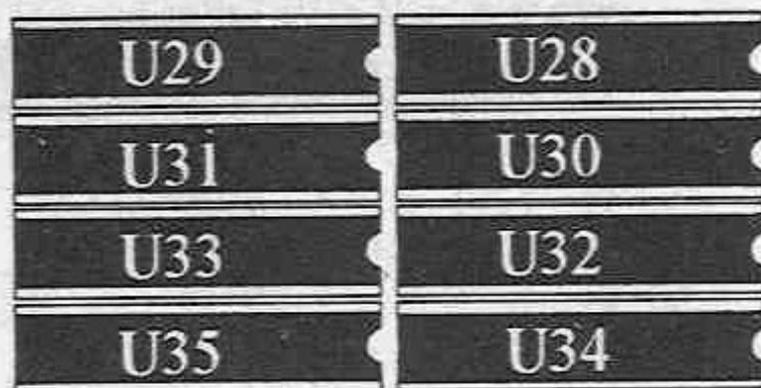
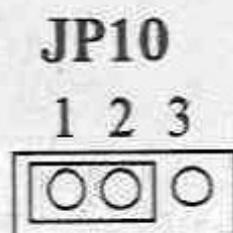
M1,M2(BANK 0) M3,M4(BANK 1) Total Size

| | | |
|-----------------|-----------------|-------|
| 1M x 32 (4 MB) | Empty | 8MB |
| 1M x 32 (4 MB) | 1M x 32 (4 MB) | 16MB |
| 1M x 32 (4 MB) | 2M x 32 (8 MB) | 24MB |
| 1M x 32 (4 MB) | 4M x 32 (16 MB) | 40MB |
| 1M x 32 (4 MB) | 8M x 32 (32 MB) | 72MB |
| 2M x 32 (8 MB) | Empty | 16MB |
| 2M x 32 (8 MB) | 1M x 32 (4 MB) | 24MB |
| 2M x 32 (8 MB) | 2M x 32 (8 MB) | 32MB |
| 2M x 32 (8 MB) | 4M x 32 (16 MB) | 48MB |
| 2M x 32 (8 MB) | 8M x 32 (32 MB) | 80MB |
| 4M x 32 (16 MB) | Empty | 32MB |
| 4M x 32 (16 MB) | 1M x 32 (4 MB) | 40MB |
| 4M x 32 (16 MB) | 2M x 32 (8 MB) | 48MB |
| 4M x 32 (16 MB) | 4M x 32 (16 MB) | 64MB |
| 4M x 32 (16 MB) | 8M x 32 (32 MB) | 96MB |
| 8M x 32 (32 MB) | Empty | 64MB |
| 8M x 32 (32 MB) | 1M x 32 (4 MB) | 72MB |
| 8M x 32 (32 MB) | 2M x 32 (8 MB) | 80MB |
| 8M x 32 (32 MB) | 4M x 32 (16 MB) | 96MB |
| 8M x 32 (32 MB) | 8M x 32 (32 MB) | 128MB |

2-3 System Memory Configuration

The P54C-IP supports different type of settings for the system memory. There is no jumper nor connector needed for memory configuration. Following figures provides all possible memory combinations.

- NOTE :
1. P54C-IP support both Fast Page DRAM or EDO DRAM SIMMs, but they cannot be mixed within the same memory bank.
 2. SIMMs may be parity(x 36) or non parity (x 32).
 3. The 70nS Fast Page Mode or 60nS EDO DRAM is necessary.
 4. "BANK" = 64 Bit = M1, M2 = M3, M4



TAG SRAM

DATA SRAM

| CACHE Size | TAG SRAM (U18) | Data SRAM Install | Jumper Setting |
|------------|---------------------------------------|--|----------------|
| | | | JP10 |
| 256KB | 8K8 x 1 or 16K8 x 1 or 32K8 x 1 | 32K8 x 8 U28,29,30,31 U32,33,34,35 | 1-2 |
| 512KB | 16K8 x 1 or 32K8 x 1 | 64K8 x 8 U28,29,30,31 U32,33,34,35 | 2-3 |