

Notes:

1. This board DOES support Cyrix/TI 486DLC-class CPUs natively, however the board may not come with the jumper necessary to disable the onboard CPU if it is in place. On similar boards, this jumper is labeled JP13. The jumper should be placed in the holes near the JP2 description silk screen.

1a. The jumper manual does not describe this jumper, only listing JP5 and JP20 for Cyrix support. This assumes there is no 386 installed as this particular board seems meant to be set up for one CPU permanently. These jumpers are also not documented on the PCB.

1b. This jumper is wired to the /FLT input on the Am386DX footprint which will disable the CPU. It is also wired to the /KEN input on the Cyrix footprint. The state of this pin is ignored by Cyrix CPUs on power-on and reset, but it is shorted to ground with no resistor. This may cause stability issues on its own, or cache/performance issues if the /KEN input is enabled via software.

2. For Cyrix support, the manual defines that J20 should be [1,2]. This is incorrect and will cause HIMEM to hang with an A20 control error as the description is electrically reversed. The correct setting is [2,3]. This connects the KBC A20 to the Cyrix /A20M line.

3. The list of supported clock speeds is stated to be 25, 33, and 40 MHz. The board may not come with the clock generator circuit present on similar variants. If this is the case, the crystal will need to be swapped, and JP16 does nothing, if it was even populated.