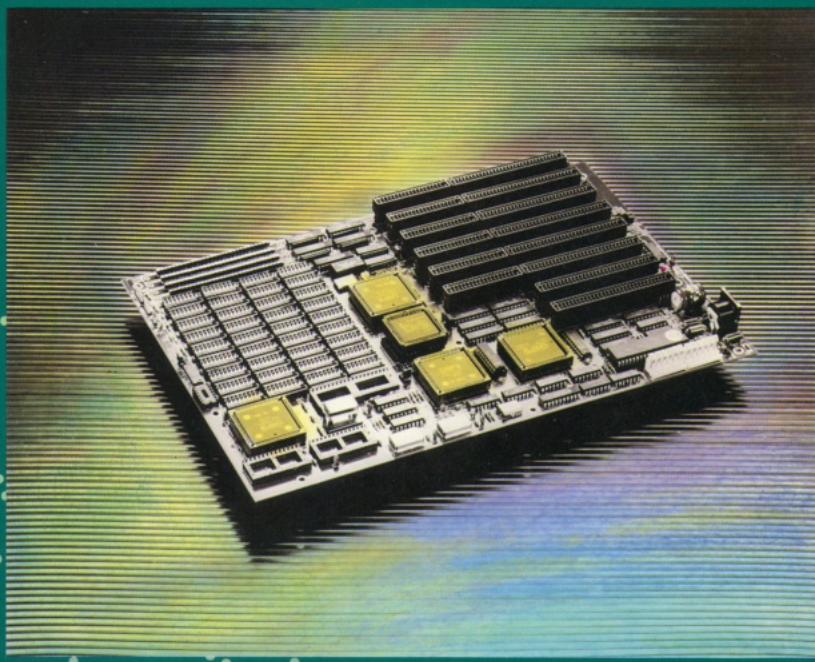
N286 Motherboard User's Manual



CONTENTS

FIGURES

TABLES

CHAPTER 1 INTRODUCTION

Congratulations on the purchase of your new N286 Main Board.

The N286 Main Board which you received has passed strict quality control procedures to ensure trouble-free operation. It is fully compatible with IBM AT computers. We are confident that you will be completely satisfied with it's high speed performances, capabilities and operation.

The operation manual has simple instructions for the installation and operation of the main board.

CHAPTER 2 FEATURE

- 80286 CPU
- INTEL 80287 MATH COPROCESSOR SOCKET
- RAM SIZE, CPU SPEED, I/O SPEED, SHADOW ROM, SHADOW VIDEO BIOS ARE ADJUSTABLE BY ON BOARD BIOS
- SYSTEM CAN BE STARTED BY 256K DRAM, 1M DRAM OR 1M SIMM RESPECTIVELY
- PAGE/INTERLEAVE MEMORY CONTROLLER
- MEMORY UP TO 8M BYTES WITH PARITY ON BOARD
- SUPPORT LIM-EMS 4.0
- CPU SPEED IS SWITCHABLE BY HARDWARE/SOFTWARE
- REAL-TIME CLOCK/CALENDER WITH BATTERY-BACKED UP TO CMOS MEMORY FOR SYSTEM CONFIGURATION DATA
- OFF BOARD BATTERY CONNECTION BUILD IN
- PROVIDE KEYLOCK INTERFACE
- 7-CHANNEL DMA
- 16 LEVEL INTERRUPTS
- ON BOARD POWER GOOD SIGNAL BUILD IN

CHAPTER 3 INSTALLATION

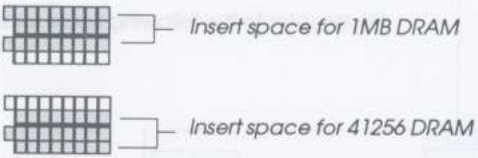
3-1 RAM INSTALLATION

The N286 motherboard can be expanded memory from 1MB to 2, 4, 6 or 8 MB. Either 256K x 1 or 1MB x 1 DRAM can be used on the N286 motherboard.

DRAM socket on the motherboard consists of 16 and 18 pin dip sockets. Plug 41256 DRAM in 16 pin socket or plug 1MB DRAM in 18 pin socket.

Here is a drawing for your reference:

◆ *FIGURE 3.1*
16/18 PIN
DRAM SOCKET

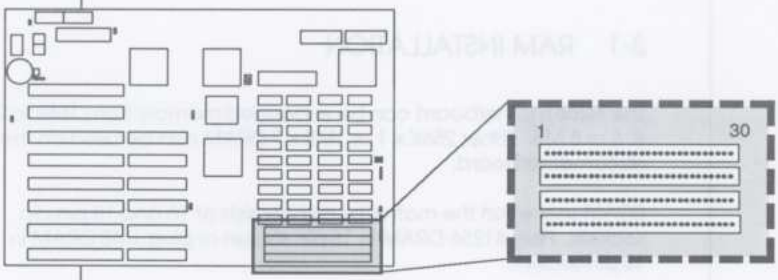


DRAM on the motherboard consists of BANK 0 and BANK 1. Each BANK has 18 pcs of DRAM. When you install the DRAM on the motherboard, first completely fill BANK 0, then fill BANK 1. The spaces of BANK 0 should be fully occupied, otherwise the motherboard will not work.

These are SIMM module RAM on the BANK 0/2 and BANK 1/3 which is a 30 pin SIP socket.

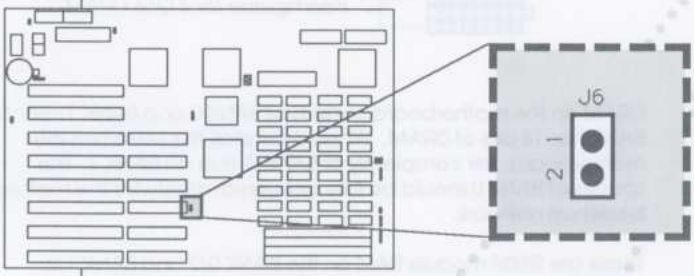
Please refer to the figure 3.2 for the Bank 0/2 and Bank 1/3 positions .

◆ *FIGURE 3.2*
THE ON BOARD
DRAM POSITION



Please refer to the following figure for setting up the Jumper J6.

◆ *FIGURE 3.3*
THE ON BOARD
J6 POSITION



For RAM installation, please refer to the following table:

◆ *TABLE 3.1 RAM SIZE SELECTION*

RAM SIZE SELECTION

J6	BANK0	BANK1	BANK0/2	BANK0/3	RAM SPACE
SHORT	N.U.	N.U.	41256	NONE	512 KB
SHORT	N.U.	N.U.	41256	41256	1MB
SHORT	N.U.	N.U.	411000	NONE	2MB
SHORT	N.U.	N.U.	411000	411000	4MB
		DIP ONLY		SIM ONLY	

J6	RAM BANK0	RAM BANK1	RAM BANK0/2	RAM BANK1/3	RAM SPACE
OPEN	41256 X 18	NONE	NONE	NONE	512KB
OPEN	41256 X 18	41256 X 18	NONE	NONE	1MB
OPEN	41256 X 18	41256 X 18	41256	NONE	1536KB
OPEN	41256 X 18	41256 X 18	41256	41256	2MB
OPEN	411000 X 18	NONE	NONE	NONE	2MB
OPEN	411000 X 18	411000 X 18	NONE	NONE	4MB
OPEN	411000 X 18	411000 X 18	411000	NONE	6MB
OPEN	411000 X 18	411000 X 18	411000	411000	8MB

Jumper J6 is used for Bank Selection. When Jumper J6 is open, the Bank 0, 1, 0/2 and 1/3 can be used as an individual Bank. When Jumper J6 is short, Bank 0/2 and Bank 1/3 will be acted as Bank 0 and Bank 1.

DRAMs can be installed either on the Bank 0 and Bank 1 or Bank 0/2 and Bank 1/3.

NOTE: *DRAM can not be installed on the Bank 0, 1, 2, 3 when Jumper J6 is short. Otherwise, the DRAM memory will be wasted.*
Normally, when you use SIMM module RAM, the Jumper J6 is short.

3-2 ROM INSTALLATION

Motherboard consists of U40 (even) and U39 (odd) sockets. Both sockets have 28 pins. 16 bits PC/AT contains 2 pcs of BIOS.
Insert these 2 BIOS in U40 and U39. U40 for even byte or low byte. U39 for odd byte or high byte.
Jumper J5 on the motherboard is used to select the ROM BIOS size.

Refer to the following table for ROM istallation:

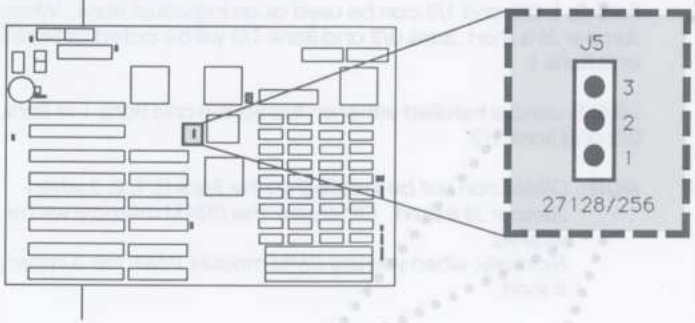
◆ *TABLE 3.2 ROM INSTALLATION*

JUMPER	MEANING	SETTING	USAGE
J5	ROM SIZE	1.2 PIN SHORT	32KB ROM SIZE (27128 X 2)
		2.3 PIN SHORT	64KB ROM SIZE (27256 X 2)

You can choose AMI, PHOENIX or AWARD BIOS for ROM Installation.

Please refer to the following figure for setting up the Jumper J5:

◆ *FIGURE 3.4 THE ON BOARD J5 POSITION*



3-3 CO-PROCESSOR (80287) INSTALLATION

If you intend to increase the co-processor speed in CAD/CAE software, then plug a 80287 into U38 - a 40 pin socket on the motherboard.

To select a proper co-processor, please consider:

Jumper J3 set up

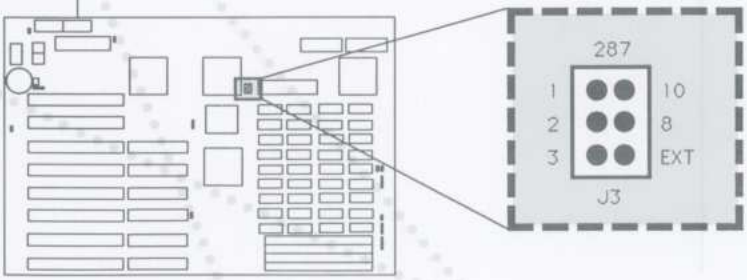
◆ *TABLE 3.3 JUMPER J3 SET UP*

POSITION	SETTING	USAGE
PIN 1	SHORT	80287-10 REQUIRED
PIN 2	SHORT	80287-6 REQUIRED
PIN 3	SHORT	EXT

If pin 1 is short, a 80287-10 is required. If pin 2 is short, a 80287-8 is required. If pin 3 is short, an external Oscillator will be added on the OSC3 to meet with your requirement. The default is 36MHz. The frequency is divided by 3, then go to the 80287's CLK pin. You should use a faster co-processor to assure the right performance.

Please refer to the following figure for setting up the Jumper J3.

◆ *FIGURE 3.5 THE ON BOARD J3 POSITION*



The math coprocessor located at U38 is optional. When a 80287 coprocessor is installed, the BIOS will check its presence automatically. Setting any switch to indicate its presence is unnecessary.

If you install a coprocessor, be certain that it is the correct one for the clock speed in which you intend to do your processing. Consult the vendor from whom you purchase the chip if you are in doubt as to which one to choose.

3-4 DISPLAY ADAPTER SET UP

The Jumper J1 is used to set the display function only. The pin 1 and pin 2 are closed when the monochrome display card is installed. The pin 2 and pin 3 are closed when the color display card is installed.

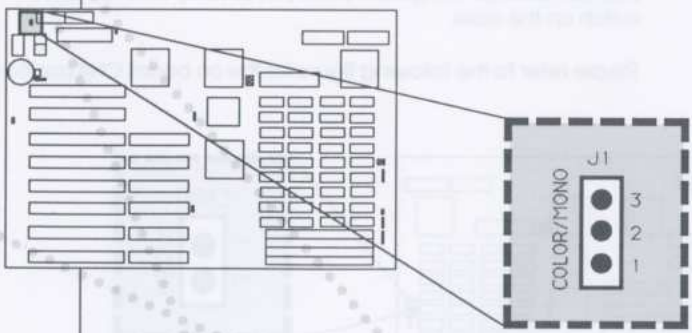
Please refer to the table below for setting up the Jumper J1.

◆ *TABLE 3.4*
JUMPER J1 SET UP

JUMPER	MEANING	SETTING	USAGE
J1	DISPLAY TYPE	PIN 1.2 SHORT	MONOCHROME DISPLAY
		PIN 2.3 SHORT	COLOR DISPLAY

Please refer to the following figure for setting up the Jumper J1:

◆ *FIGURE 3.6*
THE ON BOARD J1 POSITION



3-5 CONNECTOR FUNCTIONS

TURBO SWITCH CONNECTOR

CN4 is a turbo switch connector which is used to select the system board's system clock.

When CN4 is short and it's on the turbo mode, then the system clock is 20 MHz.

When CN4 is open and it's on the normal mode, then the system clock is 16 MHz.

The turbo switch connector pin assignments are as follow:

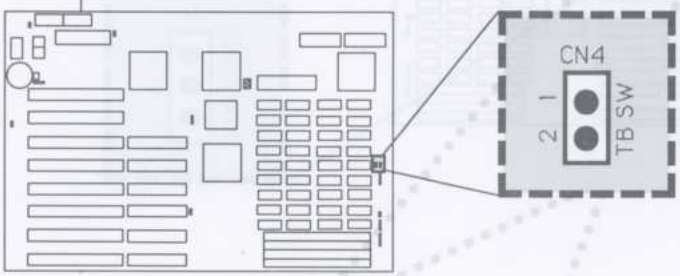
◆ *TABLE 3.5 CN4 ASSIGNMENTS*

CONNECTOR	USAGE	PIN	DESCRIPTION
CN4	turbo sw	1	select pin (0=20MHz)
		2	GROUND

If you connect the turbo switch cable on the case with CN4 then you can change the system clock (16/20 MHz) with the turbo switch on the case.

◆ *FIGURE 3.7 THE ON BOARD CN4 POSITION*

Please refer to the following figure for the on board CN4 position:



TURBO LED CONNECTOR

CN3 is a turbo LED connector used to connect the case turbo LED cable.

If system board select is in turbo mode, then the turbo LED will be lit up.

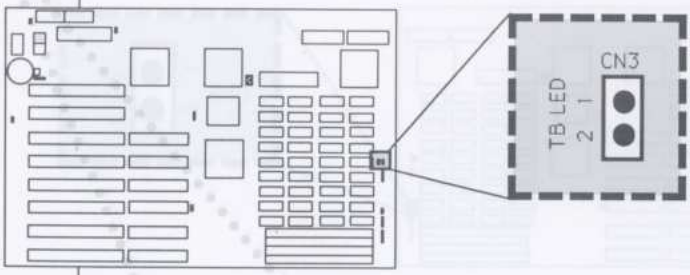
Pin assignment state as follow:

◆ *TABLE 3.4*
CN3 ASSIGNMENTS

CONNECTOR	USAGE	PIN	DESCRIPTION
CN3	turbo LED	2	+ anode
		1	- cathode

◆ *FIGURE 3.8*
THE ON BOARD
CN3 POSITION

Please refer to the following figure for setting up the Jumper CN3:



RESET SWITCH CONNECTOR

CN6 is a RESET switch connector, used to restart the system. You can connect the RESET switch cable on the case with CN6. When you press the RESET bottom on the case, the system will re-start the computer from the Ram test stage. This is a hardware RESET step similar to the power-on function.

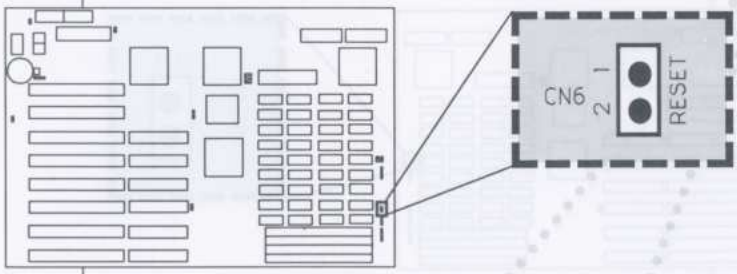
Pin assignment state as follow:

◆ *TABLE 3.7 CN6 ASSIGNMENT*

CONNECTOR	USAGE	PIN	DESCRIPTION
CN6	Reset sw	1	Reset in
	Reset	2	GROUND

◆ *FIGURE 3.9 THE ON BOARD CN6 POSITION*

Please refer to the following figure for setting up the Jumper CN6:



SPEAKER CONNECTOR

CN7 is used to connect speaker.

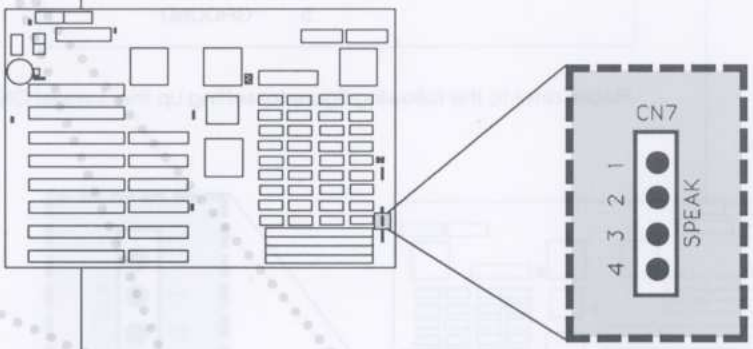
Pin assignment state as follow:

◆ *TABLE 3.8 CN7 ASSIGNMENT*

CONNECTOR	USAGE	PIN	DESCRIPTIN
CN7	speaker	1	date out
		2	not used
		3	GROUND
		4	+ 5V

◆ *FIGURE 3.10 THE ON BOARD CN7 POSITION*

Please refer to the following figure for setting up the Jumper CN7:



KEYLOCK & POWER LED CONNECTOR

CN8 is a keylock connector used to enable or disable keyboard and to move power-LED on the case.

If you connect the key-lock and power-LED cable to CN8, the case's power-LED will be lit up display the power-on state. You can also use the keyboard-lock on the case to enable or disable the keyboard.

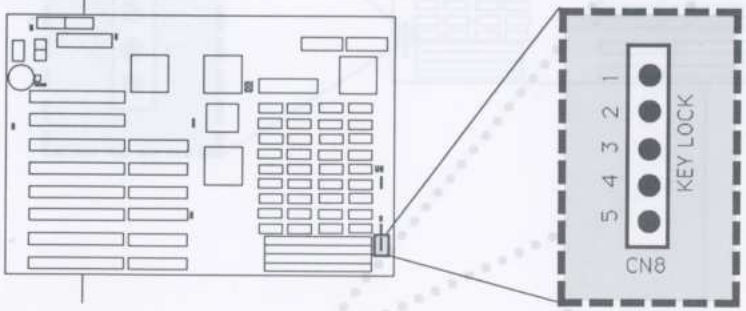
Pin assignment state is as follow:

◆ *TABLE 3.9 CN8 ASSIGNMENT*

CONNECTOR	USAGE	PIN	DESCRIPTION
CN8	keylock	1	LED power
		2	not used
		3	GROUND
		4	keyboard inhibiter
		5	GROUND

Please refer to the following figure for setting up the Jumper CN8:

◆ *FIGURE 3.11 THE ON BOARD CN8 POSITION*



EXTERNAL BATTERY

There is an on-board battery on the system board. You can also use external battery to connect with CN2 instead of using on-board battery.

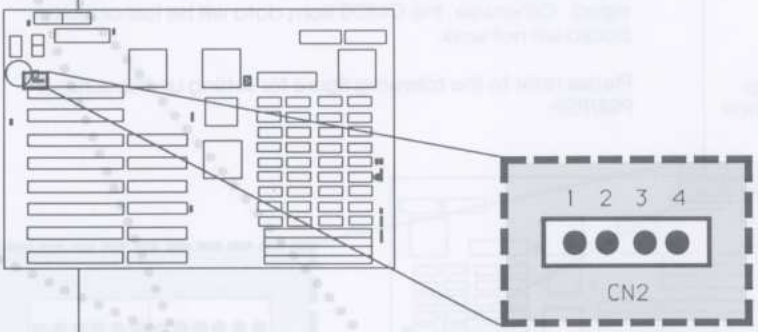
Pin assignments state as follow:

TABLE 3.10 CN2 ASSIGNMENT

PIN	DESCRIPTION
1	battery (+)
2	not used
3	GROUND
4	GROUND

Please refer to the following figure for setting up the Jumper CN2:

FIGURE 3.12 THE ON BOARD CN2 POSITION



POWER SUPPLY CONNECTOR

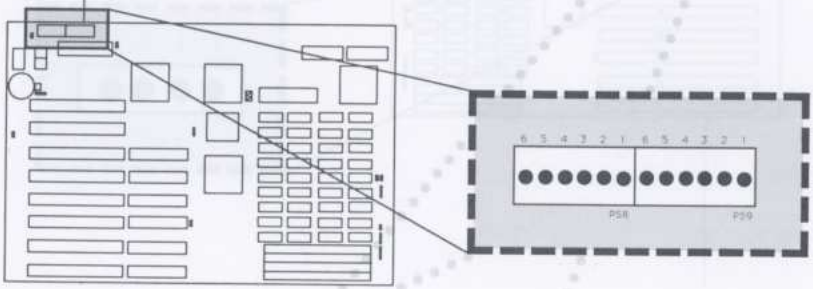
◆ *TABLE 3.11 PS8/PS9 ASSIGNMENT*

CONNECTOR	PIN	DESCRIPTION
PS9	1	+5v dc
PS9	2	+5v dc
PS9	3	+5v dc
PS9	4	-5v dc
PS9	5	GROUND
PS9	6	GROUND
PS8	1	GROUND
PS8	2	GROUND
PS8	3	-12v dc
PS8	4	+12v dc
PS8	5	+5v dc
PS8	6	power good

Both PS9 and PS8 are used to connect power supply. It is very important to select a power supply which provides a power on signal. Otherwise, the CMOS Ram data will be lost or system board will not work.

◆ *FIGURE 3.13 THE ON BOARD PS8/PS9 POSITION*

Please refer to the following figure for setting up the Jumper PS8/PS9:



KEYBOARD CONNECTOR

CN1 is a 5 pins, 90-degree pcb din connector which is used to connect with keyboard.

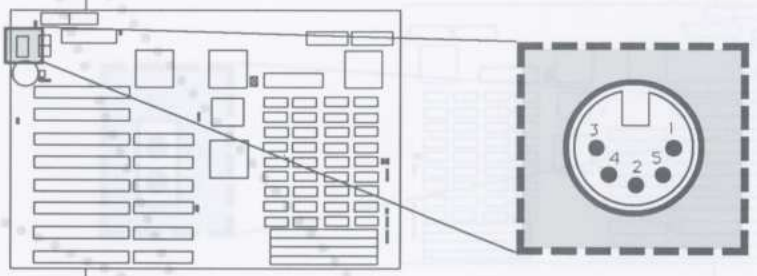
Pin assignments state as follow:

TABLE 3.12 CN1 ASSIGNMENT

PIN	DESCRIPTION
1	keyboard clock
2	keyboard data
3	spare
4	GROUND
5	+5v dc

Please refer to the following figure for setting up the Jumper CN1:

FIGURE 3.14 THE ON BOARD CN1 POSITION



BATTERY DISCHARGE CONNECTOR

If you have taken a wrong procedure to set up the internal register of the chip set, then it probably doesn't work. To solve this problem, we suggest you to turn off the Power Supply first, then short the Jumper J4 for discharging the CMOS Status. After a few seconds, you can turn on the power and restart the set-up procedure.

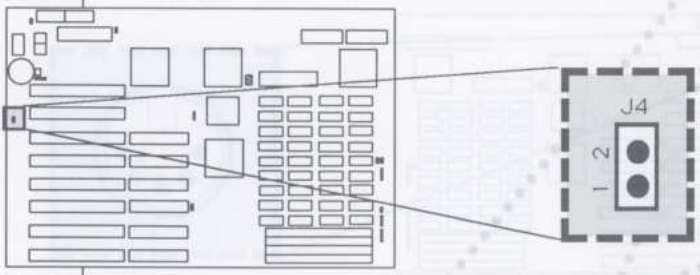
◆ *TABLE 3.13*
J4 SET UP

JUMPER	MEANING	SETTING	USAGE
J4	DISCHARGE BATTERY	SHORT	CMOS RECONFIGURATION

NOTE: For the setting up details, we will describe on thefollow ing chapter.

Please refer to the following figure for setting up the Jumper J4:

◆ *FIGURE 3.15*
THE ON BOARD J4 POSITION



CHAPTER 4 OPERATION

Now, you have properly installed the N286 Motherboard. You can trun the computer power on and start to run the set up program.

AMI, PHOENIX and AWARD BIOS are the three compatible BIOS which can be used to operate system.

NOTE: If the system memory is very large, you can bypass the memory test by pressing the <ESC> key when the system is booting.

4-1 SOFTWARE CONFIGULATION SETUP AMI BIOS AND EMS SETUP

The main purpose of this TEXT is to explain how to use NEAT CHIPS SET and EMS setup under the AMI BIOS.

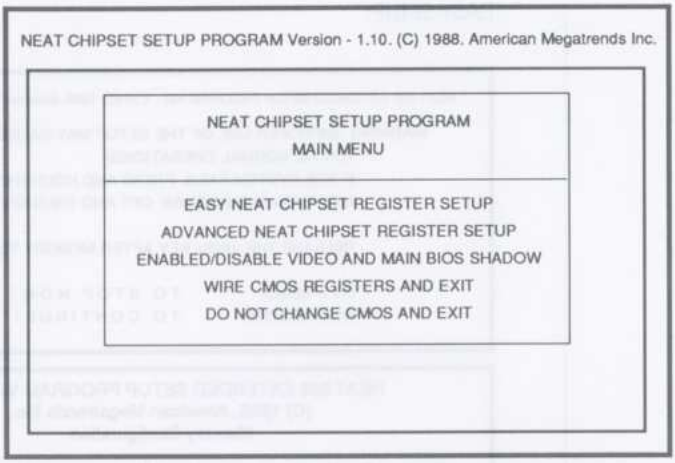
After you power on and finish the memory test, please press "DEL" key, the program will go on to next screen.

Press <DEL> key to run SETUP EXTD-SET

AMI BIOS NEAT REGISTER SETUP:

```
Entering SYSTEM SETUP due to user request
Want to run SETUP/EXTD-SET (Y/N)? Y
SETUP/EXTD-SET (1/2)? 2
```

NOTE: If you choose 1, the program will go into the system installation, yet, we want to install NEAT CHIPS DATA now, so please choose 2, and the program will into the "NEAT CHIPSET SETUP MAIN MANU".



NOTE: There are two methods about the SETUP of AMI'S NEAT Register. One is EASY SETUP to help the user to set up the sytem in high-speed, and the other is ADVANCED SETUP to help user to have more detailed operation.

Please push the " ↑ ↓" and "Enter" keys to enter EASY SETUP.

EASY SETUP:

NEAT 286 EXTENDED SETUP PROGRAM Ver - 1.10 (C) 1988. American Megatrends Inc.

WARNING -IMPROPER USE OF THE SETUP MAY CAUSE THE SYTEM
TO FAIL NORMAL OPERATIONS!
IF THE SYSTEM FAILS. PRESS AND HOLD THE <INS> KEY.
AND TURN THE MACHINE OFF AND THEN ON!

RELEASE THE <INS> KEY AFTER MEMORY TEST STARTS!

HIT <ESC> TO STOP NOW!
HIT <ENTER> TO CONTINUE!

NEAT 286 EXTENDED SETUP PROGRAM Ver - 1.10
(C) 1988, American Megatrends Inc.
Memory Configuration

Bank	Enabled/Disabled	DRAM Type	Waitstate
0	ENABLED	256K	0 WAIT STATE
1	ENABLED	256K	0 WAIT STATE
2	DISABLED		0 WAIT STATE
3	DISABLED		0 WAIT STATE

Clock Sources Selected

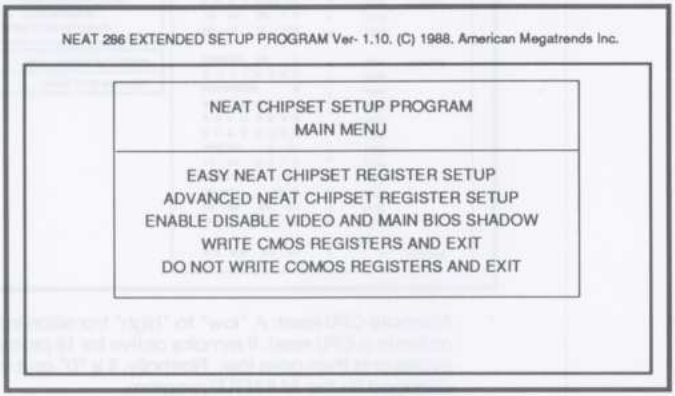
Processor Clock	Bus Clock	DMA clock
CLK2IN	CLK2IN/2	SCLK/2

Shadow RAM/Interleave

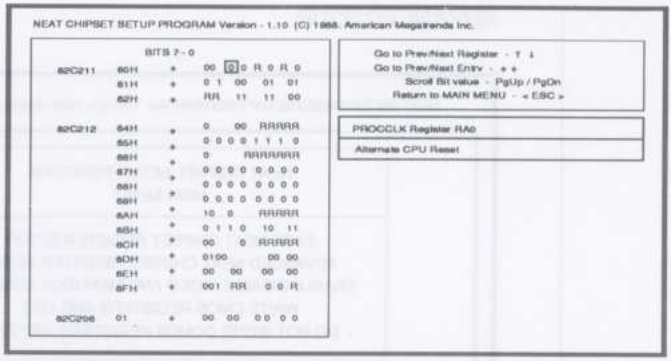
BIOS Shadow F0000H, 64K	C0000H, 16K	Video Shadow C4000H, 16K	Interleave
DISABLED	DISABLED	DISABLED	ENABLED

NOTE: (1) Use SHADOW with 1024K on board.
(2) 0 wait state needs 2 bank memory.
(3) With BUS CLOCK, please choose CLK2IN/2 otherwise the pheripheral interface cards can not keep up with the speed.

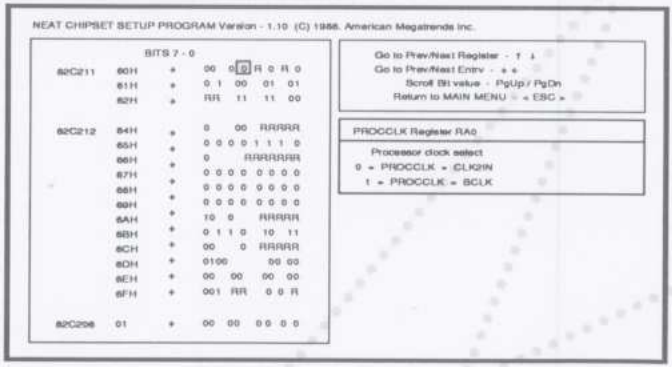
ADVANCED SETUP:



NOTE: This SETUP provide you with more details about operation, and it contains EMS function, etc.

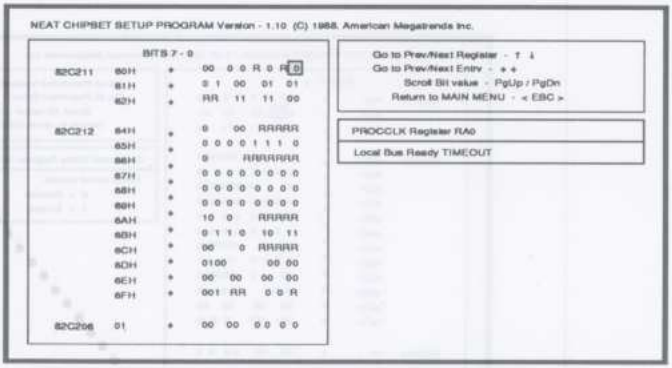


- Alternate CPU reset: A "low" to "high" transition in this bit will activate a CPU reset. It remains active for 16 processor clock cycles and then goes low. Normally, it is "0" and can not be changed by the AMI SETUP program.
- "R" means Reserved.
- The BIT's value can not be charged.

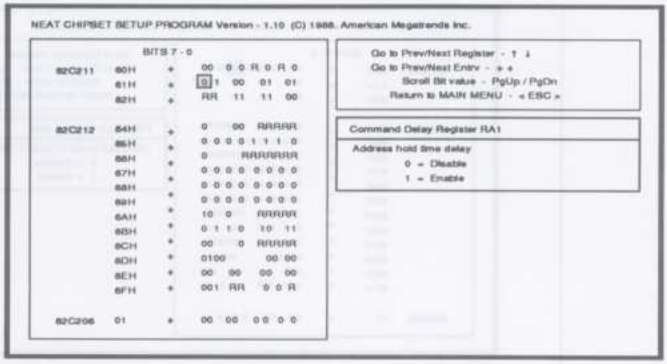


If "1", the 286 CPU-CLOCK will be half CLK2IN. For example, 16MHz will become 8MHz.
If "0", the 286 CPU-CLOCK will be one CLK2IN. For example, 16MHz will still be 16MHz.

"1" enable the NM1, and "0" disables it. Default is "0".

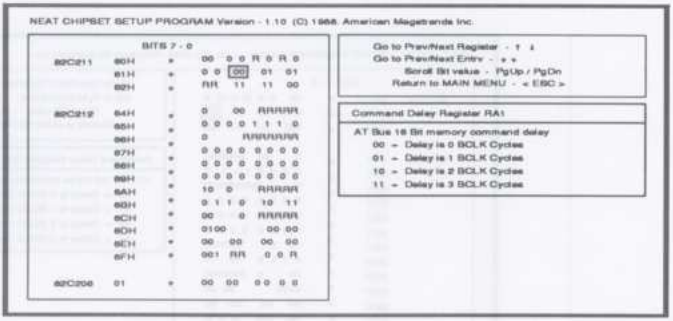


"1" indicates "READY TIMEOUT HAS OCCURED 128 286-CPU-CLOCK."
"0" indicates "READY TIMEOUT HAS NOT OCCURED".
Default is "0".

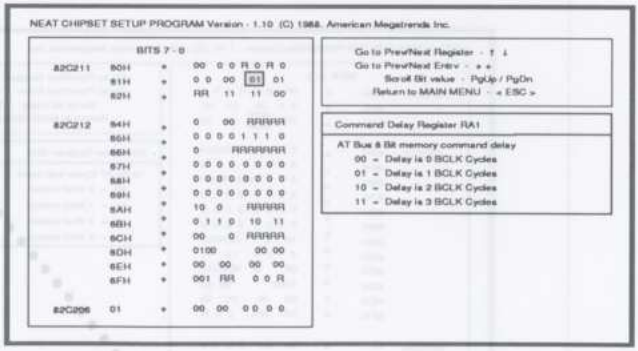


* Address hold time delay: "1" enables extra address bus hold time and "0" disables it. Default is "0".

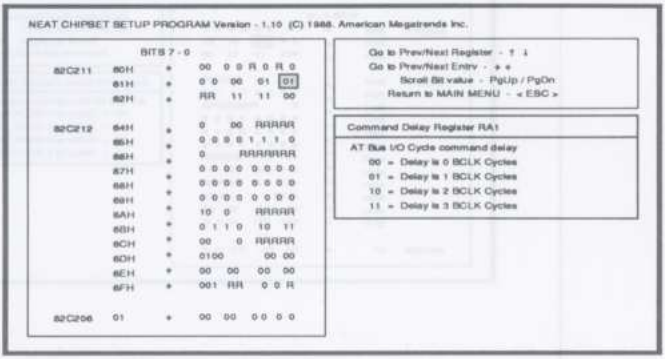
* Quick mode enable: "0" enables quick mode, and "1" disables it. Default is "1".



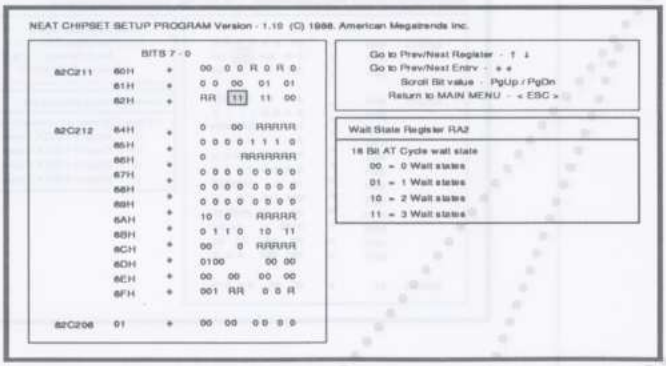
* AT BUS 16 bit memory command delay. Specifies between 0 to 3 BCLK cycle command delays for 16 bit AT MemoryCycles. Default is "00".



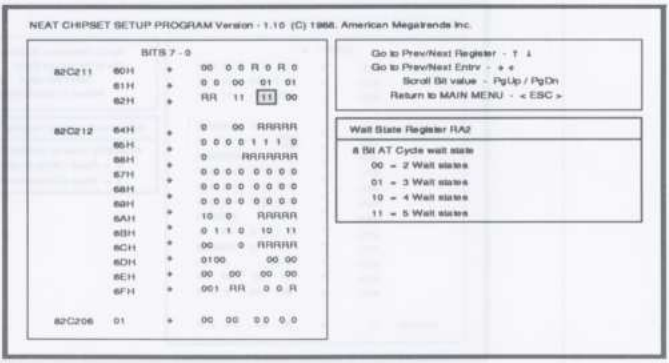
* AT BUS 8 bit memory command delay. Specifies between 0to 3 BCLK cycle command delays for 8 bit AT Memory Cycles. Default is "01".



* AT BUS I/O cycle command delay. Specifies between 0 to 3 BCLK cycles command delays for AT I/O cycles. Default is "01".

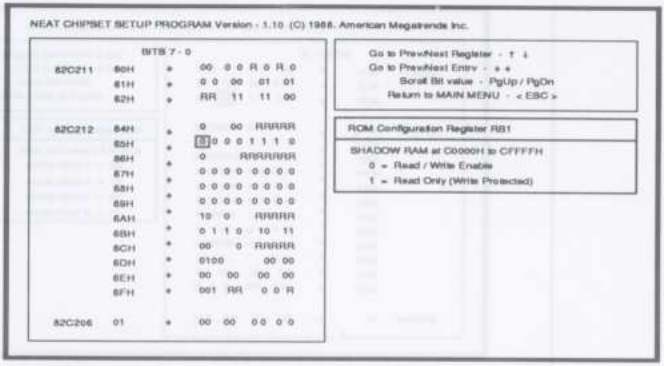


* 16 bit AT cycle wait state generation. Default is "11".



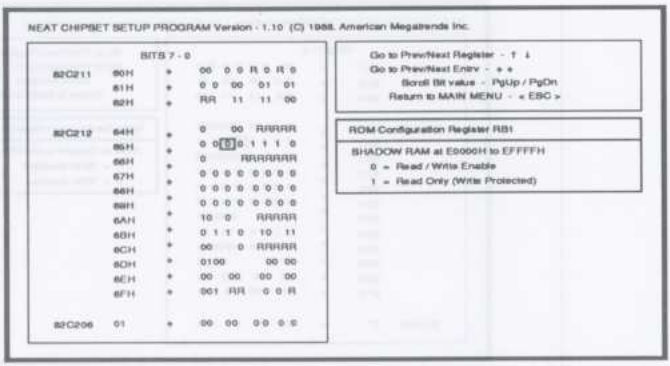
* 8 bit AT cycle wait state generation. Default is "11".

* BUS clock (BCLK) source select. Default is "00".
* When in 20 Mhz turbo mode, we suggest you to choice "10" as bus clock.

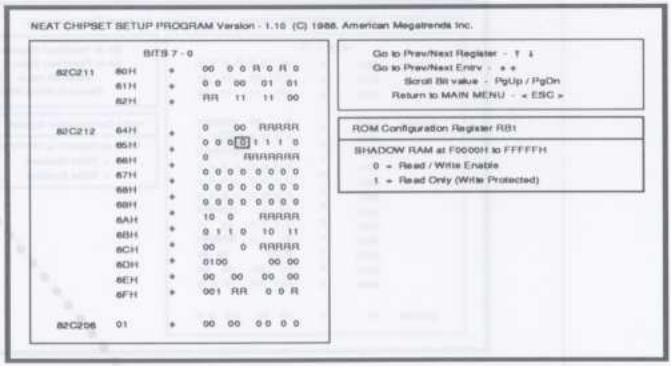


* Normally is "0".

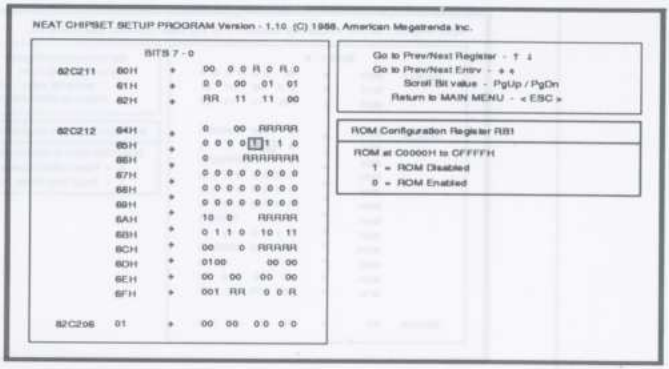
* Normally is "0".



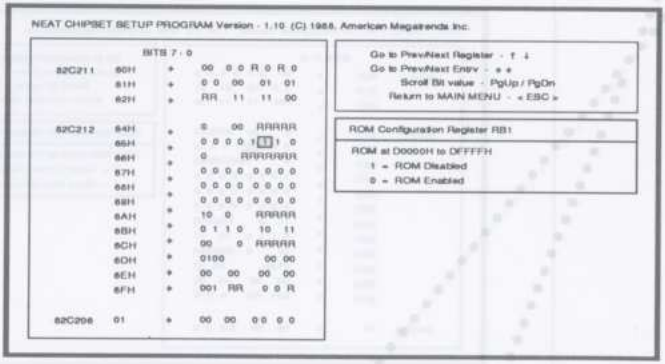
* Normally is "0".



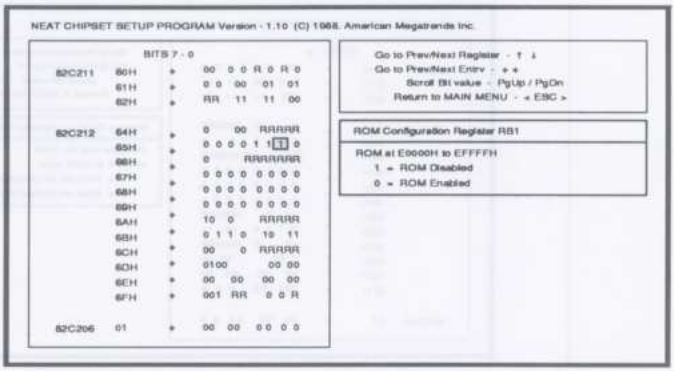
* Normally is "0".



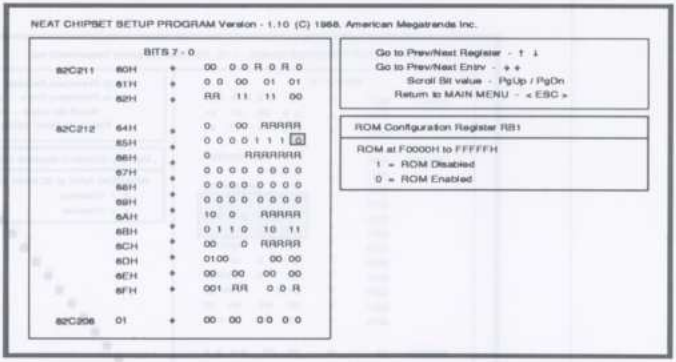
* Normally is "1".



* Normally is "1".

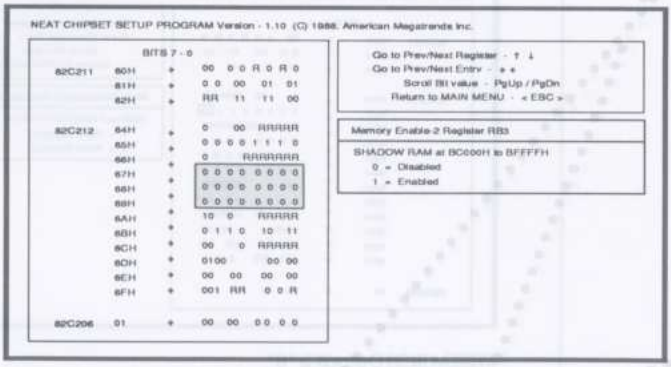


* Normally is "1".

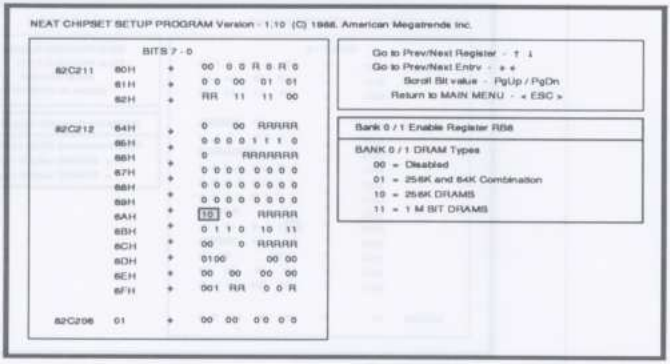


SYSTEM BIOS Default is "0".

* 512K to 640K area select "0" MEANS Address in the I/O channel "1" MEANS Address on system board. Default is "1".

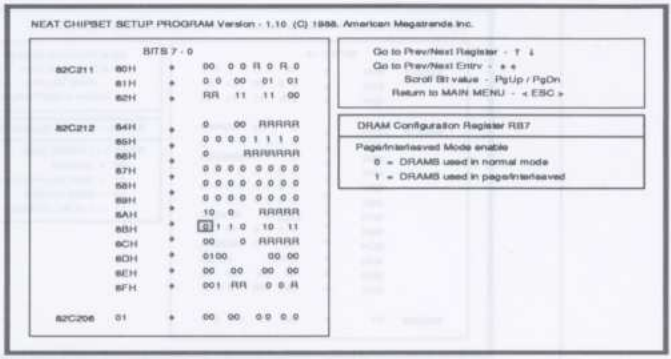


All of the SHADOW RAM ARRAY Default is "0".

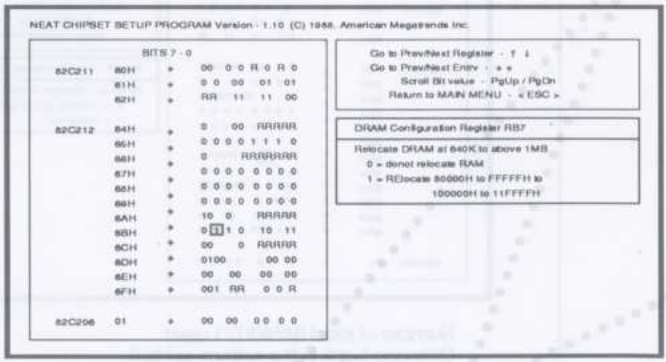


* These bits contain the information for the DRAM types used on the system board. Default is "10" 256K DRAMS.

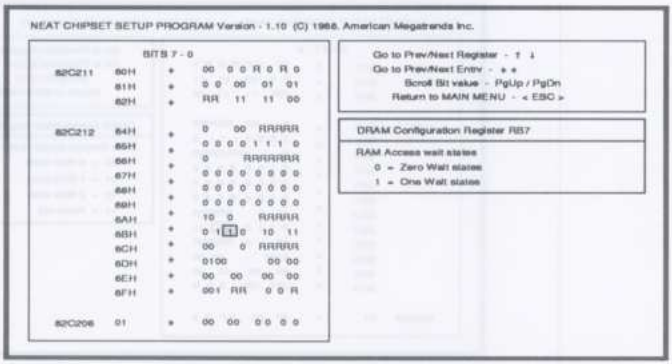
* Number of local BANKS 0/1 used:
Only one bank in the system: set to 0
Two banks in the system: set to 1.



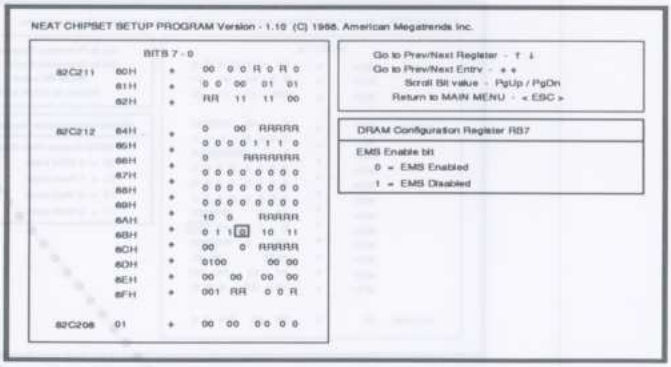
* "0" disables the page/interleaves mode, allowing usage of normal mode for the DRAMS (Default).
"1" enables PAGE/interleaved mode for the DRAMS. Please also note that there should be at least two BANKS used in the system board.



"0" does not relocate local RAM "1" (Default) relocates local RAM from 080000H - 09FFFFH to 100000H - 11FFFFH.
Provided total local RAM is 1 Mbyte only.

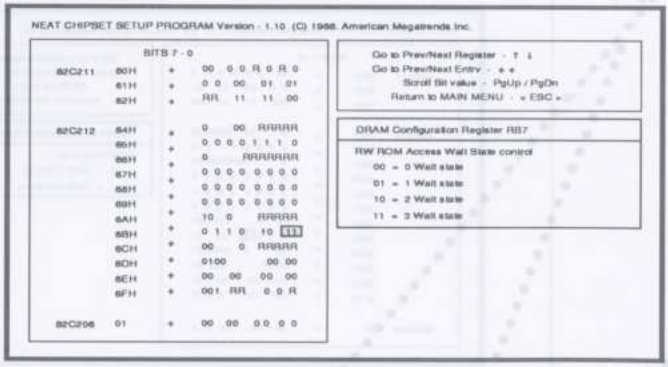


* If set to "0", accesses is 0 wait states.
If set to "1" (Default), accesses will be 1 wait state.



* If set to "0", EMS is disabled (Default).
If set to "1", EMS is enabled.

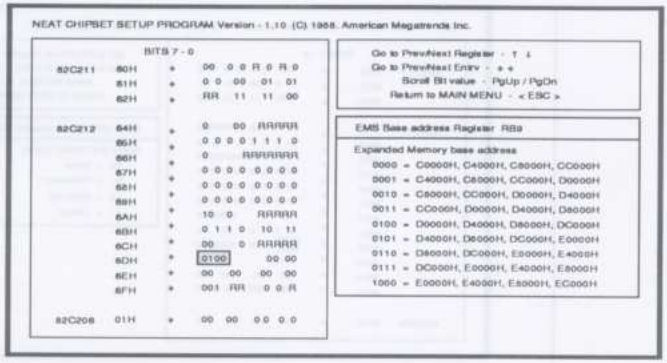
* EMS MEMORY access wait state:
Default is "10".



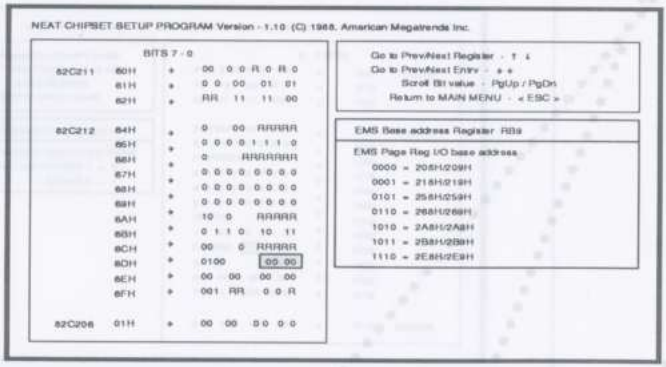
* ROM access wait state:
Default is "11".

* BANK 2 and BANK 3 DRAM TYPES select:
Default is "00".

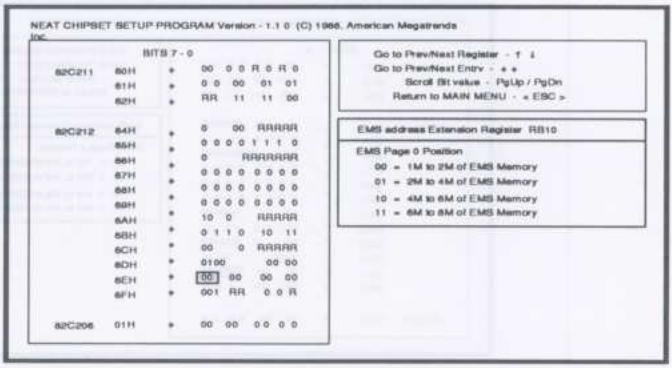
* Number of local BANKS used:
Only one bank in the system set to "0".
Two banks in the system set to "1".



* These bits are used for selecting the expanded memory ← based addresses. Default is "0100".



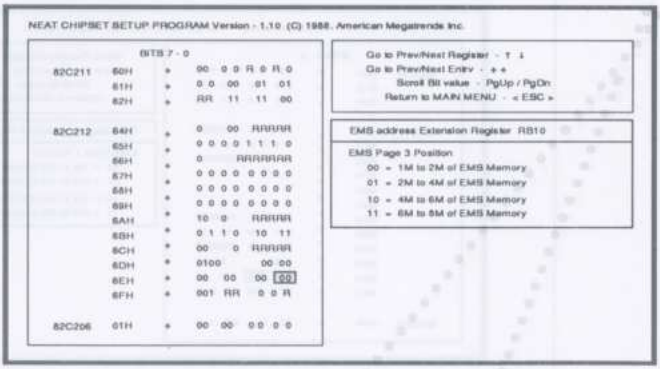
* These bits are used for the EMS page register I/O base ← address. Default is "0000"



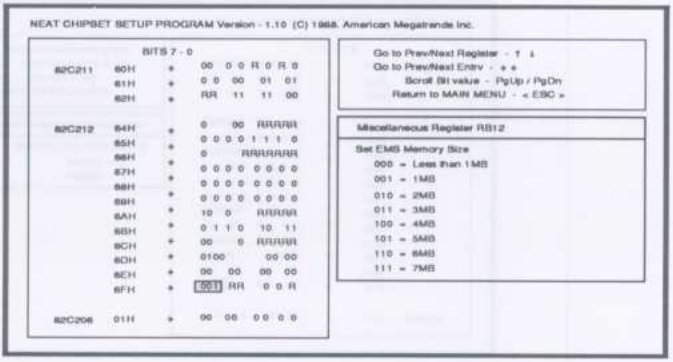
* EMS PAGE 0 address extension bits. Default is "00".

* EMS PAGE 1 address extension bits. Default is "00".

* EMS PAGE 2 address extension bits. Default is "00".

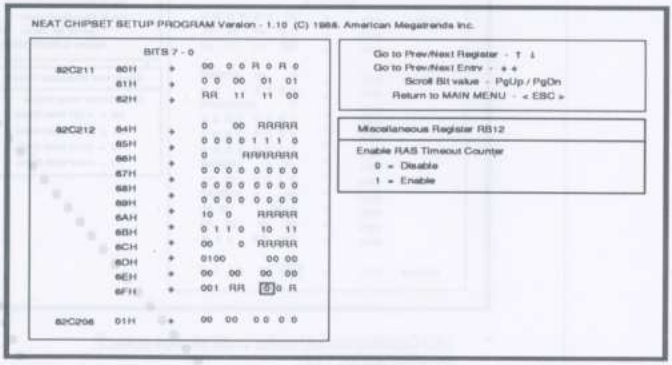


* EMS PAGE 3 address extension bits. Default is "00".



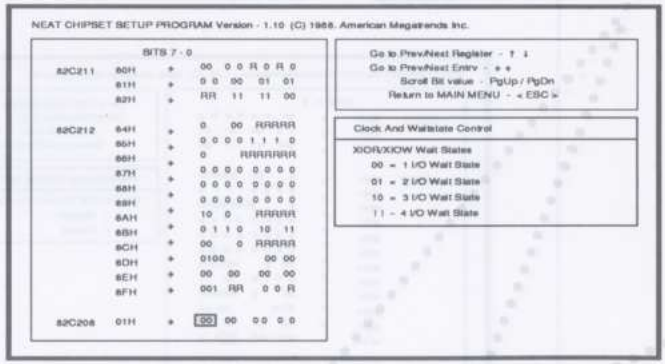
- These bits are used to set the EMS memory space according to the following coding:

000=0.5MB	011=3MB	110=6MB
001=1MB	100=4MB	111=7MB
010=2MB	101=5MB	

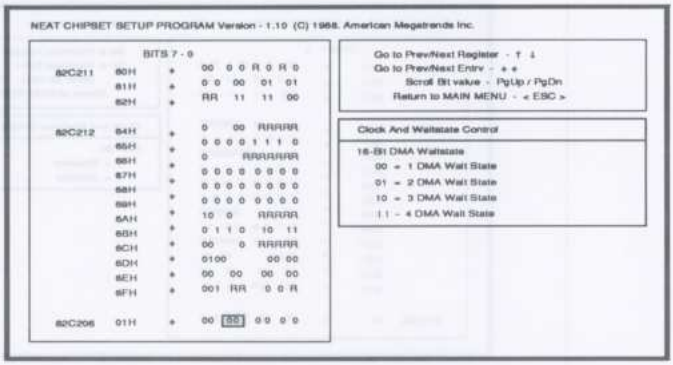


This bit is used to enable the Ras time-out counter for page mode operation. The counter is disabled if set to "0" (Default) and is enabled if set to "1".

* This bit is used for address line A20 control and provides OS/2 optimization while switching the bit defaults to "0" and enables CPUA20 onto A20, if set to "1", it sets A20 = 0.



* I/O Device read/write wait states select:
Please set to "11".



* 16-Bit Direct-Memory-Access waitstate select:
Default is "00".

* 8-Bit Direct-Memory-Access waitstate select:
Default is "00".

* This bit enables extended DMA REAR signal Default is "0".

* DMA CLOCK set:
Default is "0".

AMI BIOS NEAT REGISTER SETUP EXAMPLE

This section is to explain how to change SETUP and make the NEAT CHIPS SET develop to upmost no matter in any kind of DRAM conditions.

NOTE: 1. *If you install only one bank DRAM, please don't use PAGE/INTERLEAVED mode (82C211, 6BH bit 7), and choose 1 wait state.*

2. *If your system has only one bank, please choose "1 WAIT STATE" program.*

3. *If you use EMS function, the system will switch to 1 wait state automatically.*

4. *If you make mistake in SETUP, the system will not be booted. Please use following methods:*

   A. *Turn off the system power first, then close the Jumper J2, after 5 seconds, re-open the Jumper J2. Then power on.*

   B. *Power off first, and press "INS" key in key-board. Then power on. After the monitor displays the screen, release "INS" key, and re-run the SETUP PROGRAM.*

EXAMPLE A : 512K on Board (One Wait States)

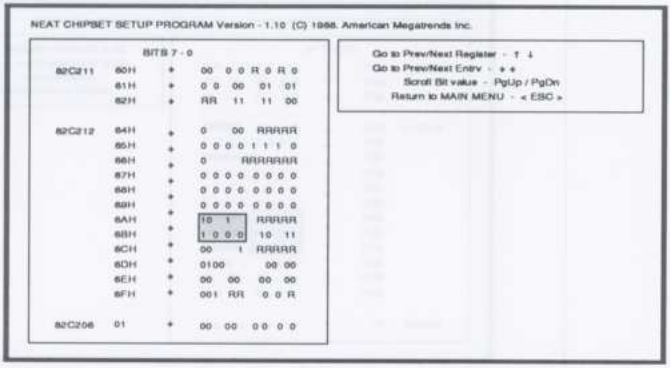
10 0

→ BANK USE 256K DRAM AND ONLY BANK 0 CAN RUN

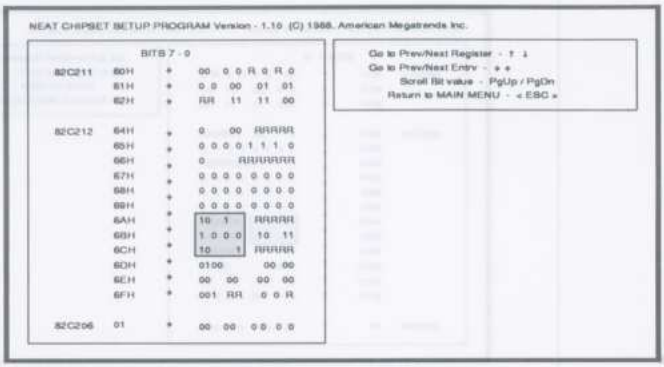
0 1 1 0

- DRAM (NORMAL MODE)
- RELOCATE
- ONE WAIT STATE
- EMS DISABLE

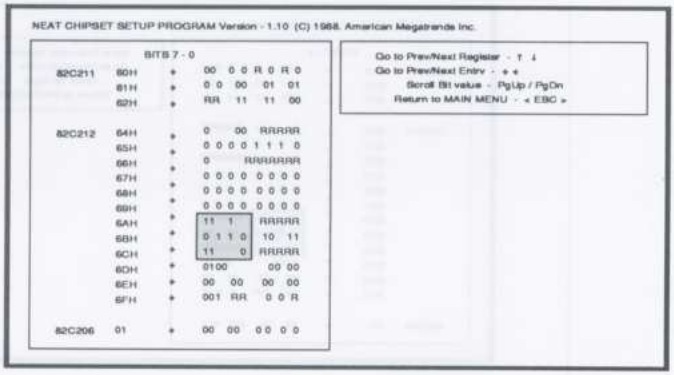
EXAMPLE B : 1024K on Board (Zero Wait States)



EXAMPLE C : 2048K ON BOARD



EXAMPLE D : 6144K ON BOARD



11 1

→ BANK0, BANK1 USE 1MB DRAM

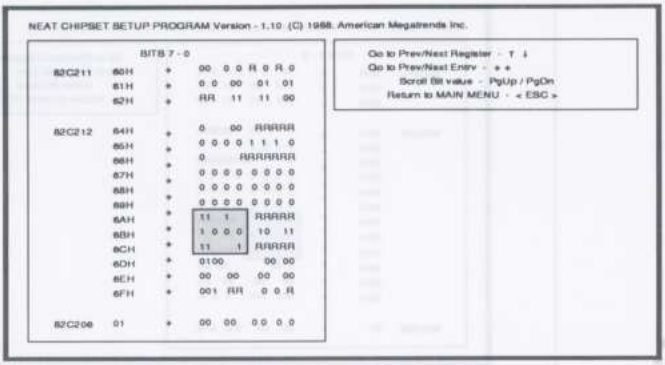
0 1 1 0

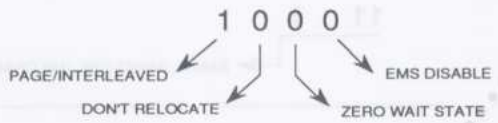
- NORMAL MODE
- RELOCATE
- ONE WAIT STATE
- EMS DISABLE

11 0

→ BANK2 USE 1MB DRAM

EXAMPLE E : 8192K ON BOARD





EMS REGISTER SETUP

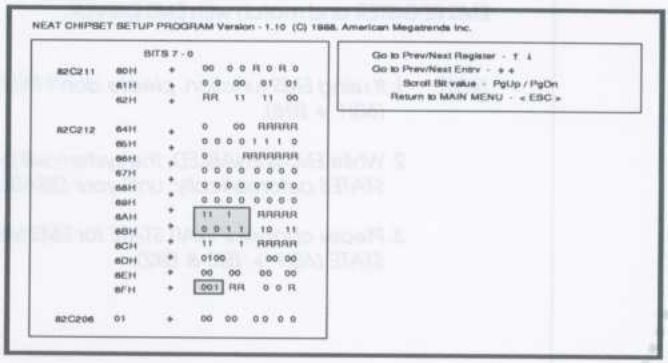
This section is to explain how to use SETUP PROGRAM to set up EMS REGISTER and match with EMS DRIVER.

NOTE: 1. *If using EMS function, please don't RELOCATE RAM (6BH → Bit8).*

2. *While EMS is ENABLED, the system will become 1 WAIT STATES automatically; until your DISABLE it (6BH → Bit4).*

3. *Please choose 2 WAIT STATE for EMS MEMORY WAIT STATE (6BH → Bit3 & Bit2).*

EXAMPLE A : USING 1M DRAM, ONE BANK, 2048K MEMORY, ON BOARD. (1024K USING EMS)



* THE FIRST 1MB IS USED FOR THE SYSTEM. SO EMS MEMORY = ALL MEMORIES - 1MB.

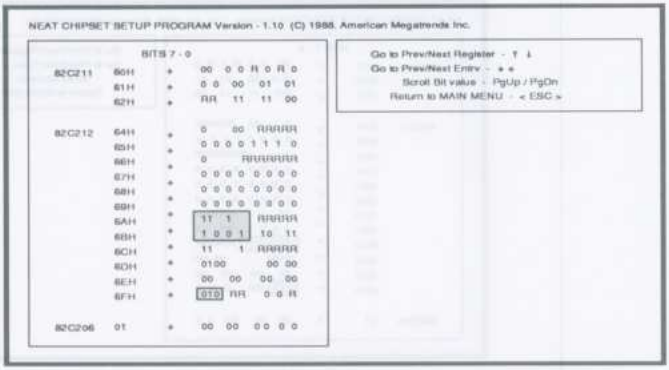
0 0 1 1

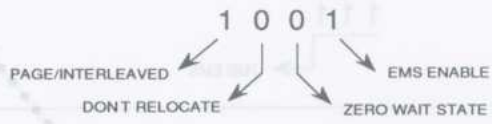
→ EMS ENABLE

0 0 1

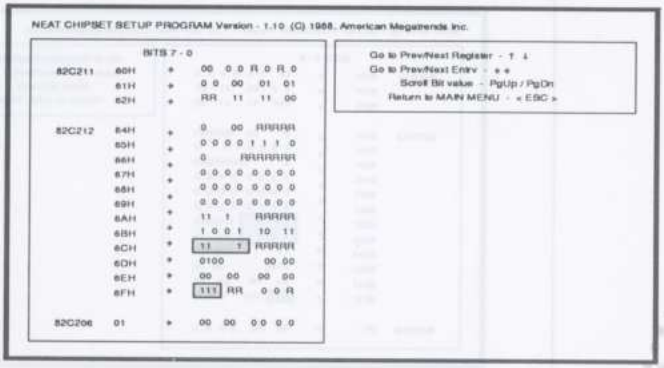
→ EMS 1MB

EXAMPLE B : USING 1M DRAM, TWO BANKS, 4096K MEMORY, ON BOARD. (2048K USING EMS).





EXAMPLE C : USING 1M DRAM, FOUR BANKS, 8192K MEMORY, ON BOARD. (7168K USING EMS).



11 1

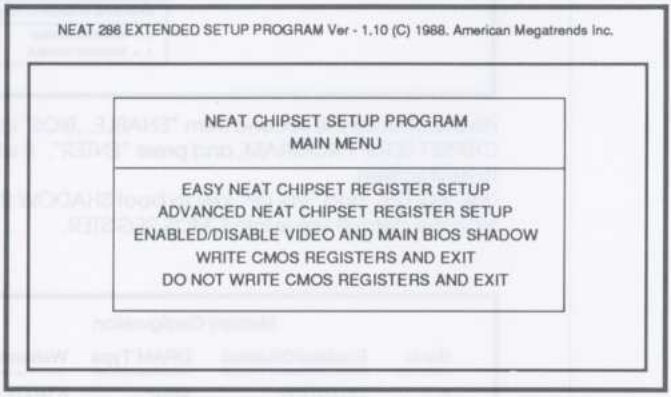
USING 1M DRAM ← → BANK2, BANK3 ENABLE

111

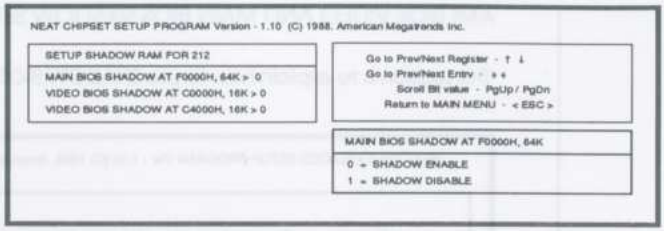
→ 7MB EMS

AMI BIOS VIDEO AND MAIN BIOS SHADOW SETUP

This section is to explain how to use SHADOW BIOS.



NOTE:
1. *At least 1024K memory on board if using SHADOW BIOS.*
2. *Please don't RELOCATE RAM (6BH →Bit7), otherwise, SHADOW will fail.*
3. *If you use VGA or PEGA card, and the BIOS in these cards are using PAGE MODE, please don't use VIDEO-SHADOW in system. Otherwise, the screen can't display.*



Please choose the second item "ENABLE...BIOS" in NEAT CHIPSET SETUP PROGRAM, and press "ENTER". It will go on to next screen.
Use "PG DN" and "PG UP" key to boot SHADOW BIOS, and type the default value into CMOS REGISTER.

Memory Configuration

Bank	Enabled/Disabled	DRAM Type	Waitstate
0	ENABLED	256K	0 WAIT STATE
1	ENABLED	256K	0 WAIT STATE
2	DISABLED		
3	DISABLED		

Clock Sources Selected

Processor Clock	Bus Clock	DMA clock
BUS CLOCK	CLK2IN/2	SCLK/2

Shadow RAM Interleave

BIOS Shadow	Video Shadow		Interleave
F0000H, 64K	C0000H, 16K	C4000H, 16K	
ENABLED	ENABLED	DISABLED	ENABLED

Current date is Mon 9-05-1988
Enter new date (mm-dd-yy):

While booting the system, the screen will list all conditions. Then, you can see whether the SHADOW BIOS is ENABLED or not.

AMI BIOS System Configuration Setup

This section will tell you how to set up the system configuration under the AMI BIOS. After booting the system and testing the memory, please press "DEL" key to go to next screen.

The SETUP program is contained in the sytem's read-only memory. rather than on a diskette.

To enter SETUP, press the "Del" key. The following menu appears:

```
Entering SYSTEM SETUP due to user request
Want to run SETUP/EXTD-SET (Y/N)? Y
SETUP/EXTD-SET (1/2)? 1
```

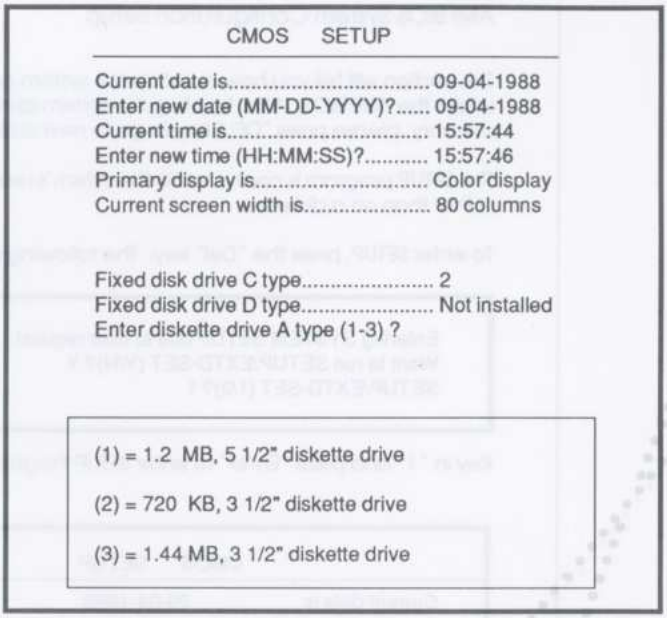
Key in "1" and press "Enter" to enter SETUP Program.

```
                    CMOS    SETUP

Current date is..... 09-04-1988
Enter new date (MM-DD-YYYY)?.....
```

Key in date and or press "Enter" to go on.

```
                    CMOS    SETUP

Current date is..... 09-04-1988
Enter new date (MM-DD-YYYY)?..... 09-04-1988
Current time is.....16:00:36
Enter new time (HH:MM:SS)?.....
```

Key in time and or press "Enter" to go on.



- Primary display is.....Color display" will auto-detected don't need to key in data.
- Fixed disk drive C type.....2": Please refer to AMI Hard Disk Table.
- Enter diskette drive A type (1-3)?: Choose your floppy disk type refer the table.

CMOS SETUP

Current date is	09-04-1988
Enter new date (MM-DD-YYYY)?	09-04-1988
Current time is	15:57:44
Enter new time (HH:MM:SS)?	15:58:12
Primary display is	Color display
Current screen width is	80 columns
Fixed disk drive C type	2
Fixed disk drive D type	Not installed
Enter diskette drive A is	1.2 MB, 5 1/4" drive
Diskette drive B is	Not installed
Base memory size is	640 KB
Expansion memory size is	0 KB
Numeric processor	Absent

Are these options correct (Y/N)?

" Are these options correct (Y/N)?"

If these options correct, please key in "Y", then system will booting.

PHOENIX BIOS AND EMS SETUP

This TEXT is descriptive the setup of NEAT CHIPS SET & SYSTEM at the PHOENIX BIOS.

When you power on, if the system has error, please press F2 key then will enter the system's SETUP program.

```
Phoenix 80286 ROM BIOS PLUS Version 3.10 12
Copyright (C) 1985-1988 Phoenix Technologies Ltd.
All Reghts Reserved

PHOENIX NEAT 286 BIOS

640K Base Memory, 00000K Extended
Invalid configuration information - please run SETUP program
```

Invalid configuration information - please run SETUP program

If these are some errors, this information will appear.

Phoenix 80286 ROM BIOS PLUS Version 3.10 12
Copyright (C) 1985-1988 Phoenix Technologies Ltd.
All Rights Reserved

PHOENIX NEAT 286 BIOS

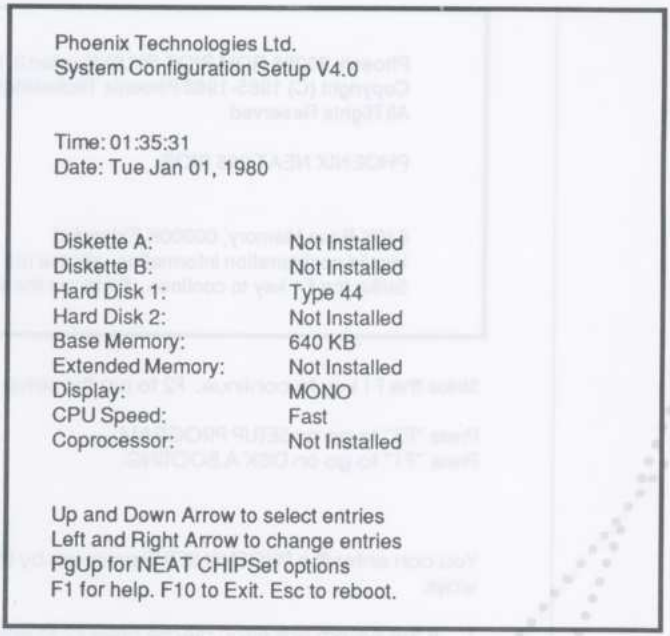
640K Base Memory, 00000K Extended
Invalid configuration information - please run SETUP program
Strike the F1 key to continue. F2 to run the setup utility

Strike the F1 key to continue. F2 to run the setup utility

Press "F2" to go on SETUP PROGRAM.
Press "F1" to go on DISK A BOOTING.

You can enter the PHOENIX SETUP program by the following two ways.

1. If the system has error, please press F2 to enter.
2. When your system has booted, please run SETUP UTILITY.



* Choose Function by ↑ ↓ key.
* Using Pg/Dn change SETUP value.

This setting is used by the power-on self-tests to help your computer identify the type of hard drives you have. If this information is not correct, then your system will not be able to use your hard-disk. The manufacturer of your hard-disk can tell you what type of drive you have. If you have no hard-disk then specify "Not Installed".

Press the <F1> key to see a list of hard-disk drive types, or any other key to return to the main menu.

The following table will be appeared when you press "PgUp" key for optional NEAT CHIPSET.

Phoenix Technologies Ltd.
C&T NEAT CHIPSet Feature Control.

Time: 01:38:06
Date: Tue Jan 01, 1980

Shadow BIOS ROM	Disable	Shadow 16K at EC000:	Disabled
Shadow Video ROM	Disabled	Memory wait States:	0 Wait States
Shadow 16K at C4000	Disabled	ROM Wait States:	3 Wait States
Shadow 16K at C8000	Disabled	640-1024K Relocation:	Disabled
Shadow 16K at CC000	Disabled	EMS Base Memory Address:	Segment C000
Shadow 16K at D0000	Disabled	EMS Base I/O Address:	208h/209h
Shadow 16K at D4000	Disabled	EMS Page 0 Reg Extension:	1M to 2M
Shadow 16K at D8000	Disabled	EMS Page 1 Reg Extension:	4M to 6M
Shadow 16K at DC000	Disabled	EMS Page 2 Reg Extension:	1M to 2M
Shadow 16K at E0000	Disabled	EMS Page 3 Reg Extension:	6M to 8M
Shadow 16K at E4000	Disabled	EMS Memory Sizes:	2.0M
Shadow 16K at E8000	Disabled	EMS Wait States:	0 Wait States
		EMS Memory:	Disabled

Up and Down Arrow to select entries
Left and Right Arrow to change entries
PgUp for standard Setup options

F1 for help. F10 to exit. Esc to reboot.

You can change entries by moving the "LEFT" and "RIGHT" keys.

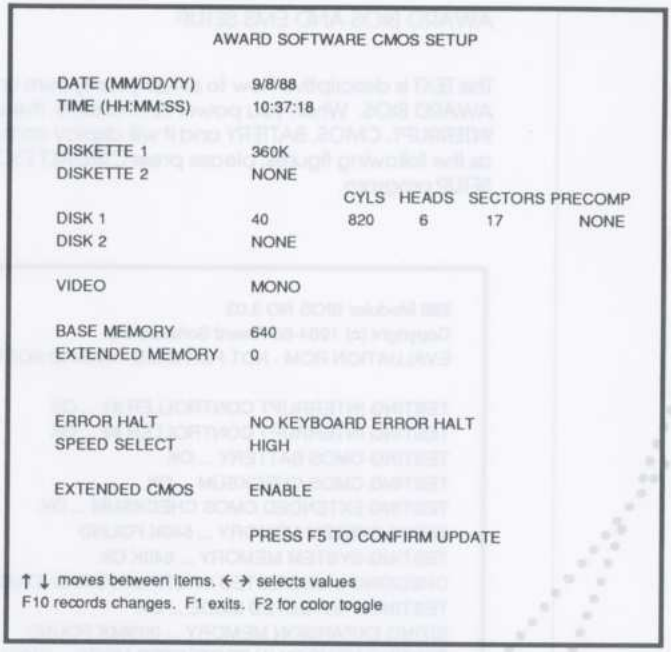
Following is an example for a special utility setup:

Disabled	SHADOW BIOS DISABLE/ENABLE
Disabled	SHADOW VIDEO DISABLE/ENABLE
Disabled	
Disabled	
Disabled	
Disabled	
Disabled	
Disabled	NORMALY SET TO DISABLE
Disabled	
Disabled	
Disabled	
Disabled	
Disabled	NORMALY SET TO DISABLE
0 Wait States	
3 Wait States	NORMALY SET TO 3 WAIT STATES
Disabled	NORMALY DISABLE
Segment C000:	EMS-ADDRESS SEGMENT NORMALY SET TO D000:
208h/209h	EMS I/O Address NORMALY SET TO 208H/209H
1M to 2M	
4M to 6M	
1M to 2M	
6M to 8M	
2.0M	EMS-MEMORY-SIZE
0 Wait States	NORMALY SET TO 2 WAIT STATES
Disabled	

AWARD BIOS AND EMS SETUP

This TEXT is descriptive how to setup your system under the AWARD BIOS. When you power on the BIOS, the system will test INTERRUPT, CMOS, BATTERY and it will display on the screen as the following figures, please press CTRL-ALT ESC key to enter SETUP program.

```
286 Modular BIOS NO 3.03
Copyright (c) 1984-88 Award Software Inc.
EVALUATION ROM - NOT FOR SALE - AWARD SOFTWARE INC.

TESTING INTERRUPT CONTROLLER #1 ... OK
TESTING INTERRUPT CONTROLLER #2 ... OK
TESTING CMOS BATTERY ... OK
TESTING CMOS CHECKSUM ... OK
TESTING EXTENDED CMOS CHECKSUM ... OK
SIZING SYSTEM MEMORY ... 640K FOUND
TESTING SYSTEM MEMORY ... 640K OK
CHECKING UNEXPECTED INTERRUPTS AND STUCK NI...OK
TESTING PROTECTED MODE ... OK
SIZING EXPANSION MEMORY ... 00384K FOUND
TESTING MEMORY IN PROTECTED MODE ... 01024K OK
TESTING PROCESSOR EXCEPTION INTERRUPTS ... OK
BIOS SHADOW RAM ... DISABLED
```



- Choose ITEM by ↑ ↓ key.
- Using PG/DN, PG/UP change SETUP value.

Please press "F10" key to go on next screen, while finishing SETUP.

AWARD SOFTWARE CMOS SETUP

DATE (MM/DD/YY)	9/8/88				
TIME (HH:MM:SS)	10:36:48				
DISKETTE 1	1.2M				
DISKETTE 2	NONE				
		CYLS	HEADS	SECTORS	PRECOMP
DISK 1	2	615	4	17	300
DISK 2	NONE				
VIDEO	EGA				
BASE MEMORY	640				
EXTENDED MEMORY	3X4				
ERROR HALT	NO KEYBOARD ERROR HALT				
SPEED SELECT	HIGH				
EXTENDED CMOS	ENABLE				

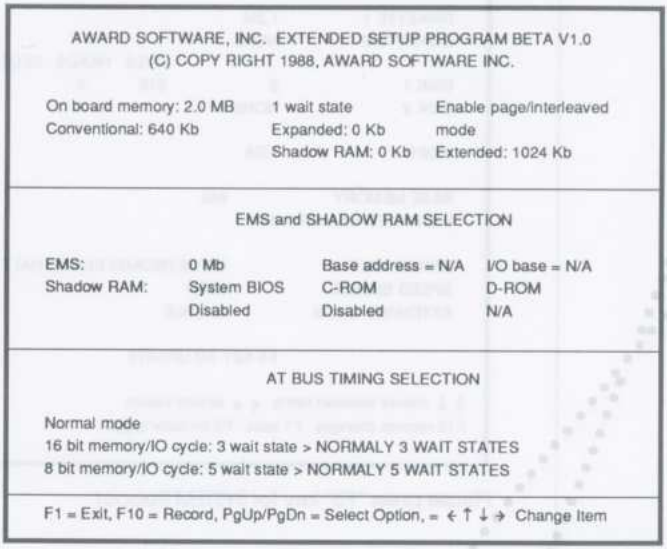
F5 KEY TO UPDATE

↑ ↓ moves between items. ← → selects values
F10 records changes. F1 exits. F2 for color toggle

Please press "F5" key for SYSTEM Reboot

AWARD provides one easy EXTENDED SETUP way.
According to the following figures, you can perform it.

Press "F3" for extended CMOS SETUP.



4-2 ALTERNATIVE SYSTEM SPEED

SOFTWARE SWITCH:

FOR AMI BIOS:

After booting the system, press "CTRL-ALT-" to become high-speed, "CTRL-ALT-" to low speed. Please see the following configuration:

CPU SPEED		CPU SPEED
16MHz	→ CTRL-ALT - →	8MHz
CPU SPEED		CPU SPEED
8MHz	→ CTRL-ALT + →	16MHz

0 WAIT STATES & 1 WAIT STATES

CTRL-SHIFT-ALT + → 0 WAIT STATES
CTRL-SHIFT-ALT - → 1 WAIT STATES

NOTE: Don't perform 0 WAIT STATES, if your system has only one bank or PAGE/INTERLEAVED MODE disable.

FOR PHOENIX BIOS:

After booting the system, press "CTRL-ALT-" to have low speed, press "CTRL-ALT-" again to have high speed.

CPU SPEED		CPU SPEED
16MHz	→ CTRL-ALT - →	8MHz
CPU SPEED		CPU SPEED
8MHz	→ CTRL-ALT - →	16MHz

For AWARD BIOS:

After booting the system, press "CTRL-ALT +" to have high speed, press "CTRL-ALT-" to have low speed, please refer to the following configuration:

CPU SPEED		CPU SPEED
8 MHz	→ CTRL-ALT + →	16MHz
CPU SPEED	CPU SPEED	
16MHz	→ CTRL-ALT - →	8MHz

NOTE: 1. If under the high speed condition, cursor looks like this: _
2. If under the low speed condition, cursor look like this: ■

HARDWARE SWITCH

TURBO SWITCH (CN4) ON THE N286 MAIN BOARD PROVIDE YOU AN EASY WAY TO CHANGE OPERATION BETWEEN THE NORMAL MODE AND THE TURBO MODE.
If CN4 is close, in the turbo mode, the CPU speed is 20MHz.
If CN4 is open, in the normal mode, the CPU speed is 16MHz.

Alternate use of both switches

Both the hardware and the software switches may be used alternatively, but this is not advised because you may become confused about the mode of operation. When using both switches alternatively, the Turbo LED will be the only accurate indicator of the actual mode: the LED will be on in Turbo mode and off in Normal mode.

4-3 EMS INSTALLATION

The EMS (Expanded Memory Specification) Version 4.0 device driver is a standard MS DOS device driver that gets loaded at boot time by the CONFIG.SYS file. Because EMS 4.0 is a device driver, it should look like this in the CONFIG.SYS file:

DEVICE = EMM.SYS

Without anything else included in this command line, the EMS driver will get loaded with the default hardware values of the I/O address that enables the EMS and the memory address used for EMS paging. These default values are dependent on the NEAT implementation of EMS.

To change these default values, as well as add a few extra features, the EMS device driver command line can look like this:

DEVICE = EMM.SYS -Ix-My-Pzz-D

Where,

I = I/O address to enable EMS pages

X = 0 == 208h
= 1 == 218h
= 5 == 258h
= 6 == 268h
= A == 2A8h
= B == 2B8h
= E == 2E8h

M = page frame address
(address of 64K window)

y = 1 == C0000h
= 2 == C4000h
= 3 == C8000h
= 4 == CC000h
= 5 == D0000h

P = maximum number of open processes
(defaults to 64)

zz = number of processes (1-128)

D = enable EMS diagnostics

The command line parameters can be in either upper or lower case.

When the EMS driver is first executed, a title and copyright notice will appear on the screen as follows:

"EMS Expanded Memory Device Driver Ver.4.0"
"Copyright(c) Chips and Technologies inc.,1987"

If the EMS driver detects that a previous EMS driver has been loaded, it will put this message on the screen:

"An Expanded Memory Manager has already been installed."

The EMS driver will then not get loaded into the system.

When the EMS driver gets loaded by MS DOS, an internal check is done on the EMS configuration in hardware. If the driver detects any conflicts that would cause EMS to not function properly, the message:

"The EMS setup has been incorrectly specified.
No EMS is available."

will appear on the screen after the EMS copyright notice and EMS will be disabled. If the EMS hardware is configured properly and the I/O address is overridden by the command line parameter, the screen will show this message:

"The EMS I/O address has been changed."

If the EMS page frame address is being overridden from the command line, the following message will appear:

"The EMS Frame Segment has been changed."

If the diagnostics option is selected, this message will appear on the screen:

"Testing EMS Expanded Memory Page Number : NNN"

The NNN represents the page number currently under test. If the diagnostics fail, the EMS will be disabled and the following message appears on the screen:

"Expanded Memory FAILED diagnostics test."

If the diagnostics pass, or if diagnostics were not specified on the command line, the EMS driver has been loaded correctly and EMS is enabled. The final message to appear on the screen is:

"There are XXX pages, or YYYY Kbytes of EMS Expanded Memory on the system."

The system can now be used to support Lotus/Intel/Microsoft EMS 4.0 in the same manner as standard EMS cards.

HOW TO SET EMS

1. Move cursor to register 6BH,bit 4;
   The right side screen message will show in the following:

DRAM Configuration Register RB7
EMS Enable bit 1=EMS Enabled 0=EMS Disabled

   This function is to enable the EMS function or not.

   Use <PgUp> and <PgDn> to set this bit to "1".

2. Move cursor to register 6FH,bit 7,6,5;
   The right side screen message will show:

Miscellaneous Register RB12
Set EMS Memory Size 000=Less than 1MB 001=1MB 010=2MB 011=3MB 100=4MB 101=5MB 110=6MB 111=7MB

   This function is to set the EMS size Because the first 1 MB is used by system EMS memory = all memory - 1 MB. Suppose you have 2 MB memory in which the first 1 MB is used by system, you have left 1 MB as EMS memory.

   Use <PgUp> or <PgDn> to set the EMS size to "001" 1MB.

3. Move cursor to register 6DH,bit 7,6,5,4;
   The right side screen message will show:

EMS Base address Register RB9
Expanded Memory Base address
0000=C0000H,C4000H,C8000H,CC000H
0001=C4000H,C8000H,CC000H,D0000H
0010=C8000H,CC000H,D0000H,D4000H
0011=CC000H,D0000H,D4000H,D8000H
0100=D0000H,D4000H,D8000H,DC000H
0101=D4000H,D8000H,DC000H,E0000H
0110=D8000H,DC000H,E0000H,E4000H
0111=DC000H,E0000H,E4000H,E8000H
1000=E0000H,E4000H,E8000H,EC000H

   This function selects the address of total 64K (Page 0,1,2,3) for EMS use. If you use D0000H,D4000H,D8000H,DC000H as EMS base address. Use <PgUp> and <PgDn> to set the EMS base address to "0100"

4. Move cursor to register 6EH,bit 7,6;
   The right side screen message show:

EMS Address Extenstion Register RB10
EMS Page 0 Position
00=1M to 2M of EMS Memory
01=2M to 4M of EMS Memory
10=4M to 6M of EMS Memory
11=6M to 8M of EMS Memory

This function selects which range the page register 0 map to. It must in the range of your EMS space. If you only have 1MB EMS between 1MB to 2MB range, so use <PgUp> and <PgDn> to set the EMS Page 0 Position to "00". Page 1 in bit 5,4, or Page 2 in bit 3,2, or Page 3 in bit 1,0 is also.

5. Move cursor to register 6DH,bit 3,2,1,0; The right side screen message will show:

EMS Base address Register RB9
EMS Page Reg I/O Base address 0000=208H/209H 0001=218H/219H 0101=258H/259H 0110=268H/269H 1010=2A8H/2A9H 1011=2B8H/2B9H 1110=2E8H/2E9H

This function is used to set Page Reg I/O Base address to avoid address conflict with other I/O device. Suppose you make sure that "208H/209H" is O.K., use <PgUp> and <PgDn> to set "0000".

CHAPTER 5 TECHNICAL INFORMATIONS

5-1 SYSTEM OVERVIEW

The system is designed for using in 16 to 20 MHZ 80286 based systems included the CS8221 NEAT CHIPSet (TM) and provides complete support for the IBM PC/AT bus.

The CS8221 NEAT CHIPSet (TM) consists of the 82C211 CPU/Bus controller, the 82C212 Page/Interleave and EMS Memory controller, the 82C215 Data/Address buffer and the 82C206 Integrated Peripherals Controller (IPC).

The NEAT CHIPSet (TM) supports the local CPU bus, a 16 bit system memory bus, and the AT buses as shown in the NEAT System Block Diagram. The 82C211 provides synchronization and control signals for all buses. The 82C211 also provides an independent AT bus clock and allows for dynamic selection between the processor clock and the user selectable AT bus clock. Command delays and wait states are software configurable, providing flexibility for slow or fast peripheral boards.

The 82C212 Page/Interleave and EMS Memory controller provides an interleaved memory sub-system design with page mode operation. It supports up to 8 MB of on-boad DRAM with combinations of 64Kbit, 256Kbit and 1Mbit DRAMs. The processor can operate at 16MHz with 0.5-0.7 wait state memory accesses, using 100 nsec DRAMs. This is possible through the Page Interleaved memory scheme. The Shadow RAM feature allows faster execution of code stored in EPROM. By down loading code from EPROM to RAM. The RAM then shadows the EPROM for futher code execution. In a DOS environment, memory above 1MB can be treated as LIM EMS memory.

The 82C215 Data/Address buffer provides the buffering and latching between the local CPU address bus and the Peripheral address bus. It also provides buffering between the local CPU data bus and the memory data bus. The parity bit generation and error detection logic resides in the 82C215.

5-2 82C211 BUS CONTROLLER

The 82C211 Bus Controller consists of the following functional sub-modules.

Reset and Shut Down Logic

When the system cold started, the power good signal from the power supply, the 82C211 asserts a reset signal for a system reset to reset the AT Bus, 82C206 IPC 8042 Keyboard controller, the 82C212 memory controller, and all of the system. The other reset signal is gernerated from the 8042(8742) Keyboard controller when a "warm reset" is required. The warm reset activates a reset signal the reset the 80286 CPU only.

Clock Generation and Selection

The 82C211 provides a flexible clock selection. It has two inputs clocks; CLK2IN and ATCLK Typically the ATCLK Should be of a lower frequency than CLK2IN. ATCLK and CLK2IN can be selected under program control.

In 20MHz system: We define CLK2IN = 40MHz and ATCLK = 20 MHz:
In 16MHz system, CLK2IN = 32MHz and ATCLK = 20MHz.

The 82C211 generates processor clock PROCCLK, for driving the CPU state machine and interface. SCLKC (internal), is PROCCLK/2 and is in phase with the internal states of the 80286. BCLK (internal) is the AT Bus state machine clock and is used for the AT bus interface. SYSCLK is the AT bus system clock and is always BCLK/2.

PROCCLK can be drived from CLK2IN or from ATCLK. In the synchronous mode, both PROCCLK and BCLK are drived from CLK2IN, so that the processor state machine and the AT bus state machine run synchronous. In the asynchronous mode, BCLK is generated from the ATCLK and PROCCLK is generated from CLK2IN or the ATCLK. In this case, the processor and AT bus state machines run asynchronous to each other.

The following clocks selections are possible:

Synchronous mode:

1 PROCCLK = BCLK = CLK2IN
SYSCLK = BCLK/2 = CLK2IN/2

2 PROCCLK = CLK2IN
BCLK = CLK2IN/2
SYSCLK = BCLK/2 = CLK2IN/4

3 PROCCLK = BCLK = CLK2IN/2
SYSCLK = BCLK/2 = CLK2IN/4

Asynchronous mode:

1 PROCCLK = CLK2IN
BCLK = ATCLK
SYSCLK = BCLK/2 = ATCLK/2

2 PROCCLK = ATCLK
BCLK = ATCLK
SYSCLK = BCLK/2 = ATCLK/2

Under normal operation, CLK2IN should be selected as the processor clock (PROCCLK) to allow the processor to run at full speed.

CPU State Machine, Bus State Machine, Bus arbitration, and Refresh Logic

In order to extract maximum performance out of the 80286 on the system board, it is desirable to run the system board at the rated maximum CPU frequency. The frequency may be too fast for the slow AT BUS. In order to overcome this problem, the 82C211 has two state machine: the CPU state machine which typically runs off CLK21N, and the AT bus state machine which runs off BCLK. The 82C211 also controls all bus activity and provides arbitration between the CPU, DMA/Master devices and DRAM refresh logic.

Port B and NMI Generation Logic

The 82C211 provides assess to Port B defined for the PC/AT as shown in this Figure:

I/O ADDR 61H	7 PCK	6 CHK	5 T20	4 RFD	3 EIC	2 EPR	1 SPK	0 T2G	PORT B

◆ *TABLE 5.1 PORT B REGISTER DEFINITION*

Bits	Read/ Write	Function
7	R	PCK-System memory parity check
6	R	CHK-I/O channel check
5	R	T20-Timer 2 out
4	R	RFD-Refresh Detect
3	R/W	EIC-Enable I/O channel check
2	R/W	ERP-Enable system memory parity check
1	R/W	SPK-Speaker Data
0	R/W	T2G-Timer 2 Gate (Speaker)

The NMI sub-module perorms the latching and enabling of I/O and parity error conditions, which will generate a non-maskable interrupt to the CPU if NMI is enabled. Reading Port B will indicate the source of the errorcondi tion (IOCK AND PCHK). Enabling and disabling of NMI is accomplished by writing to I/O address 070H. On the rising edge of XIOW. NMI will be enabled if data bit 7 (XD7) is equal to 0 and will be disabled if XD7 is equal to 1.

Numeric Co-processor Interface

Incorporated in the 82C211 is the circuitary to interface an 80287 Numeric Co-processor to 80286. The circuitary handles the decoding required for selecting and reset ting the Numeric Co-processor, handling -NPBUSY and ERROR signals from the 80287 to the CPU, and generating interrupt signals for error handling.

The -NPCS signal is active for I/O address 0F8H-0FFH, used to access the internal registers of the 80287. It is also active for I/O addresses 070H-NMI mask register. 0F0HClear the Numerical Co-processor and Numerical Coprocessor BUSY signal. While executing a task, the 80287 issues an -NPBUSY signal to the 82C211. Under normal operation, it is passed out to the CPU as -BUSY. If during this busy period, a numeric co-processor error occurs. -ERROR input to the 82C211 becomes active, resulting in latching of the BUSY output and assertion of NPINT. Both signals stay active until cleared by an I/O write cycle to address 0F0H or 0F1H. A system reset clears both NPINT and -BUSY latches in the 82C211. The 80287 is reset through the NPRESET output, which can be activated by a system reset or by performing a write operation to I/O port 0F1H.

Modes of Operation of the 82C211

The 82C211 has 4 modes of operation for different CPU and A1 bus clock selections:

Normal mode
Quick mode
Delayed mode
External mode

Normal Mode

This mode is enabled by default (without writing to the registers of 82C211).

Under Normal mode:

PROCCLK = CLK2IN
BCLK = CLK2IN/2
SYSCLK = CLK2IN/4

If activated by default, I/O cycles will have one command delay, 8 bit AT memory cycles will have 4 wait states, 16 bit AT memory cycles will have 1 wait state.

Quick Mode

This mode is also a synchronous mode and is enabled by writing a zero to REG61<6> and the following clock selections have been made:

PROCCLK = BCLK =CLK2IN
SYSCLK = CLK2IN/2

Quick mode is performance efficient when switching between local and AT bus cycles. This mode is useful for high speed add-on cards such as Laser Printer interface cards.

Delayed Mode

This mode is another synchronous mode and is enabled when Quick mode is disabled and the following clock selections have been chosen made:

PROCCLK =CLK2IN
BCLK = CLK2IN
SYSCLK = CLK2IN/2

This mode is useful for slow peripheral AT add-on cards.

External Mode

This is an asynchronous mode and is enabled when ATCLK is selected as the source for BCLK. The following clock selections are required in the mode:

PROCCLK = CLK2IN
BCLK = ATCLK
SYSCLK = ATCLK/2

chronized with CLK2IN. The CPU samples -READY low in sequence 10 and terminates the current cycle.

Configuration Registers

There are three bytes of configuration registers in the 82C211; RA0, RA1 and RA2. An indexing scheme is used to reduce the I/O ports required to access all the registers required for the NEAT CHIPSet. Port 22H is used as an indexing register and Port 23H is used as the data register. The index value is placed in port 22H to access a particular register and the data to be read from or written to that register is located in port 23H. Every access to port 23H must be preceded by a write of the index value to port 22H even if the same register data is being accessed again.

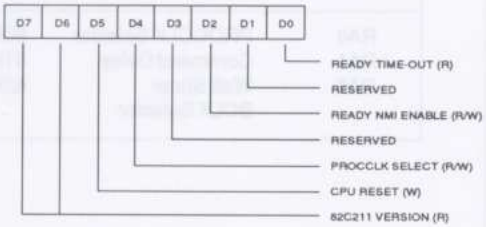
All reserved bits are set to zero by default and when written to, must be set to zero. Table 5.2 lists the three registers:

◆ *TABLE 5.2 RA0, RA1, RA2 REGISTERS*

Register Number	Register Name	Index
RA0	PROCCLK Selector	60H
RA1	Command Delay	61H
RA2	Wait State/ BCLK Selector	62H

Register Description

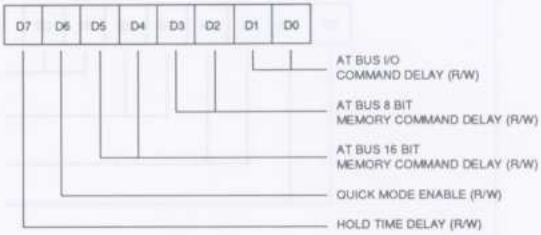
PROCCLK Register RA0
Index register port: 22H
Data register port: 23H
Index: 60H



◆ *TABLE 5.3*
RA0 REGISTER

Bits	Function
7, 6	82C211 revision number. 00 is the initial number
5	Alternate CPU reset. A low to high transition in this bit activates a CPU reset. Once active, it remains active for 16 PROCCLK cycles and then goes low.
4	Processor clock select is by default set to zero and selects PROCCLK = CLK2IN. If high, it selects PROCCLK = BCLK.
3	Reserved.
2	Local bus READY timeout NMI enable. A one enables the NMI and a zero disables it. Default is 0
1	Reserved.
0	Local bus READY timeout. A one indicates that READY timeout has occurred 128 PROCCLK cycles after-AF16 has been asserted. A zero indicates that READY time out has not occured.

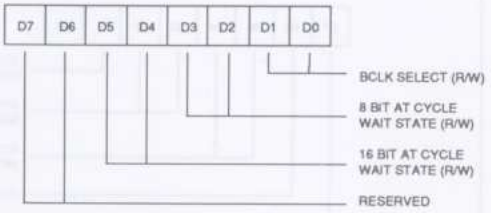
Command Delay Register RA1
Index register port: 22H
Data register port: 23H
Index: 61H



◆ *TABLE 5.4*
RA1 REGISTER

Bits	Function
1, 0	AT Bus I/O cycle command delay. Specifies between 0 to 3 BCLK cycle command delays for AT I/O cycles. Default is 1.
3, 2	AT Bus 8 bit memory command delay. Specifies between 0 to 3 BCLK cycle command delays for 8 bit AT memory cycle. Default is 1.
5, 4	AT Bus 16 bit memory command delay. Specifies between 0 and 3 BCLK cycle command delays for 16 bit AT memory cycles. Default is 0.
6	Quick mode enable. A zero enables Quick mode a one disables it. Default is 1.
7	Address hold time delay. A one enables extra address bus hold time and a zero disables it. Default is 0.

Wait States Register RA2
Index register port: 22H
Data register port: 23H
Index: 62H



◆ *TABLE 5.5*
RA2 REGISTER

Bit	Function
1, 0	Bus clock (bclk) source select. Default is 00. 0 BCLK = CLK2IN/2 01 BCLK = CLK2IN 10 BCLK = ATCLK 11 Reserved
3, 2	8 bit at cycle wait state generation. Default is 5. 00 2 wait states 01 3 wait states 10 4 wait states 11 5 wait states
5, 4	16 bit AT cycle wait state generation. Default is 3. 00 0 wait states 01 1 wait states 10 2 wiat states 11 3 wait states
7, 6	Reserved

5-3 82C212 PAGE/INTELEAVE AND EMS MEMORY CONTROLLER

The 82C211 perorms the memory control function in the system.

The 82C211 organizes memory as banks of 18 bit modules consisting of 16 bits of data and 2 bits of parity, information. The 16 bits of date are split into high and lower bytes with 1 parity bit for each byte. The minimum configuration can be a single bank operating in non-interleaved mode or can be a pair of DRAM banks operating in two way interleaved mode, the DRAMs within a pair of banks must be indentical.

However, each bank of DRAM pairs can be different from other paris. For example, Banks 0,1 may have 256K by 1 bit DRAM and Banks 2,3 could have 1M by 1 bit DRAMs. A typical sytem may be shipped with one or two banks of smaller DRAM types (eg. 256 by 1 bit DRAMs) and later upgraded with additional pairs of banks of larger DRAMs (eg. 1M by 1 bit DRAMs)

Page/Interleaved Operation

The 82C212 uses a page/interleaved design that is differ ent from most interleaved memory designs. Typical two way interleaving schemes use two banks of DRAMs with even word addresses on one bank and odd world ad dresses on the other bank. If memory acesses are sequen tial the RAS precharge time of one bank overlaps the access time of the other bank. Typically, programs consist of insturction fetches interspersed with operand accesses.

The instruction fetches tend to be sequential and the operand accesses tend to be random.

Figure 5.1 is a sequence diagram for a memory inteleaved scheme using two banks 0 and 1. The -RAS signals of the two banks are interleaved so that the RAS precharge time (Trp) of one bank is used for the -RAS active time in the other bank. This requires sequential acesses to be alternat ing between the two banks. For non-sequential accesses it is possible to get wait states due to a 'miss'. Typically this results in a 50% hit ratio (possible zero wait state accesses)

◆ *FIGURE 5.1 DRAM INTERRLEAVED OPERATION*

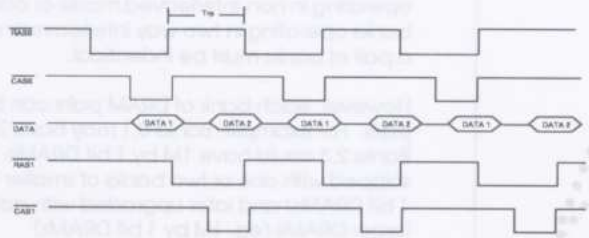


Figure 5.2 is a sequence diagram of a paged mode DRAM operation. In paged mode DRAMs. once a row access has been made, it is possible to access subsequent column address within that row, without the -RAS pre charge penalty.
However, after a -RAS active timeout, there is a -RAS precharge period which typically occurs every 10 micro seconds. Since the CAS precharge time Tcp is small, it is possible to make fast random accesses within a selected row. Typically, page mode access times are half the normal DRAM access times. For 256K x 1 DRAMs. each row has 512 bits. If eighteen 256K x 1 bit DRAMs are used to im plement a bank, a page would have 512 x 2 bits (exclud ing 2 bits for parity) = 1 Kbytes, Thus paged mode DRAMs could be interleaved at 1 Kbyte boundaries rather than 2 byte boundaries as in the regular interleaved mode operation. Any access to the currently active -RAS page would occur in a short page access time and any subse quent access could be anywhere in the same 1 Kbyte

boundary, without incurring any penalty due to -RAS precharge. If memory is configured to take advantage of this DRAM organization, significantly better performance can be a thieved over normal interleaving because:

> Page mode access time is shorter than normal DRAM access time. This allows more time in the DRAM critical paths, to achieve penalty free accesses or 'hits'.

The possibility of the next access being fast is significantly higher than in a regular interleaving scheme. This is because instructions and data tend to cluster together by principle of locality of reference.

◆ *FIGURE 5.2 DRAM PAGE MODE OPERATION*

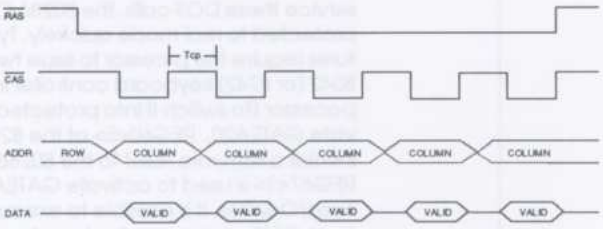
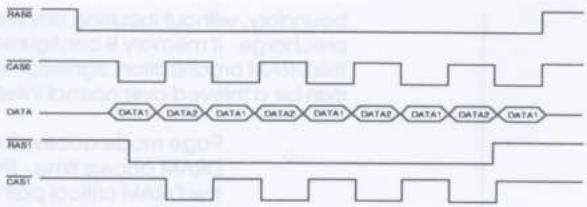


Figure 5.3 is a sequence diagram of a two way Page/ Interleaved scheme using page mode DRAMs. As seen, it is possible to make zero wait state accesses between the two banks 0 and 1, by overlapping -CAS precharge time of once bank with -CAS active time of the other bank. The DRAM -RAS lines for both banks can be held active till the -RAS active timeout period, at which time a -RAS precharge for that bank is reauired. Typical hit ratios highter than 80% are possible using this scheme. With the 82C212 memory controller, using the page/interleaved scheme, 100 nanosecond access time DRAMs at 16MHz.

◆ *FIGURE 5.3 DRAM PAGE/ INTERLEAVE OPERATION*



OS/2 OPTIMIZATION

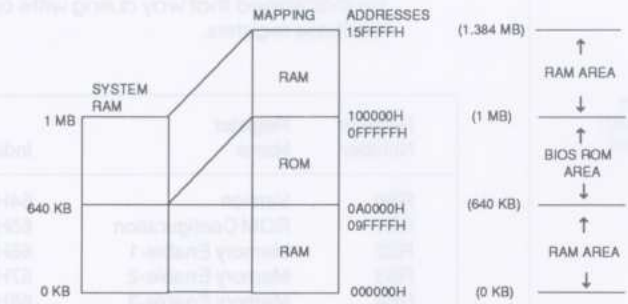
The NEAT architecture feature OS/2 optimization using REG67<1> of the 82C212 in conjunction with REG60<5> of the 82C211 OS/2 makes frequent DOS calls while operat ing in protected mode of the 80286 CPU. In order to service these DOS calls, the 80286 CPU has to switch from protected to real mode quickely. Typical PC/AT architec tures require the prcessor to issue two commands to the 8042 (or 8742) keyboard controller in order to reset the pocessor (to switch it into protected mode) and to acti vate GATEA20. REG60<5> of the 82C211 is to used to invoke a software reset to the 80286 processor and REG67<1> is used to activate GATEA20. Since this involved two I/O writes, it is possible to execute a "Fast GATEA20". In an OS/2 environment, where frequent DOS calls are made, this feature provides signficant performance improvement.

MEMORY MAPPING

The 82C212 has an extensive set of memory mapping registers for various memory organizations. Through the memory mapping logic, for up to 1 Mbyte of sytem RAM, it is possible to map RAM that overlaps the EPROM area (640Kbyte-1Mbyte) above the 1Mbyte area, as shown in Figure 5.4. Hence, for 1Mbyte of on board RAM, the soft ware can address it from 0 to 640Kbytes and from 1Mbyte to 1.384Mbytes. The EPROM can be addresed from the 640 Kbyte area to the 1Mbyte area.

For normal mode of operation, only one bank of DRAMs may be used. However, for the page/interleaved mode of opeation, RAM bank pairs must be used.

◆ *FIGURE 5.4 SYSTEM RAM/ROM MAPPING FOR 1MB SYSTEM DRAM*



CLOCK GENERATION LOGIC

The 82C212 has an oscillator circuit which uses a 14.31818MHz crystal to generate the OSC and OSC/12 clock. The 1.19381MHz OSC/12 clock is used internally to generate the -RAS timeout clocks, one for each bank. -RAS is deasserted for each bank when its -RAS time out counter times out after about 10 microseconds.

CONFIGURATION REGISTERS

There are twelve configuration and diagnostics registers in the 82C212, RB0-RB11. These are accessed through I/O ports 22H and 23H normally found in the interrrupt controller module of the 82C206 IPC. An indexing scheme is used to reduce the number of I/O addresses required to access all of the regiters needed to configure and control the memory controller. Port 22H is used as and index register that points to the required data value accessed through port 23H. A write of the index value for the required data is performed to location 22H. This is then decoded and

controls the multiplexers gating the appropriate register to the output bus. Every access to port 23H must be pre ceded by a write of the index value to port 22H even if the same data register is being accessed again. All bits marked as Reserved are set to zero by default and must be maintained that way during write operations. Table 5.6 lists these registers.

◆ *TABLE 5.6 RB0 TO RB11 REGISTERS*

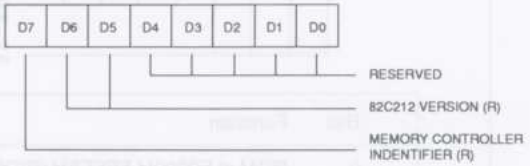
Register Number	Register Name	Index
RB0	Version	64H
RB1	ROM Configuration	65H
RB2	Memory Enable-1	66H
RB3	Memory Enable-2	67H
RB4	Memory Enable-3	68H
RB5	Memory Enable-4	69H
RB6	Bank 0/1 Enable	6AH
RB7	DRAM Configuration	6BH
RB8	Bank 2/3 Enable	6CH
RB9	EMS Base Address	6DH
RB10	EMS Address Extesion	6EH
RB11	Miscellaneous	6FH

* For correct DRAM type, please refer to the following table:

		1 WAIT STATE	0 WAIT
PAGE/ INTERLEAVED	16 MHZ 20 MHZ	150 NS 120 NS	100 NS 80 NS
CONVENSIONAL	16 MHZ 20 MHZ	100 NS 80 NS	60 NS X NS

REGISTER DESCRIPTION

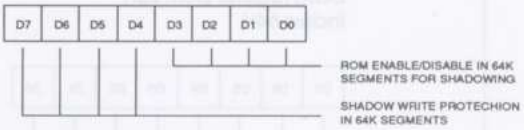
Version Register RB0
Index register port: 22H
Data register port: 23H
Index: 64H



◆ *TABLE 5.7*
RB0 REGISTER

Bits	Function
7	NEAT memory controller indentifier. 0 = 82C212
6,5	82C212 revision number.00=initial revision number
4-0	Reserved

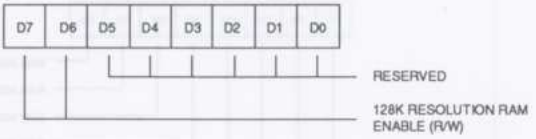
ROM configuration Register RB1
Index register port: 22H
Data register port: 23H (R/W)
Index: 65H



◆ *TABLE 5.8*
RB1 REGISTER

Bits	Function
0	ROM at F0000H-FFFFFH (BIOS). Default =0= ROM enabled -ROMCS is generated.
1	ROM at E0000H-EFFFFH. Default = 1 = ROM disabled. Shadow RAM enabled. -ROMCS is not generated unless bit is set to 0.
2	ROM at D0000H-DFFFFH. Default = 1 = ROM disabled. Shadow RAM enabled. ROMCS is not generated unless bit is set to 0.
3	ROM at C0000H-CFFFFH (EGA). Default = 1 = ROM Disabled. Shadow RAM enabled. -ROMCS is not generated unless bit is set to 0.
4	Shadow RAM at F0000H-FFFFFH in Read/Write mode. 0 = Read/Write (default). 1 = Read only (write protected).
5	Shadow RAM at E0000H-EFFFFH in Read/Write mode. 0 = Read/Write (default). 1 = Read only (write protected).
6	Shadow RAM at D0000H-DFFFFH in Read/Write mode. 0 = Read/Write (default). 1 = Read only (write protected).
7	Shadow RAM at C0000H-CFFFFH in Read/Write mode. 0 = Read/Write (default). 1 = Read only (write portedted).

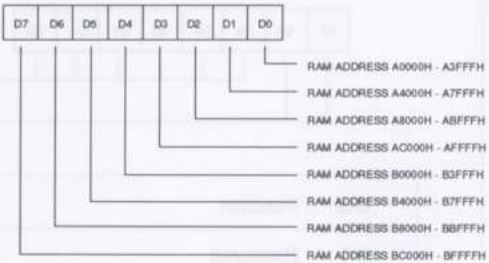
Memory Enable-1 Register RB2
Index register port: 22H
Data register port: 23H
Index: 66H



◆ *TABLE 5.9*
RB2 REGISTER

Bits	Function
0-6	Reserved
7	Address map RAM on sytem board in 80000H-9FFFFH area. 0=Address is on the I/O channel (default). 1=Address is on the system board is put out by the 82C212

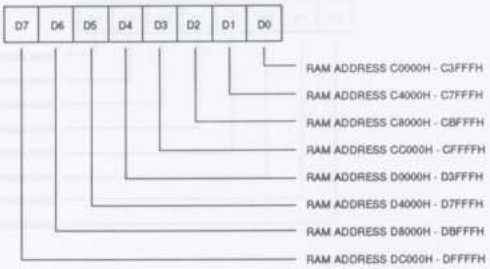
Memory Enable Register-2 RB3
Index register port: 22H
Data register port: 23H (R/W)
Index: 67H



◆ *TABLE 5.10*
RB3 REGISTER

Bits	Function
0	Enable shadow RAM in A0000H-A3FFFH area. Disable = 0 Enable = 1
1	Enable shadow RAM in A4000H-A7FFFH area. Disable = 0 Enable = 1
2	Enable shadow RAM in A8000H-ABFFFH area. Disable = 0 Enable = 1
3	Enable shadow RAM in AC000H-AFFFFH area. Disable = 0 Enable = 1
4	Enable shadow RAM in B0000H-B3FFFH area. Disable = 0 Enable = 1
5	Enable shadow RAM in B4000H-B7FFFH area. Disable = 0 Enable = 1
6	Enable shadow RAM in B8000H-BBFFFH area. Disable = 0 Enable = 1
7	Enable shadow RAM in BC000H-BFFFFH area. Disable = 0 Enable = 1

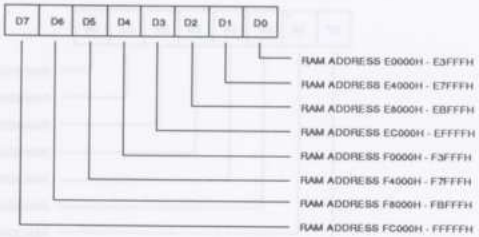
Memory Enable-3 Register RB4
Index register port: 22H
Data register port: 23H (R/W)
Index: 68H



◆ *TABLE 5.11*
RB4 REGISTER

Bits	Function
0	Enable shadow RAM in C0000H-C3FFFH area. Disable = 0 Enable = 1
1	Enable shadow RAM in C4000H-C7FFFH area. Disable = 0 Enable = 1
2	Enable shadow RAM in C8000H-CBFFFH area. Disable = 0 Enable = 1
3	Enable shadow RAM in CC000H-CFFFFH area. Disable = 0 Enable = 1
4	Enable shadow RAM in D0000H-D3FFFH area. Disable =0 Enable = 1
5	Enable shadow RAM in D4000H-D7FFFH area. Disable = 0 Enable = 1
6	Enable shadow RAM in D8000H-DBFFFH area. Disable = 0 Enable = 1
7	Enable shadow RAM in DC0006-DFFFFH area. Disable = 0 Enable = 1

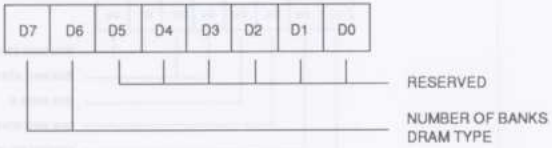
Memory Enable-4 Register (RB5)
Index register port: 22H
Data register port: 23H (R/W)
Index: 69H



◆ *TABLE 5.12*
RB5 REGISTERS

Bits	Function
0	Enable shadow RAM in E0000H-E3FFFH area. Disable = 0 Enable = 1
1	Enable shadow RAM in E4000H-E7FFFH area. Disable = 0 Enable = 1
2	Enable shadow RAM in E8000H-EBFFFH area. Disable = 0 Enable = 1
3	Enable shadow RAM in EC000H-EFFFFH area. Disable = 0 Enable = 1
4	Enable shadow RAM in E0000H-F3FFFH area. Disable = 0 Enable = 1
5	Enable shadow RAM in F4000H-F7FFFH area. Disable = 0 Enable = 1
6	Enable shadow RAM in F8000H-FBFFFH area. Disable = 0 Enable = 1
7	Enable shadow RAM in FC000H-FFFFFH area. Disable = 0 Enable = 1

Bnak0/1 Enable Regiser RB6
Index register port: 22H
Data register port: 23H
Index: 6AH

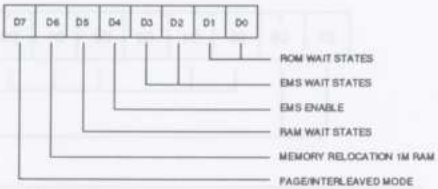


◆ *TABLE 5.13*
RB6 REGISTER

Bits	Function
0-4	Reserved
5	Number of RAM banks used. 0=1 bank. non-interleaved mode (Default) 1=2 banks
7,6	These bits contain the information for the DRAM types used on the sytem board. POST/BIOS should use the DRAM configuration data stored in the CMOS RAM of the 82C206 IPC.

7	6	DRAM Types
0	0	Disabled
0	1	256K and 64K bit DRAMs used (for 640Kbyte combination only)
1	0	256K bit DRAMs used (Default)
1	1	1M bit DRAMs used

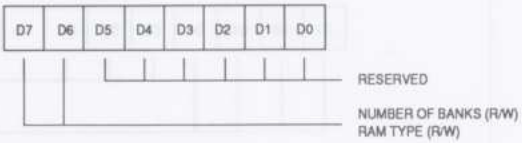
DRAM Configuration Register RB7
Index register port: 22H
Data register port: 23H (R/W)
Index: 6BH



◆ *TABLE 5.14*
RB7 REGISTER

Bits	Function
1, 0	ROM access wait states control. 1 0 Wait States 0 0 0 0 1 1 1 0 2 1 1 3 (Default)
3, 2	EMS memory access wait states. 3 2 Wait States 0 0 0 0 1 1 1 0 2 (default) 1 1 Reserved
4	EMS enable bit. If set to 0, EMS is disabled (Default). If set to 1, EMS is enabled.
5	RAM access wait states. If set to 0, accesses have 0 wait states. If set to1 (Default), accesses will have 1 wait state.
6	640Kbyte to 1Mbyte RAM relocation bit. A zero does not relocate local RAM. A one (Default) relocates local RAM from 080000H-09FFFFH to 100000H-11FFFFH, provided total local RAM is 1Mbyte only.
7	Page/Interleaved mode enable. A 0 disables the page/interleaved mode, allowing useage of normal mode for the DRAMs (Default). A 1 enables page/interleaved mode for the DRAMs.

Bank 2/3 Enable Register RB8
Index register port: 22H
Data register port: 23H
Index: 6CH

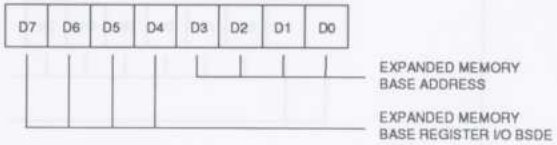


◆ *TABLE 5.15 RB8 REGISTER*

Bits	Function
0-4	Reserved
5	Number of local RAM Banks used. 0 = 1 Bank used, non-interleaved mode only (Default). 1 = 2 Banks used.
7, 6	These bits indicate the local DRAM type as listed:

7	6	RAM Type
0	0	None (Default)
0	1	Reserved
1	0	56 Kbit
1	1	1 Mbit

EMS Base Address Register RB9
Index register port: 22H
Data register port: 23H (R/W)
Index: 6DH



◆ *TABLE 5.16 RB9 REGISTER*

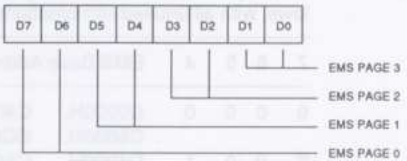
Bits	Function
0-3	These bits are used for the EMS page register I/O base address. The bits are encoded as follows. with unused combinations being reserved:

3	2	1	0	I/O Base
0	0	0	0	208H/209H
0	0	0	1	218H/219H
0	1	0	1	258H/259H
0	1	1	0	268H/269H
1	0	1	0	2A8H/2A9H
1	0	1	1	2B8H/2B9H
1	1	1	0	2E8H/2E9H

Bits	Function
7-4	These bits are used for selecting the expanded memory base addresses. They are encoded as follows, with all unused combinations being reserved:

7	6	5	4	EMS Base Addresses	
0	0	0	0	C0000H,	C4000H,
				C8000H,	CC000H
0	0	0	1	C4000H,	C8000H,
				CC000H,	D0000H
0	0	1	0	C8000H,	CC000H,
				D0000H,	D4000H
0	0	1	1	CC000H,	D4000H,
				D4000H,	D8000H
0	1	0	0	D0000H,	D4000H,
				D8000H,	DC000H
0	1	0	1	D4000H,	D8000H,
				DC000H,	E0000H
0	1	1	0	D8000H,	DC000H,
				E0000H,	E4000H
0	1	1	1	DC000H,	E0000H,
				E4000H,	E8000H
1	0	0	0	E0000H,	E4000H,
				E8000H,	EC000H

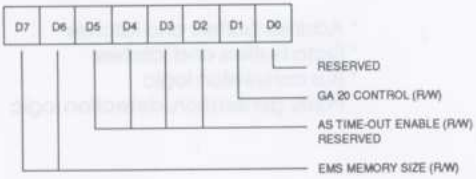
EMS Address Extention Register RB10
Index register port: 22H
Data register port: 23H
Index: 6EH



◆ *TABLE 5.17*
RB10 REGISTER

Bits	Function
1, 0	EMS Page 3 address extension bits. 1 0 Block of EMS Memory 0 0 1 Mbyte to 2 Mbyte 0 1 2 Mbyte to 4 Mbyte 1 0 4 Mbyte to 6 Mbyte 1 1 6 Mbyte to 8 Mbyte
3, 2	EMS Page 2 address extension bits. 3 2 Block of EMS Memory 0 0 1 Mbyte to 2 Mbyte 0 1 2 Mbyte to 4 Mbyte 1 0 4 Mbyte to 6 Mbyte 1 1 6 Mbyte to 8 Mbyte
5, 4	EMS Page 1 address extension bits. 5 4 Block of EMS Memory 0 0 1 Mbyte to 2 Mbyte 0 1 2 Mbyte to 4 Mbyte 1 0 4 Mbyte to 6 Mbyte 1 1 6 Mbyte to 8 Mbyte
7, 6	EMS Page 0 address extension bits. 7 6 Block of EMS Memory 0 0 1 Mbyte to 2 Mbyte 0 1 2 Mbyte to 4 Mbyte 1 0 4 Mbyte to 6 Mbyte 1 1 6 Mbyte to 8 Mbyte

Miscellaneous Register RB12
Index register port: 22H
Data register port: 23H
Index: 6FH



◆ *TABLE 5.18*
RB12 REGISTER

Bits	Function
0	Reserved
1	This bit is used for Address line A20 control and provides OS/2 optimization while switching between user and protected modes. The bit defaults to 0 and enables CPUA20 onto A20. If set to 1, it sets A20 = 0
2	This bit is used to enable the RAS time-out counter for page mode operation. The counter is disabled if set to 0 (Default) and is enabled if set to 1.
3, 4	Reserved
7-5	These bits are used to set the EMS memory space according to the following coding:

7	6	5	EMS Memory Size
0	0	0	1 Mbyte to 1.5 Mbytes (0.5MB)
0	0	1	1 Mbyte to 2 Mbytes (1 MB)
0	1	0	1 Mbyte to 3 Mbytes (2 MB)
0	1	1	1 Mbyte to 4 Mbytes (3 MB)
1	0	0	1 Mbyte to 5 Mbytes (4 MB)
1	0	1	1 Mbyte to 6 Mbytes (5 MB)
1	1	0	1 Mbyte to 7 Mbytes (6 MB)
1	1	1	1 Mbyte to 8 Mbytes (7 MB)

5-4 82C215 DATA/ADDRESS BUFFER

The 82C215 DATA/ADDRESS BUFFER consists of the following sub-modules.

* Address buffers and latches
* Data buffers and latches
* Bus conversion logic
* Parity generation/detection logic

5-5 82C206 INTEGRATED PERIPHERAL CONTROLLER

The 82C206 contains the equivalent of two 8237A DMA Controllers, a 74LS612 Mapper, two 8259A Interrupt Controllers, an 8254 Counter/Timer, and a MC146818 Real Time Clock with RAM.

Two DMA Controllers are provided and connected in such a way as to provide the user with four channels of DMA (DMA1) for 8 bit transfers and three channels of DMA (DMA2) for 16 bit transfers (the first 16-bit DMA channel is used for cascading). Included as part of the DMA subsystem is the Page Register (DMAPAGE) device which is used to supplement the DMA and drive the upper address lines when required.

Sixteen channels of interrupt are provided in the 82C206. These channels are partitioned into two cascaded controllers (INTC1, INTC2) with 8 inputs each.

Of these 16 channels, three are connected internally to various devices, allowing 13 user definable channels of interrupt. The three internally connected channels are as follows:

Channel 0 - Counter/Timer Counter 0 Interrupt

Channel 2 - Cascade to Slave Interrupt Controller (INTC2)

Channel 8 - Real Time Clock Interrupt

The remaining 13 channels may be defined and utilized as necessary to meet the users specific system requirements.

A Counter/Timer (CTC) sybsystem is provided which contains three independent counters. All three counters are driven from a clock inputs to the device. Counter 0 is connected to Interrupt 0 of INTC1. It is intended to be used as a multi-level interrupt to the system for such tasks as time keeping and task switching. Counter 1 may programmed to generate pulses or square waves for use by external devices. The third channel (Counter 2) is a full

function Counter/Timer which has a gate input for controlling the internal counter. This channel can be used as an internal counter, a timer, or as a gated rate/pulse generator.

A Real Time Clock (RTC) is included in the 82C206 for maintaining the time and date. This subsystem also contains114bytes of RAM in addition to the Clock/Calendar. The Clock/Calendar information and RAM are kept active by connecting the device to an external battery when system power is turned off.

To interconnect and control all of these major subsystems a top level control section is employed which is divided into subsystems for purposes of discussion.

The following Clock and Wait State Control subsystem controls the generation of DMA wait states and the negation of IOCHRDY (if programmed to do so) during CPU access of the device.

In order to accommodate over 200 registers in the 82C206 and maintain I/O decode compatibility with the IBM PC/AT, a multi-level decode scheme is employed. The Top Level Decode subsystem performs the function of generating enables to the various subsystem. Control and direction of the XD0-XD7 data bus buffers are also handles by this subsystem.

Each of these subsystems will now be described separately.

5-6 82C206 - Top Level Decode

The 82C206 Top Level Decode Provides 8 separate enables to various subsystems of the device. Figure 8 contains a truth table for the Top Level Decoder. The enabling of the 82C206 XD0-XD7 output buffers is also controlled by this section. The output buffers are enabled whenever an enable is generated to an internal subsystem and the XIOR signal is asserted.

◆ *TABLE 5.19 82C206 INTERAL DECODE*

-ACK	XA 9	XA 8	XA 7	XA 6	XA 5	XA 4	XA 3	XA 2	XA 1	XA 0	RANGE	DEVICE
1	0	0	0	0	0	0	X	X	X	X	000-00F	DMA1
1	0	0	0	0	1	0	0	0	0	X	020-021	INTC1
1	0	0	0	0	1	0	0	0	1	X	022-023	CONFIG
1	0	0	0	1	0	0	0	0	X	X	040-043	CTC
1	0	0	0	1	1	1	0	0	0	1	071	RTC
1	0	0	1	0	0	0	X	X	X	X	080-08F	DMAPAGE
1	0	0	1	0	1	0	0	0	0	X	0A0-0A1	INTC2
1	0	0	1	1	0	X	X	X	X	X	0C0-0DF	DMA2
0	X	X	X	X	X	X	X	X	X	X	DISABLED	
X	1	X	X	X	X	X	X	X	X	X	DISABLED	
X	X	1	X	X	X	X	X	X	X	X	DISABLED	

The decode scheme employed in the 82C206 is designed to comply with the IBM PC/AT requirements and is more fully decoded. If the user wishes to take advantage of the areas which are unused by inserting additional peripherals in the I/O map, he may do so since the subsystems in the 82C206 will not respond to the unused address spaces established by the Top Level Decoder. The extra peripherals may be tied directly to the XD0-XD7 data lines since the 82C206 output buffers are not enabled unless an internal subsystem is enabled.

5-7 CLOCK AND WAIT STATE CONTROL

The Clock and Wait State Control subsystem performs four functions, control of the DMA command width, control of the CPU read or write cycle length, and selection of the DMA clock rate. All of these functions are user selectable by writing to the Configuration Register located at address 023H.

Writing and reading this register is accomplished by first writing a 01H to location 022H to select the 82C206 Configuration Register, and then performing either a read or write to location 023H.

◆ *TABLE 5.20 CONFIGURATION REGISTER 023H*

msb							1sb
b7	b6	b5	b4	b3	b2	b1	b0
RW1	RW0	16W1	16W0	8W1	8W0	EMR	CLK

RW1-RW0-When the higher speed CPU's are accessing the 82C206, the cycle can be extended by programming up to four wait states into the Configuration Register. This will cause the 82C206 to assert a not ready condition on IOCHRDY (low) whenever a valid decode from the Top Level Decoder is detected and either XIOR or -XIOW is asserted. IOCHRDY will remain low for the number of wait states programmed into the Configuration Register bits 6 and 7.

◆ *TABLE 5.21 CONFIGURATION REGISTER BITS 6 AND 7*

RW1	RW0	Read/Write Cycle Wait States
0	0	1
0	1	2
1	0	3
1	1	4

Wait states are in increments of one SCLK cycle and are not affected by the DMA Clock Divider.

16W1-16W0—Wait states can be independently controlled for both 8-bit and 16-bit DMA cycles. This allows the user to tailor the DMA cycle more closely to the application.

◆ *TABLE 5.22 16W1, 16W0 CONFIGURATION REGISTER*

16W1	16W0	16-Bit DMA Wait States
0	0	1
0	1	2
1	0	3
1	1	4

8W1-8W0—Wait states may be inserted in 8-bit DMA cycles by programming these two bits in the Configuration Register.

◆ *TABLE 5.23 8W1, 8W0 CONFIGURATION REGISTER*

8W1	8W0	8-Bit DMA Wait States
0	0	1
0	1	2
1	0	3
1	1	4

Further control of the cycle length is available through the use of the IOCHRDY pin on the 82C206. During DMA this pin is used as an input to the wait state generation logic to extend the cycle if necessary. This input is driven low (0) by the peripheral to extend the cycle. The cycle can then be completed by releasing IOCHRDY and allowing it to return high (1).

EMR - This bit enables the extended - DMAMEMR function. Normally the assertion of -DMAMEMR is delayed one clock cycle later than - XIOR in the IBM PC/AT implementation. This may not be desirable in some systems A "1" programmend into this bit position will start - DMAMEMR at the same time as -XIOR.

CLK - This bit allow the user to insert a divider between the DMA Controller subsystems and the SCLK input pin, or connect the two directly. When this bit position contains a "0", the SCLK input is divided by two and is used to drive both the 8-bit band 16 bit DMA subsystems. A "1" in this position by passes the divider and uses the SCLK input directly. Whenever the state of this bit is changed, an internal synchronizer controls the actual switching of the clock to prevent a short clock pulse from causing a DMA malfunction.

The Configuration Register contents are preloaded by RESET to an initial value of 0C0 hex. This value establishes a default which is IBM PC/AT compatible and corresponds to:

Read/Write cycles—4 wait states

16-bit DMA transfers—1 wait state

8-bit DMA transfers—1 wait state

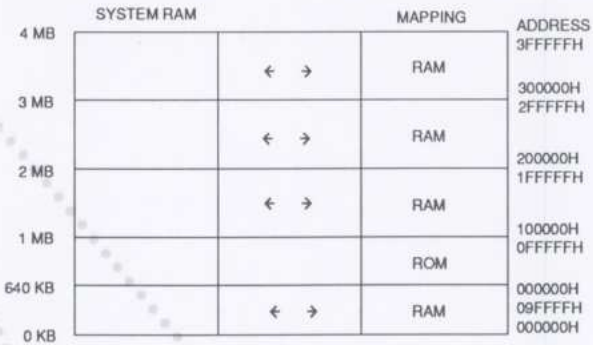
-DMAMEMR delayed 1 DMA clock cycle later than - XIOR.
DMA clock is equal to SCLK/2.

5-8 SHADOW RAM

For efficient execution of BIOS, it is preferable to execute BIOS code through RAM rather than through slower EPROMs. The 82C212 provides the shadow RAM feature which if enabled allows the BIOS code to be executed from address as the BIOS EPROM The software should transfer code stored in the BIOS EPROMs to the system RAM, before enabling the shadow RAM feature. This feature significantly improves the performance as BIOS-call intensive applications. Performance improvements as high as 300 to 400% have been observed in benckmark tests on the shadow RAM. The shadow RAM feature is invoked by enabling the corresponding bits in the ROM enable register and the RAM mapping register.

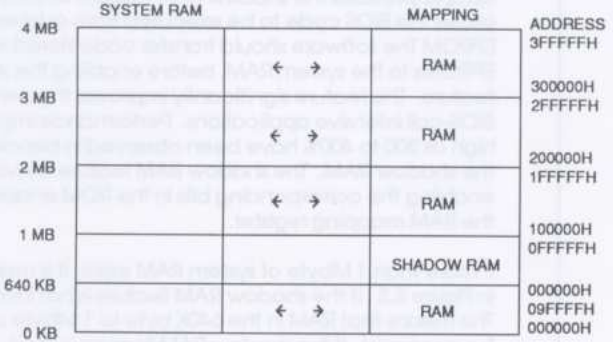
If more than 1 Mbyte of system RAM exists, it is mapped as shown in Figure 5.5 . if the shadow RAM feature is not invoked. This means that RAM in the 640K byte to 1 Mbyte area cannot be accessed. If the shadow RAM feature is used, then the RAM is mapped as

◆ *FIGURE 5.5 RAM/ROM MAPPING WITHOUT SHADOW RAM (MORE THAN 1MB OF ROM)*



shown in Fugure 5.6 , overlapping or Shadowing the EPROM area. In both cases, for accesses beyond the 1 Mbyte address range, the processor is switched from real to protected mode from BIOS.

◆ *FIGURE 5.6 RAM MAPPING WITH SHADOW RAM (MORE THAN 1MB OF RAM)*



HOW TO SETUP SHADOW RAM

In this case suppose you want your BIOS (from F0000H to FFFFFH) shadow to RAM.

1. Move cursor to register 65H, bit 4;
   The right side screen message will show:

ROM Configuration Register RB1
SHADOW RAM at F0000H to FFFFFH 0 = Read/Write Enable 1 = Read Only (Write Protected)

This function is used to set your shadow RAM to READ/Write enable or just Read only.

Suppose you don't want change your BIOS in the shadow RAM, use <PgUp> and <PgDn> to select the bit to "1"

2. Move cursor to register 65H, bit 0;
   The right side screen message will show:

ROM Configuration Register RB1
ROM at F0000H to FFFFFH 1 = ROM Disabled 0 = ROM Enabled

You must disable the ROM so that we can use the shadow RAM BIOS; use <PgUp> and <PgDn> to select the bit to "1".

3. Move cursor to register 69H, bit 4;
   The right side screen message will show:

Memory Enable-4 Register RB5
SHADOW RAM at F0000H to F3FFFFH 0 = Disable 1 = Enable

After disable the BIOS ROM above, the sequence is enable the RAM as shadow RAM.

First we enable the RAM between the address from F0000H to F3FFFFH.

Use <PgUp> and <PgDn> to select the bit to "1" move cursor to bit 5,6,7 separately; same as the bit 4 set those bits to "1"

EXIT

Now we have finished those setup, and press <ESC> to return main menu.

Move highlight bar to the "ENABLE/DISABLE VIDEO AND MAIN BIOS SHADOW" item and press <Enter> key.
In this item the screen will show as below:

SHADOW FOR ROM BIOS → 0 SHADOW FOR VIDEO RAM → 0

You want to set shadow for ROM BIOS and all setup you have done just before, here is an switch that can active your shadow RAM function.

Move cursor on the "SHADOW FOR ROM BIOS" item the message on the right side screen will show as below:

SHADOW FOR ROM BIOS

1 = SHADOW ENABLE
0 = SHADOW DISABLE

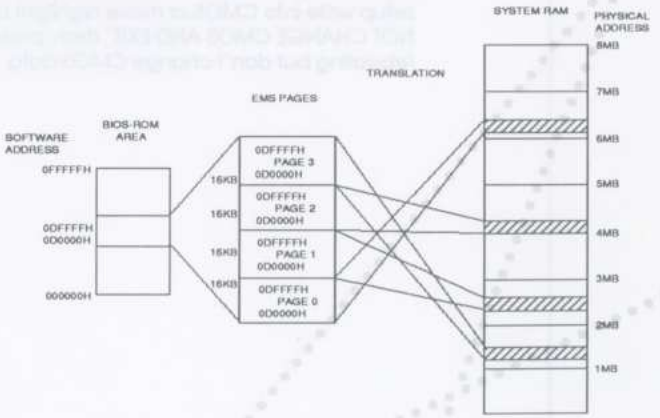
Use <PgUp> or <PgDn> to set this item to "1" and press <ESC> to return main menu.

Move highlight bar to the "WRITE CMOS REGISTERS AND EXIT" item, press <Enter> to rebooting and to let those setup write into CMOS.or move highlight bar to the "DO NOT CHANGE CMOS AND EXIT" item, press <Enter> to rebooting but don't change CMOS data.

5-9 EMS ADDRESS TRANSLATION LOGIC

Expanded Memory System or EMS is a memory mapping scheme used to map a 64 Kbyte block of memory in the EPROM area D0000H-DFFFFH to anywhere in the 1 Mbyte 8 Mbyte area. This 64 Kbyte memory block is segmented into four 16 Kbyte pages. Through a translation cable, each 16 Kbyte segment can be mapped any where in the 1 Mbyte to 8 Mbyte area. Since the 82C212 uses the translation table in the EMS mode, address lines A14 to A22 are translatied by the appropriate EMS mapping register. Hence, this scheme does not require switching between user and protected mod. Figure 5.7 shows the EMS organization with a possible traslation scheme. It is possible for the 82C212 to map this 64Kbyte block to anywere in the 0 to 8 Mbyte area. However, it is desirable to map this block above the 1 Mbyte area in order to not use the RAM space in the 0 to 640 K byte area. Although the EMS scheme translates the 64 Kbyte block in the D0000H-DFFFFH area, it is possible to select a 64K byte block from any other area.

◆ *FIGURE 5.7*
EMS MAPPING



5-10 MEMORY CONFIGURATION

The possible configurations for onboard memory are listed in the table 5.24, each bank is 16 bits wide plus two bits for parity.

◆ *TABLE 5.24 MEMORY CONFIGURATION*

	DRAM Type				Total	EMS
	BANK0	BANK1	BANK2	BANK3	Memory	Range
1	0	0	0	0	disable	0
2	256K	0	0	0	512Kb	0
3	1M	0	0	0	2Mb	1Mb to 2Mb
4	256K	64K	0	0	640Kb	0
5	256K	256K	0	0	1Mb	1Mb to 1.384Mb
6	1M	1M	0	0	4Mb	1Mb to 4Mb
7	256K	256K	256K	0	1.5Mb	1Mb to 1.5Mb
8	256K	256K	1M	0	3Mb	1Mb to 3Mb
9	1M	1M	1M	0	6Mb	1Mb to 6Mb
10	256K	64K	256K	256K	1.64Mb	1Mb to 1.64Mb
11	256K	256K	256K	256K	2Mb	1Mb to 2Mb
12	256K	64K	1M	1M	4.64Mb	1Mb to 4.64Mb
13	256K	256K	1M	1M	5Mb	1Mb to 5Mb
14	1M	1M	1M	1M	8M	1Mb to 8Mb

Page/interleaving is possible for only those combinations with similar pairs of DRAMs. In table 5.24, page/interleaving is possible with combinations 5,6,11,13 and 14.

5-11 I/O ADDRESS MAP

◆ *TABLE 5.25 I/O ADDRESS MAP*

I/O ADDRESS	FUNCTIONS
000-01F	DMA CONTROLLER 1, 8237
020-03F	INTERRUPT CONTROLLER, 8259A, MASTER
040-05F	TIMER 8254-2
060-06F	KEYBOARD CONTROLLER, 8742
070-07F	REAL-TIME CLOCK, NON-MASKABLE INTERRUPT MASK
080-09F	DMA PAGE REGISTERS 74LS612
0A0-0BF	INTERRUPT CONTROLLER 2, 8259, SLAVE
0C0-0DF	DMA CONTROLLER 2, 8237
0F0	CLEAR MATH COPROCESSOR BUSY
0F1	RESET MATH COPROCESSOR
0F8-0FF	MATH COPROCESSOR
1F0-1F8	FIXED DISK
200-207	GAME I/O
278-27F	PARALLEL PRINTER PORT 2
2F8-2FF	SERIAL PORT 2
300-31F	PROTOTYPE CARD
360-36F	PC NETWORK
378-37F	PARALLEL PRINTER PORT 1
380-38F	SDLC, BISYNCHRONOUS 2
3A0-3AF	SDLC, BISYNCHRONOUS 1
3B0-3BF	MONOCHROME DISPLAY AND PRINTER ADAPTER
3C0-3CF	RESERVED
3D0-3DF	COLOR GRAPHICS DISPLAY ADAPTER
3F0-3F7	DISK DRIVE CONTROLLER
3F8-3FF	SERIAL PORT 1

5-12 DIRECT MEMORY ACCESS (DMA)

The DMA controller is for quick data transfer between the disk drive, adaptor cards, and memory by transferring blocks of data at one time, thus free the microprocessor for other tasks.
The system supports seven DMA channels. The DMA channels are assigned as follows:

CTRL 1	CTRL 2
Ch0 - Spare	Ch4 - Cascade for CTRL 1
Ch1 - SDLC	Ch5 - Spare
Ch2 - Diskette	Ch6 - Spare
Ch3 - Spare	Ch7 - Spare

Channels 0 through 3 are contained in DMA controllers 1. These channels support 8-bit data transfers between 8-bit I/O adapters and 8- or 16-bit-system memory. Each channel can transfer data in 64K blocks throughout the 16-megabyte system address space.

Channels 4 through 7 are contained in DMA controller 2 Channel 4 is used to cascade DMA CTRL 1 to microprocessor. Channels 5, 6 and 7 can transfer only words in 128K bytes blocks in even-byte boundaries. These channels are to be used with only 16-bit devices.

The address for page register are as follows:

◆ *TABLE 5.26 PAGE REGISTER ADDRESS*

PAGE REGISTERS		I/O HEX ADDRESS
DMA	CHANNEL 0	0087
	1	0083
	2	0081
	3	0082
	5	008B
	6	0089
	7	008A
REFRESH		008F

Address generation for DMA channels is as follows:

For DMA channels 3 through 0

Source	DMA Page Registers	8237A-5
Address	A23 ..... A16	A15 - A0

NOTE: To generate the addressing signal. 1byte high enable (BHE), by inverting address line A0 for DMA channels 7 through 5.

For DMA channels 7 through 5

Source	DMA Page Registers	8237t-5
Address	A23 ..... A17	A16 - A1

NOTE: The 'BHE' and 'A0' addressing signals are forced to a logic 0. DMA channel addresses do not increase or decrease through page boundaries (64KB for channels 0 through 3 and 128KB for channel 5 through 7)

DMA controller registers are listed as follows:

◆ *TABLE 5.27 DMA CONTROLLER REGISTER*

HEX ADDRESS	COMMAND CODES
0C0	CH0 base and current address
0C2	CH0 base and current word count
0C4	CH1 base and current address
0C6	CH1 base and current word count
0C8	CH2 base and current address
0CA	CH2 base and current word count
0CC	CH3 base and current address
0CE	CH3 base and current word count
0D0	Read Status Reg./Write Command Reg.
0D2	Write Request Reg.
0D4	Write Single Mask Register Bit
0D6	Write Mode Register
0D8	Clear Byte Pointer Flip-Flop
0DA	Read Temporary Reg./Write Master Clear
0DC	Clear Mask Register
0DE	Write All Mask Reg. Bits

5-13 SYSTEM TIMERS

The system has three programmable timer/counters controlled by an Intel 8254-2 timer/counter chip. These are channels 0 through 2, defined as follows:

CHANNEL 0	SYSTEM TIMER
GATE 0	Tied on
CLK IN 0	1.190 MHz OSC
CLK OUT 0	8259A IRQ 0

CHANNEL 1	REFRESH REQUEST GENERATOR
GATE 1	Tied on
CLK IN 1	1.190 MHz OSC
CLK OUT 1	Request Refresh Cycle

NOTE: Channel 1 is programmed to generate a 15-second period signal.

CHANNEL 2	REFRESH REQUEST GENERATOR
GATE 2	Controlled by bit 0 of port hex 61, PP1 bit
CLK IN 2	1.190 MHz OSC
CLK OUT 2	Used to drive the speaker

The 8254-2 timer/counter is treated by system programs as an arrangement of four programmable external I/O ports. Three are treated as counters; the fourth is a control register for mode programming.

5-14 SYSTEM INTERRUPTS

Sixteen levels of system interrupts are provided by the 80286 NMI and two 8259A Interrupt Controller Chips. The following shows the interrupt-level assignments in decreasing priority:

LEVEL	FUNCTION	
Microprocessor NMI		Parity or I/O channel check
Interrupt Controllers		
CTLR 1	CTLR 2	
IRQ 0		Timer output 0
IRQ 1		Keyboard (Output buffer full)
IRQ 2		Interrupt from CTLR 2
	IRQ8	Realtime clock interrupt
	IRQ9	Software redirected to INT 0AH (IRQ2)
	IRQ10	Reserved
	IRQ11	Reserved
	IRQ12	Reserved
	IRQ13	Coprocessor
	IRQ14	Fixed disk controller
	IRQ15	Reserved
IRQ 3	Serial port 2	
	IRQ4	Serial port 1
	IRQ5	Parallel port 2
	IRQ6	Diskette controller
	IRQ7	Parallel port 1

5-15 I/O CHANNEL

A. SLOT

The following charts summerize pin assignments for the I/O channel connectors:

A-SIDE SLOT 1 THROUGH SLOT 8

I/O PIN	SIGNAL NAME	INPUT/OUTPUT
A 1	I/O CH CK	I
A 2	SD7	I/O
A 3	SD6	I/O
A 4	SD5	I/O
A 5	SD4	I/O
A 6	SD3	I/O
A 7	SD2	I/O
A 8	SD1	I/O
A 9	SD0	I/O
A 10	I/O CH RDY	I
A 11	AEN	O
A 12	SA19	I/O
A 13	SA18	I/O
A 14	SA17	I/O
A 15	SA16	I/O
A 16	SA15	I/O
A 17	SA14	I/O
A 18	SA13	I/O
A 19	SA12	I/O
A 20	SA11	I/O
A 21	SA10	I/O
A 22	SA9	I/O
A 23	SA8	I/O
A 24	SA7	I/O
A 25	SA6	I/O
A 26	SA5	I/O
A 27	SA4	I/O
A 28	SA3	I/O
A 29	SA2	I/O
A 30	SA1	I/O
A 31	SA0	I/O

B-SIDE SLOT 1 THROUGH SLOT 8

I/O PIN	SIGNAL NAME	INPUT/OUTPUT
B 1	GND	GROUND
B 2	RESET DRV	0
B 3	+ 5 VDC	POWER
B 4	IRQ 9	I
B 5	- 5 VDC	POWER
B 6	DRQ 2	I
B 7	-12 VDC	POWER
B 8	OWS	I
B 9	+ 12	POWER
B 10	GND	POWER
B 11	-SMEMW	O
B 12	-SMEMR	O
B 13	-IOW	I/O
B 14	-IOR	I/O
B 15	-DACK3	O
B 16	DRQ3	I
B 17	-DACK1	O
B 18	DRQ1	O
B 19	-REFRESH	I/O
B 20	CLK	O
B 21	IRQ7	I
B 22	IRQ6	I
B 23	IRQ5	I
B 24	IRQ4	I
B 25	IRQ3	I
B 26	-DACK2	O
B 27	T/C	O
B 28	BALK	O
B 29	+ 5 VDC	POWER
B 30	OSC	O
B 31	GRD	GROUND

C-SIDE SLOT 9 THROUGH SLOT 16

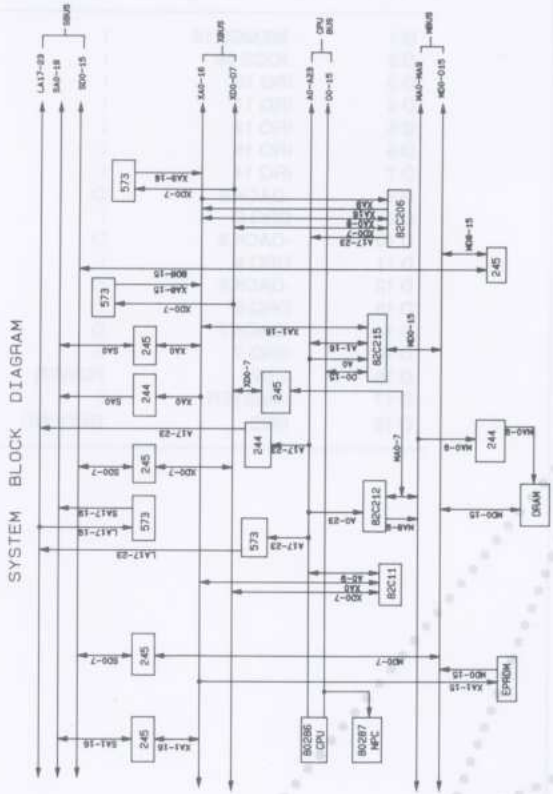
I/O PIN	SIGNAL NAME	INPUT/OUTPUT
C 1	SBHE	I/O
C 2	LA23	I/O
C 3	LA22	I/O
C 4	LA21	I/O
C 5	LA20	I/O
C 6	LA19	I/O
C 7	LA18	I/O
C 8	LA17	I/O
C 9	-MEMR	I/O
C 10	-MEMW	I/O
C 11	SD08	I/O
C 12	SD09	I/O
C 13	SD10	I/O
C 14	SD11	I/O
C 15	SD12	I/O
C 16	SD13	I/O
C 17	SD14	I/O
C 18	SD15	I/O

D-SIDE SLOT 9 THROUGH SLOT 16

I/O PIN	SIGNAL NAME	INPUT/OUPUT
D 1	-MEMCS 16	I
D 2	-IOCS 16	I
D 3	IRQ 10	I
D 4	IRQ 11	I
D 5	IRQ 12	I
D 6	IRQ 15	I
D 7	IRQ 14	I
D 8	-DACK 0	O
D 9	DRQ O	I
D 10	-DACK 5	O
D 11	DRQ 5	I
D 12	-DACK 6	O
D 13	DRQ 6	I
D 14	-DACK 7	O
D 15	DRQ 7	I
D 16	+ 5V	POWER
D 17	-MASTER	I
D 18	GND	GROUND

5-16 SYSTEM BLOCK DIAGRAM

◆ *FIGURE 5.8 SYSTEM BLOCK DIAGRAM*



◆ *FIGURE 5.9 JUMPERS / CONNECTORS LOCATION*