Version 1.0

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Mainboard Name: MS-6107
Manual Rev: 1.0
BIOS Version: W18X
Release Date: May, 1996

FCC-B Radio Frequency Interference Statement

This equipment has been tested and found to comply with the limits for a class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Notice 1
The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Notice 2
Shielded interface cables and A.C. power cord, if any, must be used in order to comply with the emission limits.

VOIR LA NOTICE D'INSTALLATION AVANT DE RACCORDER AU RESEAU.

Edition

November 1996

Trademarks

Table of Contents

About This Manual

Welcome to the Microstar MS-6107 mainboard.

Before you begin using the MS-6107 product, read this manual for installation instructions, new features in the product, and other important information. This manual provides both instructional and reference material to help you get the most from the MS-6107. It consists of the following:

Descriptions of the features availability and specifications concerning the MS-6107 mainboard.
Installation instructions for setting up the MS-6107 board.
Instructions and information on setting up the BIOS.

About the MS-6107 Package

The MS-6107 package consists of the following items:

MS-6107 Mainboard
1 floppy disk drive ribbon cable
1 IDE ribbon connector cable
Optional Pentium Pro Processor and FAN with heat sink

If your package does not include all the items on the checklist or has damaged pieces, contact your dealer.

Chapter 1

Introduction

The PCI P6 NA7 PCI/ISA system board is a high-performance personal computer system board based on the Pentium™ Pro microprocessor.

The system board utilizes the Intel® 82440FX PCI Chipset which has high integration and provides all system control functions. In addition there is an on-chipset USB and IDE controller which supports IDE PIO/Bus Master operation mode for IDE HDD/CD-ROM. The PIO mode Supports Mode 0, 1, 2, 3 and 4 with a transfer rate up to 22 MB per/sec.

1.1 System Board Specifications

CPU:

- 2 ZIF type 8 sockets for Dual Intel® Pentium™ Pro microprocessors. Each microprocessor has its own Core/Bus ratio jumper Core/Bus ratios are x2, x3, x4, x5, x2.5, x3.5, x4.5, x5.5.

VRM:

- VRM (Voltage Regulator Module) is on board. It provides power for the processor. The adjustment mechanism is controlled by the four weighted input (VID0-VID3) from the processor.

Chip Set:

- Intel® 82440FX PCI Chipset.

Clock Generator:

- There are two clocks, 60MHz/66.6MHz. Both meet Pentium™ Pro microprocessor and NATOMA (82440FX) Chipset specifications.

Main Memory:

- Supports SIX memory banks using six 72-pin SIMM sockets.
- Up to 768 Mbytes main memory.
- Supports Fast Page (FP) Mode, Extended Data Output (EDO) Mode, and Burst Extended Data Output (BEDO) Mode DRAM.

Slots:

- Five 32-bit PCI Bus slots and three 16-bit ISA bus slots. One shared slot that can be used as ISA or PCI.

On-Board Peripherals:

- On-Board peripherals include:
  —1 floppy port supports 2 FDD
  —2 serial ports (ComA + ComB)
  —1 parallel port supports SPP, EPP or ECP mode

—1 FDD port that supports 2 FDDs with 360K, 720K, 1.2M, 1.44M, and 2.88Mbytes per second transfer rate.

On-Board IDE:

- An IDE controller on the Intel® 82440FX PCI Chipset provides IDE HDD/CD-ROM with PIO and Bus Master Operation Mode. The PIO Mode supports modes 0, 1, 2, 3, and 4, with a transfer rate of 22 Mbytes second.

On-Board USB:

- 2 port USB features on the Intel® 82440FX PCI Chipset.

RTC:

- Non-Volatile RTC with 114 bytes of CMOS RAM.

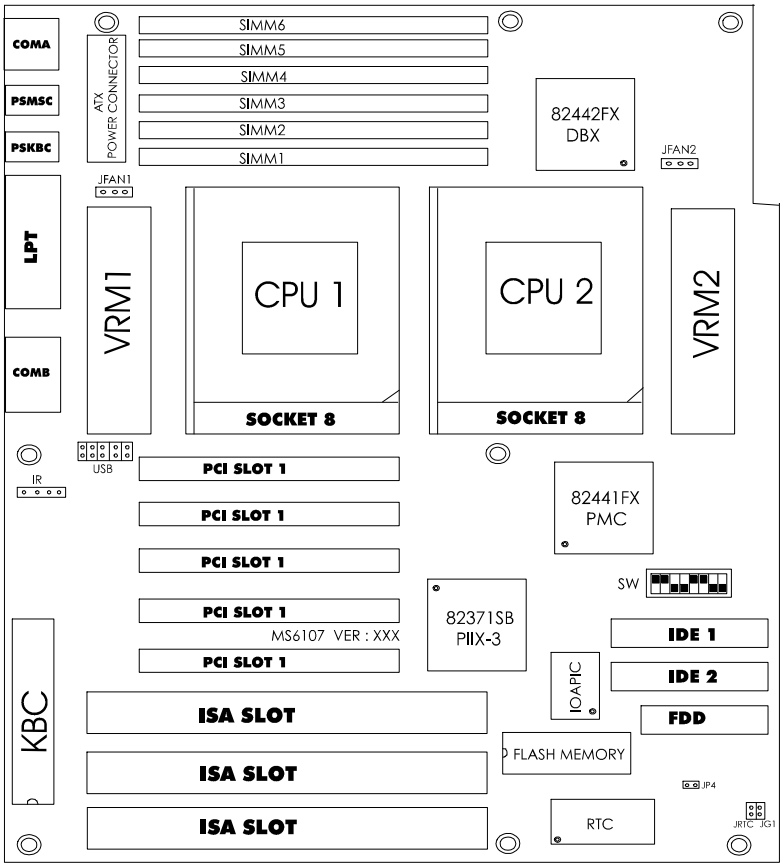
Dimensions

- ATX form factor 30cm(L)X26cm(W); 6 layer PCB

Mounting

- 8 mounting holes

1.2 System Board Layout



MS-6107

Chapter 2

HARDWARE INSTALLATION

It is important to set jumpers correctly. Improper setting will cause system instability, destruction of components, and/or system hang-up

System Speed Selection: SW

The system board have reserved all possible core/bus ratio. Please see as below **figure** 2-1 and **table** 2-1.

Figure 2-1

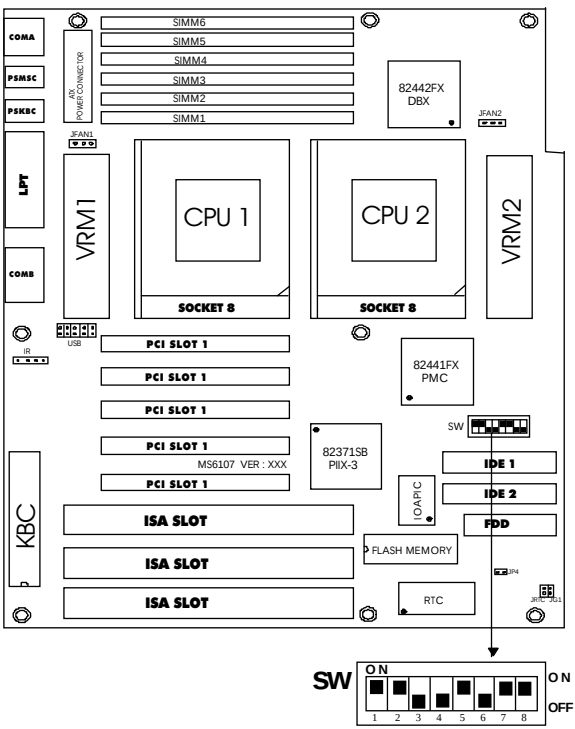
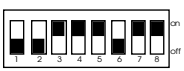


Table 2-1

CPU SPEED	SW SETTING	REMARK
150 MHZ		BUS CLOCK = 60MHZ CORE/BUS RATIO = 2.5
167 MHZ		BUS CLOCK = 66.6MHZ CORE/BUS RATIO = 2.5
180 MHZ		BUS CLOCK = 60MHZ CORE/BUS RATIO = 3
200 MHZ		BUS CLOCK = 66.6MHZ CORE/BUS RATIO = 3
233 MHZ		BUS CLOCK = 66.6MHZ CORE/BUS RATIO = 3.5

CMOS RAM CLEAR: JRTC

The system board configuration is stored in RTC's CMOS RAM. If you need to clear the system board configuration the process depends on whether or not the RTC type can be cleared or not. If the RTC is clearable then do the following:

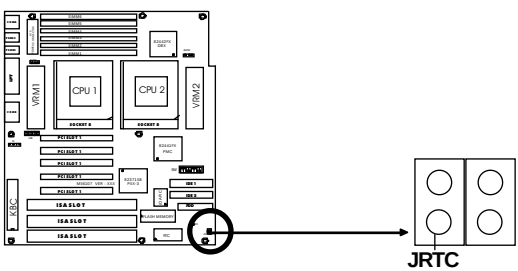
1. DALLAS's DS12887A-----Clear RTC while power is off.
    a. Turn power off.
    b. Short jumper JRTC.
    c. Turn power on.
    d. Enter the BIOS setup program to re-set up th system configuration.
    e. Reboot the system.

Note: *DALLAS DS12887 has no function for clearing.*

2. BENCHMARQ's BQ3287AMT-----Clear RTC while power is on.

    a. Turn power on.
    b. Short jumper JRTC, then open it.
    c. Reset the system by:
        - Turn off power then on.
        - Warm reset (PRESS Ctrl + Alt + Delete).
        - Use the reset button.
    d. Enter the BIOS setup program to reset the system configuration.
    e. Reboot the system.

Note: *BENCHMARQ's BQ3287 has no function for clearing.*



DRAM Population Rules

In order to create a memory array, certain rules must be followed.
The following set of rules allows optimum configuration.

1. DRAM modules must be populated in pairs; the memory array is 64 or 72 bits wide.
2. DRAM modules can be populated in any order(i.e. SIMM1/2 does not have to be populated before SIMM 3/4 are used).
3. DRAM modules pairs need to be populated with the same densities(single or double). For example, SIMM1/2 sockets must be populated with identical densities, but SIMM3/4 and SIMM5/6 sockets can be populated with different densities. In addition Asymmetric DRAMs of the same type should be used in a whole row.
4. BEDO, EDO, FP modes can be mixed in the memory array, but only one type should be used per SIMM socket pair. For example SIMM1/2 sockets can be populated with EDO while SIMM3/4 can be populated with FP mode type DRAM.
5. DRAM timing which provides the DRAM speed grade control for the entire memory array must be programmed to use the timing of the slowest DRAM that is currently installed.

Note: *1. Before using DRAM modules, make sure that the modules used is the same as in the chart next page.*
2. To use the ECC(Error Code Correct) function, a SIMM module with parity support must be used. You can turn on the ECC function in the BIOS setup

CHAPTER 2 HARDWARE INSTALLATION

System Memory Installation: SIMM6-SIMM1

To ease the user's difficulty, we're going to explain about the 72 pin SIMM DRAM Module. If the user's already familiar with this, you could skip this section. The 72 pin SIMM DRAM module are divided into two: single density and double density, each side may have 32-bits data and/or 4 parity bits(depends on what parity you have). Nowadays, DRAM Vendor only market 256Kbit, 1Mbit, 4Mbit, 8Mbit, 16Mbit and 64 Mbit DRAM chip with different density(256Kb and 1Mb are already very scarce in the market). DRAM chip with the same density may have different memory bank configuration. Lets take the density of 16Mbit may be 16MX1, 4MX4, 2MX8 or 1MX16. Please refer to the next page for the DRAM chip density, organization and SIMM module oraganization.

Fig. 2-2 DRAM Chip Density & Organization

DRAM chip density	Organization (words X bits)	Address Mode			refresh cycle	440 FX supports
		mode	# of row address	# of column address		
4Mb	1MX4	SYMM	10	10	1024	YES
	4MX1	SYMM	11	11	1024	YES
16Mb	16MX1	SYMM	12	12	4096	YES
	4MX4	SYMM	11	11	2048	YES
	2MX8	ASYMM	11	11	2048	YES
	1MX16	ASYMM	10	10	1024	YES
64Mb	16MX4	ASYMM	13	11	4096	NO
		SYMM	12	12	4096	YES
	8MX8	ASYMM	13	10	4096	NO
		ASYMM	12	11	4096	YES

Note: **SYMM** = symmetric **ASYMM** = asymmetric
If the Row address of the DRAM Chips equals the Column address then it's in the symmetric mode, otherwise it's in the asymmetric mode.

Fig. 2-3 72 Pin SIMM Module Density & Memory Size

Data DRAM Chip Density		Parity DRAM Chip Density	Module Organization				MB/SIMM	
			Single Side		Double Side			
			# of Data DRAM Chip	# of Parity DRAMChip (if have)	# of Data DRAM Chip	# of Parity DRAMChip (if have)	Single Side (S)	Double Side (D)
4Mb	1MX4	1MX1	8	4	16	8	4MB	8MB
	4MX1	4MX1	32	4	64	8	16MB	32MB
16Mb	16MX1	16MX1	32	4	64	8	64MB	128MB
	4MX4	4MX1	8	4	16	8	16MB	32MB
	2MX8	-	4	-	8	-	8MB	16MB
	1MX16	1MX1	2	4	4	8	4MB	8MB
64Mb	16MX4	16MX1	8	4	16	8	64MB	128MB

Note: **b** = bit **B** = byte

CHAPTER 2 HARDWARE INSTALLATION

DRAM Memory Installation

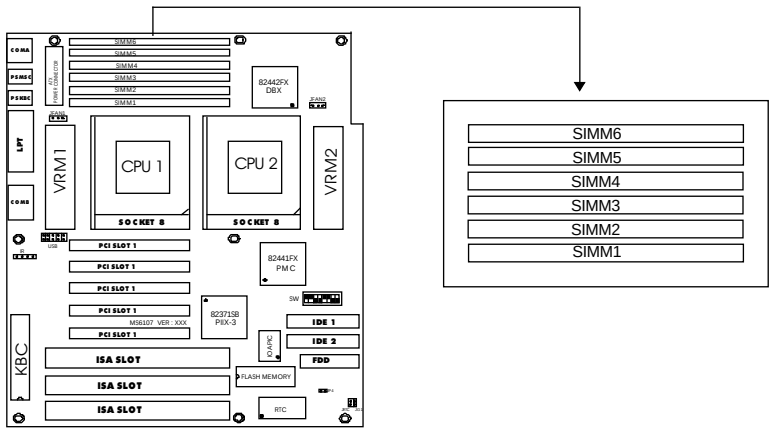


Table 2-4

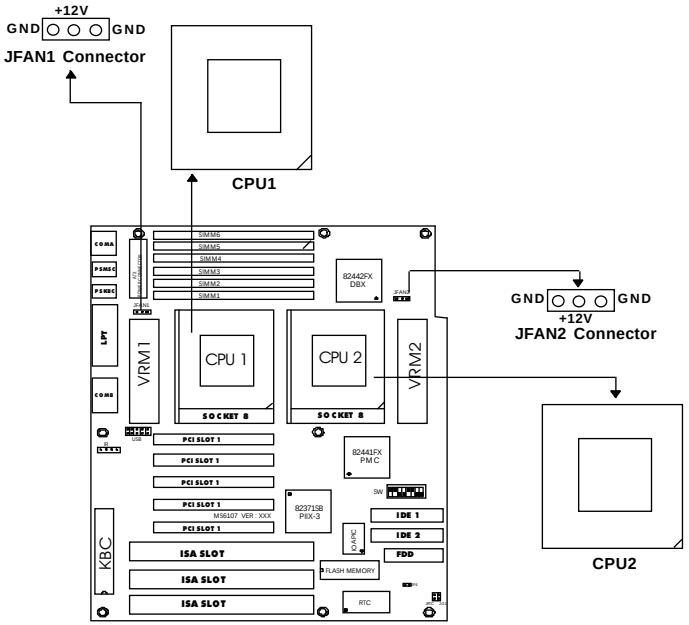
SIMM6	SIMM5	SIMM4	SIMM3	SIMM2	SIMM1
-	-	-	-	D/S	D/S
-	-	D/S	D/S	D/S	D/S
D/S	D/S	D/S	D/S	D/S	D/S
D/S	D/S	-	-	-	-
D/S	D/S	D/S	D/S	-	-

Module Population Rules

CHAPTER 2 HARDWARE INSTALLATION

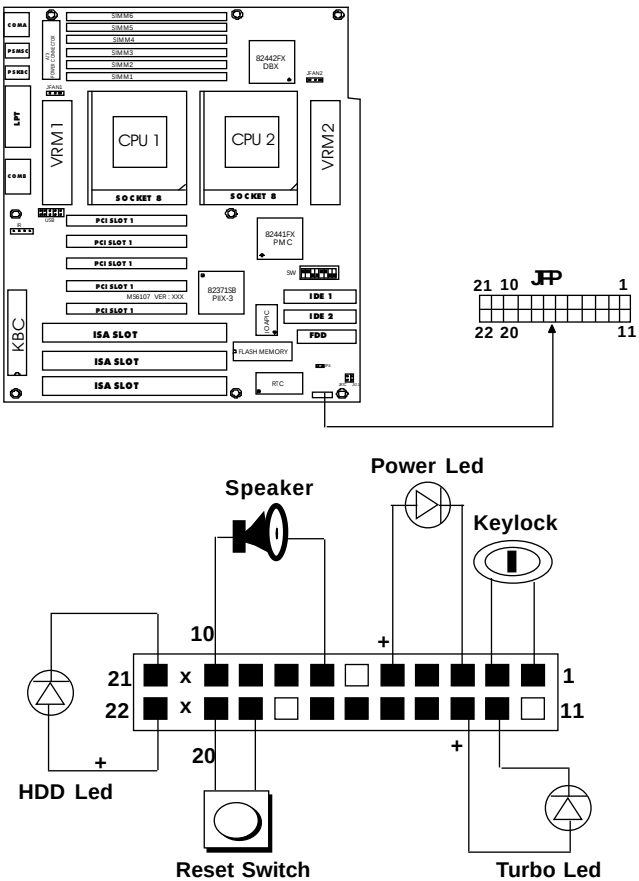
CPU Installation & Fan Power Connector: JFAN1, JFAN2

Open Socket 8 by pulling the lever away from the socket then upwards at a 90 degree right angle. Insert the CPU according to the orientation as shown. If it does not fit in easily, then try to move it in different direction, because the CPU pin configuration only fits one way as opposed to earlier CPUs. Make sure that the CPU is well seated, then close the lever. See the figure below:



Case Block Connector: JFP

The Turbo LED, Turbo switch, Hardware Reset, Key lock, Power LED, Speaker and HDD LED are all connected to the JFP connector block as shown below;

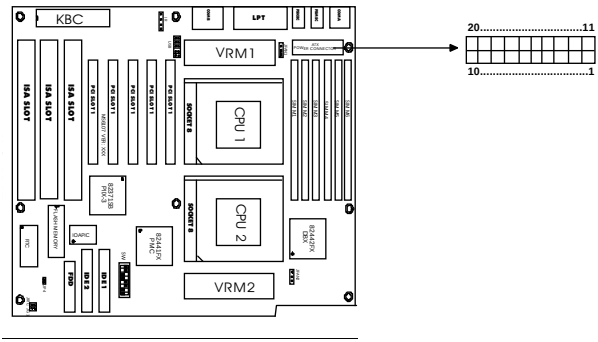


Note: *The hardware Turbo switch is non-functional, but it could be controlled by software Turbo/Deturbo*

CHAPTER 2 HARDWARE INSTALLATION

Power Supply Connector: PWR20

The power supply connector is a 20-pin ATX power connector. Connectors from the power supply can fit only in one direction as shown in the diagram below:

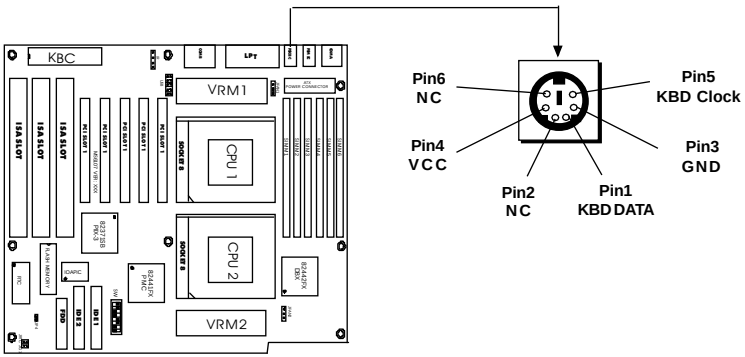


ATX Power Connector Pin Description

20	19	18	17	16	15	14	13	12	11
5V	5V	-5V	GND	GND	GND	PS_ON	GND	-12V	3.3V
12V	5V_SB	PW_Ok	GND	5V	GND	5V	GND	3.3V	3.3V
10	9	8	7	6	5	4	3	2	1

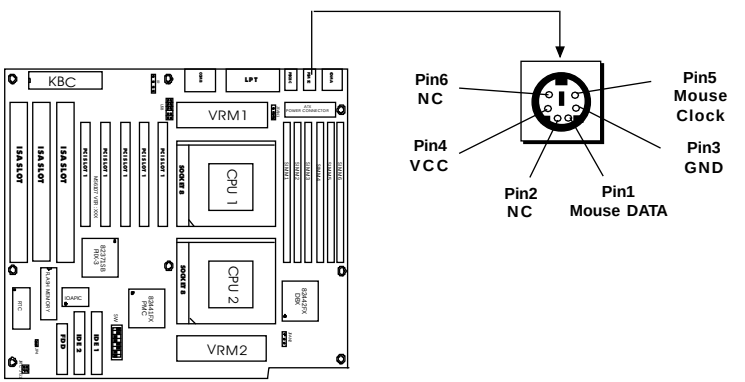
Keyboard Connector: PSKBC

The system board provides a standard PS/2 style keyboard mini DIN connector for attaching a keyboard. You can plug a keyboard cable directly to this connector.



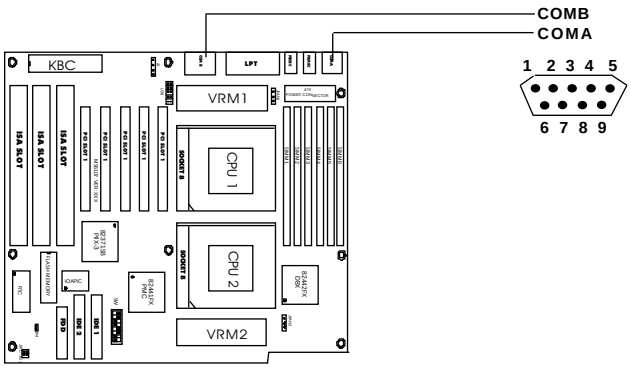
Mouse Connector: PSMSC

The system board provides a standard PS/2 style mouse mini DIN connector for attaching a PS/2 style mouse. You can plug a PS/2 style mouse directly into this connector. The connector location and pin definition as shown below:



Serial Port Connectors: COMA & COMB

The system board has two 9-pin male DIN connectors for serial ports COMA and COMB. These two ports are 16550A high speed communication ports that send/receive 16 bytes FIFOs. You can attach a mouse or a modem cable directly into these connectors.

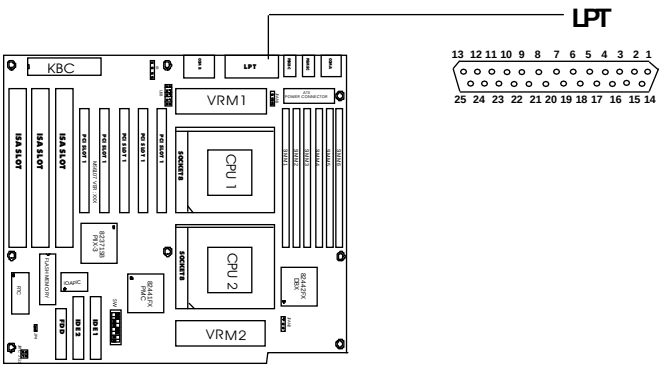


PIN DEFINITION

Pin #	Definition
1	**DCD**(Data Carry Detect)
2	**SIN**(Serial In or Receive Data)
3	**SOUT**(Serial Out or Transmit Data)
4	**DTR**(Data Terminal Ready)
5	**GND**
6	**DSR**(Data Set Ready)
7	**RTS**(Request To Send)
8	**CTS**(Clear To Send)
9	**RI**(Ring Indicate)

Parallel Port Connectors: LPT

The system board provides a 25 pin female centronic connector for LPT. A parallel port is a standard printer port that also supports Enhanced Parallel Port(EPP) and Extended capabilities Parallel Port(ECP). See connector and pin definition below:



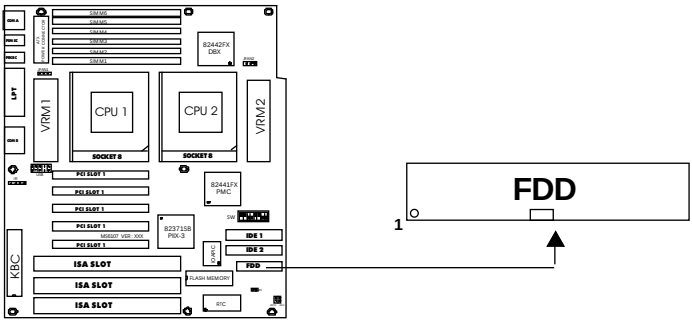
PIN DEFINITION

PIN #	DEFINITION	PIN #	DEFINITION
1	STROBE	14	AUTO FEED#
2	DATA0	15	ERR#
3	DATA1	16	INIT#
4	DATA2	17	SLIN#
5	DATA3	18	GND
6	DATA4	19	GND
7	DATA5	20	GND
8	DATA6	21	GND
9	DATA7	22	GND
10	ACK#	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SELECT		

CHAPTER 2 HARDWARE INSTALLATION

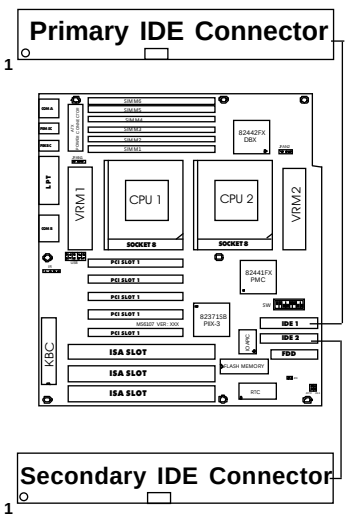
Floppy Disk Connector: FDD

The system board also provides a standard floppy disk connector FDD that supports 360K, 720K, 1.2M, 1.44M and 2.88M floppy disk types. You can attach a floppy disk cable directly to this connector.



Hard Disk Connector: IDE1 & IDE2

The system board has a 32-bit Enhanced PCI IDE Controller that provides for two HDD connectors IDE1(primary) and IDE2(secondary). You can connect up to four hard disk drives or other devices to IDE1 and IDE2.



IDE1(primary IDE connector)

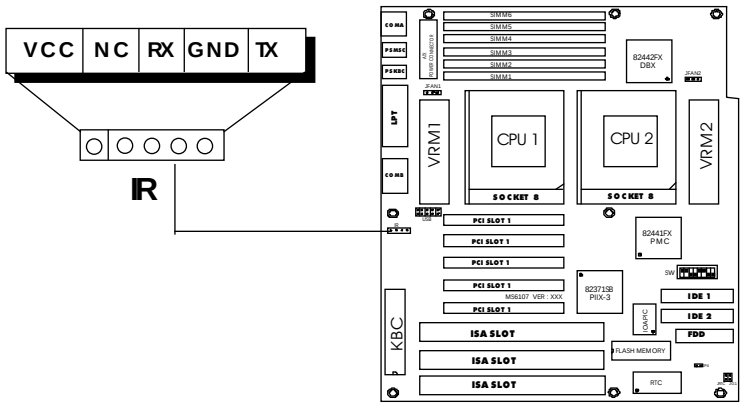
The first hard disk should always be connected to IDE1. IDE1 can connect a Master and a Slave drive.

IDE2(secondary IDE connector)

IDE2 can connect a Master and a Slave drive.

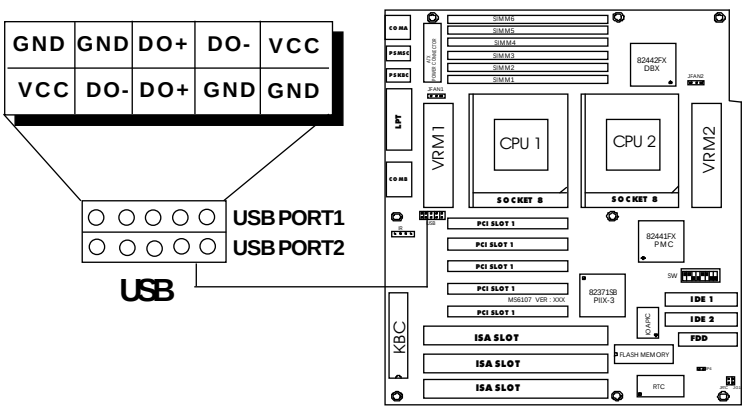
IrDA Infrared Module Connector: IR

The system board provides a 5-pin infrared connector(IR) for IR module.



USB Connector: USB

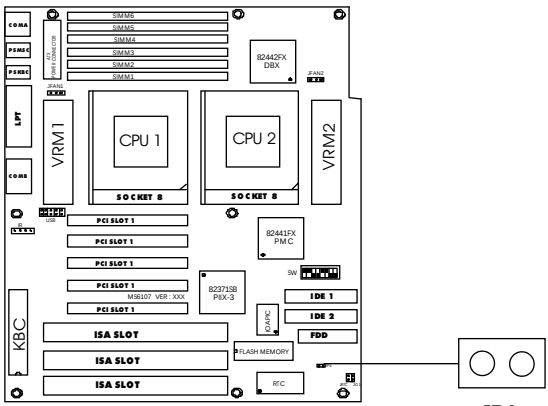
This 10-pin connector supports USB devices.



CHAPTER 2 HARDWARE INSTALLATION

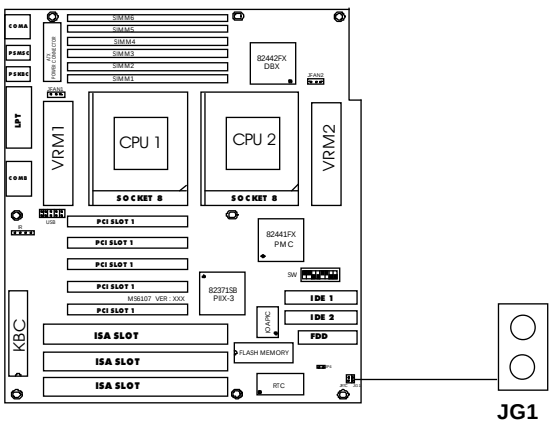
Power Switch: JP4

The 2 -pin connector must utilize a toggle swtich (one push on/ second push off).



Power Saving Switch: JG1

Attaching a power saving switch to this connector will allow the system into sleep mode whenever the switch is pressed.



CHAPTER 3 AMI BIOS USER'S GUIDE

Chapter 3

AMI BIOS USER GUIDE

The system configuration information and chipset register information is stored in the CMOS RAM. This information is retained by a battery when the power is off. Enter the BIOS setup (if need) to modify this information.

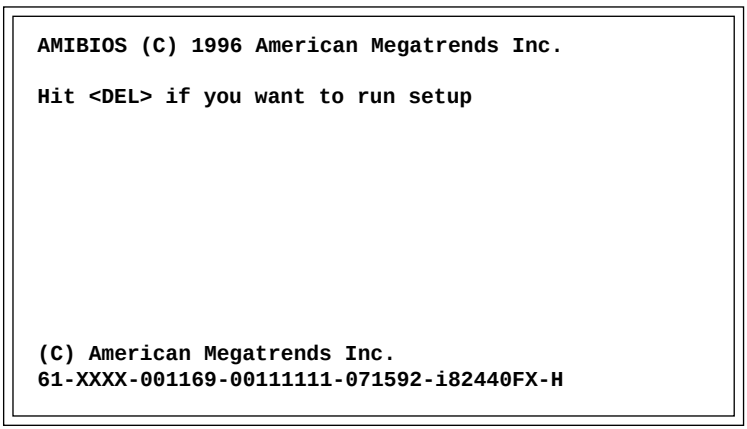
The following pages will describe how to enter BIOS setup, and all about options.

CHAPTER 3 AMI BIOS USER'S GUIDE

3.1 Enter BIOS Setup

Enter the AMI setup Program's Main Menu as follows:

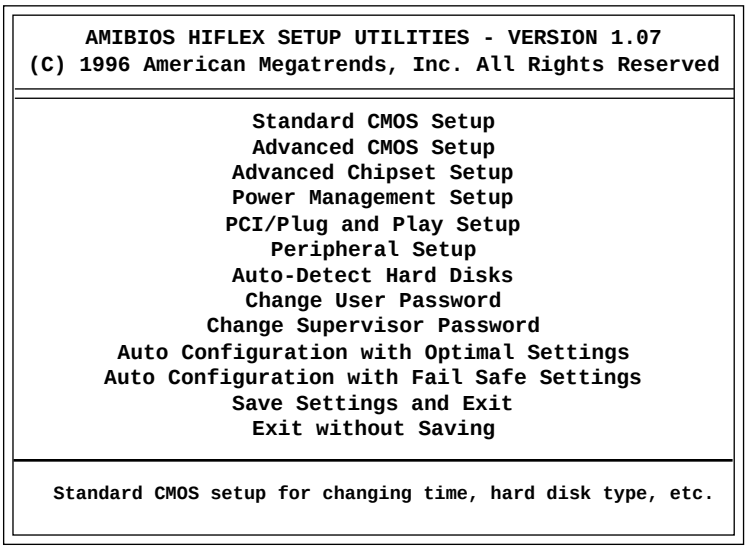
1. Turn on or reboot the system. The following screen appears with a series of diagnostic check.



2. When the "Hit <DEL>" message appears, press <DEL> key to enter the BIOS setup screen.

3. After pressing <DEL> key, the BIOS setup screen will appear.

Note: *If you don't want to modify CMOS original setting, then don't press any key during the system boot.*



4. Using the <Up> and <Down> key to move the highlight scroll up or down.

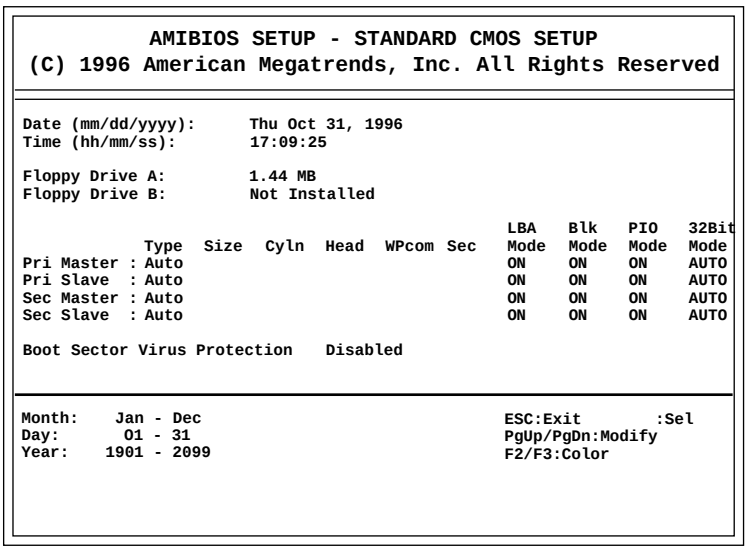
5. Using the <ENTER> key to select the option.

6. To exit press <ESC>, to save and exit press <F10>.

7. Section 3.2 to 3.7 will explain the option in more details.

3.2 Standard CMOS Setup

1. Press <ENTER> on "Standard CMOS Setup" of the main menu screen .

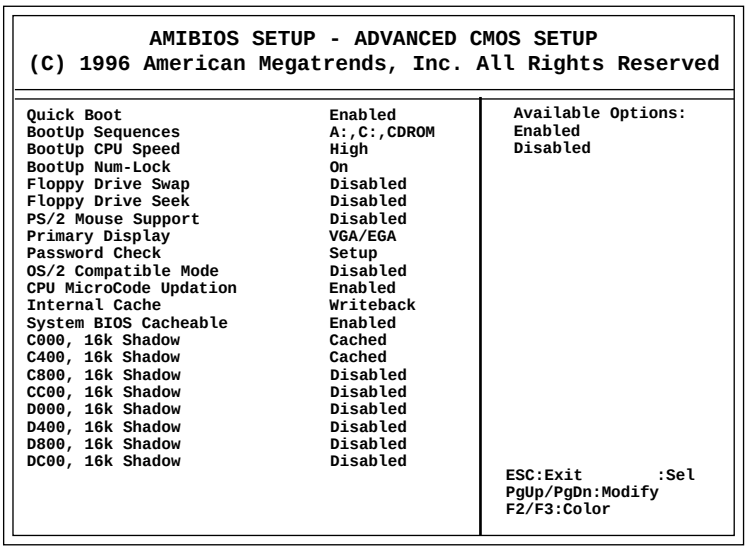


2. Using <Up> and <Down> to choose the item and <PgUp> and <PgDn> keys to modify the highlighted item.

3. After you have finished with the Standard CMOS Setup, press <ESC> to go back to the main menu.

3.3 Advanced CMOS Setup

1. Press <ENTER> on "Advanced CMOS Setup" of the main menu screen.



2. Using <Up> and <Down> to choose the item and <PgUp> and <PgDn> keys to modify the highlighted item.

3. After you have finished with the Advanced CMOS Setup, press <ESC> to go back to the main menu.

Description of the item on screen follows:

Quick Boot

Set this option to Enabled to permit AMIBIOS to boot within 5 seconds. This option replaces the old ABOVE 1 MB Memory Test option. The Optimal default setting is Enabled. The Fail-Safe default setting is Disabled.

Boot Up Sequence

This option sets the sequence of boot drives (floopy drive A:, hard disk drive C:, or a CD-ROM drive) that AMIBIOS attempts to boot from after AMIBIOS POST completes. The settings are C:, A:, CD-ROM, A:, C:, CD-ROM or CD-ROM, C:, A:,. The Optimal and Fail-safe default setting are C:, A:, CD-ROM.

Boot Up CPU Speed

This option sets the CPU speed when the computer boots. The settings are Low or High. The Optimal and Fail-Safe default settings are High.

Boot up Num Lock

When this option is set to Off, AMIBIOS turns off the Num Lock key when the system is powered on so the end user can use the arrow keys on both the numeric keypad and the keyboard. The settigs are On or Off. The optimal default and Fail-Safe default settings are On.

Floppy Drive Swap

Set this option to Enabled to specify that floppy drives A: and B: are swapped. The setting are Enabled and Disabled. The Optimal and Fail-Safe default settings are Disabled.

Floopy Drive Seek

When this option is set to Enabled, AMIBIOS performs a Seek command on floppy drive A: before booting the system. The settings are Enabled and Disabled. The Optimal and Fail-Safe default settings are Disabled.

PS/2 Mouse Support

When this option is set to Enabled, AMIBIOS supports a PS/2-type mouse. The settings are Enabled and Disabled. The Optimal and Fail-Safe default settings are Enabled.

Primary Display

This option configures the primary display subsytem in the computer. The settings are Mono(monochrome), 40CGA, 80CGA or VGA/EGA. The optimal and Fail-Safe default settings are VGA/EGA.

Password Check

This option specifies the type of AMIBIOS password protection that is implemented. The Optimal and Fail-Safe default settings are Setup.

OS/2 Compatible Mode

Set this option to Enabled to permit AMIBIOS to run properly if OS/2 or any other operating system does not support Plug and Play is to be run on this computer. The settings are Enabled or Disabled. The Optimal and Fail-safe default settings are Disabled.

CPU MicroCode Update

Set this option to Enabled to allow the CPU microcode to be updated. The settings are Enabled or Disabled. The Optimal and Fail-Safe default settings are Disabled.

Internal Cache

This option selects the type of caching algorithm used by AMIBIOS and the CPU for L1 cache memory(internal to the CPU). The settings are Writeback - a writeback algorithm is used, Write-through - a write-through algorithm is used or Disabled - AMIBIOS does not specify the type of caching algorithm. The algorithm is set by the CPU. The Optimal and Fail-Safe default settings are Writeback.

System BIOS Cacheable

AMIBIOS always copies the system BIOS from ROM to RAM for faster execution. Set this option to Enabled to permit the contents of the F0000h RAM memory segment to be written to and read from cache memory. The settings are Enabled or Disabled. The Optimal default setting is Enabled. The Fail-Safe default setting is Disabled.

C000, 16K Shadow/C400, 16k Shadow

These options specify how the contents of the video ROM are handled. The settings are:

Disabled - the Video ROM is not copied to RAM.

Cached - the contents of the video ROM are from C0000h - C7FFFh are not only copied from ROM to RAM; it can also be written to or read from cache memory.

Shadow - the Contents of the video ROM are from C0000h - C7FFFh are copied(shadowed) from ROM to RAM for faster execution.

The Optimal and Fail-Safe default setting is Cached.

C800, 16k Shadow/CC00, 16k Shadow/D000, 16K Shadow/D400, 16k Shadow/D800, 16k Shadow/DC00, 16K Shadow

These options specify how the contents of the adaptor ROM named in the option title are handled. The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards. The settings are;

Disabled - The specified ROM is not copied to RAM.

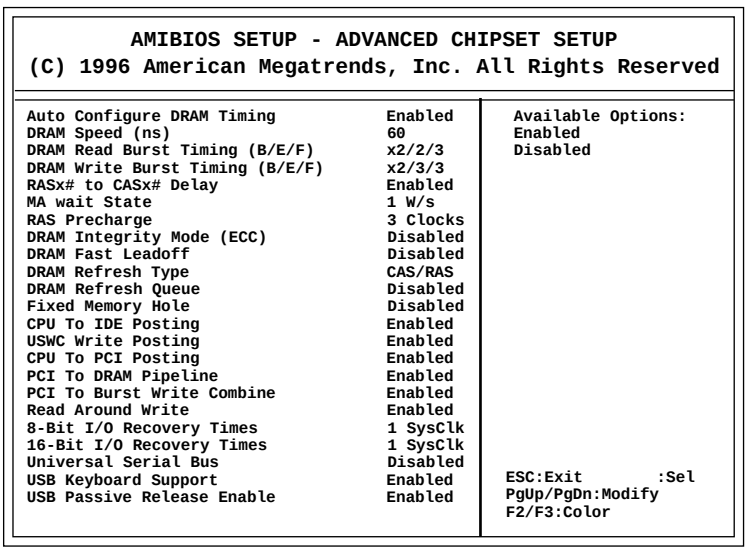
Cache - The contents of the ROM area are not only copied from ROM to RAM for faster execution, it can also be written to or read from cache memory.

Shadow - The contents of the ROM area are copied from ROM to RAM for faster execution.

The Optimal and Fail-Safe default settings are Disabled.

3.4 Advanced Chipset Setup

1. Press <ENTER> on "Advanced Chipset Setup" of the main menu screen.



```
        AMIBIOS SETUP - ADVANCED CHIPSET SETUP
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Auto Configure DRAM Timing          Enabled     Available Options:
DRAM Speed (ns)                     60          Enabled
DRAM Read Burst Timing (B/E/F)      x2/2/3      Disabled
DRAM Write Burst Timing (B/E/F)     x2/3/3
RASx# to CASx# Delay                Enabled
MA wait State                       1 W/s
RAS Precharge                       3 Clocks
DRAM Integrity Mode (ECC)           Disabled
DRAM Fast Leadoff                   Disabled
DRAM Refresh Type                   CAS/RAS
DRAM Refresh Queue                  Disabled
Fixed Memory Hole                   Disabled
CPU To IDE Posting                  Enabled
USWC Write Posting                  Enabled
CPU To PCI Posting                  Enabled
PCI To DRAM Pipeline                Enabled
PCI To Burst Write Combine          Enabled
Read Around Write                   Enabled
8-Bit I/O Recovery Times            1 SysClk
16-Bit I/O Recovery Times           1 SysClk
Universal Serial Bus                Disabled
USB Keyboard Support                Enabled     ESC:Exit        :Sel
USB Passive Release Enable          Enabled     PgUp/PgDn:Modify
                                                F2/F3:Color
```

2. Using <Up> and <Down> to choose the item and <PgUp> and <PgDn> keys to modify the highlighted item.

3. After you have finished with the Advanced Chipset Setup, press <ESC> to go back to the main menu.

Description of the item on screen follows:

Auto Configure DRAM Timing

Choose Enabled(default) will automatically configure the DRAM timing depends on "DRAM Speed" selection. Choose disable to customize setup.

DRAM Speed (ns)

This option specifies the RAS access time (in nanoseconds) for the DRAM used in the computer for system memory. The settings are 50,60 or 70. The Optimal and Fail-safe default settings are 70.

DRAM Read Burst Timing (B/E/F)

Choose DRAM read burst timing for the customize setup.
B stand for BEDO DRAM, E stand for EDO DRAM and F stand for FAST PAGE DRAM.

DRAM Write Burst Timing (B/E/F)

Choose DRAM write burst timing for the customize setup.

RASx# to CASx# Delay

Choose Enabled will insert 3 clock delay between the RASx# and CASx#. There will be 2 clock delay if disabled (default) is chosen.

MA Wait State

Choose Enabled, one additional wait state is inserted before the assertion of the first MA and CAS/RAS assertion during DRAM read or write leadoff cycles.

RAS Precharge

Choose the DRAM's RASx# precharge time.

DRAM Integrity Mode (ECC)

Set this option to Enabled to ECC(Error Checking and Correction) DRAM integrity mode. The settings are Enabled or Disabled. The Optimal and Fail-Safe default settings are Disabled.

Note: *To enable this function, you have to used SIMM w/Parity*

DRAM Fast Leadoff

Choose Enabled, one additional wait state is added to the DRAM leadoff timing for page/row miss cycles. The leadoff controls the MA setup to the first CASx# assertion.

DRAM Refresh Type

This option sets the type of system memory refresh that is used in the computer. The settings are RAS only or CAS/RAS (CAS before RAS refresh). The Optimal and Fail-Safe default settings are CAS/RAS.

DRAM Refresh Queue

Choose Enabled, the system will provides 4-deep refresh queue. All refresh request are queued, with the 4th refresh request being the priority request. All refresh requests are priority when the refresh queue is Disabled.

Fixed Memory Hole

This option allows the end user to specify the location of a memory hole. The cycle matching the selected memory hole will be passed to the ISA bus. If Enabled, the selected hole is not remapped.

CPU To IDE Posting

Set this option to Enabled to enable posted messages from the CPU to the IDE controller. The settings are Enabled or Disabled. The Optimal and Fail-Safe default settings are Enabled.

USWC Write Posting

Set this option to Enabled to use USWC(Uncacheable, Speculatable, Write-Combined) memory. The settings are Enabled or Disabled. The Optimal and Fail-Safe default settings are Enabled.

CPU To PCI Posting

Set this option to Enabled to give priority to posted messages from the CPU to the PCI bus. The settings are Enabled or Disabled. The Optimal and Fail-Safe default settings are Enabled.

PCI to DRAM Pipeline

Set this option to Enabled the pipeline from the PCI bus to system memory. The settings are Enabled or Disabled. The Optimal and Fail-Safe Default settings are Enabled.

PCI Burst Write Combine

Set this option to Enabled to allow write instructions to be combined in PCI Burst mode. The settings are Enabled or Disabled. The Optimal and Fail-Safe default settings are Enabled.

Read Around Write

Set this option to Enabled to allow read operations to bypass write operations in the memory controller. The settings are Enabled or Disabled. The Optimal and Fail-Safe default settings are Enabled.

8-Bit I/O Recovery Times / 16-Bit I/O Recovery Times

Choose the recovery time for 8-bit and 16-bit I/O cycles respectively.

Universal Serial Bus

Set this option to Enabled or Disabled on chip(piix3) USB controller. The Optional and Fail-Safe default settings are Disabled.

USB keyboard Support

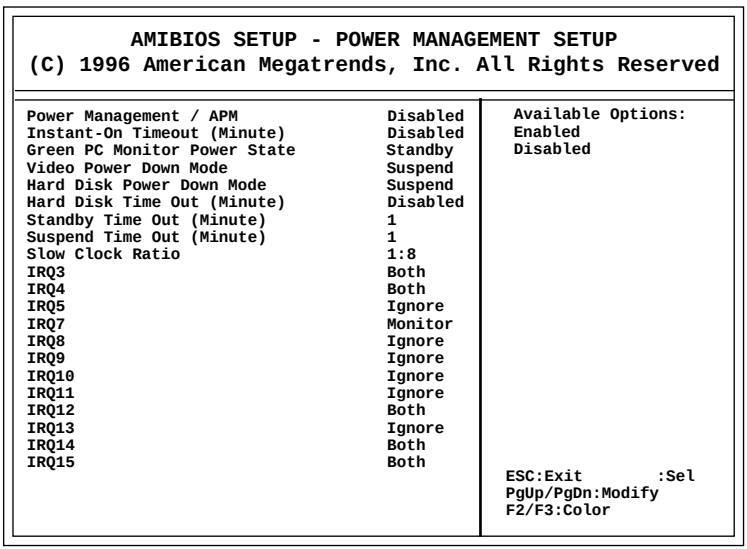
Set this option to Enabled or Disabled USB keyboard.
The Optional and Fail-Safe default settings are Disabled.

USB Passive Release Enable

The system ISA bridge supports GAT mode, which will violate the spirit of the PCI specification. The system provides a programmable passive release mechanism to meet the required master latencies. Choose Enabled to ISA masters may see long delays in accessed to any PCI memory, including the main DRAM array.

3.5 Power Management Setup

1. Press <ENTER> on "Power Management Setup" of the main menu screen.



2. Using <Up> and <Down> to choose the item and <PgUp> and <PgDn> keys to modify the highlighted item.

3. After you have finished with the Power Management Setup, press <ESC> to go back to the main menu.

Description of the item on screen follows:

Power Management/APM

Set this option to Enabled to enable the Intel 82440FX ISA power management features and APM(Advanced Power Management). The settings are Enabled, Inst-On(instant-on) or Disabled. The Optimal and Fail-Safe default settings are Disabled.

Instant-On Timeout (Minute)

This option specifies the length of a period of system inactivity while the computer is in Full power on state. When this length of time expires, AMIBIOS takes the computer to a lower power consumption state, but the computer can return to full power instantly when any system activity occurs. This option is only available if supported by the computer hardware. The settings are Disabled, 1 min, 2 min, 3 min, 4 min, 5 min, 6 min, 7 min, 8 min, 9 min, 10 min, 11 min, 12 min, 13 min, 14 min or 15 min. The Optimal and Fail-Safe default settings are Disabled.

Green PC Monitor Power State

This option specifies the power state that the green PC-compliant video monitor enters when AMIBIOS places it in a power savings state after the specified period of display inactivity has expired. The settings are Off, Standby, Suspend or Disabled. The Optimal and Fail-Safe default settings are Standby.

Video Power Down Mode

This option specifies the power conserving state that the VESA VGA video subsystem enters after the specified period of display inactivity has expired. The settings are Disabled, Standby or Suspend. The Optimal and Fail-Safe default settings are Disabled.

Hard Disk Power Down Mode

This option specifies the power conserving state that the hard disk drive enters after the specified period of hard drive inactivity has expired. The settings are Disabled, Standby or Suspend. The Optimal and Fail-Safe default settings are Disabled.

Hard Disk Timeout (Minutes)

This option specifies the length of a period of hard disk drive inactivity. When this length of time expires, the computer enters power-conserving state specified in the Hard Disk Power Down mode option (see the previous page). The settings are Disabled, 1 min, 2 min, 3 min, 4 min, 5 min, 6 min, 7 min, 8 min, 9 min, 10 min, 11 min, 12 min, 13 min, 14 min or 15 min. The Optimal and Fail-Safe default settings are Disabled.

Standby Timeout (Minute)

This option specifies the length of a period of system inactivity while in Full power on state. When this length of time expires, the computer enters Standby power state. The settings are Disabled, 1 min, 2 min, 3 min, 4 min, 5 min, 6 min, 7 min, 8 min, 9 min, 10 min, 11 min, 12 min, 13 min, 14 min or 15 min. The Optimal and Fail-Safe default settings are Disabled.

Suspend Timeout (Minute)

This option specifies the length of a period of system inactivity while in Standby state. When this length of time expires, the computer enters Suspend power state. The settings are Disabled, 1 min, 2 min, 3 min, 4 min, 5 min, 6 min, 7 min, 8 min, 9 min, 10 min, 11 min, 12 min, 13 min, 14 min or 15 min. The Optimal and Fail-Safe default settings are Disabled.

Slow Clock Ratio

This option specifies the speed at which the system clock runs in power saving states. The settings are expressed as a ratio between the normal CPU clock speed and the CPU clock speed when the computer is in the power-conserving state. The settings are 1:1, 1:2, 1:4, 1:8, 1:16, 1:32, 1:64 or 1:128. The Optimal and Fail-Safe defaults are 1:8.

IRQ3/IRQ4/IRQ5/RQ7/IRQ8/IRQ9/IRQ10/IRQ11/IRQ12/ IRQ13/IRQ14/IRQ15

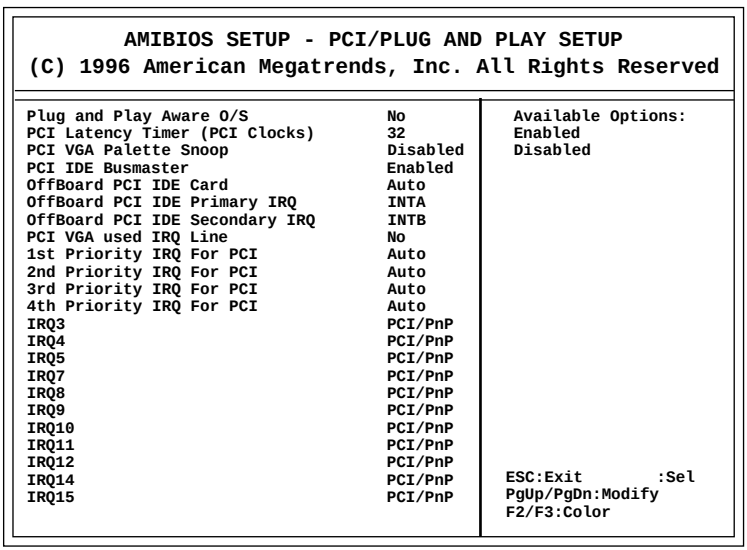
When set to Monitor, these options enable event monitoring on the specified hardware interrupt request line. If set to Monitor and the computer is in a power saving state, AMIBIOS watches for activity on the specified IRQ line. The computer enters the full on power state if any activity occurs.

AMIBIOS reloads the Standby and Suspend timeout timers if activity occurs on the specified IRQ line.

The settings for each of these options are Monitor or Ignore. The Optimal and Fail-Safe default settings are Disabled for all the above options except IRQ3, IRQ4, IRQ7, IRQ12, IRQ14 or IRQ15. The Optimal default settings for these options is Monitor.

3.6 PCI/Plug and Play Setup

1. Press <ENTER> on "PCI/Plug and Play Setup" of the main menu screen.



```
        AMIBIOS SETUP - PCI/PLUG AND PLAY SETUP
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Plug and Play Aware O/S                 No          Available Options:
PCI Latency Timer (PCI Clocks)          32          Enabled
PCI VGA Palette Snoop                   Disabled    Disabled
PCI IDE Busmaster                       Enabled
OffBoard PCI IDE Card                   Auto
OffBoard PCI IDE Primary IRQ            INTA
OffBoard PCI IDE Secondary IRQ          INTB
PCI VGA used IRQ Line                   No
1st Priority IRQ For PCI                Auto
2nd Priority IRQ For PCI                Auto
3rd Priority IRQ For PCI                Auto
4th Priority IRQ For PCI                Auto
IRQ3                                    PCI/PnP
IRQ4                                    PCI/PnP
IRQ5                                    PCI/PnP
IRQ7                                    PCI/PnP
IRQ8                                    PCI/PnP
IRQ9                                    PCI/PnP
IRQ10                                   PCI/PnP
IRQ11                                   PCI/PnP
IRQ12                                   PCI/PnP
IRQ14                                   PCI/PnP     ESC:Exit        :Sel
IRQ15                                   PCI/PnP     PgUp/PgDn:Modify
                                                    F2/F3:Color
```
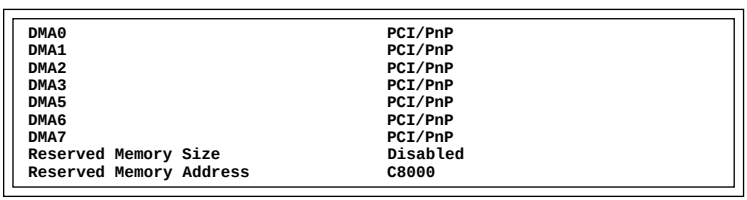



```
DMA0                                    PCI/PnP
DMA1                                    PCI/PnP
DMA2                                    PCI/PnP
DMA3                                    PCI/PnP
DMA5                                    PCI/PnP
DMA6                                    PCI/PnP
DMA7                                    PCI/PnP
Reserved Memory Size                    Disabled
Reserved Memory Address                 C8000
```

2. Using <Up> and <Down> to choose the item and <PgUp> and <PgDn> keys to modify the highlighted item.

3. After you have finished with the PCI/Plug and Play Setup, press <ESC> to go back to the main menu.

Description of the item on screen follows:

Plug and Play Aware O/S

Set this option to Yes if the operating system in this computer is aware of and follows the Plug and Play specification. Currently, only Windows 95 is PnP-aware. The settings are Yes or No. The Optimal and Fail-Safe default settings No.

PCI Latency Timer (PCI Clocks)

This option specifies the latency timings (in PCI clocks) for all PCI devices on the PCI bus. The settings are 32, 64, 96, 128, 160, 192, 224 or 248. The Optimal and Fail-Safe default settings are 64.

PCI VGA Palette Snoop

When this option is set to Enabled, multiple VGA devices operating on different buses can handle data from the CPU on each set of palette registers on every video device. Bit 5 of the command register in the PCI device configuration space is the VGA Palette Snoop bit (0 is disabled). For example, if there are two VGA devices in the computer (one PCI and ISA) and the Bit settings are:

Disabled - Data read and written by the CPU is only dircted to the PCI VGA device's palette registers.

Enabled - Data read and written by the CPU is directed to the both the PCI VGA device's palette registers and the ISA VGA device palette registers, permitting the palette registers of both devices to be identical.

This option must be set to Enabled if an ISA adapter card requires VGA palette snooping. The settings are Enabled or Disabled. The Optimal and Fail-Safe default settings are Disabled.

PCI IDE BusMaster

Set this option to Enabled to specify that the IDE controller on the PCI local bus includes a bus mastering capability. The settings are Enabled or Disabled. The Optimal and Fail-Safe default settings are Disabled.

Offboard PCI IDE Card

This option specifies if an offboard PCI IDE controller adapter card is installed in the computer. You must specify the PCI expansion slot on the motherboard where the offboard PCI IDE controller is installed. If an offboard PCI IDE controller is used, the onboard IDE controller is automatically disabled. The settings are Auto(AMIBIOS automatically determines where the offboard PCI IDE controller adaper card is installed), Slot1, Slot2, Slot3 or Slot4. The Optimal and Fail-Safe settings are Auto.

In the AMIBIOS for the Intel 82440FX ISA chipset, this option forces IRQ14 and IRQ15 to a PCI slot on the PCI Local bus. This is necessary to support non-compliant ISA IDE controller adapter cards.

If an offboard PCI IDE controller adapter card is installed in the computer, you must also set the Offboard PCI IDE Primary IRQ and Offboard PCI IDE Secondary IRQ options.

Offboard PCI IDE Primary IRQ/ Offboard PCI IDE Secondary IRQ

These options specify the PCI interrupt used by the Primary (or Secondary) IDE channel on the offboard PCI IDE controller. The settings are Disabled, Hardwired, INTA, INTB, INTC or INTD. The Optimal and Fail-Safe default settings are Disabled.

PCI VGA Used IRQ Line

Choose PCI VGA display adapter card using IRQ line. The Optimal and Fail-Safe default settings No.

1st Priority IRQ for PCI/2nd Priority IRQ for PCI/ 3rd Priority IRQ for PCI/4th Priority IRQ for PCI

These options specify the priority IRQ to be used for any PCI devices installed in PCI expansion slots 1 through 4. The settings are Auto(AMIBIOS automatically determines the priority IRQ), (IRQ) 3, 4, 5, 7, 9, 10 or 11. The Optimal and Fail-Safe default settings are Auto.

IRQ3/IRQ4/IRQ5/RQ7/IRQ9/IRQ10/IRQ11/IRQ14/IRQ15

These options specify the bus that the specified IRQ line is used on. These options allow you to reserve IRQs for legacy ISA adapter cards.

These options determine if AMIBIOS should remove an IRQ from the pool of available IRQs passed to devices that are configurable by the system BIOS. The available IRQ pool is determined by reading the ESCD NVRAM. If more IRQs must be removed from the pool, the end user can use these options to reserve the IRQ by assigning an ISA/EISA setting to it. Onboard I/O is configured by AMIBIOS. All IRQs used by onboard I/O are configured as PCI/PnP. IRQ14 and 15 will not be available if the onboard 82440FX ISA PCI IDE is enabled. If all IRQs are set to ISA/EISA and IRQ14 and 15 are allocated to the onboard PCI IDE, IRQ9 will still be available for PCI and PnP devices, because at least one IRQ must be available for PCI and PnP devices. The settings are ISA/EISA or PCI/PnP. The Optimal and Fail-Safe default settings are IRQ3 through 7 are ISA/ EISA. The Optimal and Fail-Safe default settings PCI/PnP.

DMA0/DMA1/DMA2/DMA3/DMA5/DMA6/DMA7

These options specify the bus that the specified DMA channel is used. These options allow you to reserve DMAs for legacy ISA adapter cards.

These options determine if AMIBIOS should remove a DMA from the available DMAs passed to devices that are configurable by the system BIOS. The available DMA pool is determined by reading the ESCD NVRAM. If more DMAs must be removed from the pool, the end user can use these options to reserve the DMA by assigning an ISA/EISA setting to it.

Reserved Memory Size

This option specifies the size of the memory area reserved for legacy ISA adapter cards. The settings are Disabled, 16K, 32K or 64K. The Optimal and Fail-Safe default settings are Disabled.

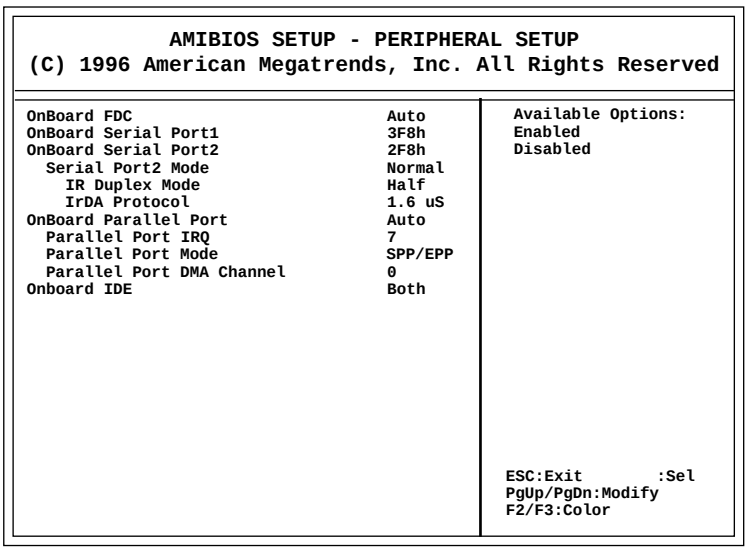
Reserved Memory Address

This option specifies the beginning address (in hex) of the reserved memory area. The specified ROM memory area is reserved for use by legacy ISA adapter cards.

The settings are C0000, C4000, C8000, CC000, D0000, D4000, D8000 or DC000. The Optimal and Fail-Safe default settings are C4000.

3.7 Peripheral Setup

1. Press <ENTER> on "Peripheral Setup" of the main menu screen.



2. Using <up> and <down> to choose the item and <PgUp> and <PgDn> keys to modify the highlighted item.

3. After you have finished with the Peripheral Setup, press <ESC> to go back to the main menu.

Description of the item on screen follows:

Onboard FDC

Choose Auto, The BIOS automatically select.

If the ISA add-on card had	Onboard FDC to be set at
FDC exist	Disabled
none FDC exist	Enabled

Choose Enabled, Enabling onboard FDC.
Choose Disabled, Disabling onboard FDC.
The Optimal and Fail-Safe default settings are Auto.

Onboard Serial Port1/Onboard Serial Port2

Choose Auto, The BIOS automatically select.

If the ISA add-on card had				Onboard Serial port to be set at			
COM1 (I/O:3F8H)	COM2 (I/O:3F8H)	COM3 (I/O:3E8H)	COM4 (I/O:2E8H)	PORT1	IRQ ASSIGNED	PORT2	IRQ ASSIGNED
✓	✓	✓	✓	DISABLED	X	DISABLED	X
✓	✓	X	X	COM3	4	COM4	3
X	X	✓	✓	COM1	4	COM2	3
✓	X	X	✓	COM2	3	COM3	4
X	✓	✓	X	COM1	4	COM4	3
✓	✓	✓	X	COM4	3	DISABLED	X
✓	✓	X	✓	COM3	4	DISABLED	X
✓	X	✓	✓	COM2	3	DISABLED	X
X	✓	✓	✓	COM1	4	DISABLED	X
X	X	X	X	COM1	4	COM2	3
✓	X	X	X	COM2	3	COM3	4
X	✓	X	X	COM1	4	COM3	4
X	X	✓	X	COM1	4	COM2	3
X	X	X	✓	COM1	4	COM2	3

Note: *If the onboard serial port interrupt and ISA add- on card interrupt are in conflict. The serial port will not work properly. Please disable one of the devices.*

Serial Port2 Mode

Choose onboard Serial Port2 operation mode as standard UART or as IR/Infrared.

IR Duplex Mode

Choose full duplex or half duplex operation mode when the onboard Serial Port2 operation mode be selected as IR.

IrDA Protocol

If onboard Serial Port2 is selected as IrDA mode. The user has to set the IR transmit active pulse time according to the specification of IR module. Based on different IR module the user can select active pulse time as 1.6us or 3/16 bit.

Onboard Parallel Port

Choose Auto, the BIOS automatically assigned onboard parallel port to available parallel port or disabled

If the ISA add-on card had			**Onboard parallel port**	
LPT1 I/O:378H	LPT2 I/O:278H	LPT3 I/O:3BCH	PORT ASSIGNED	IRQ ASSIGNED
✓	✓	✓	Disabled	X
✓	✓	X	LPT3	5
✓	X	✓	LPT2	5
X	✓	✓	LPT1	7
✓	X	X	LPT2	5
X	✓	X	LPT1	7
X	X	✓	LPT1	7
X	X	X	LPT1	7

Note: *If the onboard parallel port interrupt and ISA add-on card interrupt are in conflict. The parallel port will not work properly. Please disable one of the devices.*

Parallel Port IRQ

If the onboard parallel mode is not on auto mode. The user can select the interrupt line for onboard parallel port. We suggest that the user select the interrupt for the onboard parallel port as show below:

Onboard parallel port be set at	Parallel Port IRQ
LPT1(378H)	7
LPT2(278H)	5
LPT3(3BCH)	5

Parallel Port Mode

This option allows user to choose the operating mode of the onbaord parallel port. The settings are Normal, SPP/EPP or ECP mode.

Paralle Port DMA Channel

This option allows user to choose DMA channel 1 to 3 for the onboard parallel port on ECP mode.

Onboard IDE

Set this option to enable or disable on board IDE controller.