—2 serial ports (ComA + ComB)
—1 parallel port supports ECP or EPP mode
—1 FDD port that supports 2 FDDs with 360K, 720K, 1.2M, 1.44M, and 2.88Mbytes per second transfer rate.

On-Board IDE:

- An IDE controller on the Intel® 82440FX PCI Chipset provides IDE HDD/CD-ROM with PIO and Bus Master Operation Mode. The PIO Mode supports modes 0, 1, 2, 3, and 4, with a transfer rate of 22 Mbytes second.

On-Board USB: (Reserved)

- 2 port USB features on the Intel® 82440FX PCI Chipset.

RTC:

- Non-Volatile RTC with 114Kbytes of CMOS RAM.

Dimensions

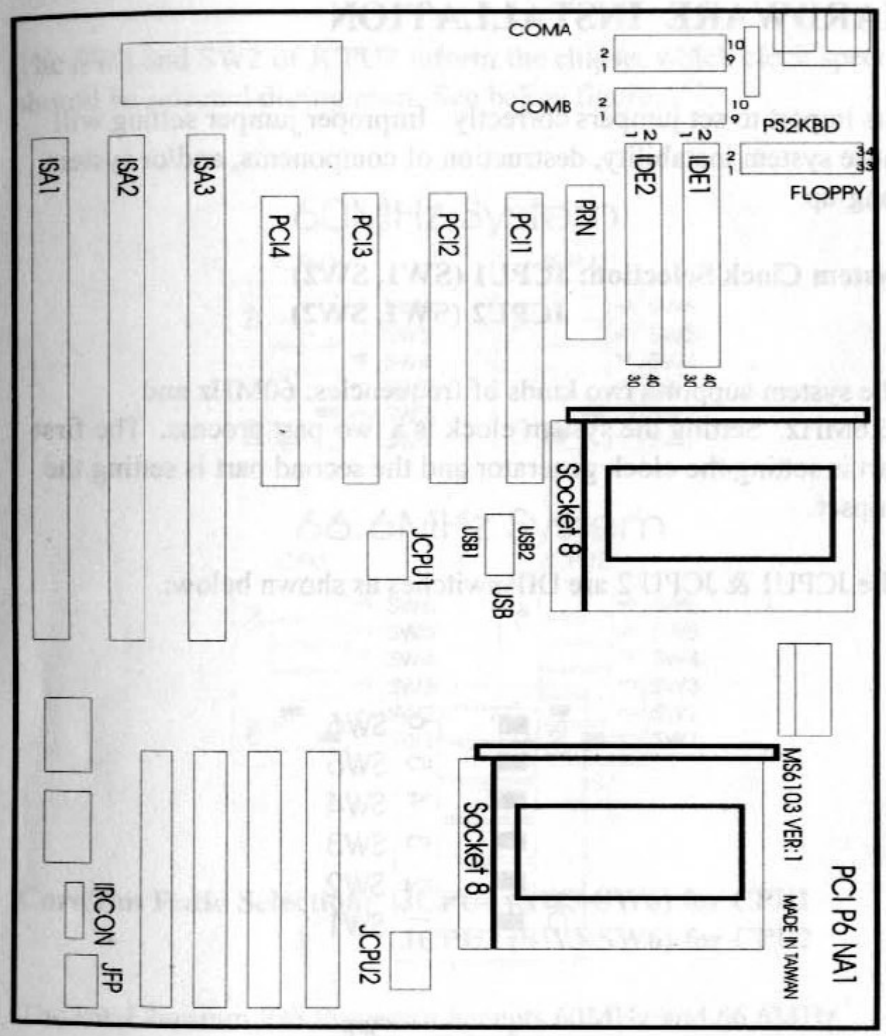
- Standard Baby AT size: 33 cm(L) x 22 cm (W) x 6 layer PCB

Mounting

- 7 mounting holes

1.2 System Board Layout

Figure 1-1



Chapter 2

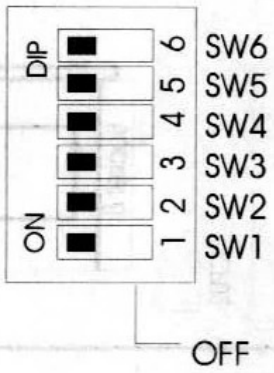
HARDWARE INSTALLATION

It is import to set jumpers correctly. Improper jumper setting will cause system instability, destruction of components, and/or system hang-up.

System Clock Selection: JCPU1 (SW1, SW2)
JCPU2 (SW1, SW2)

The system supports two kinds of frequencies: 60MHz and 66.6MHz. Setting the system clock is a two-part process. The first part is setting the clock generator and the second part is setting the chipset.

The JCPU1 & JCPU 2 are DIP switches as shown below:

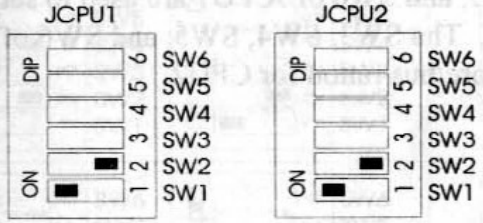


When the black switch is moved to the "on" side of the DIP switch the switch is said to be on.

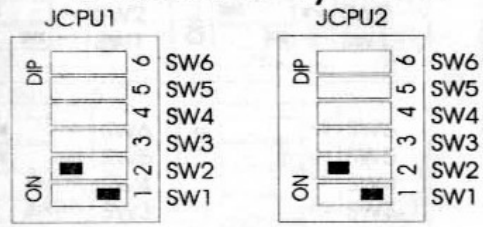
The SW1 and SW2 of JCPU1 are DIP switches used to select the clock speed from the clock generator.

The SW1 and SW2 of JCPU2 inform the chipset which clock speed should be selected during reset. See below figure:

60MHz System



66.6MHz System



Core/Bus Ratio Selection: JCPU1 (SW3-SW6) for CPU1
JCPU2 (SW3-SW6) for CPU2

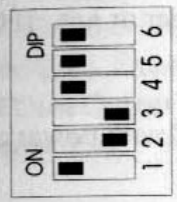
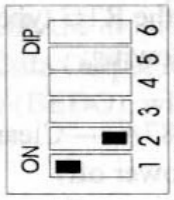
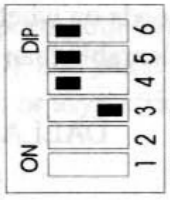
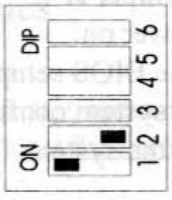
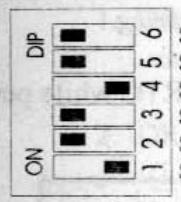
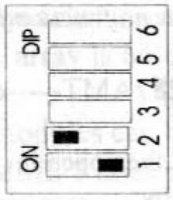
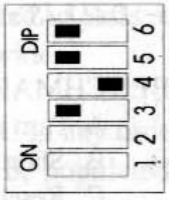
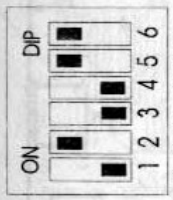
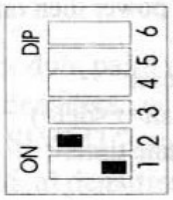
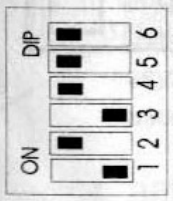
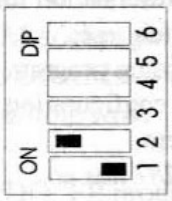
The Intel Pentium Pro Processor accepts 60MHz and 66.6MHz external clock frequencies. However, actual CPU speed is the external clock frequency multiplied by the core/bus ratio.

Example: If the CPU speed is 180MHz then the user would have had to select 60MHz for the external clock speed. In this case the core/bus ratio would be 3. (60MHz x 3 = 180MHz)

This system supports a dual core/bus ratio switch for dual processors. Each processor has one core bus/bus ratio switch. This allows the dual processors to run at different speeds but only if both processors have the same external clock frequency.

The core/bus switch supports all core/bus ratios which Intel has currently defined and will support all future core/bus ratios. The SW3, SW4, SW5, and SW6 of JCPU1 are used to set the core/bus ration for CPU1. The SW3, SW4, SW5, and SW6 of JCPU2 are used to set the core/bus ration for CPU2.

See following figure for JCPU1 & JCPU2 settings:

CPU SPEED	CPU 1 JCPU1	CPU 1 JCPU2	CPU 2 JCPU2
150 MHz			
180 MHz			
200 MHz			
233 MHz			
167 MHz			

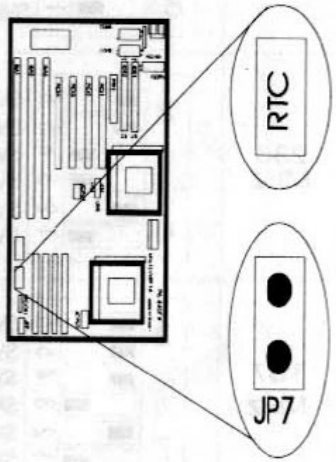
CMOS RAM Clear: JP7

The system board configuration is stored in RTC's CMOS RAM. If you need to clear the system board configuration the process depends on whether of not the RTC type is clear or not. If the RTC is clearable than do the following:

1. DALLAS's DSI2887A-----Clear RTC with power off.
   - A. Turn power off.
   - B. Short jumper JP7.
   - C. Turn power on.
   - D. Enter the BIOS setup program to re-setup the system configuration.
   - E. Reboot the system.

Note: DALLAS's DSI2887 has no function for clearing.

2. BENCHMARQ's BQ3287AMT-----clear RTC while power is on.
   - A. Turn power on.
   - B. Short jumper JP7 then open it.
   - C. Reset the system by:
     1. Turn off power then on.
        or
     2. Warm reset:
        (press <ctrl>+<alt>+<del>)
        at the same time.
        or
     3. Use the reset button for a hard switch reset.
   - E. Enter the BIOS setup program to reset the system configuration.
   - F. Reboot the system.



Note: BENCHMARQ's BQ3287 has no function for clearing.

System Memory Installation: SIMM4-SIMM1

The system board provides four 72-pin SIMM sockets which are numbered from SIMM1 to SIMM4. The system board supports memory sizes from 8MB to 512MB using 4MB, 8MB, 16MB, 32MB, 64MB, and 128MB DRAM modules. It supports both Fast Page Mode (FP), Extended Data Output Mode (EDO), and Burst Extended Data Output Mode (BEDO), with symetric or asymetric row/colum address.

DRAM Population Rules

In order to create a memory array, certain rules must be followed. The following set of rules allows for optimum configuration.

1. DRAM modules must be populated in pairs; the memory array is 64-or-72-bits wide.

2. DRAM modules can be populated in any order (i.e. SIMM2/1 does not have to be populated before SIMM3/4 are used.)

3. DRAM module pairs need to be populated with the same densities...single or double. For example, SIMM1/2 sockets must be populated with identical densities. However SIMM3/4 sockets can be populated with different densities than SIMM socket pair 1/2. In addition, asymetric DRAMs of the same type should be used in a whole row.

4. BEDO, EDO, FP modes can be mixed in the memory array. However only one type should be

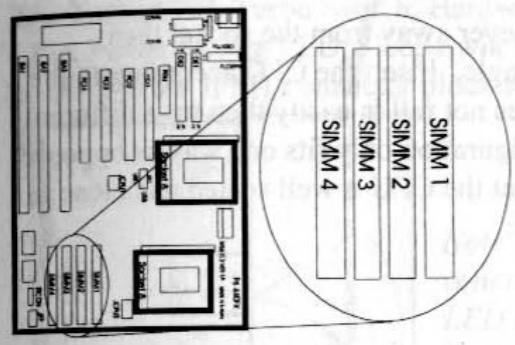
used per SIMM socket pair. For example: SIMM sockets 1 & 2 can be populated with EDO while SIMM sockets 3 & 4 can be populated with FP mode type DRAM.

5. The DRAM timing which provides the DRAM speed grade control for the entire memory array must be programmed to use the timing of the slowest DRAM that is currently installed.

Note: Before using DRAM modules, make sure that that the modules used is the same as in the above chart.

Note: To use the ECC (Error Code Correct) function, a SIMM module with parity support must be used. At this time you can turn on the ECC function in the BIOS setup.

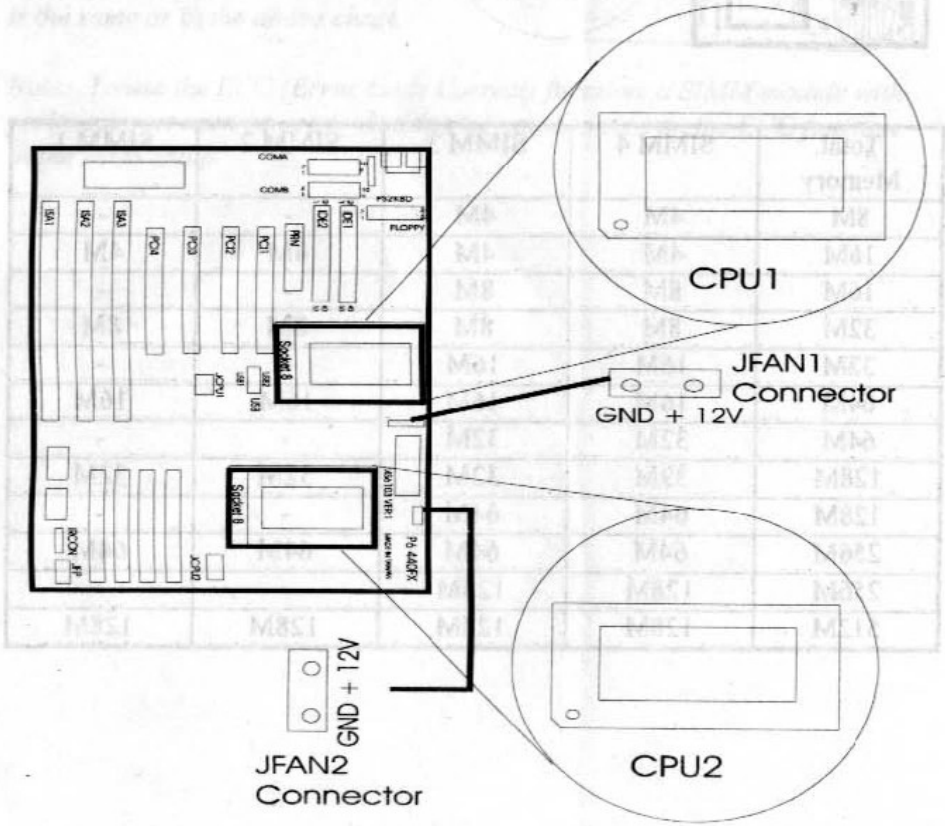
DRAM Memory Installation



Total Memory	SIMM 4	SIMM 3	SIMM 2	SIMM 1
8M	4M	4M	-	-
16M	4M	4M	4M	4M
16M	8M	8M	-	-
32M	8M	8M	8M	8M
32M	16M	16M	-	-
64M	16M	16M	16M	16M
64M	32M	32M	-	-
128M	32M	32M	32M	32M
128M	64M	64M	-	-
256M	64M	64M	64M	64M
256M	128M	128M	-	-
512M	128M	128M	128M	128M

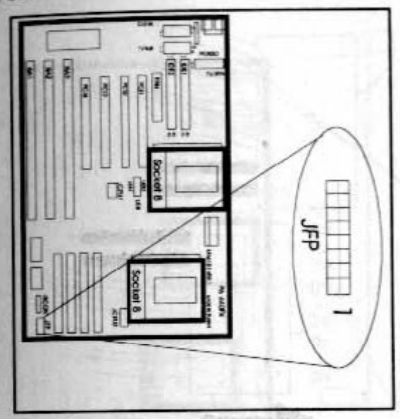
CPU Installation & Fan Power Connector: JFAN1, JFAN2

Open Socket 8 by pulling the lever away from the socket then upwards at a 90 degree right angle. Insert the CPU according to the orientation as shown. IF it does not fall in easily then try a different direction because the pin configuration only fits one way as opposed to earlier CPUs. Make sure that the CPU is well seated and close to the lever. See following figure:



Case Block Connector : JFP

The Turbo LED, Turbo Switch, Hardware Reset, Key lock, Power LED, Power Saving LED, Sleep Switch, Speaker,and HDD LED all connect to the JFM1 connector block as below.



Note : The hardware Turbo switch is not functional. But the Turbo LED be controled by software Turbo/Deturbo.