

**Main memory:**

- Supports four memory banks (two rows) using four 72-pin SIMM modules.
- Up to 128 Mbytes main memory.
- Supports EDO/Hyper Page Mode DRAM or Standard Fast Page mode DRAM.

**VRM Header Socket: (OPTIONAL)**

- See page 14.

**Slots:**

- Three 32-bit Master PCI Bus slots and four 16-bit ISA bus slots.

**On-Board Peripherals:**

- On-board peripherals include
  - 1 floppy port supports 2 FDD
  - 2 serial ports
  - 1 parallel port supports ECP or EPP mode
  - 2 PCI Bus Master IDE ports (up to four IDE HDD)
    - PIO Mode: mode 2, 3, 4
    - DMA Mode: Single-word DMA Mode 2 or slower
    - Multi-word DMA Mode 1
    - Single word DMA Mode 2 or faster
    - Multi-word DMA Mode 1 or faster
    - Multi-word DMA Mode 2 or faster

**Dimensions:**

- 26 cm(L) x 22 cm(W) x 4 layer PCB

**Mounting:**

- 7 mounting holes

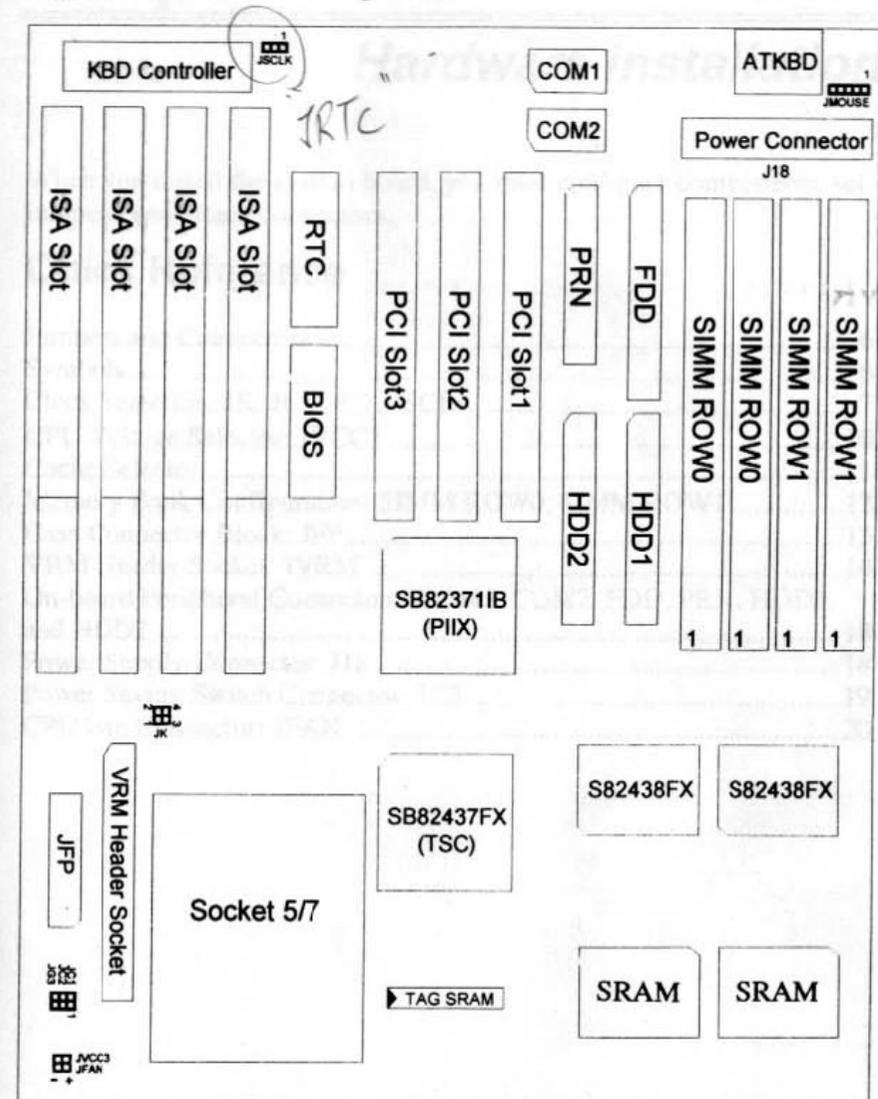
**System Board Layout**

Figure 1-1. System board Layout

## Jumpers and Connectors

Refer to Figure 1-1 for jumper and connector locations.

**Jumpers** Jumpers on the system board provide information to your operating system about installed options and system settings. You need to configure jumpers when you install the CPU, select cache size.

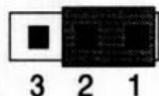
**Connectors** Connectors attach control panel switches and indicators, as well as the speaker, keyboard and power supply.

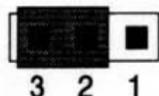
**Setting Jumpers** Configure system board options by setting jumper switches. Use your fingers to position a jumper cap over the desired pin setting and gently press down.

*Note:* When you open a jumper, leave the plastic jumper cap attached to one of the pins so you don't lose it.

### Symbols:

For 3-pin jumpers, the following symbols are used:

 — Close pins 1 and 2 with a jumper cap.

 — Close pins 2 and 3 with a jumper cap.

For 2-pin jumpers, the following symbols are used:

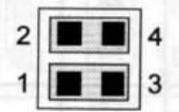
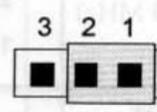
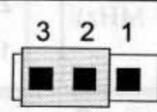
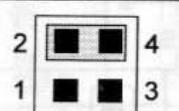
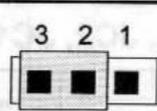
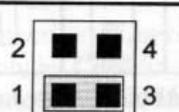
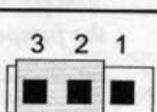
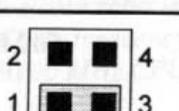
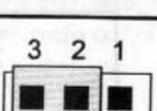
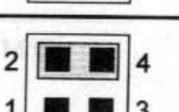
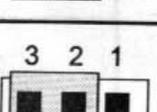
 — Close the jumper by inserting the jumper cap over the two pins of the jumper.

 — Open the jumper by inserting the jumper cap over one or neither of the pins of the jumper.

## Clock Selection: JK, JC2, JC1, JSCLK

### I. INTEL® PENTIUM™ CPU clock jumper setting

#### JK, JC2, JC1, JSCLK Settings

CPU Speed	JK Note 1	JC2 Note 2	JC1 Note 2	JSCLK Note 3
75 MHz				
90 MHz				
100 MHz				
120 MHz				
133 MHz				
150 MHz				
166 MHz				

**II. CYRIX® 6x86 CPU clock jumper setting**  
**JK, Jc2, Jc1, JSCLK Settings**

JK	Note 1			100 MHz
Jc2	Note 2			120 MHz
Jc1	Note 2			133 MHz
JSCLK	Note 3			150 MHz

P120+			100 MHz
P150+			120 MHz
P166+			133 MHz

**III. AMD® 5K86 CPU clock jumper setting**  
**JK, Jc2, Jc1, JSCLK Settings**

JK		50 MHz
		60 MHz
		66.6 MHz

*Note 1: The 3 Host Clock frequencies that the system supports are 50MHz, 60MHz, and 66.6 MHz. See the following chart to set the jumper JK for the different Host Clock frequencies.*

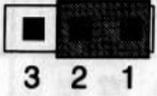
*Note 2 The jumpers Jc2 and Jc1 set the Bus/Core (Fraction) ration of the CPU. See below.*

Bus/Core ratio	Jc2	Jc1			2/3
	Previous P54C/CQ5/CS	Previous P54C/CQ5/CS			1/4
					1/3
					1/2
					2/5

*The actual core speed of CPU is the Host Clock frequency multiply by Core/Bus ratio. For example, if the Host Clock frequency is 66.6 MHz and the Core/Bus ratio is 3/2, the Actual CPU core speed will be 66.6 x 3/2 = 100 MHz.*

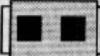
*The system has reserved space for future usage of 150/60MHz and 180/60 MHz CPU. The Host Clock frequency is 60MHz and Bus/core ratio is 2/5 for the 150/60 MHz CPU, and, the Host Clock frequency is 60MHz and Bus/core ratio is 1/3 for the 180/60 MHz CPU.*

**Note 3** The PCI Bus Clock is the Host Clock Frequency divided by 2 and the ISA Bus Clock is the PCI Bus clock divided by 3 or 4. We recommend that the ISA Bus Clock is the PCI Bus Clock divided by 3 when the Host Clock frequency is 50 MHz and divided by 4 when the Host Clock frequency is 60 MHz or 66.6 MHz. The jumper JSCLK is to set the PCI Bus Clock either divided by 3 or 4 for the ISA Bus Clock.

 <p>3 2 1</p>	<p>ISA Bus Clock = PCI Bus Clock divided by 3</p>
 <p>3 2 1</p>	<p>ISA Bus Clock = PCI Bus Clock divided by 4</p>

Jumper JVCC3 selects a 3.4V/3.5V voltage power source for P54C. See figure 1-1 for the location of the jumper.

### JVCC3 Settings

CPU Voltage	JVCC3
3.4V	
3.5V	

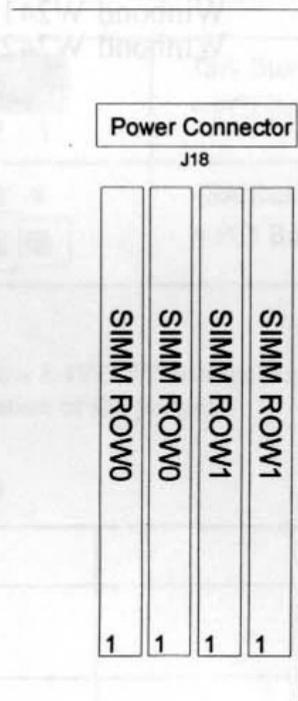
## Cache Selection

The system board supports 256K of cache memory. Suitable TAG SRAM are as follows:

8Kx8 SRAM	Winbond W24128AK-15
16Kx8 SRAM	Winbond W24129AK-15
32Kx8 SRAM	Winbond W24257AK-15

## Memory Bank Configuration

The system board supports two rows, four memory banks (i.e., two banks per row) and provides four 72-pin Single In-line Memory Module (SIMM) sockets on-board. Each row accepts single density or double density banks in the following sizes: 4M, 8M, 16M, and 32M.



**Note:** Make sure the SIMMs are of the same type with equal size and density when installing new memory.

**Note:** If you only install two SIMM modules, install them on ROW0 to get better performance.

## Case Connector Block: JFP

The Turbo LED, Turbo Switch, Hardware Reset, Keylock, Power LED, Power Saving LED, Sleep Switch, Speaker and HDD LED all connect to the JFP Connector Block as shown below. See Figure 1-1 for JFP's location.

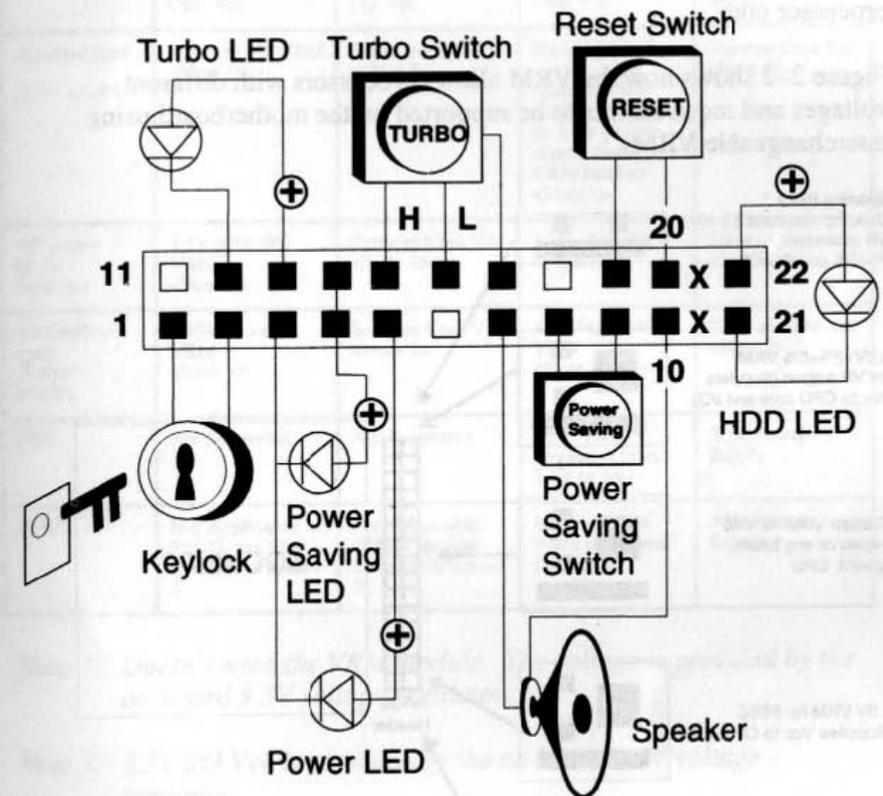


Figure 2-1. Case Connector Block – JFP

**Note** The hardware Turbo switch is not functional. Please press <Ctrl>+<Alt>+<+> or <Ctrl>+<Alt>+<-> for software Turbo/De-turbo function. The LED is always ON and cannot be toggled.

## VRM Header Socket: JVRM

The VRM (Voltage Regulator Module) offers flexibility in that it allows processors with different voltages and requirements to be easily supported on the motherboard. The VRM can be defined as a voltage converter with a standardized pinout capable of converting a system power supply voltage so that it matches the voltage necessary for the processor core.

Figure 2-2 shows how the VRM allows processors with different voltages and requirements to be supported on the motherboard using interchangeable VRMs.

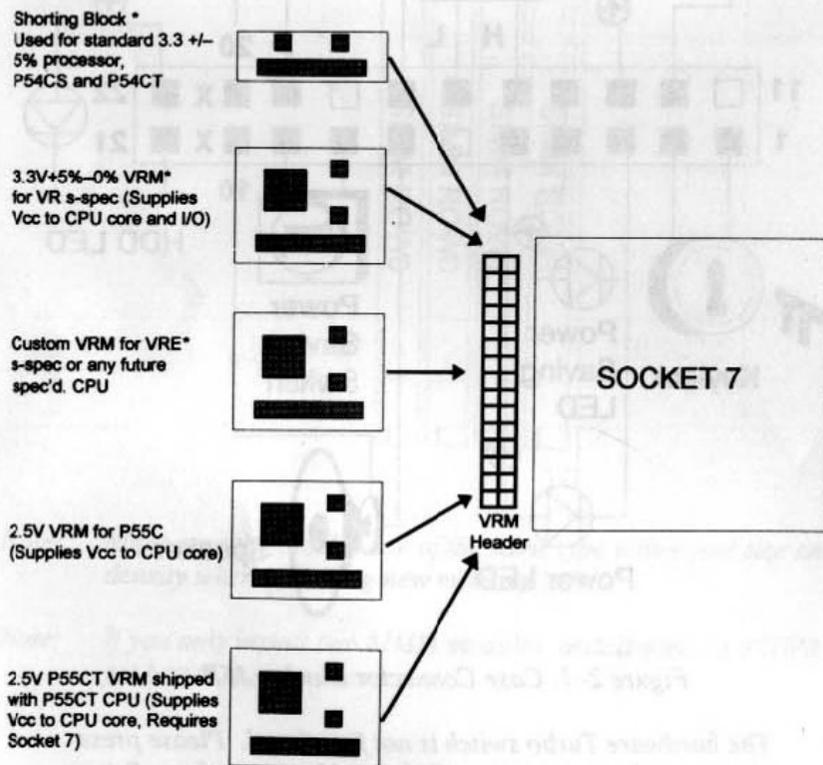


Figure 2-2. Voltage Regulator Modules

\* The on-board Voltage Regulator has covered the first 3 situations in Table 2-1 (i.e., Standard spec., VR spec, and VRE spec, 3 different specs of Pentium CPU).

Table 2-1. On-board 3.3V Voltage Regulator and Different Spec. of CPU Types

	Flexible Motherboard with Socket 5 and VRM (Phase 1)		Flexible Motherboard with Socket 7 and VRM (Phase 2)	
	5V or 3.3V Power Supply		3.3V Power Supply	
	Core Vcc	I/O Vcc	Core Vcc	I/O Vcc
Standard Spec (3.3V +/- 5%)	3.3V +/- 5% VRM <Note 1>	Same as Core Vcc <Note 2>	Shorting Block (Core and I/O voltage is supplied by 3.3V power supply through VRM header) <Note 1>	Same as Core Vcc <Note 2>
VR s-spec (3.3V - 0%+5%)	3.3V +5%-0% VRM <Note 1>	Same as Core Vcc <Note 2>	3.3V +5%-0% <Note 1>	Same as Core Vcc <Note 2>
VRE/MD s-spec (3.45V - 3.60V)	3.45V to 3.6V VRM <Note 1>	Same as Core Vcc <Note 2>	3.45V to 3.6V VRM <Note 1>	Same as Core Vcc <Note 2>
P55C	Not Supported	Not Supported	2.5V VRM (regulates from 3.3V or 5V)	3.3V Power Supply
P55CT	Not Applicable. P55CT can't be installed in Socket 5	Not Applicable. P55CT can't be installed in Socket 5	Intel Supplied VRM (regulated from 5V)	3.3V Power Supply

Note 1: Doesn't need the VRM module. The voltage is provided by the on-board 3.3V voltage regulator.

Note 2: 3.3V I/O Vcc is provided by the on-board 3.3V voltage regulator.

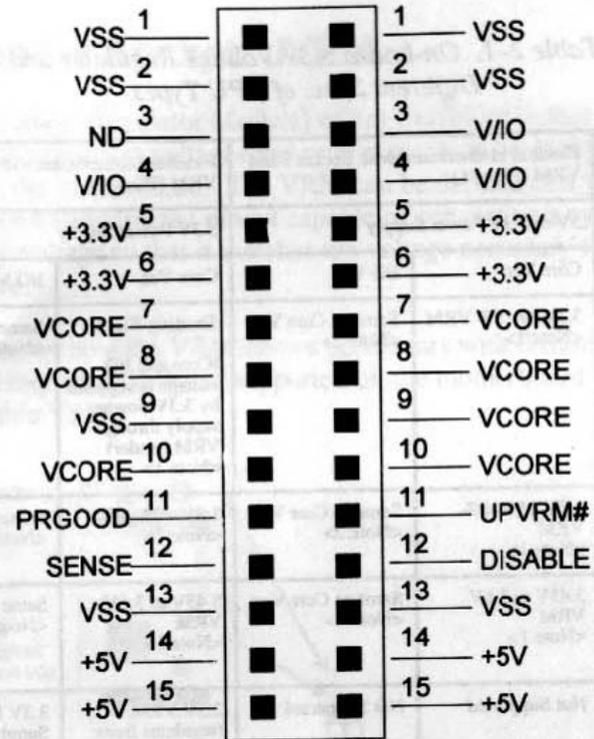


Figure 2-3: Voltage Regulator Module Header Pin Diagram & Description

Pin Name	Type	Usage	Function
+3.3V	Input	Optional	+3.3V Supply, may be used for OEM CPU regulation supply or control signal pull-up.
+5V	Input	Required	+5V Supply required for P55CT VRM.
DISABLE	Input	Optional	When driven high, this input will disable the Voltage Regulator Module output and the output of the module will float.
PWRGOOD	Output	Optional	Power Good is driven high upon the VRM output reaching valid levels.
ND			Not Defined. Reserved for OEM use.
SENSE	Input	Required	Sense is provided for the regulator to correct for voltage drops across the connector and motherboard power plane.
UPVRM#	Output	Required	The P55CT module will drive this signal low to indicate to the CPU that the module is intended for P55CT usage. This signal must be tied high for modules not designed for P55CT.
VCORE	Output	Required	Voltage Regulator Module Output, typically 2.5V for P55C and P55CT.
V/I/O	Output	Optional	CPU I/O power connection. Allows for VRM to specify I/O voltage. Connected directly to +3.3V input on P55CT VRM.
VSS	Input	Required	Ground Reference.

Also see Figure 1-1 for VRM Header Socket (JVRM) location.