System Board Specifications

CPU:

Supports one of the following CPUs:

- 486 SX/DX/DX2 - 25/33/40/50/66
- Cyrix M7 DX/DX2-40/50/66
- Intel S-series 486 SX/DX/DX2-33/66, DX4-75/100
- AMD-DXL, DX/DX2 40/50/66

Cache memory:

- Supports 128K, 256K, or 512K cache memory

Main memory:

- Four 72-pin SIMM sockets support 8 banks of memory with 1M, 2M, 4M, 8M, 16M, and 32M DRAM.

Slots:

- Seven 16-bit AT bus slots
- Three 32-bit VL bus slots, 2 Master slots and one Slave slot for the VESA standard.

Battery:

- 3.6V/480mA Li-battery, or 3.6V/210mA on-board coin battery

Dimensions:

- 26cm x 22 cm x 4 layers

Mounting:

- 6 mounting holes

System Board Layout

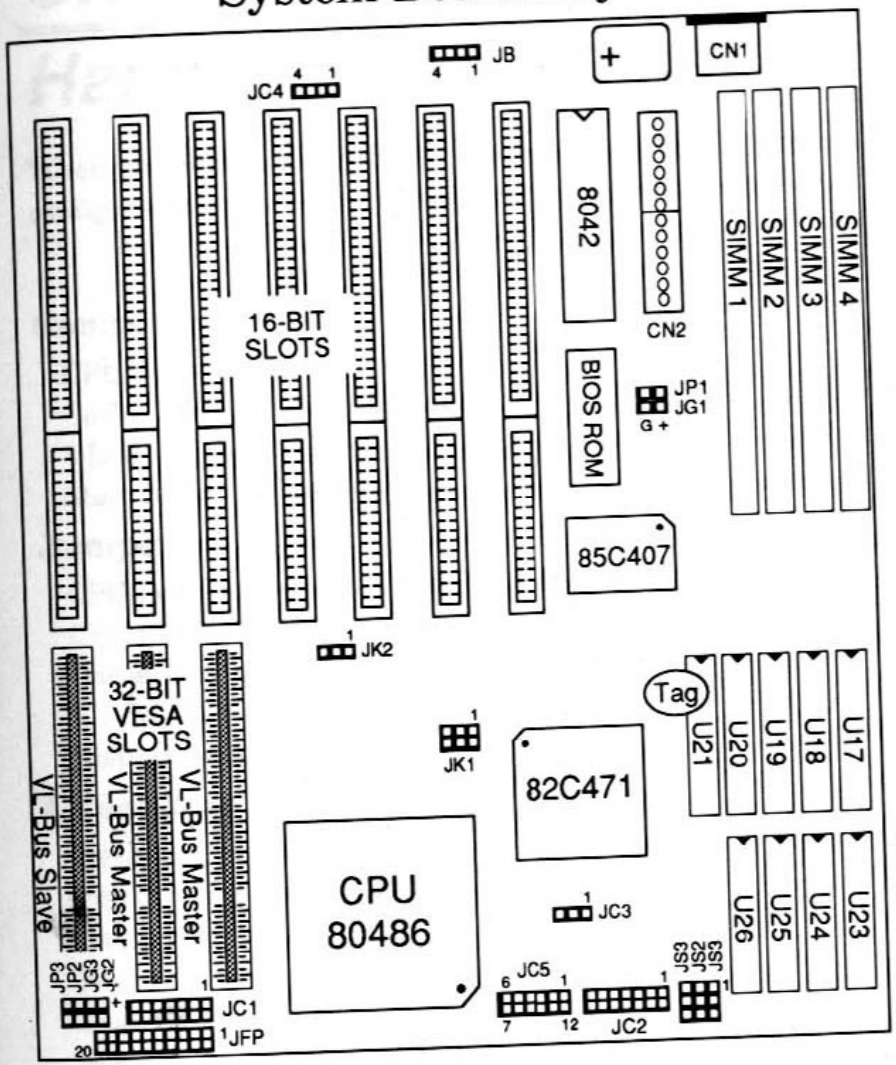


Figure 1-1. System board Layout

Display Adaptor Selection: JP1

If you are using a monochrome or color (CGA) display adaptor you must set the jumper JP1. If you are using an EGA or VGA adaptor, the JP1 setting is irrelevant. See Figure 1-1 for jumper location.

Display Adaptor Jumper: JP1

Display type	JP1
Color Graphics Adaptor	
Monochrome Adaptor (default)	

Keyboard Connectors: CN1

You can plug a keyboard cable directly into the standard five-pin female DIN connector. See Figure 1-1 for the connector's location.

Power Supply Connector: CN2

The power supply connector is a twelve-pin male connector. Dual connectors from the power supply can fit in only one direction. Make sure to attach the connectors with the two black wires at the center, as show in the diagram below. See Figure 1-1 for the connector's location.

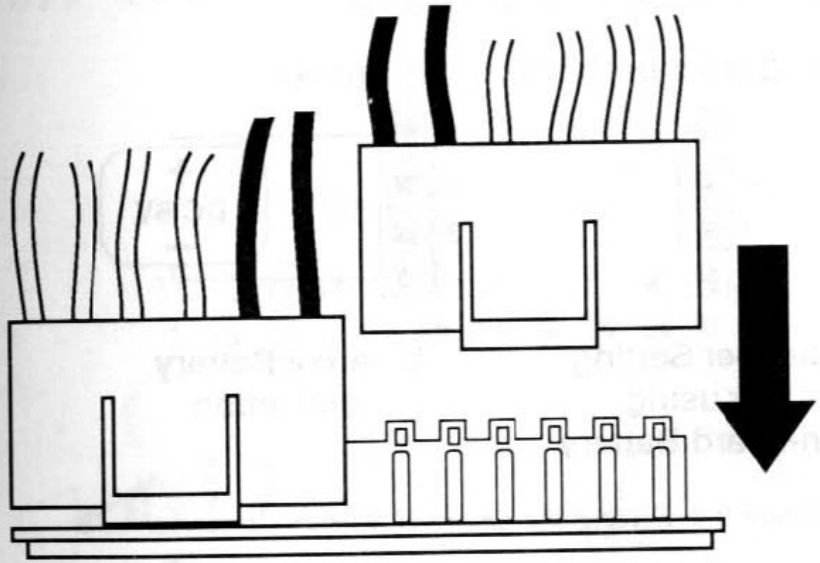


Figure 2-1. Attaching Power Supply Connectors

Connector Pin Description

Pin	Description	Pin	Description
1	Power Good	1	Ground
2	+5V DC	2	Ground
3	+12V DC	3	-5V DC
4	-12V DC	4	+5V DC
5	Ground	5	+5V DC
6	Ground	6	+5V DC

External Battery Connector: JB

A battery must be used to retain the system board configuration in CMOS RAM. You can use either the on-board battery or an external battery. If you use the on-board battery you must short pins 2-3 of JB. For an external battery, the battery's cable connector attaches to pins 1 and 4 of JB. See Figure 1-1 for the connector's location.

JB: External Battery Connector

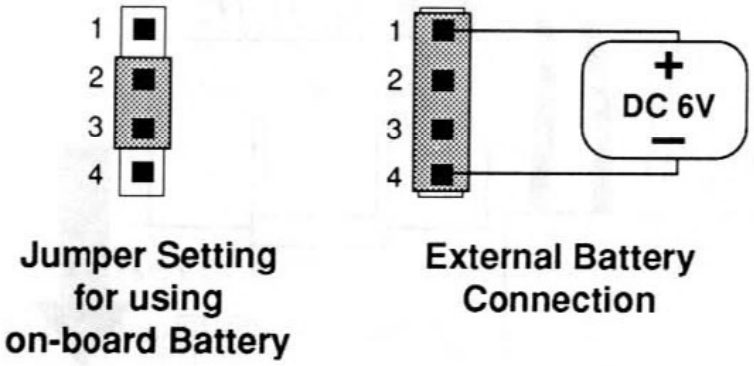


Figure 2-2. Setting the External Battery Connector - JB

Case Connector Block: JFP

The Turbo LED, Turbo switch, Hardware Reset, Keylock, Power LED, Power Saving LED, Sleep switch, and Speaker are all connected to the JFP Connector Block as shown below. See Figure 1-1 for the connector block's location.

JFP: Case Connector Block

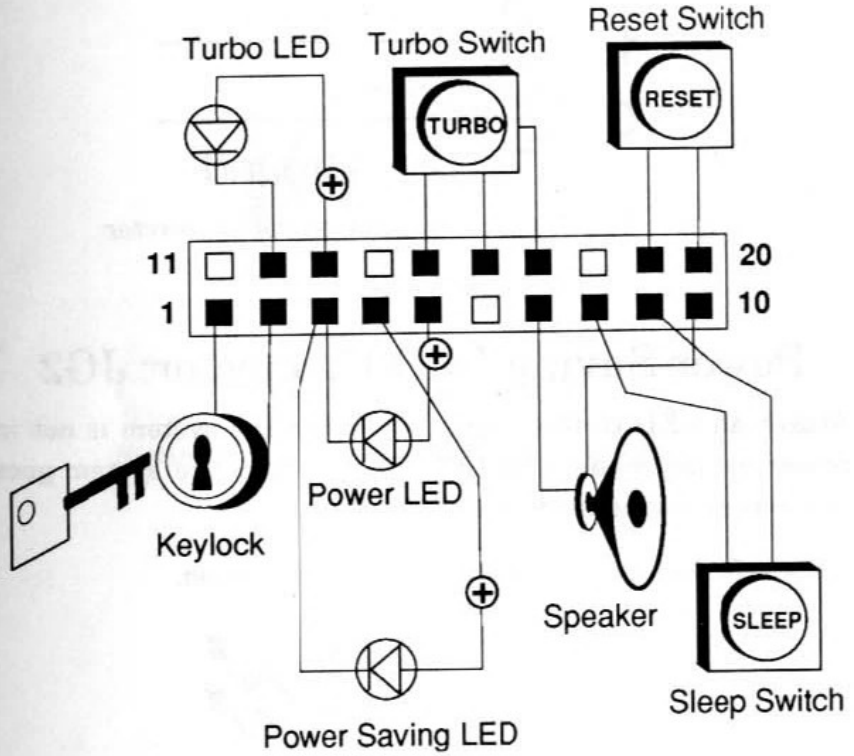


Figure 2-3. Case Connector Block - JFP

DRAM Configuration

The SIS 486 green system board provides four 72-pin Single In-line Memory Module (SIMM) sockets: SIMM 1, SIMM 2, SIMM 3, and SIMM 4, that can support 8 banks of memory.

Each 72-pin SIMM socket can use single density or double density memory modules. Each socket accepts one of the following modules.

- 1MB (256Kb x 36) single-sided SIMM
- 2MB (256Kb x 36 x 2) double-sided SIMM
- 4MB (1024Kb x 36) single-sided SIMM
- 8MB (1024Kb x 36 x 2) double-sided SIMM
- 16MB (4096Kb x 36) single-sided SIMM
- 32MB (4096Kb x 36 x 2) double-sided SIMM

Although the system board accepts combinations of different capacity memory modules, it does not allow you to combine different module capacities within a memory bank. All of the modules within a bank must be of the same type.

Minimum memory configuration for the system is 1MB. The maximum memory configuration is 128MB. See the following table for possible configurations.

Total	SIMM 1	SIMM 2	SIMM 3	SIMM 4
1M	1M	—	—	—
2M	1M	1M	—	—
5M	1M	4M	—	—
17M	1M	16M	—	—
4M	1M	1M	1M/1M	—
6M	1M	1M	4M	—
8M	1M	1M	1M/1M	4M
10M	1M	1M	4M	4M
18M	1M	1M	16M	—
2M	1M/1M	—	—	—
4M	1M/1M	1M/1M	—	—
6M	1M/1M	4M	—	—
8M	1M/1M	1M/1M	4M	—
12M	1M/1M	1M/1M	4M	4M
18M	1M/1M	16M	—	—
20M	1M/1M	1M/1M	16M	—
24M	1M/1M	1M/1M	4M	16M
36M	1M/1M	1M/1M	16M	16M
4M	4M	—	—	—
8M	4M	4M	—	—
12M	4M	4M	4M	—
16M	4M	4M	4M	4M
20M	4M	16M	—	—
24M	4M	4M	16M	—
36M	4M	16M	16M	—

Table 2-1. Memory Configurations

Total	SIMM 1	SIMM 2	SIMM 3	SIMM 4
40M	4M	4M	16M	16M
36M	4M	16M/16M	—	—
40M	4M	4M	16M/16M	—
68M	4M	16M/16M	16M/16M	—
72M	4M	4M	16M/16M	16M/16M
8M	4M/4M	—	—	—
16M	4M/4M	4M/4M	—	—
24M	4M/4M	4M/4M	4M/4M	—
32M	4M/4M	4M/4M	4M/4M	4M/4M
16M	16M	—	—	—
32M	16M	16M	—	—
48M	16M	16M	16M	—
64M	16M	16M	16M	16M
48M	16M	16M/16M	—	—
80M	16M	16M/16M	16M/16M	—
64M	16M	16M	16M/16M	—
96M	16M	16M	16M/16M	16M/16M
32M	16M/16M	—	—	—
64M	16M/16M	16M/16M	—	—
96M	16M/16M	16M/16M	16M/16M	—
128M	16M/16M	16M/16M	16M/16M	16M/16M

Table 2-1 (continued). Memory Configurations

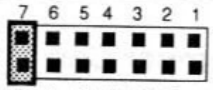
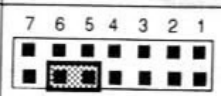
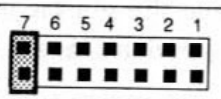
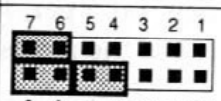
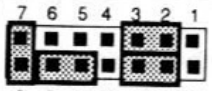
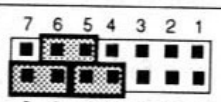
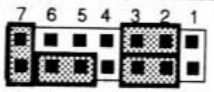
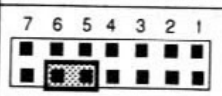
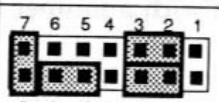
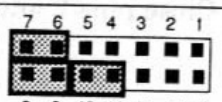
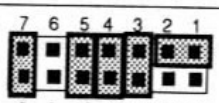
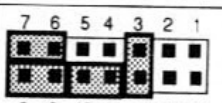
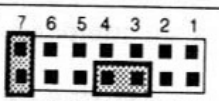
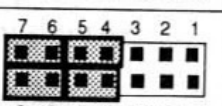
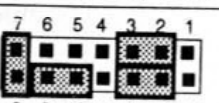
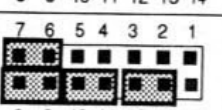
Total	SIMM 1	SIMM 2	SIMM 3	SIMM 4
12M	4M	4M/4M	—	—
20M	4M	4M/4M	4M/4M	—
28M	4M	4M/4M	4M/4M	4M/4M
16M	4M	4M	4M/4M	—
24M	4M	4M	4M/4M	4M/4M
24M	4M/4M	16M	—	—
32M	4M/4M	4M/4M	16M	—
40M	4M/4M	4M/4M	4M/4M	16M
48M	4M/4M	4M/4M	16M	16M
48M	4M/4M	4M/4M	16M/16M	—
80M	4M/4M	4M/4M	16M/16M	16M/16M

Table 2-1 (continued). Memory Configurations

CPU Type Jumpers: JC1, JC2, JC3, JC4

The SIS 486 supports several types of CPU. Some board models have an optional Zero Insertion Force (ZIF) Socket. For the board to recognize the type of CPU installed, you must set jumpers as below. See Figure 1-1 for jumper locations.

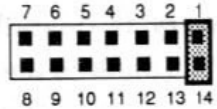
CPU Type Settings: JC1, JC2, JC3, JC4

CPU	JC1	JC2	JC3	JC4
486SX				
486DX				
Over-drive				
SX-SL				
DX-SL				
M7				
AMD-DXL				
DX4				

See Notes on the following page.

Notes:

1. If you use a 3.3V CPU (not including the P24C), short pins 1-14 of JC2.

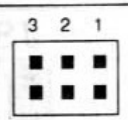
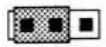
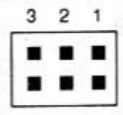
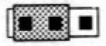
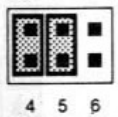
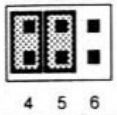
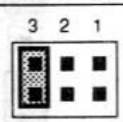
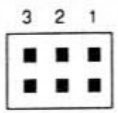
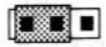
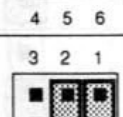
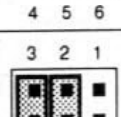


2. AMD-DXL CPUs are not supported by the SIS85C-471 E version chipset. If you want to use this CPU, use the same jumper settings as for the 486DX.
3. The SIS 85C471 G version completely supports the specs for AMD-DXL, Cyrix M7, and Intel S-Series CPUs. Set the CPU type jumpers as described on the previous page.

CPU Clock Selection: JK1, JK2

Jumpers JK1 and JK2 select the frequency of the clock generator chip (G clock). See Figure 1-1 for jumper locations.

JK1, JK2 Settings

Clock	JK1	JK2	Clock	JK1	JK2
25 MHz			**DX2-50**		
33 MHz			**DX2-66**		
40 MHz			**DX4-75**		
50 MHz			**DX4-100**		

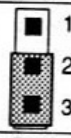
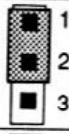
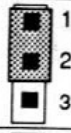
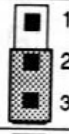
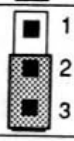
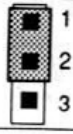
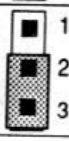
Cache Memory Selection: JS1, JS2, JS3

The system board supports 128K/256K/512K of cache memory. You configure cache memory by installing SRAM chips in Data RAM socketsU23~U26 (Bank 0) and U17~U20 (Bank 1), and in Tag RAM socket U21, and then setting the cache jumpers JS1, JS2, and JS3. Note that the speed required for SRAM chips is 20ns.

Cache Size and Memory Locations

Cache Size	Tag RAM (U21)	Data RAM (U23~U26)	Data RAM (U17~U20)
128K	8, 16, 32K8	32K8	None
256K	16, 32K8	32K8	32K8
256K	16, 32K8	64K8	None
512K	32K8	128K8	None

Cache Size Selection: JS3, JS2, JS1

Cache Size	JS3	JS2	JS1
128K (32K x 4)			
256K (32K x 8)			
256K (64K x 4)			
512K (128K x 4)			

VL-Bus Master Setting: JP2, JP3

Set JP2 and JP3 to configure the VL-Bus for use with zero wait state or one wait state, and CPU speed.

JP2 Settings

High Speed Write	JP2
Zero Wait State	
One Wait State (Default)	

JP3 Settings

CPU Speed	JP3
< = 33 MHz	
> 33 MHz