

SIS 486
SYSTEM BOARD
USER'S MANUAL

MS-4126
Version 2.2

FCC-B Radio Frequency Interference Statement

This equipment has been tested and found to comply with the limits for a class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Notice 1

The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Notice 2

Shielded interface cables and A.C. power cord, if any, must be used in order to comply with the emission limits.

**VOIR LA NOTICE D' INSTALLATION AVANT
DE RACCORDER AU RESEAU.**

Edition

June 1993

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CHAPTER 1

Introduction

The SIS 486 system board is a high-performance personal computer system board based on an 80486 microprocessor running at 25/33/40/50 MHz. The board offers an optional surface mounted CPU, as well as a socket for a hand-inserted CPU.

A cache subsystem can be configured for 128Kb, or 256Kb cache memory to improve overall throughput. The board also features three 32-bit Local Bus slots for the VESA standard.

The SIS 486 system board uses the highly integrated SIS 85C461 VTQ chip that integrates all system control functions.

System Board Specifications

CPU:

- 80486DX/SX-50, 40, 33, 25 (inserted)
- 80486SX (SMT)
- 80486DX2-50, 66
- 80487SX

Cache memory:

- Supports 128K/256K cache memory

Main memory:

- Supports 256K, 1M, and 4M SIMM module DRAM.
- 80ns Fast Page mode DRAM required
- Up to 32 Mbytes on-board memory

Slots:

- Two 32-bit VESA Local Bus Master slots and one 32-bit VESA Local Bus Slave slot.
- Four 16-bit AT bus slots

Battery:

- 3.6V/60mA on-board rechargeable battery

Dimensions:

- 26cm x 22.1cm x 4 layers

Mounting:

- 6 mounting holes

System Board Layout

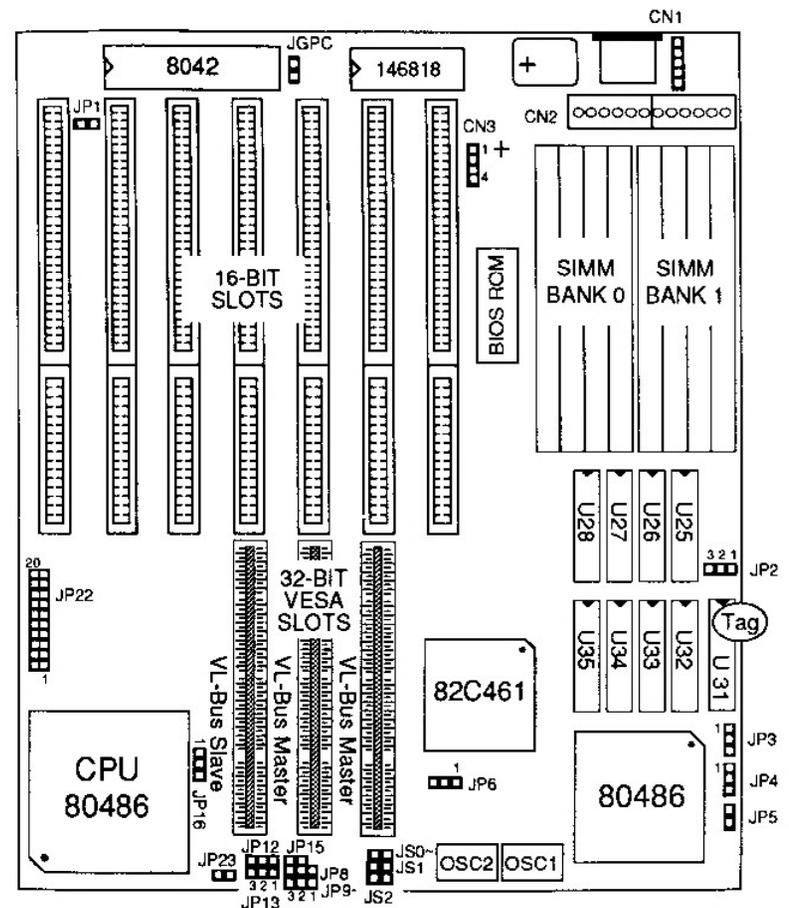


Figure 1-1. System board Layout

CHAPTER 2

Hardware Installation

When you install the SIS 486 system board, you must configure components, set jumpers, and attach connectors.

Quick Reference

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Jumpers and Connectors

Refer to Figure 1-1 for jumper and connector locations.

Jumpers

Jumpers on the system board provide information to your operating system about installed options and system settings. You need to configure jumpers when you install a CPU, select cache size, add an external battery, or clear CMOS memory.

Connectors

Connectors attach control panel switches and indicators, as well as the speaker, external battery, keyboard and power supply.

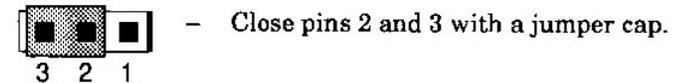
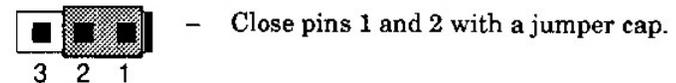
Setting Jumpers

Configure system board options by setting jumper switches. Use your fingers to position a jumper cap over the desired pin setting and gently press down.

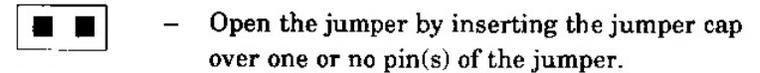
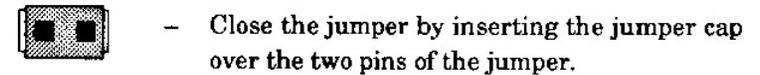
Note: When you open a jumper, leave the plastic jumper cap attached to one of the pins so you don't lose it.

Symbols:

For 3-pin jumpers, the following symbols are used:



For 2-pin jumpers, the following symbols are used:

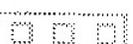
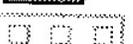
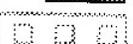
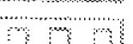
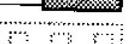
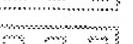


CPU Type Selectors: JP12, JP13, JP15

The SIS 486 system board can support several types of CPU. Note that some models of the system board may have an optional Zero Insertion Force (ZIF) Socket for CPUs.

To configure the system board to recognize which type of CPU is installed, you must set jumpers JP12, JP13, and JP15 as below. See Figure 1-1 for jumper locations.

CPU Type Settings: JP12, JP13, JP15

CPU	Settings
486SX	<p style="text-align: center;">3 2 1 JP15</p> <p>JP12  </p> <p>JP13  </p> <p> </p>
487SX	<p style="text-align: center;">3 2 1 JP15</p> <p>JP12  </p> <p>JP13  </p> <p> </p>
486DX/DX2	<p style="text-align: center;">3 2 1 JP15</p> <p>JP12  </p> <p>JP13  </p> <p> </p>

CPU Clock Selection: JS0, JS1, JS2

Jumpers JS0, JS1 and JS2 select the frequency of the clock generator chip (G clock). Note that if oscillators (OSC1, OSC2) are installed, the settings of these jumpers have no effect. See Figure 1-1 for the location of the jumpers.

JS0, JS1, JS2 Settings

Jumper	25 MHz	33 MHz	40 MHz	50 MHz
JS0				
JS1				
JS2				

SMT CPU Selection: JP5

Enable jumper JP5 if a surface mounted CPU is on the board. Disable JP5 if a hand-inserted CPU is installed. See Figure 1-1 for the location of the jumper.

JP5 Settings

SMT CPU	Setting
Enabled	
Disabled	

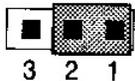
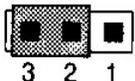
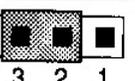
Cache Memory Selection: JP2~JP4, JP6

The system board supports 128K or 256K of cache memory. You configure cache memory by installing 8K8 or 32K8 SRAM chips in Data RAM sockets U25~U28 and U32~U35, and in Tag RAM socket U31, and then setting the cache jumpers JP2, JP3 and JP4. Note that the speed required for SRAM chips is 20ns.

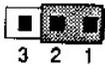
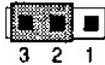
Cache Size and Memory Locations

Cache Size	Tag RAM (U31)	Data RAM (U25~U28)	Data RAM (U32~U35)
128K	8K8	None	32K8
256K	32K8	32K8	32K8

Cache Size Selection: JP2, JP3, JP4

Cache Size	JP2	JP3	JP4
128K			
256K			

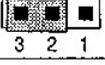
JP6 Settings

CPU Speed	JP6
= 50 MHz or For Cyrix CPU	
< 50 MHz (25, 33, 40)	

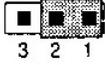
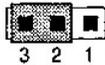
VL-Bus Master Setting: JP8, JP9

Set JP8 to configure the VL-Bus for zero wait state or one wait state.

JP8 Settings

High Speed Write	JP8
Zero Wait State	
ONE Wait State (Default)	

JP9 Settings

CPU Speed	JP9
< = 33 MHz	
> 33 MHz (Default)	

Special VL-Bus Setting: JP23

Short JP23 as below and then add a 150P capacitor on signal /BS16 when using the Genoa or other special V-L Bus VGA Card. The default setting is open.

JP23 Settings

Description	JP23
Setting for Special V-L Bus Cards	
Normal (Default)	

Memory Bank Configuration

The SIS 486 system board supports two memory banks on-board, numbered bank 0 and bank 1. Each bank consists of four Single In-line Memory Module (SIMM) sockets. Each socket accepts a 256K SIMM, a 1M SIMM or a 4M SIMM.

Although the system board accepts combinations of different capacity memory modules, it does not allow you to combine different module capacities within a memory bank. All of the modules within a bank must be of the same type.

Minimum memory configuration for the system is 1MB (four 256K SIMMs installed in bank 0.) The maximum memory configuration is 32M. See Table 2-1 below for possible configurations.

Bank 0	Bank 1	Memory
256K	—	1M
256K	256K	2M
1M	—	4M
256K	1M	5M
1M	256K	5M
1M	1M	8M
4M	—	16M
256K	4M	17M
4M	256K	17M
1M	4M	20M
4M	1M	20M
4M	4M	32M

Table 2-1. Memory Configurations

Display Adaptor Selection: JP1

If you are using a monochrome or color (CGA) display adaptor you must set the jumper JP1. If you are using an EGA or VGA adaptor, the JP1 setting is irrelevant. See Figure 1-1 for jumper location.

Display Adaptor Jumper: JP1

Display type	JP1
Color Graphics Adaptor	
Monochrome Adaptor (default)	

Keyboard Connectors: CN1

The system board offers the choice of two connectors for attaching a keyboard. See figure 1-1 for connector locations.

Keyboard Connector - DIN

You can plug a keyboard cable directly into the standard five-pin female DIN connector.

Keyboard Connector - PIN

The five-pin male PIN connector attaches to an extended keyboard cable for PIN to DIN connection. It is suitable for connecting to a DIN connector at the front of the case, which then connects to the keyboard cable jack.

Power Supply Connector: CN2

The power supply connector is a twelve-pin male connector. Dual connectors from the power supply can fit in only one direction. Make sure to attach the connectors with the two black wires at the center, as show in the diagram below. See Figure 1-1 for the connector's location.

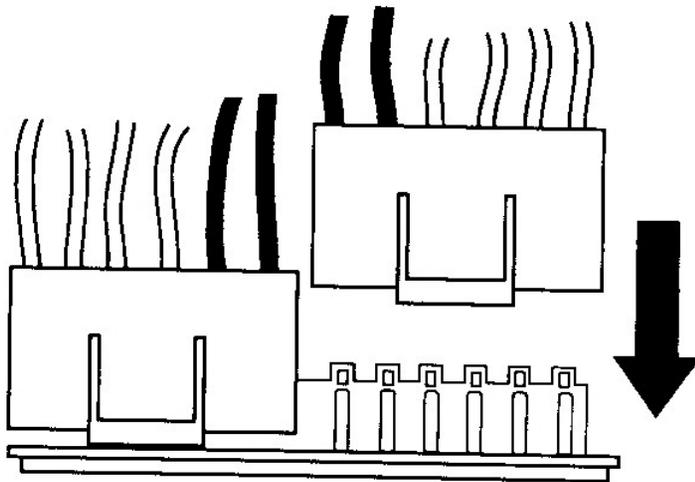


Figure 2-1. Attaching Power Supply Connectors

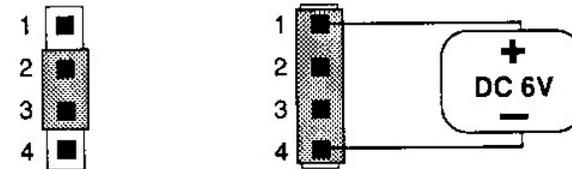
Connector Pin Description

Pin	Description	Pin	Description
1	Power Good	1	Ground
2	+5V DC	2	Ground
3	+12V DC	3	-5V DC
4	-12V DC	4	+5V DC
5	Ground	5	+5V DC
6	Ground	6	+5V DC

External Battery Connector: CN3

A battery must be used to retain the system board configuration in CMOS RAM. You can use either the on-board rechargeable battery or an external battery. If you use the on-board rechargeable battery you must short pins 2-3 of CN3. For an external battery, the battery's cable connector attaches to pins 1 and 4 of CN3. See Figure 1-1 for the connector's location.

CN3: External Battery Connector



Jumper Setting
for using
on-board Battery

External Battery
Connection

Figure 2-2. Setting the External Battery Connector - CN3

Reserve Jumpers: JP16

CPU Type	JP16
DX-50, DX-40	
Others	

Case Connector Block: JP22

The Turbo LED, Turbo switch, Hardware Reset, Keylock, Power LED, and Speaker are all connected to the JP22 Connector Block as shown below. See Figure 1-1 for the connector block's location.

JP22: Case Connector Block

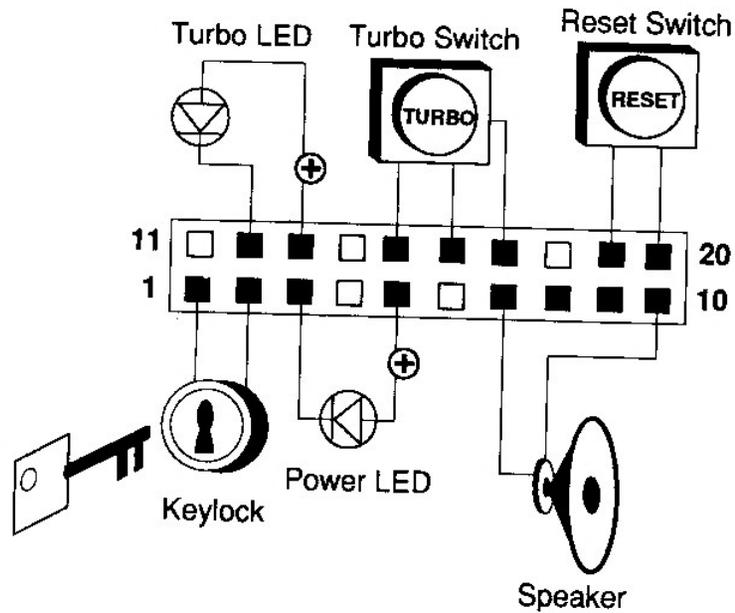


Figure 2-3. Case Connector Block - JP22

CHAPTER 3

AMI BIOS Setup

The system contains user modifiable system configuration and chipset internal register information in the CMOS RAM. This information is retained by a battery when the power is turned off.

You can modify this system information with the system's BIOS setup program. The system board comes with the AMI BIOS setup program from American Megatrends Inc.

AMI BIOS Setup

Enter the AMI Setup program's Main Menu as follows:

1. Turn on or reboot the system. The following screen appears with a series of diagnostic checks.

```
AMI-BIOS (C) 1992 American Megatrends Inc.,
A75X 051493
```

```
XXXX KB OK
```

```
Hit <DEL>, if you want to run SETUP
```

```
(C) American Megatrends Inc.,
```

```
40-0100-001169-00101111-111192-SIS461
```