# PATX5000
# Dual Pentium® III
# ATX Motherboard

# Installation and Use

**PATX5A/IH1**

May 2001 Edition

# Safety Summary

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

## Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. If the equipment is supplied with a three-conductor AC power cable, the power cable must be plugged into an approved three-contact electrical outlet, with the grounding wire (green/yellow) reliably connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards and local electrical regulatory codes.

## Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in any explosive atmosphere such as in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment could result in an explosion and cause injury or damage.

## Keep Away From Live Circuits Inside the Equipment.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Service personnel should not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, such personnel should always disconnect power and discharge circuits before touching components.

## Use Caution When Exposing or Handling a CRT.

Breakage of a Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, do not handle the CRT and avoid rough handling or jarring of the equipment. Handling of a CRT should be done only by qualified service personnel using approved safety mask and gloves.

## Do Not Substitute Parts or Modify Equipment.

Do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that all safety features are maintained.

## Observe Warnings in Manual.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

**Warning**

To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.

## Flammability

All Motorola PWBs (printed wiring boards) are manufactured with a flammability rating of 94V-0 by UL-recognized manufacturers.

## EMI Caution


This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used with adequate EMI protection.

## CE Notice (European Community)

Motorola Computer Group products with the CE marking comply with the EMC Directive (89/336/EEC). Compliance with this directive implies conformity to the following European Norms:

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>
> EN50082-1:1997 “Electromagnetic Compatibility—Generic Immunity Standard, Part 1. Residential, Commercial and Light Industry”

System products also fulfill EN60950 (product safety) which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

Board products are tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a CE-marked system will maintain the required EMC/safety performance.

In accordance with European Community directives, a “Declaration of Conformity” has been made and is on file within the European Union. The “Declaration of Conformity” is available on request. Please contact your sales representative.

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# Contents

## About This Book



## CHAPTER 1 Hardware Preparation and Installation

## CHAPTER 2 BIOS Self-Test and Startup



## CHAPTER 3 Functional Description



## CHAPTER 4 Connector Pin Assignments



## APPENDIX A Specifications

## APPENDIX B Thermal Validation



## APPENDIX C Battery Replacement



## APPENDIX D Related Documentation

# List of Figures

# List of Tables

# About This Book

The *PATX5000 Dual Pentium® III ATX Motherboard Installation and Use* manual provides general information, instructions for hardware preparation and installation, operating instructions, a functional description, and various types of interfacing information for the PATX5000 family of ATX form factor boards.

PATX5000 series boards are a high-performance, long-life embedded platform for operating systems such as Windows NT® and Linux®. Powered by dual Pentium III Socket 370 processors in tandem with a high-speed Intel® 840 chipset operating at up to 133MHz processor-side bus speeds with dual Rambus memory channels supporting up to 2GB of memory at up to 400MHz bus speeds, the PATX5000 series provides robust building blocks for a variety of industrial applications. With its versatile combination of performance and functionality, the board is well suited for embedded applications in such areas as semiconductor manufacturing, voice-over IP, high-speed data communications, medical imaging, and high-resolution color printing. The information in this manual applies to the following PATX5000 boards and accessories.

| **Part Number** | **Description** |
|---|---|
| PATX5000-101 | Single Ethernet, no SCSI |
| PATX5000-102 | Single Ethernet, dual-channel Ultra2 SCSI |
| PATX5000-103 | Dual Ethernet, dual-channel Ultra2 SCSI |
| Processor Options | |
| IA-CPU-733-01-F/K | 733MHz Pentium III CPU, 133MHz processor-side bus, active heatsink |
| IA-CPU-866-01-F/K | 866MHz Pentium III CPU, 133MHz processor-side bus, active heatsink |
| IA-CPU-TERM-01-F/K | CPU terminator (required in single-CPU configuration) |
| I/O Shield Options | |
| ATXIO-101-K | I/O shield for one Ethernet interface |
| ATXIO-102-K | I/O shield for two Ethernet interfaces |
| ECC Rambus Memory Options (128MB with ECC) | |
| RIMM-128-03-F | Two PC800 RIMMs and two CRIMMs |
| RIMM-128-04-F | Four PC800 RIMMs |

| Part Number | Description |
|---|---|
| ECC Rambus Memory Options (256MB with ECC) | |
| RIMM-256-03-F | Two PC800 RIMMs and two CRIMMs |
| RIMM-256-04-F | Four PC800 RIMMs |
| ECC Rambus Memory Options (512MB with ECC) | |
| RIMM-512-03-F | Two PC800 RIMMs and two CRIMMs |
| RIMM-512-04-F | Four PC800 RIMMs |

# Overview of Contents

This manual is divided into the following chapters and appendices:

- Chapter 1, *Hardware Preparation and Installation*: guidelines for preparing and installing the board
- Chapter 2, *BIOS Self-Test and Startup*: a description of procedures for startup and operation of the board
- Chapter 3, *Functional Description*: an overview of the main board components
- Chapter 4, *Connector Pin Assignments*: a tabulation of board connector pin assignments
- Appendix A, *Specifications*: electrical and mechanical board specifications
- Appendix B, *Thermal Validation*: thermally significant components on the board
- Appendix C, *Battery Replacement*: procedures for replacement of the lithium battery on the board and guidelines as to its service life
- Appendix D, *Related Documentation*: other publications that may be helpful in using the board

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In all your correspondence, please list your name, position, and company. Be sure to include the title and part number of the manual and tell how you used it. Then tell us your feelings about its strengths and weaknesses and any recommendations for improvements.

# Terminology

A pound sign (#) following the signal name for signals which are *level significant* denotes that the signal is *true* or valid when the signal is low.

A pound sign (#) following the signal name for signals which are *edge significant* denotes that the actions initiated by that signal occur on high-to-low transitions.

Data and address sizes are defined as follows:

- A *byte* is eight bits, numbered 7 through 0, with bit 7 being the most significant.
- A *half-word* is 16 bits, numbered 15 through 0, with bit 15 being the most significant.
- A *word* or *single word* is 32 bits, numbered 31 through 0, with bit 31 being the most significant.
- A *double word* is 64 bits, numbered 63 through 0, with bit 63 being the most significant.

# Conventions Used in This Manual

The following typographical conventions are used in this document:

**bold**

is used for user input that you type just as it appears; it is also used for commands, options and arguments to commands, and names of programs, directories and files.

*italic*

is used for names of variables to which you assign values. Italic is also used for comments in screen displays and examples, and to introduce new terms.

`courier`

is used for system output (for example, screen displays, reports), examples, and system prompts.

**<Enter>**, **<Return>** or **<CR>**

represents the carriage return or Enter key.

**Ctrl**

represents the Control key. Execute control characters by pressing the **Ctrl** key and the letter simultaneously, for example, **Ctrl-d**.

# Hardware Preparation and Installation

1

## Introduction

This chapter describes the equipment you need and the tasks you will perform to set up a PATX5000-based system.

### Equipment Required

To complete a PATX5000 system, you need the following equipment:

- ❏ Enclosure or chassis with power supply
- ❏ Display console (or monitor with video card)
- ❏ Operating system, application software, etc.

## Overview of Installation Procedure

The following table lists the things you will need to do to use this board and tells where to find the information you need to perform each step. Be sure to read this entire chapter, including all cautions and warnings, before you begin.

**Table 1-1. Startup Overview**

| What you need to do... | Refer to... |
|---|---|
| Unpack the hardware. | *Guidelines for Unpacking* on page 1-2. |
| Configure the PATX5000 series motherboard as appropriate to your application by setting jumpers. | *Hardware Configuration* on page 1-4. |
| If necessary, install an I/O shield on the board. | *I/O Shield* on page 1-15. |
| Install the PATX5000 series motherboard in the chassis. | *Motherboard* on page 1-16. |

**Table 1-1. Startup Overview (continued)**

| What you need to do... | Refer to... |
|---|---|
| Ensure that the processors are properly installed on the motherboard. | *CPU Cooler* on page 1-21. |
| Ensure that memory modules are properly installed on the board. | *RIMM Memory* on page 1-24. |
| If applicable, install an AGP module on the motherboard. | *AGP Graphics Card* on page 1-25. |
| If applicable, install PCI expansion card(s) on the board. | *PCI Expansion Cards* on page 1-27. |
| If applicable, install ISA module(s) on the board. | *ISA Modules* on page 1-29. |
| If applicable, install an IDE CompactFlash card on the board. | *IDE CompactFlash* on page 1-30. |
| Connect a display terminal and any other equipment you will be using. | *Connection to Peripherals* on page 1-32. |
| | For more information on optional devices and equipment, refer to the documentation provided with the equipment. |
| Power up the system. | *Initial Conditions* on page 2-1. |
| Note that the BIOS firmware initializes and tests the board. | *Initial Conditions* on page 2-1. |
| | You may also wish to consult the *BIOS and Programmer's Reference Guide*, listed in Appendix D, *Related Documentation*. |
| Initialize the system clock. | *Configuration Information* on page 2-1. |
| Program the board as needed for your applications. | *PATX5000 BIOS and Programmer's Reference Guide*, listed in Appendix D, *Related Documentation*. |

# Guidelines for Unpacking

If the shipping carton is damaged upon receipt, request that the carrier's agent be present during the unpacking and inspection of the equipment.

**Caution**

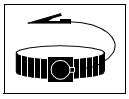
When unpacking, avoid touching areas of integrated circuitry; static discharge can damage circuits.

Refer to the packing list and verify that all items are present. Save the packing material for storing and reshipping of equipment.

# Installation Preliminaries

This section applies to all hardware installations you may perform that involve the PATX5000 board.

**Use ESD**



**Wrist Strap**

Motorola strongly recommends the use of an antistatic wrist strap and a conductive foam pad when you install or upgrade the board. Electronic components can be extremely sensitive to ESD. After removing the board from the chassis or from its protective wrapper, place the board flat on a grounded, static-free surface, component side up. Do not slide the board over any surface.

If no ESD station is available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores). Place the strap around your wrist and attach the grounding end (usually a piece of copper foil or an alligator clip) to an electrical ground. An electrical ground can be a piece of metal that literally runs into the ground (such as an unpainted metal pipe) or a metal part of a grounded electrical appliance. An appliance is grounded if it has a three-prong plug and is plugged into a three-prong grounded outlet. You cannot use the chassis in which you are installing the PATX5000 itself as a ground, because the enclosure is unplugged while you work on it.

**Warning**

Turn the system's power off before you perform these procedures. Failure to turn the power off before opening the enclosure can result in personal injury or damage to the equipment. Hazardous voltage, current, and energy levels are present in the chassis. Hazardous voltages may be present on power switch terminals even when the power switch is off. Never operate the system with the cover removed. Always replace the cover before powering up the system.

# Hardware Configuration

To produce the desired configuration and ensure proper operation, you may need to set jumpers or carry out other hardware modifications before you install the PATX5000 series motherboard.

Some PATX5000 motherboard functions, such as the timers, are controlled in software by setting bits in registers. (PATX5000 control registers are described in the *PATX5000 BIOS and Programmer's Reference Guide* or in vendor documentation as listed in the *Related Documentation* appendix.)

Many operating parameters, however, are controlled through manual installation or removal of header jumpers on the motherboard.

**Caution**

When setting jumpers, avoid touching areas of integrated circuitry; static discharge can damage circuits.

# Preparing the Board

Figure 1-1 illustrates the placement of the jumper headers, connectors, and various other components on the PATX5000 motherboard.

## Setting Jumpers

Manually configurable jumper headers on the motherboard are listed in the following table. Default settings are enclosed in brackets. For the functions of the *connector* headers on the PATX5000, refer to Table 1-3.

### Table 1-2. PATX5000 Jumper Settings

| Jumper | Function | Settings | |
|---|---|---|---|
| J8 | CompactFlash configuration | 1-2<br>[No jumper] | CompactFlash is master device<br>CompactFlash is slave device |
| J9 | Backup battery selection | [1-2]<br>No jumper | On-board battery selected<br>External battery selected (cable installed) |
| J23 | USB Port 1 routing | [1-3, 2-4, 9-10]<br>3-5, 4-6, 7-8 | Rear panel connector J7 selected<br>Board connector header J20 selected |
| J27 | Factory use only | [1-2]<br>2-3 | Normal operation<br>Factory use only |
| J30 | Speaker selection | No jumper<br>[25-26] | PC alarm beeps routed to chassis speaker<br>PC alarm beeps routed to on-board speaker |
| J34 | CMOS restore from backup | 1-2<br>[2-3] | CMOS restore from EEPROM not enabled<br>CMOS restore from EEPROM enabled |
| J37 | Boot block write protection | [1-2]<br>No jumper | Write protection on (writes disabled)<br>Write protection off (writes enabled) |
| J41 | FPGA EEPROM program enable | 1-2<br>[No jumper] | FPGA EEPROM programming enabled<br>FPGA EEPROM programming disabled |

**Notes**

1. Items in brackets are factory default settings.
2. J9 is also used in clearing CMOS (refer to *Clearing CMOS* on page 1-9).

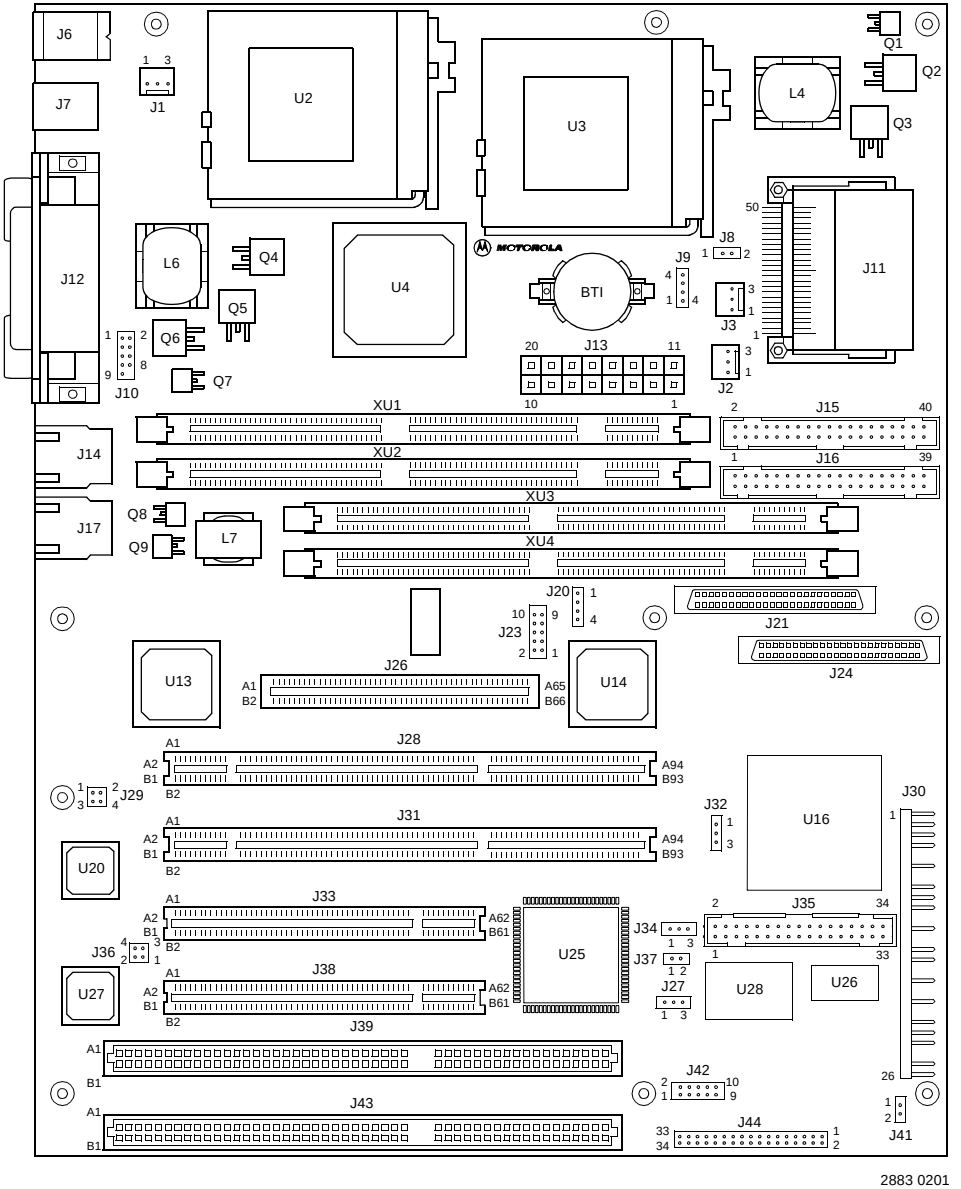



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**Figure 1-1. PATX5000 Board Layout**

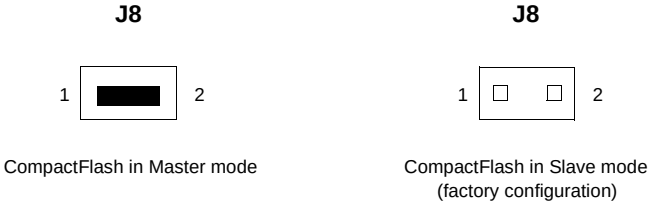
The PATX5000 motherboard is tested and shipped with the configurations described in the following sections. The PATX5000's required and factory-installed BIOS performs its Power-Up Self-Test (POST) with those factory settings.

## CompactFlash Configuration (J8)

The CompactFlash™ cards which can be used on the PATX5000 contain an intelligent controller for management of the Flash media. The CompactFlash implementation mimics the file structure of a hard disk drive. These characteristics make it possible for the PATX5000 to treat the CompactFlash card as a bootable device.

With a jumper installed across J8 pins 1-2, the CompactFlash device is in ''master'' mode. This configuration enables the PATX5000 to boot from the CompactFlash card.

With the jumper removed from J8 (the factory configuration), the CompactFlash device is in ''slave'' mode. This configuration allows the PATX5000 to boot from a source other than the CompactFlash.




CompactFlash in Master mode

CompactFlash in Slave mode (factory configuration)

### Custom Configurations

MCG Engineering has identified a hardware incompatibility in applications that employ IBM MicroDrive cards: The PATX5000's factory configuration does not support DMA transfer modes for IBM MicroDrives.

If you anticipate using IBM MicroDrives capable of DMA transfers, it will be necessary to manually set the MicroDrive parameters via the Setup utility. You do this as follows:

1. During POST (the power-on self-test), start the Setup utility by pressing <F2>.
2. After the main Setup screen appears, go to the Advanced menu and select the IDE Configuration submenu.
3. On the IDE Configuration submenu, step down to Secondary Master (or Secondary Slave) to select the MicroDrive device for configuration.
4. Change the Type selection from "Auto" to "User".
5. Set the Transfer Mode option to a non-DMA mode (i.e., use the fastest PIO mode supported by the MicroDrive device).
6. Set the LBA Mode option to "Enabled".
7. Press <F10> to leave the Setup utility with the "Exit Saving Changes" option.

If your application requires that you use DMA transfer modes with the IBM MicroDrive device, contact your MCG representative for guidance.

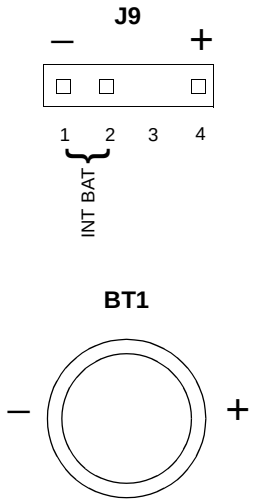
## Backup Battery Selection and Clearing CMOS (J9)

BT1 is the socket for the on-board battery. Jumper header J9 is the battery backup configuration point. J9 is also used in clearing CMOS RAM when necessary.

### Configuring the Battery Backup

To configure the PATX5000 for on-board battery backup, verify that a battery (part number CR2032) is installed securely in socket BT1. Then jumper J9 pins 1-2 together to enable the on-board battery (this is the factory default).

To use an external battery for backup, remove the jumper from pins 1-2 and instead connect the external battery cable to J9. Pin 1 connects to the negative side of the external battery, pin 4 to the positive side.




## Clearing CMOS

Jumper header J9 is also used in clearing CMOS RAM when necessary. To clear CMOS RAM, perform the following steps:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to a suitable ground as described under *Installation Preliminaries* on page 1-3. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Switch off the power to the board.
3. Remove standby power from the board (either by removing AC power from the PATX5000 power supply, or by unplugging the supply from POWER IN board connector J13).

**Caution**

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

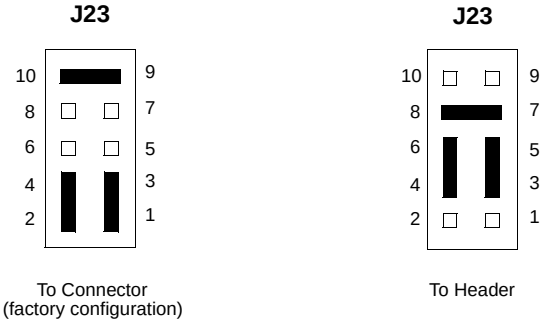
4. Disconnect the backup battery connection at J9 for a minimum of 30 seconds.
5. Reconnect the backup battery connection at J9.
6. Restore standby power to the board.

When the CMOS memory is cleared, the BIOS default settings take over unless the CMOS Restore from Backup function is enabled (refer to *CMOS Restore from Backup (J34)* on page 1-12).

## USB Port 1 Routing (J23)

The PATX5000 is equipped with two USB (Universal Serial Bus) ports. The primary port (Port 0) is routed to a USB panel connector. The secondary USB port (Port 1) may be directed either to a panel connector or to a connector header on the board.

J23 is the *2ND USB* routing header. The setting of J23 determines whether I/O signals on USB port 1 are directed to a panel connector or to a connector header on the board. The default factory configuration has jumpers between pins 1-3, 2-4, and 9-10, directing the signals to the upper panel connector of J7. To route the signals to board connector header J20, place the jumpers between pins 3-5, 4-6, and 7-8.



## Factory Use (J27)

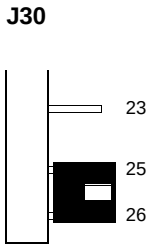
J27 is used during the board manufacturing process. It is for factory use only. The jumper should remain installed on J27 pins 1-2 in normal operation.


Factory Use Only

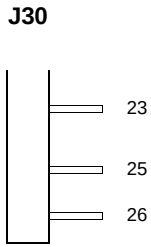

Normal Operation
(factory configuration)

## Speaker Selection (J30)

Pins 25-26 on header J30 enable or disable the PATX5000's internal speaker. The setting of those pins determines whether audio signals (standard PC alarm beeps) on the board are applied to the onboard speaker or to an external speaker. The default factory configuration has a jumper between J30 pins 25-26, enabling the onboard speaker. To route the beeps to an external speaker, remove the jumper from pins 25-26 and attach the speaker leads to pins 23 (+ side) and 26 (– side).




Onboard speaker enabled
(Factory configuration)




Onboard speaker disabled
(External speaker to pins 23/26)

## CMOS Restore from Backup (J34)

Using the Setup utility, you have the ability to modify the BIOS configuration stored in CMOS RAM in the Intel 82801 I/O Control Hub (ICH). When you select the "Exit Saving Changes" option as you leave the Setup utility, a copy of the CMOS RAM contents is stored in serial EEPROM. Should the BIOS configuration in CMOS RAM become corrupted, you may wish to retrieve a valid BIOS image from the backup copy in EEPROM. The setting of J34 determines whether a corrupted CMOS configuration will be restored from the serial EEPROM image.

The factory configuration has a jumper between J34 pins 2-3: If the BIOS detects that the CMOS image has been corrupted, the CMOS will be restored from the copy in EEPROM. If you move the jumper to J34 pins 1-2, the CMOS Restore from Backup function is disabled.


CMOS Restore enabled
(factory configuration)


CMOS Restore disabled

While the BIOS is booting, it calculates a checksum of the CMOS contents. If the checksum is valid, the POST continues. If the checksum is invalid, the BIOS reads the setting of J34.

If J34 indicates that the CMOS Restore from Backup function is not enabled, the BIOS loads a fresh copy of the default configuration from Flash memory. If J34 indicates that the CMOS Restore from Backup function is enabled, AND the EEPROM is found to contain a valid image, then the BIOS will restore the CMOS contents from the serial EEPROM image and booting continues normally.

If the CMOS Restore from Backup function is enabled but the EEPROM image is invalid, the CMOS contents will be restored from the BIOS defaults in Flash memory and those default values will be used to boot the system.

If the BIOS configuration data becomes corrupted while you are operating the board with the CMOS Restore from Backup function enabled, you may need to momentarily disable the backup, clear CMOS, and reconfigure the BIOS. This is done as follows:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to a suitable ground as described under *Installation Preliminaries* on page 1-3. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Turn off the power to the board.


**Caution**

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

3. Move the jumper on J34 from pins 2-3 to pins 1-2, disabling the CMOS Restore from Backup function.
4. Clear the CMOS RAM as described under *Clearing CMOS* on page 1-9.
5. Turn on the power to the board, start the Setup utility, and reconfigure the BIOS as needed (refer to Chapter 2, *BIOS Self-Test and Startup*). As you leave the Setup utility, select the "Exit Saving Changes" option to copy the CMOS customizations to the serial EEPROM.
6. Power down the board once more. Return the jumper on J34 to pins 2-3, reenabling the the CMOS Restore from Backup function.
7. Power up the board once more. The board will reinitialize using the BIOS configuration data you have entered.

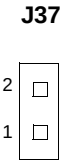
## Boot Block Write Protection (J37)

Header J37 controls the write protect flag for the boot block segment of Flash memory, which contains the BIOS firmware used at system startup. (The BIOS is originally loaded at the factory, but the contents of the boot block can be reprogrammed if necessary.) The factory configuration has a jumper on J37 pins 1-2, indicating to the BIOS that no writes to the boot

block should be attempted. Removing the jumper allows you to reprogram the boot block portion of Flash ROM.

**Caution**

Reprogramming the boot block will erase its existing contents, disabling the board until the procedure is complete. It cannot be undone. Unless you are sure that you wish to do this, do **not** remove the jumper from J37.

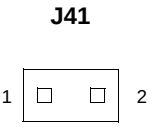



Flash boot block write-enabled

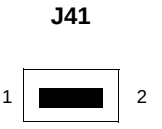

Flash boot block write-protected (factory configuration)

## FPGA Program Enable (J41)

Header J41 is the FPGA configuration EEPROM program enable header. Putting a jumper on J41 pins 1-2 permits reprogramming of the FPGA configuration EEPROM. J41 is empty in the factory configuration, leaving the configuration EEPROM write-protected.




FPGA EEPROM write-protected (factory configuration)




FPGA EEPROM write-enabled

# Installing the Hardware

With headers properly configured, you are ready to mount (if necessary) the I/O shield and install the PATX5000 motherboard in a chassis or system

enclosure. You can then plug the CPUs, memory modules, CompactFlash card and the various application-specific daughter boards into the motherboard and cable up the peripherals. Proceed as described in the following sections to accomplish these tasks.

## I/O Shield

The I/O shield for the PATX5000 fits all ATX-compliant chassis. The shield must be in place before you install the board in a chassis. To install the I/O shield, refer to the illustration and follow the procedure below.

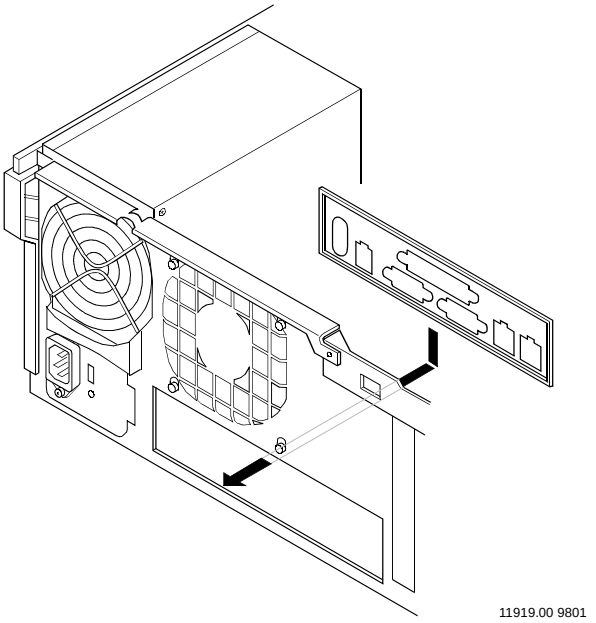
No tools are necessary for this procedure.

**Warning**

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

1. Remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the card cage.
2. Position the I/O shield in the connector cutout from within the chassis.

3. Press the edges of the I/O shield until the shield snaps into place.




## Motherboard

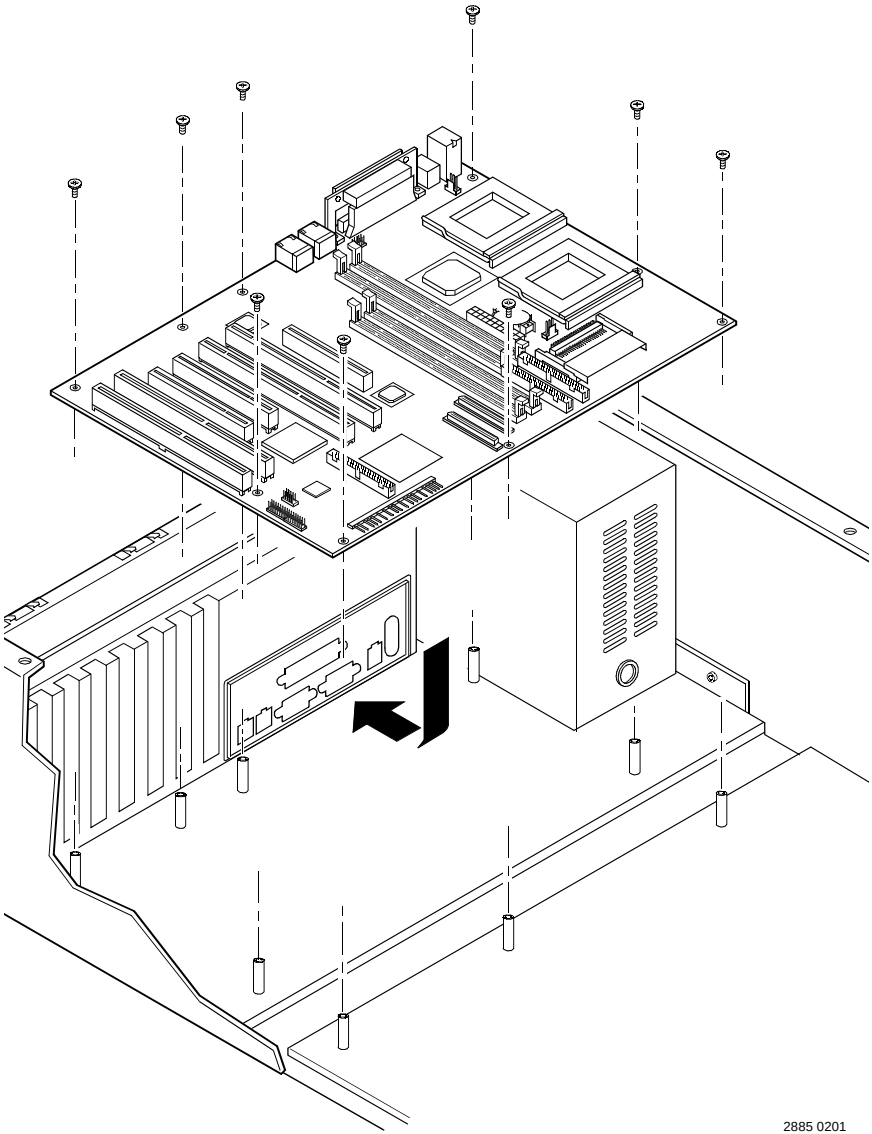
To install the PATX5000 board in a chassis (user-supplied), refer to the illustration and follow the steps below.

You need a Phillips screwdriver for this procedure. Depending on the design of the board-to-chassis standoffs, you may need a hex nut driver, typically $^{3}/_{16}$-inch, as well.

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to a suitable ground as described under *Installation Preliminaries* on page 1-3. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the card cage.

**Caution**

Inserting or removing modules with power applied may result in damage to module components.



2885 0201


Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. If necessary, loosen or temporarily remove chassis components (fans, etc.) as needed for access to the interior of the chassis.
4. Install metal standoffs on the floor of the chassis in alignment with the PATX5000 motherboard mounting holes. Use as many standoffs as practicable.


Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

5. Set the PATX5000 motherboard on the chassis standoffs, aligning the panel connectors with the I/O shield as you do so.
6. Start the screw(s) provided into the standoffs, without tightening them completely. (The chassis shown is a Motorola unit. With other chassis, the procedure may differ slightly.)
7. With all screws in place, tighten them snugly.

## CPU

To install a CPU in the primary (U2) or secondary (U3) Socket 370 processor socket on the PATX5000 board, refer to the illustration and follow the steps below.

No tools are necessary for this procedure.

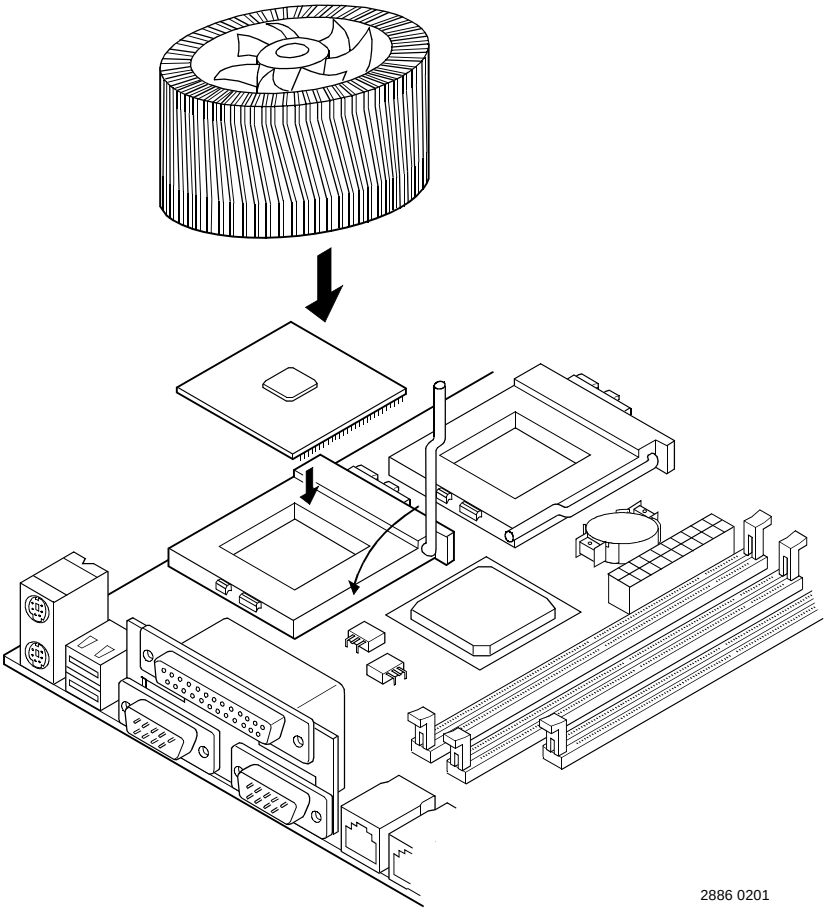
1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to a suitable ground as described under *Installation Preliminaries* on page 1-3. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Loosen the CPU cooler retention clip and separate the CPU cooler from the processor socket as described in the procedures under *CPU*

*Cooler* on page 1-21. Take care not to damage the plastic ears on the socket.

**Caution**

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

3. Unclip the lever from the side of the processor socket and swing it 90° up to the *FREE* position. Remove the existing processor module, if present.
4. Align the new processor module with the socket and seat it on the connector, taking care not to bend any pins. Little pressure should be necessary.
5. Swing the lever 90° down to the *LOCK* position and resecure it between the plastic clips on the side of the processor socket.
6. Reinstall the CPU cooler on the socket as described in the procedures under *CPU Cooler* on page 1-21.




**Notes**

1. If two CPUs are installed, they should be identical.
2. If you are using only one CPU, a CPU terminator module must be installed in the remaining CPU socket. You can install the single CPU in either socket.

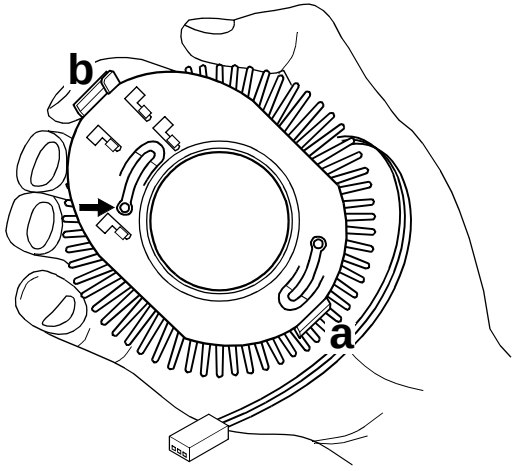
# CPU Cooler

CPU coolers are installed on the Intel PGA 370 sockets to keep your microprocessor(s) cool. A CPU cooler includes a heat sink as well as a fan and is more efficient than a heat sink alone. To install a CPU cooler on the primary (U2) or secondary (U3) processor slot on the PATX5000 board, refer to the illustrations and follow the steps below.

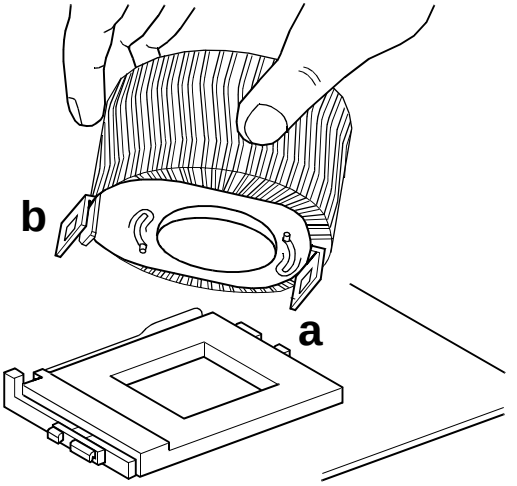
No tools are necessary for this procedure.

**Note** In dual-processor applications, it is advisable to install the CPU cooler on CPU A (U2) *first*, and to remove it *last*. This improves access to the spring clips.

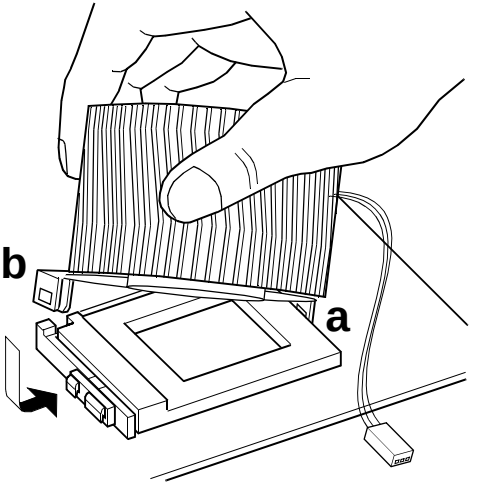
1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to a suitable ground as described under *Installation Preliminaries* on page 1-3. The ESD strap must be secured to your wrist and to ground throughout the procedure.



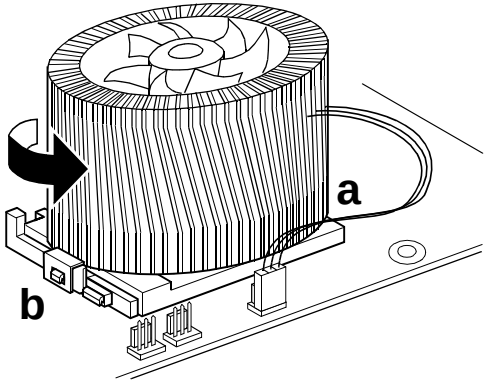

2. Hold the air cooler with the shorter end metal spring clip (point "a") toward your wrist.
3. Set the guide pin (arrow in above illustration) all the way to the left end of the slot as shown.




4. Clasp the spring clip over the tab (point **a**) at the narrow end of the socket (opposite CAM side of socket).




5. Clasp the spring clip over the tab (point **b**) at the CAM end of the socket. Help the clip onto the tab with your fingers if necessary.




6. Twist the air cooler counter-clockwise about 1/2 inch, making sure the spring clip features are securely seated over the socket tabs. Verify the heat sink is firmly locked in place.

7. Plug the 3-pin fan connector into the corresponding 3-pin header (J1 for CPU A or J3 for CPU B) on the motherboard.

**Caution**

As you route the fan wires to the connector headers, ensure that the wires will stay out of the cooler fins.

**Note** With standard air coolers installed, the cooler on CPU A extends over the edge of the board slightly. This is a deviation from the ATX standard, and you may need to compensate for it in some installations.

To remove a CPU cooler, proceed as follows:

1. Unplug the 3-pin fan connector from the header (J1 for CPU A or J3 for CPU B) on the motherboard.
2. Twist the air cooler clockwise about 1/2 inch to unlock the spring clip at the CAM end of the socket. Help the clip off the tab with your fingers if necessary.
3. With a rocking motion, lift the air cooler off the CAM end of the socket and slide the spring clip off the tab at the opposite end of the socket.

## RIMM Memory

To install RIMMs (Rambus Inline Memory Modules) on the PATX5000 board, refer to the illustration and follow the steps below.

Note that RIMMS are installed in pairs. The RIMMs you install should all be identical. The RIMM sockets are paired as follows:

- ❏ XU1 and XU3
- ❏ XU2 and XU4

If you install only a single pair of RIMMs, you will need to place C-RIMMs (continuity RIMMs) in the remaining socket pair.

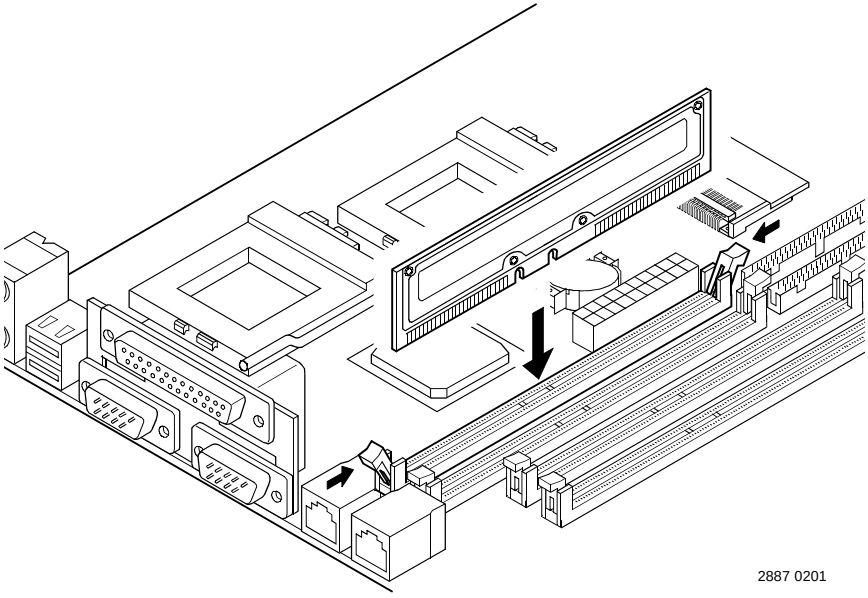
No tools are necessary for this procedure.

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to a suitable ground as described under *Installation Preliminaries* on page 1-3. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Align the memory module with the desired slot, XU4-XU1. Seat the module firmly in the slot.

**Caution**

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

3. Push the locking tabs on each end of the memory module inward until they snap into the ‘‘locked’’ position.




## AGP Graphics Card

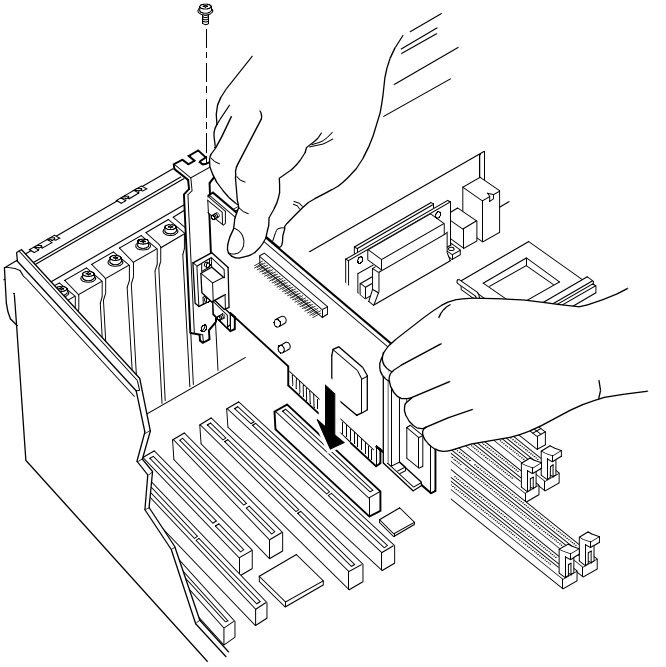
You can install an AGP (Accelerated Graphics Port) graphics card in J26, the AGP slot on PATX5000 motherboards. To install an AGP graphics card on the board, refer to the illustration and follow the steps below.

You need a Phillips screwdriver for this procedure.

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to a suitable ground as described under *Installation Preliminaries*

on page 1-3. The ESD strap must be secured to your wrist and to ground throughout the procedure.

2. Align the AGP card with the slot, J26. Seat the card firmly in the slot.



2888 0201

**Caution**

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

To avoid damaging pins in J26, be sure to keep the AGP card straight during installation or removal.

3. Fasten the connector end of the card to the chassis with the screw provided.

## PCI Expansion Cards

You can install one, two, three, or four PCI expansion cards on the PATX5000. You can install the cards in any order, but you may find it more convenient to start with the inner PCI slot and finish with the outer one. In other words, install PCI module(s) first in J28, then J31, then J33, then J38 (*SLOT 1*, *SLOT 2*, *SLOT 3*, *SLOT 4*).

Note that PCI **slots 1 and 2** are 64-bit 66MHz slots attached to the PCI-64 Hub (Intel 82806AA) as illustrated in Figure 3-1 on page 3-2. These are +3.3V signaling slots, which accommodate either +3.3V or universal PCI cards. Slots 1 and 2 accept:

- ❏ Either 64- or 32-bit cards
- ❏ Either 66MHz or 33MHz cards

Installing a 33MHz card in either slot will drop the bus speed from 66MHz to 33MHz, which is detrimental to performance if the remaining card is 66MHz-capable. It is best, therefore, to put 66MHz-capable cards in slots 1 and 2, while keeping 33MHz-only cards in slots 3 and 4 if possible.

PCI slots **3 and 4** are 32-bit 33MHz slots attached to the I/O Controller Hub (Intel 82801AA) as illustrated in Figure 3-1 on page 3-2. These are +5V signaling slots, which accommodate either +5V or universal PCI cards. Slots 3 and 4 accept:

- ❏ Either 64- or 32-bit cards (while limiting 64-bit cards to 32-bit transfers)
- ❏ Either 66MHz or 33MHz cards (with 66MHz cards dropping to 33MHz in these slots)

Keeping the above considerations in mind may aid in determining how to distribute a payload of PCI cards for best performance.

To install a PCI expansion card on the board, refer to the illustration and follow the steps below.

You need a Phillips screwdriver for this procedure.

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to a suitable ground as described under *Installation Preliminaries*

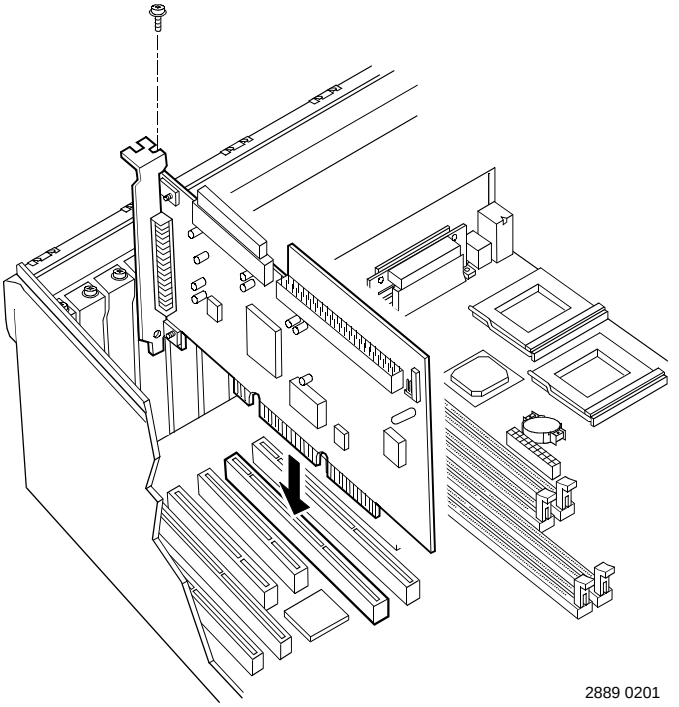
on page 1-3. The ESD strap must be secured to your wrist and to ground throughout the procedure.

2. Align the PCI expansion card with the desired slot, J28-J38. Seat the card firmly in the slot.

**Caution**

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

3. Fasten the connector end of the card to the chassis with the screw provided.



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**Notes**

1. Boards that occupy PCI slot 4 and the adjacent ISA slot (J39) share I/O space in the back panel. If the ISA slot is occupied, PCI slot 4 must remain vacant, and vice-versa.
2. The two PCI slots closest to the processors are the primary PCI slots and provide higher performance. If an expansion card fails to operate in any of the primary PCI slots, however, install the card in a secondary PCI slot.

## ISA Modules

You can install either one or two ISA modules on the PATX5000. You can install the cards in either order, but you may find it more convenient to start with the inner ISA slot and finish with the outer one. In other words, install the first ISA module in slot J39, the second in slot J43. To install an ISA module on the board, refer to the illustration and follow the steps below.

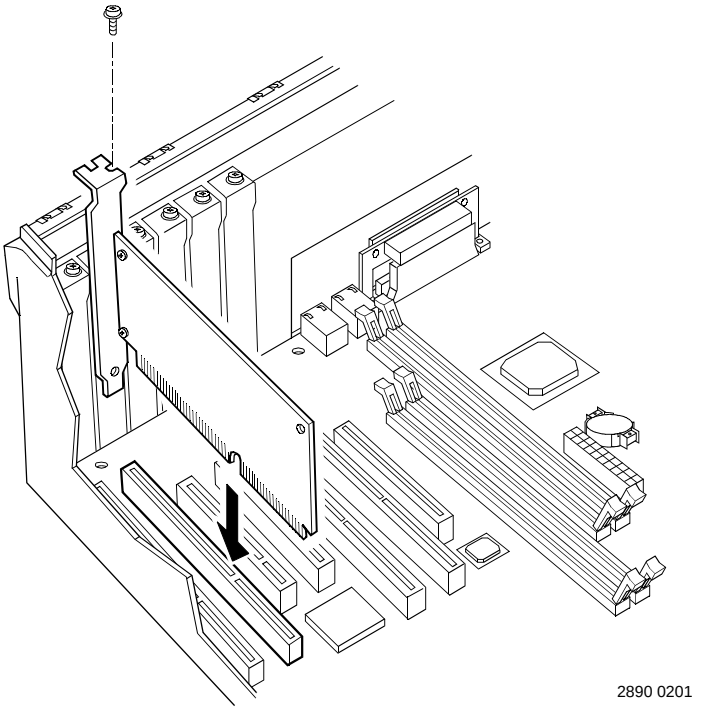
You need a Phillips screwdriver for this procedure.

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to a suitable ground as described under *Installation Preliminaries* on page 1-3. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Align the ISA module with the desired slot, J39 or J43. Seat the card firmly in the slot.

**Caution**

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

3. Fasten the connector end of the card to the chassis with the screw provided.




**Note** Boards that occupy ISA slot J39 and the adjacent PCI slot 4 share I/O space in the back panel. If the ISA slot is occupied, PCI slot 4 must remain vacant, and vice-versa.

## IDE CompactFlash

The CompactFlash™ cards which can be used on the PATX5000 contain an intelligent controller for management of the Flash media. The CompactFlash implementation mimics the file structure of a hard disk drive. With a CompactFlash card installed, you can store and manipulate files on the card as you would on a hard disk or floppy disk. For details on installing this component, you may wish to refer to specific vendor information, such as the *SanDisk IDE FlashDrive Installation Guide* available at **http://www.sandisk.com**.

For the general installation procedure applicable to the PATX5000, refer to the illustration and follow the steps below.

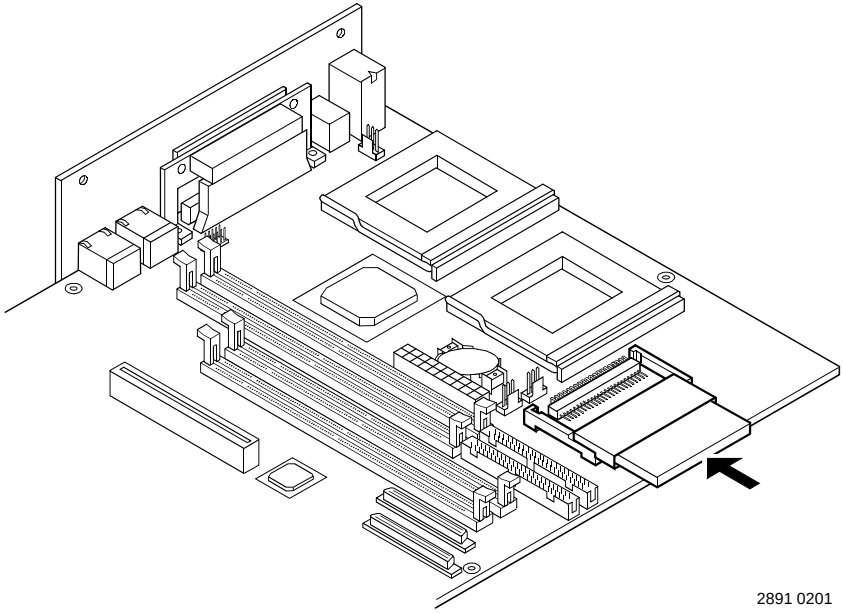
No tools are necessary for this procedure.

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to a suitable ground as described under *Installation Preliminaries* on page 1-3. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Start the CompactFlash card into the card guides on the CompactFlash connector, J11.

**Caution**

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

3. Press the card gently and securely into the connector until it seats.



**Notes**

1. Be sure that the CompactFlash master/slave setting (jumper header J8) is compatible with the secondary IDE devices installed.
2. If the CompactFlash card is the only device installed on the secondary bus, set it to master mode. If an additional IDE device is present on the bus, the CompactFlash card can be in either master or slave mode, with the other IDE device being set the opposite way. (If an ATAPI device is present on the bus, however, the CompactFlash card must be in master mode and the ATAPI device in slave mode.)
3. When you power up the system, ensure that the secondary on-chip PCI IDE is set to "enabled" in the BIOS IDE Configuration submenus.

## Connection to Peripherals

With the I/O shield in place, the PATX5000 motherboard installed in a chassis, and modules installed on the PATX5000, you are ready to connect peripherals and apply power to the board. Figure 1-1 shows the locations of the various cable connectors. They are also listed in Table 1-3 with the rest of the connectors. For the pin assignments of the connectors listed, refer to Chapter 4, *Connector Pin Assignments*.

### Table 1-3. PATX5000 Board Connectors

| Connector | Function |
|---|---|
| I/O Panel Connectors | |
| J6 (bottom) | KB (keyboard) panel connector |
| J6 (top) | MSE (mouse) panel connector |
| J7 (bottom) | USB0 (Universal Serial Bus 0) panel connector |
| J7 (top) | USB1 (Universal Serial Bus 1) panel connector |
| J12 (left) | COM1 panel connector (serial port) |
| J12 (right) | COM2 panel connector (serial port) |

## Table 1-3. PATX5000 Board Connectors (continued)

| Connector | Function |
|---|---|
| J12 (top) | PARALLEL printer panel connector |
| J14 | ETHERNET A panel connector |
| J17 | ETHERNET B panel connector |
| Board Surface Connectors | |
| J1 | CPU A Fan cable header |
| J2 | Chassis Fan cable header |
| J3 | CPU B Fan cable header |
| J10 | COM2 auxiliary board connector |
| J11 | CompactFlash board connector |
| J13 | POWER IN board connector |
| J15 | SECONDARY (IDE) board connector |
| J16 | PRIMARY (IDE) board connector |
| J20 | USB1 (Universal Serial Bus 1) auxiliary board connector |
| J21 | SCSI (Channel A) board connector |
| J24 | SCSI (Channel B) board connector |
| J26 | AGP board connector |
| J28 | PCI Slot 1 board connector |
| J29 | Ethernet LED cable header (channel A) |
| J31 | PCI Slot 2 board connector |
| J32 | Chassis intrusion detection cable header |
| J33 | PCI Slot 3 board connector |
| J35 | FLOPPY board connector |
| J36 | Ethernet LED cable header (channel B) |
| J38 | PCI Slot 4 board connector |
| J39 | ISA Slot 1 board connector |

**Table 1-3. PATX5000 Board Connectors (continued)**

| Connector | Function |
|---|---|
| J42 | Infrared interface cable header |
| J43 | ISA Slot 2 board connector |
| J44 | "Advantage" I/O header |
| U2 | Primary CPU (Slot A) connector |
| U3 | Secondary CPU (Slot B) connector |
| XU1-XU4 | RIMM module sockets |

## Completing the Installation

Verify that hardware is installed and the power/peripheral cables connected as appropriate for your system configuration.

Replace the chassis or system cover, reconnect the system to the AC or DC power source, and turn the equipment power on.

# BIOS Self-Test and Startup 2

## Introduction

The Phoenix BIOS (Basic I/O System) on the PATX5000 motherboard is a customized version of an industry-standard BIOS for IBM PC AT–compatible personal computers. It supports Intel x86 and compatible processors, including those of the Pentium® family. The BIOS provides important low-level support for the board's central processing, memory, and I/O subsystems.

## Initial Conditions

After you have verified that all necessary hardware preparation has been done, that all connections have been made correctly, and that the installation is complete, you can power up the system.

### BIOS Startup

The BIOS is activated as soon as you turn the computer on. The BIOS reads system configuration information from CMOS RAM and begins the process of checking out the system and configuring it through the power-on self-test (POST).

When these preliminaries are finished, the BIOS seeks an operating system on one of the data storage devices (hard drive, floppy drive, etc.). The BIOS then launches the operating system and surrenders control of system operations to it.

### Configuration Information

The system configuration information which the BIOS reads from CMOS RAM during power-up has been stored there by means of the Setup utility. The Setup utility uses a number of menus for making changes and for turning special features on or off. Should you wish to change any of the

configuration information, you can start the Setup utility during POST by pressing <F2> at any time while the following message is displayed at the bottom of the screen:

```
PRESS <F2> TO ENTER SETUP
```

If the message disappears before you respond and you still wish to enter Setup, you can restart the system for another attempt by any of the following means:

- ❏ Cycling power
- ❏ Pressing the RESET button on the system case
- ❏ Simultaneously pressing the <Ctrl>, <Alt>, and <Delete> keys

# The Setup Interface

The Setup utility uses a menu-driven interface. As shown in the following illustration, each Setup screen has a menu bar, a legend bar, and a field-specific help window. For each field with predefined values, an options window is available as well.

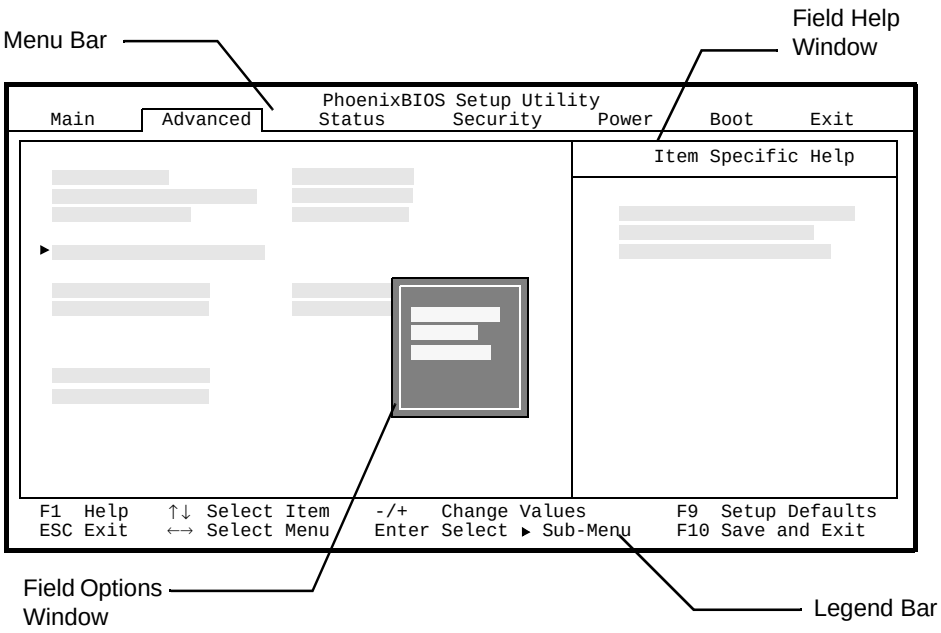



**Figure 2-1. The Basic Setup Screen**

# Elements of the Setup Screen

The various components of the Setup Screen are described below.

## Menu Bar

The menu bar at the top of the window enables you to select from the principal Setup functions. Use the left/right arrow keys to select among the principal functions; use the up/down arrow keys and the <Return> key to accept and enter the associated sub-menus.

The Setup menus are summarized below. For further details on using the Setup utility, consult the *PATX5000 BIOS and Programmer's Reference Guide* (PATX5BOSA/RM), listed in Appendix D, *Related Documentation*.

**Table 2-1. Startup Overview**

| Menu | Function |
|---|---|
| Main | Set time and other basic elements of system configuration. |
| Advanced | Set up drives or view and configure system memory, I/O, and advanced chipset features. |
| Status | Configure options for hardware monitoring or view fan, temperature, and power status. |
| Security | Change, set, or disable passwords and configure access parameters. |
| Power | Configure options for power management. |
| Boot | Specify boot options. |
| Exit | Exit the Setup utility with or without saving changes. |

## Legend Bar

The legend bar lists keys and commands that are helpful in navigating the Setup utility and configuring its functions. Refer to *Setup Navigation* below for details.

## Field Help Window

For most fields and submenus, item-specific help is displayed in a field help window on the right side of each screen. The help window contains a brief description of the field or sub-menu, and/or directions for using it.

## Field Options Window

Pressing the <Return> key after you select a given field or submenu displays the options available for that field.

## Navigation in Setup

The arrow keys, <Return>, and <Esc> enable you to access most functions of the Setup utility. Use the left/right arrow keys to select among the principal functions; use the up/down arrow keys and the <Return> key to accept and enter the associated sub-menus. To exit, press <Esc>. The following table lists all keys available for navigation in the Setup utility.

**Table 2-2. Keys for Navigation in Setup**

| Key | Function |
|---|---|
| <F1> or <Alt-H> | Open General Help Window. |
| <Esc> | Exit a menu or window. |
| → ← arrow keys | Select a different menu. |
| ↑ ↓ arrow keys | Move cursor up and down. |
| <Tab> or <Shift-Tab> | Move cursor within a field. |
| <Home> or <End> | Move cusor to top or bottom of window. |
| <PgUp> or <PgDn> | Move cursor to next or previous page (in Help). |
| Move cursor to next or previous page (in Help). | Select the previous value for a field. |
| <F6> or <+> or <Space> | Select the next value for a field. |
| <F9> | Load the default configuration values for all menus. |
| <F10> | Save all changes and exit. |
| <Enter> | Execute command, select submenu (>), or display options window. |

# In Case of Difficulty

As indicated in the ‘‘Navigation’’ table, pressing <F1> or <Alt-H> brings up a Help window with information pertaining to specific menus.

If the system can no longer boot after you have modified the system configuration via Setup, an automatic override feature restores the BIOS default settings after a certain number of failed boot attempts.

In addition, the hardware override described under *Clearing CMOS* in Chapter 1 enables you to restore the BIOS default settings without resorting to repeated boot attempts. Once the defaults are restored, you can restart the Setup utility and make necessary adjustments.

For further details on the Setup menus and the BIOS in general, refer to the *PATX5000 BIOS and Programmer's Reference Guide*, listed in Appendix D, *Related Documentation*.

# BIOS Messages and Beep Codes

Listed in this section are error/status messages that the BIOS may display. Some of them display information about a hardware component (for example, the amount of memory installed). Others indicate some problem with a device, such as the way it has been configured. Most of them occur during the power-on self-test (POST). When the BIOS detects a correctable error, it either sounds a beep code or displays a message.

The messages listed below are those pertaining to the BIOS kernel. Specific chipset ports and BIOS extensions may generate additional messages.

If your system displays one of the messages marked below with an asterisk (*), take note of the message and contact your dealer. Should the system fail after you have made changes in the Setup menus, reset the computer, reenter Setup, and correct the error or restore the Setup default values.

**Beep**

A single long beep followed by two short beeps indicates that the video configuration has failed (due to a missing or defective video card), or that an external ROM module did not properly checksum to zero.

In addition, a number of POST routines that shut down the system upon failure display error messages and issue beep codes before shutdown to identify the test point that produced the error. For details on those beep codes, refer to the *PATX5000 BIOS and Programmer's Reference Guide*, listed in Appendix D, *Related Documentation.*

**0200 Failure Fixed Disk**

Fixed disk improperly configured or not working. Verify that the fixed disk is properly attached. Run Setup. Verify that the fixed-disk type is correctly identified.

**0210 Stuck key**

Key stuck on keyboard.

**0211 Keyboard error**

Keyboard malfunctioning.

∗**0212 Keyboard Controller Failed**

Keyboard controller did not pass power-on self-test. The keyboard controller may need to be replaced.

**0213 Keyboard locked — Unlock key switch**

Unlock the system to proceed.

**0220 Monitor type does not match CMOS — Run SETUP**

The monitor type is incorrectly identified in Setup.

∗**0230 Shadow RAM Failed at offset: *nnnn***

Failure detected during the shadow RAM test at offset *nnnn* of the 64K block under test.

∗**0231 System RAM Failed at offset: *nnnn***

Failure detected during the system RAM test at offset *nnnn* of the 64K block under test.

∗**0232 Extended RAM Failed at offset: *nnnn***

Extended RAM improperly configured or not functioning at offset *nnnn* of the 64K block under test.

**0250 System battery is dead — Replace and run SETUP**

CMOS clock battery indicator shows battery is dead. Replace the battery and run Setup to reconfigure the system.

**0251 System CMOS checksum bad — Default configuration used**

System CMOS corrupted or incorrectly modified, possibly by an application program that changed data stored in CMOS. Because the CMOS checksum was invalid, the BIOS has installed a fresh configuration.

If CMOS-to-EEPROM backups are enabled (refer to *CMOS Restore from Backup (J34)* on page 1-12) *and* the EEPROM contains a valid backup image, the new configuration comes from EEPROM. Otherwise, the BIOS loads default setup values from Flash memory.

If the default values are not appropriate, run the Setup utility and enter your own values. Should the error persist, check the system battery or contact your dealer.

**∗0260 System Timer Error**

Timer test failed. The motherboard is in need of repair.

**∗0270 Real time clock error**

Real-time clock failed BIOS test. You may need to set a valid date (1991-2099), or the motherboard may need repair.

**0271 Check date and time settings**

You may need to set a valid date (1991-2099).

**0280 Previous boot incomplete — default configuration used**

The previous POST did not complete. The BIOS has loaded default values and will offer to run Setup with those values. If the boot failure was caused by incorrect values and they are not corrected, the next boot attempt will likely fail as well.

Improper Setup values on systems that give you control of wait states may also terminate the POST with this error. Run the Setup utility and verify that the wait-state configuration is correct. The error should then clear upon the next boot attempt.

**0281 Memory size found by POST differed from CMOS**

The POST has detected a disparity between the memory size stored in CMOS and the actual memory size.

**02B0 Diskette drive A error**
**02B1 Diskette drive B error**

Drive A: or B: is present but fails the BIOS POST diskette tests. Verify that the drive is defined with the proper diskette type in Setup and that the diskette drive is attached correctly.

**02B2 Incorrect Drive A type — run SETUP**

Floppy drive A: type not correctly identified in Setup. Rerun the Setup utility.

**02B3 Incorrect Drive B type — run SETUP**

Floppy drive B: type not correctly identified in Setup. Rerun the Setup utility.

**02D0 System cache error — cache disabled**

RAM cache failed and the BIOS disabled the cache. On older boards, check the cache jumpers. You may have to replace the cache, as a disabled cache slows the system considerably. Contact your dealer if necessary.

**02F0 CPU ID:**

Processor error. **CPU ID** is the CPU logical ID.

∗**02F4: EISA CMOS not writable**

ServerBIOS2 test error: Writing to EISA CMOS not possible.

∗**02F5: DMA Test Failed**

ServerBIOS2 test error: Writing to extended DMA registers not possible.

∗**02F6: Software NMI Failed**

ServerBIOS2 test error: Generation of software NMI (non-maskable interrupt) not possible.

∗**02F7: Fail-Safe Timer NMI Failed**

ServerBIOS2 test error: Fail-Safe Timer takes too long.

***device* Address Conflict**

Address conflict for specified device.

**Allocation error for: *device***

Resource conflict for specified device. Run the ISA or EISA Configuration utility to resolve the conflict.

**CD ROM Drive**

CD ROM drive identified.

**Entering SETUP...**

The Setup utility is starting.

∗**Failing bits: *nnnn***

The hexadecimal number *nnnn* is a map of the bits at a RAM address which failed the memory test. Each 1 (one) in the map indicates a failed bit. See errors 230, 231, or 232 above for the offset address of the failure in System, Extended, or Shadow memory.

**Fixed disk *n***

Fixed disk *n* (0-3) identified.

**Invalid System Configuration Data**

Problem with NVRAM (CMOS) data.

**I/O device IRQ conflict**

Problem with processing I/O devices' interrupt requests.

**PS/2 Mouse Boot Summary Screen**

PS/2 mouse installed.

***nnnn* kB Extended RAM Passed**

The amount of RAM in kilobytes represented by *nnnn* has been successfully tested.

***nnnn* kB Cache SRAM Passed**

The amount of system cache in kilobytes represented by *nnnn* has been successfully tested.

***nnnn* kB Shadow RAM Passed**

The amount of shadow RAM in kilobytes represented by *nnnn* has been successfully tested.

***nnnn* kB System RAM Passed**

The amount of system RAM in kilobytes represented by *nnnn* has been successfully tested.

**One or more I2O Block Storage Devices were excluded from the Setup Boot Menu**

There was not enough room in the IPL table to display all installed $I^2O$ block-storage devices.

**Operating system not found**

The operating system cannot be located on either drive A: or drive C:. Enter Setup and verify that the fixed disk and drive A: are properly identified.

∗**Parity Check 1 *nnnn***

A parity error was detected on the system bus, indicating that some data has been corrupted. The BIOS attempts to locate the address and display it on the screen. If the BIOS cannot locate the address, it displays ???? .

∗**Parity Check 2 *nnnn***

A parity error was detected on the I/O bus, indicating that some data has been corrupted. The BIOS attempts to locate the address and display it on the screen. If the BIOS cannot locate the address, it displays ???? .

**Press <F1> to resume, <F2> to Setup, <F3> for previous**

Displayed after any recoverable error message. Press <F1> to start the boot process or <F2> to enter Setup and change the settings. Press <F3> to display the previous screen (usually an initialization error of an Option ROM, i.e., an add-on card). Write down and follow the information on the screen.

**Press <F2> to enter Setup**

Optional message displayed during POST. Can be turned off in Setup.

**PS/2 Mouse:**

PS/2 mouse identified.

**Run the I2O Configuration Utility**

One or more unclaimed block storage devices has the Configuration Request bit set in the LCT. Run an $I^2O$ configuration utility (e.g., the SAC utility).

**System BIOS shadowed**

System BIOS copied to shadow RAM.

**UMB upper limit segment address: *nnnn***

Displays the address *nnnn* of the upper limit of Upper Memory Blocks, indicating released segments of the BIOS which can be reclaimed by a virtual memory manager.

**Video BIOS shadowed**

Video BIOS copied to shadow RAM.

# Functional Description 3

## Introduction

This chapter describes the PATX5000 series motherboard on a block diagram level. Figure 3-1 presents the overall board architecture. The *General Description* provides an overview of the PATX5000 board, followed by a detailed description of several sections of circuitry.

Detailed descriptions of other PATX5000 functions, including programmable registers, can be found in the *Programmer's Reference Guide* (listed in the *Related Documentation* section). Refer to that document for a functional description of the PATX5000 series motherboard in greater depth.

## Block Diagram

Figure 3-1 shows the overall architecture of the PATX5000 series motherboard.

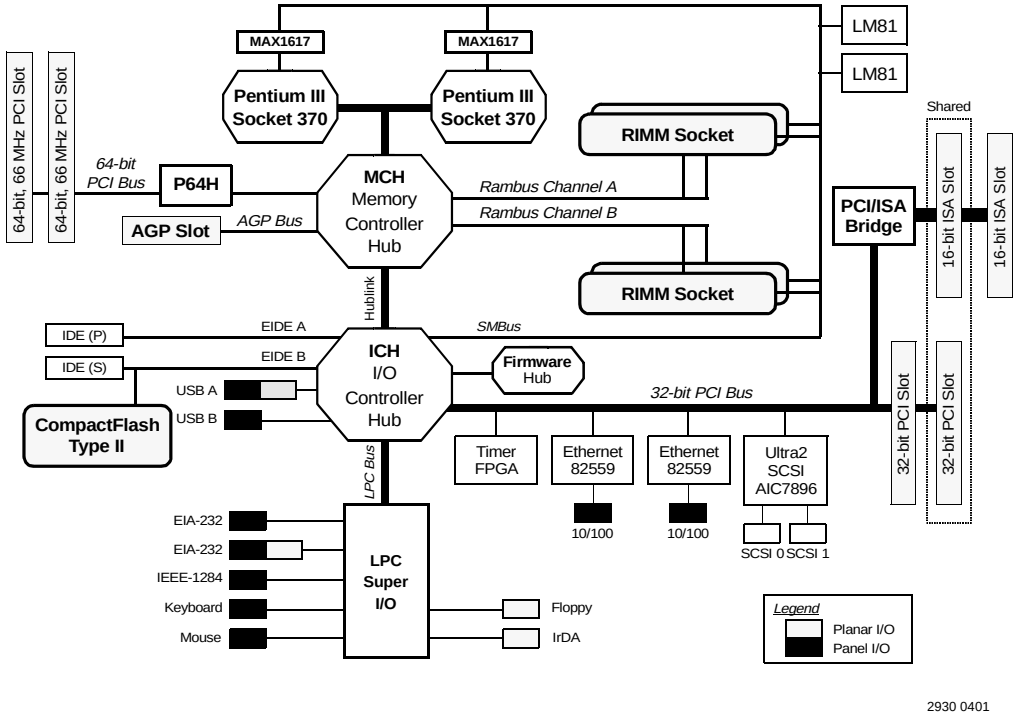



**Figure 3-1. PATX5000 Block Diagram**

# Features



The following table summarizes the characteristics of PATX5000 series boards.

**Table 3-1. PATX5000 Series Motherboard: Features**

| Feature | Description |
|---|---|
| Microprocessor | Dual PGA370 sockets. Board supports single or dual 370-pin FC-PGA, 500MHz-1GHz Pentium® III processors (100MHz or 133MHz Front Side Bus clock frequencies). |
| Cache Memory | L1: 16/16KB instruction/data cache (Pentium III-resident)<br>L2: 256KB on-die cache |
| DRAM | Four 184-pin RIMM sockets on board<br>Up to 2GB ECC Rambus memory supporting real and protected (36-bit) addressing |
| Intel 840 Chip Set | Intel 82802 Firmware Hub (FWH)<br>8Mb (1MB) BIOS Flash<br>Random number generator<br>Intel 82840 Memory Controller Hub (MCH)<br>AGP 4X/2X support<br>Hub interface to I/O Controller Hub<br>Hub interface to PCI-64 Hub<br>Intel 82801AA I/O Controller Hub (ICH)<br>32-bit 33MHz PCI Bus support<br>IDE Ultra ATA/66 on primary IDE<br>IDE Ultra ATA/33 on secondary IDE<br>Integrated APIC- and 82C59-type interrupts<br>Interfaces to Firmware Hub and LPC Super I/O device<br>Intel 82806AA PCI-64 Hub (P64H)<br>64-bit 66MHz PCI Bus support<br>533MB/s bandwidth to Memory Controller Hub |

## Table 3-1. PATX5000 Series Motherboard: Features (continued)

| Feature | Description |
|---|---|
| Peripheral Support | SMC LPC47B277 ISA Super I/O device with:<br>– Two asynchronous serial ports<br>– One IEEE-1284 parallel port<br>– One PS/2 floppy port<br>– One PS/2 keyboard port and one PS/2 mouse port<br>– One IrDA (infrared) port |
| | EIDE: Dual-channel IDE Ultra ATA/66, Ultra ATA/33 hard drive interface via I/O Controller Hub |
| | Ethernet: Dual 10BaseT/100BaseTx Ethernet interface (Intel 82559), routed through RJ45 panel connectors |
| | USB: Dual independent USB ports via I/O Controller Hub, with 1.5Mb/s and 12Mb/s transfer rates. |
| | 64-bit PCI: 3.3V 64-bit PCI interface at up to 66MHz (via Memory Controller Hub and PCI-64 Hub), with two 32-/64-bit compatible PCI expansion slots |
| | 32-bit PCI: 5V 32-bit PCI interface at up to 33MHz (via I/O Controller Hub), with one PCI/ISA shared slot and one PCI-only slot |
| | ISA: 5V ISA interface (National PC87200 PCI-to-ISA bridge), operating at ¼ of PCI frequency with one PCI/ISA shared slot and one ISA-only slot |
| | Graphics: AGP slot at up to 133MHz, or PCI graphics |
| | SCSI: Dual-channel Ultra 2 SCSI (Adaptec AIC-7896), via I/O Controller Hub and PCI-32 bus |
| RTC and CMOS RAM | MC146818B compatibility via I/O Controller Hub<br>256 bytes of battery-backed RAM (242 bytes available for BIOS)<br>EEPROM backup for CMOS RAM via SMbus |
| Environmental Monitoring | Hardware monitors (two National LM81 devices) allowing software to track system voltages and fan operation<br>Temperature monitors (two MAX1617 devices) allowing software to track CPU temperatures |
| Flash memory | ATA Flash socket for IDE-compatible CompactFlash memory cards |

**Table 3-1. PATX5000 Series Motherboard: Features (continued)**

| Feature | Description |
|---|---|
| Form Factor | Standard ATX (9.6 inches by 12 inches) |
| Interrupt Management | Intel 82801AA I/O Controller Hub (ICH)<br>ISA-compatible legacy interrupt controller (dual 8259 functionality) Advanced Programmable Interrupt Controller (I/O APIC)<br>Intel 82806AA PCI-64 Hub (P64H)<br>Advanced Programmable Interrupt Controller (I/O APIC) |
| Timers | Xilinx Advantage FPGA<br>Two-level programmable watchdog timer<br>Timestamp timer<br>Three programmable 32-bit interval timers (counters 1 and 2 cascadable to form 64-bit timer)<br>Watchdog timer on SMC LPC47B277 ISA Super I/O device<br>Three interval timers (82C54 functionality) on Intel 82801AA I/O Controller Hub |
| BIOS | Support for 8Mb (1MB) BIOS Flash in Intel 82802 Firmware Hub |

# General Description

The PATX5000 is an ATX form factor motherboard. It supports Linux®, Microsoft Windows NT® and various other Intel x86-based real-time operating systems in an embedded environment.

The PATX5000 supports single or dual Intel Pentium® III Socket 370 processors in a flip-chip pin grid array (FC-PGA) package. The board's architecture incorporates an Intel 840 chip set, which fully supports both symmetrical multiprocessing (SMP) and dual channels of RAMbus memory. The 840 chip set is capable of 133MHz front-side-bus performance. It supports up to 2GB of RAMbus memory, 64-bit/66MHz as well as 32-bit/33MHz PCI buses, and 4X AGP graphics.

As implemented on the PATX5000, the 840 chip set includes a Memory Controller Hub (MCH), a PCI-64 Hub (P64H), an I/O Controller Hub (ICH), and a Firmware Hub (FWH).

The MCH contains the following:

- ❏ Front-Side Bus interface
- ❏ System RDRAM controller
- ❏ AGP controller
- ❏ Hub Link interfaces for connection to the P64H and the ICH

The ICH contains the following:

- ❏ Dual-channel EIDE interface
- ❏ Two USB ports
- ❏ LPC (Low Pin Count) interface
- ❏ SMbus controller
- ❏ 32-bit 33MHz PCI interface (PCI-32 bus)

The P64H contains a 64-bit 66MHz PCI interface (PCI-64 bus) that supports two expansion slots.

The FWH supplies 8Mb (1MB) of Flash memory for BIOS storage. The BIOS occupies the upper 512KB of the Flash PROM. The lower 512KB are available to user applications.

The SMC LPC47B277 Super I/O device resides on the LPC interface. It supplies the following functions:

- ❏ IEEE-1284 parallel port
- ❏ Two asynchronous serial ports
- ❏ IrDA (Infrared) port
- ❏ Floppy disk interface
- ❏ Keyboard and mouse ports

The PATX5000 board includes four RIMM sockets for RDRAM memory in addition to four PCI slots for PCI expansion and two ISA slots for legacy ISA expansion. There are two independent Ultra2 SCSI channels as well as two independent 10/100 Mb Ethernet interfaces.

The I/O panel contains:

- ❏ Dual stacked keyboard and mouse connectors
- ❏ Dual stacked USB connectors
- ❏ Two nine-pin serial port connectors
- ❏ 25-pin parallel port connector
- ❏ Two RJ45 Ethernet connectors

Planar connectors on the board surface include:

- ❏ Two 68-pin SCSI connectors
- ❏ Two 40-pin EIDE connectors
- ❏ 34-pin floppy disk connector
- ❏ Serial port header
- ❏ USB header
- ❏ CompactFlash socket
- ❏ Various expansion slots

# Environmental Monitoring

The two National LM81 hardware monitor devices on the PATX5000 motherboard operate in tandem with the dual MAX1617 CPU temperature sensors and the ICH interrupt controller circuitry to provide a number of useful system management features. These features are summarized below; for details on their implementation, refer to the device data sheets and to the *PATX5000 BIOS and Programmer's Reference Guide*, listed in Appendix D, *Related Documentation*.

## LM81 Hardware Monitors

The LM81 devices monitor system voltages and fan speeds. Their readings can be sampled by system management software at any time. The devices have programmable limit registers which can be configured to generate system interrupts as appropriate for your application. Interrupt signals

from the LM81s are routed across the SMbus to the GPIO(11) input to the interrupt controller circuitry on the Intel 82801AA I/O Controller Hub.

For further information and details of programming, refer to the *PATX5000 BIOS and Programmer's Reference Guide*, listed in Appendix D, *Related Documentation*.

## Chassis Intrusion

The PATX5000 includes circuitry for the detection of chassis intrusion events. When implemented with appropriate sensory devices in an enclosure, the intrusion detection circuitry is active continually (even while the system is shut down, as long as backup battery or standby power is present). Interrupts generated through chassis intrusion are fed to the primary LM81 chip as well as to the INTRUDER_L input to the interrupt controller circuitry on the Intel 82801AA I/O Controller Hub.

For further information and details of programming, refer to the *PATX5000 BIOS and Programmer's Reference Guide*, listed in Appendix D, *Related Documentation*.

## CPU Temperature Monitor

PATX5000 boards include a pair of Maxim MAX1617 devices to directly monitor the temperature of each Pentium® III processor. An overtemperature condition produces an alarm signal. The MAX1617s allow system management software to read processor temperatures, set temperature sample rates, specify alarm threshold values, and clear the alarm output after processing the interrupt. Alarm signals from a MAX1617 are routed to the THRM_L input to the interrupt controller circuitry on the Intel 82801AA I/O Controller Hub (refer to the device data sheets and to the *PATX5000 BIOS and Programmer's Reference Guide* for programming details).

# Connector Pin Assignments

# 4

## PATX5000 Cable Connectors

This section summarizes the pin assignments for I/O and power cable interconnect signals on the PATX5000 motherboard. The next section lists the pin assignments for device sockets on the board. For the placement of the principal connectors on the PATX5000, see Figure 1-1.

### Table 4-1. CPU A Fan Cable Header (J1)

| | |
|---|---|
| 1 | GND |
| 2 | +12.0V |
| 3 | FANTACH1 |

### Table 4-2. Chassis Fan Cable Header (J2)

| | |
|---|---|
| 1 | GND |
| 2 | +12.0V |
| 3 | FANTACH2 |

### Table 4-3. CPU B Fan Cable Header (J3)

| | |
|---|---|
| 1 | GND |
| 2 | +12.0V |
| 3 | FANTACH3 |

## Table 4-4. Keyboard/Mouse Panel Connector (J6)

| | | |
|---|---|---|
| 1 | KBDAT_FB# | Keyboard Interface (Bottom) |
| 2 | | |
| 3 | KYMSE_GND | |
| 4 | KB5V_FB | |
| 5 | KBCLK_FB# | |
| 6 | | |
| 7 | MSDAT_FB# | Mouse Interface (Top) |
| 8 | | |
| 9 | KYMSE_GND | |
| 10 | KB5V_FB | |
| 11 | MSCLK_FB# | |
| 12 | | |

## Table 4-5. USB Panel Connector (J7)

| | | |
|---|---|---|
| 1 | Vcc | USB Port 1 (Upper) |
| 2 | Port 1 Data (–) | |
| 3 | Port 1 Data (+) | |
| 4 | GND | |
| 1 | Vcc | USB Port 0 (Lower) |
| 2 | Port 0 Data (–) | |
| 3 | Port 0 Data (+) | |
| 4 | GND | |

### Table 4-6. COM2 Auxiliary Board Connector (J10)

| | | | |
|---|---|---|---|
| 1 | SP_DCD1 | SP_DSR1 | 2 |
| 3 | SP_RXD1 | SP_RTS1 | 4 |
| 5 | SP_TXD1 | SP_CTS1 | 6 |
| 7 | SP_DTR1 | SP_RI1 | 8 |
| 9 | GND | Key | 10 |

### Table 4-7. Parallel Port Panel Connector (J12-A)

| | | | |
|---|---|---|---|
| 1 | PP_STB# | PP_AFD# | 14 |
| 2 | PP_PD0 | PP_ERR# | 15 |
| 3 | PP_PD1 | PP_INIT# | 16 |
| 4 | PP_PD2 | PP_SLIN# | 17 |
| 5 | PP_PD3 | GND | 18 |
| 6 | PP_PD4 | GND | 19 |
| 7 | PP_PD5 | GND | 20 |
| 8 | PP_PD6 | GND | 21 |
| 9 | PP_PD7 | GND | 22 |
| 10 | PP_ACK# | GND | 23 |
| 11 | PP_BUSY | GND | 24 |
| 12 | PP_PE | GND | 25 |
| 13 | PP_SLCT | | |

## Table 4-8. Dual Serial Port Panel Connector (J12-B/C)

| | | |
|---|---|---|
| B1 | SP_DCD0 | COM1 Serial Port (Left) |
| B2 | SP_RXD0 | |
| B3 | SP_TXD0 | |
| B4 | SP_DTR0 | |
| B5 | GND | |
| B6 | SP_DSR0 | |
| B7 | SP_RTS0 | |
| B8 | SP_CTS0# | |
| B9 | SP_RI0 | |
| C1 | SP_DCD1 | COM2 Serial Port (Right) |
| C2 | SP_RXD1 | |
| C3 | SP_TXD1 | |
| C4 | SP_DTR1 | |
| C5 | GND | |
| C6 | SP_DSR1 | |
| C7 | SP_RTS1 | |
| C8 | SP_CTS1# | |
| C9 | SP_RI1 | |

## Table 4-9. POWER IN Board Connector (J13)

| | | | |
|---|---|---|---|
| 1 | +3.3V | +3.3V | 11 |
| 2 | +3.3V | –12V | 12 |
| 3 | GND | GND | 13 |
| 4 | +5V | PS_ON# | 14 |
| 5 | GND | GND | 15 |
| 6 | +5V | GND | 16 |

### Table 4-9. POWER IN Board Connector (J13) (continued)

| | | | |
|---|---|---|---|
| 7 | GND | GND | 17 |
| 8 | POWER_OK | –5V | 18 |
| 9 | +5VSTB | +5V | 19 |
| 10 | +12V | +5V | 20 |



### Table 4-10. Ethernet Panel Connectors (J14/J17)

| | |
|---|---|
| 1 | TX+ |
| 2 | TX– |
| 3 | RX+ |
| 4 | AC Terminated |
| 5 | AC Terminated |
| 6 | RX– |
| 7 | AC Terminated |
| 8 | AC Terminated |

### Table 4-11. IDE Board Connectors (J15/J16)

| | | | |
|---|---|---|---|
| 1 | RESET# | GND | 2 |
| 3 | DD7 | DD8 | 4 |
| 5 | DD6 | DD9 | 6 |
| 7 | DD5 | DD10 | 8 |
| 9 | DD4 | DD11 | 10 |
| 11 | DD3 | DD12 | 12 |
| 13 | DD2 | DD13 | 14 |
| 15 | DD1 | DD14 | 16 |
| 17 | DD0 | DD15 | 18 |
| 19 | GND | KEY | 20 |

### Table 4-11. IDE Board Connectors (J15/J16) (continued)

| | | | |
|---|---|---|---|
| 21 | DMARQ | GND | 22 |
| 23 | DIOW# | GND | 24 |
| 25 | DIOR# | GND | 26 |
| 27 | IORDY | CSEL | 28 |
| 29 | DMACK# | GND | 30 |
| 31 | INTRQ | No Connection | 32 |
| 33 | DA1 | PDIAG# | 34 |
| 35 | DA0 | DA2 | 36 |
| 37 | CS0# | CS1# | 38 |
| 39 | DASP# | GND | 40 |

### Table 4-12. USB1 Board Header (J20)

| | |
|---|---|
| 1 | Vcc |
| 2 | Port 1 Data (–) |
| 3 | Port 1 Data (+) |
| 4 | GND |

**Note** You cannot use this header and the USB1 connector on the I/O panel simultaneously. Select one or the other via USB Port 1 Routing jumper J23.

### Table 4-13. SCSI Channel A/B Connectors (J21/J24)

| | | | |
|---|---|---|---|
| 1 | Data_12 (+) | Data_12 (–) | 35 |
| 2 | Data_13 (+) | Data_13 (–) | 36 |
| 3 | Data_14 (+) | Data_14 (–) | 37 |
| 4 | Data_15 (+) | Data_15 (–) | 38 |
| 5 | DP_1 (+) | DP_1 (–) | 39 |

## Table 4-13. SCSI Channel A/B Connectors (J21/J24)

| | | | |
|---|---|---|---|
| 6 | Data_0 (+) | Data_0 (–) | 40 |
| 7 | Data_1 (+) | Data_1 (–) | 41 |
| 8 | Data_2 (+) | Data_2 (–) | 42 |
| 9 | Data_3 (+) | Data_3 (–) | 43 |
| 10 | Data_4 (+) | Data_4 (–) | 44 |
| 11 | Data_5 (+) | Data_5 (–) | 45 |
| 12 | Data_6 (+) | Data_6 (–) | 46 |
| 13 | Data_7 (+) | Data_7 (–) | 47 |
| 14 | DP_0 (+) | DP_0 (–) | 48 |
| 15 | GND | GND | 49 |
| 16 | DIFFSENSE | GND | 50 |
| 17 | TERMPWR | TERMPWR | 51 |
| 18 | TERMPWR | TERMPWR | 52 |
| 19 | No Connection | No Connection | 53 |
| 20 | GND | GND | 54 |
| 21 | ATN (+) | ATN (–) | 55 |
| 22 | GND | GND | 56 |
| 23 | BSY (+) | BSY (–) | 57 |
| 24 | ACK (+) | ACK (–) | 58 |
| 25 | RST (+) | RST (–) | 59 |
| 26 | MSG (+) | MSG (–) | 60 |
| 27 | SEL (+) | SEL (–) | 61 |
| 28 | CD (+) | CD (–) | 62 |
| 29 | REQ (+) | REQ (–) | 63 |
| 30 | IO (+) | IO (–) | 64 |

## Table 4-13. SCSI Channel A/B Connectors (J21/J24)

| | | | |
|---|---|---|---|
| 31 | Data_8 (+) | Data_8 (–) | 65 |
| 32 | Data_9 (+) | Data_9 (–) | 66 |
| 33 | Data_10 (+) | Data_10 (–) | 67 |
| 34 | Data_11 (+) | Data_11 (–) | 68 |

## Table 4-14. Floppy Disk Drive Header (J35)

| | | | |
|---|---|---|---|
| 1 | GND | DRVDEN0# | 2 |
| 3 | GND | Reserved | 4 |
| 5 | | DRVDEN1# | 6 |
| 7 | GND | INDEX# | 8 |
| 9 | GND | MTR0# | 10 |
| 11 | GND | DS1# | 12 |
| 13 | GND | DS0# | 14 |
| 15 | GND | MTR1# | 16 |
| 17 | GND | DIR# | 18 |
| 19 | GND | STEP# | 20 |
| 21 | GND | WDATA# | 22 |
| 23 | GND | WGATE# | 24 |
| 25 | GND | TRK0# | 26 |
| 27 | GND | WRTPRT# | 28 |
| 29 | GND | RDATA# | 30 |
| 31 | GND | HDSEL# | 32 |
| 33 | GND | DSKCHG# | 34 |

### Table 4-15. Infrared Interface Cable Header (J42)

| | | | |
|---|---|---|---|
| 1 | +3.3V | IR LED Resistor | 2 |
| 3 | No Connection | GND | 4 |
| 5 | IRRXD | Pulldown Resistor | 6 |
| 7 | GND | Filter Capacitor | 8 |
| 9 | IRTXD | GND | 10 |

### Table 4-16. Advantage I/O Header (J44)

| | | | |
|---|---|---|---|
| 1 | CTROUT_1 | CTRGATE_1 | 2 |
| 3 | GND | CTRCLK_1 | 4 |
| 5 | CTROUT_2 | CTRGATE_2 | 6 |
| 7 | GND | CTRCLK_2 | 8 |
| 9 | CTROUT_3 | CTRGATE_3 | 10 |
| 11 | GND | CTRCLK_3 | 12 |
| 13 | ADV_CFG_3 | ADV_CFG_4 | 14 |
| 15 | GND | ADV_CFG_5 | 16 |
| 17 | ADV_GPI_0 | ADV_GPI_1 | 18 |
| 19 | ADV_GPI_2 | ADV_GPI_3 | 20 |
| 21 | ADV_GPI_4 | ADV_GPI_5 | 22 |
| 23 | ADV_GPI_6 | ADV_GPI_7 | 24 |
| 25 | GND | +3.3V | 26 |
| 27 | ADV_GPO_0 | ADV_GPO_1 | 28 |
| 29 | ADV_GPO_2 | ADV_GPO_3 | 30 |
| 31 | ADV_GPO_4 | ADV_GPO_5 | 32 |
| 33 | ADV_GPO_6 | ADV_GPO_7 | 34 |

# PATX5000 Socket Connectors

This section lists the pin assignments for device sockets on the board. For the placement of the principal connectors on the PATX5000, see Figure 1-1.



### Table 4-17. CompactFlash Board Connector (J11)

| | | | |
|---|---|---|---|
| 1 | GND | CD1# | 26 |
| 2 | CF_D3 | CF_D11 | 27 |
| 3 | CF_D4 | CF_D12 | 28 |
| 4 | CF_D5 | CF_D13 | 29 |
| 5 | CF_D6 | CF_D14 | 30 |
| 6 | CF_D7 | CF_D15 | 31 |
| 7 | CF_CS1# | CF_CS3# | 32 |
| 8 | GND | CF_VS1# | 33 |
| 9 | GND | CF_IOR# | 34 |
| 10 | GND | CF_IOW# | 35 |
| 11 | GND | +3.3V | 36 |
| 12 | GND | CF_IRQ15 | 37 |
| 13 | +3.3V | +3.3V | 38 |
| 14 | GND | CF_CSEL# | 39 |
| 15 | GND | CF_VS2# | 40 |
| 16 | GND | IDERST# | 41 |
| 17 | GND | CF_IORDY | 42 |
| 18 | CF_DA2 | CF_INPACK# | 43 |
| 19 | CF_DA1 | +3.3V | 44 |
| 20 | CF_DA0 | CF_DASP# | 45 |
| 21 | CF_D0 | CF_PDIAG# | 46 |

## Table 4-17. CompactFlash Board Connector (J11)

| | | | |
|---|---|---|---|
| 22 | CF_D1 | CF_D8 | 47 |
| 23 | CF_D2 | CF_D9 | 48 |
| 24 | CF_IOCS16# | CF_D10 | 49 |
| 25 | CD2# | GND | 50 |



## Table 4-18. AGP Connector (J26)

| | Row A | | | | Row B | | |
|---|---|---|---|---|---|---|---|
| 1 | +12V | TYPEDET# | 2 | 1 | AGPOC# | +5V | 2 |
| 3 | Reserved | USB– | 4 | 3 | +5V | USB_AGP+ | 4 |
| 5 | GND | PIRQA# | 6 | 5 | GND | PIRQB# | 6 |
| 7 | PCIRST2# | GGNT# | 8 | 7 | CLK66 | GREQ# | 8 |
| 9 | +3.3V | GST1 | 10 | 9 | +3.3V | GST0 | 10 |
| 11 | Reserved | GPIPE# | 12 | 11 | GST2 | GRBF# | 12 |
| 13 | GND | Reserved | 14 | 13 | GND | Reserved | 14 |
| 15 | GSBA1 | +3.3V | 16 | 15 | GSBA0 | +3.3V | 16 |
| 17 | GSBA3 | Reserved | 18 | 17 | GSBA2 | GSB_STB | 18 |
| 19 | GND | GSBA5 | 20 | 19 | GND | GSBA4 | 20 |
| 21 | GSBA7 | Reserved | 22 | 21 | GSBA6 | Reserved | 22 |
| 23 | Reserved | Reserved | 24 | 23 | GND | +3.3VSB | 24 |
| 25 | Reserved | GAD30 | 26 | 25 | +3.3V | GAD31 | 26 |
| 27 | GAD28 | +3.3V | 28 | 27 | GAD29 | +3.3V | 28 |
| 29 | GAD26 | GAD24 | 30 | 29 | GAD27 | GAD25 | 30 |
| 31 | GND | Reserved | 32 | 31 | GND | GAD_STB1 | 32 |
| 33 | GCBE3# | +3.3V | 34 | 33 | GAD23 | +3.3V | 34 |
| 35 | GAD22 | GAD20 | 36 | 35 | GAD21 | GAD19 | 36 |
| 37 | GND | GAD18 | 38 | 37 | GND | GAD17 | 38 |

## Table 4-18. AGP Connector (J26) (continued)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 39 | GAD16 | +3.3V | 40 | 39 | GCBE2# | +3.3V | 40 |
| 41 | GFRAME# | Reserved | 42 | 41 | GIRDY# | Reserved | 42 |
| 43 | GND | Reserved | 44 | 43 | GND | Reserved | 44 |
| 45 | +3.3V | GTRDY# | 46 | 45 | +3.3V | GDEVSEL# | 46 |
| 47 | GSTOP# | AGP_PME# | 48 | 47 | +3.3V | GPERR# | 48 |
| 49 | GND | GPAR | 50 | 49 | GND | GSERR# | 50 |
| 51 | GAD15 | +3.3V | 52 | 51 | GCBE1# | +3.3V | 52 |
| 53 | GAD13 | GAD11 | 54 | 53 | GAD14 | GAD12 | 54 |
| 55 | GND | GAD09 | 56 | 55 | GND | GAD10 | 56 |
| 57 | GCBE0# | +3.3V | 58 | 57 | GAD08 | +3.3V | 58 |
| 59 | Reserved | GAD06 | 60 | 59 | GAD_STB0 | GAD07 | 60 |
| 61 | GND | GAD04 | 62 | 61 | GND | GAD05 | 62 |
| 63 | GAD02 | +3.3V | 64 | 63 | GAD03 | +3.3V | 64 |
| 65 | GAD00 | Reserved | 66 | 65 | GAD01 | Reserved | 66 |

## Table 4-19. PCI Slots 1 and 2 (J28/J31)

| | Row A | | | | Row B | | |
|---|---|---|---|---|---|---|---|
| 1 | TRST# | +12V | 2 | 1 | –12V | TCK | 2 |
| 3 | TMS | TDI | 4 | 3 | GND | Reserved | 4 |
| 5 | +5V | PIRQA# | 6 | 5 | +5V | +5V | 6 |
| 7 | PIRQC# | +5V | 8 | 7 | PIRQB# | PIRQD# | 8 |
| 9 | Reserved | +3.3V | 10 | 9 | Reserved | Reserved | 10 |
| 11 | Reserved | | 12 | 11 | Reserved | | 12 |
| 13 | | +3.3VSB | 14 | 13 | | Reserved | 14 |
| 15 | RST# | +3.3V | 16 | 15 | GND | PCLK1 | 16 |
| 17 | GNT0# | GND | 18 | 17 | GND | REQ0# | 18 |

## Table 4-19. PCI Slots 1 and 2 (J28/J31) (continued)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 19 | PME# | AD30 | 20 | 19 | +3.3V | AD31 | 20 |
| 21 | +3.3V | AD28 | 22 | 21 | AD29 | GND | 22 |
| 23 | AD26 | GND | 24 | 23 | AD27 | AD25 | 24 |
| 25 | AD24 | Reserved | 26 | 25 | +3.3V | CBE3# | 26 |
| 27 | +3.3V | AD22 | 28 | 27 | AD23 | GND | 28 |
| 29 | AD20 | GND | 30 | 29 | AD21 | AD19 | 30 |
| 31 | AD18 | AD16 | 32 | 31 | +3.3V | AD17 | 32 |
| 33 | +3.3V | FRAME# | 34 | 33 | CBE2# | GND | 34 |
| 35 | GND | TRDY# | 36 | 35 | IRDY# | +3.3V | 36 |
| 37 | GND | STOP# | 38 | 37 | DEVSEL# | GND | 38 |
| 39 | +3.3V | SDONE | 40 | 39 | PLOCK# | PERR# | 40 |
| 41 | SBO# | GND | 42 | 41 | +3.3V | SERR# | 42 |
| 43 | PAR | AD15 | 44 | 43 | +3.3V | CBE1# | 44 |
| 45 | +3.3V | AD13 | 46 | 45 | AD14 | GND | 46 |
| 47 | AD11 | GND | 48 | 47 | AD12 | AD10 | 48 |
| 49 | AD9 | GND | 50 | 49 | M66EN | GND | 50 |
| 51 | GND | CBE0# | 52 | 51 | GND | AD8 | 52 |
| 53 | +3.3V | AD6 | 54 | 53 | AD7 | +3.3V | 54 |
| 55 | AD4 | GND | 56 | 55 | AD5 | AD3 | 56 |
| 57 | AD2 | AD0 | 58 | 57 | GND | AD1 | 58 |
| 59 | +3.3V | REQ64# | 60 | 59 | +3.3V | ACK64# | 60 |
| 61 | +5V | +5V | 62 | 61 | +5V | +5V | 62 |
| 63 | GND | CBE7# | 64 | 63 | Reserved | GND | 64 |
| 65 | CBE5# | +3.3V | 66 | 65 | CBE6# | CBE4# | 66 |
| 67 | PAR64 | AD62 | 68 | 67 | GND | AD63 | 68 |
| 69 | GND | AD60 | 70 | 69 | AD61 | +3.3V | 70 |

## Table 4-19. PCI Slots 1 and 2 (J28/J31) (continued)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 71 | AD58 | GND | 72 | 71 | AD59 | AD57 | 72 |
| 73 | AD56 | AD54 | 74 | 73 | GND | AD55 | 74 |
| 75 | +3.3V | AD52 | 76 | 75 | AD53 | GND | 76 |
| 77 | AD50 | GND | 78 | 77 | AD51 | AD49 | 78 |
| 79 | AD48 | AD46 | 80 | 79 | +3.3V | AD47 | 80 |
| 81 | GND | AD44 | 82 | 81 | AD45 | GND | 82 |
| 83 | AD42 | +3.3V | 84 | 83 | AD43 | AD41 | 84 |
| 85 | AD40 | AD38 | 86 | 85 | GND | AD39 | 86 |
| 87 | GND | AD36 | 88 | 87 | AD37 | +3.3V | 88 |
| 89 | AD34 | GND | 90 | 89 | AD35 | AD33 | 90 |
| 91 | AD32 | Reserved | 92 | 91 | GND | Reserved | 92 |
| 93 | GND | Reserved | 94 | 93 | Reserved | GND | 94 |

## Table 4-20. PCI Slots 3 and 4 (J33/J38)

| | Row A | | | | Row B | | |
|---|---|---|---|---|---|---|---|
| 1 | TRST# | +12V | 2 | 1 | –12V | TCK | 2 |
| 3 | TMS | TDI | 4 | 3 | GND | Reserved | 4 |
| 5 | +5V | PIRQC# | 6 | 5 | +5V | +5V | 6 |
| 7 | PIRQA# | +5V | 8 | 7 | PIRQD# | PIRQB# | 8 |
| 9 | Reserved | +5V | 10 | 9 | Reserved | Reserved | 10 |
| 11 | Reserved | GND | 12 | 11 | Reserved | GND | 12 |
| 13 | GND | +3.3VSB | 14 | 13 | GND | Reserved | 14 |
| 15 | RST1# | +5V | 16 | 15 | Reserved | PCLK3 | 16 |
| 17 | GNT0# | GND | 18 | 17 | GND | REQ0# | 18 |
| 19 | PME# | AD30 | 20 | 19 | +5V | AD31 | 20 |
| 21 | +3.3V | AD28 | 22 | 21 | AD29 | GND | 22 |

## Table 4-20. PCI Slots 3 and 4 (J33/J38) (continued)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 23 | AD26 | GND | 24 | 23 | AD27 | AD25 | 24 |
| 25 | AD24 | IDSEL | 26 | 25 | +3.3V | CBE3# | 26 |
| 27 | +3.3V | AD22 | 28 | 27 | AD23 | GND | 28 |
| 29 | AD20 | GND | 30 | 29 | AD21 | AD19 | 30 |
| 31 | AD18 | AD16 | 32 | 31 | +3.3V | AD17 | 32 |
| 33 | +3.3V | FRAME# | 34 | 33 | CBE2# | GND | 34 |
| 35 | GND | TRDY# | 36 | 35 | IRDY# | +3.3V | 36 |
| 37 | GND | STOP# | 38 | 37 | DEVSEL# | GND | 38 |
| 39 | +3.3V | SDONE | 40 | 39 | PLOCK# | PERR# | 40 |
| 41 | SBO# | GND | 42 | 41 | +3.3V | SERR# | 42 |
| 43 | PAR | AD15 | 44 | 43 | +3.3V | CBE1# | 44 |
| 45 | +3.3V | AD13 | 46 | 45 | AD14 | GND | 46 |
| 47 | AD11 | GND | 48 | 47 | AD12 | AD10 | 48 |
| 49 | AD9 | | 50 | 49 | GND | | 50 |
| 51 | | CBE0# | 52 | 51 | | AD8 | 52 |
| 53 | +3.3V | AD6 | 54 | 53 | AD7 | +3.3V | 54 |
| 55 | AD4 | GND | 56 | 55 | AD5 | AD3 | 56 |
| 57 | AD2 | AD0 | 58 | 57 | GND | AD1 | 58 |
| 59 | +5V | REQ64# | 60 | 59 | +5V | ACK64# | 60 |
| 61 | +5V | +5V | 62 | 61 | +5V | +5V | 62 |

## Table 4-21. ISA Slots 1 and 2 (J39/J43)

| | Row A | Row B | Row C | Row D | |
|---|---|---|---|---|---|
| 1 | IOCHK# | GND | SBHE# | MEMCS16# | 1 |
| 2 | SD7 | RSTISA | LA23 | IOCS16# | 2 |
| 3 | SD6 | +5V | LA22 | IRQ10 | 3 |

## Table 4-21. ISA Slots 1 and 2 (J39/J43) (continued)

| | | | | | |
|---|---|---|---|---|---|
| 4 | SD5 | IRQ9 | LA21 | IRQ11 | 4 |
| 5 | SD4 | –5V | LA20 | IRQ12 | 5 |
| 6 | SD3 | DRQ2 | LA19 | IRQ15 | 6 |
| 7 | SD2 | –12V | LA18 | IRQ14 | 7 |
| 8 | SD1 | ZWS# | LA17 | DACK0# | 8 |
| 9 | SD0 | +12V | MEMR# | DRQ0 | 9 |
| 10 | IOCHRDY | GND | MEMW# | DACK5# | 10 |
| 11 | AEN | SMEMW# | SD8 | DRQ5 | 11 |
| 12 | SA19 | SMEMR# | SD9 | DACK6# | 12 |
| 13 | SA18 | IOW# | SD10 | DRQ6 | 13 |
| 14 | SA17 | IOR# | SD11 | DACK7# | 14 |
| 15 | SA16 | DACK3# | SD12 | DRQ7 | 15 |
| 16 | SA15 | DRQ3 | SD13 | +5V | 16 |
| 17 | SA14 | DACK1# | SD14 | MASTER# | 17 |
| 18 | SA13 | DRQ1 | SD15 | GND | 18 |
| 19 | SA12 | REFRESH# | | | |
| 20 | SA11 | SYSCLK | | | |
| 21 | SA10 | IRQ7 | | | |
| 22 | SA9 | IRQ6 | | | |
| 23 | SA8 | IRQ5 | | | |
| 24 | SA7 | IRQ4 | | | |
| 25 | SA6 | IRQ3 | | | |
| 26 | SA5 | DACK2# | | | |
| 27 | SA4 | TC | | | |

## Table 4-21. ISA Slots 1 and 2 (J39/J43) (continued)

| | | |
|---|---|---|
| 28 | SA3 | BALE |
| 29 | SA2 | GND |
| 30 | SA1 | OSC |
| 31 | SA0 | GND |



## Table 4-22. PGA370 Socket Connectors (U2, U3)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| A3 | D29# | A5 | D28# | A7 | D43# | A9 | D37# |
| A11 | D44# | A13 | D51# | A15 | D47# | A17 | D48# |
| A19 | D57# | A21 | D46# | A23 | D53# | A25 | D60# |
| A27 | D61# | A29 | DEP7# | A31 | DEP3# | A33 | DEP2# |
| A35 | PRDY# | A37 | GND | AA1 | A27# | AA3 | A30# |
| AA5 | $Vcc_{CORE}$ | AA33 | $V_{TT}$ | AA35 | $V_{TT}$ | AA37 | $Vcc_{CORE}$ |
| AB2 | $Vcc_{CORE}$ | AB4 | A24# | AB6 | A23# | AB32 | GND |
| AB34 | $Vcc_{CORE}$ | AB36 | $Vcc_{CMOS}$ | AC1 | A33# | AC3 | A20# |
| AC5 | GND | AC33 | GND | AC35 | FERR# | AC37 | RSP# |
| AD2 | GND | AD4 | A31# | AD6 | $V_{REF}$ | AD32 | $Vcc_{CORE}$ |
| AD34 | GND | AD36 | $Vcc_{1.5}$ | AE1 | A17# | AE3 | A22# |
| AE5 | $Vcc_{CORE}$ | AE33 | A20M# | AE35 | IERR# | AE37 | FLUSH# |
| AF2 | $Vcc_{CORE}$ | AF4 | A35# | AF6 | A25# | AF32 | GND |
| AF34 | $Vcc_{CORE}$ | AF36 | GND | AG1 | EDGCTRL | AG3 | A19# |
| AG5 | GND | AG33 | INIT# | AG35 | STPCLK# | AG37 | IGNNE# |
| AH2 | GND | AH4 | RESET# | AH6 | A10# | AH8 | A5# |
| AH10 | A8# | AH12 | A4# | AH14 | BNR# | AH16 | REQ1# |
| AH18 | REQ2# | AH20 | $V_{TT}$ | AH22 | RS1# | AH24 | $Vcc_{CORE}$ |
| AH26 | RS0# | AH28 | THERMTRIP# | AH30 | SLP# | AH32 | $Vcc_{CORE}$ |
| AH34 | GND | AH36 | $Vcc_{CORE}$ | AJ1 | A21# | AJ3 | GND |

## Table 4-22. PGA370 Socket Connectors (U2, U3) (continued)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| AJ5 | $Vcc_{CORE}$ | AJ7 | GND | AJ9 | $Vcc_{CORE}$ | AJ11 | GND |
| AJ13 | $Vcc_{CORE}$ | AJ15 | GND | AJ17 | $Vcc_{CORE}$ | AJ19 | GND |
| AJ21 | $Vcc_{CORE}$ | AJ23 | GND | AJ25 | $Vcc_{CORE}$ | AJ27 | GND |
| AJ29 | $Vcc_{CORE}$ | AJ31 | BSEL1 | AJ33 | BSEL0 | AJ35 | SMI# |
| AJ37 | VID3 | AK2 | $Vcc_{CORE}$ | AK4 | GND | AK6 | A28# |
| AK8 | A3# | AK10 | A11# | AK12 | $V_{REF}$ | AK14 | A14# |
| AK16 | $V_{TT}$ | AK18 | REQ0# | AK20 | LOCK# | AK22 | $V_{REF}$ |
| AK24 | AERR# | AK26 | PWRGOOD | AK28 | RS2# | AK30 | Reserved |
| AK32 | TMS | AK34 | $Vcc_{CORE}$ | AK36 | GND | AL1 | GND |
| AL3 | GND | AL5 | A15# | AL7 | A13# | AL9 | A9# |
| AL11 | AP0# | AL13 | $V_{TT}$ | AL15 | A7# | AL17 | REQ4# |
| AL19 | REQ3# | AL21 | $V_{TT}$ | AL23 | HITM# | AL25 | HIT# |
| AL27 | DBSY# | AL29 | THERMDN | AL31 | THERMDP | AL33 | TCK |
| AL35 | VID0 | AL37 | VID2 | AM2 | Reserved | AM4 | $Vcc_{CORE}$ |
| AM6 | GND | AM8 | $Vcc_{CORE}$ | AM10 | GND | AM12 | $Vcc_{CORE}$ |
| AM14 | GND | AM16 | $Vcc_{CORE}$ | AM18 | GND | AM20 | $Vcc_{CORE}$ |
| AM22 | GND | AM24 | $Vcc_{CORE}$ | AM26 | GND | AM28 | $Vcc_{CORE}$ |
| AM30 | GND | AM32 | $Vcc_{CORE}$ | AM34 | GND | AM36 | VID1 |
| AN3 | GND | AN5 | A12# | AN7 | A16# | AN9 | A6# |
| AN11 | $V_{TT}$ | AN13 | AP1# | AN15 | $V_{TT}$ | AN17 | BPRI# |
| AN19 | DEFER# | AN21 | $V_{TT}$ | AN23 | RP# | AN25 | TRDY# |
| AN27 | DRDY# | AN29 | BR0# | AN31 | ADS# | AN33 | TRST# |
| AN35 | TDI | AN37 | TDO | B2 | D35# | B4 | GND |
| B6 | $Vcc_{CORE}$ | B8 | GND | B10 | $Vcc_{CORE}$ | B12 | GND |
| B14 | $Vcc_{CORE}$ | B16 | GND | B18 | $Vcc_{CORE}$ | B20 | GND |
| B22 | $Vcc_{CORE}$ | B24 | GND | B26 | $Vcc_{CORE}$ | B28 | GND |

## Table 4-22. PGA370 Socket Connectors (U2, U3) (continued)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| B30 | $Vcc_{CORE}$ | B32 | GND | B34 | $Vcc_{CORE}$ | B36 | BINIT# |
| C1 | D33# | C3 | $Vcc_{CORE}$ | C5 | D31# | C7 | D34# |
| C9 | D36# | C11 | D45# | C13 | D49# | C15 | D40# |
| C17 | D59# | C19 | D55# | C21 | D54# | C23 | D58# |
| C25 | D50# | C27 | D56# | C29 | DEP5# | C31 | DEP1# |
| C33 | DEP0# | C35 | BPM0# | C37 | CPUPRES# | D2 | GND |
| D4 | GND | D6 | $Vcc_{CORE}$ | D8 | D38# | D10 | D39 |
| D12 | D42 | D14 | D41# | D16 | D52# | D18 | GND |
| D18 | GND | D20 | $Vcc_{CORE}$ | D22 | GND | D24 | $Vcc_{CORE}$ |
| D26 | GND | D28 | $Vcc_{CORE}$ | D30 | GND | D32 | $Vcc_{CORE}$ |
| D34 | GND | D36 | $Vcc_{CORE}$ | E1 | D26# | E3 | D25# |
| E5 | $Vcc_{CORE}$ | E7 | GND | E9 | $Vcc_{CORE}$ | E11 | GND |
| E13 | $Vcc_{CORE}$ | E15 | GND | E17 | $Vcc_{CORE}$ | E19 | GND |
| E21 | RESERVE | E23 | $V_{TT}$ | E25 | D62# | E27 | SLEWCTRL |
| E29 | DEP6# | E31 | DEP4# | E33 | $V_{REF}$ | E35 | BPM1# |
| E37 | BP3# | F2 | $Vcc_{CORE}$ | F4 | $Vcc_{CORE}$ | F6 | D32# |
| F8 | D22# | F10 | Reserved | F12 | D27# | F14 | $Vcc_{CORE}$ |
| F16 | D63# | F18 | $V_{REF}$ | F20 | GND | F22 | $Vcc_{CORE}$ |
| F24 | GND | F26 | $Vcc_{CORE}$ | F28 | GND | F30 | $Vcc_{CORE}$ |
| F32 | GND | F34 | $Vcc_{CORE}$ | F36 | GND | G1 | D21# |
| G3 | D23# | G5 | GND | G33 | BP2# | G35 | $V_{TT}$ |
| G37 | Reserved | H2 | GND | H4 | D16# | H6 | D19# |
| H32 | $Vcc_{CORE}$ | H34 | GND | H36 | $Vcc_{CORE}$ | J1 | D7# |
| J3 | D30# | J5 | $Vcc_{CORE}$ | J33 | PICCLK | J35 | PICD0 |
| J37 | PREQ# | K2 | $Vcc_{CORE}$ | K4 | $V_{REF}$ | K6 | D24# |
| K32 | $Vcc_{CORE}$ | K34 | $Vcc_{CORE}$ | K36 | GND | L1 | D13# |

## Table 4-22. PGA370 Socket Connectors (U2, U3) (continued)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| L3 | D20# | L5 | GND | L33 | Reserved | L35 | PICD1 |
| L37 | LINT1/NMI | M2 | GND | M4 | D11# | M6 | D3# |
| M32 | $Vcc_{CORE}$ | M34 | GND | M36 | LINT0/INTR | N1 | D2# |
| N3 | D14# | N5 | $Vcc_{CORE}$ | N33 | Reserved | N35 | Reserved |
| N37 | Reserved | P2 | $Vcc_{CORE}$ | P4 | D18# | P6 | D9# |
| P32 | GND | P34 | $Vcc_{CORE}$ | P36 | GND | Q1 | D12# |
| Q3 | D10# | Q5 | GND | Q33 | Reserved | Q35 | Reserved |
| Q37 | Reserved | R2 | Reserved | R4 | D17# | R6 | $V_{REF}$ |
| R32 | $Vcc_{CORE}$ | R34 | GND | R36 | $Vcc_{CORE}$ | S1 | D8# |
| S3 | D5# | S5 | $Vcc_{CORE}$ | S33 | $V_{TT}$ | S35 | RTTCTRL |
| S37 | $V_{TT}$ | T2 | $Vcc_{CORE}$ | T4 | D1# | T6 | D6# |
| T32 | GND | T34 | $Vcc_{CORE}$ | T36 | GND | U1 | D4# |
| U3 | D15# | U5 | GND | U33 | PLL2 | U35 | $V_{TT}$ |
| U37 | $V_{TT}$ | V2 | GND | V4 | BERR# | V6 | $V_{REF}$ |
| V32 | $Vcc_{CORE}$ | V34 | GND | V36 | $Vcc_{CORE}$ | W1 | D0# |
| W3 | A34# | W5 | $Vcc_{CORE}$ | W33 | PLL1 | W35 | Reserved |
| W37 | BCLK | X2 | BR1# | X4 | RESET2# | X6 | A32# |
| X32 | GND | X34 | $Vcc_{CORE}$ | X36 | GND | Y1 | Reserved |
| Y3 | A26# | Y5 | GND | Y33 | CLKREF | Y35 | $Vcc_{CORE}$ |
| Y37 | GND | Z2 | GND | Z4 | A29# | Z6 | A18# |
| Z32 | $Vcc_{CORE}$ | Z34 | GND | Z36 | $Vcc_{2.5}$ | | |

## Table 4-23. RIMM Sockets (XU1-XU4)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| A1 | GND | B1 | GND | A47 | No Conn. | B47 | No Conn. |
| A2 | LDQA8 | B2 | LDQA7 | A48 | No Conn. | B48 | No Conn. |
| A3 | GND | B3 | GND | A49 | No Conn. | B49 | No Conn. |
| A4 | LDQA6 | B4 | LDQA5 | A50 | No Conn. | B50 | No Conn. |
| A5 | GND | B5 | GND | A51 | $V_{REF}$ | B51 | $V_{REF}$ |
| A6 | LDQA4 | B6 | LDQA3 | A52 | GND | B52 | GND |
| A7 | GND | B7 | GND | A53 | SCL | B53 | SA0 |
| A8 | LDQA2 | B8 | LDQA1 | A54 | $V_{DD}$ | B54 | $V_{DD}$ |
| A9 | GND | B9 | GND | A55 | SDA | B55 | SA1 |
| A10 | LDQA0 | B10 | LCFM | A56 | $SV_{DD}$ | B56 | $SV_{DD}$ |
| A11 | GND | B11 | GND | A57 | SWP | B57 | SA2 |
| A12 | LCTMN | B12 | LCFMN | A58 | $V_{DD}$ | B58 | $V_{DD}$ |
| A13 | GND | B13 | GND | A59 | RSCK | B59 | RCMD |
| A14 | LCTM | B14 | No Conn. | A60 | GND | B60 | GND |
| A15 | GND | B15 | GND | A61 | RDQB7 | B61 | RDQB8 |
| A16 | No Conn. | B16 | LROW2 | A62 | GND | B62 | GND |
| A17 | GND | B17 | GND | A63 | RDQB5 | B63 | RDQB6 |
| A18 | LROW1 | B18 | LROW0 | A64 | GND | B64 | GND |
| A19 | GND | B19 | GND | A65 | RDQB3 | B65 | RDQB4 |
| A20 | LCOL4 | B20 | LCOL3 | A66 | GND | B66 | GND |
| A21 | GND | B21 | GND | A67 | RDQB1 | B67 | RDQB2 |
| A22 | LCOL2 | B22 | LCOL1 | A68 | GND | B68 | GND |
| A23 | GND | B23 | GND | A69 | RCOL0 | B69 | RDQB0 |
| A24 | LCOL0 | B24 | LDQB0 | A70 | GND | B70 | GND |
| A25 | GND | B25 | GND | A71 | RCOL2 | B71 | RCOL1 |
| A26 | LDQB1 | B26 | LDQB2 | A72 | GND | B72 | GND |

## Table 4-23. RIMM Sockets (XU1-XU4) (continued)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| A27 | GND | B27 | GND | A73 | RCOL4 | B73 | RCOL3 |
| A28 | LDQB3 | B28 | LDQB4 | A74 | GND | B74 | GND |
| A29 | GND | B29 | GND | A75 | RROW1 | B75 | RROW0 |
| A30 | LDQB5 | B30 | LDQB6 | A76 | GND | B76 | GND |
| A31 | GND | B31 | GND | A77 | No Conn. | B77 | RROW2 |
| A32 | LDQB7 | B32 | LDQB8 | A78 | GND | B78 | GND |
| A33 | GND | B33 | GND | A79 | RCTM | B79 | No Conn. |
| A34 | LSCK | B34 | LCMD | A80 | GND | B80 | GND |
| A35 | $V_{CMOS}$ | B35 | $V_{CMOS}$ | A81 | RCTMN | B81 | RCFMN |
| A36 | SOUT | B36 | SIN | A82 | GND | B82 | GND |
| A37 | $V_{CMOS}$ | B37 | $V_{CMOS}$ | A83 | RDQA0 | B83 | RCFM |
| A38 | No Conn. | B38 | No Conn. | A84 | GND | B84 | GND |
| A39 | GND | B39 | GND | A85 | RDQA2 | B85 | RDQA1 |
| A40 | No Conn. | B40 | No Conn. | A86 | GND | B86 | GND |
| A41 | $V_{DD}$ | B41 | $V_{DD}$ | A87 | RDQA4 | B87 | RDQA3 |
| A42 | $V_{DD}$ | B42 | $V_{DD}$ | A88 | GND | B88 | GND |
| A43 | No Conn. | B43 | No Conn. | A89 | RDQA6 | B89 | RDQA5 |
| A44 | No Conn. | B44 | No Conn. | A90 | GND | B90 | GND |
| A45 | No Conn. | B45 | No Conn. | A91 | RDQA8 | B91 | RDQA7 |
| A46 | No Conn. | B46 | No Conn. | A92 | GND | B92 | GND |

# Specifications

# A

## Board Specifications

Table A-1 lists the general specifications for the PATX5000 family of ATX form factor motherboards. Subsequent sections detail cooling requirements and FCC compliance.

### Table A-1. PATX5000 Motherboard Specifications

| Characteristics | | Specifications |
|---|---|---|
| **Power Requirements (exclusive of attached daughter boards and/or peripherals)** | | |
| Dual 733MHz Pentium III, two 256MB/800MHz ECC RIMMs | | +5Vdc (±5%), 8.23A typical, 18.6A maximum<br>+3.3Vdc (±5%), 3.31A typical, 10.2A maximum<br>+12Vdc (±5%), 0.4A typical, 1A maximum<br>+5VSB (±5%), 0.16A typical, 0.34A maximum<br>–12Vdc (±5%), 0A typical, 0A maximum<br>–5Vdc (±5%), 0A typical, 0A maximum |
| **Environmental Parameters** | | |
| Temperature | Operating | 0-45° C (32-113° F) at entry point of forced air cooling |
| | Non-operating | –40-85° C (–40-185° F) |
| Altitude | Operating | –1000 to 10,000 feet (–305 to 3048 meters) |
| | Non-operating | –1000 to 30,000 feet (–305 to 9144 meters) |
| Relative humidity | Operating | 5% to 90% at 40° C (non-condensing) |
| | Non-operating | 5% to 95% at 40° C (non-condensing) |
| Vibration | Operating | 0.5G RMS (20-2000Hz random) |
| | Non-operating | 6G RMS (20-2000Hz random) |

**Table A-1. PATX5000 Motherboard Specifications (continued)**

| Characteristics | | Specifications |
|---|---|---|
| **Physical Dimensions** | | |
| Motherboard | Height | 3.2 inches (81 mm) with CPUs and expansion modules |
| | Length/Width | Standard ATX form factor:<br>9.6 inches wide by 12 inches long (244mm x 305mm) |
| **Motherboard I/O Panel Connectors** | | |
| Ethernet interface | | Single/dual RJ45 connectors. 10 Mbit/second for 10BaseT; 100 Mbit/second for 100BaseTx. |
| Serial port interface (asynchronous) | | DTE EIA-232-D on two DB9 connectors. COM1 and COM2 ports support 115.2K baud |
| Parallel port interface | | IEEE-1284 printer interface on a DB25 connector. |
| Mouse interface | | Circular 6-pin mini-DIN connector provides the mouse interface with existing PS/2 type peripheral devices. |
| Keyboard interface | | Circular 6-pin mini-DIN connector provides the keyboard interface with existing PS/2 type peripheral devices |
| USB | | 1.5 Mb/second, or 12 Mb/second using shielded cables |
| **Board Planar I/O Connectors** | | |
| SCSI interface | | Dual-channel Ultra 2 SCSI, with maximum transfer rates of 80 Mbit/second per channel. Two HD68 board connectors |
| EIDE interface | | Ultra ATA/66 EIDE interface, with two 40-pin board headers |
| CompactFlash | | CompactFlash type II socket available on secondary EIDE interface |

# Cooling Requirements

The PATX5000 motherboard is designed and tested to operate reliably with an incoming air temperature range of from 0° to 45° C (32° to

113° F) with forced air cooling of the entire assembly (motherboard and expansion modules).

The processors come with associated fans for cooling. A power supply fan and a chassis fan are required as well. The PATX5000 provides headers to power these fans if necessary (in Motorola-supplied chassis, they are connected directly to the power supply).

While the exact amount of airflow required for cooling depends on the ambient air temperature and the type, number, and location of boards and other heat sources, adequate cooling can usually be achieved with 10 CFM (490 LFM) flowing over the assembly.

# EMC Compliance

The Motorola PATX5000 family of ATX form factor motherboards was tested in a CE-marked EMC-compliant chassis and meets the requirements for Class B equipment. Compliance was achieved under the following conditions:

- ❏ Shielded cables on all external I/O ports.
- ❏ Cable shields connected to earth ground.
- ❏ Board standoffs connected to earth ground via conductive chassis panels.
- ❏ I/O shield installed on external I/O connector cluster.

For minimum RF emissions, it is essential that the conditions above be implemented. Failure to do so could compromise the CE compliance of the equipment containing the PATX5000.

# Thermal Validation

B

Board component temperatures are affected by ambient temperature, air flow, board electrical operation, and software operation. In order to evaluate the thermal performance of a circuit board assembly, it is necessary to test the board under actual operating conditions. These operating conditions vary depending on system design.

While Motorola Computer Group performs thermal analysis in a representative system to verify operation within specified ranges (see Appendix A, *Specifications*), you should evaluate the thermal performance of the board in your application.

This appendix provides systems integrators with information which can be used to conduct thermal evaluations of the board in their specific system configuration. It identifies thermally significant components and lists the corresponding maximum allowable component operating temperatures. It also provides example procedures for component-level temperature measurements.

## Thermally Significant Components

The following table summarizes components that exhibit significant temperature rises. These are the components that should be monitored in order to assess thermal performance. The table also supplies the component reference designator and the maximum allowable operating temperature.

You can find components on the board by their reference designators as shown in Figure B-1 and Figure B-2. Versions of the board that are not fully populated may not contain some of these components.

The preferred measurement location for a component may be *junction*, *case*, or *air* as specified in the table. Junction temperature refers to the temperature measured by an on-chip thermal device. Case temperature

refers to the temperature at the top, center surface of the component. Air temperature refers to the ambient temperature near the component.

## Table B-1. Thermally Significant Components

| Reference Designator | Generic Description | Max. Allowable Component Temperature (deg. C) | Measurement Location |
|---|---|---|---|
| U20, U27 | Intel 82559 Ethernet chip | 85 | Case |
| U49 | NSC 87200 PCI-to-ISA Bridge chip | 110 | Case |
| U25 | Xilinx XCS40XL Advantage FPGA | 85 | Junction |
| U28 | SMC LPC47B277 Super I/O device | 70 | Ambient |
| U14 | Intel 82801AA I/O Controller Hub (ICH) | 100 | Case |
| U13 | Intel 82806AA PCI-64 Hub (P64H) | 93 | Case |
| U16 | Adaptec AIC-7896 SCSI controller | 85 | Case |
| XU1, XU2, XU3, XU4 | 128MB, 256MB, or 512MB RIMM | 92 | Plate |
| U4 | Intel 82840 Memory Controller Hub (MCH) | 70 | Ambient |
| U2, U3 | Pentium III processor at 700MHz, 733MHz, 850MHz, or 866 MHz | 80 | Junction |

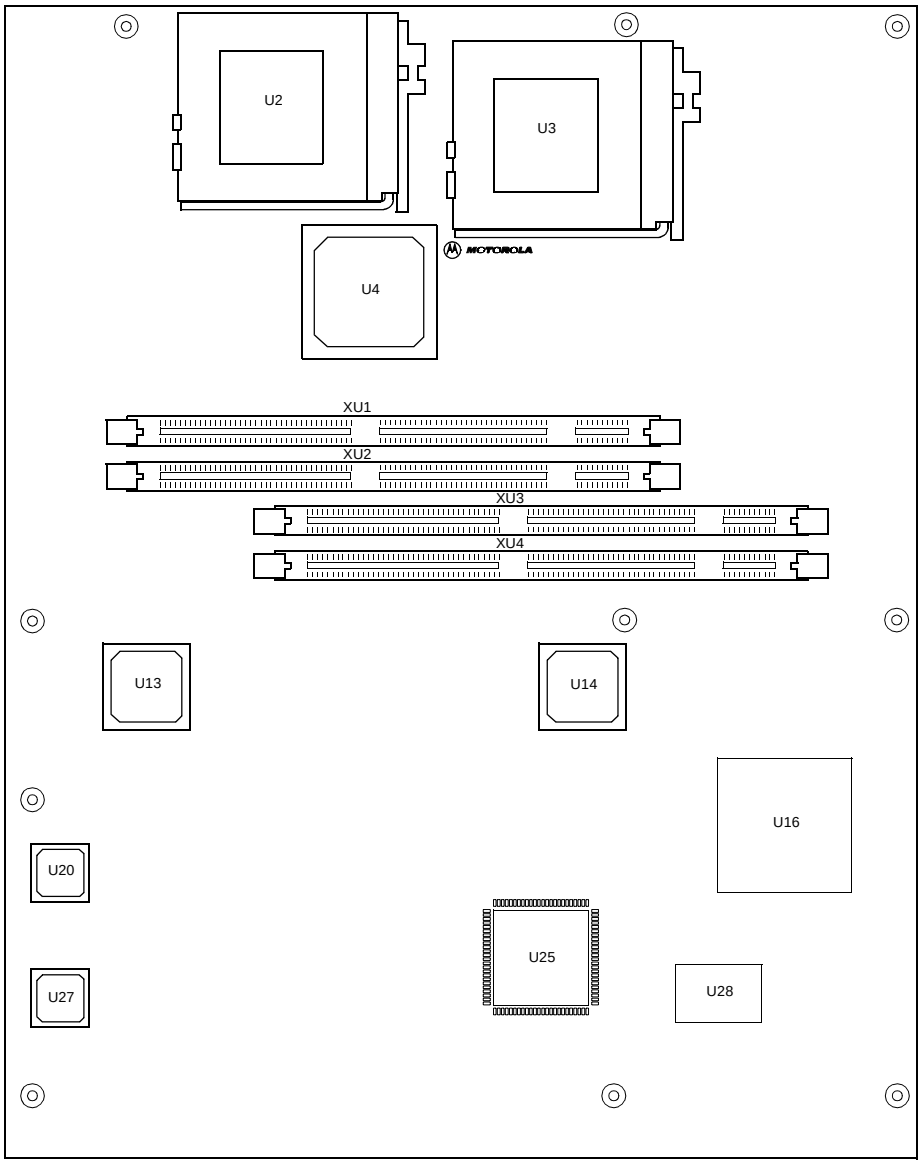



**Figure B-1. Thermally Significant Components—Primary Side**

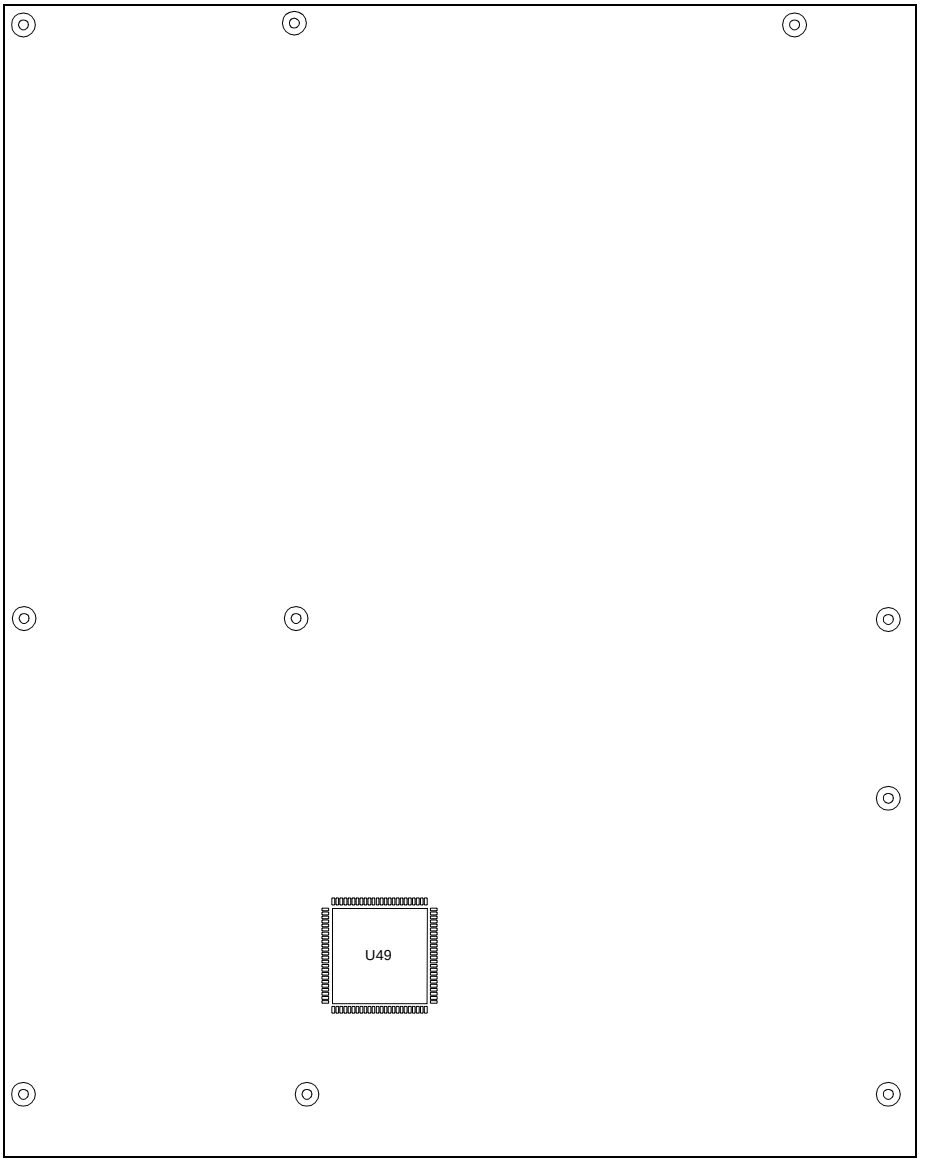



**Figure B-2. Thermally Significant Components—Secondary Side**

# Component Temperature Measurement



The following sections outline general temperature measurement methods. For the specific types of measurements required for thermal evaluation of this board, see Table B-1.

## Preparation

We recommend 40 AWG (American wire gauge) thermocouples for all thermal measurements. Larger gauge thermocouples can wick heat away from the components and disturb air flowing past the board.

Allow the board to reach thermal equilibrium before taking measurements. Most circuit boards will reach thermal equilibrium within 30 minutes. After the warm up period, monitor a small number of components over time to assure that equilibrium has been reached.

## Measuring Junction Temperature

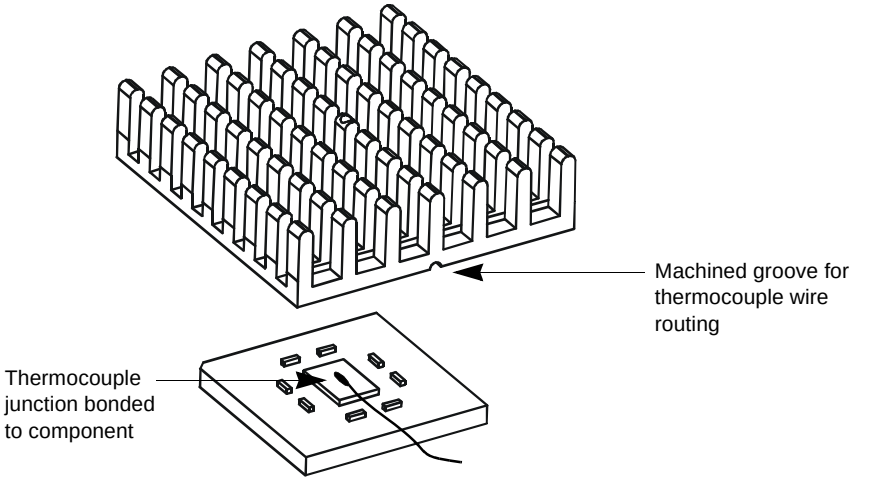
Some components have an on-chip thermal measuring device such as a thermal diode. For instructions on measuring temperatures using the on-board device, refer to the *PATX5000 BIOS and Programmer's Reference Guide* and to the component manufacturer's documentation listed in Appendix D, *Related Documentation*.

## Measuring Case Temperature

Measure the case temperature at the center of the top of the component. Make sure there is good thermal contact between the thermocouple junction and the component. We recommend you use a thermally conductive adhesive such as Loctite 384.

If components are covered by mechanical parts such as heatsinks, you will need to machine these parts to route the thermocouple wire. Make sure that the thermocouple junction contacts *only* the electrical component. Also make sure that heatsinks lay flat on electrical components. Figure B-3 shows one method of machining a heatsink base to provide a thermocouple routing path.

**Note** Machining a heatsink base reduces the contact area between the heatsink and the electrical component. You can partially compensate for this effect by filling the machined areas with thermal grease. The grease should not contact the thermocouple junction.



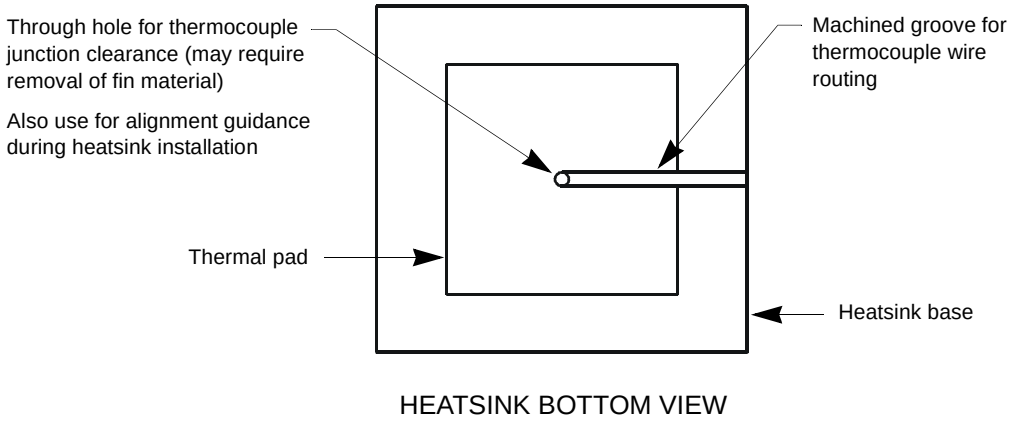




**Figure B-3. Mounting a Thermocouple Under a Heatsink**

## Measuring Local Air Temperature

Measure local component ambient temperature by placing the thermocouple downstream of the component. This method is conservative since it includes heating of the air by the component. The following figure illustrates one method of mounting the thermocouple.

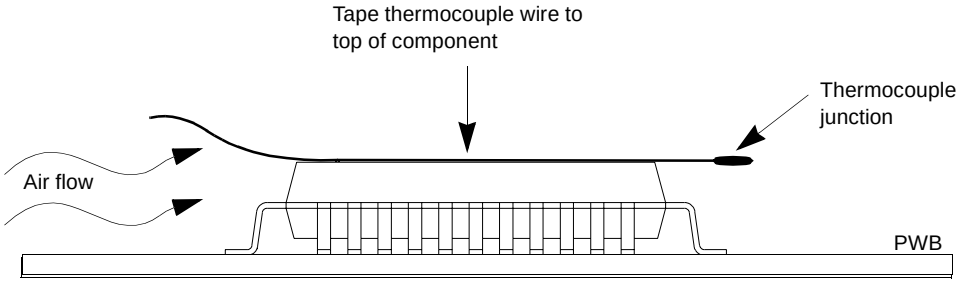



**Figure B-4. Measuring Local Air Temperature**

# Battery Replacement

C

Should it become necessary to replace the lithium battery on the PATX5000, follow the safety guidelines for handling lithium batteries given in this appendix to reduce hazards to users and equipment and to ensure proper battery operation. Use the batteries for their intended application only.

## Safety Guidelines

Lithium batteries incorporate flammable materials such as lithium and organic solvents. If lithium batteries are short-circuited or exposed to high temperature or pressure, they may burst open and ignite, possibly resulting in injury and/or fire. Lithium batteries are *never* to be recharged, opened, punctured, crushed, incinerated, exposed to high temperatures, or discarded in your general trash collection.

When dealing with lithium batteries, carefully follow the precautions listed below in order to prevent accidents:

- ❏ Do not short-circuit.
- ❏ Do not disassemble, deform, or apply excessive pressure.
- ❏ Do not heat or incinerate.
- ❏ Do not apply solder directly.
- ❏ Do not use different models, or new and old batteries together.
- ❏ Do not charge.
- ❏ Always check for proper polarity.

Replace the battery only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to local regulations and manufacturer’s instructions.

# Replacing Lithium Batteries



To replace the lithium battery on the PATX5000 motherboard, follow the procedure below and observe the guidelines for safety.

No tools are necessary for this procedure.

**Note** To prevent data loss, power must be applied to the board when you replace the battery.

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to a suitable ground as described under *Installation Preliminaries* on page 1-3. The ESD strap must be secured to your wrist and to ground throughout the procedure.

**Warning**

To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.

2. To remove the battery from the motherboard, carefully pull the battery from the socket.

**Caution**

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

3. Before installing a new battery, ensure that the battery pins are clean.

**Caution**

There is danger of explosion if the battery is replaced incorrectly.

4. Note the battery polarity and press the new battery into the socket.

   **Note** When the battery is in the socket, no soldering is required.

5. Recycle or dispose of the old battery according to local regulations and manufacturer's instructions.

# Battery Life



The service life of the lithium battery is very dependent on the ambient temperature of the board and the power-on duty cycle. In the case of the PATX5000, the anticipated battery life is typically 9.45 years at a storage temperature of 25° C. However, battery life may be drastically reduced at elevated storage temperatures (above 45° C).

# Related Documentation

D

## MCG Documents

The Motorola Computer Group publication listed below is referenced in this manual. You can obtain paper or electronic copies of MCG publications by:

- ❏ Contacting your local Motorola sales office
- ❏ Visiting MCG's World Wide Web literature site, http://www.motorola.com/computer/literature

**Table D-1. Motorola Computer Group Documents**

| Document Title | Publication Number |
|---|---|
| PATX5000 BIOS and Programmer's Reference Guide | PATX5BOSA/RM |

To locate and view the most up-to-date product information in PDF or HTML format, visit http://www.motorola.com/computer/literature.

## Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As a further help, a source for the listed document is also provided. Please note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

D

## Table D-2. Manufacturers' Documents

| Document Title and Source | Publication Number |
|---|---|
| Pentium III Processor for the PGA370 Socket at 500MHz to 1GHz — Data Sheet<br>Intel Corporation<br>Web: http://developer.intel.com/design/PentiumIII/datashts | 24526407.pdf |
| Intel 82840 Memory Controller Hub (MCH) — Data Sheet<br>Intel Corporation<br>Web: http://developer.intel.com/design/chipsets/datashts | 29802002.pdf |
| Intel 82806AA PCI 64 Hub (P64H) — Data Sheet<br>Intel Corporation<br>Web: http://developer.intel.com/design/chipsets/datashts | 29802501.pdf |
| Intel 82801AA (ICH) and 82801AB (ICH0) I/O Controller Hub — Data Sheet<br>Intel Corporation<br>Web: http://developer.intel.com/design/chipsets/datashts | 29065503.pdf |
| Intel 82802AB/82802AC Firmware Hub (FWH) — Data Sheet<br>Intel Corporation<br>Web: http://developer.intel.com/design/chipsets/datashts | 29065804.pdf |
| Intel 82559 Fast Ethernet Multifunction PCI/Cardbus Controller — Data Sheet<br>Intel Corporation<br>Web: http://developer.intel.com/design/network/datashts | 73825902.pdf |
| LPC47B27x 100 Pin Enhanced Super I/O Controller with LPC Interface — Data Sheet<br>Standard Microsystems Corporation (SMC)<br>Web: http://www.smsc.com/main | 47b27x.pdf |
| PC87200 PCI-to-ISA Bridge — Data Sheet<br>National Semiconductor<br>Web: http://www.national.com/pf/PC | PC87200.pdf |

**Table D-2. Manufacturers' Documents (continued)**

| Document Title and Source | Publication Number |
|---|---|
| LM81 Serial Interface ACPI-Compatible Microprocessor System Hardware Monitor — Data Sheet<br>National Semiconductor<br>Web: http://www.national.com/pf/LM | LM81.pdf |
| MAX1617 Remote/Local Temperature Sensor with SMbus Serial Interface — Data Sheet<br>Maxim Integrated Products<br>Web: http://www.maxim-ic.com/Datasheets | 1855.pdf |
| Cypress W134M Direct Rambus Clock Generator — Data Sheet<br>Cypress Semiconductor<br>Web: http://www.cypress.com/clock/datasheets | w134.pdf |
| Cypress W158 Spread Spectrum System Frequency Synthesizer — Data Sheet<br>Cypress Semiconductor<br>Web: http://www.cypress.com/clock/datasheets | w158.pdf |



# Related Specifications

For additional information, refer to the following table for related specifications. As an additional aid, sources for the listed documents are provided as well. Please note that in some cases, the information may be preliminary and the revision levels of the documents are subject to change without notice.

D

## Table D-3. Related Specifications

| Document Title and Source | Publication Number |
|---|---|
| ATX Specification, version 2.03<br>Created by Intel Corporation<br>Available on the World Wide Web through Teleport Internet Services at URL: http://www.teleport.com/~atx/index.htm | atx2_03.pdf |
| Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.1<br>PCI Special Interest Group<br>2575 NE Kathryn St. #17<br>Hillsboro, OR 97124<br>Telephone: 1-800-433-5177 or (503) 693-6232<br>FAX: (503) 693-8344<br>Web: http://www.pcisig.com | PCI Local Bus Specification |
| Bidirectional Parallel Port Interface Specification<br>Institute of Electrical and Electronics Engineers, Inc.<br>Publication and Sales Department<br>345 East 47th Street<br>New York, NY 10017-21633<br>Telephone: 1-800-678-4333 | IEEE Standard 1284 |
| IEEE Standard for Local Area Networks: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications<br>Institute of Electrical and Electronics Engineers, Inc.<br>Publication and Sales Department<br>345 East 47th Street<br>New York, NY 10017-21633<br>Telephone: 1-800-678-4333 | IEEE Standard 802.3 |

## Table D-3. Related Specifications (continued)

| Document Title and Source | Publication Number |
|---|---|
| Information Technology - Local and Metropolitan Networks - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications<br>Global Engineering Documents<br>Suite 400<br>1991 M Street, NW<br>Washington, DC 20036<br>Telephone: 1-800-854-7179<br>Telephone: (303) 397-7956<br>Web: http://global.ihs.com | ISO/IEC 8802-3 |
| Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange (EIA-232-D)<br>Global Engineering Documents<br>Suite 400<br>1991 M Street, NW<br>Washington, DC 20036<br>Telephone: 1-800-854-7179<br>Telephone: (303) 397-7956<br>Web: http://global.ihs.com | ANSI/EIA-232-D Standard |
| Universal Host Controller Interface (UHCI) — Design Guide<br>Intel Corporation | UHCI Revision 1.1 |
| Accelerated Graphics Port Interface Specification, Revision 2.0<br>Open Host Controller Interface Specification for USB<br>Intel Corporation<br>Web: http://www.intel.com/pc-supp/platform/agfxport | agp20.pdf |
| Universal Serial Bus (USB)<br>Intel Corporation | 297773-001 |
| Open HCI<br>Open Host Controller Interface Specification for USB<br>Compaq Corporation<br>Microsoft Corporation<br>National Semiconductor | Open HCI Release 1.0 12/15/95 |

# Index

INDEX

## T



## U



INDEX