Phoenix AT

Motherboard
Installation Guide

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First Edition.

Introduction

Thank you for your purchase of the Phoenix AT industrial embedded motherboard. The Phoenix AT design was based on the Intel 875P chipset providing the ideal platform to industrial applications. The Phoenix AT design is based on the Intel Pentium IV (mPGA478) processor.

With proper installation and maintenance, your Phoenix AT will provide years of high performance and trouble free operation.

This manual provides a detailed explanation into the installation and use of the Phoenix AT industrial embedded motherboard. This manual is written for the novice PC user/installer. However, as with any major computer component installation, previous experience is helpful and should you not have prior experience, it would be prudent to have someone assist you in the installation. This manual is broken down into 3 chapters and 3 appendixes.

Chapter 1 - System Board Pre-Configuration

This chapter provides all the necessary information for installing the Phoenix AT. Topics discussed include: installing the CPU (if necessary), DRAM installation and jumper settings. Connecting all the cables from the system board to the chassis and peripherals is also explained.

Chapter 2 - BIOS Configuration

This chapter shows the final step in getting your system firmware setup.

Chapter 3 - Upgrading

The Phoenix AT provides a number of expansion options including memory. All aspects of the upgrade possibilities are covered.

Appendix A - Technical Specifications

A complete listing of all the major technical specifications of the Phoenix AT is provided.

Appendix B - Flash BIOS Programming and Codes

Provides all information necessary to program your AMIBIOS8 Flash BIOS. POST Codes and beep codes are described in details.

Appendix C – On-Board Industrial Devices

Two on-board 10/100/1000 (one 10/100 optional) Ethernet controllers (second 10/100/1000 Ethernet optional), three serial ports (one optional RS422/485), ISA bridge and Post Code Display.

Static Electricity Warning!

The Phoenix AT has been designed as rugged as possible but can still be damaged if jarred sharply or struck. Handle the motherboard with care.
The Phoenix AT also contains delicate electronic circuits that can be damaged or weakened by static electricity. Before removing the Phoenix AT from its protective packaging, it is strongly recommended that you use a grounding wrist strap. The grounding strap will safely discharge any static electricity build up in your body and will avoid damaging the motherboard. Do not walk across a carpet or linoleum floor with the bare board in hand.

Warranty

This product is warranted against material and manufacturing defects for two years from the date of delivery. Buyer agrees that if this product proves defective the manufacturer is only obligated to repair, replace or refund the purchase price of this product at manufacturer's discretion. The warranty is void if the product has been subjected to alteration, misuse or abuse; if any repairs have been attempted by anyone other than the manufacturer; or if failure is caused by accident, acts of God, or other causes beyond the manufacturer's control.

Phoenix AT - An Overview

The Phoenix AT represents the ultimate in industrial embedded motherboard technology. No other system board available today provides such impressive list of features:

CPU Support

- Supports full series of Intel Pentium IV (mPGA478 4000MHZ, 533MHz and 800MHz PSB) processors featuring Intel Hyper-Threading technology.

Supported Bus Clocks

- 400MHz, 533MHz and 800MHz.

Memory

- Four DIMM sockets up to 4GB DDR SDRAM, PC2100 (DDR 266MHz), PC2700 (DDR 333MHz) and PC3200 (DDR 400MHz) featuring dual channel and dynamic mode. Please, refer to chapter 3 for memory details.

On-Board I/O

- 2 Floppies up to 2.88 MB.
- Dual/Quad independent Serial ATA ports with transfer rates up to 150 MB/s per port (optional).
- Dual channel PCI 32-bit EIDE controller – UDMA 66/100 supported. One extra connector (mini-Header 44 pin) in parallel to IDE2 for Solid State IDE disk or any 44 pin IDE device support.
- Three high speed RS-232 serial ports 16 Bytes FIFO (16550). COMB optional RS-232 IrDA, COMC optional RS-422/485.
- One Centronics™ compatible bi-directional parallel port. EPP/ECP mode compatible.
- One AT keyboard connectors.
- Auxiliary Keyboard/Mouse header for front panel access.
- Six Universal Serial Bus connectors, USB 1.1 and USB 2.0 compliant.
- Three 32-bit PCI slots, three 16-bit ISA slots (one sharing location with PCI slot 3) and one AGP PRO 8x slot.

- Two Ethernet header connectors (second 10/100/1000 optional, first optional 10/100/1000).
- Power Button – advanced management support.
- Ten GPIOs in a Header (optional).
- Automatic CPU voltage & temperature monitoring device (optional).
- On-board Buzzer.
- Audio AC97 compliant. Microphone In, Stereo Line In and Out, Auxiliary CD/Audio In.
- On-board POST Display Diagnostics.

ROM BIOS

- American Megatrends AMIBIOS8 with FLASH ROM.

Conventions Used in this Manual

Notes - Such as a brief discussion of memory types.

Important Information - such as static warnings, or very important instructions.

When instructed to enter keyboard keystrokes, the text will be noted by this graphic.

Chapter 1 Pre-Configuration

This chapter provides all the necessary information for installing the Phoenix AT into a standard PC chassis. Topics discussed include: installing the CPU (if necessary), DRAM installation and jumper settings.

Handling Precautions

The Phoenix AT has been designed to be as rugged as possible but it can be damaged if dropped, jarred sharply or struck. Damage may also occur by using excessive force in performing certain installation procedures such as forcing the system board into the chassis or placing too much torque on a mounting screw.

Take special care when installing or removing the system memory DIMMs. Never force a DIMM into a socket. Screwdrivers slipping off a screw and scraping the board can break a trace or component leads, rendering the board unusable. Always handle the Phoenix AT with care.

Special Warranty Note:

Products returned for warranty repair will be inspected for damage caused by improper installation and misuse as described in the previous section and the static warning below. Should the board show signs of abuse, the warranty will become void and the customer will be billed for all repairs and shipping and handling costs.

Static Warning

The Phoenix AT contains delicate electronic semiconductors that are highly sensitive to static electricity. These components, if subjected to a static electricity discharge, can be weakened thereby reducing the serviceable life of the system board. BEFORE THE BOARD IS

REMOVED FROM ITS PROTECTIVE ANTISTATIC PACKAGING, TAKE PROPER PRECAUTIONS! Work on a conductive surface that is connected to the ground. Before touching any electronic device, ground yourself by touching an unpainted metal object or, and highly recommended, use a grounding strap.

Step 1 Setting the Jumpers

Your Phoenix AT is equipped with a large number of peripherals. As such, there are a large number of configuration jumpers on the board. Taken step by step, setting these jumpers is easy. We suggest you review each section and follow the instructions.

Special note about operating frequency:
The Phoenix AT has the ability to run at a variety of speeds without the need to change any crystal, oscillator or jumper.

Jumper Types

Jumpers are small copper pins attached to the system board. Covering two pins with a shunt closes the connection between them. The Phoenix AT examines these jumpers to determine specific configuration information. There are two different categories of jumpers on the Phoenix AT.

A. Two pin jumpers are used for binary selections such as enable, disable. Instructions for this type of jumper are open, for no shunt over the pins or closed, when the shunt covers the pins.

B. Three or four pin jumpers are used for multiple selections. Instructions for these jumpers will indicate which two pins to cover. For example: for JP*x* 2-3 the shunt will be covering pins 2 and 3 leaving pins 1 and 4 exposed.

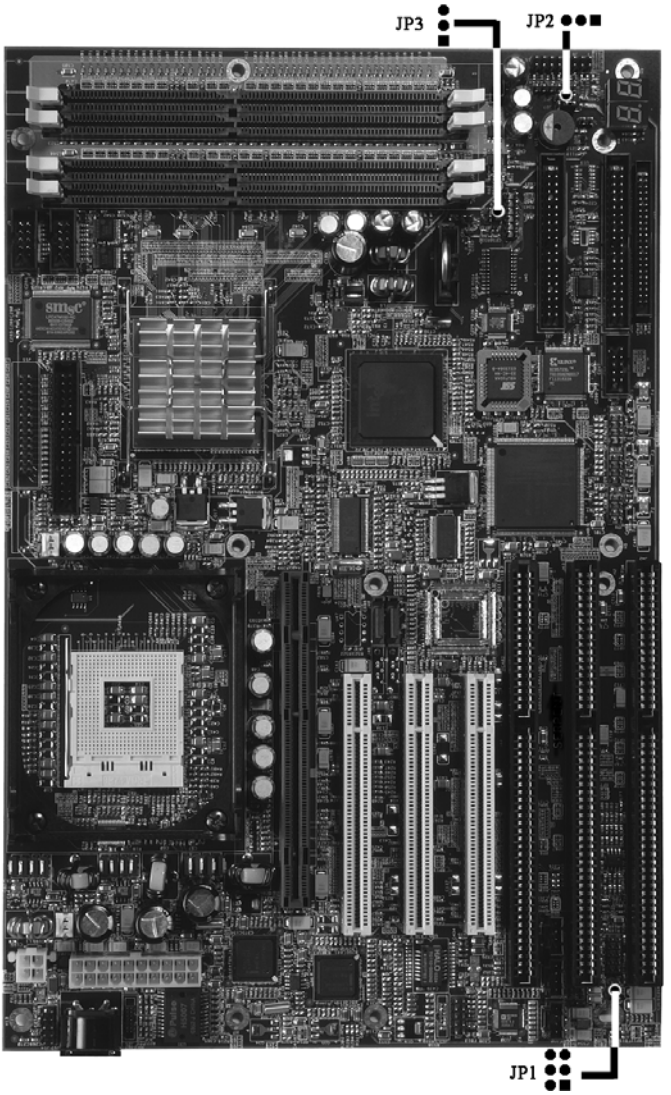
How to identify pin number 1 on *Figure 1-1*: Looking to the solder side (The board side without components) of the PCB (Printed Circuit Board), pin number 1 will have a squared pad ■. Other pins will have a circular pad ●. They are numbered sequentially.

Double row jumpers are numbered alternately, i.e. pin number 2 is in the other row, but in the same column of pin number 1. Pin number 3 is in the same row of pin 1, but in the next column and so forth.

Jumper Locations

Use the diagram below and the tables on the following pages to locate and set the on-board configuration jumpers.

Figure 1-1 Jumper Locations



CMOS Reset

This option is provided as a convenience for those who need to reset the CMOS registers. It should always be set to "Normal" for standard operation. If the CMOS needs to be reset, turn off the system, move JP3 to 2-3, move jumper to 1-2 and turn the system on.

Table 1-1 CMOS Reset

Reset CMOS	Normal	Clear CMOS
JP3	1-2*	2-3

** Manufacturer's Settings.*

ATA-Disk Connector Voltage Selection

The ATA-Disk Connector J33 can provide either 5Vcc or 3.3Vcc. The jumper JP2 selects the voltage.

Table 1-2 ATA-Disk Connector Voltage Select

ATA-Disk Voltage	5Vcc	3.3Vcc
JP2	1-2*	2-3

**Manufacturer's Settings.*

Audio Jack Output Selection

The audio output on the header audio connector J17 can be selected to be stereo line out or stereo headphone out (amplified signal). The jumper JP1 selects the audio output signals.

Table 1-3 Audio Output Mode Selection

Audio Output Mode Selection	Headphone	Line Out
JP1	1-3, 2-4	3-5, 4-6*

** Manufacturer's Settings.*

Step 2 SDRAM, CPU, and Cables Installation

Depending upon how your Phoenix AT is configured you may need to install the following:

- SDRAM (DIMMs)
- CPU

Phoenix AT Memory Configuration

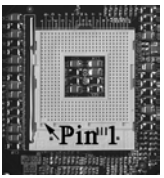
The Phoenix AT offers 4 DIMM memory sockets (Locations J34, J35, J36 and J37 – *Figure 1-3*). They can be configured with 2.5V unbuffered SDRAM DDR modules. It is very important that the quality of the DIMMs is good. Unreliable operation of the system may result if poor quality DIMMs are used. Always purchase your memory from a reliable source. Please, refer to chapter 3 for memory details.

CPU Installation

The Phoenix AT currently supports the following CPUs:

- Full series of Intel Pentium IV 400MHz, 533MHz and 800MHz PSB mPGA478 processors featuring Intel Hyper-Threading technology.

1. Improper installation of the CPU may cause permanent damage to both the system board and the CPU. -- Void of warranty
2. Always handle the CPU by the edges, never touch the pins.
3. Always use a heat-sink and a CPU fan.



Locate the CPU socket on your Phoenix AT system board (mPGA478 Socket – Location U43 – *Figure 1-3*). To install the processor, lift the lever of the ZIF socket and gently insert the CPU. The CPU will fit only in the right alignment. Make sure the CPU is inserted all the way. Lower the lever. Install the CPU

fan. Make sure it is locked and connected to J4 (see pin-out in Appendix A).

The continued push of technology to increase performance levels (higher operating speeds) and packaging density (more transistors) is aggravating the thermal management of the CPU. As operating frequencies increase and packaging sizes decreases, the power density increases and the thermal cooling solution space and airflow become more constrained. The result is an increased importance on system design to ensure that thermal design requirements are met for the CPU.

The objective of thermal management is to ensure that the temperature of the processor is maintained within functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet their specified performance requirements. Operation outside the functional limit can degrade system performance, cause logic errors or cause component and/or system damage. Temperatures exceeding the maximum operating limits may result in irreversible changes in the operating characteristics of the component.

If the Phoenix AT industrial embedded motherboard is acquired without the CPU and the thermal solution, extremely care must be taken to avoid improper thermal management. All Intel thermal solution specifications, design guidelines and suggestions to the CPU being used must be followed. The Phoenix AT warranty is void if the thermal management does not comply with Intel requirements.

Designing for thermal performance
In designing for thermal performance, the goal is to keep the processor within the operational thermal specifications. The inability to do so will shorten the life of the processor.

Fan Heatsink
An active fan heatsink can be employed as a mechanism for cooling the Intel processors. This is the acceptable solution for most chassis.
Adequate clearance must be provided around the fan heatsink to ensure unimpeded airflow for proper cooling.

Airflow management
It is important to manage the velocity, quantity and direction of air that flows within the system (and how it flows) to maximize the volume of air that flows over the processor.

Thermal interface management
To optimize the heatsink design for the Pentium IV processor, it is important to understand the impact of factors related to the interface between the processor and the heatsink base. Specifically, the bond line thickness, interface material area, and interface material thermal conductivity should be managed to realize the most effective thermal solution.
Once used, the thermal interface should be discarded and a new one installed. Never assemble the heatsink with a previously used thermal interface.

This completes the installation of the CPU. Now is it a good time to double check both the CPU and DIMM installation to make sure that these devices have been properly installed.

Installing Cables

Power and Control Panel Cables

The Phoenix AT gets power from the power connectors J2 and J3 (*Figure 1-3*). Use only ATX12V-compliant power supplies with the board. ATX12V power supplies have an additional power lead that provides required supplemental power for the processor. Always connect the 20-pin and 4-pin leads of ATX12V power supply to the corresponding connectors, otherwise the board will not boot. Do not use a standard ATX power supply. The board will not boot with a standard ATX power supply.

Installing Peripheral Cables

Now it is a good time to install the internal peripherals such as floppy and hard disk drives. Do not connect the power cable to these peripherals, as it is easier to attach the bulky ribbon cables before the smaller power connectors. If you are installing more than one IDE drive double check your master/slave jumpers on the drives. Review the information supplied with your drive for more information on this subject.

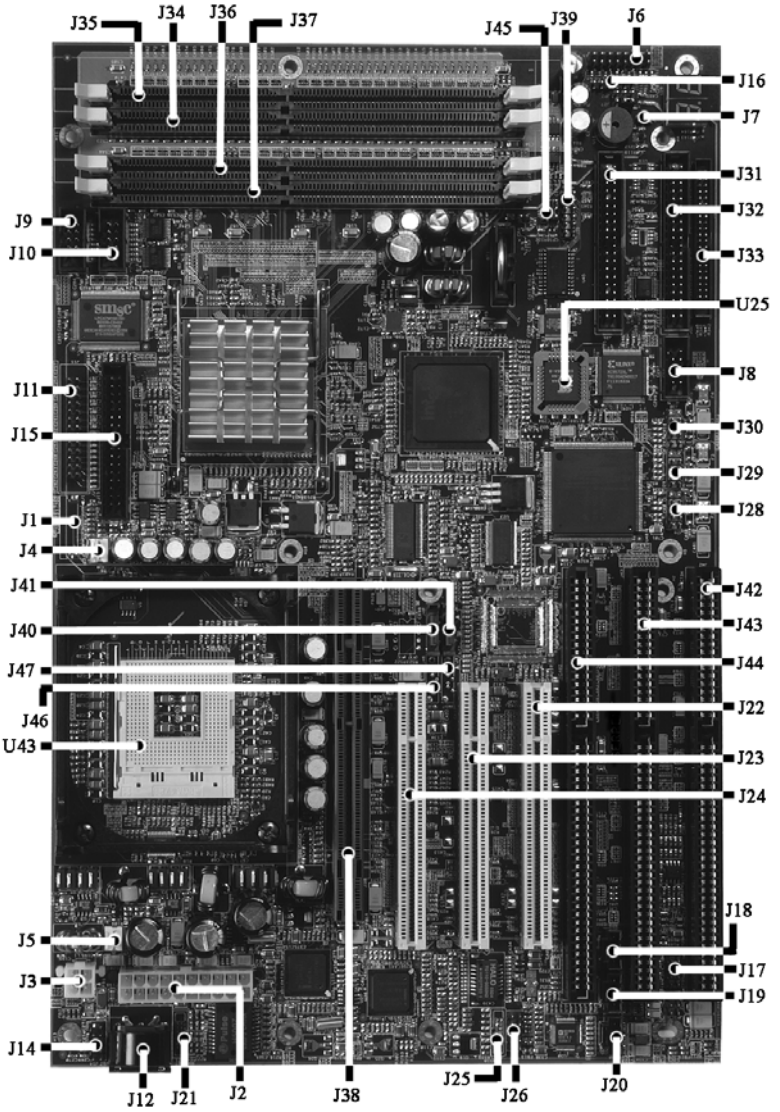
Most modern HDDs are UDMA-5 capable. To make use of the Ultra DMA-5 capabilities, 80-conductor cables must be used. The BIOS and the HDD will check for the existence of the 80-conductor cable. The

long leg of the cable must be connected to the board; otherwise it won't work as an 80-conductor cable. If connecting another peripheral that is not UDMA-5 capable (most optical devices are not), the whole IDE channel will be downgraded to UDMA-2. In that case, it is recommended to use a different IDE channel for the non-UDMA-5 capable peripherals.

Connect the floppy cable (not included) to the system board. Finally, connect the IDE cable (not included) to the system. If using a Solid State Device, connect it to the mini-ATA connector. Connect all interface cables to their headers. Then connect remaining ends of the ribbon cable to the appropriate peripherals.

This concludes the hardware installation of your Phoenix AT system. Now it is a good time to re-check all of the cable connections to make sure they are correct.

Figure 1-3 Location of Components and Connectors



Index of Connectors

Please refer to Appendix A for pin-out descriptions.

Table 1-4 Connectors description

Connector	Description
J1	ITP Header
J2	ATX Power Connector
J3	ATX Power Aux. Connector
J4	CPU Fan
J5	Rear Chassis Fan
J6	Front Panel Header
J7	Buzzer/Speaker Alt. Connector
J8	COM C
J9	COM A
J10	COM B
J11	LPT - Parallel
J12	Keyboard – AT Connector
J14	Keyboard/Mouse Header
J15	Floppy Disk Drive Connector
J16	JTAG
J17	Audio – Mic. In and Line Out/Headphone
J18	Audio – Aux. In
J19	Audio – CD In
J20	Audio – Line In
J21	Ethernet 2 10/100/1000 (Optional) Header
J22	PCI Connector 3
J23	PCI Connector 2
J24	PCI Connector 1
J25	Ethernet 1 10/100/1000 (Optional) Header
J26	Ethernet 1 10/100 Header
J28	USB Header (Ports 0 & 1)
J29	USB Header (Ports 2 & 3)
J30	USB Header (Ports 4 & 5)
J31	Primary IDE
J32	Secondary IDE

Connector	Description
J33	Alt. Secondary IDE – 44-pin
J34	DDR Channel B DIMM Socket 1
J35	DDR Channel B DIMM Socket 0
J36	DDR Channel A DIMM Socket 1
J37	DDR Channel A DIMM Socket 0
J38	AGP PRO 8x Slot
J39	GPIO Header (optional)
J40	SATA 1 (optional)
J41	SATA 2 (optional)
J42	ISA Slot 1
J43	ISA Slot 2
J44	ISA Slot 3
J45	Intruder detection Header
J46	SATA 3 (optional)
J47	SATA 4 (optional)
U25	BIOS Socket
U43	CPU Socket

User's Notes:

Chapter 2 AMIBIOS8 Setup

Your Phoenix AT features American Megatrends AMIBIOS8. The system configuration parameters are set via the BIOS setup. Since the BIOS Setup resides in the ROM BIOS, it is available each time the computer is turned on.

American Megatrends's AMIBIOS8 brand BIOS (Basic Input/Output System) pre-boot firmware is the industry's standard product used by most designers of X86 computer equipment in the world today. Its superior combination of configurability and functionality enables it to satisfy the most demanding ROM BIOS needs for x86 designers. Its modular architecture and high degree of configurability make it the most flexible BIOS in the world.

When your platform is powered on, AMIBIOS8 tests and initializes the hardware and programs the chipset and other peripheral components. During this time, Power On Self Test (POST) progress codes are written by the system BIOS to I/O port 80h, allowing the user to monitor the progress with a special monitor. Appendix B lists the POST codes and their meanings.
During early POST, no video is available to display error messages should a critical error be encountered; therefore, POST uses beeps on the speaker to indicate the failure of a critical system component during this time. Consult Appendix B for a list of Beep codes used by the BIOS.

Starting BIOS Setup

AMIBIOS has been integrated into many motherboards for over a decade. In the past, people often referred to the AMIBIOS setup menu as BIOS, BIOS setup, or CMOS setup.
American Megatrends refers to this setup as ezPORT. Specifically, it is the name of theAMIBIOS8 BIOS setup utility. This chapter describes the basic navigation of the ezPORT setup screens.

To enter the ezPORT setup screens, follow the steps below:
1 Power on the motherboard
2 Press the <Delete> key on your keyboard when you see the following text prompt:
`Press DEL to run Setup`

3 After you press the <Delete> key, the ezPORT main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as the Chipset and PCI/PnP menus.

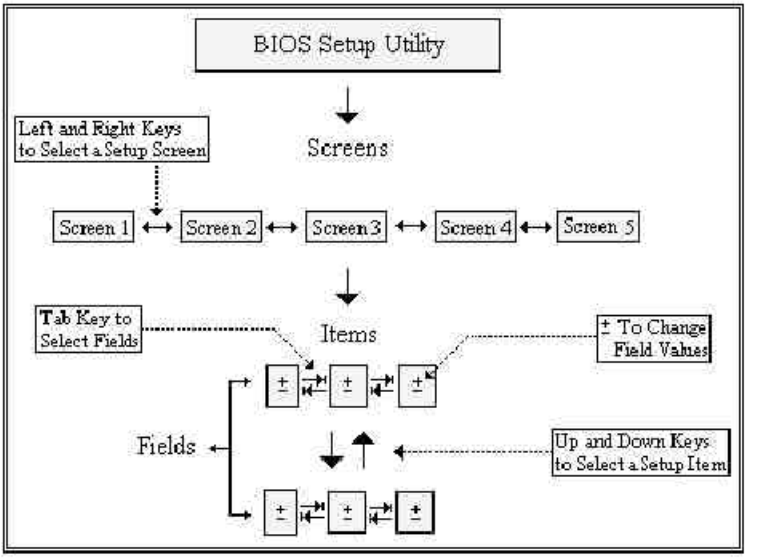
BIOS Setup Main Menu

The ezPORT main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in the Chapter 2.

The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed-out" options cannot be configured. Options in blue can be.

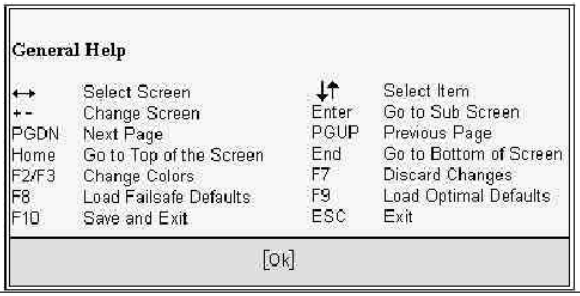
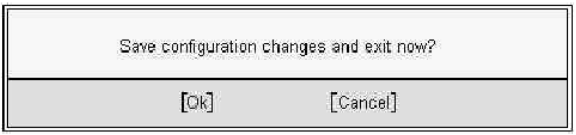
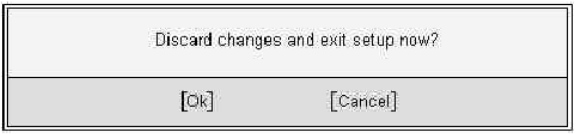
The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

The ezPORT BIOS setup/utility uses a key-based navigation system called hot keys. Most of the ezPORT BIOS setup utility hot keys can be used at any time during the setup navigation process. These keys include <F1>, <F10>, <Enter>, <ESC>, <Arrow> keys, and so on.



The <F8> key on your keyboard is the Fail-Safe key. It is not displayed on the ezPORT key legend by default. To set the Fail-Safe settings of the BIOS, press the <F8> key on your keyboard. It is located on the upper row of a standard 101 keyboard. The Fail-Safe settings allow the motherboard to boot up with the least amount of options set. This can lessen the probability of conflicting settings.

Hot Key	Description
→← Left/Right	The *Left and Right* <Arrow> keys allow you to select an ezPORT setup screen. For example: Main screen, Advanced screen, Chipset screen, and so on.
↑↓ Up/Down	The *Up and Down* <Arrow> keys allow you to select an ezPORT setup item or sub-screen.
+- Plus/Minus	The *Plus and Minus* <Arrow> keys allow you to change the field value of a particular setup item. For example: Date and Time.
Tab	The <Tab> key allows you to select ezPORT setup fields.

Hot Key	Description
F1	The <F1> key allows you to display the *General Help screen*. Press the <F1> key to open the *General Help screen*. 
F10	The <F10> key allows you to save any changes you have made and exit ezPORT Setup. Press the <F10> key to save your changes. The following screen will appear:  Press the <Enter> key to save the configuration and exit. You can also use the <Arrow> key to select *Cancel* and then press the <Enter> key to abort this function and return to the previous screen.
ESC	The <Esc> key allows you to discard any changes you have made and exit the ezPORT Setup. Press the <Esc> key to exit the ezPORT setup without saving your changes. The following screen will appear:  Press the <Enter> key to discard changes and exit. You can also use the <Arrow> key to select *Cancel* and then press the <Enter> key to abort this function and return to the previous screen.
Enter	The <Enter> key allows you to display or change the setup option listed for a particular setup item. The <Enter> key can also allow you to display the setup sub- screens.

Main Setup

When you first enter the ezPORT Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the *Main* tab. There are two Main Setup options.

System Time/System Date
Use this option to change the system time and date. Highlight *System Time* or *System Date* using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.
Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

Advanced BIOS Setup

Select the *Advanced* tab from the ezPORT setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as SuperIO Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section.

CPU CONFIGURATION SCREEN

Information about the CPU
If using an unlocked ratio CPU (Intel Engineering Samples), the Ratio CMOS Setting and VID CMOS settings become valid. For regular commercial CPUs those settings have no effect.

Max CPUID Value Limit
Enable this option to boot OSes that don't support CPUs with extended CPUID functions. The Optimal and Fail-Safe default setting is *Disabled.*

Disabled.
Enabled.

Hyper Threading Technology
Set this option to enable or disable Hyper-Threading technology. This option should only be enabled if the OS is capable of handling Hyper-Threading, e.g. Windows XP SP1 and some Linux flavors. The optimal and fail-safe default is *disabled*.

Disabled.
Enabled.

IDE CONFIGURATION SCREEN

IDE Configuration Settings

You can use this screen to select options for the IDE Configuration Settings. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. A description of the selected item appears on the right side of the screen.

Onboard PCI IDE Controller

This item specifies the IDE channels used by the onboard PCI IDE controller. The settings are *Disabled, Primary, Secondary,* or *Both.* The Optimal and Fail-Safe default setting is *Both.*

Disabled Set this value to prevent the computer system from using the onboard IDE controller.

Primary Set this value to allow the computer system to detect only the Primary IDE channel. This includes both the Primary Master and the Primary Slave.

Secondary Set this value to allow the computer system to detect only the Secondary IDE channel. This includes both the Secondary Master and the Secondary Slave.

Both Set this value to allow the computer system to detect the Primary and Secondary IDE channels.

This includes both the Primary Master, Primary Slave, Secondary Master, and Secondary Slave. This is the default setting.

Primary IDE Master, Primary IDE Slave, Secondary IDE Master, Secondary IDE Slave

Select one of the hard disk drives to configure it. Press <Enter> to access the sub menu. The options on the sub menu are described in the following sections.

Hard disk drive Write Protect

Set this option to protect the hard disk drive from being overwritten. The Optimal and Fail-Safe default setting is *Disabled*.

Disabled Set this value to allow the hard disk drive to be used normally. Read, write, and erase functions can be performed to the hard disk drive. This is the default setting.

Enabled Set this value to prevent the hard disk drive from being erased.

IDE Detect Time Out (Seconds)

Set this option to stop the AMIBIOS from searching for IDE devices within the specified number of seconds. Basically, this allows you to fine-tune the settings to allow for faster boot times. Adjust this setting until a suitable timing that can detect all IDE disk drives attached is found.

The Optimal and Fail-Safe default setting is *35*.

0 This value is the best setting to use if the onboard IDE controllers are set to a specific IDE disk drive in the AMIBIOS.

5 Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in five seconds. A large majority of ultra ATA hard disk drives can be detected well within five seconds.

10 Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 10 seconds.

15 Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 15 seconds.

20 Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 20 seconds.

25 Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 25 seconds.

30 Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 30 seconds.

35 *35* is the default value. It is the recommended setting when all IDE connectors are set to *AUTO* in the AMIBIOS setting.

Note: Different IDE disk drives take longer for the BIOS to locate than others do.

ATA (PI) 80 pin Cable Detection

Set this option to select the method used to detect the ATA (PI) 80 pin cable. The Optimal and Fail-Safe setting is *Host & Device*.

Host & Device Set this value to use both the motherboard onboard IDE controller and IDE disk drive to detect the type of IDE cable used. This is the default setting.

Host Set this value to use motherboard onboard IDE controller to detect the type of IDE cable used.

Device Set this value to use IDE disk drive to detect the type of IDE cable used.

The use of an 80-conductor ATA cable is mandatory for running Ultra ATA/66 and Ultra ATA/100 IDE hard disk drives. The standard 40-conductor ATA cable cannot handle the higher speeds.

80-conductor ATA cable is plug compatible with the standard 40-conductor ATA cable. Because of this, the system must determine the presence of the correct cable. This detection is achieved by having a break in one of the lines on the 80-conductor ATA cable that is normally an unbroken connection in the standard 40-conductor ATA cable. It is this break that is used to make this determination. The AMIBIOS can instruct the drive to run at the correct speed for the cable type detected.

PRIMARY AND SECONDARY IDE MASTER AND SLAVE SUB MENU

Primary and Secondary IDE Master and Slave Settings

From the IDE Configuration screen, press <Enter> to access the sub menu for the primary and secondary IDE master and slave drives. Use this screen to select options for the Primary and Secondary IDE drives. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages.

Drive Parameters

The "grayed-out" items in the left frame are the IDE disk drive parameters taken from the firmware of the IDE disk drive selected. The drive parameters listed are as follows:

Device Type of device, such as Hard disk drive.

Vendor Manufacturer of the device.

Size The size of the device.

LBA Mode LBA (Logical Block Addressing) is a method of addressing data on a disk drive. Your AMIBIOS is already equipped with 48-bit LBA mode addressing.

Block Mode Block mode boosts IDE drive performance by increasing the amount of data transferred. Only 512 bytes of data can be transferred per interrupt if block mode is not used. Block mode allows transfers of up to 64 KB per interrupt.

PIO Mode IDE PIO mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases.

Async DMA This indicates the highest Asynchronous DMA Mode that is supported.

Ultra DMA This indicates the highest Synchronous DMA Mode that is supported.

S.M.A.R.T. Self-Monitoring Analysis and Reporting Technology protocol used by IDE drives of some manufacturers to predict drive failures.

Type

This option sets the type of device that the AMIBIOS attempts to boot from after the Power-On Self-Test (POST) has completed. The Optimal and Fail-Safe default setting is *Auto.*

Not Installed Set this value to prevent the BIOS from searching for an IDE disk drive on the specified channel.

Auto Set this value to allow the BIOS auto detect the IDE disk drive type attached to the specified channel. This setting should be used if an IDE hard disk drive is attached to the specified channel. This is the default setting.

CDROM This option specifies that an IDE CD-ROM drive is attached to the specified IDE channel. The BIOS will not attempt to search for other types of IDE disk drives on the specified channel.
ARMD This option specifies an ATAPI Removable Media Device. This includes, but is not limited to:

- ZIP
- LS-120
- MO

LBA/Large Mode

LBA (Logical Block Addressing) is a method of addressing data on a disk drive. The Optimal and Fail-Safe default setting is *Auto.*

Note: Your AMIBIOS is equipped with 48-bit LBA mode addressing for drive capacities over 137 GB.

Disabled Set this value to prevent the BIOS from using Large Block Addressing mode control on the specified channel.
Auto Set this value to allow the BIOS to auto detect the Large Block Addressing mode control on the specified channel. This is the default setting.

Block (Multi-Sector Transfer)

This option sets the block mode multi sector transfers option. The Optimal and Fail-Safe default setting is *Auto.*

Disabled Set this value to prevent the BIOS from using Multi-Sector Transfer on the specified channel. The data to and from the device will occur one sector at a time.
Auto Set this value to allow the BIOS to auto detect device support for Multi-Sector Transfers on the specified channel. If supported, Set this value to allow the BIOS to auto detect the number of sectors per block for transfer from the hard disk drive to the memory. The data transfer to and from the device will occur multiple sectors at a time. This is the default setting.

PIO Mode

IDE PIO (Programmable I/O) mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases. The Optimal and Fail-Safe default setting is *Auto*.

Auto Set this value to allow the BIOS to auto detect the PIO mode. Use this value if the IDE disk drive support cannot be determined. This is the default setting.
0 Set this value to allow the BIOS to use PIO mode 0. It has a data transfer rate of 3.3 MBs.
1 Set this value to allow the BIOS to use PIO mode 1. It has a data transfer rate of 5.2 MBs.
2 Set this value to allow the BIOS to use PIO mode 2. It has a data transfer rate of 8.3 MBs.

3 Set this value to allow the BIOS to use PIO mode 3. It has a data transfer rate of 11.1 MBs.
4 Set this value to allow the BIOS to use PIO mode 4. It has a data transfer rate of 16.6 MBs. This setting generally works with all hard disk drives manufactured after 1999. For other disk drive, such as IDE CD-ROM drives, check the specifications of the drive.

DMA Mode

This setting allows you to adjust the DMA mode options. The Optimal and Fail-Safe default setting is *Auto*.

Auto Set this value to allow the BIOS to auto detect the DMA mode. Use this value if the IDE disk drive support cannot be determined. This is the default setting.
SWDMA0 Set this value to allow the BIOS to use Single Word DMA mode 0. It has a data transfer rate of 2.1 MBs.
SWDMA1 Set this value to allow the BIOS to use Single Word DMA mode 1. It has a data transfer rate of 4.2 MBs.
SWDMA2 Set this value to allow the BIOS to use Single Word DMA mode 2. It has a data transfer rate of 8.3 MBs.
MWDMA0 Set this value to allow the BIOS to use Multi Word DMA mode 0. It has a data transfer rate of 4.2 MBs.
MWDMA1 Set this value to allow the BIOS to use Multi Word DMA mode 1. It has a data transfer rate of 13.3 MBs.
MWDMA2 Set this value to allow the BIOS to use Multi Word DMA mode 2. It has a data transfer rate of 16.6 MBs.
UDMA0 Set this value to allow the BIOS to use Ultra DMA mode 0. It has a data transfer rate of 16.6 MBs. It has the same transfer rate as PIO mode 4 and Multi Word DMA mode 2.
UDMA1 Set this value to allow the BIOS to use Ultra DMA mode 1. It has a data transfer rate of 25 MBs.
UDMA2 Set this value to allow the BIOS to use Ultra DMA mode 2. It has a data transfer rate of 33.3 MBs.
UDMA3 Set this value to allow the BIOS to use Ultra DMA mode 3. It has a data transfer rate of 44.4 MBs. To use this mode, it is required that an 80-conductor ATA cable is used.
UDMA4 Set this value to allow the BIOS to use Ultra DMA mode 4. It has a data transfer rate of 66.6 MBs. To use this mode, it is required that an 80-conductor ATA cable is used.
UDMA5 Set this value to allow the BIOS to use Ultra DMA mode 5. It has a data transfer rate of 99.9 MBs. To use this mode, it is required that an 80-conductor ATA cable is used.

S.M.A.R.T. for Hard disk drives

Self-Monitoring Analysis and Reporting Technology (SMART) feature can help predict impending drive failures. The Optimal and Fail-Safe default setting is *Auto*.

Auto Set this value to allow the BIOS to auto detect hard disk drive support. Use this setting if the IDE disk drive support cannot be determined. This is the default setting.

Disabled Set this value to prevent the BIOS from using the SMART feature.

Enabled Set this value to allow the BIOS to use the SMART feature on support hard disk drives.

32Bit Data Transfer

This option sets the 32-bit data transfer option. The Optimal and Fail-Safe default setting is *Enabled*.

Disabled Set this value to prevent the BIOS from using 32-bit data transfers.

Enabled Set this value to allow the BIOS to use 32-bit data transfers on support hard disk drives. This is the default setting.

ARMD Emulation Type

ATAPI Removable Media Device (ARMD) is a device that uses removable media, such as the LS120, MO (Magneto-Optical), or Iomega Zip drives. If you want to boot up from media on an ARMD, it is required that you emulate boot up from a floppy or hard disk drive. This is especially necessary when trying to boot to DOS. You can select the type of emulation used if you are booting from such a device. The Optimal and Fail-Safe default setting is *Auto*.

Auto Set this value to allow the BIOS to automatically set the emulation used by ARMD. This is the default setting.

Floppy Set this value for ARMD to emulate a floppy drive during boot up.

Hard disk drive Set this value for ARMD to emulate a hard disk drive during boot up.

FLOPPY CONFIGURATION SCREEN

Floppy Configuration Settings

You can use this screen to specify options for the Floppy Configuration Settings. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option.

Floppy Drive A: and B:

Move the cursor to these fields via up and down <arrow> keys. Select the floppy type. The Optimal setting for floppy drive A: is *1.44 MB 3½"*. The Fail-Safe setting for floppy drive A: is *1.44 MB 3½"*. The Optimal setting for floppy drive B: is *Disabled.* The Fail- Safe setting for floppy drive B: is *Disabled*.

Disabled Set this value to prevent the use of the selected floppy disk drive channel. This option should be set if no floppy disk drive is installed on the specified channel. This is the default setting for *Floppy Drive B*.

360 KB 5 ¼ " Set this value if the floppy disk drive attached to the corresponding channel is a 360 KB 5¼ " floppy disk drive.

1.2 MB 5 ¼ " Set this value if the floppy disk drive attached to the corresponding channel is a 1.2 MB 5¼ " floppy disk drive.
720 KB 3 ½ " Set this value if the floppy disk drive attached to the corresponding channel is a 720 KB 3½ " floppy disk drive.
1.44 MB 3 ½ " Set this value if the floppy disk drive attached to the corresponding channel is a 1.44 MB 3½ " floppy disk drive. This is the default setting for *Floppy Drive A*.

SUPER IO CONFIGURATION SCREEN

SuperIO Configuration Screen
You can use this screen to select options for the Super I/O settings. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option.

OnBoard Floppy Controller
Set this option to Enabled to enable the floppy drive controller on the motherboard. The settings are Enabled and Disabled. The default setting is Enabled.

Serial Port1 Address
This option specifies the base I/O port address and Interrupt Request address of serial port 1. The Optimal setting is *3F8/IRQ4*. The Fail-Safe default setting is *Disabled.*

Disabled Set this value to prevent the serial port from accessing any system resources. When this option is set to *Disabled*, the serial port physically becomes unavailable.
3F8/IRQ4 Set this value to allow the serial port to use 3F8 as its I/O port address and IRQ 4 for the interrupt address. This is the default setting. The majority of serial port 1 or COM1 ports on computer systems use IRQ4 and I/O Port 3F8 as the standard setting. The most common serial device connected to this port is a mouse. If the system will not use a serial device, it is best to set this port to *Disabled*.
2F8/IRQ3 Set this value to allow the serial port to use 2F8 as its I/O port address and IRQ 3 for the interrupt address. If the system will not use a serial device, it is best to set this port to *Disabled*.
3E8/IRQ4 Set this value to allow the serial port to use 3E8 as its I/O port address and IRQ 4 for the interrupt address. If the system will not use a serial device, it is best to set this port to *Disabled*.
2E8/IRQ3 Set this value to allow the serial port to use 2E8 as its I/O port address and IRQ 3 for the interrupt address. If the system will not use a serial device, it is best to set this port to *Disabled*.

Serial Port2 Address
This option specifies the base I/O port address and Interrupt Request address of serial port 2. The Optimal setting is *2F8/IRQ3*. The Fail-Safe setting is *Disabled.*

Disabled Set this value to prevent the serial port from accessing any system resources. When this option is set to *Disabled*, the serial port physically becomes unavailable.

3F8/IRQ4 Set this value to allow the serial port to use 3F8 as its I/O port address and IRQ 4 for the interrupt address. If the system will not use a serial device, it is best to set this port to Disabled.

2F8/IRQ3 Set this value to allow the serial port to use 2F8 as its I/O port address and IRQ 3 for the interrupt address. This is the default setting. The majority of serial port 2 or COM2 ports on computer systems use IRQ3 and I/O Port 2F8 as the standard setting. The most common serial device connected to this port is an external modem. If the system will not use an external modem, set this port to *Disabled*.

Note: Most internal modems require the use of the second COM port and use 3F8 as its I/O port address and IRQ 4 for its interrupt address. This requires that the Serial Port2 Address be set to *Disabled* or another base I/O port address and Interrupt Request address.

3E8/IRQ4 Set this value to allow the serial port to use 3E8 as its I/O port address and IRQ 4 for the interrupt address. If the system will not use a serial device, it is best to set this port to Disabled.

2E8/IRQ3 Set this value to allow the serial port to use 2E8 as its I/O port address and IRQ 3 for the interrupt address. If the system will not use a serial device, it is best to set this port to *Disabled*.

Serial Port2 Mode

This option allows installation of an Infra-red device by the Serial Port. The settings are Normal (*default*), IRDA and ASK IR.

Infra-Red Transmission Mode

The settings are Full Duplex (*default*) or Half Duplex.

Receiver/Transmitter Polarity

Sets polarity for IR modes.

Serial Port3 Address

This option specifies the base I/O port address and Interrupt Request address of serial port 3. The Optimal setting is *3E8/IRQ4*. The Fail-Safe default setting is *Disabled.*

Disabled Set this value to prevent the serial port from accessing any system resources. When this option is set to *Disabled*, the serial port physically becomes unavailable.

3F8/IRQ4 Set this value to allow the serial port to use 3F8 as its I/O port address and IRQ 4 for the interrupt address. If the system will not use a serial device, it is best to set this port to *Disabled*.

2F8/IRQ3 Set this value to allow the serial port to use 2F8 as its I/O port address and IRQ 3 for the interrupt address. If the system will not use a serial device, it is best to set this port to *Disabled*.

3E8/IRQ4 Set this value to allow the serial port to use 3E8 as its I/O port address and IRQ 4 for the interrupt address. If the system will not use a serial device, it is best to set this port to *Disabled*.

2E8/IRQ3 Set this value to allow the serial port to use 2E8 as its I/O port address and IRQ 3 for the interrupt address. If the system will not use a serial device, it is best to set this port to *Disabled*.

Parallel Port Address

This option specifies the I/O address used by the parallel port. The Optimal setting is *378*. The Fail-Safe setting is *Disabled*.

Disabled Set this value to prevent the parallel port from accessing any system resources. When the value of this option is set to *Disabled*, the printer port becomes unavailable.

378 Set this value to allow the parallel port to use 378 as its I/O port address. This is the default setting. The majority of parallel ports on computer systems use IRQ7 and I/O Port 378H as the standard setting.

278 Set this value to allow the parallel port to use 278 as its I/O port address.

3BC Set this value to allow the parallel port to use 3BC as its I/O port address.

Parallel Port Mode

This option specifies the parallel port mode. The Optimal setting is *Normal*. The Fail- Safe setting is *Disabled*.

Normal Set this value to allow the standard parallel port mode to be used. This is the default setting.

Bi-Directional Set this value to allow data to be sent to and received from the parallel port.

EPP The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bi-directional data transfer driven by the host device.

ECP The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits per second. ECP provides symmetric bi-directional communication.

Parallel Port IRQ

This option specifies the IRQ used by the parallel port. The Optimal and Fail-Safe default setting is *7*.

5 Set this value to allow the serial port to use Interrupt 5.

7 Set this value to allow the serial port to use Interrupt 7. This is the default setting. The majority of parallel ports on computer systems use IRQ7 and I/O Port 378h as the standard setting.

ACPI CONFIGURATION SCREEN

ACPI Configuration Screen

You can use this screen to select options for the ACPI settings. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option.

ACPI Aware O/S

Set this value to allow the system to utilize the Intel ACPI (Advanced Configuration and Power Interface) specification. The Optimal and Fail-Safe default setting is *Yes*.

No This setting should be set if the operating system in use does not comply with the ACPI (Advanced Configuration and Power Interface) specification. DOS® , Windows 3.x® , and Windows NT® are examples of non-ACPI aware operating systems.

Yes This setting should be set if the operating system complies with the ACPI (Advanced Configuration and Power Interface) specification. This is the default setting. Windows 95® , Windows 98® and Windows 2000® are examples of ACPI aware operating systems.

Advanced ACPI Configuration

You can use this screen to select options for the ACPI Advanced Configuration Settings. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. A description of the selected item appears on the right side of the screen.

ACPI 2.0

Set this value to allow or prevent the system to be complaint with the ACPI 2.0 specification.

No This setting prevents the BIOS from supporting the ACPI 2.0 specification. This is the default setting.

Yes This setting allows the BIOS to support the ACPI 2.0 specification.

AMI OEM Table

Set this value to allow the ACPI BIOS to add a pointer to an OEMB table in the Root System Description Table (RSDT) table.

Disabled This option disables adding an OEMB table.

Enabled This option enables adding an OEMB table. This is the default setting.

Note: OEMB table is used to pass POST data to the AML code during ACPI O/S operations.

RSDT

RSDT is the main ACPI table. It has no fixed place in memory. During the boot up process, the BIOS locates a pointer to the table during the memory scan. A Root System Descriptor Pointer (RSDP) is located in low memory space of the system. It provides the physical address of the RSDT. The RSDT itself is identified in memory because it starts with the signature "RSDT." Following the signature is an array of pointers that tell the operating system the location of other description tables that provide it with the information it needs about the standards defined on the current system and individual devices.

AML

ACPI Machine Language (AML) is a binary code format that the operating system's ACPI AML interpreter parses to discover the machine's properties. On boot up the BIOS startup code copies it into system memory, where it can be interpreted by the operating system's ACPI AML interpreter.

Headless Mode

This option is used to update the ACPI FACP table to indicate headless operations.

Disabled This option disables updating the ACPI FACP table to indicate headless operation. This is the default setting.

Enabled This option enables updating the ACPI FACP table to indicate headless operation.

MPS CONFIGURATION SCREEN

MPS Configuration Screen

You can use this screen to select options for the MPS settings. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option.

MPS Revision

MPS tables are requested for multi processors systems. To make use of the Intel Hyper-Threading technology, MPS tables must be built. Set this value to the desired MPS revision. The Optimal and Fail-Safe default setting is *1.1*.

1.1 revision 1.1 of the MPS specification standard.

1.4 revision 1.4 of the MPS specification standard.

USB CONFIGURATION SCREEN

USB Configuration Screen
You can use this screen to select options for the USB Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option.

Legacy USB Support
Legacy USB Support refers to the USB mouse and USB keyboard support. Normally if this option is not enabled, any attached USB mouse or USB keyboard will not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there is no USB drivers loaded on the system. Set this value to enable or disable the Legacy USB Support. The Optimal and Fail-Safe default setting is *Auto*.

Disabled Set this value to prevent the use of any USB device in DOS or during system boot.

Enabled Set this value to allow the use of USB devices during boot and while using DOS.

Auto This option auto detects USB Keyboards or Mice and if found, allows them to be utilized during boot and while using DOS.

USB 2.0 Controller Mode
Set this option to HiSpeed for 480Mbps or FullSpeed for 12Mbps.

USB Mass Storage Device Configuration Screen
You can use this screen to select options for the USB Mass Storage Devices Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option.

USB Mass Storage Device Delay
Set the value for the number of seconds that POST waits for the USB mass storage device after start unit command is issued. The options are 10, 20, 30 and 40 seconds.

Emulation Type
Set the emulation type to Auto, Floppy, Forced FDD, Hard Disk or CDROM. If Auto, USB devices less than 530MB will be emulated as floppy and remaining devices as Hard Drive. Forced FDD option can be used to force a formatted HDD device to boot as FDD (ex. ZIP Drive).

PCI/PnP Setup

Select the *PCI/PnP* tab from the ezPORT setup screen to enter the Plug and Play BIOS Setup screen. You can display a Plug and Play BIOS Setup option by highlighting it using the <Arrow> keys.

Plug and Play O/S
Set this value to allow the system to modify the settings for Plug and Play operating system support. The Optimal and Fail-Safe default setting is *Yes*.

No The *No* setting is for operating systems that do not meet the Plug and Play specifications. It allows the BIOS to configure all the devices in the system.

Yes The *Yes* setting allows the operating system to change the interrupt, I/O, and DMA settings. Set this option if the system is running Plug and Play aware operating systems.

PCI Latency Timer
Set this value to allow the PCI Latency Timer to be adjusted. This option sets the latency of all PCI devices on the PCI bus. The Optimal and Fail-Safe default setting is *64*.

32 This option sets the PCI latency to 32 PCI clock cycles.
64 This option sets the PCI latency to 64 PCI clock cycles. This is the default setting.
96 This option sets the PCI latency to 96 PCI clock cycles.
128 This option sets the PCI latency to 128 PCI clock cycles.
160 This option sets the PCI latency to 160 PCI clock cycles.
192 This option sets the PCI latency to 192 PCI clock cycles.
224 This option sets the PCI latency to 224 PCI clock cycles.
248 This option sets the PCI latency to 248 PCI clock cycles.

Allocate IRQ to VGA
Set this value to allow or restrict the system from giving the VGA adapter card an interrupt address. The Optimal and Fail-Safe default setting is *Yes*.

Yes Set this value to allow the allocation of an IRQ to a VGA adapter card that uses the PCI local bus. This is the default setting.

No Set this value to prevent the allocation of an IRQ to a VGA adapter card that uses the PCI local bus.

Palette Snooping
Set this value to allow the system to modify the Palette Snooping settings. The Optimal and Fail-Safe default setting is *Disabled*.

Disabled This is the default setting and should not be changed unless the VGA card manufacturer requires Palette Snooping to be Enabled.

Enabled This setting informs the PCI devices that an ISA based Graphics device is installed in the system. It does this so the ISA

based Graphics card will function correctly. This does not necessarily indicate a physical ISA adapter card. The graphics chipset can be mounted on a PCI card. Always check with your adapter card's manuals first, before modifying the default settings in the BIOS.

PCI IDE BusMaster

Set this value to allow or prevent the use of PCI IDE bus mastering. The Optimal and Fail-Safe default setting is *Disabled*.

Disabled Set this value to prevent PCI bus mastering. This is the default setting.

Enabled This option specifies that the IDE controller on the PCI local bus has mastering capabilities.

OffBoard PCI/ISA IDE Card

Set this value to allow the OffBoard PCI/ISA IDE Card to be selected. The Optimal and Fail-Safe default setting is *Auto*.

Auto This setting will auto select the location of an OffBoard PCI IDE adapter card. This is the default setting.

PCI Slot1 This setting will select PCI Slot 1 as the location of the OffBoard PCI IDE adapter card. Use this setting only if there is an IDE adapter card installed in PCI Slot 1.

PCI Slot2 This setting will select PCI Slot 2 as the location of the OffBoard PCI IDE adapter card. Use this setting only if there is an IDE adapter card installed in PCI Slot 2.

PCI Slot3 This setting will select PCI Slot 3 as the location of the OffBoard PCI IDE adapter card. Use this setting only if there is an IDE adapter card installed in PCI Slot 3.

PCI Slot4 This setting will select PCI Slot 4 as the location of the OffBoard PCI IDE adapter card. Use this setting only if there is an IDE adapter card installed in PCI Slot 4.

PCI Slot5 This setting will select PCI Slot 5 as the location of the OffBoard PCI IDE adapter card. Use this setting only if there is an IDE adapter card installed in PCI Slot 4.

PCI Slot6 Do not use this option.

IRQ

Set this value to allow the IRQ settings to be modified. The Optimal and Fail-Safe default setting is *Available*.

IRQ3
IRQ4
IRQ5
IRQ7
IRQ9
IRQ10
IRQ11
IRQ14
IRQ15

Available This setting allows the specified IRQ to be used by a PCI/PnP device. This is the default setting.

Reserved This setting allows the specified IRQ to be used by a legacy ISA device.

DMA

Set this value to allow the DMA setting to be modified. The optimal and Fail-Safe default setting is *Available.*

DMA Channel 0
DMA Channel 1
DMA Channel 3
DMA Channel 5
DMA Channel 6
DMA Channel 7

Available This setting allows the specified DMA to be used by PCI/PnP device. This is the default setting.

Reserved This setting allows the specified DMA to be used by a legacy ISA device.

Reserved Memory Size

Set this value to allow the system to reserve memory that is used by ISA devices. The optimal and Fail-Safe default setting is *Disabled.*

Disabled Set this value to prevent BIOS from reserving memory to ISA devices.

16K Set this value to allow the system to reserve 16K of the system memory to the ISA devices.

32K Set this value to allow the system to reserve 32K of the system memory to the ISA devices.

64K Set this value to allow the system to reserve 64K of the system memory to the ISA devices.

Reserved Memory Address

Set this value to the base address of memory block to reserve for legacy ISA devices. The optimal and Fail-Safe default setting is *C8000.*

C0000
C4000
C8000
CC000
D0000
D4000
D8000
DC000

PCI Slot-1 IRQ Preference

Set this value to the preferred IRQ to be used by a device plugged in the PCI Slot-1. The optimal and fail-safe default is *Auto*.

Auto
3

4
5
6
7
9
10
11
12
14
15

PCI Slot-2 IRQ Preference
Set this value to the preferred IRQ to be used by a device plugged in the PCI Slot-2. The optimal and fail-safe default is *Auto*.

Auto
3
4
5
6
7
9
10
11
12
14
15

PCI Slot-3 IRQ Preference
Set this value to the preferred IRQ to be used by a device plugged in the PCI Slot-3. The optimal and fail-safe default is *Auto*.

Auto
3
4
5
6
7
9
10
11
12
14
15

Note: Manual IRQ selection does not guarantee that the PCI slot device will be configured with the choice because PnP ISA cards (if present) are assigned the available resources before the PCI devices. The PCI slot INT A signals are connected to PIRQ lines together with internal devices in PCI Bus 0. PCI Bus 0 devices have higher priority

over PCI slot devices; therefore, the internal device must be disabled to allow the manual IRQ selection to take effect.

Boot Setup

Select the *Boot* tab from the ezPORT setup screen to enter the Boot BIOS Setup screen. You can select any of the items in the left frame of the screen, such as Boot Device Priority, to go to the sub menu for that item. You can display an Boot BIOS Setup option by highlighting it using the <Arrow> keys.

BOOT SETTINGS CONFIGURATION SCREEN

Boot Settings Configuration
Use this screen to select options for the Boot Settings Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option.

Quick Boot
The Optimal and Fail-Safe default setting is *Disabled*.

Disabled Set this value to allow the BIOS to perform all POST tests.
Enabled Set this value to allow the BIOS to skip certain POST tests to boot faster.

Quiet Boot
Set this value to allow the boot up screen options to be modified between POST messages or OEM logo. The Optimal and Fail-Safe default setting is *Enabled.*

Disabled Set this value to allow the computer system to display the POST messages.
Enabled Set this value to allow the computer system to display the OEM logo. This is the default setting.

Add-On ROM Display Mode
Set this option to display add-on ROM (read-only memory) messages. The Optimal and Fail-Safe default setting is *Force BIOS*. An example of this is a SCSI BIOS or VGA BIOS.

Force BIOS Set this value to allow the computer system to force a third party BIOS to display during system boot. This is the default setting.
Keep Current Set this value to allow the computer system to display the ezPORT information during system boot.

Boot up Num-Lock

Set this value to allow the Number Lock setting to be modified during boot up. The Optimal and Fail-Safe default setting is *Off*.

Off This option does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard will light up when the Number Lock is engaged.

On Set this value to allow the Number Lock on the keyboard to be enabled automatically when the computer system is boot up. This allows the immediate use of 10-keys numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard will be lit.

PS/2 Mouse Support

Set this value to allow the PS/2 mouse support to be adjusted. The Optimal and Fail-Safe default setting is *Enabled*.

Disabled This option will prevent the PS/2 mouse port from using system resources and will prevent the port from being active. Use this setting if installing a serial mouse.

Enabled Set this value to allow the system to use a PS/2 mouse. This is the default setting.

Wait for 'F1' If Error

Set this value to allow the Wait for 'F1' Error setting to be modified. The Optimal and Fail-Safe default setting is *Enabled*.

Disabled This prevents the ezPORT to wait on an error for user intervention. This setting should be used if there is a known reason for a BIOS error to appear. An example would be a system administrator must remote boot the system. The computer system does not have a keyboard currently attached. If this setting is set, the system will continue to boot up in to the operating system. If 'F1' is enabled, the system will wait until the BIOS setup is entered.

Enabled Set this value to allow the system BIOS to wait for any error. If an error is detected, pressing <F1> will enter Setup and the BIOS setting can be adjusted to fix the problem. This normally happens when upgrading the hardware and not setting the BIOS to recognize it. This is the default setting.

Hit 'DEL' Message Display

Set this value to allow the *Hit "DEL" to enter Setup* Message Display to be modified. The Optimal and Fail-Safe default setting is *Enabled*.

Disabled This prevents the ezPORT to display

```
Hit Del to enter Setup
```

during memory initialization. If Quiet Boot is enabled, the Hit 'DEL' message will not display.

Enabled This allows the ezPORT to display

```
Hit Del to enter Setup
```

during memory initialization. This is the default setting.

Interrupt 19 Capture
Set this value to allow option ROMs such as network controllers to trap BIOS interrupt 19.

Disabled The BIOS prevents option ROMs from trapping interrupt 19.

Enabled The BIOS allows option ROMs to trap interrupt 19.

BOOT DEVICE PRIORITY

Boot Device Priority
Use this screen to specify the order in which the system checks for the device to boot from. To access this screen, select Boot Device Priority on the Boot Setup screen and press <Enter>.

1st Boot Device
2nd Boot Device
3rd Boot Device
Set the boot device options to determine the sequence in which the computer checks which device to boot from. The settings are *Removable Dev., Hard Drive, or ATAPI CDROM.* The Optimal and Fail-Safe settings are:

- 1st boot device – Removable Device
- 2nd boot device – Hard Drive
- 3rd boot device – ATAPI CDROM

To change the boot order, select a boot category type such as Hard disk drives, Removable media, or ATAPI CD ROM devices from the boot menu. For example, if the 1st boot device is set to Hard disk drives, then BIOS will try to boot to hard disk drives first.

Note: When you select a boot category from the boot menu, a list of devices in that category appears. For example, if the system has three hard disk drives connected, then the list will show all three hard disk drives attached.

HARD DISK DRIVES

Hard disk drives
Use this screen to view the hard disk drives in the system. To access this screen, select Hard disk drives on the Boot Setup screen and press <Enter>.

REMOVABLE DEVICES

Removable Devices
Use this screen to view the removable drives attached to the system. To access this screen, select Removable Devices on the Boot Setup screen and press <Enter>.

ATAPI CDROM DRIVES

ATAPI CD-ROM Drives
Use this screen to view the ATAPI CD-ROM drives in the system. To access this screen, select ATAPI CDROM Drives on the Boot Setup screen and press <Enter>.

Security Setup

ezPORT Password Support

Two Levels of Password Protection
ezPORT provides both a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first. The system can be configured so that all users must enter a password every time the system boots or when ezPORT Setup is executed, using either or either the Supervisor password or User password. The Supervisor and User passwords activate two different levels of password security. If you select password support, you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed. Make sure you write it down. If you forget it, you must drain NVRAM and reconfigure.

Remember the Password
Keep a record of the new password when the password is changed. If you forget the password, you must erase the system configuration information in NVRAM. See (Deleting a Password) for information about erasing system configuration information.

Select Security Setup from the ezPORT Setup main BIOS setup menu. All Security Setup options, such as password protection and virus protection, are described in this section. To access the sub menu for the following items, select the item and press <Enter>:

- Change Supervisor Password
- Change User Password

- Clear User Password

Supervisor Password
Indicates whether a supervisor password has been set. If the password has been installed, *Installed* displays. If not, *Not Installed* displays.

User Password
Indicates whether a user password has been set. If the password has been installed, *Installed* displays. If not, *Not Installed* displays.

Change Supervisor Password
Select this option and press <Enter> to access the sub menu. You can use the sub menu to change the supervisor password.

Change User Password
Select this option and press <Enter> to access the sub menu. You can use the sub menu to change the user password.

Clear User Password
Select this option and press <Enter> to access the sub menu. You can use the sub menu to clear the user password.

Boot Sector Virus Protection
This option is near the bottom of the Security Setup screen. The Optimal and Fail-Safe default setting is *Disabled*

Disabled Set this value to prevent the Boot Sector Virus Protection. This is the default setting.

Enabled Select Enabled to enable boot sector protection. ezPORT displays a warning when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive. If enabled, the following appears when a write is attempted to the boot sector. You may have to type N several times to prevent the boot sector write.

Boot Sector Write!
Possible VIRUS: Continue (Y/N)? _

The following appears after any attempt to format any cylinder, head, or sector of any hard disk drive via the BIOS INT 13 Hard disk drive Service:

Format!!!
Possible VIRUS: Continue (Y/N)? _

CHANGE SUPERVISOR PASSWORD

Change Supervisor Password

Select Change Supervisor Password from the Security Setup menu and press <Enter>.

Enter New Password:

appears. Type the password and press <Enter>. The screen does not display the characters entered. Retype the password as prompted and press <Enter>. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after ezPORT completes.

Change User Password

Select Change User Password from the Security Setup menu and press <Enter>.

Enter New Password:

appears. Type the password and press <Enter>. The screen does not display the characters entered. Retype the password as prompted and press <Enter>. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after ezPORT completes.

Clear User Password

Select Clear User Password from the Security Setup menu and press <Enter>.

Clear New Password
[Ok] [Cancel]

appears. Type the password and press <Enter>. The screen does not display the characters entered. Retype the password as prompted and press <Enter>. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after ezPORT completes.

Deleting a Password

If you forget the passwords you set up through ezPORT Setup, the only way you can reset the password is to erase the system configuration information where the passwords are stored. System configuration data is stored in CMOS RAM, a type of memory that consumes very little power. You can drain CMOS RAM power by removing the battery or resetting CMOS information using the CMOS erase jumper.

Chipset Setup

Select the *Chipset* tab from the ezPORT setup screen to enter the Chipset BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. You can display a Chipset BIOS Setup option by highlighting it using the <Arrow> keys. All Chipset BIOS Setup options are described in this section.

NORTH BRIDGE CONFIGURATION

North Bridge Chipset Configuration
You can use this screen to select options for the North Bridge Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option.

DRAM Frequency
Set this value to force a specific DRAM frequency (266 MHz, 333 MHz or 400 MHz) or to allow the setting to be based on the SPD information (Auto). The Optimal and Fail-Safe default setting is *Auto*.

Configure DRAM timing by SPD
Set this value to select how the DRAM timing parameters will be set. The Optimal and Fail-Safe default setting is *Enabled*.

Enabled This setting will enable the SPD information to be used as the source to DRAM timing settings. This is the default setting.
Disabled This setting will allow manual DRAM timing configuration.

DRAM CAS# Latency
DRAM RAS# Precharge
DRAM RAS# to CAS# Delay
DRAM Precharge Delay
DRAM Burst Length

DRAM Integrity Mode
Set this value to select the integrity mode. The Optimal and Fail-Safe default setting is *Disabled*.

Memory Hole
Set this value to select the memory hole. The Optimal and Fail-Safe default setting is *Disabled*.

Primary Graphics Adapter
Set this value to allow the Primary video device to be selected. The Optimal and Fail-Safe default setting is *AGP*.

PCI This setting will force any PCI video card to be the primary video device.
AGP This setting will force any AGP video card to be the primary video device.

Graphics Aperture Size
Set this value to select the size of the AGP aperture
4MB
8MB
16MB
32MB
64MB Default.
128MB
256MB

C.S.A Gigabit Ethernet
Set this value to enable the optional second gigabit Ethernet controller (Intel 82547GI). The Optimal and Fail-Safe default setting is A*uto.*

C000, 16k Shadow
Select the type of cache scheme to be used for this memory range. The optimal and fail-safe default is *disabled*.
Disabled.
Uncached.
Write Protect Cached.
Write Through Cached.
Write Back Cached.

C400, 16k Shadow
Select the type of cache scheme to be used for this memory range. The optimal and fail-safe default is *disabled*.
Disabled.
Uncached.
Write Protect Cached.
Write Through Cached.
Write Back Cached.

C800, 16k Shadow
Select the type of cache scheme to be used for this memory range. The optimal and fail-safe default is *disabled*.
Disabled.
Uncached.
Write Protect Cached.
Write Through Cached.
Write Back Cached.

CC00, 16k Shadow

Select the type of cache scheme to be used for this memory range. The optimal and fail-safe default is *disabled*.

Disabled.
Uncached.
Write Protect Cached.
Write Through Cached.
Write Back Cached.

D000, 16k Shadow

Select the type of cache scheme to be used for this memory range. The optimal and fail-safe default is *disabled*.

Disabled.
Uncached.
Write Protect Cached.
Write Through Cached.
Write Back Cached.

D400, 16k Shadow

Select the type of cache scheme to be used for this memory range. The optimal and fail-safe default is *disabled*.

Disabled.
Uncached.
Write Protect Cached.
Write Through Cached.
Write Back Cached.

D800, 16k Shadow

Select the type of cache scheme to be used for this memory range. The optimal and fail-safe default is *disabled*.

Disabled.
Uncached.
Write Protect Cached.
Write Through Cached.
Write Back Cached.

DC00, 16k Shadow

Select the type of cache scheme to be used for this memory range. The optimal and fail-safe default is *disabled*.

Disabled.
Uncached.
Write Protect Cached.
Write Through Cached.
Write Back Cached.

SOUTH BRIDGE CONFIGURATION

Intel ICH4 South Bridge Configuration

You can use this screen to select options for the South Bridge Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option.

Restore on A/C Power Loss

Set this value to select how the CPU board will recover from an accidental A/C power failure – Mechanical off G3 State.

Power ON This setting will force the CPU board to turn ON as soon as A/C power is reestablished. This is the default setting.

Power OFF This setting will keep the CPU board OFF when A/C power is reestablished. To turn the board ON, the power button must be used.

Last State This setting will put the CPU board back to its state before the accidental power failure. It requires ACPI enabled and an ACPI capable OS. The board must be normally turned OFF through a controlled S5 (soft OFF/Power button) transition if it is not an accidental power failure.

ICH4 Dev 31 Func1, IDE

Set this option to Enable or Disable the on board IDE controller. It must be enabled if any Hard Disk Drive, CDROM or other IDE devices will be connected to the on board IDE connectors.

Enabled This setting will keep the onboard IDE Controller enabled. This is the default setting.

Disabled This setting will turn off the on board IDE controller.

ICH4 Dev 31 Func3, SMBUS

Set this option to Enable or Disable the on board SMBUS controller. The SMBUS controller is used for memory detection and other board management functions.

Enabled This setting will keep the onboard SMBUS Controller enabled. This is the default setting.

Disabled This setting will turn off the on board SMBUS controller.

ICH4 Dev 31 Func5, AC97

Set this option to Enable or Disable the on board Audio AC97 controller. If Audio is enabled, certain OSs will require a driver installation on every boot.

Enabled This setting will keep the onboard Audio Controller enabled. This is the default setting.

Disabled This setting will turn off the on board Audio controller.

ICH4 Dev29 Func0, USB#1

Set this option to Enable or Disable the first on board USB 1.1 controller that controls USB Ports 0 and 1.

Enabled This setting will keep the onboard USB#1 Controller enabled. This is the default setting.

Disabled This setting will turn off the on board USB#1 controller. USB controller #1 can only be disabled if USB controllers #2 and #3 are already disabled.

ICH4 Dev29 Func1, USB#2

Set this option to Enable or Disable the second on board USB 1.1 controller that controls USB Ports 2 and 3.

Enabled This setting will keep the onboard USB#2 Controller enabled. This is the default setting.

Disabled This setting will turn off the on board USB#2 controller. USB controller #2 can only be disabled if USB controller #3 is already disabled.

ICH4 Dev29 Func2, USB#3

Set this option to Enable or Disable the third on board USB 1.1 controller that controls USB Ports 4 and 5.

Enabled This setting will keep the onboard USB#3 Controller enabled. This is the default setting.

Disabled This setting will turn off the on board USB#3 controller.

ICH4 Dev29 Func7, EHC

Set this option to Enable or Disable the on board USB 2.0 controller. If USB 2.0 is enabled, certain OSs will require a driver installation on every boot. The USB 2.0 controller is able to handle all 6 ports on board at the same time. The ports are physically shared with the 3 USB 1.1 controllers.

Enabled This setting will keep the onboard USB 2.0 Controller enabled. The USB 1.1 controllers #1, #2, and #3 must be enabled first.

Disabled This setting will turn off the on board USB 2.0 controller. This is the default setting.

LPC 4E-4F Decode

Set this option to Enable or Disable the decoding of I/O addresses 4eh and 4fh by the LPC bridge.

Enabled This is the default setting.

Disabled

Primary LAN

Set this option to Enable or Disable the on board primary LAN controller. This option does not appear on boards without the optional secondary LAN controller.

Enabled This setting will keep the optional onboard secondary Ethernet Controller enabled. This is the default setting.
Disabled This setting will turn off the optional on board secondary Ethernet controller.

Moon ISA Device
Set this option to Enable or Disable the on board ISA bridge.
Enabled This setting will keep the onboard ISA bridge enabled. When the ISA bridge is enabled, the LPC bridge goes into positive decoding. This is the default setting.
Disabled This setting will turn off the on board ISA bridge. The LPC bridge will be in subtractive decoding.

ISA 8-bit I/O Recovery
Set this value to the number of ISA bus clocks between back-to- back 8 bit I/O read cycles.
1-15 Clocks. This option is only available when the ISA bridge is enabled. The Default is 5 Clks.

ISA 16-bit I/O Recovery
Set this value to the number of ISA bus clocks between back-to- back 16 bit I/O read cycles.
1-15 Clocks. This option is only available when the ISA bridge is enabled. The Default is 4 Clks.

IOAPIC
Set this option to Enable or Disable the IOAPIC. The I/O Advanced Programmable Interrupt Controller allows extra functionality to the traditional 8259 Interrupt controller, including the ability for ACPI OSs to redirect interrupts.
Enabled This is the default setting.
Disabled

Extended IOAPIC
Set this option to Enable or Disable the Extended features of the IOAPIC.
Enabled This is the default setting.
Disabled

CPU B.I.S.T.
Set this option to Enable or Disable the CPU Built In Self Test.
Enabled
Disabled This is the default setting.

ICH4 DMA Collection

Set this option to Enable or Disable the DMA Buffer Collection. The DMA buffer Collection enabled increases the performance of DMA transactions.

Enabled This is the default setting.
Disabled

DMA – 0 Type

Set this value to select the DMA channel 0 to the LPC DMA (legacy devices on the LPC bus) or to the PC/PCI protocol used by ISA devices connected to the ISA bridge. There is no legacy LPC device using channel 0.

LPC DMA This is the default setting.
PC/PCI Used by ISA devices.

DMA – 1 Type

Set this value to select the DMA channel 1 to the LPC DMA (legacy devices on the LPC bus) or to the PC/PCI protocol used by ISA devices connected to the ISA bridge. There is no legacy LPC device using channel 1.

LPC DMA This is the default setting.
PC/PCI Used by ISA devices.

DMA – 2 Type

Set this value to select the DMA channel 2 to the LPC DMA (legacy devices on the LPC bus) or to the PC/PCI protocol used by ISA devices connected to the ISA bridge. **ATTENTION**: The floppy controller uses channel 2. Leave it to LPC DMA if FDD enabled.

LPC DMA This is the default setting.
PC/PCI Used by ISA devices.

DMA – 3 Type

Set this value to select the DMA channel 3 to the LPC DMA (legacy devices on the LPC bus) or to the PC/PCI protocol used by ISA devices connected to the ISA bridge. There is no legacy LPC device using channel 3.

LPC DMA This is the default setting.
PC/PCI Used by ISA devices.

DMA – 5 Type

Set this value to select the DMA channel 5 to the LPC DMA (legacy devices on the LPC bus) or to the PC/PCI protocol used by ISA devices connected to the ISA bridge. There is no legacy LPC device using channel 5.

LPC DMA This is the default setting.

PC/PCI Used by ISA devices.

DMA – 6 Type

Set this value to select the DMA channel 6 to the LPC DMA (legacy devices on the LPC bus) or to the PC/PCI protocol used by ISA devices connected to the ISA bridge. There is no legacy LPC device using channel 6.

LPC DMA This is the default setting.
PC/PCI Used by ISA devices.

DMA – 7 Type

Set this value to select the DMA channel 7 to the LPC DMA (legacy devices on the LPC bus) or to the PC/PCI protocol used by ISA devices connected to the ISA bridge. There is no legacy LPC device using channel 7.

LPC DMA This is the default setting.
PC/PCI Used by ISA devices.

Exit Menu

Select the *Exit* tab from the ezPORT setup screen to enter the Exit BIOS Setup screen. You can display an Exit BIOS Setup option by highlighting it using the <Arrow> keys. All Exit BIOS Setup options are described in this section.

Exit Saving Changes

When you have completed the system configuration changes, select this option to leave ezPORT Setup and reboot the computer so the new system configuration parameters can take effect. Select Exit Saving Changes from the Exit menu and press <Enter>.

Save Configuration Changes and Exit Now?
[Ok] [Cancel]

appears in the window. Select Ok to save changes and exit.

Exit Discarding Changes

Select this option to quit ezPORT Setup without making any permanent changes to the system configuration. Select Exit Discarding Changes from the Exit menu and press <Enter>.

Discard Changes and Exit Setup Now?
[Ok] [Cancel]

appears in the window. Select *Ok* to discard changes and exit.

Load Optimal Defaults

ezPORT automatically sets all ezPORT Setup options to a complete set of default settings when you Select this option. The Optimal settings are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Optimal

ezPORT Setup options if your computer is experiencing system configuration problems.
Select Load Optimal Defaults from the Exit menu and press <Enter>.
Select *Ok* to load optimal defaults.

Load Fail-Safe Defaults
ezPORT automatically sets all ezPORT Setup options to a complete set of default settings when you Select this option. The Fail-Safe settings are designed for maximum system stability, but not maximum performance. Select the Fail-Safe ezPORT Setup options if your computer is experiencing system configuration problems. Select Load Fail-Safe Defaults from the Exit menu and press <Enter>.

Load Fail-Safe Defaults?
[Ok] [Cancel]

appears in the window. Select *Ok* to load Fail-Safe defaults.

Discard Changes
Select Discard Changes from the Exit menu and press <Enter>.
Select *Ok* to discard changes.

User's Notes:

User's Notes:

Chapter 3 Upgrading

Upgrading the Microprocessor

The latest revision of the Phoenix AT currently supports full series of Intel Pentium IV (mPGA478 400MHz, 533MHz and 800MHz PSB) processors featuring Intel Hyper-Threading technology. Please, check the manufacturer's web site for details and revisions regarding CPU speed.
Since the Phoenix AT features CPU auto-sensing device there is no jumper to be set when changing the CPU.

Upgrading the System Memory

The Phoenix AT allows an upgrade of the system memory with up to 4GB SDRAM DDR DIMM modules in four memory slots with the following features:

System Memory Features:

- 2.6 V (only) 184-pin DDR SDRAM DIMMs with gold-plated contacts.
- Unbuffered, single-sided or double-sided DIMMs with the following restriction:
  - Double-sided DIMMs with x16 organization are not supported.
- Maximum total system memory: 4 GB; minimum total system memory: 64 MB .
- DDR266 MHz (PC2100), DDR333 MHz (PC2700) and DDR400 MHz (PC3200) DDR SDRAM DIMMs only.
- Serial Presence Detect (SPD).
- ECC and non-ECC DIMMs supported.

Supported System Bus Frequency and Memory Speed Combinations

To use this type of DIMM…	The processor's system bus frequency must be…
DDR400	800 MHz
DDR333	800 or 533 MHz (Note)
DDR266	800, 533 or 400 MHz

Note: When using an 800 MHz system bus frequency processor, DDR333 memory is clocked at 320 MHz. This minimizes system latencies to optimize system throughput.

Addressable Memory

The Phoenix AT utilizes 4 GB of addressable system memory. Typically the address space that is allocated for PCI add-in cards, AGP aperture, BIOS (firmware hub), and chipset overhead resides above the top of DRAM (total system memory). On a system that has 4 GB of system memory installed, it is not possible to use all of the installed memory due to system address space being allocated for other system critical functions. These functions include the following:

- Memory-mapped I/O that is dynamically allocated for PCI and AGP cards.
- AGP aperture.
- APIC and chipset overhead (approximately 18 MB).
- BIOS/firmware hub (approximately 2 MB).

The amount of installed memory that can be used will vary based on add-in cards and BIOS settings. For example, if the PCI cards are requesting 200 MB of system memory and the AGP aperture is set to 256 MB in the BIOS Setup program, there will be approximately 3.54 GB of memory that can be accessed. All installed system memory can be used when there is no overlap of system addresses. For example, all of the system address space can be utilized on a system that has 2 GB of installed system memory, AGP aperture set for 256 MB, and the PCI cards are requesting 200 MB of system address space.

NOTES

• When ECC DIMMs are used, the Power-On Self Test (POST) will take longer to complete.

• To be fully compliant with all applicable DDR SDRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance.

The following table lists the supported DDR DIMM Configurations:

Table 3-1 Supported DDR DIMM Configurations

DIMM Capacity	# of Dev./ DIMM	# of Sides	DRAM Tech.	Front Side Population		Back Side Population	
				Count	Config	Count	Config
64 MB	8	SS	64 Mbit	8	8 M x 8		
64 MB	4	SS	128 Mbit	4	8 M x 16		
128 MB	16	DS	64 Mbit	8	8 M x 8	8	8 M x 8
128 MB	8	SS	128 Mbit	8	16 M x 8		
128 MB	4	SS	256 Mbit	4	16 M x 16		
256 MB	16	DS	128 Mbit	8	16 M x 8	8	16 M x 8
256 MB	8	SS	256 Mbit	8	32 M x 8		
256 MB	4	SS	512 Mbit	4	32 M x 16		
512 MB	16	DS	256 Mbit	8	32 M x 8	8	32 M x 8
512 MB	8	SS	512 Mbit	8	64 M x 8		
1024 MB	16	DS	512 Mbit	8	64 M x 8	8	64 M x 8

Memory Configurations

The Phoenix AT 875P MCH component provides two features for enhancing memory throughput:

- Dual Channel memory interface. The board has two memory channels, each with two DIMM sockets, as shown in *Figure 3-1*.
- Dynamic Addressing Mode. Dynamic mode minimizes overhead by reducing memory accesses.

Table 3-2 summarizes the characteristics of Dual and Single Channel configurations with and without the use of Dynamic Mode.

Figure 3-1 Memory Channel Configuration

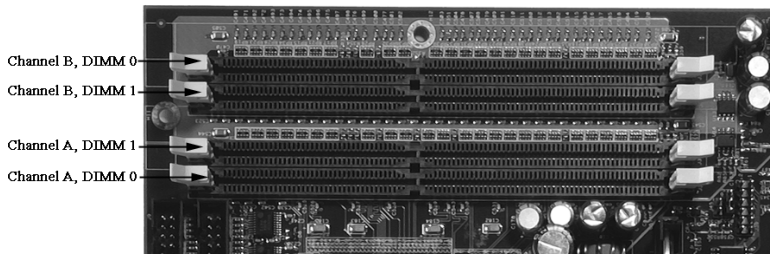


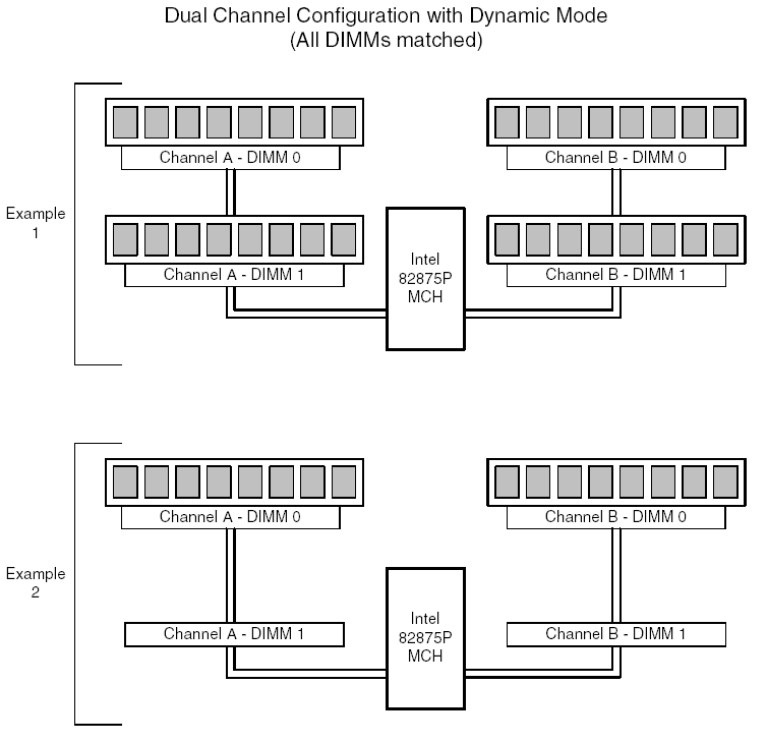
Table 3-2 Characteristics of Dual and Single Channel Configuration with and without Dynamic Mode

Throughput Level	Configuration	Characteristics
Highest	Dual Channel with Dynamic Mode	All DIMMs matched (Example configurations are shown in *Figure 3-2*)
	Dual Channel without Dynamic Mode	• DIMMs matched from Channel A to Channel B • DIMMs not matched within channels (Example configuration is shown in *Figure 3-3*)
	Single Channel with Dynamic Mode	Single DIMM or DIMMs matched within a channel (Example configurations are shown in *Figure 3-4*)
Lowest	Single Channel without Dynamic Mode	DIMMs not matched (Example configurations are shown in *Figure 3-5*)

If either only channel A or only channel B is populated then the MCH is set to operate in single-channel mode. Data will be accessed in chunks of 64 bits (8 B) from the memory channels. If both the channels are populated with uneven memory (DIMMs), then the MCH defaults to virtual single-channel mode. The MCH behaves identically in both single-channel and virtual single-channel modes. In dual-channel mode of operation the data accessed by the MCH from the memory will be in chunks of 128 bits (16 B) from both the channels, hence the bandwidth in this case will be double that of in SC mode.

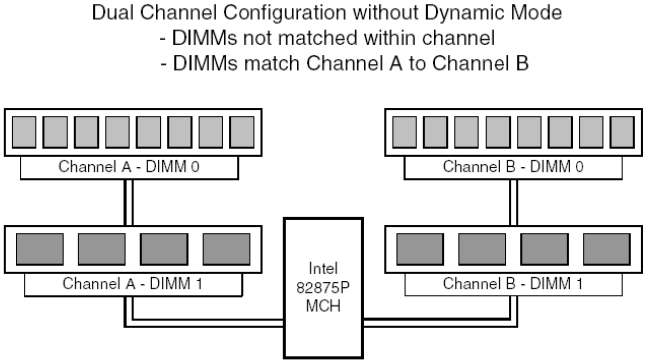
When the MCH is configured to operate in Dynamic Paging mode, Front-Side Bus (FSB) to Memory Bus address mapping undergoes a significant change compared to that of in a linear operating mode (normal operating mode). In non-dynamic paging mode, the Rank selection (Rank or ROW indicates the side of a DIMM) via chip select signals, is done based on the size of the ROW. For example, for a 512-Mb 16MX8X4b will have a ROW size of 512 MB, selected by CS0#, and only four open pages can be maintained for the full 512 MB. This will lower the memory performance (increases READ latencies) if most of the memory cycles are targeted to that single ROW resulting in opening and closing of accessed pages in that ROW. In this example, the memory configuration was DS DIMM, hence FSB address bit A[19] will be used for Rank selection between Rank 0 and 1. By doing this the Rank switching was done for every 512 KB, which under non-dynamic mode used to be for 128 MB. The advantage lies in having eight open pages (four per Rank) for every 512 KB, compared to that of having four open pages for 128 MB.

Figure 3-2 Examples of Dual Channel Configuration with Dynamic Mode



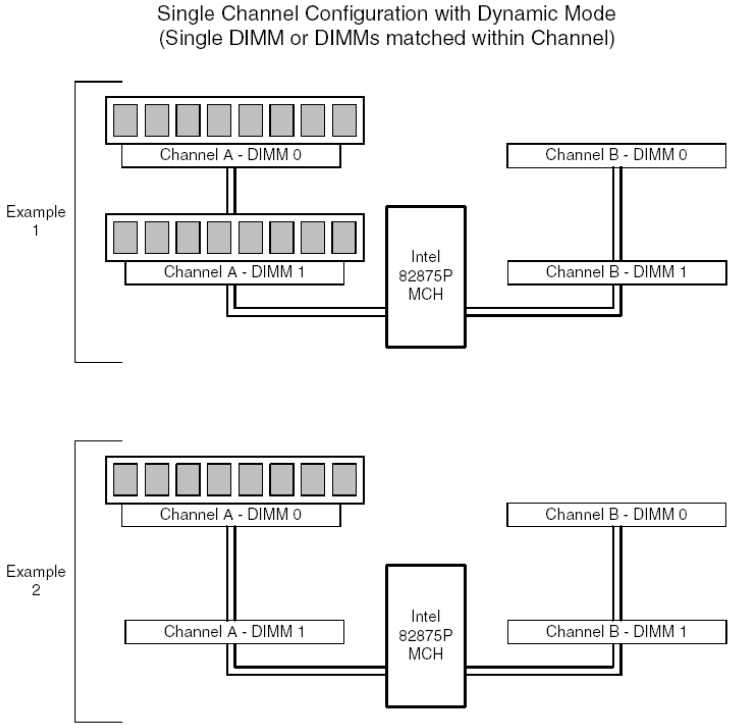
Throughput Level	Configuration	Characteristics
Highest	Dual Channel with Dynamic Mode	All DIMMs matched
↑	Dual Channel without Dynamic Mode	• DIMMs matched from Channel A to Channel B • DIMMs not matched within channels
	Single Channel with Dynamic Mode	Single DIMM or DIMMs matched within a channel
Lowest	Single Channel without Dynamic Mode	DIMMs not matched

Figure 3-3 Examples of Dual Channel Configuration without Dynamic Mode



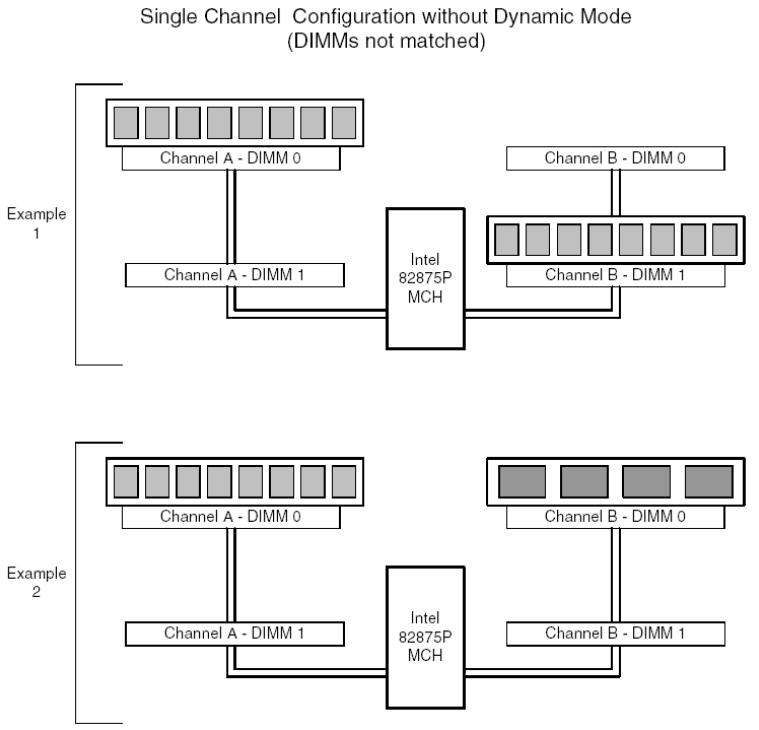
Throughput Level	Configuration	Characteristics
Highest	Dual Channel with Dynamic Mode	All DIMMs matched
↑	Dual Channel without Dynamic Mode	• DIMMs matched from Channel A to Channel B • DIMMs not matched within channels
	Single Channel with Dynamic Mode	Single DIMM or DIMMs matched within a channel
Lowest	Single Channel without Dynamic Mode	DIMMs not matched

Figure 3-4 Examples of Single Channel Configuration with Dynamic Mode



Throughput Level	Configuration	Characteristics
Highest	Dual Channel with Dynamic Mode	All DIMMs matched
↑	Dual Channel without Dynamic Mode	• DIMMs matched from Channel A to Channel B • DIMMs not matched within channels
	Single Channel with Dynamic Mode	Single DIMM or DIMMs matched within a channel
Lowest	Single Channel without Dynamic Mode	DIMMs not matched

Figure 3-5 Examples of Single Channel Configuration without Dynamic Mode



Throughput Level	Configuration	Characteristics
Highest	Dual Channel with Dynamic Mode	All DIMMs matched
	Dual Channel without Dynamic Mode	• DIMMs matched from Channel A to Channel B • DIMMs not matched within channels
	Single Channel with Dynamic Mode	Single DIMM or DIMMs matched within a channel
Lowest	Single Channel without Dynamic Mode	DIMMs not matched

Appendix A Technical Specifications

Chipsets

Core Logic

North Bridge - Intel 875P.

South Bridge – Intel ICH4.

ISA Bridge – National PC87200.

Peripheral I/O

Standard Microsystems (SMSC) LPC47M192.

BIOS

System BIOS

American Megatrends AMIBIOS8.

Flash BIOS

Standard feature for System BIOS. Flash programming built into the BIOS. BIOS to be flashed is read from a floppy.

Embedded I/O

Floppy

2 Floppies up to 2.88 MB.

IDE

The board provides up to seven IDE interface connectors:

- Two Parallel ATA IDE connectors, which support a total of four devices (two per connector) and one extra connector (mini-Header 44 pin) in parallel to IDE2 for Solid State IDE disk or any 44 pin IDE device support.
- Two/Four Serial ATA IDE connectors (optional), which support one device per connector.

Parallel ATA IDE Interfaces

The ICH4 Parallel ATA IDE controller has two independent bus-mastering Parallel ATA IDE interfaces that can be independently enabled. The Parallel ATA IDE interfaces support the following modes:

- Programmed I/O (PIO): processor controls data transfer.
- 8237-style DMA: DMA offloads the processor, supporting transfer rates of up to 16 MB/sec.
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec.
- ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to Ultra DMA and is device driver compatible.
- ATA-100: DMA protocol on IDE bus allows host and target throttling. The ICH ATA-100 logic can achieve read transfer rates up to 100 MB/sec and write transfer rates up to 88 MB/sec.

NOTE

ATA-66 and ATA-100 are faster timings and require a specialized cable (80-conductor) to reduce reflections, noise, and inductive coupling.

The Parallel ATA IDE interfaces also support ATAPI devices (such as CD-ROM drives).

The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS. The Phoenix AT supports Laser Servo (LS-120) diskette technology through the Parallel ATA IDE interfaces. The BIOS supports booting from an LS-120 drive.

NOTE

The BIOS will always recognize an LS-120 drive as an ATAPI floppy drive. To ensure correct operation, do not configure the drive as a hard disk drive.

Serial ATA Interfaces (optional)

The Phoenix AT may optionally feature two (Sil 3512) or four (Sil 3114) independent Serial ATA ports with a theoretical maximum transfer rate of 150 MB/s per port. One device can be installed on each port for a maximum of two Serial ATA devices. A point-to-point interface is used for host to device

connections, unlike Parallel IDE, which supports a master/slave configuration and two devices per channel.
For compatibility, the underlying Serial ATA functionality is transparent to the operating system.
NOTE
Many Serial ATA drives use new low-voltage power connectors and require adaptors or power supplies equipped with low-voltage power connectors.

Serial Ports

Three high speed RS-232 serial ports 16 Bytes FIFO (16550/16550D). Com B optional RS-232 IrDA. Com C optional RS-422/485.

Parallel Port

One Centronics™ compatible bi-directional parallel port. EPP/ECP mode compatible.

Keyboard/Mouse Port

One AT style keyboard connector.

Auxiliary Keyboard/Mouse header for front panel access.

USB Interfaces

Six Universal Serial Bus connectors. USB 1.1 and USB 2.0 compliant.

On-board Ethernet

Two RJ45 Ethernet connectors (second 10/100/1000 optional, first optional 10/100/1000).

On-board Buzzer

Audio

Audio (AD1981B) AC97 compliant. Microphone In, Stereo Line In and Out, Auxiliary CD/Audio In.

AGP

The AGP PRO connector supports the following:

- 4x, 8x AGP 3.0 add-in cards with 0.8 V I/O.
- 1x, 4x AGP 2.0 add-in cards with 1.5 V I/O.
- AGP PRO add-in cards with the above characteristics.

AGP is a high-performance interface for graphics-intensive applications, such as 3D applications. While based on the *PCI Local Bus Specification*, Rev. 2.2, AGP is independent of the PCI bus and is intended for exclusive use with graphical display devices. AGP overcomes certain limitations of the PCI bus related to handling large amounts of graphics data with the following features:

- Pipelined memory read and write operations that hide memory access latency.
- Demultiplexing of address and data on the bus for nearly 100 percent efficiency.

NOTES

- *AGP 2x operation is not supported.*
- *The AGP connector is keyed for Universal 0.8 V AGP 3.0 cards or 1.5 V AGP 2.0 cards only.*
- *Do not attempt to install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards.*

Industrial Devices

Temperature and Voltage Device

Automatic CPU voltage & temperature monitoring device (optional).

Power Management

Power button function: advanced power management support.

General Purpose I/O lines

Ten general purpose I/O lines in a header (optional).

On-Board POST Display Diagnostics

Miscellaneous

CMOS/Battery

RTC with lithium battery.

Control Panel Connections

Reset, Soft Power, Speaker. LEDs for power and IDE.

CPU Socket

Standard ZIF (Zero Insertion Force), mPGA 478.

Form Factor

Baby AT form factor (8.6" x 13").

PCB Construction

Six Layers, dry film mask.

Manufacturing Process

Automated surface mount.

Table A-1 Environmental

Environmental	Operating	Non-operating
Temperature	0° to +55° C	-40° to +65° C
Humidity	5 to 95% @ 40° C non-condensing	5 to 95% @ 40° C non-condensing
Shock	2.5G @ 10ms	10G @ 10ms
Vibration	0.25 @ 5-100Hz	5 @ 5-100Hz

Memory Map

Address Range Decimal	Address Range Hexadecimal	Size	Description
960K-1M	0F0000-0FFFFF	64 KB	Upper BIOS
896K-960K	0E0000-0EFFFF	64 KB	Lower BIOS
768K-896K	0C0000-0DFFFF	128 KB	Expansion Card BIOS and Buffer
640K-768K	0A0000-0BFFFF	128 KB	Standard PCI/ISA Video Memory
633K-640K	09E400-09FFFF	7KB	BIOS Reserved
512K-633K	080000-09E3FF	121 KB	Ext. Conventional memory
0K- 512K	000000-07FFFF	512 KB	Conventional memory

DMA Channels

DMA #	Data Width	System Resource
0	8- or 16-bits	Open
1	8- or 16-bits	Parallel port (for ECP) (if selected)
2	8- or 16-bits	Floppy Drive
3	8- or 16-bits	Parallel port (for ECP) (if selected)
4	Reserved-	cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

I/O Map

Address (hex)	Description
0000-000F	DMA 1
0020-0021	Interrupt Controller 1
0040	Timer/Counter 0
0041	Timer/Counter 1
0042	Timer/Counter 2
0043	Timer Control Word
0060	Keyboard Controller Byte _ Reset IRQ
0061	NMI Status and Control
0070, bit 7	NMI enable
0070, bits 6:0	RTC Index
0071	RTC Data
0072	RTC Extended Index
0073	RTC Extended Data
0080-008F	DMA page registers / POST code display also located at 0080h
0092	Port 92
00A0-00A1	Interrupt Controller 2
00B2-00B3	APM control
00C0-00DE	DMA 2
00F0	Coprocessor Error
0170 _ 0177	Secondary IDE channel
01F0 _ 01F7	Primary IDE channel
0278-027F	LPT2 (if selected)
02E8-02EF	COM4 (default) (if selected)
02F8-02FF	COM2 (default)
0376	Secondary IDE channel command port
0377	Floppy channel 2 command
0377, bit 7	Floppy disk change, channel 2
0377, bits 6:0	Secondary IDE channel status port
0378-037F	LPT1 (default)
03B4-03B5	Video (VGA)
03BA	Video (VGA)
03BC-03CD	LPT3 (if selected)
03C0-03CA	Video (VGA)
03CC	Video (VGA)
03CE-03CF	Video (VGA)
03D4-03D5	Video (VGA)
03DA	Video (VGA)

Address (hex)	Description
03E8-03EF	COM3 (default)
03F0-03F5	Floppy Channel 1
03F6	Primary IDE channel command port
03F7	Floppy Channel 1 command
03F7, bit 7	Floppy disk change channel 1
03F7, bits 6:0	Primary IDE channel status report
03F8-03FF	COM1 (default)
0CF8-0CFB - 4 bytes	PCI configuration address register
0CF9	Reset control register
0CFC-0CFF - 4 bytes	PCI configuration data register

PCI Configuration Space Map

Bus #	Device #	Function #	Description
00	00 and 06	00	875P Memory Controller
00	01	00	875P Host to AGP Bridge
00	03	00	PCI to CSA Bridge
00	1D	00	ICH4 USB UHC 1
00	1D	01	ICH4 USB UHC 2
00	1D	02	ICH4 USB UHC 3
00	1D	07	ICH4 USB EHC
00	1E	00	Hub Interface to PCI Bridge
00	1F	00	ICH4 LPC Bridge
00	1F	01	ICH4 Master IDE Controller
00	1F	03	ICH4 SMBus Controller
00	1F	05	ICH4 AC97 Audio Controller
01	00	00	AGP Card
02	01	00	Intel 82547GI LAN (optional)
03	00	00	PCI expansion slot 1
03	01	00	PCI expansion slot 2
03	02	00	PCI expansion slot 3
03	03	00	LAN1 Controller
03	04	00	Serial ATA Controller (optional)
03	06	00	NSC PCI to ISA Bridge

Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved (keyboard)
2	Reserved (cascade)
3	COM2*
4	COM1*
5	COM3*
6	Floppy Drive
7	LPT1*
8	Real time clock
9	User Available for PCI
10	User Available for PCI
11	User Available for PCI
12	PS/2 mouse port
13	Reserved (math coprocessor)
14	Primary IDE
15	Secondary IDE

**Default, but can be changed to another IRQ*

SMBUS

Device	Slave Address
SIO	00101101b
DIMM0 Channel A	01010000b
DIMM1 Channel A	01010001b
DIMM0 Channel B	01010010b
DIMM1 Channel B	01010011b
Clock Chip Write	11010010b
Clock Chip Read	11010011b

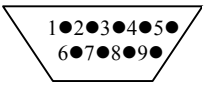
PCI Interrupt Routing Map

PCI Device	ID SEL	PIRQA	PIRQB	PIRQC	PIRQD	PIRQE	PIRQF	PIRQG	PIRQH
PCI Slot 1	AD16			INTA	INTB	INTC	INTD		
PCI Slot 2	AD17			INTB	INTC	INTD	INTA		
PCI Slot 3	AD18			INTC	INTD	INTA	INTB		
Ethernet 1	AD19								INTA
SATA	AD20							INTA	
IDE				INTA					
Audio			INTA						
ISA Br.	AD22								
USB 1		INTA							
USB 2					INTA				
USB 3				INTA					
USB 2.0									INTA
SMBus			INTA						
AGP		INTA	INTB						
CSA				INTA					

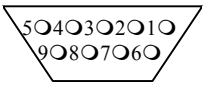
Connectors Pin-out

How to identify pin number 1: Looking to the solder side (The board side without components) of the PCB (Printed Circuit Board), pin number 1 will have a squared pad ■. Other pins will have a circular pad ●.

How to identify other pins: Connectors type DB, PS/2, RJ45, Power ATX and USB are industry standards. DB connectors, for instance, are numbered sequentially. The first row is numbered in sequence (be aware that male and female connectors are mirrored – male connectors are numbered from left to right when viewed from front and female connectors are numbered from right to left when viewed from front). The following rows resume the counting on the same side of pin number 1. The counting is NOT circular like Integrated Circuits (legacy from electronic tubes).

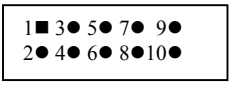


DB9 Male
Front view



DB9 Female
Front view

Header connectors are numbered alternately, i.e. pin number 2 is in the other row, but in the same column of pin number 1. Pin number 3 is in the same row of pin 1, but in the next column and so forth.



Header 10 pin connector
View from solder side of the PCB

Table A-9 J28 USB Ports 0 & 1 Header Connector

Pin#	USB Header – J28
1	+5V – USB0
2	+5V – USB1
3	-D – USB0
4	-D – USB1
5	+D – USB0
6	+D – USB1
7	GROUND – USB0
8	GROUND – USB1

Table A-10 J29 USB Ports 2 & 3 Header Connector

Pin#	USB Header – J29
1	+5V – USB2
2	+5V – USB3
3	-D – USB2
4	-D – USB3
5	+D – USB2
6	+D – USB3
7	GROUND – USB2
8	GROUND – USB3

Table A-11 J30 USB Ports 4 & 5 Header Connector

Pin#	USB Header – J30
1	+5V – USB4
2	+5V – USB5
3	-D – USB4
4	-D – USB5
5	+D – USB4
6	+D – USB5
7	GROUND – USB4
8	GROUND – USB5

Table A-12 J9 Serial Port COMA Header Connector

Pin#	Serial Port Header – J9
1	DCD
2	DSR
3	RX
4	RTS
5	TX
6	CTS
7	DTR
8	RI
9	GND
10	KEY

Table A-13 J10 Serial Port COMB Header Connector

Pin#	Serial Port Header – J10
1	DCD
2	DSR
3	RX
4	RTS
5	TX
6	CTS
7	DTR
8	RI
9	GND
10	KEY

Table A-14 J8 Serial Port COMC Header Connector

Pin#	Serial Port Header – J8
1	DCD - RS-422/485RXB(opt.)
2	DSR
3	RX - RS-422/485TXB(opt.)
4	RTS
5	TX - RS-422/485TXA(opt.)
6	CTS
7	DTR
8	RI – RS-422/485RXA(opt.)
9	GND
10	Key

Table A-15 J26 Ethernet 1 10/100 Header

Pin#	Ethernet Header – J26
1	Termination
2	Termination
3	RX+
4	RX-
5	LED_SPEED
6	330Ω to 3.3VDC
7	LED_LINK
8	LED_ACT
9	TX+
10	TX-

Table A-16 J25 Ethernet 1 10/100/1000 (optional) Header

Pin#	Ethernet Header – J25
1	TX1+
2	RX0-
3	TX1-
4	RX0-
5	RX1+
6	TX0-
7	RX1-
8	TX0+
9	GND
10	GND
11	LED_ACT
12	LED_LINK
13	LED_SPEED 1G
14	LED_SPEED 100M

Table A-17 J21 Ethernet 2 10/100/1000 (optional) Header

Pin#	Ethernet Header – J21
1	TX1+
2	RX0-
3	TX1-
4	RX0-
5	RX1+
6	TX0-
7	RX1-
8	TX0+
9	GND
10	GND
11	LED_ACT
12	LED_LINK
13	LED_SPEED 1G
14	LED_SPEED 100M

Table A-18 J14 Keyboard/Mouse Header Connector

Pin#	Keyboard/Mouse Header – J14
1	Mouse CLK
2	Keyboard CLK
3	HDD LED
4	Keyboard Data
5	VCC
6	VCC
7	GND
8	Mouse Data
9	GND
10	Key

Table A-19 J6 Front Panel Header Connector

Pin#	Front Panel Header – J6
1	HDD LED Anode
2	Power LED Green Blink
3	HDD LED Cathode
4	Power LED Yellow Blink
5	Reset - GND
6	Power Switch
7	Reset
8	Power Switch - GND
9	+5V
10	NC
11	Infra Red Rx (Opt.)
12	GND
13	GND
14	Power LED Cathode - GND
15	Infra Red Tx (Opt.)
16	Power LED Anode

Table A-20 J11 Parallel Header Connector

Pin#	Parallel Header – J11
1	-STROBE
2	AUTOFEED
3	+DATA BIT 0
4	ERROR
5	+DATA BIT 1
6	INIT
7	+DATA BIT 2
8	SLCT IN
9	+DATA BIT 3
10	GND
11	+DATA BIT 4
12	GND
13	+DATA BIT 5
14	GND
15	+DATA BIT 6
16	GND
17	+DATA BIT 7
18	GND
19	ACK1
20	GND
21	BUSY
22	GND
23	PAPER EMPTY
24	GND
25	SLCT
26	NC

Table A-21 J39 GPIO (optional) Header Connector

Pin#	GPIO Header – J39
1	GPIO24
2	GPIO25
3	GPIO27
4	GPIO37
5	GPIO38
6	GND
7	GPIO39
8	GPIO40
9	GPIO41
10	GPIO42
11	GPIO43
12	GND

Table A-22 CPU Fan, Rear Chassis Fan, Intruder, Speaker, CD IN, AUX IN and LINE IN.

Connector	Description			
J4	**CPU FAN**			
	1) Sense	2)+12V	3) GND (PWM)	
J5	**Rear Chassis FAN**			
	1)Sense	2)+12V	3) GND (PWM)	
J45	**Intruder**			
	1)Sense		2) GND	
J7	**Speaker (Alternate)**			
	1)VCC		2) GND (PWM)	
J18	**AUX IN**			
	1)Left	2)GND	3)GND	4)Right
J19	**CD IN**			
	1)Left	2)GND	3)GND	4)Right
J20	**LINE IN**			
	1)Left	2)GND	3)GND	4)Right

Table A-23 J17 Microphone IN, Line OUT/Headphone Header Connector

Pin#	Audio Header – J17
1	MIC IN
2	GND
3	MIC BIAS
4	+5VDC
5	Line OUT/Headphone Right
6	NC
7	NC
8	NC
9	Line OUT/Headphone Left
10	Line OUT sense

Appendix B Flash BIOS programming and codes

The Phoenix AT offers the standard FLASH BIOS. When installed, you will be able to update your BIOS without having to replace the EEPROM. The AMIBIOS8 will read the new BIOS file from a floppy disk during boot and replace the old BIOS.

When updating your BIOS, make sure you have a disk with the correct BIOS file (its size should be 4Mb (512kB)) named AMIBOOT.ROM.

How to reflash the BIOS:

- Insert a floppy containing AMIBOOT.ROM into floppy A:
- Press [ctrl][home] during the beginning of POST(boot).
- Wait for the procedure to finish and reboot.

Please never turn the power off while reprogramming a FLASH BIOS.

Troubleshooting POST

AMIBIOS8 writes progress codes, also known as POST codes, to I/O port 80h during POST, in order to provide information to OEM developers about system faults. These POST codes may be monitored by the On-board POST Display.

Table B-1 Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS.

Checkpoint Code	Description
Before D1	Early chipset initialization is done. Early super I/O initialization is done including RTC and keyboard controller. NMI is disabled.
D1	Perform keyboard controller BAT test. Check if waking up from power management suspend state. Save power-on CPUID value in scratch CMOS.
D0	Go to flat mode with 4GB limit and GA20 enabled. Verify the bootblock checksum.
D2	Disable CACHE before memory detection. Execute full memory sizing module. Verify that flat mode is enabled.
D3	If memory sizing module not executed, start memory refresh and do memory sizing in Bootblock code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. Main BIOS checksum is tested. If BIOS recovery is necessary, control flows to checkpoint E0. See *Bootblock Recovery Code Checkpoints* section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See *POST Code Checkpoints* section of document for more information.
E1-E8 EC-EE	OEM memory detection/configuration error. This range is reserved for chipset vendors & system manufacturers.

Table B-2 Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS:

Checkpoint Code	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.

Table B-3 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Checkpoint Code	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
C0	Early CPU Init Start -- Disable Cache - Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor
C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
24	Uncompress and initialize any platform specific BIOS

	modules.
30	Initialize System Management Interrupt.
2A	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, … etc.) successfully installed in the system and update the BDA, EBDA…etc.
50	Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7A	Initializes remaining option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.

85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disable NMI as selected
90	Late POST initialization of system management interrupt.
A0	Check boot password if installed.
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A8	Prepare CPU for OS boot including final MTRR values.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector. Deinitializes the ADM module.
AB	Prepare BBS for Int 19 boot.
AC	End of POST initialization of chipset registers.
B1	Save system context for ACPI.
00	Passes control to OS Loader (typically INT19h).
61-70	OEM POST Error.

Table B-4 DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST to initialize different system busses. The following table describes the main checkpoints where the DIM module is accessed:

Checkpoint Code	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function 1); Boot Output Device

	Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

While control is in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:

HIGH BYTE XY

The upper nibble 'X' indicates the function number that is being executed. 'X' can be from 0 to 7.

0 = func#0, disable all devices on the BUS concerned.
1 = func#1, static devices initialization on the BUS concerned.
2 = func#2, output device initialization on the BUS concerned.
3 = func#3, input device initialization on the BUS concerned.
4 = func#4, IPL device initialization on the BUS concerned.
5 = func#5, general device initialization on the BUS concerned.
6 = func#6, error reporting for the BUS concerned.
7 = func#7, add-on ROM initialization for all BUSes.
8 = func#8, BBS ROM initialization for all BUSes.

The lower nibble 'Y' indicates the BUS on which the different routines are being executed. 'Y' can be from 0 to 5.

0 = Generic DIM (Device Initialization Manager).

1 = On-board System devices.
2 = ISA devices.
3 = EISA devices.
4 = ISA PnP devices.
5 = PCI devices.

Table B-5 ACPI Runtime Checkpoints

ACPI checkpoints are displayed when an ACPI capable operating system either enters or leaves a sleep state. The following table describes the type of checkpoints that may occur during ACPI sleep or wake events:

Checkpoint Code	Description
AC	First ASL check point. Indicates the system is running in ACPI mode.
AA	System is running in APIC mode.
01, 02, 03, 04, 05	Entering sleep state S1, S2, S3, S4, or S5.
10, 20, 30, 40, 50	Waking from sleep state S1, S2, S3, S4, or S5.

Critical Error BEEP Codes

The following table describes the beep codes that are used by AMIBIOS:

Table B-6 AMIBIOS Beep Codes

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error
3	Main memory read / write test error.
4	Motherboard timer not operational
5	Processor error
6	Keyboard controller BAT test error.
7	General exception error.
8	Display memory error.
9	ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory bad

Appendix C On-Board Industrial Devices

The Phoenix AT offers On-board two (optional second one) 10/100/1000 Ethernet controllers (First one optional 10/100/1000) and Three serial ports (one RS-422/485 optional). The Phoenix AT also offers two other On-Board Industrial devices: One ISA bridge and a Post Code display that will help you on troubleshooting.

Post Code Display

The POST code display is a device implemented on the Phoenix AT to help on failure diagnostics. A POST code is transmitted by the BIOS during the POST (Power On Self Test). It is a number that refers to the state or test condition of a circuit or group of circuits. Knowing the results of these tests (hence the POST code) can be very important in debugging a system.

POST Checkpoint Codes

When AMIBIOS8 performs the Power On Self Test, it writes diagnostic codes checkpoint codes to I/O port 0080h where the POST code display is connected. Please, refer to Appendix B for POST codes description.

ISA Bridge

The Phoenix ATX features a National Semiconductor PC87200 PCI to ISA Bridge. The PC87200 Enhanced Integrated PCI-to-ISA bridge works with an LPC chipset to provide ISA slot support.

The following summarizes the PCI to ISA bridge features:

- 5.0 V tolerant PCI and ISA interfaces.
- Slave mode serialized IRQ support for both quiet and continuous modes.
- PC/PCI DMA support.
- Supports ISA bus mastering.
- PCI 2.1 compliant 33 MHz bus.
- Supports PCI initiator-to-ISA and ISA master-to-PCI cycle translations.

- Subtractive agent for unclaimed transactions.
- Parallel to Serial IRQ conversion including IRQ3,4,5,6,7,9,10,11,12,14,15.
- Supports 3 ISA slots directly without buffering.
- Slow slew rate on edges.

On-board Ethernet

The Phoenix AT features two 10/100/1000 Ethernet controllers. Ethernet controller 1 is an Intel 82559ER 10/1000 (or 82551ER), that may optionally be upgraded to an Intel 82541ER, which is a 10/100/1000Mbps device. The optional Ethernet controller 2 is the Intel 82547GI 10/100/1000 Ethernet controller.

The 82559ER/551ER is a 32-bit PCI controller that features enhanced scatter-gather bus mastering capabilities, which enable the 82559ER/551ER to perform high-speed data transfers over the PCI bus. The 82559ER/551ER bus master capabilities enable the component to process high-level commands and to perform multiple operations, thereby off-loading communication tasks from the system CPU.

It can operate in either full duplex or half duplex mode. In full duplex mode it adheres to the IEEE 802.3x Flow Control specification. Half duplex performance is enhanced by a proprietary collision reduction mechanism.

The Intel® 82541ER (optional) integrates fourth generation gigabit MAC design with fully integrated, physical layer circuitry to provide a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE_TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). The controller is capable of transmitting and receiving data at rates of 1000 Mbps, 100 Mbps, or 10 Mbps. In addition to managing MAC and PHY layer functions, the controller provides a 32-bit wide direct Peripheral Component Interconnect (PCI) 2.3 compliant interface capable of operating at 33 or 66 MHz.

The 82541ER Architecture is designed for high performance and low memory latency. Wide internal data paths eliminate performance bottlenecks by efficiently handling large address and data words. The 82541ER controller includes advanced interrupt handling features to limit PCI bus traffic and a PCI interface that maximizes efficient bus usage. The 82541ER uses efficient ring buffer descriptor data structures, with up to 64 packet descriptors cached on chip. A large

64Kbyte onchip packet buffer maintains superior performance as available PCI bandwidth changes. In addition, using hardware acceleration, the controller offloads tasks from the host controller, such as TCP/UDP/IP checksum calculations and TCP segmentation.

It can be enabled or disabled through the BIOS.

The Intel® 82547GI(EI) (optional second Ethernet) Gigabit Ethernet Controller is a single, compact component with integrated Gigabit Ethernet Media Access Control (MAC) and physical layer (PHY) functions. This device utilizes the Communications Streaming Architecture (CSA) port of the 875P chipset. The Intel® 82547GI(EI) allows for a Gigabit Ethernet implementation in a very small area that is footprint compatible with current generation 10/100 Mbps Fast Ethernet designs. The Intel® 82547GI(EI) integrates Intel's fourth generation gigabit MAC design with fully integrated, physical layer circuitry to provide a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE_TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). The controller is capable of transmitting and receiving data at rates of 1000 Mbps, 100 Mbps, or 10 Mbps. In addition to managing MAC and PHY layer functions, the controller utilizes dedicated CSA port capability with a theoretical bandwidth of 266 MBytes/second. The 82547GI(EI) Gigabit Ethernet Controller with Communications Streaming Architecture is designed for high performance and low memory latency. The CSA port architecture is invisible to both system software and the operating system, allowing conventional "PCI-like" configuration. Wide internal data paths eliminate performance bottlenecks by efficiently handling large address and data words. The 82547GI(EI) controller includes advanced interrupt handling features. The 82547GI(EI) uses efficient ring buffer descriptor data structures, with up to 64 packet descriptors cached on chip. A large 40 KByte on-chip packet buffer maintains superior performance. In addition, by using hardware acceleration, the controller offloads tasks from the host, such as TCP/UDP/IP checksum calculations and TCP segmentation.

The Header Ethernet Connector pin-out of Ethernet 2 can be seen on *Table A-17*, and the Header Ethernet Connector pin-out of Ethernet 1 can be seen on *Table A-15 and Table A-16.*

Serial Ports

The Phoenix AT has three fixed RS-232 serial ports (RS-422/485 optional on SERC).

TIA/EIA-232

RS is the abbreviation for recommended standard. Usually, it is based on or is identical to other standards, e.g., EIA/TIA-232-F. TIA/EIA-232, previously known as RS-232 was developed in the 1960's to interconnect layers of the interface (ITU–T V.11), but also the pignut of the appropriate connectors (25-pin D-type or 9-pin DB9S) (ISO 2210) and the protocol (ISSUED-T V.24). The interface standard specifies also handshake and control lines in addition to the 2 unidirectional receive data line (RD) and transmit data line (TD). The control lines data carrier detect (DCD), data set ready (DSR), request to send (RTS), clear to send (CTS), data terminal ready (DTR), and the ring indicator (RI) might be used, but do not necessarily have to be (for example, the PC-serial-mouse utilizes only RI, TD, RD and GND). Although the standard supports only low speed data rates and line length of approximately 20 m maximum, it is still widely used. This is due to its simplicity and low cost.

Electrical

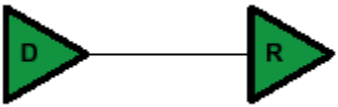
TIA/EIA-232 has high signal amplitudes of ±(5 V to 15 V) at the driver output. The triggering of the receiver depends on the sign of the input voltage: that is, it senses whether the input is above 3 V or less than –3 V. The line length is limited by the allowable capacitive load of less than 2500 pF. This results in a line length of approximately 20 m. The maximum slope of the signal is limited to 30 V/ms. The intention here is to limit any reflections that can occur to the rise-and fall-times of the signal. Therefore, transmission line theory does not need to be applied, so no impedance matching and termination measures are necessary.

Do not connect termination resistor when operating in RS-232 mode.

Protocol

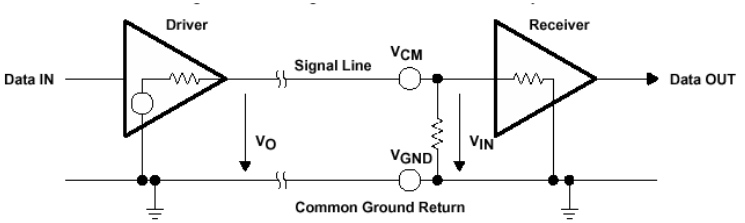
Different from other purely electrical-layer-standards, TIA/EIA-232 defines not only the physical layer of the interface (ITU-T V.11), but also the pinout of the appropriate connectors (25-pin D-type or 9-pin DB9S) (ISO 2210) and the protocol (ITU-T V.24). The interface standard specifies also handshake and control lines in addition to the 2 unidirectional receive data line (RD) and transmit data line (TD). The control lines might be used, but do not necessarily have to be.

RS-232 is Single-Ended Point-to-point Transmission



Single-Ended, Point-to-Point

Single-ended transmission is performed on one signal line, and the logical state is interpreted with respect to ground. For simple, low-speed interfaces, a common ground return path is sufficient; for more advanced interfaces featuring higher speeds and heavier loads, a single return path for each signaling line (twisted pair cable) is recommended. The figure below shows the electrical schematic diagram of a single-ended transmission system.



Advantages of Single-Ended Transmission

The advantages of single-ended transmission are simplicity and low cost of implementation. A single-ended system requires only one line per signal. It is therefore ideal for cabling, and connector costs are more important than the data transfer rate, e.g. PC, parallel printer port or serial communication with many handshaking lines, e.g. EIA-232. Cabling costs can be kept to a minimum with short distance communication, depending on data throughput, requiring no more than

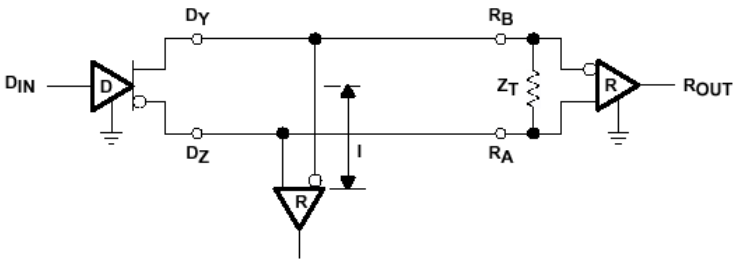
a low cost ribbon cable. For longer distances and/or noisy environments, shielding and additional ground lines are essential. Twisted pair cables are recommended for line lengths of more than 1 meter.

TIA/EIA-422

TIA/EIA-422 (RS-422) allows a multi-drop interconnection of one driver, transmitting unidirectionally to up to 10 receivers. Although it is not capable of bidirectional transfer, it is still applicable and used for talker-audience scenarios.

Electrical

TIA/EIA-422 (ITU-T V.11) is comparable to TIA/EIA-485. It is limited to unidirectional data traffic and is **terminated only at the line-end opposite to the driver**. The maximum line length is 1200m, the maximum data rate is determined by the signal rise- and fall-times at the receiver's side (requirement: <10% of bit duration). TIA/EIA-422 allows up to ten receivers (input impedance of 4 kΩ attached to one driver. The maximum load is limited to 80 Ω. Although any TIA/EIA-485 transceiver can be used in a TIA/EIA-422 system, dedicated TIA/EIA-422 circuits are not feasible for TIA/EIA-485, due to short circuit current limitations. The TIA/EIA-422 standard requires only short circuit limitation to 150 mA to ground, while TIA/EIA-485 additionally has to limit short circuit currents to 250 mA from the bus pins to –7 V and 12 V to address malfunctions in combination with ground shifts.

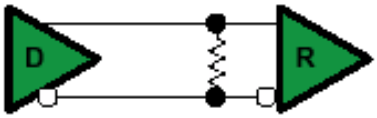


RS-422 is terminated only at the line-end opposite to the driver even if there is only one receiver.

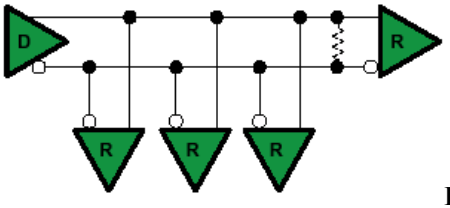
Protocol

Not applicable/none specified.

RS-422 is Differential and may be either Point-to-Point or Multi-Drop Connected



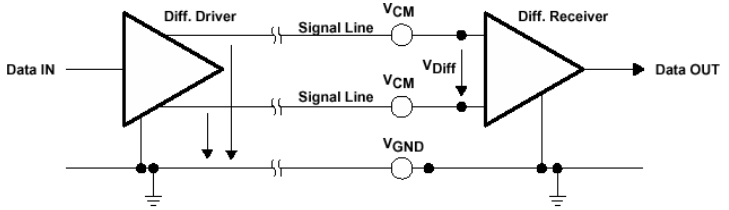
Differential, Point-to-Point



Differential, Multi-Drop

Differential Transmission

For balanced or differential transmission, a pair of signal lines is necessary for each channel. On one line, a true signal is transmitted, while on the second one, the inverted signal is transmitted. The receiver detects voltage difference between the inputs and switches the output depending on which input line is more positive. As shown below, there is additionally a ground return path.



Balanced interface circuits consist of a generator with differential outputs and a receiver with differential inputs. Better noise performance stems from the fact that noise is coupled into both wires of

the signal pair in much the same way and is common to both signals. Due to the common mode rejection capability of a differential amplifier, this noise will be rejected. Additionally, since the signal line emits the opposite signal like the adjacent signal return line, the emissions cancel each other. This is true in any case for crosstalk from and to neighboring signal lines. It is also true for noise from other sources as long as the common mode voltage does not go beyond the common mode range of the receiver. Since ground noise is also common to both signals, the receiver rejects this noise as well. The twisted pair cable used in these interfaces in combination with a correct line termination—to avoid line reflections—allows very high data rates and a cable length of up to 1200 m.

Advantages of Differential Transmission

Differential data transmission schemes are less susceptible to common-mode noise than single-ended schemes. Because this kind of transmission uses two wires with opposite current and voltage swings compared to only one wire for single-ended, any external noise is coupled onto the two wires as a common mode voltage and is rejected by the receivers. This two-wire approach with opposite current and voltage swings also radiates less electro-magnetic interference (EMI) noise than single-ended signals due to the canceling of magnetic fields.

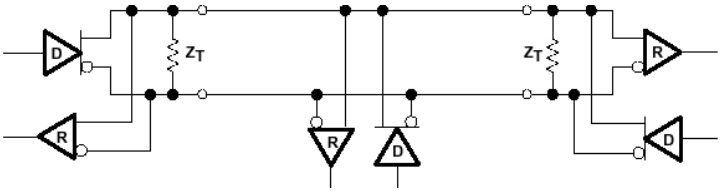
TIA/EIA-485

Historically, TIA/EIA-422 was on the market before TIA/EIA-485. Due to the lack of bi-directional capabilities, a new standard adding this feature was created: TIA/EIA-485 . The standard (TIA/EIA-485-A or ISO/IEC 8284) defines the electrical characteristics of the interconnection, including driver, line, and receiver. It allows data rates in the range of 35 Mbps and above and line lengths of up to 1200 m. Of course both limits can not be reached at the same time. Furthermore, recommendations are given regarding wiring and termination. The specification does not give any advice on the connector or any protocol requirements.

Electrical

TIA/EIA-485 describes a half-duplex, differential transmission on cable lengths of up to 1200 m and at data rates of typically up to 35 Mbps (requirement similar to TIA/EIA-422, but tr<30% of the bit duration, there are also faster devices available, suited for higher rates

under certain load-conditions). The standard allows a maximum of 32 unit loads of 12 kΩ, equal to 32 standard nodes or even higher count with increased input impedance. The maximum total load should not drop below 52 Ω. The common-mode voltage levels on the bus have to maintain between –7 V and 12 V. The receivers have to be capable to detect a differential input signal as low as 200 mV.

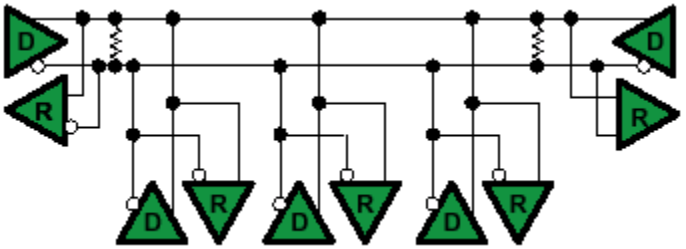


RS-485 is terminated at both sides of the common bus, even if only two stations are connected to the backbone.

Protocol

Not applicable/none specified; exceptions: SCSI systems and the DIN-Bus DIN66348.

RS-485 is Differential and Multi-Point Connected



Differential Transmission

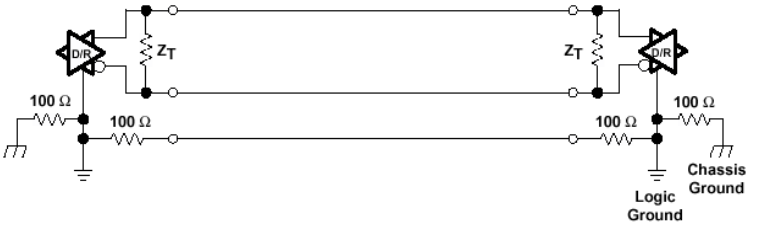
Please, read the Differential Transmission explanation in the previous RS-422 section.

Termination Resistors

Follow instructions in the previous RS-422 and RS-485 sections. The termination resistors available are rated to 120Ω.

Ground Connections

All 422- and 485-compliant system configurations shown up to this point do not have incorporated signal-return paths to ground. Obviously, having a solid ground connection so that both receivers and drivers can talk error free is imperative. The figure below shows how to make this connection and recommends adding some resistance between logic and chassis ground to avoid excess ground-loop currents. Logic ground does not have any resistance in its path from the driver or receiver. A potential problem might exist, especially during transients, when a high-voltage potential between the remote grounds could develop. Therefore, some resistance between them is recommended.



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