

# ***Gator ATX***

**Motherboard  
Installation Guide**



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First Edition.

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# **Introduction**

Thank you for your purchase of the Gator ATX industrial embedded motherboard. The Gator ATX design was based on the Intel 845GE chipset providing the ideal platform to industrial applications. The Gator ATX design is based on the Intel Pentium IV-M (mPGA478) processor, the low power mobile Pentium IV.

With proper installation and maintenance, your Gator ATX will provide years of high performance and trouble free operation.

This manual provides a detailed explanation into the installation and use of the Gator ATX industrial embedded motherboard. This manual is written for the novice PC user/installer. However, as with any major computer component installation, previous experience is helpful and should you not have prior experience, it would be prudent to have someone assist you in the installation. This manual is broken down into 3 chapters and 4 appendixes.

## **Chapter 1 - System Board Pre-Configuration**

This chapter provides all the necessary information for installing the Gator ATX. Topics discussed include: installing the CPU (if necessary), DRAM installation and jumper settings. Connecting all the cables from the system board to the chassis and peripherals is also explained.

## **Chapter 2 - BIOS Configuration**

This chapter shows the final step in getting your system firmware setup.

## **Chapter 3 - Upgrading**

The Gator ATX provides a number of expansion options including memory. All aspects of the upgrade possibilities are covered.

## **Appendix A - Technical Specifications**

A complete listing of all the major technical specifications of the Gator ATX is provided.

## **Appendix B - Flash BIOS Programming (optional) and Codes**

Provides all information necessary to program your optional General Software Embedded 2000 Flash BIOS. POST Codes and beep codes are described in details.

## **Appendix C – On-Board Industrial Devices**

Two on-board 10/100 (one 10/100/1000 optional) Ethernet controllers (second 10/100 Ethernet optional), ISA bridge, two serial ports (one optional RS422/485) and Post Code Display.

## **Appendix D - On-Board Video Controller**

On-board CRT video controller.

## ***Static Electricity Warning!***

The Gator ATX has been designed as rugged as possible but can still be damaged if jarred sharply or struck. Handle the motherboard with care. The Gator ATX also contains delicate electronic circuits that can be damaged or weakened by static electricity. Before removing the Gator ATX from its protective packaging, it is strongly recommended that you use a grounding wrist strap. The grounding strap will safely discharge any static electricity build up in your body and will avoid damaging the motherboard. Do not walk across a carpet or linoleum floor with the bare board in hand.

## ***Warranty***

This product is warranted against material and manufacturing defects for two years from the date of delivery. Buyer agrees that if this product proves defective the manufacturer is only obligated to repair, replace or refund the purchase price of this product at manufacturer's

discretion. The warranty is void if the product has been subjected to alteration, misuse or abuse; if any repairs have been attempted by anyone other than the manufacturer; or if failure is caused by accident, acts of God, or other causes beyond the manufacturer's control.

## **Gator ATX - An Overview**

The Gator ATX represents the ultimate in industrial embedded motherboard technology. No other system board available today provides such impressive list of features:

### **CPU Support**

- Supports full series of Intel Pentium IV-M (mPGA478 400MHz PSB - Mobile) processors.

### **Supported Bus Clocks**

- 400MHz.

### **Memory**

- Two DIMM sockets up to 2GB (unbuffered, non-ECC) DDR SDRAM, PC2100 (DDR 266MHz). Please, refer to chapter 3 for memory details.

### **On-Board I/O**

- 2 Floppies up to 2.88 MB.
- Dual channel PCI 32-bit EIDE controller – UDMA 66/100 supported. One extra connector (mini-Header 44 pin) in parallel to IDE2 for Solid State IDE disk or any 44 pin IDE device support.
- Two high speed RS-232 serial ports 16 Bytes FIFO (16550). Com B optional RS-232 IrDA or optional RS-422/485.
- One Centronics™ compatible bi-directional parallel port. EPP/ECP mode compatible.
- One PS/2 mouse and one PS/2 keyboard connectors.
- Auxiliary Keyboard/Mouse header for front panel access.

- Six Universal Serial Bus connectors, USB 1.1 and USB 2.0 compliant.
- Five 32-bit PCI slots, two 16-bit ISA slots (one sharing location with PCI slot 5) and one AGP 4x slot (Intel ADD compliant).
- DVO Header.
- Two RJ45 Ethernet connectors (second 10/100 optional, first optional 10/100/1000).
- Power Button – advanced management support.
- Eight GPIOs in a Header.
- Automatic CPU voltage & temperature monitoring device.
- On-board Buzzer.
- Audio (AD1885) AC97 compliant. Microphone In, Stereo Line In and Out, Auxiliary CD/Audio In.
- On-board POST Display Diagnostics.

### **ROM BIOS**

- General Software Embedded 2000 BIOS with optional FLASH ROM.

### **On-Board CRT video controller**

- Standard CRT video controller (Intel 845GE chipset).
- DVO connector.
- AGP 4X capable and ADD compliant.

### ***Conventions Used in this Manual***



*Notes - Such as a brief discussion of memory types.*



*Important Information - such as static warnings, or very important instructions.*



*When instructed to enter keyboard keystrokes, the text will be noted by this graphic.*

# Chapter 1 Pre-Configuration

This chapter provides all the necessary information for installing the Gator ATX into a standard PC chassis. Topics discussed include: installing the CPU (if necessary), DRAM installation and jumper settings.

## Handling Precautions

The Gator ATX has been designed to be as rugged as possible but it can be damaged if dropped, jarred sharply or struck. Damage may also occur by using excessive force in performing certain installation procedures such as forcing the system board into the chassis or placing too much torque on a mounting screw.

Take special care when installing or removing the system memory DIMMs. Never force a DIMM into a socket. Screwdrivers slipping off a screw and scraping the board can break a trace or component leads, rendering the board unusable. Always handle the Gator ATX with care.



### **Special Warranty Note:**

*Products returned for warranty repair will be inspected for damage caused by improper installation and misuse as described in the previous section and the static warning below. Should the board show signs of abuse, the warranty will become void and the customer will be billed for all repairs and shipping and handling costs.*

## **Static Warning**

The Gator ATX contains delicate electronic semiconductors that are highly sensitive to static electricity. These components, if subjected to a static electricity discharge, can be weakened thereby reducing the serviceable life of the system board. BEFORE THE BOARD IS REMOVED FROM ITS PROTECTIVE ANTISTATIC PACKAGING,

TAKE PROPER PRECAUTIONS! Work on a conductive surface that is connected to the ground. Before touching any electronic device, ground yourself by touching an unpainted metal object or, and highly recommended, use a grounding strap.

## Step 1 **Setting the Jumpers**

Your Gator ATX is equipped with a large number of peripherals. As such, there are a large number of configuration jumpers on the board. Taken step by step, setting these jumpers is easy. We suggest you review each section and follow the instructions.



**Special note about operating frequency:**  
*The Gator ATX has the ability to run at a variety of speeds without the need to change any crystal, oscillator or jumper.*

### Jumper Types

Jumpers are small copper pins attached to the system board. Covering two pins with a shunt closes the connection between them. The Gator ATX examines these jumpers to determine specific configuration information. There are two different categories of jumpers on the Gator ATX.

A. Two pin jumpers are used for binary selections such as enable, disable. Instructions for this type of jumper are open, for no shunt over the pins or closed, when the shunt covers the pins.

B. Three or four pin jumpers are used for multiple selections. Instructions for these jumpers will indicate which two pins to cover. For example: for JPx 2-3 the shunt will be covering pins 2 and 3 leaving pins 1 and 4 exposed.

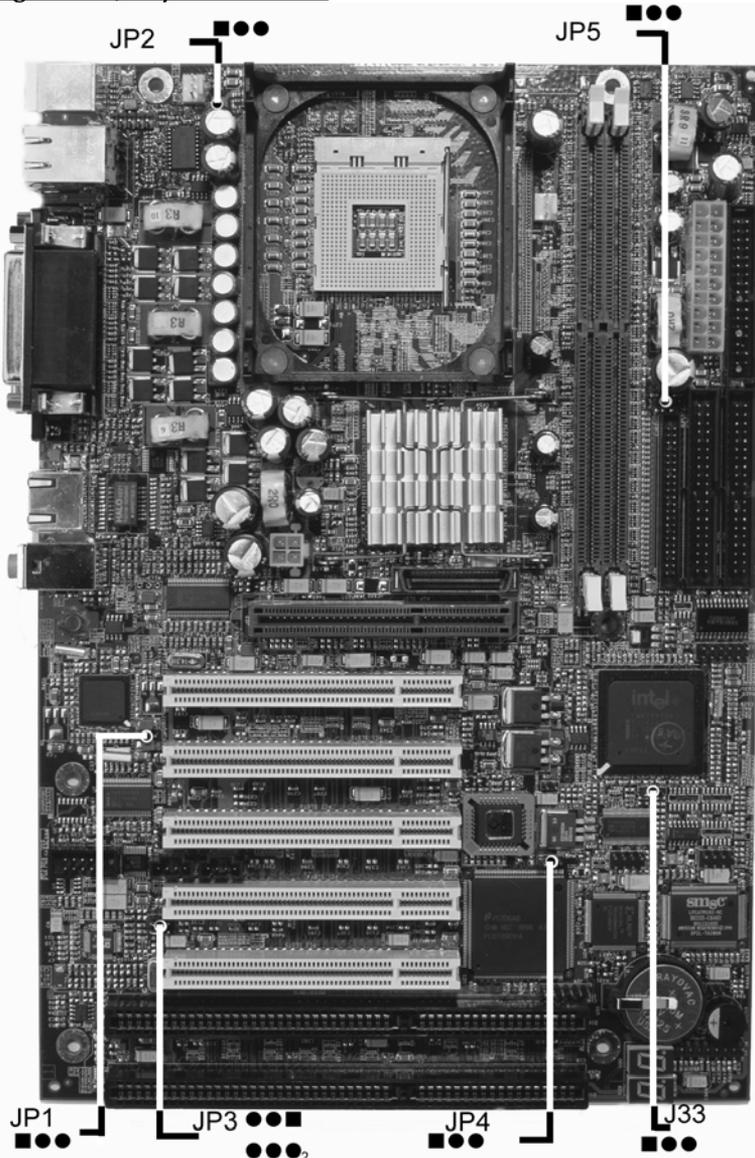
How to identify pin number 1 on *Figure 1-1*: Looking to the solder side (The board side without components) of the PCB (Printed Circuit Board), pin number 1 will have a squared pad ■. Other pins will have a circular pad ●. They are numbered sequentially.

Double row jumpers are numbered alternately, i.e. pin number 2 is in the other row, but in the same column of pin number 1. Pin number 3 is in the same row of pin 1, but in the next column and so forth.

## **Jumper Locations**

Use the diagram below and the tables on the following pages to locate and set the on-board configuration jumpers.

***Figure 1-1 Jumper Locations***



## **CMOS Reset**

This option is provided as a convenience for those who need to reset the CMOS registers. It should always be set to "Normal" for standard operation. If the CMOS needs to be reset, turn off the system, move J33/JP33 to 2-3, turn the system on, move jumper to 1-2 and press reset.

*Table 1-1 CMOS Reset*

<b>Reset CMOS</b>	<b>Normal</b>	<b>Clear CMOS</b>
J33/JP33	1-2*	2-3

\* *Manufacturer's Settings.*

## **ATX Power Supply Enhancements**

The Gator ATX has a Power on mode selection. The jumper JP4 selects the power on mode.

*Table 1-2 POWER ON Mode Select*

<b>Power on mode</b>	<b>Power on immediately</b>	<b>Power on upon PWR_SW signal (Button press)</b>
JP4	1-2*	2-3

\* *Manufacturer's Settings.*

## **ATA-Disk Connector Voltage Selection**

The ATA-Disk Connector J35 can provide either 5Vcc or 3.3Vcc. The jumper JP5 selects the voltage.

*Table 1-3 ATA-Disk Connector Voltage Select*

<b>ATA-Disk Voltage</b>	<b>5Vcc</b>	<b>3.3Vcc</b>
JP5	1-2*	2-3

\* *Manufacturer's Settings.*

## **Audio Jack Output Selection**

The audio output on the stacked audio jack connector J5 (green color) can be selected to be stereo line out or stereo headphone out (amplified signal). The jumper JP3 selects the audio output signals.

*Table 1-4 Audio Output Mode Selection*

<b>Audio Output Mode Selection</b>	<b>Headphone</b>	<b>Line Out</b>
JP3	1-3, 2-4	3-5, 4-6*

\* *Manufacturer's Settings.*

## **CPU Voltage Selection**

The Gator ATX can only support the Pentium IV-M Mobile CPU. Therefore, Jumper JP2 must always be selected to 2-3.



**ATTENTION:** changing this jumper may cause serious damage to your motherboard and CPU.

*Table 1-5 CPU Voltage Select*

<b>CPU Voltage</b>	<b>Desktop</b>	<b>Mobile</b>
JP2	1-2	2-3*

\* *Manufacturer's Settings.*

## **On-board Ethernet 10/100 Enabling**

The On-Board Ethernet 10/100 (Intel 82559ER/82551ER) may be Enabled or Disabled. The jumper JP1 selects the option. The disable option also disables the 66MHz of the 10/100/1000 Ethernet controller when the optional 1Gb Ethernet is present, this is mandatory for the 1Gb option.

*Table 1-6 On-Board Ethernet Select*

<b>On-Board Ethernet</b>	<b>Enabled</b>	<b>Disabled</b>
JP1	1-2*	2-3

\* *Manufacturer's Settings.*

## Step 2      **SDRAM, CPU, and Cables Installation**

Depending upon how your Gator ATX is configured you may need to install the following:

- SDRAM (DIMMs)
- CPU

### **Gator ATX Memory Configuration**

The Gator ATX offers 2 DIMM memory sockets (Locations J30 and J31 – *Figure 1-3*). They can be configured with 2.5V unbuffered SDRAM DDR modules. It is very important that the quality of the DIMMs is good. Unreliable operation of the system may result if poor quality DIMMs are used. Always purchase your memory from a reliable source. Please, refer to chapter 3 for memory details.

### **CPU Installation**

The Gator ATX currently supports the following CPUs:

- Full series of Intel Pentium IV-M 400MHz mPGA478 Mobile processors.



- 1. Improper installation of the CPU may cause permanent damage to both the system board and the CPU. -- Void of warranty*
- 2. Always handle the CPU by the edges, never touch the pins.*
- 3. Always use a heat-sink and a CPU fan.*

Locate the CPU socket on your Gator ATX system board (mPGA478 Socket – Location J22 – *Figure 1-3*). To install the processor, lift the lever of the ZIF socket and gently insert the CPU. The CPU will fit only in the right alignment. Make sure the CPU is inserted all the way. Lower the lever. Install the CPU fan. Make sure it is locked and connected to J26 (see pin-out in Appendix A).

The continued push of technology to increase performance levels (higher operating speeds) and packaging density (more transistors) is aggravating the thermal management of the CPU. As operating frequencies increase and packaging sizes decrease, the power density increases and the thermal cooling solution space and airflow become more constrained. The result is an increased importance on system design to ensure that thermal design requirements are met for the CPU.

The objective of thermal management is to ensure that the temperature of the processor is maintained within functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet their specified performance requirements. Operation outside the functional limit can degrade system performance, cause logic errors or cause component and/or system damage. Temperatures exceeding the maximum operating limits may result in irreversible changes in the operating characteristics of the component.

If the Gator ATX industrial embedded motherboard is acquired without the CPU and the thermal solution, extremely care must be taken to avoid improper thermal management. All Intel thermal solution specifications, design guidelines and suggestions to the CPU being used must be followed. The Gator ATX warranty is void if the thermal management does not comply with Intel requirements.

### **Designing for thermal performance**

In designing for thermal performance, the goal is to keep the processor within the operational thermal specifications. The inability to do so will shorten the life of the processor.

### **Fan Heatsink**

An active fan heatsink can be employed as a mechanism for cooling the Intel processors. This is the acceptable solution for most chassis.

Adequate clearance must be provided around the fan heatsink to ensure unimpeded air flow for proper cooling.

### **Airflow management**

It is important to manage the velocity, quantity and direction of air that flows within the system (and how it flows) to maximize the volume of air that flows over the processor.

### **Thermal interface management**

To optimize the heatsink design for the Pentium IV-M processor, it is important to understand the impact of factors related to the interface between the processor and the heatsink base. Specifically, the bond line thickness, interface material area, and interface material thermal

conductivity should be managed to realize the most effective thermal solution.

Once used, the thermal interface should be discarded and a new one installed. Never assemble the heatsink with a previously used thermal interface.

This completes the installation of the CPU. Now is it a good time to double check both the CPU and DIMM installation to make sure that these devices have been properly installed.

## **Installing Cables**

### **Power and Control Panel Cables**

The Gator ATX gets power from the power connectors J36 and J14 (*Figure 1-3*).

### **Installing Peripheral Cables**

Now it is a good time to install the internal peripherals such as floppy and hard disk drives. Do not connect the power cable to these peripherals, as it is easier to attach the bulky ribbon cables before the smaller power connectors. If you are installing more than one IDE drive double check your master/slave jumpers on the drives. Review the information supplied with your drive for more information on this subject.

Connect the floppy cable (not included) to the system board. Then connect remaining ends of the ribbon cable to the appropriate peripherals. Connect the serial port cable (included) and the auxiliary Keyboard/Mouse cable (not included) if using the alternative Keyboard/Mouse header connector. Finally, connect the IDE cable (not included) to the system. If using a Solid State Device, connect it to the mini-ATA connector. Then connect remaining ends of the ribbon cable to the appropriate peripherals. This concludes the hardware installation of your Gator ATX system. Now it is a good time to re-check all of the cable connections to make sure they are correct.

The connector hole layouts on the Gator ATX I/O Gasket (optional) are designed according to Intel ATX specifications.

*Figure 1-2 Gator ATX I/O Gasket*

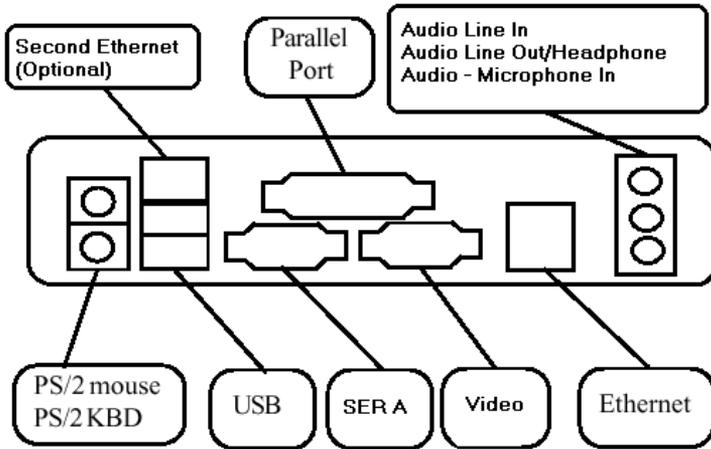
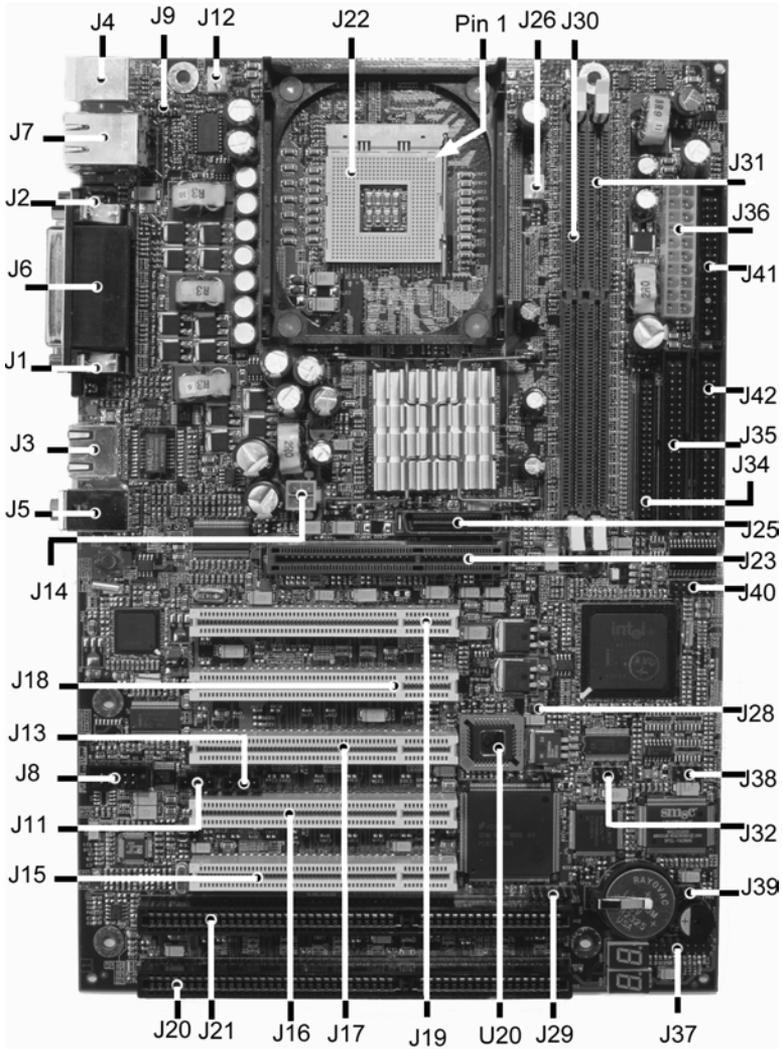


Figure 1-3 Location of Components and Connectors



## **Index of Connectors**

Please refer to Appendix A for pin-out descriptions.

*Table 1-7 Connectors description*

<b>Connector</b>	<b>Description</b>
J1	VGA DB15
J2	SER A
J3	Ethernet 1 (Optional 10/100/1000) RJ45
J4	(Bottom)Keyboard – PS/2 (Top)Mouse – PS/2
J5	Audio – Mic. In (pink), Line Out/Headphone (green) and Line In (blue)
J6	LPT - Parallel
J7	(Bottom) USB (Ports 2 & 3) - (Top) Ethernet 2 (Optional)
J8	SER B
J9	Keyboard/Mouse Header
J11	Audio - Aux. In Header
J12	Rear Chassis Fan
J13	Audio – CD In Header
J14	ATX Power Aux. Connector
J15	PCI Connector 5
J16	PCI Connector 4
J17	PCI Connector 3
J18	PCI Connector 2
J19	PCI Connector 1
J20	ISA Slot 1
J21	ISA Slot 2
J22	CPU Socket
J23	AGP Slot/ADD Connector
J25	DVO Connector
J26	CPU Fan
J28	Intruder detection Header
J29	JTAG
J30	DDR DIMM Socket 0
J31	DDR DIMM Socket 1

<b>Connector</b>	<b>Description</b>
J32	USB Header (Ports 4 & 5)
J34	Alt. Secondary IDE
J35	Secondary IDE
J36	ATX Power Connector
J37	Front Panel Header
J38	USB Header (Ports 0 & 1)
J39	Keylock Header
J40	GPIO Header
J41	Floppy Disk Drive Connector
J42	Primary IDE

**User's Notes:**

**User's Notes:**

## **Chapter 2**

# **Embedded BIOS 2000 Setup**

Your Gator ATX features General Software Embedded BIOS 2000. The system configuration parameters are set via the BIOS setup. Since the BIOS Setup resides in the ROM BIOS, it is available each time the computer is turned on.

General Software's EMBEDDED BIOS brand BIOS (Basic Input/Output System) pre-boot firmware is the industry's standard product used by most designers of embedded X86 computer equipment in the world today. Its superior combination of configurability and functionality enables it to satisfy the most demanding ROM BIOS needs for embedded designers. Its modular architecture and high degree of configurability make it the most flexible BIOS in the world.

When your platform is powered on, Embedded BIOS tests and initializes the hardware and programs the chipset and other peripheral components. During this time, Power On Self Test (POST) progress codes are written by the system BIOS to I/O port 80h, allowing the user to monitor the progress with a special monitor. Appendix B lists the POST codes and their meanings.

During early POST, no video is available to display error messages should a critical error be encountered; therefore, POST uses beeps on the speaker to indicate the failure of a critical system component during this time. Consult Appendix B for a list of Beep codes used by the BIOS.

### ***Starting BIOS Setup***

When a keyboard and video device are attached, the GatorATX can display either a traditional character-based PC BIOS display with memory count-up, or it can display a graphical POST with splash screen and progress icons. Both POST displays accept a <DEL> key press to enter the setup screen, and both display boot-time progress activity displays. The graphical display shows the status of file system devices, but omits character-based PCI resource display. The text-based POST displays the memory count-up and the PCI resource assignment table.

### ***BIOS Setup Main Menu***

The Gator ATX is configured from within the Setup Screen System, a series of menus that can be invoked from POST by pressing the <DEL> key.

Once in the Setup Screen System, the user can navigate with the UP and DOWN arrow keys from the main. TAB and ENTER are used to advance to the next field, and '+' and '-' keys cycle through values, such as those in the Basic Setup Screen.

The BIOS Setup main menu is organized into 14 windows. Each window is discussed in this chapter.

Each window contains several options. Clicking on each option activates a specific function. The BIOS Setup options and functions are described in this chapter. Some options may not be available in your BIOS. The windows are:

- Basic CMOS Configuration
- Features Configuration
- Custom Configuration
- Shadow Configuration
- Reset CMOS to Last Known Values
- Reset CMOS to Factory Defaults
- Write to CMOS and Exit
- Exit Without Saving CMOS

### **Basic CMOS Configuration Setup Screen**

The drive types, boot activities, and POST optimizations are configured from the Basic Setup Screen (Figure 2-1). In order to use disk drives with your system, you must select appropriate assignments of drive types in the left-hand column. Then, if you are using true floppy and IDE drives (not memory disks that emulate these drives), you need to configure the drive types themselves in the Floppy Drive Types and IDE Drive Geometry sections. Finally, you'll need to configure the boot sequence in the middle of the screen. Once these selections have been made, your system is ready to use.

System Bios Setup - Basic CMOS Configuration (C) 2001 General Software, Inc. All rights reserved			
<b>DRIVE ASSIGNMENT ORDER:</b>	Date: Aug 09, 2001	Typeomatic Delay : 250 ms	
Drive A: Floppy 0	Time: 17 : 24 : 52	Typeomatic Rate : 30 cps	
Drive B: <None>	NumLock: Disabled	Seek at Boot : Floppy	
Drive C: Ide 0/Pri Master		Show "Hit Del" : Enabled	
Drive D: <None>	<b>BOOT ORDER:</b>	Config Box : Enabled	
Drive E: <None>	Boot 1st: Drive A:	Fl Error Wait : Enabled	
Drive F: <None>	Boot 2nd: Drive G:	Parity Checking : <Unused>	
Drive G: <None>	Boot 3rd: <None>	Memory Test Tick : Enabled	
Drive H: <None>	Boot 4th: <None>	Debug Breakpoints: Disabled	
Drive I: <None>	Boot 5th: <None>	Debugger Hex Case: Upper	
Drive J: <None>	Boot 6th: <None>	Memory Test : StdLo FastHi	
Drive K: <None>			
Boot Method: Boot Sector	<b>ATA DRU ASSIGNMENT:</b> Sect Hds Cyls	Memory	
<b>FLOPPY DRIVE TYPES:</b>	Ide 0: 3 - AUTOCONFIG, LBA	Base:	
Floppy 0: 1.44 MB, 3.5"	Ide 1: 3 - AUTOCONFIG, LBA	512KB	
Floppy 1: 1.44 MB, 3.5"	Ide 2: 3 - AUTOCONFIG, LBA	Ext:	
	Ide 3: 3 - AUTOCONFIG, LBA	254MB	
↑/←/→/↓/CR/Tab to select or PgUp/PgDn/+/= to modify Esc to return to main menu			

**Figure 2-1: The Embedded BIOS Basic Setup Screen is used to configure drives, boot actions, and POST.**

### Configuring Drive Assignments

Embedded BIOS allows the user to map a different file system to each drive letter. The BIOS allows file systems for each floppy (Floppy0 and Floppy1), and each IDE drive (Ide0, Ide1, Ide2, and Ide3). Figure 2-1 shows how the first floppy drive (Floppy0) is assigned to drive A: in the system, and then shows how the first IDE drive (Ide0) is assigned to drive C: in the system.

To switch two floppy disks around or two hard disks around, just map Floppy0 to B: and Floppy1 to A:, and for hard disks map Ide0 to D: and Ide1 to C:.



**Caution:** Take care to not skip drive A: when making floppy disk assignments, as well as drive C: when making hard disk assignments. The first floppy should be A:, and the first hard drive should be C:. Also, do not assign the same file system to more than one drive letter. Thus, Floppy0 should not be used for both A: and B:. The BIOS permits this to allow embedded devices to alias drives, but desktop operating systems may not be able to maintain cache coherency with such a mapping in place.

### ***Date/Time***

Select the Date/Time option to change the date or time. The current date and time are displayed. Enter new values through the displayed window.

### ***NumLock***

Set this option to Disabled to turn the Num Lock key off when the computer is booted so you can use the arrow keys on both the numeric keypad and the keyboard.

### ***Seek at Boot***

Set this option to the device that will perform a Seek operation at system boot. The settings are Floppy (*default*), IDE, Both, and None.

### ***Typematic Rate***

The settings are 30 cps (*default*), 24, 20, 15, 12, 10, 8, and 6.

### ***Typematic Delay***

The settings are 250 ms (*default*), 500 ms, 750 ms, 1000 ms, and disabled.

### ***Config Box***

Set this option to show the configuration box during boot. The settings are Enabled (*default*) and Disabled.

### ***Memory Test Tick***

The settings are Enabled (*default*) and Disabled.

### **Memory Test**

This option configures the test that will be performed on the Low memory (below 1 MB) and the High Memory (above 1MB). The settings are Full (exhaustive testing), Standard, and Fast. The default is StdLo and FullHi.

### **Loader**

#### **Parity Checking**

#### **Debug Breakpoints**

#### **Debugger Hex Case**

These options are not available.

### **Show "Hit Del"**

Set this option to Disabled to prevent the message

*Hit <DEL> if you want to run Setup*

from appearing on the first BIOS screen when the computer boots. The setting is either Disabled or Enabled. The default setting is Enabled.

### **F1 Error Wait**

If this option is set to Enabled, the BIOS waits for the user to press <F1> before continuing. If this option is set to Disabled, the BIOS continues the boot process without waiting for <F1> to be pressed.

### **Configuring Floppy Drive Types**

Choose either Floppy Drive 0 or 1 to specify the floppy drive type. The settings are *360 KB 5¼"*, *1.2 MB 5¼"*, *720 KB 3½"*, *1.44 MB 3½"* and *2.88 MB 3½"*.

Floppy0 refers to the first floppy disk drive on the drive ribbon cable (normally drive A:), and Floppy1 refers to the second drive (drive B:).

### **Configuring IDE Drive Types**

The following table shows the drive assignments for Ide0-Ide3:

<b>File System</b>	<b>Controller</b>	<b>Master/Slave</b>
Ide0	Primary (1f0h)	Master
Ide1	Primary (1f0h)	Slave
Ide2	Secondary (170h)	Master
Ide3	Secondary (170h)	Slave

To use the primary master IDE drive in your system (the typical case), just configure Ide0 in this section, and map Ide0 to drive C: in the Configuring Drive Assignments section.

The IDE Drive Types section lets you select the type for each of the four IDE drives: None, User, Physical, LBA, or CHS.

The **User** type allows the user to select the maximum cylinders, heads, and sectors per track associated with the IDE drive. This method is now rarely used since LBA is now in common use.

The **Physical** type instructs the BIOS to query the drive's geometry from the controller on each POST. No translation on the drive's geometry is performed, so this type is limited to drives of 512MB or less. Commonly, this is used with embedded ATA PC Cards.

The **LBA** type instructs the BIOS to query the drive's geometry from the controller on each POST, but then translate the geometry according to the industry-standard LBA convention. This supports up to 128GB drives. **Use this method for all new drives.**

The **CHS** type instructs the BIOS to query the drive's geometry from the controller on each POST, but then translate the geometry according to the Gator CHS convention. Using this type on a drive previously formatted with LBA or Physical geometry might show data as being missing or corrupted.

EMBEDDED BIOS supports user-defined steps in the boot sequence. When the entire system has been initialized, POST executes these steps in order until an operating system successfully loads. In addition, other pre-boot features can be run before, after, or between operating system load attempts.

The following actions are supported:

**Drive A: - D:** Boot operating system from specified drive. The standard boot record will be invoked, causing DOS, Windows95, Windows 98, Windows ME, Windows 2000, Windows NT, Windows XP, Linux, or other industry-standard operating systems to load.

**CDROM:** Boot from the first IDE CDROM found that contains an El Torito bootable CDROM.

**None:** No action; POST proceeds to the next activity in the sequence.

**Reboot:** Reboot the board.

**Debugger; MFGMODE; DOS in ROM; Alarm; Maintenance; RAS; Power Off; CLI:** Options not available.

## **Features Configuration Setup Screen**

### ***Advanced Power Management***

Set this option to Enabled the power management and APM (Advanced Power Management) features. The settings for this option are: Disabled (*default*) and Enabled.

### ***Graphical/Audio POST***

Set this option to Enabled (*default*) the Splash Screen during boot. The settings for this option are: Disabled and Enabled (*default*).

### ***POST Memory Manager***

The settings are Enabled and Disabled (*default*).

### ***System Management BIOS***

The settings are Enabled (*default*) and Disabled. This option assembles the SMBIOS (formerly DMI) information.

## **Custom Configuration Setup Screen**

The hardware-specific features are configured with the Custom Setup Screen.

### ***L2 Cache***

This option enables or disables the L2 Cache.

### ***(Redir Debugger)***

This option is not available.

### ***Parallel Port***

This option enables (*default*) or disables the Parallel Port.

### ***Parallel Port IRQ***

This option specifies the IRQ always used by the parallel port. The settings are (IRQ) 5 and (IRQ) 7 (*default*).

### ***Parallel Port Address***

This option specifies the base I/O port address of the parallel port on the motherboard. The settings are 378h (*default*), 278h and 3BCh.

### ***Parallel Port Mode***

This option specifies the parallel port mode. The settings are: Printer (*default*), ECP/EPP 1.7, SPP, SPP/EPP 1.9, ECP, ECP/EPP 1.9, and SPP/EPP 1.7.

### **SER A**

This option enables (*default*) or disables the Serial Port A.

### **SER A Address**

This option specifies the base I/O port address of the Serial port A on the motherboard. The settings are 3F8h (*default*), 2F8h, 3E8h, 2E8h, 338h, 220h, 228h, and 238.

### **SER A IRQ**

This option specifies the IRQ of the Serial port A on the motherboard. The settings are 4 (*default*), 3, 5, 7, 12, 14, and 15.

### **SER B**

This option enables (*default*) or disables the Serial Port B.

### **SER B Address**

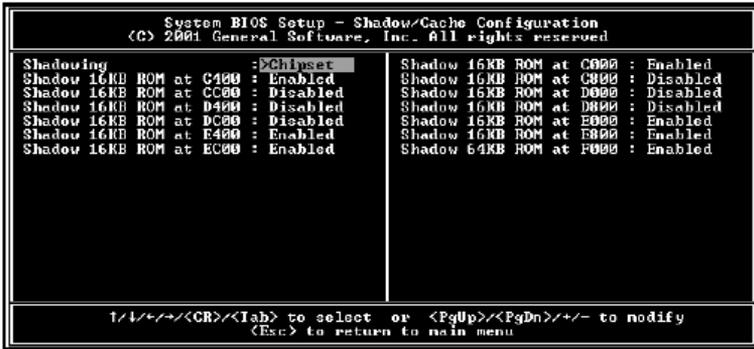
This option specifies the base I/O port address of the Serial port B on the motherboard. The settings are 3F8h, 2F8h (*default*), 3E8h, 2E8h, 338h, 220h, 228h, and 238.

### **SER B IRQ**

This option specifies the IRQ of the Serial port A on the motherboard. The settings are 4, 3 (*default*), 5, 7, 12, 14, and 15.

## **Shadow Configuration Setup Screen**

The Shadow Configuration Setup Screen (Figure 2-2) allows the selective enabling and disabling of shadowing in 16KB sections, except for the top 64KB of the BIOS ROM, which is shadowed as a unit. Normally, shadowing should be enabled at C000/C400 (to enhance VGA ROM BIOS performance) and then E000-F000 should be shadowed to maximize system ROM BIOS performance.



*Figure 2-2: The Embedded BIOS Shadow Setup Screen is used to configure ROM shadowing.*

## **Reset CMOS to Last Known Values**

Loads the CMOS to the last known values.

## **Reset CMOS to Factory Defaults**

The Fail-Safe CMOS factory Setup option settings can be loaded by selecting the Reset CMOS to Factory Defaults. Use this option as a diagnostic aid if the system is behaving erratically.

## **Write to CMOS and Exit**

Exit BIOS saving the changes.

## **Exit without Changing CMOS**

This option allows exiting the BIOS setup without saving any change to the CMOS.

## Chapter 3

## Upgrading

### Upgrading the Microprocessor

The latest revision of the Gator ATX currently supports full series of Intel Pentium IV-M (mPGA478 400MHz PSB - Mobile) processors. Please, check the manufacturer's web site for details and revisions regarding CPU speed.

Since the Gator ATX features CPU auto-sensing device there is no jumper to be set when changing the CPU.

### Upgrading the System Memory

The Gator ATX allows an upgrade of the system memory with up to 2GB unbuffered SDRAM DDR DIMM modules in two memory slots. Only non-ECC modules are supported. It is very important that the quality of the DIMMs is good. Unreliable operation of the system may result if poor quality DIMMs are used. Always purchase your memory from a reliable source. DDR266 memory modules are the only ones that can be used. DDR200 and DDR333 memory modules cannot be used

System Memory Features:

- 2.5 V (only) 184-pin DDR SDRAM DIMMs with gold-plated contacts.
- Unbuffered, unregistered single-sided or double-sided DIMMs.
- Maximum total system memory: 2 GB; minimum total system memory: 32 MB .
- DDR266 MHz (PC2100) DDR SDRAM DIMMs only.
- Serial Presence Detect (SPD).
- Do not use ECC DIMMs.
- Do not use Registered DIMMs.
- Do not use DDR200 DIMMs.
- Do not use DDR333 DIMMs.
- Double sided x16 DIMMs are not supported.

The following table lists the supported DDR DIMM Configurations:

***Table 3-1 Supported DDR DIMM Configurations***

DIMM Capacity	# of Dev./ DIMM	# of Sides	DRAM Tech.	Front Side Population		Back Side Population	
				Count	Config	Count	Config
32 MB	4	SS	64 Mbit	4	4 M x 16		
64 MB	8	SS	64 Mbit	8	8 M x 8		
64 MB	4	SS	128 Mbit	4	8 M x 16		
128 MB	16	DS	64 Mbit	8	8 M x 8	8	8 M x 8
128 MB	8	SS	128 Mbit	8	16 M x 8		
128 MB	4	SS	256 Mbit	4	16 M x 16		
256 MB	16	DS	128 Mbit	8	16 M x 8	8	16 M x 8
256 MB	8	SS	256 Mbit	8	32 M x 8		
256 MB	4	SS	512 Mbit	4	32 M x 16		
512 MB	16	DS	256 Mbit	8	32 M x 8	8	32 M x 8
512 MB	8	SS	512 Mbit	8	64 M x 8		
1024 MB	16	DS	512 Mbit	8	64 M x 8	8	64 M x 8

**User's Notes:**

# **Appendix A**

# **Technical Specifications**

## **Chipsets**

### *Core Logic*

North Bridge - Intel 845GE.

South Bridge – Intel ICH4.

### *Peripheral I/O*

Standard Microsystems (SMSC) LPC47M192.

### *Micro Processor Support*

Full series of Intel Pentium IV-M (mPGA478 400MHz PSB - Mobile) processors.

## **System Memory**

### *Memory Capacity*

Up to 2GB unbuffered SDRAM DDR DIMM Modules. Please, refer to chapter 3 for memory details.

### *Memory Type*

Two sockets for JEDEC standard (184 pins) DIMMs. The memory configuration is set automatically through BIOS via SPD. Supports SDRAM DDR 2.5V PC2100 (DDR 266 MHz) memory modules. Only non-ECC, unbuffered modules are supported. Please, refer to chapter 3 for memory details.

## **BIOS**

### ***System BIOS***

General Software Embedded BIOS 2000 with Flash BIOS option.

### ***Flash BIOS***

Optional feature for System BIOS. Flash programming built into the BIOS. BIOS to be flashed is read from a floppy when system booted from MS-DOS.

## **Embedded I/O**

### ***Floppy***

2 Floppies up to 2.88 MB.

### ***IDE***

Dual channel PCI 32-bit EIDE controller – UDMA 66/100 supported. One extra connector (mini-Header 44 pin) in parallel to IDE2 for Solid State IDE disk or any 44 pin IDE device support.

### ***Serial Ports***

Two high speed RS-232 serial ports 16 Bytes FIFO (16550/16550D). Com B optional RS-232 IrDA or optional RS-422/485.

### ***Parallel Port***

One Centronics™ compatible bi-directional parallel port. EPP/ECP mode compatible.

***Mouse Port***

One PS/2 mouse and one PS/2 keyboard connectors.  
Auxiliary Keyboard/Mouse header for front panel access.

***USB Interfaces***

Six Universal Serial Bus connectors. USB 1.1 and USB 2.0 compliant.

***On-board Ethernet***

Two RJ45 Ethernet connectors (second 10/100 optional, first optional 10/100/1000).

***On-board Buzzer***

***Audio***

Audio (AD1885) AC97 compliant. Microphone In, Stereo Line In and Out, Auxiliary CD/Audio In.

**Industrial Devices**

***Temperature and Voltage Device***

Automatic CPU voltage & temperature monitoring device (optional).

***Power Management***

Power button function: advanced power management support.

***General Purpose I/O lines***

Eight general purpose I/O lines in a header.

***On-Board POST Display Diagnostics***

## **Miscellaneous**

### ***CMOS/Battery***

RTC with lithium battery. No external battery is required.

### ***Control Panel Connections***

Reset, Keylock, Soft Power. LEDs for power and IDE.

### ***CPU Socket***

Standard ZIF (Zero Insertion Force), mPGA 478.

### ***Form Factor***

ATX form factor (12" x 8.2").

### ***PCB Construction***

Six Layers, dry film mask.

### ***Manufacturing Process***

Automated surface mount.

### **Table A-1 Environmental**

<b>Environmental</b>	<b>Operating</b>	<b>Non-operating</b>
Temperature	0° to +55° C	-40° to +65° C
Humidity	5 to 95% @ 40° C non-condensing	5 to 95% @ 40° C non-condensing
Shock	2.5G @ 10ms	10G @ 10ms
Vibration	0.25 @ 5-100Hz	5 @ 5-100Hz

## **Memory Map**

<b>Address Range Decimal</b>	<b>Address Range Hexadecimal</b>	<b>Size</b>	<b>Description</b>
960K-1M	0F0000-0FFFFFFF	64 KB	Upper BIOS
896K-960K	0E0000-0EFFFFF	64 KB	Lower BIOS
768K-896K	0C0000-0DFFFFF	128 KB	Expansion Card BIOS and Buffer
640K-768K	0A0000-0BFFFFF	128 KB	Standard PCI/ISA Video Memory
633K-640K	09E400-09FFFFF	7KB	BIOS Reserved
512K-633K	080000-09E3FF	121 KB	Ext. Conventional memory
0K- 512K	000000-07FFFFF	512 KB	Conventional memory

## **DMA Channels**

<b>DMA #</b>	<b>Data Width</b>	<b>System Resource</b>
<b>0</b>	8- or 16-bits	
<b>1</b>	8- or 16-bits	Parallel port (for ECP) (if selected)
<b>2</b>	8- or 16-bits	Floppy Drive
<b>3</b>	8- or 16-bits	Parallel port (for ECP) (if selected)
<b>4</b>	Reserved-	cascade channel
<b>5</b>	16-bits	Open
<b>6</b>	16-bits	Open
<b>7</b>	16-bits	Open

## **I/O Map**

<b>Address (hex)</b>	<b>Description</b>
0000-000F	DMA 1
0020-0021	Interrupt Controller 1
0040	Timer/Counter 0
0041	Timer/Counter 1
0042	Timer/Counter 2
0043	Timer Control Word
0060	Keyboard Controller Byte _ Reset IRQ
0061	NMI Status and Control
0070, bit 7	NMI enable
0070, bits 6:0	RTC Index
0071	RTC Data
0072	RTC Extended Index
0073	RTC Extended Data
0080-008F	DMA page registers / POST code display also located at 0080h
0092	Port 92
00A0-00A1	Interrupt Controller 2
00B2-00B3	APM control
00C0-00DE	DMA 2
00F0	Coprocessor Error
0170 _ 0177	Secondary IDE channel
01F0 _ 01F7	Primary IDE channel
0278-027F	LPT2 (if selected)
02E8-02EF	COM4 (default)
02F8-02FF	COM2 (default)
0310	Watch-Dog Timer (if selected)
0376	Secondary IDE channel command port
0377	Floppy channel 2 command
0377, bit 7	Floppy disk change, channel 2
0377, bits 6:0	Secondary IDE channel status port
0378-037F	LPT1 (default)
03B4-03B5	Video (VGA)
03BA	Video (VGA)
03BC-03CD	LPT3 (if selected)
03C0-03CA	Video (VGA)
03CC	Video (VGA)
03CE-03CF	Video (VGA)
03D4-03D5	Video (VGA)
03DA	Video (VGA)

<b>Address (hex)</b>	<b>Description</b>
03E8-03EF	COM3 (default)
03F0-03F5	Floppy Channel 1
03F6	Primary IDE channel command port
03F7	Floppy Channel 1 command
03F7, bit 7	Floppy disk change channel 1
03F7, bits 6:0	Primary IDE channel status report
03F8-03FF	COM1 (default)
0CF8-0CFB - 4 bytes	PCI configuration address register
0CF9	Reset control register
0CFC-0CFF - 4 bytes	PCI configuration data register

## **PCI Configuration Space Map**

<b>Bus #</b>	<b>Device #</b>	<b>Function #</b>	<b>Description</b>
00	00	00	845GE (Host Bridge)
00	01	00	845GE PCI to PCI Bridge
00	02	00	845GE VGA Controller
00	1D	00	ICH4 USB UHC 1
00	1D	01	ICH4 USB UHC 2
00	1D	02	ICH4 USB UHC 3
00	1D	07	ICH4 USB EHC
00	1E	00	Hub Interface to PCI Bridge
00	1F	00	ICH4 LPC Bridge
00	1F	01	ICH4 Master IDE Controller
00	1F	03	ICH4 SMBus Controller
00	1F	05	ICH4 AC97 Audio Controller
01	00	00	AGP Card
02	06	00	NSC PCI to ISA Bridge
02	08	00	LAN2 Controller (optional)
02	09	00	LAN1 Controller
02	0A	00	PCI expansion slot 1
02	0B	00	PCI expansion slot 2
02	0D	00	PCI expansion slot 3
02	0D	00	PCI expansion slot 4
02	0E	00	PCI expansion slot 5

## **Interrupts**

<b>IRQ</b>	<b>System Resource</b>
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved (keyboard)
2	Reserved (cascade)
3	COM2*
4	COM1*
5	User Available for PCI
6	Floppy Drive
7	LPT1*
8	Real time clock
9	User Available for PCI
10	User Available for PCI
11	User Available for PCI
12	PS/2 mouse port
13	Reserved (math coprocessor)
14	Primary IDE
15	Secondary IDE

*\*Default, but can be changed to another IRQ*

## **SMBUS**

<b>Device</b>	<b>Slave Address</b>
SIO	00101101b
Optional EEPROM	10100110b
DIMM0	01010000b
DIMM1	01010001b
Clock Chip Write	11010010b
Clock Chip Read	11010011b

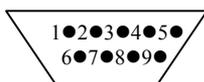
## PCI Interrupt Routing Map

ICH4 Signal	ID SEL	PIRQA	PIRQB	PIRQC	PIRQD	PIRQE	PIRQF	PIRQG	PIRQH
PCI Slot 1	AD26			INTA	INTB	INTC	INTD		
PCI Slot 2	AD27			INTB	INTC	INTD	INTA		
PCI Slot 3	AD28			INTC	INTD	INTA	INTB		
PCI Slot 4	AD29			INTD	INTA	INTB	INTC		
PCI Slot 5	AD30			INTB	INTC	INTD		INTA	
Ethernet 1	AD25								INTA
Ethernet 2						INTA			
IDE				INTA					
Audio			INTA						
ISA Br.	AD22								
USB 1		INTA							
USB 2					INTA				
USB 3				INTA					
USB 2.0									INTA
SMBus			INTA						
AGP		INTA	INTB						
VGA		INTA							

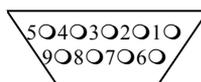
## Connectors Pin-out

How to identify pin number 1: Looking to the solder side (The board side without components) of the PCB (Printed Circuit Board), pin number 1 will have a squared pad ■. Other pins will have a circular pad ●.

How to identify other pins: Connectors type DB, PS/2, RJ45, Power ATX and USB are industry standards. DB connectors, for instance, are numbered sequentially. The first row is numbered in sequence (be aware that male and female connectors are mirrored – male connectors are numbered from left to right when viewed from front and female connectors are numbered from right to left when viewed from front). The following rows resume the counting on the same side of pin number 1. The counting is NOT circular like Integrated Circuits (legacy from electronic tubes).

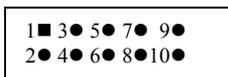


DB9 Male  
Front view



DB9 Female  
Front view

Header connectors are numbered alternately, i.e. pin number 2 is in the other row, but in the same column of pin number 1. Pin number 3 is in the same row of pin 1, but in the next column and so forth.



Header 10 pin connector  
View from solder side of the PCB

*Table A-9 Serial Port SER A DB9 Connector*

Pin#	Serial Port DB9M – J2
1	DCD
2	RX
3	TX
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

*Table A-10 Serial Port SER B Header Connector*

Pin#	Serial Port Header - J8
1	DCD - RS-422/485RXA(opt.)
2	DSR
3	RX - RS-422/485TXB(opt.)
4	RTS
5	TX - RS-422/485TXA(opt.)
6	CTS
7	DTR
8	RI – RS-422/485RXB(opt.)
9	GND
10	Key

**Table A-11 J3 Ethernet 1 RJ45**

<b>Pin#</b>	<b>Ethernet RJ45 – J3</b>
1	TX+
2	TX-
3	RX+
4	Shorted to 5
5	Shorted to 4
6	RX-
7	Shorted to 8
8	Shorted to 7

**Table A-12 J7 USB/Ethernet 2 (optional) Connector**

<b>Pin#</b>	<b>USB Connector – J7A</b>
1	+5V – USB2
2	-D – USB2
3	+D – USB2
4	GROUND – USB2
5	+5V – USB3
6	-D – USB3
7	+D – USB3
8	GROUND – USB3
<b>Pin#</b>	<b>Ethernet 2 (optional) Connector – J7B</b>
1	TX+
2	TX-
3	RX+
4	Shorted to 5
5	Shorted to 4
6	RX-
7	Shorted to 8
8	Shorted to 7

***Table A-13 J6 Parallel DB25 Connector***

<b>Pin#</b>	<b>Parallel DB25F – J6</b>
1	-STROBE
2	+DATA BIT 0
3	+DATA BIT 1
4	+DATA BIT 2
5	+DATA BIT 3
6	+DATA BIT 4
7	+DATA BIT 5
8	+DATA BIT 6
9	+DATA BIT 7
10	ACK1
11	BUSY
12	PAPER EMPTY
13	SLCT
14	AUTOFEED
15	ERROR
16	INIT
17	SLCT IN
18-25	GND

***Table A-14 J9 Keyboard/Mouse Header Connector***

<b>Pin#</b>	<b>Keyboard/Mouse Header - J11</b>
1	Mouse CLK
2	Keyboard CLK
3	HDD LED
4	Keyboard Data
5	VCC
6	VCC
7	GND
8	Mouse Data
9	GND
10	Key

***Table A-15 J32 USB Ports 4 & 5 Header Connector***

<b>Pin#</b>	<b>USB Header – J32</b>
1	+5V – USB5
2	+5V – USB4
3	-D – USB5
4	-D – USB4
5	+D – USB5
6	+D – USB4
7	GROUND – USB5
8	GROUND – USB4

***Table A-16 CPU Fan, Rear Chassis Fan, , Intruder, and Keylock.***

<b>Connector</b>	<b>Description</b>		
J26	<b>CPU FAN (pin out for PCB rev.3+)</b>		
	1) Sense	2)+12V	3) GND (PWM)
J12	<b>Rear Chassis FAN</b>		
	1)Sense	2)+12V	3) GND (PWM)
J28	<b>Intruder</b>		
	1)Sense	2) GND	
J39	<b>Keylock</b>		
	1)Keylock#	2) GND	

***Table A-17 J38 USB Ports 0 & 1 Header Connector***

<b>Pin#</b>	<b>USB Header – J38</b>
1	+5V – USB0
2	+5V – USB1
3	-D – USB0
4	-D – USB1
5	+D – USB0
6	+D – USB1
7	GROUND – USB0
8	GROUND – USB1

***Table A-18 J40 GPIO Header Connector***

<b>Pin#</b>	<b>GPIO Header – J40</b>
1	GPIO34
2	GPIO35
3	GPIO36
4	GPIO37
5	GPIO38
6	GND
7	GPIO39
8	GPIO40
9	GPIO41
10	GPIO42
11	GPIO43
12	GND

***Table A-19 J37 Front Panel Header Connector***

<b>Pin#</b>	<b>Front Panel Header – J37</b>
1	HDD LED Anode
2	Power LED Green Blink
3	HDD LED Cathode
4	Power LED Yellow Blink
5	Reset - GND
6	Power Switch
7	Reset
8	Power Switch - GND
9	+5V
10	NC
11	Infra Red Rx (Opt.)
12	GND
13	GND
14	Power LED Cathode - GND
15	Infra Red Tx (Opt.)
16	Power LED Anode

## **Appendix B**

# **Flash BIOS programming and codes**

The Gator ATX offers the optional FLASH BIOS. When installed, you will be able to update your BIOS without having to replace the EPROM. The General Software embedded BIOS 2000 will read the new BIOS file from a floppy disk when running MS-DOS, replace the old BIOS and ask you to reboot your computer.

When updating your BIOS, make sure you have a disk with the correct BIOS file (its size should be 4Mb (512kB)).

How to reflash the BIOS:

About the General Software Reflash utility:

Reflash is a simple utility that loads a valid Embedded BIOS image, and uses the media driver from the BIOS within that image to reflash the BIOS. Be aware that this operation **MUST NOT BE INTERRUPTED!** A power outage may be fatal. No recovery method is provided, since Embedded BIOS does not support a boot block recovery structure at this time.

Running Reflash from the command line:

- Boot from MS-DOS without loading EMM386.exe and HIMEM.SYS.
- Have a directory containing the following files:
  - Reflash.exe
  - Reflash.cmd
  - BIOS.bin
  - BIOS.abs

Where “BIOS” is the BIOS revision file that you want to load in the flash part.

- Type reflash and hit <enter>.
- Answer yes to the confirmation question.
- Reboot the machine when the procedure is over.

## **Troubleshooting POST**

Embedded BIOS writes progress codes, also known as POST codes, to I/O port 80h during POST, in order to provide information to OEM developers about system faults. These POST codes may be monitored by the On-board POST Display.

*Table B-1 Embedded BIOS 2000 POST Codes*

<b>Mnemonic Code</b>	<b>Code</b>	<b>System Progress Report</b>
POST_STATUS_START	00h	Start POST (BIOS is executing).
POST_STATUS_CPUTEST	01h	Start CPU register test.
POST_STATUS_DELAY	02h	Start power-on delay.
POST_STATUS_DELAYDONE	03h	Power-on delay finished.
POST_STATUS_KBDBATRDY	04h	Keyboard BAT finished.
POST_STATUS_DISABSHADOW	05h	Disable shadowing & cache.
POST_STATUS_CALCKSUM	06h	Compute ROM CRC, wait for KBC.
POST_STATUS_CKSUMGOOD	07h	CRC okay, KBC ready.
POST_STATUS_BATVRFY	08h	Verifying BAT command to KB.
POST_STATUS_KBDCMD	09h	Start KBC command.
POST_STATUS_KBDDATA	0ah	Start KBC data.
POST_STATUS_BLKUNBLK	0bh	Start pin 23,24 blocking & unblocking.
POST_STATUS_KBDNOP	0ch	Start KBC NOP command.
POST_STATUS_SHUTTEST	0dh	Test CMOS RAM shutdown register.
POST_STATUS_CMOSDIAG	0eh	Check CMOS checksum.
POST_STATUS_CMOSINIT	0fh	Initialize CMOS contents.
POST_STATUS_CMOSSTATUS	10h	Initialize CMOS status for date/time.
POST_STATUS_DISABDMAINT	11h	Disable DMA, PICs.
POST_STATUS_DISABPORTB	12h	Disable Port B, video display.

Mnemonic Code	Code	System Progress Report
POST_STATUS_BOARD	13h	Initialize board, start memory detection.
POST_STATUS_TESTTIMER	14h	Start timer tests.
POST_STATUS_TESTTIMER2	15h	Test 8254 T2, for speaker, port B.
POST_STATUS_TESTTIMER1	16h	Test 8254 T1, for refresh.
POST_STATUS_TESTTIMER0	17h	Test 8254 T0, for 18.2Hz.
POST_STATUS_MEMREFRESH	18h	Start memory refresh.
POST_STATUS_TESTREFRESH	19h	Test memory refresh.
POST_STATUS_TEST15US	1ah	Test 15usec refresh ON/OFF time.
POST_STATUS_TEST64KB	1bh	Test base 64KB memory.
POST_STATUS_TESTDATA	1ch	Test data lines.
POST_STATUS_TESTADDR	20h	Test address lines.
POST_STATUS_TESTPARITY	21h	Test parity (toggling).
POST_STATUS_TESTMEMRDWR	22h	Test Base 64KB memory.
POST_STATUS_SYSINIT	23h	Prepare system for IVT initialization.
POST_STATUS_INITVECTORS	24h	Initialize vector table.
POST_STATUS_8042TURBO	25h	Read 8042 for turbo switch setting.
POST_STATUS_POSTTURBO	26h	Initialize turbo data.
POST_STATUS_POSTVECTORS	27h	Modification of IVT.
POST_STATUS_MONOMODE	28h	Video in monochrome mode verified.
POST_STATUS_COLORMODE	29h	Video in color mode verified.
POST_STATUS_TOGGLEPARITY	2ah	Toggle parity before video ROM test.
POST_STATUS_INITBEFOREVIDEO	2bh	Initialize before video ROM check.

<b>Mnemonic Code</b>	<b>Code</b>	<b>System Progress Report</b>
POST_STATUS_VIDEOROM	2ch	Passing control to video ROM.
POST_STATUS_POSTVIDEO	2dh	Control returned from video ROM.
POST_STATUS_CHECKEGA_VGA	2eh	Check for EGA/VGA adapter.
POST_STATUS_TESTVIDEOMEMORY	2fh	No EGA/VGA found, test video memory.
POST_STATUS_RETRACE	30h	Scan for video retrace signal.
POST_STATUS_ALTDISPLAY	31h	Primary retrace failed.
POST_STATUS_ALTRETRACE	32h	Alternate found.
POST_STATUS_VRFYSWADAPTER	33h	Verify video switches.
POST_STATUS_SETDISPMODE	34h	Establish display mode.
POST_STATUS_CHECKSEG40A	35h	Initialize ROM BIOS data area.
POST_STATUS_SETCURSOR	36h	Set cursor for power-on msg.
POST_STATUS_PWRONDISPLAY	37h	Display power-on message.
POST_STATUS_SAVECURSOR	38h	Save cursor position.
POST_STATUS_BIOSIDENT	39h	Display BIOS identification string.
POST_STATUS_HITDEL	3ah	Display “Hit <DEL> to ...” message.
POST_STATUS_VIRTUAL	40h	Prepare protected mode test.
POST_STATUS_DESCR	41h	Prepare descriptor tables.
POST_STATUS_ENTERVM	42h	Enter virtual mode for memory test.
POST_STATUS_ENABINT	43h	Enable interrupts for diagnostics mode.
POST_STATUS_CHECKWRAP1	44h	Initialize data for memory wrap test.
POST_STATUS_CHECKWRAP2	45h	Test for wrap, find total memory size.
POST_STATUS_HIGHPATTERNS	46h	Write extended memory test patterns.

Mnemonic Code	Code	System Progress Report
POST_STATUS_ LOWPATTERNS	47h	Write conventional memory test patterns.
POST_STATUS_ FINDLOWMEM	48h	Find low memory size from patterns.
POST_STATUS_ FINDHIMEM	49h	Find high memory size from patterns.
POST_STATUS_ CHECKSEG40B	4ah	Verify ROM BIOS data area again.
POST_STATUS_ CHECKDEL	4bh	Check for <DEL> pressed.
POST_STATUS_ CLREXTMEM	4ch	Clear extended memory for soft reset.
POST_STATUS_ SAVEMEMSIZE	4dh	Save memory size.
POST_STATUS_ COLD64TEST	4eh	Cold boot: Display 1st 64KB memtest.
POST_STATUS_ COLDLOWTEST	4fh	Cold boot: Test all of low memory.
POST_STATUS_ ADJUSTLOW	50h	Adjust memory size for EBDA usage.
POST_STATUS_ COLDHITEST	51h	Cold boot: Test high memory.
POST_STATUS_ REALMODETEST	52h	Prepare for shutdown to real mode.
POST_STATUS_ ENTERREAL	53h	Return to real mode.
POST_STATUS_ SHUTDOWN	54h	Shutdown successful.
POST_STATUS_ DISABA20	55h	Disable A20 line.
POST_STATUS_ CHECKSEG40C	56h	Check ROM BIOS data area again.
POST_STATUS_ CHECKSEG40D	57h	Check ROM BIOS data area again.
POST_STATUS_ CLRHITDEL	58h	Clear “Hit <DEL>” message.
POST_STATUS_ TESTDMAPAGE	59h	Test DMA page register file.
POST_STATUS_ VRFYDISPMEM	60h	Verify from display memory.
POST_STATUS_ TESTDMA0BASE	61h	Test DMA0 base register.

<b>Mnemonic Code</b>	<b>Code</b>	<b>System Progress Report</b>
POST_STATUS_ TESTDMA1BASE	62h	Test DMA1 base register.
POST_STATUS_ CHECKSEG40E	63h	Checking ROM BIOS data area again.
POST_STATUS_ CHECKSEG40F	64h	Checking ROM BIOS data area again.
POST_STATUS_PROGDMA	65h	Program DMA controllers.
POST_STATUS_ INITINTCTRL	66h	Initialize PICs.
POST_STATUS_ STARTKBDTEST	67h	Start keyboard test.
POST_STATUS_KBDRESET	80h	Issue KB reset command.
POST_STATUS_ CHECKSTUCKKEYS	81h	Check for stuck keys.
POST_STATUS_ INITCIRCBUFFER	82h	Initialize circular buffer.
POST_STATUS_ CHECKLOCKEDKEYS	83h	Check for locked keys.
POST_STATUS_ MEMSIZEMISMATCH	84h	Check for memory size mismatch.
POST_STATUS_ PASSWORD	85h	Check for password or bypass setup.
POST_STATUS_ BEFORESETUP	86h	Password accepted.
POST_STATUS_ CALLSETUP	87h	Entering setup system.
POST_STATUS_ POSTSETUP	88h	Setup system exited.
POST_STATUS_ DISPPWRON	89h	Display power-on screen message.
POST STATUS DISPWAIT	8ah	Display “Wait...” message.
POST_STATUS_ ENABSHADOW	8bh	Shadow system & video BIOS.
POST_STATUS_ STDCMOSSETUP	8ch	Load standard setup values from CMOS.
POST STATUS MOUSE	8dh	Test and initialize mouse.
POST STATUS FLOPPY	8eh	Test floppy disks.
POST_STATUS_ CONFIGFLOPPY	8fh	Configure floppy drives.
POST STATUS IDE	90h	Test hard disks.
POST_STATUS_ CONFIGIDE	91h	Configure IDE drives.

Mnemonic Code	Code	System Progress Report
POST_STATUS_CHECKSEG40G	92h	Checking ROM BIOS data area.
POST_STATUS_CHECKSEG40H	93h	Checking ROM BIOS data area.
POST_STATUS_SETMEMSIZE	94h	Set base & extended memory sizes.
POST_STATUS_SIZEADJUST	95h	Adjust low memory size for EBDA.
POST_STATUS_INITC8000	96h	Initialize before calling C800h ROM.
POST_STATUS_CALLC8000	97h	Call ROM BIOS extension at C800h.
POST_STATUS_POSTC8000	98h	ROM C800h extension returned.
POST_STATUS_TIMERPRNBASE	99h	Configure timer/printer data.
POST_STATUS_SERIALBASE	9ah	Configure serial port base addresses.
POST_STATUS_INITBEFORENPX	9bh	Prepare to initialize coprocessor.
POST_STATUS_INITNPX	9ch	Initialize numeric coprocessor.
POST_STATUS_POSTNPX	9dh	Numeric coprocessor initialized.
POST_STATUS_CHECKLOCKS	9eh	Check KB settings.
POST_STATUS_ISSUEKBDID	9fh	Issue keyboard ID command.
POST_STATUS_RESETID	0a0h	KB ID flag reset.
POST_STATUS_TESTCACHE	0a1h	Test cache memory.
POST_STATUS_DISPSTERR	0a2h	Display soft errors.
POST_STATUS_TYPMATIC	0a3h	Set keyboard typematic rate.
POST_STATUS_MEMWAIT	0a4h	Program memory wait states.
POST_STATUS_CLRSCR	0a5h	Clear screen.
POST_STATUS_ENABPTYNMI	0a6h	Enable parity and NMIs.
POST_STATUS_INITE000	0a7h	Initialize before calling ROM at E000h.

<b>Mnemonic Code</b>	<b>Code</b>	<b>System Progress Report</b>
POST_STATUS_CALLE000	0a8h	Call ROM BIOS extension at E000h.
POST_STATUS_POSTE000	0a9h	ROM extension returned.
POST_STATUS_DISPCONFIG	0b0h	Display system configuration box.
POST_STATUS_INT19BOOT	00h	Call INT 19h bootstrap loader.
POST_STATUS_LOWMEMEXH	0b1h	Test low memory exhaustively.
POST_STATUS_EXTMEMEXH	0b2h	Test extended memory exhaustively.
POST_STATUS_PCIENUM	0b3h	Enumerate PCI busses.

## **Critical Error BEEP Codes**

Embedded BIOS tests much of the hardware early in POST before messages can be displayed on the screen. When system failures are encountered at these early stages, POST uses beep codes (a sequence of tones on the speaker) to identify the source of the error.

The following is a comprehensive list of POST beep codes for the system BIOS. BIOS extensions, such as VGA ROMs and SCSI adapter ROMs, may use their own beep codes, including short/long sequences, or possibly beep codes that sound like the ones below. When diagnosing a system failure, remove these adapters if possible before making a final determination of the actual POST test that failed.

***Table B-2 Flash BIOS Beep Errors***

<b>Mnemonic Code</b>	<b>Beep Count</b>	<b>Description of Problem</b>
POST_BEEP_REFRESH	1	Memory refresh is not working.
POST_BEEP_PARITY	2	Parity error found in 1st 64KB of memory.
POST_BEEP_BASE64KB	3	Memory test of 1st 64KB failed.
POST_BEEP_TIMER	4	T1 timer test failed.
POST_BEEP_CPU	5	CPU test failed.

<b>Mnemonic Code</b>	<b>Beep Count</b>	<b>Description of Problem</b>
POST_BEEP_GATEA20	6	Gate A20 test failed.
POST_BEEP_DMA	7	DMA page/base register test failed.
POST_BEEP_VIDEO	8	Video controller test failed.
POST_BEEP_KEYBOARD	9	Keyboard test failed.
POST_BEEP_SHUTDOWN	10	CMOS shutdown register test failed.
POST_BEEP_CACHE	11	External cache test failed.
POST_BEEP_BOARD	12	General board initialization failed.
POST_BEEP_LOWMEM	13	Exhaustive low memory test failed.
POST_BEEP_EXTMEM	14	Exhaustive extended memory test failed.
POST_BEEP_CMOS	15	CMOS restart byte test failed.
POST_BEEP_ADDRESS_LINE	16	Address line test failed.
POST_BEEP_DATA_LINE	17	Data line test failed.
POST_BEEP_INTERRUPT	18	Interrupt controller test failed.
POST_BEEP_PASSWORD	1	Incorrect password used to access SETUP.

**User's Notes:**

# **Appendix C      On-Board Industrial Devices**

The Gator ATX offers On-board two (optional second one) 10/100 Ethernet controllers (First one optional 10/100/1000) and two serial ports (one RS-422/485 optional). The Gator ATX also offers two other On-Board Industrial devices: One ISA bridge and a Post Code display that will help you on troubleshooting.

## **Post Code Display**

The POST code display is a device implemented on the Gator ATX to help on failure diagnostics. A POST code is transmitted by the BIOS during the POST (Power On Self Test). It is a number that refers to the state or test condition of a circuit or group of circuits. Knowing the results of these tests (hence the POST code) can be very important in debugging a system.

### **POST Checkpoint Codes**

When Embedded BIOS 2000 performs the Power On Self Test, it writes diagnostic codes checkpoint codes to I/O port 0080h where the POST code display is connected. Please, refer to Appendix B for POST codes description.

## **ISA Bridge**

The Gator ATX features a National Semiconductor PC87200 PCI to ISA Bridge. The PC87200 Enhanced Integrated PCI-to-ISA bridge works with an LPC chipset to provide ISA slot support.

The following summarizes the PCI to ISA bridge features:

- 5.0 V tolerant PCI and ISA interfaces.
- Slave mode serialized IRQ support for both quiet and continuous modes.
- PC/PCI DMA support.
- Supports ISA bus mastering.
- PCI 2.1 compliant 33 MHz bus.
- Supports PCI initiator-to-ISA and ISA master-to-PCI cycle translations.

- Subtractive agent for unclaimed transactions.
- Parallel to Serial IRQ conversion including IRQ3,4,5,6,7,9,10,11,12,14,15.
- Supports 2 ISA slots directly without buffering.
- Slow slew rate on edges.

### **On-board Ethernet**

The Gator ATX features two 10/100 Ethernet controllers. Ethernet controller 1 is an Intel 82559ER (or 82551ER), that may optionally be upgraded to an Intel 82540EM, which is a 10/100/1000Mbps device. The optional Ethernet controller 2 is the Intel ICH4 internal MAC + Intel 82562EM PHY.

The 82559ER/551ER is a 32-bit PCI controller that features enhanced scatter-gather bus mastering capabilities, which enable the 82559ER/551ER to perform high-speed data transfers over the PCI bus. The 82559ER/551ER bus master capabilities enable the component to process high-level commands and to perform multiple operations, thereby off-loading communication tasks from the system CPU.

It can operate in either full duplex or half duplex mode. In full duplex mode it adheres to the IEEE 802.3x Flow Control specification. Half duplex performance is enhanced by a proprietary collision reduction mechanism.

It can be enabled or disabled through jumper JP1.

The ICH4's integrated LAN controller (optional second Ethernet) includes a 32-bit PCI controller that provides enhanced scatter-gather bus mastering capabilities and enables the LAN controller to perform high-speed data transfers over the PCI bus. Its bus master capabilities enable the component to process high level commands and perform multiple operations, which lowers processor utilization by off-loading communication tasks from the processor. Two large transmit and receive FIFOs of 3 KB each help prevent data underruns and overruns while waiting for bus accesses. This enables the integrated LAN controller to transmit data with minimum interframe spacing (IFS).

The ICH4 integrated LAN controller can operate in either full-duplex or half-duplex mode. In full- duplex mode the LAN controller adheres with the IEEE 802.3x Flow Control specification. Half duplex

performance is enhanced by a proprietary collision reduction mechanism.

The following summarizes the ICH4 LAN controller features:

- Compliance with Advanced Configuration and Power Interface and PCI Power Management standards.
- Support for wake-up on interesting packets and link status change.
- Support for remote power-up using Wake on LAN (WOL) technology.
- Deep power-down mode support.
- Support of Wired for Management (WfM) Rev 2.0.
- Backward compatible software with 82557, 82558 and 82559.
- TCP/UDP checksum off load capabilities.
- Support for Intel's Adaptive Technology.

The Intel 82540EM (optional for Ethernet 1) combines Intel's fourth-generation Gigabit MAC design, with fully integrated, physical-layer circuitry to provide a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, 802.3ab).

The Intel 82540EM Gigabit Ethernet Controller architecture is optimized to deliver both high-performance networking and PCI bus efficiency with the lowest power and smallest size. Using state logic design with a pipelined DMA Unit and 128-bit-wide buses for the fastest performance, the 82540EM controller handles Gigabit Ethernet traffic with low network latency and minimal internal processing overhead. The controller's architecture includes independent transmit and receive queues to limit PCI bus traffic, and a PCI interface that maximizes the use of bursts for efficient bus usage. The Intel 82540EM Gigabit Ethernet Controller prefetches up to 64 packet descriptors in a single burst for efficient PCI-bandwidth usage. A 64KB, on-chip packet buffer maintains superior performance as available PCI bandwidth changes. Advanced interrupt moderation hardware manages interrupts generated by the 82540EM controller to further improve system efficiency. In addition, using hardware acceleration, the controller also offloads tasks from the host processor, such as TCP/UDP/IP checksum calculations and TCP segmentation.

The RJ45 Ethernet Connector pin-out of Ethernet 1 can be seen on *Table A-11*, and the RJ45 Ethernet Connector (USB/RJ45 combo) pin-out of Ethernet 2 (optional) can be seen on *Table A-12*.

### **Serial Ports**

The Gator ATX has two fixed RS-232 serial ports SER A and SER B (RS-422/485 optional).

#### **TIA/EIA-232**

RS is the abbreviation for recommended standard. Usually, it is based on or is identical to other standards, e.g., EIA/TIA-232-F. TIA/EIA-232, previously known as RS-232 was developed in the 1960's to interconnect layers of the interface (ITU-T V.11), but also the pignut of the appropriate connectors (25-pin D-type or 9-pin DB9S) (ISO 2210) and the protocol (ISSUED-T V.24). The interface standard specifies also handshake and control lines in addition to the 2 unidirectional receive data line (RD) and transmit data line (TD). The control lines data carrier detect (DCD), data set ready (DSR), request to send (RTS), clear to send (CTS), data terminal ready (DTR), and the ring indicator (RI) might be used, but do not necessarily have to be (for example, the PC-serial-mouse utilizes only RI, TD, RD and GND). Although the standard supports only low speed data rates and line length of approximately 20 m maximum, it is still widely used. This is due to its simplicity and low cost.

#### **Electrical**

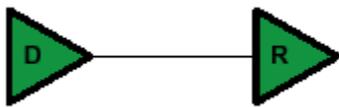
TIA/EIA-232 has high signal amplitudes of  $\pm(5\text{ V to }15\text{ V})$  at the driver output. The triggering of the receiver depends on the sign of the input voltage: that is, it senses whether the input is above 3 V or less than -3 V. The line length is limited by the allowable capacitive load of less than 2500 pF. This results in a line length of approximately 20 m. The maximum slope of the signal is limited to 30 V/ms. The intention here is to limit any reflections that can occur to the rise-and fall-times of the signal. Therefore, transmission line theory does not need to be applied, so no impedance matching and termination measures are necessary.

Do not connect termination resistor when operating in RS-232 mode.

## Protocol

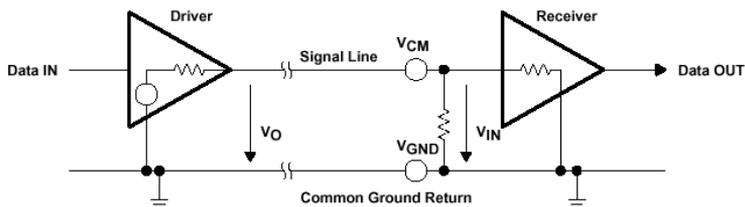
Different from other purely electrical-layer-standards, TIA/EIA-232 defines not only the physical layer of the interface (ITU-T V.11), but also the pinout of the appropriate connectors (25-pin D-type or 9-pin DB9S) (ISO 2210) and the protocol (ITU-T V.24). The interface standard specifies also handshake and control lines in addition to the 2 unidirectional receive data line (RD) and transmit data line (TD). The control lines might be used, but do not necessarily have to be.

## RS-232 is Single-Ended Point-to-point Transmission



Single-Ended, Point-to-Point

Single-ended transmission is performed on one signal line, and the logical state is interpreted with respect to ground. For simple, low-speed interfaces, a common ground return path is sufficient; for more advanced interfaces featuring higher speeds and heavier loads, a single return path for each signaling line (twisted pair cable) is recommended. The figure below shows the electrical schematic diagram of a single-ended transmission system.



## Advantages of Single-Ended Transmission

The advantages of single-ended transmission are simplicity and low cost of implementation. A single-ended system requires only one line per signal. It is therefore ideal for cabling, and connector costs are more important than the data transfer rate, e.g. PC, parallel printer port or serial communication with many handshaking lines, e.g. EIA-232. Cabling costs can be kept to a minimum with short distance communication, depending on data throughput, requiring no more than

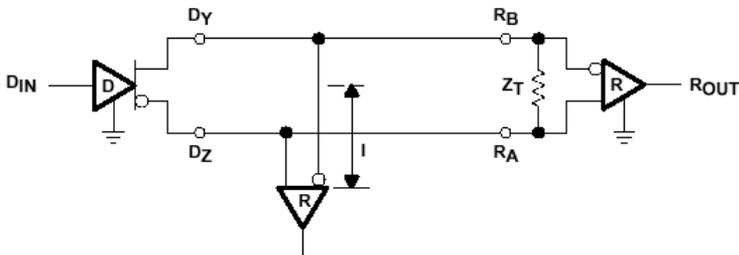
a low cost ribbon cable. For longer distances and/or noisy environments, shielding and additional ground lines are essential. Twisted pair cables are recommended for line lengths of more than 1 meter.

### TIA/EIA-422

TIA/EIA-422 (RS-422) allows a multi-drop interconnection of one driver, transmitting unidirectionally to up to 10 receivers. Although it is not capable of bidirectional transfer, it is still applicable and used for talker-audience scenarios.

### Electrical

TIA/EIA-422 (ITU-T V.11) is comparable to TIA/EIA-485. It is limited to unidirectional data traffic and is **terminated only at the line-end opposite to the driver**. The maximum line length is 1200m, the maximum data rate is determined by the signal rise- and fall-times at the receiver's side (requirement: <10% of bit duration). TIA/EIA-422 allows up to ten receivers (input impedance of 4 k $\Omega$  attached to one driver. The maximum load is limited to 80  $\Omega$ . Although any TIA/EIA-485 transceiver can be used in a TIA/EIA-422 system, dedicated TIA/EIA-422 circuits are not feasible for TIA/EIA-485, due to short circuit current limitations. The TIA/EIA-422 standard requires only short circuit limitation to 150 mA to ground, while TIA/EIA-485 additionally has to limit short circuit currents to 250 mA from the bus pins to -7 V and 12 V to address malfunctions in combination with ground shifts.

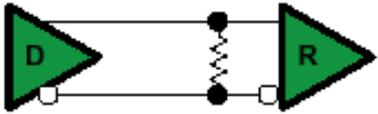


**RS-422 is terminated only at the line-end opposite to the driver even if there is only one receiver.**

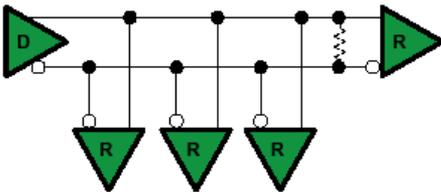
### Protocol

Not applicable/none specified.

**RS-422 is Differential and may be either Point-to-Point or Multi-Drop Connected**



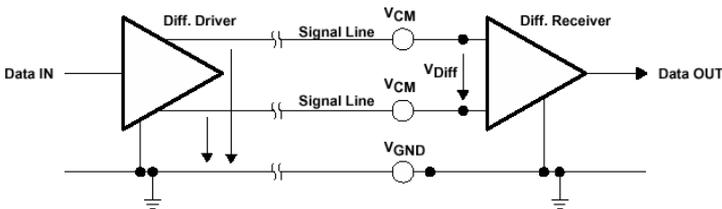
Differential, Point-to-Point



Differential, Multi-Drop

### Differential Transmission

For balanced or differential transmission, a pair of signal lines is necessary for each channel. On one line, a true signal is transmitted, while on the second one, the inverted signal is transmitted. The receiver detects voltage difference between the inputs and switches the output depending on which input line is more positive. As shown below, there is additionally a ground return path.



Balanced interface circuits consist of a generator with differential outputs and a receiver with differential inputs. Better noise performance stems from the fact that noise is coupled into both wires of

the signal pair in much the same way and is common to both signals. Due to the common mode rejection capability of a differential amplifier, this noise will be rejected. Additionally, since the signal line emits the opposite signal like the adjacent signal return line, the emissions cancel each other. This is true in any case for crosstalk from and to neighboring signal lines. It is also true for noise from other sources as long as the common mode voltage does not go beyond the common mode range of the receiver. Since ground noise is also common to both signals, the receiver rejects this noise as well. The twisted pair cable used in these interfaces in combination with a correct line termination—to avoid line reflections—allows very high data rates and a cable length of up to 1200 m.

### **Advantages of Differential Transmission**

Differential data transmission schemes are less susceptible to common-mode noise than single-ended schemes. Because this kind of transmission uses two wires with opposite current and voltage swings compared to only one wire for single-ended, any external noise is coupled onto the two wires as a common mode voltage and is rejected by the receivers. This two-wire approach with opposite current and voltage swings also radiates less electro-magnetic interference (EMI) noise than single-ended signals due to the canceling of magnetic fields.

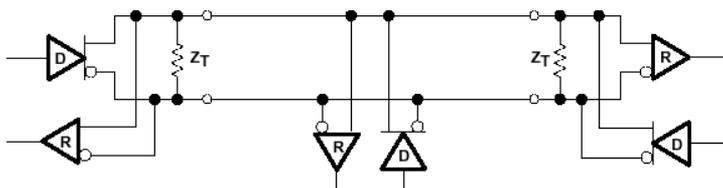
### **TIA/EIA-485**

Historically, TIA/EIA-422 was on the market before TIA/EIA-485. Due to the lack of bi-directional capabilities, a new standard adding this feature was created: TIA/EIA-485. The standard (TIA/EIA-485-A or ISO/IEC 8284) defines the electrical characteristics of the interconnection, including driver, line, and receiver. It allows data rates in the range of 35 Mbps and above and line lengths of up to 1200 m. Of course both limits can not be reached at the same time. Furthermore, recommendations are given regarding wiring and termination. The specification does not give any advice on the connector or any protocol requirements.

### **Electrical**

TIA/EIA-485 describes a half-duplex, differential transmission on cable lengths of up to 1200 m and at data rates of typically up to 35 Mbps (requirement similar to TIA/EIA-422, but  $t_r < 30\%$  of the bit duration, there are also faster devices available, suited for higher rates

under certain load-conditions). The standard allows a maximum of 32 unit loads of  $12\text{ k}\Omega$ , equal to 32 standard nodes or even higher count with increased input impedance. The maximum total load should not drop below  $52\ \Omega$ . The common-mode voltage levels on the bus have to maintain between  $-7\text{ V}$  and  $12\text{ V}$ . The receivers have to be capable to detect a differential input signal as low as  $200\text{ mV}$ .

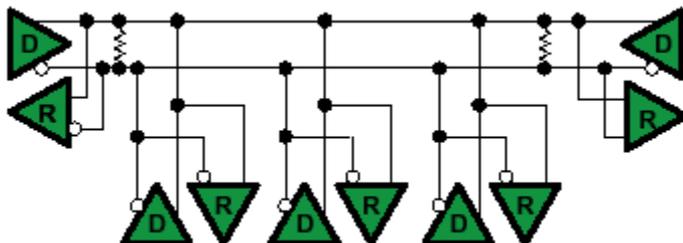


**RS-485 is terminated at both sides of the common bus, even if only two stations are connected to the backbone.**

### Protocol

Not applicable/none specified; exceptions: SCSI systems and the DIN-Bus DIN66348.

### RS-485 is Differential and Multi-Point Connected



### Differential Transmission

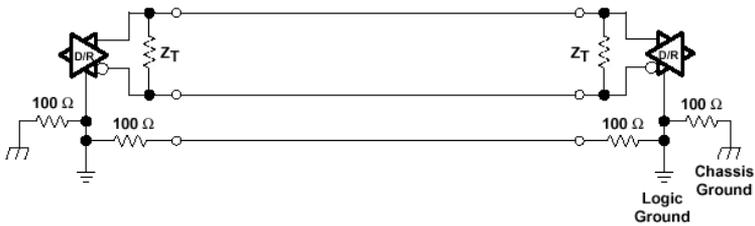
Please, read the Differential Transmission explanation in the previous RS-422 section.

## Termination Resistors

Follow instructions in the previous RS-422 and RS-485 sections. The termination resistors available are rated to  $120\Omega$ .

## Ground Connections

All 422- and 485-compliant system configurations shown up to this point do not have incorporated signal-return paths to ground. Obviously, having a solid ground connection so that both receivers and drivers can talk error free is imperative. The figure below shows how to make this connection and recommends adding some resistance between logic and chassis ground to avoid excess ground-loop currents. Logic ground does not have any resistance in its path from the driver or receiver. A potential problem might exist, especially during transients, when a high-voltage potential between the remote grounds could develop. Therefore, some resistance between them is recommended.



# **Appendix D**

# **On-Board Video Controller**

The Gator ATX has an On-board video controller. The On-board video controller is based on the Intel 82845GE GMCH.

## **82845GE GMCH Integrated Graphics Support**

The 82845GE GMCH provides a highly integrated graphics accelerator while allowing a flexible integrated system graphics solution. High-bandwidth access to data is provided through the system memory port. The GMCH can access graphics data located in system memory at 2.1 GB/s (DDR266). The GMCH uses Intel's Direct Memory Execution model to fetch textures from system memory. The GMCH includes a cache controller to avoid frequent memory fetches of recently used texture data.

The GMCH is able to drive an integrated DAC, and/or two DVO ports (multiplexed with AGP) capable of driving an ADD card. The DAC is capable of driving a standard progressive scan analog monitor with resolutions up to 2048x1536 at 60 Hz. The DVO ports are capable of driving a variety of TV-Out, TMDS, and LVDS transmitters.

The GMCH's IGD contains several functional units. The major components in the IGD are the graphics engines, planes, pipe, and ports. The GMCH has a 3D/2D Instruction Processing unit to control the 3D and 2D engines. Data is input to the IGD's 2D and 3D engines from the system memory controller. The output of the engines are surfaces sent to memory, which are then retrieved and processed by GMCH's planes.

The GMCH contains a variety of planes (e.g., primary display, overlay, cursor, and VGA). The IGD does not support VGA memory accesses during graphics accelerator operations (e.g., 2D and 3D engine activity). The Intel graphics driver controls VGA and high-resolution graphics interaction. VGA and high resolution interaction will remain exclusive. A plane consists of a rectangular shaped image that has characteristics such as source, size, position, method, and format. These planes get attached to source surfaces that are rectangular memory surfaces with a similar set of characteristics. They are also associated with a destination pipe. A pipe consists of a set of combined planes and

a timing generator. The GMCH has a single display pipe, which means that the GMCH can support a single display stream. A port is the destination for the result of the pipe. The GMCH contains three display ports, one analog (DAC), and two digital (DVO ports B and C). The ports will be explained in more detail in a subsequent section.

The entire IGD is fed with data from the memory controller. The performance of the IGD is directly related to the amount of bandwidth available. If the engines are not receiving data fast enough from the memory controller, the rest of the IGD will also be affected.

### **Display Interfaces**

The 82845GE GMCH has three display ports, one analog and two digital. Each port can transmit data according to one or more protocols. The digital ports are connected to an external device that converts one protocol to another. Examples of this are TV encoders, external DACs, LVDS transmitters, and TMDS transmitters. Each display port has control signals that may be used to control, configure, and/or determine the capabilities of an external device.

The GMCH has one dedicated display port, the analog port. DVO ports B and C are multiplexed with the AGP interface. When a system utilizes an AGP connector, DVO ports B and C can be utilized via an ADD (AGP Digital Display) card. Ports B and C can also operate in dual-channel mode, where the data bus is connected to both display ports, allowing a single device to take data at twice the pixel rate.

The GMCH's analog port uses an integrated 350 MHz RAMDAC that can directly drive a standard progressive scan analog monitor up to a resolution of 2048x1536 pixels with 32-bit color at 60 Hz.

The GMCH's DVO ports are each capable of driving a 165 MHz pixel clock. Each port is capable of driving a digital display up to 1600x1200 at 60 Hz. When in dual-channel mode, the GMCH can drive a flat panel up to 2048x1536 at 60 Hz or dCRT/HDTV up to 1920x1080 at 85 Hz.

The GMCH is compliant with *Digital Visual Interface (DVI) Specification, Revision 1.0*. When combined with a DVI compliant external device and connector, the GMCH has a high-speed interface to a digital display (e.g., flat panel or digital CRT).

## **Analog Display Port Characteristics**

The analog display port provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated DDC signal pair that is implemented using GPIO pins dedicated to the analog port. The intended target device is for a CRT-based monitor with a VGA connector. Display devices such as LCD panels with analog inputs may work satisfactory but no functionality has been added to the signals to enhance that capability.

## **Integrated RAMDAC**

The display function contains a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics and video subsystems to analog data for the CRT monitor. The GMCH's integrated 350 MHz RAMDAC supports resolutions up to 1920x1080 at 85 Hz and 2048x1536 at 60 Hz. Three 8-bit DACs provide the R, G, and B signals to the monitor.

## **VESA/VGA Mode**

VESA/VGA mode provides compatibility for pre-existing software that sets the display mode using the VGA CRTC registers. Timings are generated based on the VGA register values and the timing generator registers are not used.

## **DDC (Display Data Channel)**

DDC is a standard defined by VESA. Its purpose is to allow communication between the host system and display. Both configuration and control information can be exchanged allowing plug-and-play systems to be realized. Support for DDC 1 and 2 is implemented. The GMCH uses the DDCA\_Clk and Data to communicate with the analog monitor.

## **Digital Display Interface**

The GMCH has several options for driving digital displays. The GMCH contains two DVO ports that are multiplexed on the AGP interface. When an external AGP graphics accelerator is not present, the GMCH can use the multiplexed DVO ports to provide extra digital display options. These additional digital display capabilities may be

provided through an ADD card, which is designed to plug in to a 1.5 V AGP connector.

### **Digital Display Channels – DVOB and DVOC**

The shared DVO ports each support a pixel clock up to 165 MHz and can support a variety of transmission devices. When using a 24-bit external transmitter, it will be possible to pair the two DVO ports in dual-channel mode to support a single digital display with higher resolutions and refresh rates. In this mode, the GMCH is capable of driving pixel clock up to 330 MHz.

### **ADD Card**

The multiplexed DVO ports can be used via an ADD card. The ADD card fits in a 1.5 V AGP connector.

### **TMDS Capabilities**

The GMCH is compliant with *Digital Visual Interface (DVI) Specification, Revision 1.0*. When combined with a DVI compliant external device and connector, the GMCH has a high-speed interface to a digital display (e.g., flat panel or digital CRT). When combining the two multiplexed DVO ports, the GMCH can drive a flat panel up to 2048x1536 at 60 Hz or a dCRT/HDTV up to 1920x1080 at 85 Hz. Flat Panel is a fixed resolution display. While the GMCH has no native panel fitting capabilities, it supports panel fitting in the transmitter, receiver, or an external device. The GMCH, however, provides unscaled mode where the display is centered on the panel.

### **LVDS Capabilities**

The GMCH can use the multiplexed DVO ports to drive an LVDS transmitter. A Flat Panel is a fixed resolution display. While the GMCH has no native panel fitting capabilities, it supports panel fitting in the transmitter, receiver, or an external device. The GMCH provides unscaled mode where the display is centered on the panel. The GMCH supports scaling in the LVDS transmitter through the DVOB (or DVOC)\_STL pin, multiplexed with DVOB (or DVOC)\_FLD.

*LVDS module solution available from the Gator ATX manufacturer.*

## **TV-Out Capabilities**

While traditional TVs are not digital displays, the GMCH uses a digital display channel to communicate with a TV-Out transmitter. For that reason, the GMCH considers a TV-Output to be a digital display. The GMCH supports NTSC/PAL/SECAM standard definition formats. The GMCH generates the proper timing for the external encoder.

## **DDC (Display Data Channel)**

The GMCH supports the DDC2B protocol to initiate the transfer of EDID data. The multiplexed digital display interface uses the M\_I2C bus to interrogate the external transmitter.

## **Optional High Speed (Dual-Channel) Interface**

The multiplexed digital display ports can operate in a single 24-bit mode. The 24-bit mode uses the 12-bit DVOC data pins combined with the DVOB data pins to make a 24-bit bus. This doubles the transfer rate capabilities of the port. In the single port case, horizontal periods have a granularity of a single pixel clock; in the double case, horizontal periods have a granularity of two pixel clocks. In both cases, data is transferred on both edges of the differential clock. The GMCH can output the data in a high-low fashion, with the lower 12 bits of the pixel on one DVO port and the upper 12 bits of data on the other DVO port. In this manner, the GMCH transfers an entire pixel per clock edge (2 pixels per clock). In addition to this, the GMCH also can transfer dual-channel data in odd-even format. In this mode, the GMCH transfers all odd pixels on DVOC and all even pixels on DVOB. In this format, each DVO port sees both the high and low half of the pixel, but only sees half of the pixels transferred. As in high-low mode, two full pixels are transferred per clock period. The high-low ordering within each pixel can be modified through DVO control registers.

## **DVO Modes**

In single-channel mode, the order of pixel transmission (high-low vs. low-high) can be adjusted via the data ordering bit of that DVO port's control register. As mentioned above, when in dual-channel mode, the GMCH can transmit data in a high-low or odd-even format. In high-low mode, software can choose which half goes to which port. A 0 = DVOB Lo/DVOC Hi, and a 1 = DVOB Hi/ DVOC Lo. In odd/even mode, the odd pixels will always go out to DVOC and even pixels will

always go out to DVOB. Which DVO port is even and which is odd cannot be switched, but the data order bit can be used to change the active data order within the even and odd pixels. The GMCH considers the first pixel to be pixel zero and sends it out to DVOB.

### **Synchronous Display**

Microsoft Windows\* 98 and Windows\* 2000 have enabled support for multi-monitor display. Synchronous mode will display the same information on multiple displays. Since the GMCH has several display ports available for its single pipe, it can support synchronous display on two displays, unless one of the displays is a TV. No synchronous display is available when a TV is in use. The GMCH does not support two synchronous digital displays. The GMCH cannot drive multiple displays concurrently (different data or timings). In addition, the GMCH cannot operate in parallel with an external AGP device. The GMCH can, however, work in conjunction with a PCI graphics adapter.

Connectors J23 (AGP/ADD), J25 (DVO) and J1 (VGA) have standard industry pin outs.

**User's Notes:**

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**MN-G4GAX-01**