User Manual

MIO-2261

Intel® Atom™ N2600/ N2800 Pico-ITX SBC, DDR3, 18/24-bit LVDS, VGA, 1 GbE, Half-size Mini

PCIe, 4 USB, 2 COM, SMBus, I^{2}C, mSATA & MIOe

Copyright

The documentation and the software included with this product are copyrighted 2012 by Advantech Co., Ltd. All rights are reserved. Advantech Co., Ltd. reserves the right to make improvements in the products described in this manual at any time without notice.

No part of this manual may be reproduced, copied, translated or transmitted in any form or by any means without the prior written permission of Advantech Co., Ltd. Information provided in this manual is intended to be accurate and reliable. However, Advantech Co., Ltd. assumes no responsibility for its use, nor for any infringements of the rights of third parties, which may result from its use.

Acknowledgements

AMI is a trademark of AMI Software International, Inc.

Intel® is a trademark of Intel® Technologies, Inc.

IBM, PC/AT, PS/2 and VGA are trademarks of International Business Machines Corporation.

Intel and Atom® are trademarks of Intel Corporation.

Microsoft Windows® is a registered trademark of Microsoft Corp.

RTL is a trademark of Realtek Semi-Conductor Co., Ltd.

ESS is a trademark of ESS Technology, Inc.

UMC is a trademark of United Microelectronics Corporation.

SMI is a trademark of Silicon Motion, Inc.

Creative is a trademark of Creative Technology LTD.

All other product names or trademarks are properties of their respective owners.

Product Warranty (1 year)

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Please consult your dealer for more details.

If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages you get when the problem occurs.

2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.

3. If your product is diagnosed as defective, obtain an RMA (return merchandize authorization) number from your dealer. This allows us to process your return more quickly.

4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.

5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Technical Support and Assistance

1. Visit the Advantech web site at www.advantech.com/support where you can find the latest information about the product.

2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
   – Product name and serial number
   – Description of your peripheral attachments
   – Description of your software (operating system, version, application software, etc.)
   – A complete description of the problem
   – The exact wording of any error messages

Packing List

Before installation, please ensure the following items have been shipped:

Item Part Number

- 1 MIO-2261 SBC
- 1 Startup manual
- 1 Utility CD (User Manual & Driver)
- Cables

Part Number	Description
1700006291	SATA cable 7P 30 cm w/ right angle
1700019156	Audio Cable 2*5P-2.0/JACK*2 20cm
1701200220	COM PORT cable 2*10P-2.0/D-SUB 9P(M)*2 22 cm
1700019656	SATA Power cable 5P-1.25/5P-2.0+SATA 5P 15 cm
1700002172	USB cable 2.0mm pitch USB-A(F) 17cm
1700019705	AT Power cable 12cm

- Heatsink:

1960055792T001	99.5 x 70.5 x 15.7 mm

- Stud & Screw

Part Number	Description
9666226000E	Stud and screw pack, including:
1910002088	Stud F=M3*10L M=M3*5L B=5 H=16, 4 pcs
1935032000	Screw R/S 5.5 2.0 +M M3*20L, 4 pcs
193B0204C0	Screw F/S D=3.5 H=0.8 + M2*4L, 1 pcs

Ordering Information

Model Number	Description
MIO-2261N-S6A1E	Intel® Atom™ N2600, fanless, LVDS, VGA, Gigabit Ethernet, 4 USB, mSATA, SMBus, GPIO, 2 COM, mini PCIe, MIOe
MIO-2261N-S8A1E	Intel® Atom™ N2800, fanless, LVDS, VGA, Gigabit Ethernet, 4 USB, mSATA, SMBus, GPIO, 2 COM, mini PCIe, MIOe

Optional Accessories

Part No.	Description
1960055791T001	Heat Spreader (99.5 x 70.5 x 11.2 mm)

Declaration of Conformity

This device complies with the requirements in part 15 of the FCC rules: Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation

FCC Class A

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this device in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his/her own expense. The user is advised that any equipment changes or modifications not expressly approved by the party responsible for compliance would void the compliance to FCC regulations and therefore, the user's authority to operate the equipment.

Caution! *There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.*

Safety Instructions

1. Read these safety instructions carefully.
2. Keep this User Manual for later reference.
3. Disconnect this equipment from any AC outlet before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.
4. For plug-in equipment, the power outlet socket must be located near the equipment and must be easily accessible.
5. Keep this equipment away from humidity.
6. Put this equipment on a reliable surface during installation. Dropping it or letting it fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. DO NOT COVER THE OPENINGS.
8. Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.
9. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.
12. Never pour any liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If one of the following situations arises, get the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated into the equipment.
    - The equipment has been exposed to moisture.
    - The equipment does not work well, or you cannot get it to work according to the user's manual.
    - The equipment has been dropped and damaged.
    - The equipment has obvious signs of breakage.
15. DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -20° C (-4° F) OR ABOVE 60° C (140° F). THIS COULD DAMAGE THE EQUIPMENT. THE EQUIPMENT SHOULD BE IN A CONTROLLED ENVIRONMENT.
16. CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER, DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS.

The sound pressure level at the operator's position according to IEC 704-1:1982 is no more than 70 dB (A).

DISCLAIMER: This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.
- Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a card may damage sensitive electronic components.

Contents

Chapter 4   S/W Introduction & Installation........ 35

Appendix A   PIN Assignments 45

Appendix B   WDT & GPIO 65

Appendix C   System Assignments........................ 69

Chapter 1

General Introduction

This chapter gives background information on the MIO-2261.

Sections include:

- Introduction
- Product Features
- Specifications

1.1 Introduction

MIO-2261 is a MI/O-Ultra SBC (Single Board Computer) with Embedded Intel® Atom™ N2600 1.6 GHz and N2800 1.86 GHz Processor. The MIO-2261 can support DDR3 memory up to 4 GB, has four USB 2.0 compatible ports, one GbE (up to 1000 Mbps) interface, LVDS and VGA support, HD (High Definition) audio, and one half size mini-PCIe and MIOe expansion slot. In addition, MIO-2261 also supports one SATA drive, two COM ports, one SMBus, one GPIO and one mSATA slot. Advantech's innovative MI/O (multiple I/O) Extension SBC is equipped with flexible multiple I/O to assist integrators in developing optimized solutions.

1.2 Specifications

1.2.1 General Specifications

- **CPU:** Intel® Atom™ processor N2600 / N2800
- **System Chipset** Intel® Atom™ N2600 / N2800 + NM10
- **BIOS:** AMI EFI 16 Mbit Flash BIOS
- **System Memory:** DDR3 800 MHz(N2600), 1066 MHz (N2800) up to 4 GB
- **Watchdog Timer:** Single chip Watchdog 255-level interval timer, setup by software
- **Expansion Interface:**
  - 1 x half size mini-PCIe slot
  - 1 x MIOe connector: supports 2 x USB 2.0, 2 x PCIe x1, LPC, HD Audio line-out, SMBus, DP (or HDMI, supported by request), 5 Vsb/12 Vsb power
- **Battery:** Lithium 3 V / 210 mAH

I/O
- **Internal I/O interface:** 2 x USB2.0, 2 x RS-232, 1 x HD Audio (line in, line out), GPIO, SMBus, I^2C (supported by request, share with SMBus pin)
- **Rear I/O ports:** 1 x RJ45 Ethernet, 1 x VGA, 2 x USB, 1 x Power connector (or DC jack, supported by request):

Ethernet
- **Controller:** Intel 82583V (GbE1)
- **Speed:** 10/100/1000 Mbps
- **Connector:** 1 x RJ45
- **Standard:** Compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3x, IEEE 8023y, IEEE 802.ab
- Support wake-on-LAN

Display
- **Controller:** Intel® Atom™ N2600/ N2800, Directx* 9 and OpenGL 3.0 support
- **Resolution:**
  - VGA: 1920 x 1200 60 Hz at 267 MHz Max
  - LVDS: 18/24-bit LVDS1, up to 1366 x 768

1.2.2 Functional Specifications

Processor

Processor	■ Intel® Atom™ Processor N2600/ N2800
	■ Frequency
	  – - N2600 1.6 GHz
	  – - N2800 1.86 GHz
	■ Manufacturing Technology: 32 nm
	■ L2 catch: 1 MB

Memory	■ Supports DDR3 800 MHz (N2600), DDR3 1066 MHz (N2800), up to 4 GB ■ SODIMM Socket: 204-pin SODIMM socket type *1

Graphic Engine	■ Directx* 9 compliant Pixel Shader 2.0 and OGL 3.0 support
	■ Hardware decode/ acceleration:
	  – MPEG2 (VLD / iDCT / MC)
	  – WMV9
	  – MPEG4 Part 10 (AVC/ H.264)
	  – VC-1

Display	■ VGA: 1920 x 1200 (WUXGA) @ 60Hz ■ LVDS1: 18/24-bit, up to 1366 x 768 (WXGA) @ 60 Hz ■ Dual independent display: LVDS + VGA

Chipset

Control Hub	■ Intel® NM10
Audio	■ High Definition Audio (HD) ALC892 codec ■ Up to 2 channel of PCM (Pulse Code Modulation) audio output ■ Connectors: Line-out, Line-in
PCI-Express Interface	■ 4 PCI-Express x1 Lanes ■ Lane 1: Intel 82583V GbE controller ■ Lane 2: Half-size Mini PCIe connector ■ Lane 3 & 4: MIOe connector
SATA Interface	■ 1 x mSATA by mini-PCIe socket (Integrates USB signal, supports either mSATA or USB interface module) ■ 1 x SATAII (Max. Data transfer Rate 300 MB/s)
USB Interface	■ 2 x internal USB ports ■ 2 x rear I/O ports at coastline ■ Transmission speed up to 480 Mbps
Power Management	■ Full ACPI (Advanced Configuration and Power Interface) 3.0 ■ Supports S1, S3, S4, S5 ■ Support wake on LAN
BIOS	AMI EFI 16 Mbit Flash BIOS via SPI

Others

Ethernet	■ Controller: Intel® 82583V (GbE1)
	 ■ Compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3x, IEEE 8023y, IEEE 802.ab
	 ■ Support 10/100/1000 Mbps
	 ■ Connectors: RJ45
	 ■ LAN1 LED
	   – Link: Green(100Mbps)/ Orange (1000Mbps)
	   – Active: Green (flash)
	 ■ Support wake on LAN

Serial ports	■ Controller: SMSC SCH 3114 ■ 2 x RS-232 serial ports with ESD protection: air gap ± 15 kV, contact ± 8 kV
GPIO	■ Controller: SMSC SCH 3114 ■ 8-Bit (programming) through Super I/O, pin header ■ 5 V tolerance
SMBus	Default is SMBus, I^2C support by request (share pin with SMBus)

1.2.3 Mechanical Specifications

1.2.3.1 Dimensions (mm)
L100.00 mm x W72 mm (3.9" x 2.8")

1.2.3.2 Height on top (mm)
15.7 mm (Heatsink)

1.2.3.3 Height under bottom (mm)
16.4 mm (Rear I/O USB)

1.2.3.4 Weight (g)
42g (0.93 lb, weight of total package)

1.2.4 Electrical Specifications
Power Supply Type: Single 12 V DC power input (support DC power hot plug)

1.2.4.1 Power supply Voltage
■ Single 12 V input ± 10%
■ Total peripheral power supply output: 5 V @ 3 A for CPU board and MIOe module totally, 12 V @ 2 A for MIOe module

1.2.4.2 Power Consumption
■ **Typical in Win7 Idle Mode:**
N2600: 0.35 A @ 12 V (4.2 W)
N2800: 0.46 A@ 12 V (5.52 W)
■ **Max in Win7 HCT12 (10 minutes):**
N2600: 0.76 A @ 12 V (9.12 W)
N2800: 0.80 A @ 12 V (9.6 W)

1.2.4.3 RTC Battery
■ **Typical Voltage:** 3.0 V

■ **Normal discharge capacity:** 210 mAh

1.2.5 Environmental Specifications

1.2.5.1 Operating Humidity
40 °C @ 95% RH Non-Condensing

1.2.5.2 Operating Temperature
0 ~ 60 °C (32~140 °F)

1.2.5.3 Storage Humidity
60 °C @ 95% RH Non-Condensing

1.2.5.4 Storage Temperature
-40 ~ 85 °C (-40 ~ 185 °F)

Chapter 2

H/W Installation

This chapter explains the setup procedures of the MIO-2261 hardware, including instructions on setting jumpers and connecting peripherals, as well as switches, indicators and mechanical drawings. Be sure to read all safety precautions before you begin the installation procedure.

2.1 Jumpers

2.1.1 Jumper Description

Cards can be configured by setting jumpers. A jumper is a metal bridge used to close an electric circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To close a jumper, you connect the pins with the clip. To open a jumper, you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2, or 2 and 3.
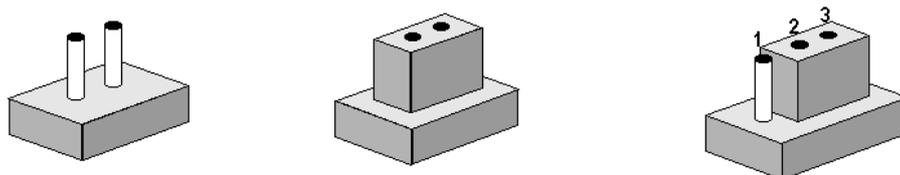
The jumper settings are schematically depicted in this manual as follows.

A pair of needle-nose pliers may be helpful when working with jumpers. If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

Generally, you simply need a standard cable to make most connections.

Warning! *To avoid damaging the computer, always turn off the power supply before setting jumpers.*

2.1.2 Jumper list

Table 2.1: Jumper List	
J1	LCD Power / Auto Power on

2.1.3 Jumper Settings

Table 2.2: J1: LCD Power/Auto Power on	
Part Number	1653003260
Footprint	HD_3x2P_79
Description	PIN HEADER 3*2P 180D(M) 2.0mm SMD SOUARE PIN
Setting	**Function**
(1-2)	+5V
(3-4) (default)	+3.3V
(5-6) (default)	Auto Power On
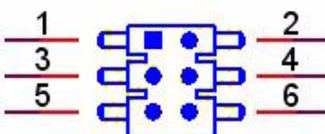
2.2   Connectors

2.2.1   Connector list

CN1	12 V Power Input
CN2	DC JACK (by request)
CN3	DDR3 SO-DIMM
CN4	GPIO
CN5	VGA
CN6	mSATA
CN7	SATA
CN8	Mini PCIe
CN9	External USB
CN10	Internal USB
CN11	COM1/COM2
CN12	SMBus (or I^{2}C, by request)
CN13	Front Panel
CN14	Gigabit Ethernet
CN15	HD Audio
CN16	MIOe
CN17	Inverter Power/Internal SATA Power
CN18	24 bits LVDS Panel
BH1	Battery

2.2.2   Connector Settings

2.2.2.1   Battery Connector (BH1)

MIO-2261 supports Lithium 3 V/210 mAH CR2032 battery with wire via battery connector (BH1).

> *Note!*   *How to clear CMOS: (Must follow below steps)*
>
> *1. Turn off system power*
>
> *2. Unplug CR2032 battery cable on BH1*
>
> *3. Waiting for 15sec or short BH1 pin1-2*
>
> *4. Connect battery cable on BH1*
>
> *5. Turn on system power*

2.2.2.2   12 V Power Input Connector (CN1)

Main power connector supports single 12 V input, and there's an optional choice of **DC/Jack (CN2, co-layout with 2pin power connector)**

2.2.2.3   DDRIII SODIMM Socket (CN3)

One 204-pin/H9.2 mm DDRIII DIMM socket supports DDR3 800 MHz (N2600)/ 1066 MHz (N2800) up to 4 GB.

2.2.2.4   GPIO (General Purpose Input Output) (CN4)

The board supports 8-bit GPIO (5 V tolerance) through GPIO pin header. The 8 digital inputs and outputs can be programmed to read or control devices, with each input or output defined.

2.2.2.5 VGA/LVDS Interface Connections (CN5 and CN18)

The MIO-2261's VGA interface can drive conventional CRT displays and is capable of driving a wide range of flat panel displays, including passive LCD and active LCD displays.The board has two connectors to support these displays: one for standard CRT VGA monitors and one for LVDS type LCD panels.

CRT display connector (CN5)

The CRT display 15pins connector is a rear I/O connector on coastline used for conventional CRT displays. Resolution: up to 1920 x 1200 (WUXGA).

LVDS LCD panel connector (CN18)

The board supports single channel 18/24-bit LVDS LCD panel displays via 14*1pin wafer box. Resolution: up to 1366 x 768 (WXGA).

2.2.2.6 mSATA Connector (CN6)

MIO-2260 provides a mini-PCIe socket which integrates USB and SATAII signals, supports either mSATA or USB interface modules.

2.2.2.7 SATA Connector (CN7)

MIO-2261 features one high performance Serial ATA interfaces. Data transfer rates up to 300 MB/s enabling very fast data and file transfer, and independent DMA operation on two ports.

2.2.2.8 Mini PCIe Connector (CN8)

MIO-2261 supports a half size mini PCIe slot. PCI Express Mini Card (also known as Mini PCI Express, Mini PCIe, and Mini PCI-E) is a replacement for the Mini PCI form factor based on PCI Express. It is developed by the PCI-SIG. The host device supports both PCI Express and USB 2.0 connectivity.

2.2.2.9 USB Connectors (CN9 and CN10)

The board provides four USB (Universal Serial Bus) ports, two are rear I/O on coastline (CN9); and the other two are internal USB ports (CN10). This gives complete Plug and Play, and hot attach/detach for up to 127 external devices. The USB interfaces comply with USB specification Rev. 2.0 which supports 480 Mbps transfer rate and are fuse protected.

2.2.2.10 COM Port Connectors (CN11)

MIO-2261 provides 2 x RS-232 serial ports in 10*2pin pin header. It provides connections for serial devices or a communication network. The pin assignments for the COM port connector can be found in Appendix.

2.2.2.11 SMBus Connector (CN12)

MIO-2261 provides SMBus connector for customer connection to SMBus protocol embedded device. It can be configured to I^2C by customer's request.

Advantech also provide SMBus API allowing developers to interface with an embedded system environment and transfer serial messages using the SMBus protocols, allowing multiple simultaneous device control.

2.2.2.12 Front Panel Connector(CN13)

MIO-2261 integrates below functions as front panel 6pin connector.

Power button

Supports power on/off button in ATX mode.

Reset

If you install a reset switch, it should be an open single pole switch. Momentarily pressing the switch will activate a reset.

Power LED

Power LED indicator would light when power is on.

HDD LED

HDD LED indicator for hard disk access is an active low signal\

2.2.2.13 Gigabit Ethernet Connector (CN14)

MIO-2261 uses Intel® 82583V Ethernet chip (10/100/1000 Mbps) linked to dedicated PCIe x1 lane via RJ-45 connector.

2.2.2.14 High Definition Audio Interface (CN15)

MIO-2261 provides one 5x 2 pin box header for audio device. It can support high definition audio stereo by customized audio module that has codec onboard.

2.2.2.15 MIOe connector (CN16)

MIO-2261 supports MIOe connector to extend flexible I/Os.

Interface

2 x USB 2.0, 2 x PCIe x1, LPC, HD Audio line-out, SMBus, DP (or HDMI, supported by request), 5 Vsb/12 Vsb power.

Total peripheral power supply output

5 V @ 3 A for CPU board and MI/O Extension module totally, 12 V @ 2 A for MI/O Extension module.

2.2.2.16 Inverter Power/Internal SATA Power Connector (CN17)

The LCD inverter is connected to CN17 via a 5-pin connector to provide +5 V/+12 V power to the LCD display, and 5V power can be provided for 2.5" SATA HDD via CN17.

SATA power's current is only sufficient for 2.5" HDD, and LVDS inverter's current is 5 V @ less than 1 A, 12 V @ 500 mA.

2.3 Mechanical

2.3.1 Jumper and Connector Locations
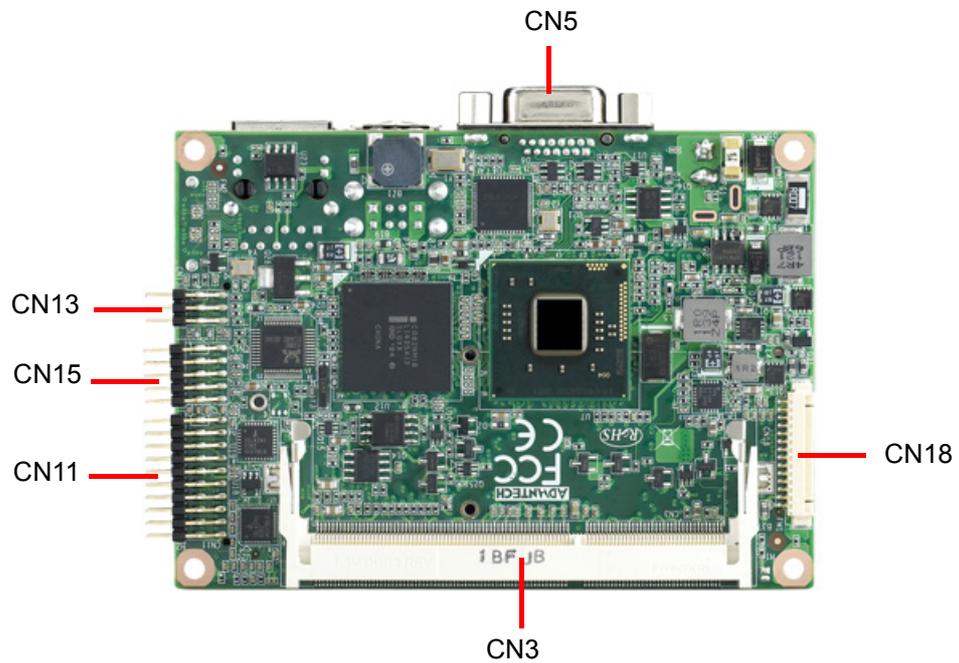
Figure 2.1 Jumper and Connector layout (Top side)
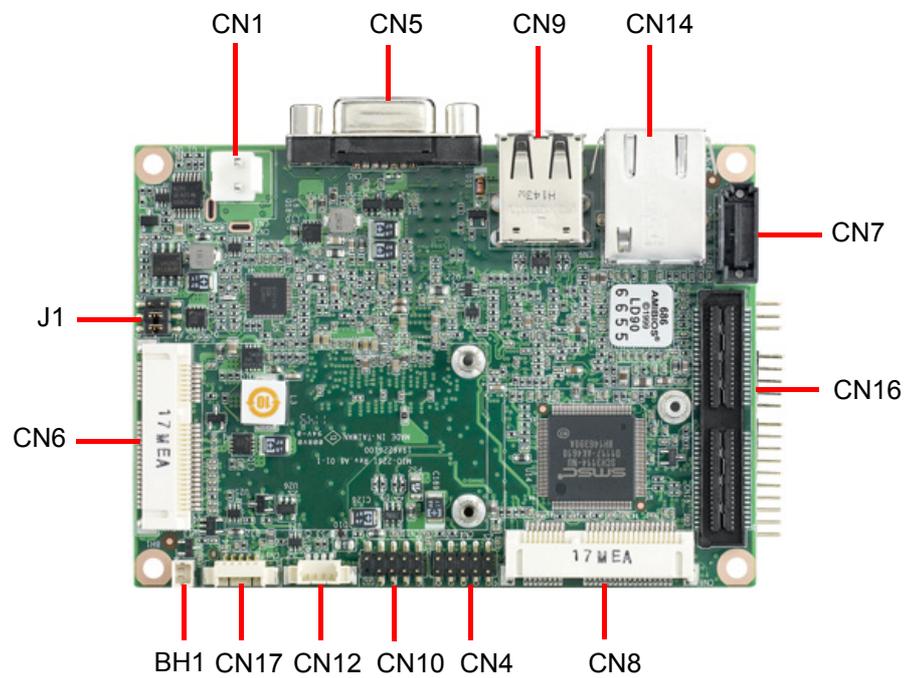
Figure 2.2 Jumper and connector layout (Bottom side)

2.3.2 Board Dimensions

2.3.2.1 CPU Board Drawing
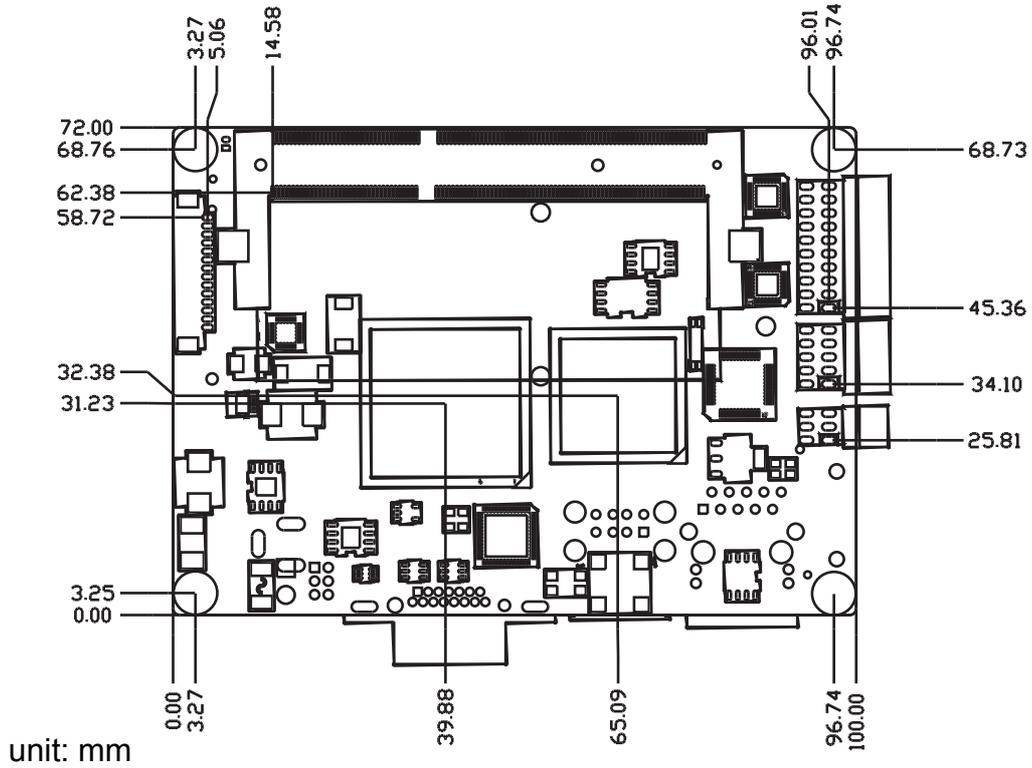
unit: mm

Figure 2.3 Board dimension layout (Top side)

unit: mm

Figure 2.4 Board dimension layout (Bottom side)
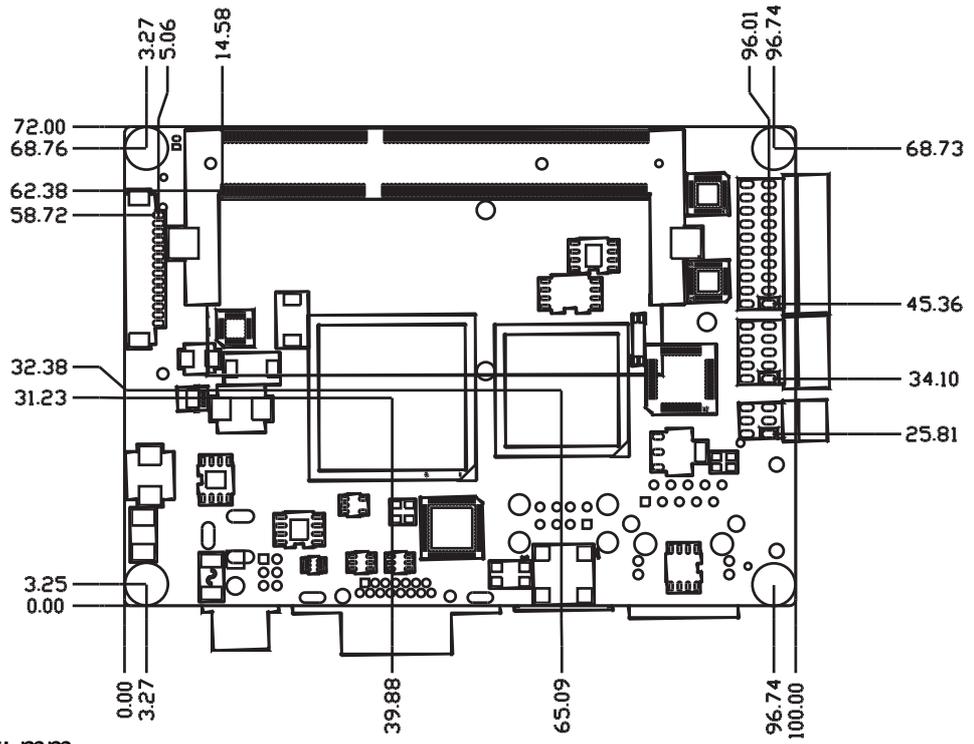
unit: mm

Figure 2.5 Board dimension layout (Top side with optional DC/Jack)
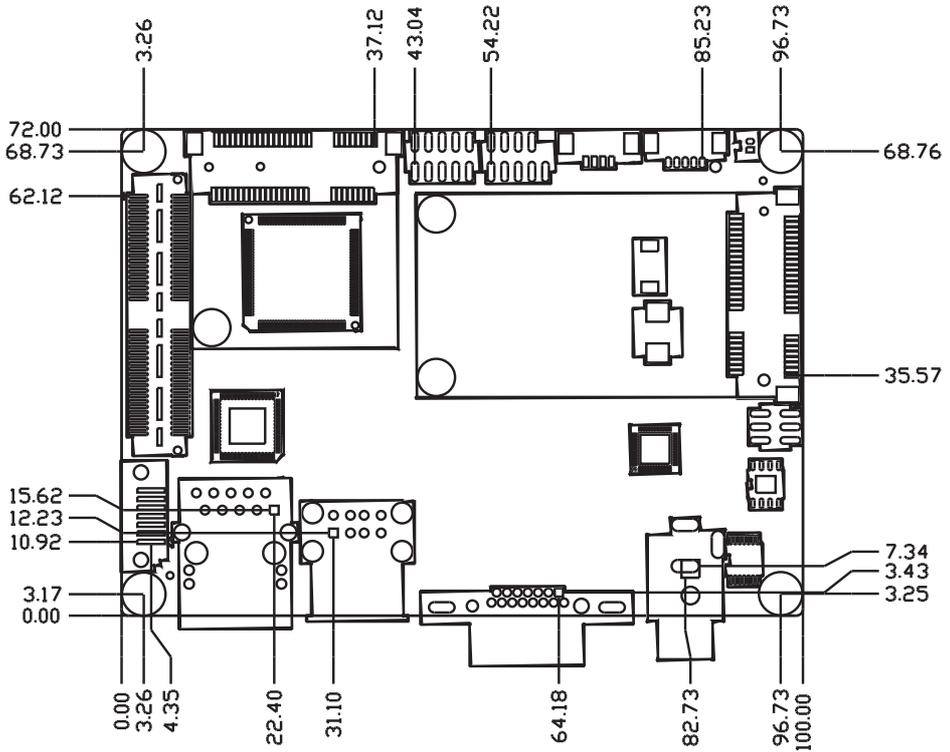
unit: mm

Figure 2.6 Board dimension layout (Bottom side with optional DC/Jack)
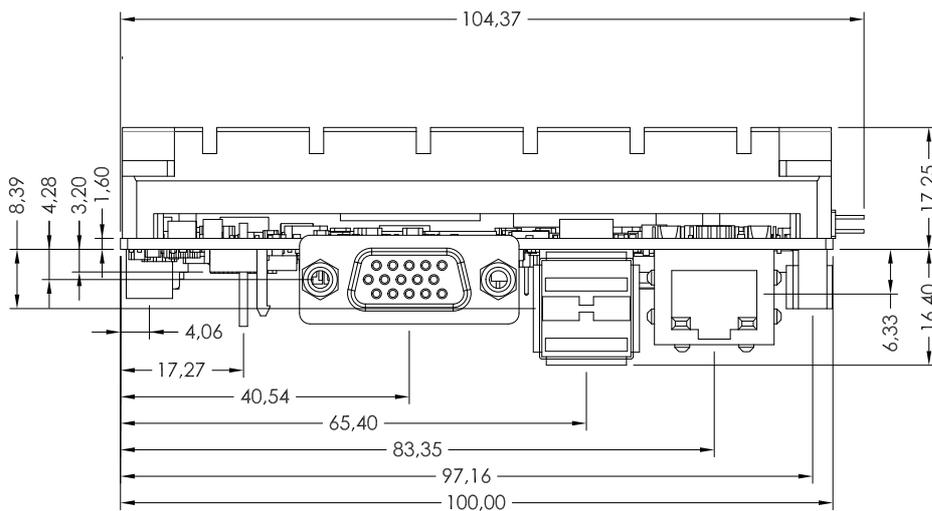
Figure 2.7 Board dimension layout (coastline with power connector and heatsink)
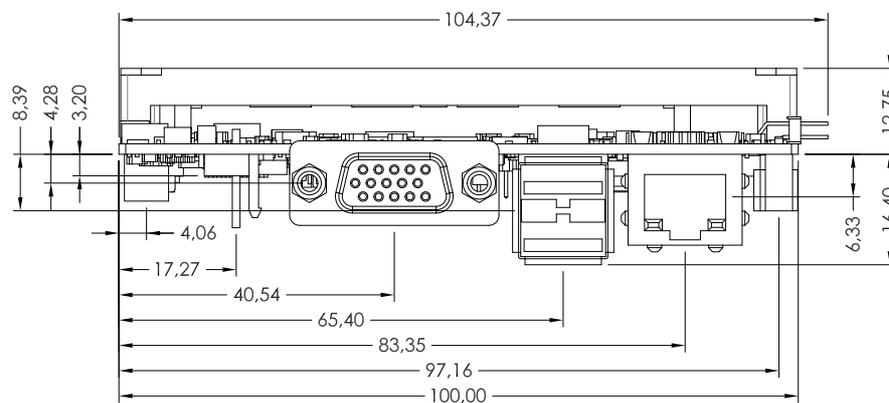
Figure 2.8 Board dimension layout (coastline with Power connector and optional heatspreader)
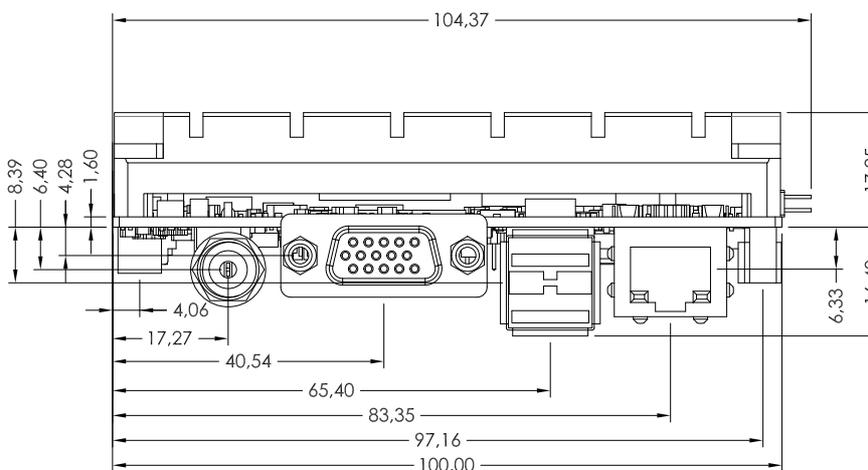
Figure 2.9 Board dimension layout (coastline with heatsink and optional DC/ jack)
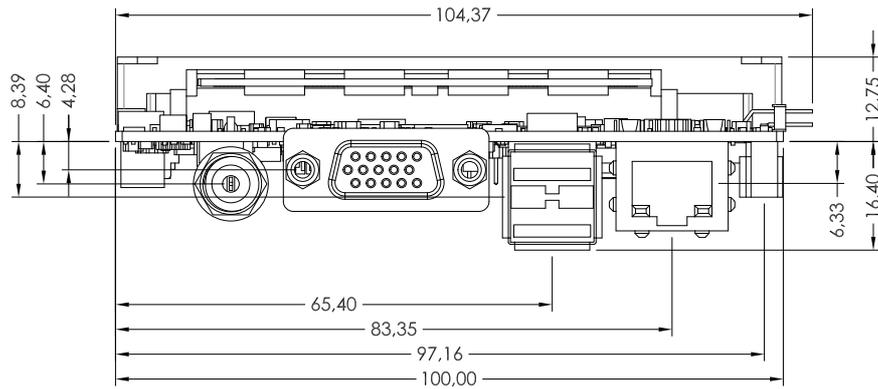
Figure 2.10 Board dimension layout (coastline with optional heatspreader and DC/Jack)

2.3.2.2 MI/O Module Height Constraint

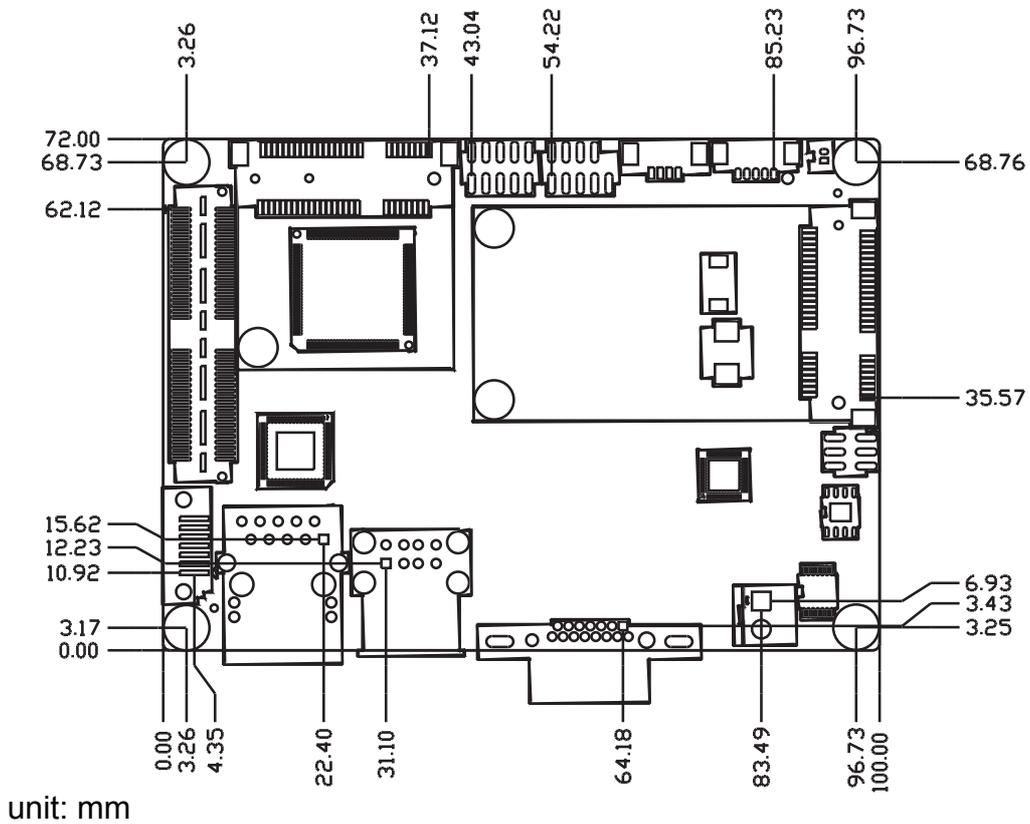To avoid mechanical conflict with MI/O-Ultra CPU board, it's recommended to refer to the following drawing of MI/O module height constraint.

unit: mm
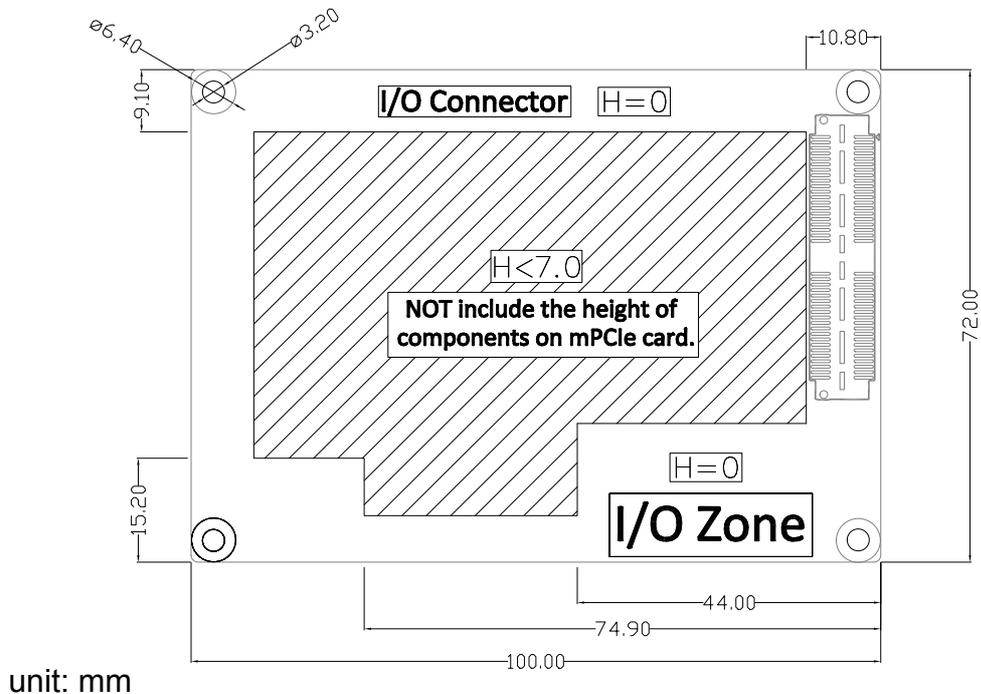
Figure 2.11 MI/O Module height constraint

> **Note!**
>
> 1. Constraint of components' max. height of MI/O module base on 16 mm height MIOe connector. If needed, there's 19 mm height as well.
> 2. The height of power connector (including of cable) on MIO-2261 should be considered when assembling the system or stacking the MI/O module.

2.3.2.3 Another Thermal Solution - Heat Spreader

MIO-2261 has an optional heat spreader to make whole system more compact. Using a heat spreader to conduct heat to your chassis can help a lot when system is extra compact or limited space for heat convection. Here are some guidelines for heat spreader:

1. For best heat conduction, the gap between chassis and heat spreader should be smaller, the smaller the better.

2. The height of existing heat spreader is 11.2mm (Advantech P/N: 1960055791T001). If you need some other height to fit chassis better, Advantech could customize it for you. (Please contact our sales for details)

3. There are thermal grease and screws in heat spreader kit, thermal grease helps conduct better if chassis is quite close to heat spreader. Another suggestion is to use a thermal pad if the chassis isn't close enough to the heat spreader. (The gap is suggested to be less than 3mm for better heat conduction)

Screw hole of your chassis
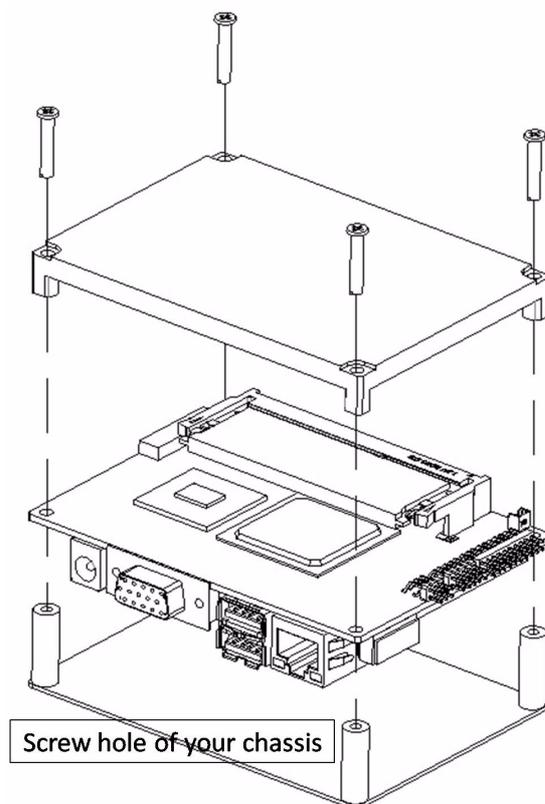
Figure 2.12 Illustration of heat spreader assembly

Chapter   3

BIOS Settings

3.1 BIOS Setup

AMIBIOS has been integrated into many motherboards for over a decade. With the AMIBIOS Setup program, users can modify BIOS settings and control various system features. This chapter describes the basic navigation of the MIO-2261 BIOS setup screens.

Figure 3.1 Setup program initial screen

AMI's BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This information is stored in flash ROM so it retains the Setup information when the power is turned off.

3.2 Entering Setup

Turn on the computer and then press <F2> or <DEL> to enter Setup menu.

3.2.1 Main Setup

When users first enter the BIOS Setup Utility, users will enter the Main setup screen.

Users can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.

Figure 3.2 Main setup screen

The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the key legend.

Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

■ **System time / System date**
Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

3.2.2 Advanced BIOS Features Setup

Select the Advanced tab from the MIO-520 setup screen to enter the Advanced BIOS Setup screen. Users can select any item in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. Users can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screens are shown below. The sub menus are described on the following pages.
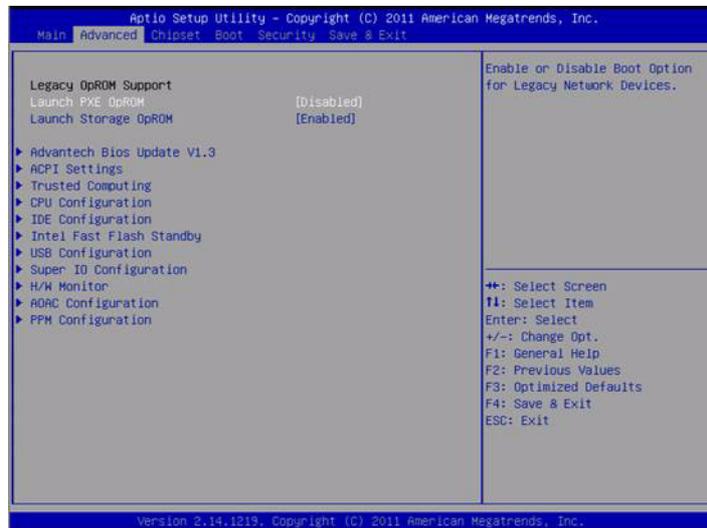
Figure 3.3 Advanced BIOS features setup screen

■ **Launch PXE OpROM**

This item allows users to enable or disable launch PXE OpROM if available.

■ **Launch Storage OpROM**

This item allows users to enable or disable launch storage OpROM if available.

3.2.2.1 Advantech BIOS Update V1.3

This item allows users to flash BIOS.

3.2.2.2 ACPI Settings

Figure 3.4 ACPI Setting

■ **Enable ACPI Auto Configuration**
This item allows users to enable or disable BIOS ACPI auto configuration.

■ **Enable Hibernation**
This item allows users to enable or disable hibernation.

■ **ACPI Sleep State**
This item allows users to set the ACPI sleep state.

■ **Lock Legacy Resources**
This item allows users to lock legacy devices' resources.

■ **S3 Video Report**
This item allows users to enable or disable S3 resume for VBIOS.

3.2.2.3 TPM Configuration
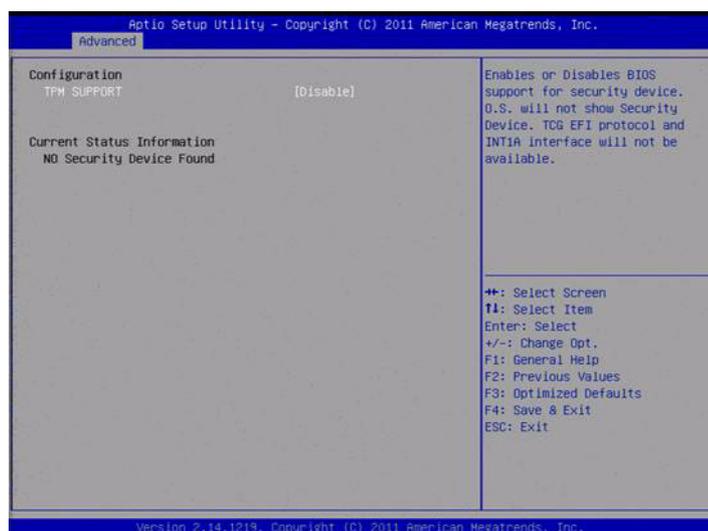
Figure 3.5 TPM Configuration

■ **TPM Support**
Disable/Enable TPM if available.

3.2.2.4 CPU Configuration

Figure 3.6 CPU Configuration

■ **Hyper Threading Technology**
This item allows users to enable or disable Intel Hyper Threading technology.
■ **Execute Disable Bit**
This item allows users to enable or disable the No-Execution page protection.
■ **Limit CPUID Maximum**
This item allows users to enable or disable limit CPUID maximum for Windows XP.

3.2.2.5 SATA Configuration
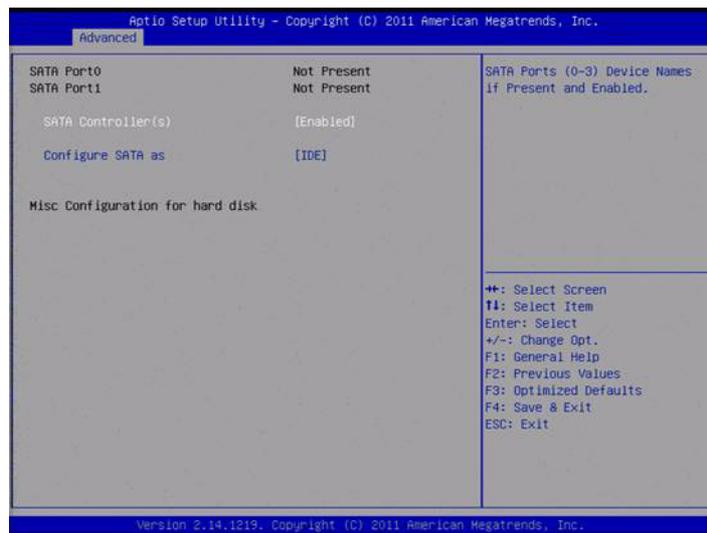
Figure 3.7 SATA Configuration

■ **SATA Controller(s)**
This item allows users to enable or disable the SATA controller(s).
■ **SATA Mode Selection**
This item allows users to select mode of SATA controller(s).

3.2.2.6 Intel Fast Flash Standby

Figure 3.8 Intel Fast Flash Standby

■ **IFFS Support**
This item allows users to enable or disable iFFS.

3.2.2.7 USB Configuration
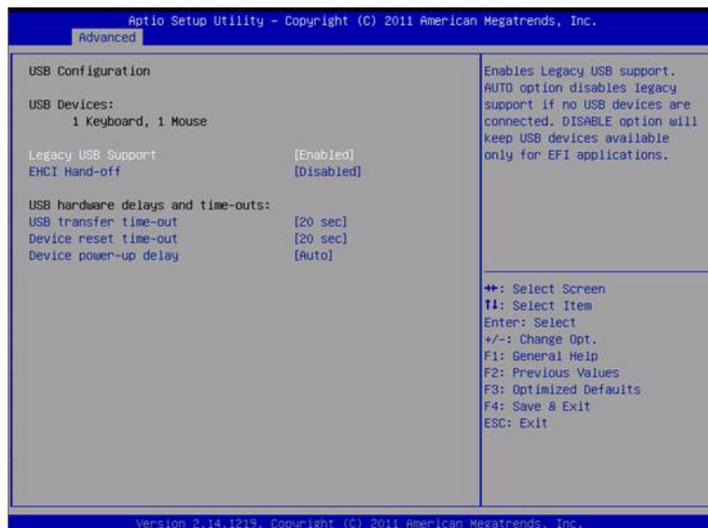
Figure 3.9 USB Configuration

■ **Legacy USB Support**

Enable the support for legacy USB. Auto option disables legacy support if no USB devices are connected.

■ **EHCI Hand-Off**

This is a workaround for the OS without EHCI hand-off support. The EHCI ownership change should claim by EHCI driver.

■ **USB transfer time-out**

Set the time-out value for Control, Bulk, and Interrupt transfers.

■ **Device reset time-out**

Set USB mass storage device Start Unit command time-out value.

■ **Device power-up delay**

Sets the maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses a default value: for a Root port it is 100 ms, for a Hub port the delay is taken from the Hub descriptor.

3.2.2.8 Super IO Configuration
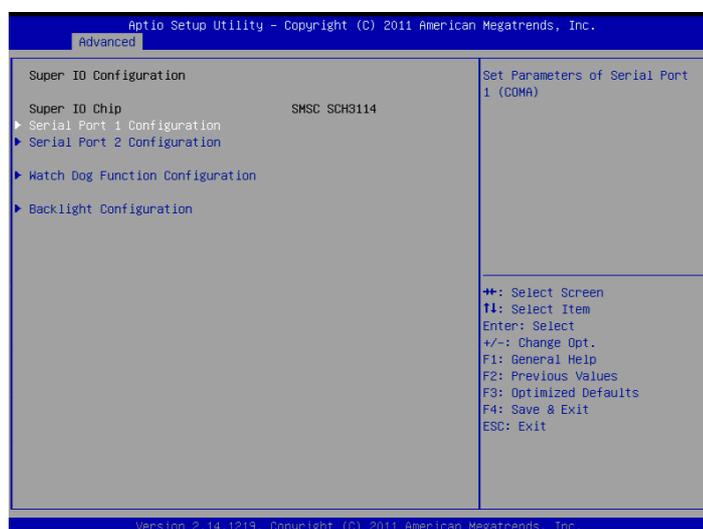
Figure 3.10 Super IO Configuration

- **Serial Port 1 Configuration**
  This item allows users to configure serial port 1.
- **Serial Port 2 Configuration**
  This item allows users to configure serial port 2.
- **Watch Dog Function Configuration**
  This item allows users to configure watch dog settings.
- **Backlight Configuration**
  This item allows users to configure backlight control settings.

3.2.2.9 H/W Monitor Configuration
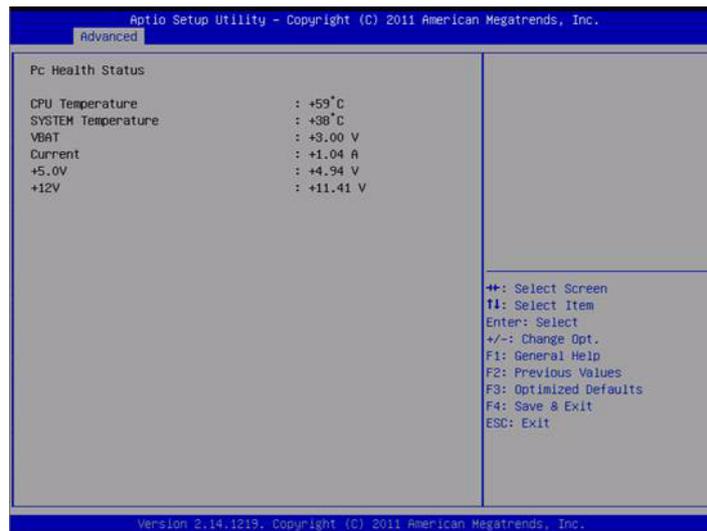
Figure 3.11 HW Monitor Configuration

This page display all information about system Temperature/Voltage/Current.

3.2.2.10 AOAC Configuration
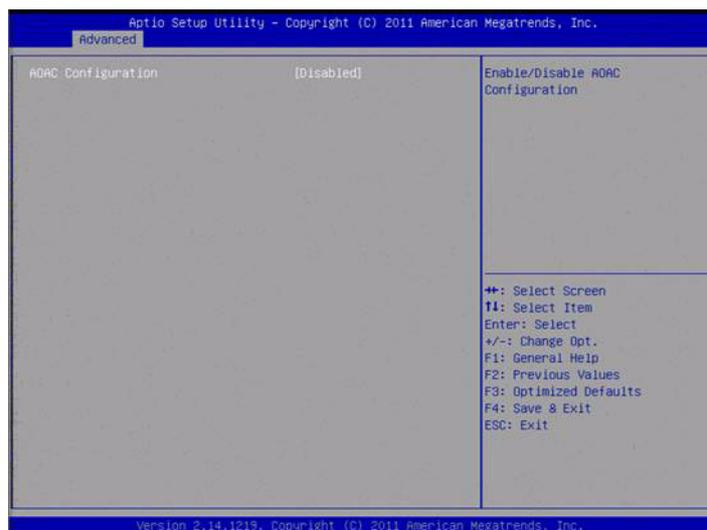
Figure 3.12 AOAC Configuration

- **AOAC Configuration**
  This item allows users to enable or disabled AOAC function.

3.2.2.11 PPM Configuration
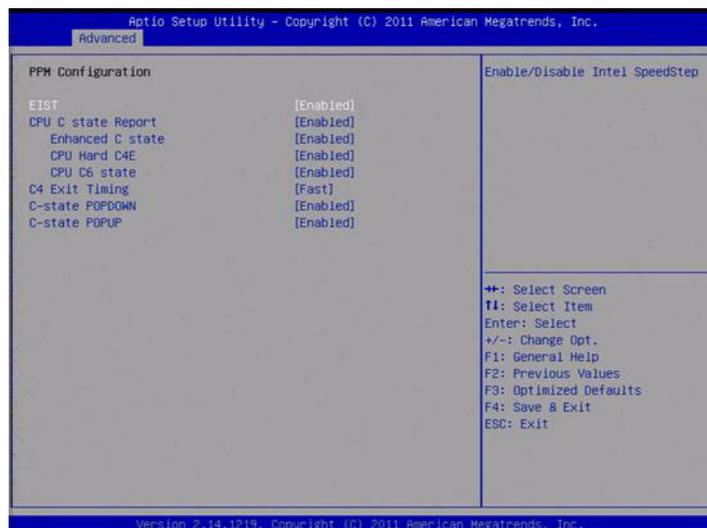
Figure 3.13 PPM Configuration

- ◼ **EIST**

  This item allows users to enable or disabled Intel SpeedStep function.

- ◼ **CPU C state Report**

  This item allows users to enable or disabled CPU C state report to OS.

- ◼ **Enhanced C state**

  This item allows users to enable or disabled Enhanced CPU C state.

- ◼ **CPU Hard C4E**

  This item allows users to enable or disabled CPU Hard C4E function.

- ◼ **CPU C6 state**

  This item allows users to enable or disabled CPU C6 state.

- ◼ **C4 Exit Timing**

  This item allows users to control a programmable time for the CPU voltage to stabilize when exiting from a C4 state.

- ◼ **C-state POPDOWN**

  This item allows users to enable or disabled Intel C-state POPDOWN function.

- ◼ **C-state POPUP**

  This item allows users to enable or disabled Intel C-state POPUP function.

3.2.3 Chipset

Select the Chipset tab from the MIO-2261 setup screen to enter the Chipset BIOS Setup screen. You can display a Chipset BIOS Setup option by highlighting it using the <Arrow> keys. All Plug and Play BIOS Setup options are described in this section.

The Plug and Play BIOS Setup screen is shown below.

Figure 3.14 Chipset Setup

3.2.3.1 Host Bridge/Intel IGD Configuration

Figure 3.15 Intel IGD Configuration

- ■ **Auto Disable IGD**
  This item allows users to auto disable IGD upon external GFX detected.
- ■ **IGFX - Boot Type**
  This item allows users to select which output device during POST.
- ■ **LCD Panel Type**
  This item allows users to select LCD panel by internal graphic device.
- ■ **Panel Scaling**
  This item allows users to select LCD panel scaling by internal graphic device.

- **Backlight Control**

  This item allows users to select backlight control setting.
- **Active LFP**

  This item allows users to select the active LFP configuration.
- **IGD Clock Source**

  This item allows users to select IGD clock.
- **Fixed Graphics Memory Size**

  This item allows users to configure fixed graphic memory size.
- **ALS Support**

  This item allows users to select ASL support for ACPI.
- **Backlight Control Support**

  This item allows users to select backlight control support.
- **BIA**

  This item allows users to select BIA with selected aggressiveness level.

3.2.3.2 South Bridge
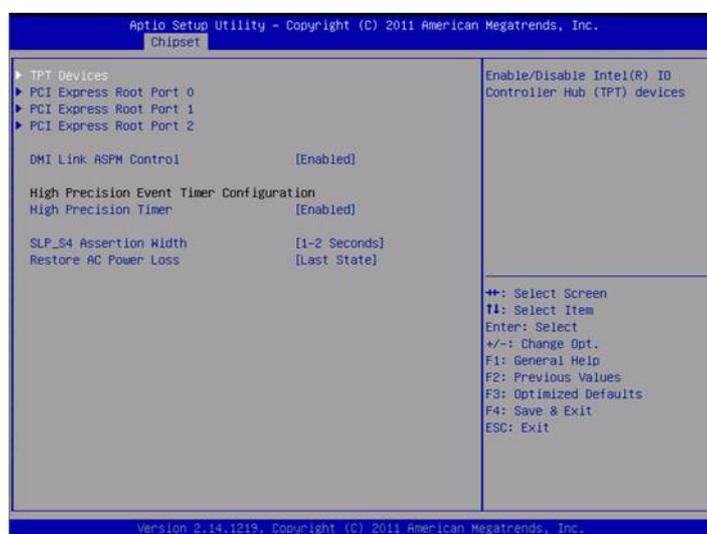
Figure 3.16 South Bridge

- **PCI Express Root Port 0/1/2**

  This item allows users to config PCIe port 0/1/2 settings.
- **DMI Link ASPM Control**

  This item Enables or disables control of active state power management on both NB and SB side of DMI link.
- **High Precision Timer**

  Enables or disables the high precision timer.
- **SLP_S4 Assertion Width**

  This item allows users to set a delay of sorts.
- **Restore AC Power Loss**
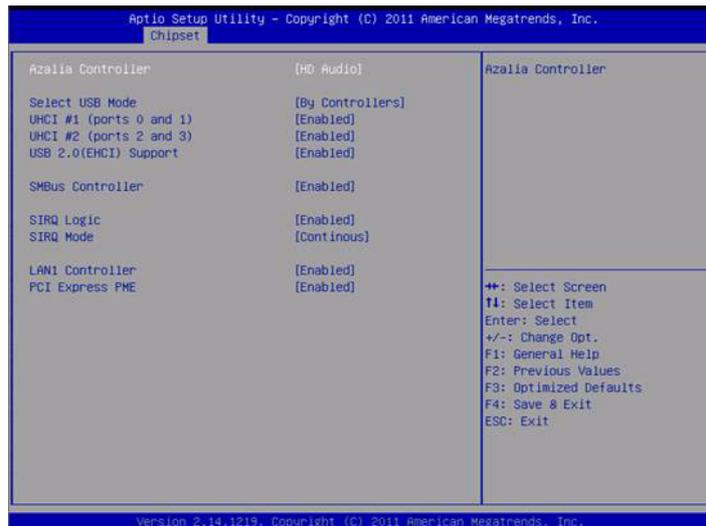
Figure 3.17 TPT Device

■ **Azalia Controller**
Enables or disables the azalia controller.

■ **Select USB Mode**
Select USB mode by controllers or ports.

■ **SMBus Controller**
Enables or disables the onchip SMBus controller.

■ **SIRQ Logic**
Enables or disables the SIRQ logic.

■ **SIRQ Mode**
Set SIRQ mode.

■ **MSATA/PCIe Switch**
Enables for MSATA disables for PCIe.

■ **LAN1 Controller**
This item allows users to enables or disables LAN device.

■ **PCI Express PME**
This item allows users to enables or disables PCIe PME function.

3.2.4 Boot Settings
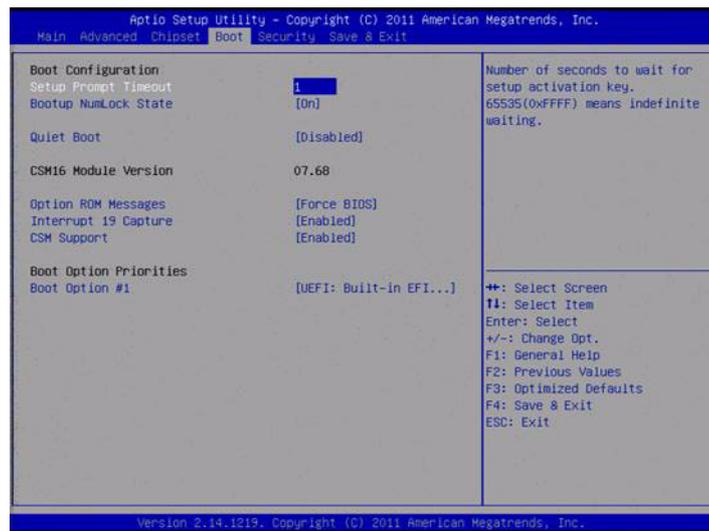
Figure 3.18 Boot Setup Utility

■ **Setup Prompt Timeout**

This item allows users to select the number of seconds to wait for setup activation key.

■ **Bootup NumLock State**

Select the Power-on state for Numlock.

■ **Quiet Boot**

If this option is set to Disabled, the BIOS displays normal POST messages. If Enabled, an OEM Logo is shown instead of POST messages.

■ **Option ROM Message**

Set display mode for option ROM.

■ **Interrupt 19 Capture**

This item allows option ROMs to trap interrupt 19.

■ **1st/2nd/3rd/4th/5th/6th/7th Boot**

This item allows users to set boot device priority.

3.2.5 Security Setup
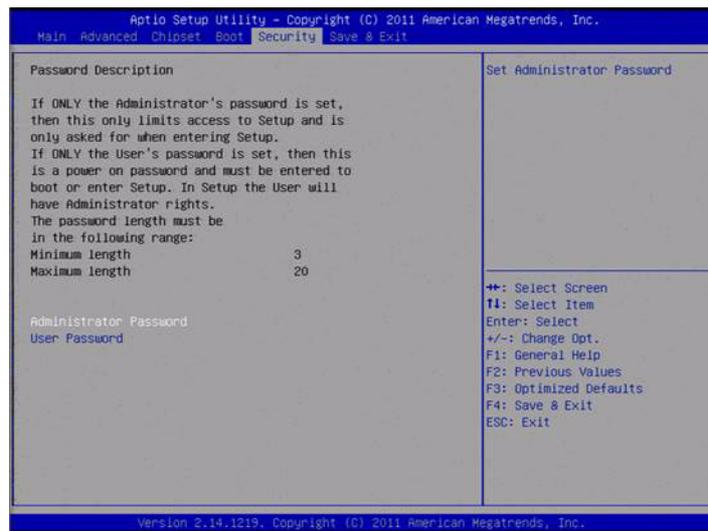
Figure 3.19 Password Configuration

Select Security Setup from the MIO-2261 Setup main BIOS setup menu. All Security Setup options, such as password protection is described in this section. To access the sub menu for the following items, select the item and press <Enter>:

■ **Change Administrator / User Password**

Select this option and press <ENTER> to access the sub menu, and then type

in the password.

3.2.6 Save & Exit
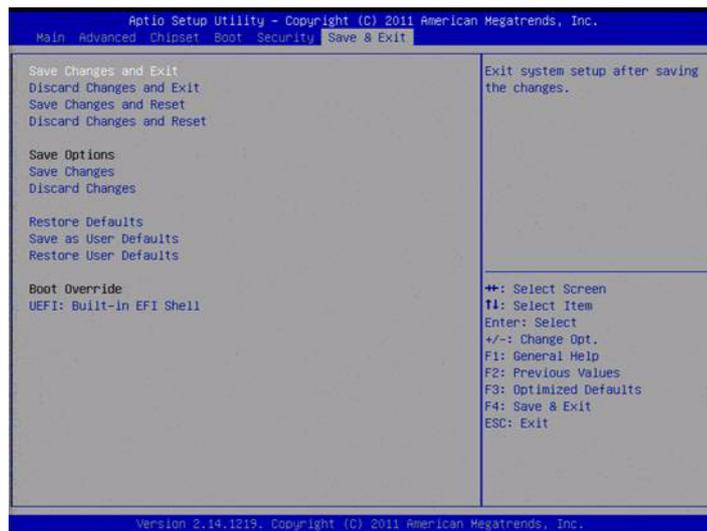
Figure 3.20 3.22 Save & Exit

3.2.6.1 Save Changes and Exit

When users have completed system configuration, select this option to save changes, exit BIOS setup menu and reboot the computer if necessary to take effect of all system configuration parameters.

3.2.6.2 Discard Changes and Exit

Select this option to quit Setup without making any permanent changes to the system configuration.

3.2.6.3 Save Changes and Reset

When users have completed system configuration, select this option to save changes, exit the BIOS setup menu and reboot the computer to take effect of all system configuration parameters.

3.2.6.4 Discard Changes and Reset

Select this option to quit Setup without making any permanent changes to the system configuration and reboot the computer.

3.2.6.5 Save Changes

When users have completed system configuration, select this option to save changes without exiting the BIOS setup menu.

3.2.6.6 Discard Changes

Select this option to discard any current changes and load previous system configuration.

3.2.6.7 Restore Defaults

The MIO-2261 automatically configures all setup items to optimal settings when users select this option. Optimal Defaults are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Optimal Defaults if the user's computer is experiencing system configuration problems.

3.2.6.8 Save User Defaults

When users have completed system configuration, select this option to save changes as user defaults without exit BIOS setup menu.

3.2.6.9 Restore User Defaults

The users can select this option to restore user defaults.

3.2.6.10 Boot Override

You select device you want to do boot override.

Chapter 4

S/W Introduction & Installation

4.1 S/W Introduction

The mission of Advantech Embedded Software Services is to "Enhance quality of life with Advantech platforms and Microsoft® Windows® embedded technology." We enable Windows embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (Hardware suppliers, System integrators, Embedded OS distributor) for projects. Our goal is to make Windows embedded software solutions easily and widely available to the embedded computing community.

4.2 Driver Installation

4.2.1 Windows 7 Professional

To install the drivers, insert the driver CD into DVD-ROM, select the drivers that need to be installed, then launch setup file under each function folder and follow Driver Setup instructions to complete the process.

4.2.2 Other OS

To install the drivers for another Windows OS or Linux, please browse the CD to run the setup file under the appropriate OS folder (s).

4.3 Value-Added Software Services

Software API: An interface that defines the ways by which an application program may request services from libraries and/or operating systems. Provides not only the underlying drivers required but also a rich set of user-friendly, intelligent and integrated interfaces, which speeds development, enhances security and offers add-on value for Advantech platforms.

4.3.1 SUSI Introduction

To make hardware easier and more convenient to access for programmers, Advantech has released a suite of API (Application Programming Interface) in the form of a program library. The program Library is called Secured and Unified Smart Interface or SUSI for short.

In modern operating systems, user space applications cannot access hardware directly. Drivers are required to access hardware. User space applications access hardware through drivers. Different operating systems usually define different interface for drivers. This means that user space applications call different functions for hardware access in different operating systems. To provide a uniform interface for accessing hardware, an abstraction layer is built on top of the drivers and SUSI is such an abstraction layer. SUSI provides a uniform API for application programmers to access the hardware functions in different Operating Systems and on different Advantech hardware platforms.

Application programmers can invoke the functions exported by SUSI instead of calling the drivers directly. The benefit of using SUSI is portability. The same set of APIs is defined for different Advantech hardware platforms. Also, the same API set is implemented in different Operating Systems. This user's manual describes some sample programs and the API in SUSI. The hardware functions currently supported by SUSI can be grouped into a few categories including Watchdog, I^2C, SMBus, GPIO, and VGA control. Each category of API in SUSI is briefly described below.

4.3.2 Software APIs

4.3.2.1 The GPIO API

General Purpose Input/Output is a flexible parallel interface that allows a variety of custom connections. It allows users to monitor the level of signal input or set the output status to switch on/off a device. Our API also provides Programmable GPIO, which allows developers to dynamically set the GPIO input or output status.

4.3.2.2 The I^2C API

I^2C is a bi-directional two-wire bus that was developed by Phillips for use in their televisions in the 1980s and nowadays is used in various types of embedded systems. The strict timing requirements defined in the I^2C protocol has been taken care of by SUSI. Instead of asking application programmers to figure out the strict timing requirements in the I^2C protocol, the I^2C API in SUSI can be used to control I^2C devices by invoking other function calls. SUSI provides a consistent programming interface for different Advantech boards. That means user programs using SUSI are portable among different Advantech boards as long as the boards and SUSI provide the required functionalities. Overall product development times can be greatly reduced using SUSI.

4.3.2.3 The SMBus API

The System Management Bus (SMBus) is a two-wire interface defined by Intel Corporation in 1995. It is based on the same principles of operation of I^2C and is used in personal computers and servers for low-speed system management communications. Nowadays, it can be seen in many types of embedded systems. As with other API in SUSI, the SMBus API is available on many platforms including Windows 7.

4.3.2.4 The Display Control API

There are two kinds of VGA control APIs, backlight on/off control and brightness control. Backlight on/off control allows a developer to turn on or off the backlight, and to control brightness smoothly.

1. Brightness Control
    – The Brightness Control API allows a developer to interface with an embedded device to easily control brightness.
2. Backlight Control
    – The Backlight API allows a developer to control the backlight (screen) on/off in an embedded device.

4.3.2.5 The Watchdog API

A watchdog timer (abbreviated as WDT) is a hardware device which triggers an action, e.g. rebooting the system, if the system does not reset the timer within a specific period of time. The WDT API in SUSI provides developers with functions such as starting the timer, resetting the timer, and setting the timeout value if the hardware requires customized timeout values.

4.3.2.6 The Hardware Monitor API

The hardware monitor (abbreviated as HWM) is a system health supervision capability achieved by placing certain I/O chips along with sensors for inspecting the target of interests for certain condition indexes, such as fan speed, temperature and voltage etc.

However, due to the inaccuracy among many commercially available hardware monitoring chips, Advantech has developed a unique scheme for hardware monitoring - achieved by using a dedicated micro-processor with algorithms specifically designed

for providing accurate, real-time and reliable data content; helping protect your system in a more reliable manner.

4.3.2.7 The Power Saving API
1. CPU Speed
   – Make use of Intel SpeedStep technology to reduce power consumption. The system will automatically adjust the CPU Speed depending on system loading.
2. System Throttling
   – Refers to a series of methods for reducing power consumption in computers by lowering the clock frequency. APIs allow the user to lower the clock from 87.5% to 12.5%.

4.3.3 SUSI Installation

SUSI supports many different operating systems. Each subsection below describes how to install SUSI and related software on a specific operating system. Please refer to the subsection matching your operating system.

4.3.3.1 Windows 7
In Windows 7, you can install the library, drivers and demo programs onto the platform easily using the installation tool--The SUSI Library Installer. After the installer has executed, the SUSI Library and related files for Windows 7 can be found in the target installation directory. The files are listed in the following table.

Directory	Contents
\Library	■ Susi.lib
	Library for developing the applications on Windows 7.
	■ Susi.dll
	Dynamic library for SUSI on Windows 7.
\Demo	■ SusiDemo.EXE
	Demo program on Windows® 7.
	■ Susi.dll
	Dynamic library for SUSI on Windows 7.
\Demo\SRC	Source code of the demo program on Windows 7.

The following section illustrates the installation process.

> *Note!* *The SUSI Library Installer screen shots shown below are examples only. Your screens may vary depending on your particular version.*

1. Extract Susi.zip.
2. Double-click the "Setup.exe" file.

The installer searches for a previous installation of the SUSI Library. If it locates one, a dialog box opens asking whether you want to modify, repair or remove the software. If a previous version is located, please see the [Maintenance Setup] section. If it is not located, an alternative window appears. Click Next.

4.3.4 SUSI Sample Programs

Sample Programs

The sample programs demonstrate how to incorporate SUSI into your program. The sample programs run in graphics mode in Windows® 7 are described in the subsections below.

Windows Graphics Mode

Each demo application contains an executable file SusiDemo.exe, a shared library Susi.dll and source code within the release package.

SusiDemo.exe is an executable file and it requires the shared library, Susi.dll, to demonstrate the SUSI functions. The source code of SusiDemo.exe must be compiled under Microsoft Visual C++ 6.0 on Windows 7. Developers must add the header file Susi.h and library Susi.lib to their own projects when they want to develop something with SUSI.

SusiDemo.exe

The SusiDemo.exe test application is an application which uses all functions of the

SUSI Library. It has five major function blocks: Watchdog, GPIO, SMBus, I^{2}C and VGA control. The following screen shot appears when you execute SusiDemo.exe. You can click function tabs to select test functions respectively. Some function tabs will not show on the test application if your platform does not support such functions. For a complete support list, please refer to Appendix A. We describe the steps to test all functions of this application.

GPIO
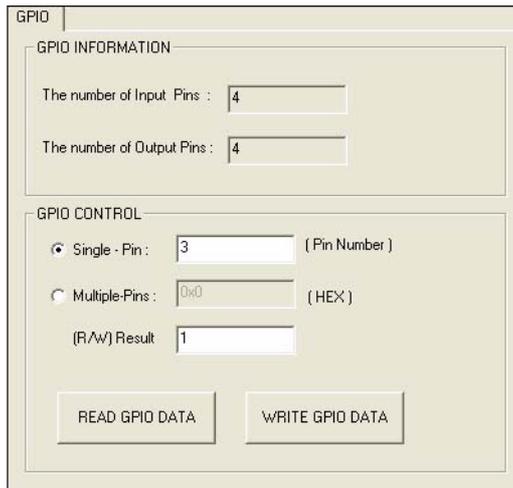
When the application is executed, it will display GPIO information in the GPIO INFORMATION group box. It displays the number of input pins and output pins. You can click the radio button to choose to test either the single pin function or multiple pin functions. The GPIO pin assignments of the supported platforms are located in Appendix B.

■ Test Read Single Input Pin
  – Click the radio button- Single-Pin.
  – Key in the pin number to read the value of the input pin. The Pin number starts from '0'.
  – Click the READ GPIO DATA button and the status of the GPIO pin will be displayed in (R/W) Result field.

■ Test Read Multiple Input Pin
  – Click the radio button- Multiple-Pins.
  – Key in the pin number from '0x01' to '0x0F' to read the value of the input pin. The pin numbers are ordered bitwise, i.e. bit 0 stands for GPIO 0, bit 1 stands for GPIO 1, etc. For example, if you want to read pin 0, 1, and 3, the pin numbers should be '0x0B'.
  – Click READ GPIO DATA button and the statuses of the GPIO pins will be displayed in (R/W) Result field.

■ Test Write Single Output Pin
  – Click the radio button- Single-Pin.
  – Key in the pin numbers you want to write. Pin numbers start from '0'.
  – Key in the value either '0' or '1' in (R/W) Result field to write the output pin you chose above step.
  – Click the WRITE GPIO DATA button to write the GPIO output pin.

■ Test Write Multiple Output Pins
  – Click the radio button- Multiple-Pins.
  – Key in the pin number from '0x01' to '0x0F' to choose the multiple pin numbers to write the value of the output pin. The pin numbers are ordered bitwise, i.e. bit 0 stands for GPIO 0, bit 1 stands for GPIO 1, etc. For example, if you want to write pin 0, 1, and 3, the pin numbers should be '0x0B'.
  – Key in the value in (R/W) Result field from '0x01' to '0x0F' to write the value of the output pin. The pin numbers are ordered bitwise, i.e. bit 0 stands for GPIO 0, bit 1 stands for GPIO 1, etc. For example, if you want to set pin 0

and 1 high, 3 to low, the pin number should be '0x0B/, and then you should key in the value '0x0A' to write.
– Click the WRITE GPIO DATA button to write the GPIO output pins.

I²C

When the application is executed, you can read or write a byte of data through I²C devices. All data must be read or written in hexadecimal system.

■ Read a byte
– Key in the slave device address in Slave address field.
– Key in the register offset in Register Offset field.
– Click the READ A BYTE button and then a byte of data from the device will be shown on the Result field.

■ Write a byte
– Key in the slave device address in Slave address field.
– Key in the register offset in Register Offset field.
– Key in the desirous of data in Result field to write to the device.
– Click the WRITE A BYTE button and then the data will be written to the device through I²C.

SMBus

When the application has executed, you can click the radio button to choose to test each access mode, i.e. Access a byte, Access multiple bytes and Access a word. All data must be read or written in hexadecimal except the numbers for radio button: Access multiple bytes mode must be written in decimal. You can test the functionalities of the watchdog as follows:

- ■ Read a byte
  - – Click the radio button- Access a byte.
  - – Key in the slave device address in the Slave address field.
  - – Key in the register offset in the Register Offset field.
  - – Click the READ SMBus DATA button and a byte of data from the device will be shown on the Result field.

- ■ Write a byte
  - – Click the radio button- Access a byte.
 - – Key in the slave device address in Slave address field.
  - – Key in the register offset in Register Offset field.
  - – Key the desired data in the Result field to write to the device.
  - – Click the WRITE SMBus DATA button and then the data will be written to the device through SMBus.

- ■ Read a word
  - – Click the radio button- Access a word.
  - – Key in the slave device address in the Slave address field.
  - – Key in the register offset in the Register Offset field.
  - – Click the READ SMBus DATA button and then a word of data from the device will be shown on the Result field.

- ■ Write a word
  - – Click the radio button- Access a word.
  - – Key in the slave device address in the Slave address field.
  - – Key in the register offset in the Register Offset field.
  - – Key in the desired data, such as 0x1234, in the Result field to write to the device.
  - – Click the WRITE SMBus DATA button and the data will be written to the device through the SMBus.
- ■ Read Multiple bytes
  - – Click the radio button- Access multiple bytes.
  - – Key in the slave device address in the Slave address field.
  - – Key in the register offset in the Register Offset field.
  - – Key in the desired number of bytes, such as 3, in the right side field of radio button- Access multiple bytes. The number must be written in decimal.
  - – Click the READ SMBus DATA button and then all data from the device will be divided from each other by commas and be shown in the Result field.
- ■ Write Multiple bytes
  - – Click the radio button- Access multiple bytes.
  - – Key in the slave device address in the Slave address field.
  - – Key in the register offset in the Register Offset field.
  - – Key in the desired number of bytes, such as 3, in the right side field of the radio button- Access multiple bytes. The number must be written in decimal.
  - – Key in all the desired data in the Result field in hexadecimal format, divided by commas, for example, 0x50,0x60,0x7A.
  - – Click the WRITE SMBus DATA button and all of the data will be written to the device through the SMBus.

Display Control
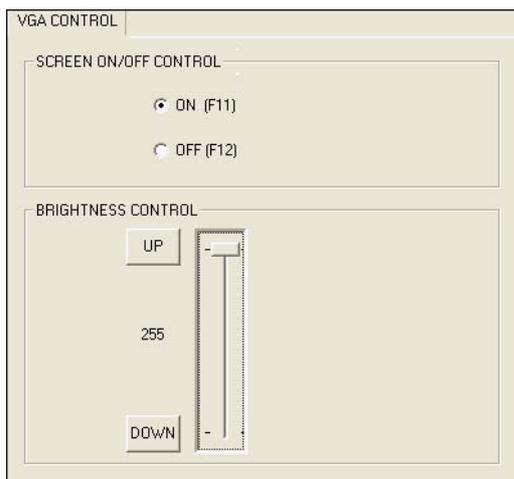
When the application is executed, it will display two blocks of VGA control functions. The application can turn on or turn off the screen shot freely, and it also can tune the brightness of the panels if your platform is being supported. You can test the functionalities of VGA control as follows:

■ Screen on/off control
  – Click the radio button ON or push the key F11 to turn on the panel screen.
  – Click the radio button OFF or push the key F12 to turn off the panel screen.
  – The display chip of your platform must be in the support list in Appendix A, or this function cannot work.
■ Brightness control
  – Move the slider in increments, using either the mouse or the direction keys, or click the UP button to increase the brightness.
  – Move the slider in decrements, using either the mouse or the direction keys, or click the DOWN button to decrease the brightness.

Watchdog
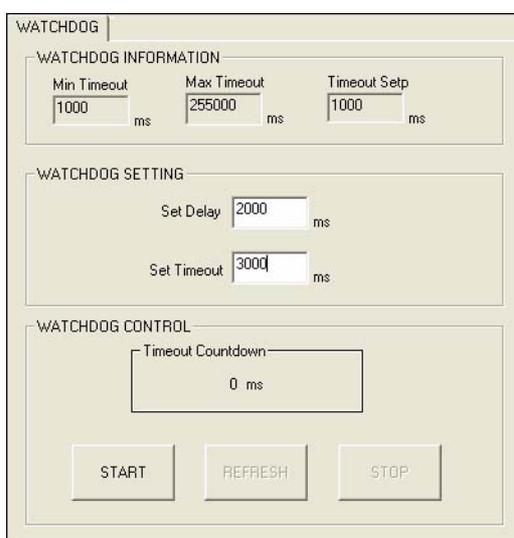
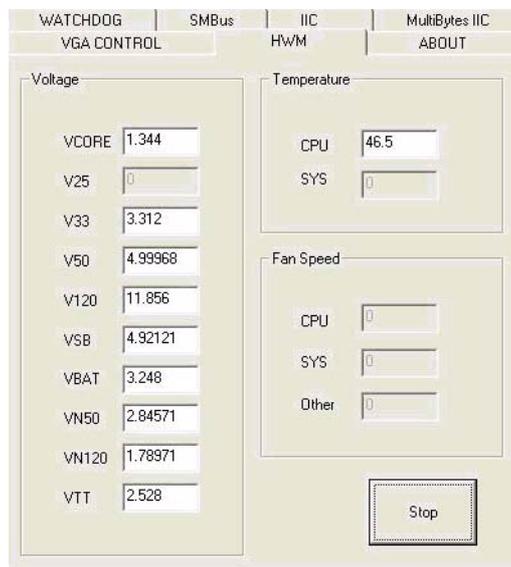When the application is executed, it will display watchdog information in the WATCH-DOG INFORMATION group box. It displays max timeout, min timeout, and timeout steps in milliseconds. For example, a 1~255 seconds watchdog will have 255000 max timeout, 1000 min timeout, and 1000 timeout steps. You can test the functionality of the watchdog as follows:

■   Set the timeout value 3000 (3 sec.) in the SET TIMEOUT field and set the delay value 2000 (2 sec.) in the SET DELAY field, then click the START button. The Timeout Countdown field will countdown the watchdog timer and display 5000 (5 sec.).

■   Before the timer counts down to zero, you can reset the timer by clicking the REFRESH button. After you click this button, the Timeout Countdown field will display the value of the SET TIMEOUT field.

■   If you want to stop the watchdog timer, just click the STOP button.

Hardware Monitor

When the Monitor application is executed by clicking the button, hardware monitoring data values will be displayed. If certain data values are not supported by the platform, the correspondent data field will be grayed-out with a value of 0.

For more details on MIO-2261 software API, please contact your dealer or Advantech AE.

Appendix A

PIN Assignments

A.1 Jumper Setting

Table A.1: Jumper List	
J1	LCD Power / Auto Power on

A.2 Connectors

Table A.2: Connectors	
CN1	12 V Power Input
CN2	DC JACK (by request)
CN3	DDR3 SO-DIMM
CN4	GPIO
CN5	VGA
CN6	mSATA
CN7	SATA
CN8	Mini PCIe
CN9	External USB
CN10	Internal USB
CN11	COM1/COM2
CN12	SMBus (or I^2C, by request)
CN13	Front Panel
CN14	Gigabit Ethernet
CN15	HD Audio
CN16	MIOe
CN17	Inverter Power / Internal SATA Power
CN18	24 bits LVDS Panel
BH1	Battery

Table A.3: J1: LCD Power/Auto Power On	
Part Number	1653003260
Footprint	HD_3x2P_79
Description	PIN HEADER 3*2P 180D(M) 2.0mm SMD SOUARE PIN
Setting	**Function**
(1-2)	+5 V
(3-4) (default)	+3.3 V
(5-6) (default)	Auto Power On
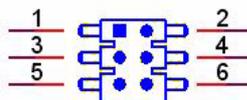
CN1	12 V Power Input
Part Number	1655003962
Footprint	WF_2P_156_D_A3963WV2
Description	
Pin	Pin Name
1	+12 V
2	GND
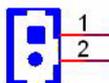
CN2	DC JACK (by request)
Part Number	1652005684
Footprint	PJ_3P_DCJ-RPBT5NW-25
Description	
Pin	Pin Name
1	+VIN
2	GND
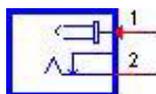
CN3	DDR3 SO-DIMM
Part Number	1651002083
Footprint	DDR3_204P_AS0A626-JA
Description	
Pin	Pin Name

CN4	GPIO
Part Number	1653005261
Footprint	HD_5x2P_79
Description	PIN HEADER SMD 5*2P 180D(M) 2.0 mm
Pin	Pin Name
1	+5 V
2	GPIO4
3	GPIO0
4	GPIO5
5	GPIO1
6	GPIO6
7	GPIO2
8	GPIO7
9	GPIO3
10	GND
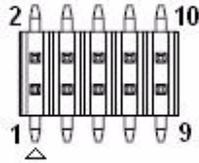
CN5	VGA
Part Number	1654000055
Footprint	DBVGA-VF5MS
Description	D-SUB Conn. 15P 90D(F) DIP 070242FR015S200ZU
Pin	Pin Name
1	RED
2	GREEN
3	BLUE
4	NC
5	GND
6	GND
7	GND
8	GND
9	NC
10	GND
11	NC
12	DDAT
13	HSYNC
14	VSYNC
15	DCLK
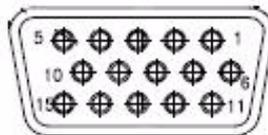
CN6	mSATA
Part Number	**00A00000770**
Footprint	**MINIPCIE_HALF_PICO_ITX**
Description	
Pin	Pin Name
1	NC
2	+3.3V
3	NC
4	GND
5	NC
6	+1.5V
7	NC
8	NC
9	GND
10	NC
11	NC
12	NC
13	NC
14	NC
15	GND
16	NC
17	NC
18	GND
19	NC
20	NC
21	GND
22	NC
23	B+
24	+3.3V
25	B-
26	GND

CN6	mSATA
Part Number	00A00000770
Footprint	MINIPCIE_HALF_PICO_ITX
Description	
Pin	Pin Name
27	GND
28	+1.5V
29	GND
30	SMB_CLK
31	A-
32	SMB_DAT
33	A+
34	GND
35	GND
36	USB D-
37	GND
38	USB D+
39	+3.3V
40	GND
41	+3.3V
42	NC
43	NC
44	NC
45	NC
46	NC
47	NC
48	+1.5V
49	NC
50	GND
51	NC
52	+3.3V

CN7	SATA
Part Number	1654007578
Footprint	SATA_7P_WATF-07DBN6SB1U
Description	
Pin	Pin Name
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND
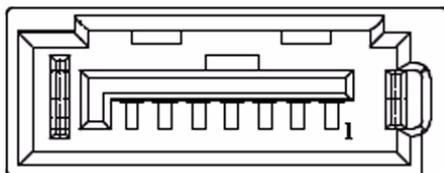
CN8	Mini PCIe
Part Number	00A00000660
Footprint	MINIPCIE_HALF_PICO2600
Description	
Pin	Pin Name
1	WAKE#
2	+3.3VSB
3	NC
4	GND
5	NC
6	+1.5V
7	NC
8	NC
9	GND
10	NC
11	REFCLK-
12	NC
13	REFCLK+
14	NC
15	GND
16	NC
17	NC
18	GND
19	NC
20	NC
21	GND
22	PERST#
23	PERn0
24	+3.3VSB
25	PERp0
26	GND

CN8	Mini PCIE
Part Number	00A00000660
Footprint	MINIPCIE_HALF_PICO2600
Description	
Pin	Pin Name
27	GND
28	+1.5 V
29	GND
30	SMB_CLK
31	PETn0
32	SMB_DAT
33	PETp0
34	GND
35	GND
36	USB D-
37	GND
38	USB D+
39	+3.3 VSB
40	GND
41	+3.3 VSB
42	NC
43	GND
44	NC
45	NC
46	NC
47	NC
48	+1.5 V
49	NC
50	GND
51	NC
52	+3.3 VSB

CN9	External USB
Part Number	1654009513
Footprint	USB_8P_UB1112C-8FDE-4F
Description	
Pin	Pin Name
1	+5 V
2	D-
3	D+
4	GND
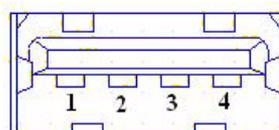
CN10	Internal USB
Part Number	1653005260
Footprint	HD_5x2P_79_N10
Description	PIN HEADER 2*5P 180D(M) 2.0 mm SMD IDIOT-PROOF
Pin	Pin Name
1	+5 V
2	+5 V
3	A_D-
4	B_D-
5	A_D+
6	B_D+
7	GND
8	GND
9	GND
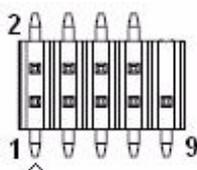
CN11	COM1/COM2
Part Number	1653003720
Footprint	HD_10x2P_79_RA
Description	
Pin	Pin Name
1	DCD1#
2	DSR1#
3	RXD1
4	RTS1#
5	TXD1
6	CTS1#
7	DTR1#
8	RI1#
9	GND
10	GND
11	DCD2#
12	DSR2#
13	RXD2
14	RTS2#
15	TXD2
16	CTS2#
17	DTR2#
18	RI2#
19	GND
20	GND
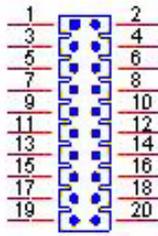
CN12	SMBus (or I^{2}C, by request)
Part Number	1655904020
Footprint	FPC4V-125M
Description	Wafer SMT 1.25 mm S/T type 4P 180D(M) 85205-04001
Pin	Pin Name
1	GND
2	SMB_DAT
3	SMB_CLK
4	+5 V
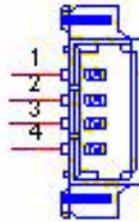
CN13	Front Panel
Part Number	1653004883
Footprint	HD_3x2P_79_RA_21N22050
Description	
Pin	Pin Name
1	Power Button Pin1
2	Power LED+
3	Power/Reset Button Pin2
4	HDD LED+
5	Reset Button Pin1
6	HDD LED-
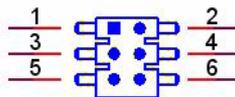
CN14	Gigabit Ethernet
Part Number	1652004356
Footprint	RJ45_14P_RT7-194AAM1A
Description	
Pin	Pin Name
1	BI_DA+(GHz)
2	BI_DA-(GHz)
3	BI_DB+(GHz)
4	BI_DC+(GHz)
5	BI_DC-(GHz)
6	BI_DB-(GHz)
7	BI_DD+(GHz)
8	BI_DD-(GHz)
H3	GND
H4	GND
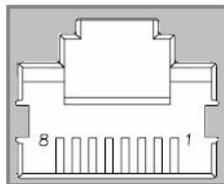
CN15	HD Audio
Part Number	1653003719
Footprint	HD_5x2P_79_RA_21N22050
Description	
Pin	Pin Name
1	LOUTR
2	LINR
3	GND
4	GND
5	LOUTL
6	LINL
7	NC
8	NC
9	NC
10	NC
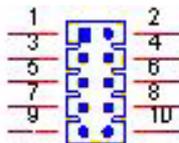
CN16	MIOe
Part Number	1654006235
Footprint	BB_40x2P_32_1625x285_2HOLD
Description	
Pin	Pin Name
1	GND
2	GND
3	PCIE_RX0+
4	PCIE_TX0+
5	PCIE_RX0-
6	PCIE_TX0-
7	GND
8	GND
9	PCIE_RX1+
10	PCIE_TX1+
11	PCIE_RX1-
12	PCIE_TX1-
13	GND
14	GND
15	PCIE_RX2+
16	PCIE_TX2+
17	PCIE_RX2-
18	PCIE_TX2-
19	GND
20	GND
21	PCIE_RX3+
22	PCIE_TX3+
23	PCIE_RX3-
24	PCIE_TX3-
25	GND
26	GND
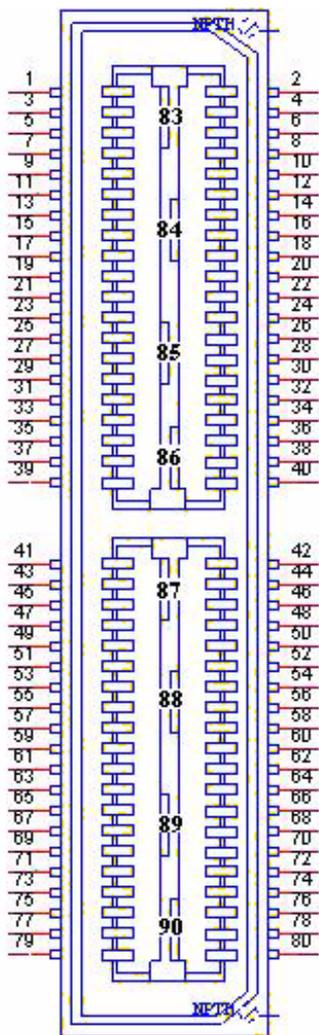
CN16	MIOe
Part Number	1654006235
Footprint	BB_40x2P_32_1625x285_2HOLD
Description	
Pin	Pin Name
27	PCIE_CLK+
28	LOUTL
29	PCIE_CLK-
30	LOUTR
31	GND
32	AGND
33	SMB_CLK
34	NC
35	SMB_DAT
36	NC
37	PCIE_WAKE#
38	NC
39	RESET#
40	NC
41	SLP_S3#
42	CLK33M
43	NC
44	LPC_AD0
45	DDP_HPD
46	LPC_AD1
47	GND
48	LPC_AD2
49	DDP_AUX+
50	LPC_AD3
51	DDP_AUX-
52	LPC_DRQ#0
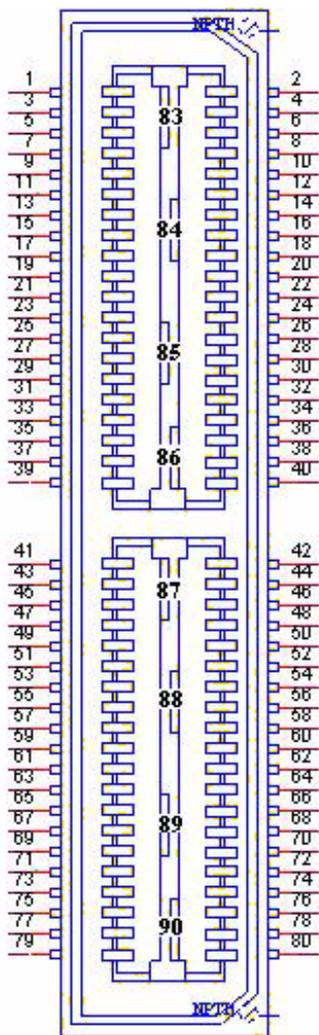
CN16	MIOe
Part Number	1654006235
Footprint	BB_40x2P_32_1625x285_2HOLD
Description	
Pin	Pin Name
53	GND
54	LPC_SERIRQ
55	DDP_D0+
56	LPC_FRAME#
57	DDP_D0-
58	GND
59	GND
60	USB0_D+
61	DDP_D1+
62	USB0_D-
63	DDP_D1-
64	GND
65	GND
66	USB1_D+/USB_SSTX+
67	DDP_D2+
68	USB1_D-/USB_SSTX-
69	DDP_D2-
70	GND
71	GND
72	USB2_D+/USB_SSRX+
73	DDP_D3+
74	USB2_D-/USB_SSRX-
75	DDP_D3-
76	GND
77	GND
78	USB_OC#
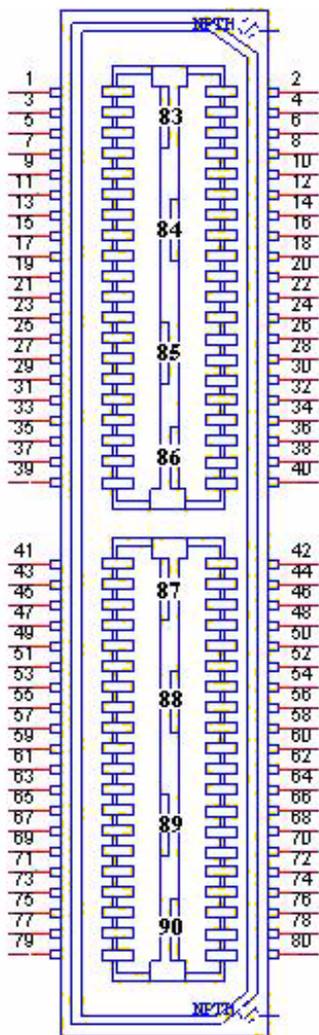
CN16	MIOe
Part Number	1654006235
Footprint	BB_40x2P_32_1625x285_2HOLD
Description	
Pin	Pin Name
79	+12VSB
80	+12VSB
83	GND
84	GND
85	GND
86	GND
87	+5VSB
88	+5VSB
89	+5VSB
90	+5VSB
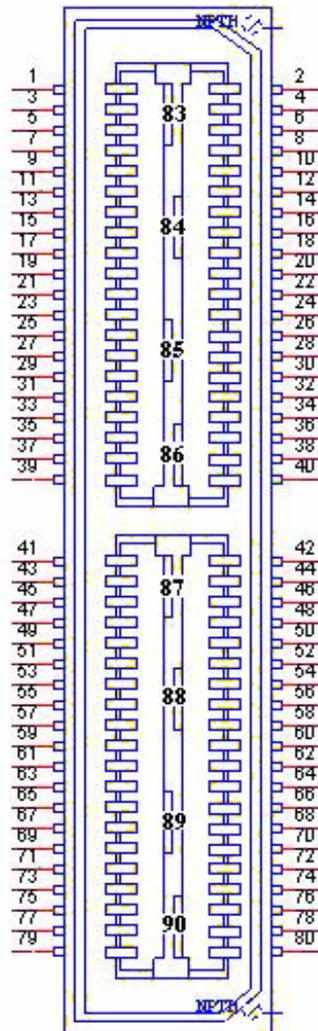
CN17	Inverter Power/ Internal SATA Power
Part Number	1655905100
Footprint	WF_5P_49_BOX_RA
Description	Wafer 1.25mm 5P 90D Male SMD 852040
Pin	Pin Name
1	+12V
2	GND
3	ENABKL
4	VBR
5	+5V
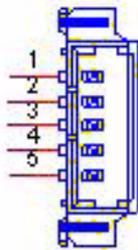
CN18	24 bits LVDS Panel
Part Number	1655000753
Footprint	WF14P_49_BOX_RA_85204-14001
Description	
Pin	Pin Name
1	GND
2	GND
3	LVDS0_CLK-
4	LVDS0_CLK+
5	LVDS0_D3-
6	LVDS0_D3+
7	LVDS0_D2-
8	LVDS0_D2+
9	LVDS0_D1-
10	LVDS0_D1+
11	LVDS0_D0-
12	LVDS0_D0+
13	+5 V or +3.3 V
14	+5 V or +3.3 V
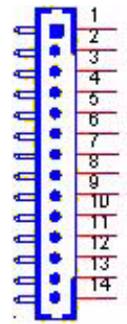
Appendix B

WDT & GPIO

B.1 Watchdog Timer Sample Code

Watchdog function:

The SCH3114 Runtime base I/O address is 600h

Setting WatchDog time value location at offset 66h

If set value "0", it is mean disable WatchDog function.

```
Superio_GPIO_Port = 600h
mov dx,Superio_GPIO_Port + 66h
mov al,00h
out dx,al
.model small
.486p
.stack 256
.data
SCH3114_IO EQU 600h
.code
org 100h
.STARTup
;=====================================================
;47H
;enable WDT function bit [0]=0Ch
;=====================================================
mov dx,SCH3114_IO + 47h
mov al,0Ch
out dx,al
;=====================================================
;65H
;bit [1:0]=Reserved
;bit [6:2]Reserve=00000
;bit [7] WDT time-out Value Units Select
;Minutes=0 (default) Seconds=1
;=====================================================
mov dx,SCH3114_IO + 65h;
mov al,080h
out dx,al
;=====================================================
;66H
;WDT timer time-out value
;bit[7:0]=0~255
;=====================================================
mov dx,SCH3114_IO + 66h
mov al,01h
out dx,al
;=====================================================
;bit[0] status bit R/W
;WD timeout occurred =1
```

```
;WD timer counting = 0
;=====================================================
mov dx,SCH3114_IO + 68h
mov al,01h
out dx,al
.exit
END
```

B.2 GPIO Sample Code

The SCH3114 Runtime base I/O address is 600h

```
.model small
.486p
.stack 256
.data
SCH3114_IO EQU 600h
.code
org 100h
.STARTup
;=====================================================
; Configuration GPIO as GPI or GPO by below register:
; GPIO0 = 23H, GPIO4 = 27H
; GPIO1 = 24H, GPIO5 = 29H
; GPIO2 = 25H, GPIO6 = 2AH
; GPIO3 = 26H, GPIO7 = 2BH
; Set 00H as output type, set 01H as input type
;=====================================================
;=====================================================
; Register 4BH configuration GPO value as high or low:
; 1 = HIGH
; 0 = LOW
;=====================================================

mov dx,SCH3114_IO + 23h     ;GPIO 0
mov al,00h                  ;Set GPIO 0 as output type
out dx,al

mov dx,SCH3114_IO + 4Bh
mov al,01h                  ;Set GPIO 0 as high value.
out dx,al

.exit
END
```

Appendix C

System Assignments

C.1 System I/O Ports

Table C.1: System I/O Ports	
Addr. Range (Hex)	**Device**
000-01Fh	DMA Controller
20h-2Dh	Interrupt Controller
50h-52h	Timer/Counter
060h-06Fh	8042 (keyboard controller)
070h-07Fh	Real-time clock, non-maskable interrupt (NMI) mask
080h-09Fh	DMA page register
0A0h-0BFh	0A0-0BF
0C0h-0DFh	DMA controller
F0C0h-F0C7h	IDE Controller
F0E0h-F0E7h	IDE Controller
2F8h-2FFh	Communications Port (COM2)
3C0h-3DFh	Motherboard resources
3F8h-3FFh	Communications Port (COM1)
400h-4FFh	Motherboard resources
500h-53Fh	Motherboard resources
600h-67Fh	Motherboard resources

C.2 DMA Channel Assignments

Table C.2: DMA Channel Assignments	
Channel	**Function**
0	Available
1	Available
2	Available
3	Available
4	Direct memory access controller
5	Available
6	Available
7	Available

C.3 1st MB Memory Map

Table C.3: 1st MB Memory Map	
Addr. Range (Hex)	Device
E0000h - FFFFFh	System board
D0000h - DFFFFh	PCI Bus
C0000h - CFFFFh	System board
A0000h - BFFFFh	PCI Bus
A0000h - BFFFFh	Intel® HD Graphic
00000h - 9FFFFh	System board

C.4 Interrupt Assignments

Table C.4: Interrupt Assignments	
Interrupt#	Interrupt Source
NMI	Parity error detected
IRQ0	System timer
IRQ1	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
IRQ2	Interrupt from controller 2 (cascade)
IRQ3	Communications Port (COM2)
IRQ4	Communications Port (COM1)
IRQ5	Available
IRQ6	Available
IRQ7	Available
IRQ8	System CMOS/real time clock
IRQ9	Microsoft ACPI-Compliant System
IRQ10	Available
IRQ11	Available
IRQ12	PS/2 Compatible Mouse
IRQ13	Numeric data processor
IRQ14	Primary IDE
IRQ15	Secondary IDE

ADVANTECH

Enabling an Intelligent Planet

www.advantech.com