MB740

AMD Geode NX
Mini-ITX Motherboard

USER'S MANUAL

Version 1.0

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THE MB740 MINI ITX MOTHERBOARD

Introduction

Product Description

The MB740 Mini ITX board incorporates a Socket A processor socket that supports AMD Geode NX series processors that support processor speed up to 1.4GHz. With the SIS 741CX chipset, it delivers maximum performance for demanding thin client or embedded applications that require silent system operation. With a higher processor speed and active cooling, it is best suited for demanding applications such as graphics and point of sales systems. The board comes with integrated chipset VGA and Ethernet controllers. Optionally provided is a Realtek Gigabit Ethernet and daughter cards for CRT2/TMDS or LVDS/TV out interface.

Features

- Socket A for AMD Geode NX processor
  Up to 1.4GHz speed, 133MHz FSB
- DDR DIMM x 1, max. 1GB, DDR266/333
- Onboard 10/100 and Optional Realtek 8110S Gigabit LAN
- Integrated SiS 741CX CRT VGA
- Optional CRT2/DVI, optional LVDS/TV out
- 2 x SATA, 6 x USB 2.0, 2 x COM, watchdog timer
- Digital I/O, optional 1394, 1x PCI, 1x Mini PCI

Dimensions of the board are 170mm x 170mm. Optional daughter cards include IBA140-301 support CRT2/DVI and IBA140-302 supporting LVDS/TV out.

Checklist

Your MB740 package should include the items listed below.

- The MB740 AMD Geode Mini-ITX motherboard
- This User's Manual
- 1 CD containing chipset drivers and flash memory utility
- Cable kit (40-pin IDE, Serial port, Serial ATA)

MB740 Specifications

Features

- Socket A for AMD Geode NX processor
  Up to 1.4GHz speed, 133MHz FSB
- DDR DIMM x 1, max. 1GB, DDR266/333
- Onboard 10/100 and Optional Realtek 8110S Gigabit LAN
- Integrated SiS 741CX CRT VGA
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- 2 x SATA, 6 x USB 2.0, 2 x COM, watchdog timer
- Digital I/O, optional 1394, 1x PCI, 1x Mini PCI

System

CPU	Socket A (462-pin) for AMD Geode, up to 1.4GHz (NX1250 = 667MHz, NX1500 = 1GHz, NX1750 =1.4GHz)
System Memory	DDR DIMM x 1, max. 1GB, DDR333
System Chipset	SiS 741CX + SiS 964
BIOS	Award 4Mbit
Watchdog Timer	256 levels
SSD	Optional CF socket (on solder side via IDE2)
H/W Monitor	Yes
Expansion Slot	1 PCI, 1 Mini PCI, 1 MicroAGP

Graphics

VGA Controller	SiS 741CX integrated for CRT
VGA Memory	Shared memory; Max. 64MB
LCD / TV-out / DVI / CRT2	Optional SiS 302LV MicroAGP card (IBA140-302) supports 18/24-bit dual channel LVDS and TV out; Optional SiS 301 MicroAGP card (IBA140-301) supports DVI/CRT2 interface

Ethernet

Controller	SiS 964 built-in 10/100 and Optional Realtek RTL8110S-32 Gigabit LAN

Multi I/O

Chipset	SiS 964, ITE 8705 2x IDE (UDMA33/66/100), 1x FDD, 1x KB, 1x Mouse; 2x RS-232, 2x SATA
USB	4 ports on board Pin header for 2 additional ports (USB 2.0)
Audio	SiS 964 built-in audio + AC97 codec, SPDIF support; 2W+2W volume amplifier
Others	1394, ATX power connector

Mechanical and Environmental

Dimensions	170mm x 170mm

Board Dimensions

Installations

This section provides information on how to use the jumpers and connectors on the MB740 in order to set up a workable system. The topics covered are:

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Installing the CPU

The MB740 board supports a Socket A processor socket for AMD NX Series processors.

The Socket A processor socket comes with a lever to secure the processor. Raise this lever to about a 90° angle to allow the insertion of the processor. Place the processor into the socket by making sure the notch on the corner of the CPU corresponds with the notch on the inside of the socket. Once the processor has slide into the socket, return the lever to the lock position. Refer to the figures below.

After you have installed the processor into the socket, check if the jumpers for the CPU type and speed are correct.

***NOTE**: Ensure that the CPU heat sink and the CPU top surface are in total contact to avoid CPU overheating problem that would cause your system to hang or be unstable.*

Installing the Memory

The MB740 board supports one DDR memory socket for a maximum total memory of 1GB in DDR memory type.

Installing and Removing Memory Modules

To install the DDR modules, locate the memory slot on the board and perform the following steps:

1. Hold the DDR module so that the key of the DDR module align with those on the memory slot.
2. Gently push the DDR module in an upright position until the clips of the slot close to hold the DDR module in place when the DDR module touches the bottom of the slot.
3. To remove the DDR module, press the clips with both hands.

Setting the Jumpers

Jumpers are used on MB740 to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on MB740 and their respective functions.

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Jumper Locations on MB740

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JP9: 1394 EPROM Write Selection..... 10
JP12: Clear CMOS Setting 10
JP14: RTL8110S-32 LAN Enable / Disable..... 10

JP8: CompactFlash Slave/Master Selection (option)

Remarks: The CF socket and its corresponding slave/master Selection is optional.

JP8	CF Setting
Short	Master
Open	Slave

JP9: 1394 EPROM Write Selection

JP9	1394 EPROM
Short	For EPROM Write
Open	Normal

JP12: Clear CMOS Setting

JP12	Setting
1 2 3	Normal
1 2 3	Clear CMOS

JP14: RTL8110S-32 LAN Enable / Disable

JP14	Gigabit LAN
Short	Disable
Open	Enable

Connectors on MB740

The connectors on MB740 allows you to connect external devices such as keyboard, floppy disk drives, hard disk drives, printers, etc. The following table lists the connectors on MB740 and their respective functions.

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PCI1: PCI Slot (supports 2 Master) 19
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Connector Locations on MB740

Remarks: GB LAN and 1394 are options found on MB740F only.

KBMS1: PS/2 Keyboard and PS/2 Mouse Connectors

PS/2 Mouse

PS/2 Keyboard

Signal Name	Keyboard	Mouse	Signal Name
Keyboard data	1	1	Mouse data
N.C.	2	2	N.C.
GND	3	3	GND
5V	4	4	5V
Keyboard clock	5	5	Mouse clock
N.C.	6	6	N.C.

CN3: COM1 and VGA Connector

Signal Name	Pin #	Pin #	Signal Name
DCD	1	6	DSR
RXD	2	7	RTS
TXD	3	8	CTS
DTR	4	9	RI
GND	5	10	Not Used

Signal Name	Pin #	Pin #	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
N.C.	9	10	GND
N.C.	11	12	N.C.
HSYNC	13	14	VSYNC
NC	15		

CN4: 10/100 RJ-45 and USB1/2 Ports

CN5: 1394 Connector

J3: SPDIF Out Connector

CN6: GbE RJ-45 and USB3/4 Ports

CN7: Audio Connector

The audio connector, from top to bottom, is composed of Line in, Line out and Microphone jacks.

PWR1: ATX Power Supply Connector

Signal Name	Pin #	Pin #	Signal Name
3.3V	13	1	3.3V
-12V	14	2	3.3V
Ground	15	3	Ground
PS-ON	16	4	+5V
Ground	17	5	Ground
Ground	18	6	+5V
Ground	19	7	Ground
-5V	20	8	Power good
+5V	21	9	5VSB
+5V	22	10	+12V
+5V	23	11	+12V
Ground	24	12	+3.3V

FAN1: System Fan Power Connector

FAN1 is a 3-pin header for system fans. The fan must be a 12V (500mA) fan.

Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection

FAN2: CPU Fan Power Connector

FAN2 is a 3-pin header for the CPU fan. The fan must be a 12V fan. ***The CPU fan has a Smart Fan function that can be enabled with the BIOS.***

Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection

IDE1, IDE2: 40-pin and 44-pin IDE Connectors

IDE1

Signal Name	Pin #	Pin #	Signal Name
Reset IDE	1	2	Ground
Host data 7	3	4	Host data 8
Host data 6	5	6	Host data 9
Host data 5	7	8	Host data 10
Host data 4	9	10	Host data 11
Host data 3	11	12	Host data 12
Host data 2	13	14	Host data 13
Host data 1	15	16	Host data 14
Host data 0	17	18	Host data 15
Ground	19	20	Protect pin
DRQ0	21	22	Ground
Host IOW	23	24	Ground
Host IOR	25	26	Ground
IOCHRDY	27	28	Host ALE
DACK0	29	30	Ground
IRQ14	31	32	No connect
Address 1	33	34	No connect
Address 0	35	36	Address 2
Chip select 0	37	38	Chip select 1
Activity	39	40	Ground

IDE2

Signal Name	Pin #	Pin #	Signal Name
Reset IDE	1	2	Ground
Host data 7	3	4	Host data 8
Host data 6	5	6	Host data 9
Host data 5	7	8	Host data 10
Host data 4	9	10	Host data 11
Host data 3	11	12	Host data 12
Host data 2	13	14	Host data 13
Host data 1	15	16	Host data 14
Host data 0	17	18	Host data 15
Ground	19	20	Key
DRQ0	21	22	Ground
Host IOW	23	24	Ground
Host IOR	25	26	Ground
IOCHRDY	27	28	Host ALE
DACK0	29	30	Ground
IRQ14	31	32	No connect
Address 1	33	34	No connect
Address 0	35	36	Address 2
Chip select 0	37	38	Chip select 1
Activity	39	40	Ground
Vcc	41	42	Vcc
Ground	43	44	N.C.

FDD1: Floppy Drive Connector

FDD1is a slim 26-pin connector and will support up to 2.88MB FDD.

Signal Name	Pin #	Pin #	Signal Name
VCC	1	2	INDEX
VCC	3	4	DRV_SEL
VCC	5	6	DSK_CH
NC	7	8	NC
NC	9	10	MOTOR
DINST	11	12	DIR
NC	13	14	STEP
GND	15	16	WDATA
GND	17	18	WGATE
GND	19	20	TRACK
NC	21	22	WPROT
GND	23	24	RDATA
GND	25	26	SIDE

CN1: Digital I/O

Signal Name	Pin	Pin	Signal Name
GND	1	2	VCC
OUT3	3	4	OUT1
OUT2	5	6	OUT0
IN3	7	8	IN1
IN2	9	10	IN0

J1: USB5/6 Port Pin Header

Signal Name	Pin	Pin	Signal Name
Vcc	1	5	Ground
D-	2	6	D+
D+	3	7	D-
Ground	4	8	Vcc

CN2: COM2 Serial Port

COM2

Signal Name	Pin #	Pin #	Signal Name
DCD, Data carrier detect	1	6	DSR, Data set ready
RXD, Receive data	2	7	RTS, Request to send
TXD, Transmit data	3	8	CTS, Clear to send
DTR, Data terminal ready	4	9	RI, Ring indicator
GND, ground	5	10	Not Used

J2: 1394 Pin Header

Signal Name	Pin	Pin	Signal Name
TPA+	1	2	TPB+
TPA-	3	4	TPB-
+12V	5	6	NC
GND7	7	8	NC

J4: Mini PCI Connector

J5: System Function Connector

Signal Name	Pin	Pin	Signal Name
Ground	1	2	PS_ON
Power LED	3	4	Ground
5V	5	6	HDD Active
Ground	7	8	Reset

ATX power on switch: Pins 1-2
Power LED: Pins 3-4
HDD LED: Pins 5-6
Reset switch: Pins 7-8

J6: Front Audio Connector

Signal Name	Pin	Pin	Signal Name
Rear Audio R	1	2	Rear Audio L
Front Audio R	3	4	Front Audio L
Ground	5	6	Ground
MIC1/MICPWR	7	8	MIC2

REMARKS: To use the front audio connector, the jumpers from pin 1-3 and pin 2-4 must be removed.

J7: CD-In Pin Header

Pin #	Signal Name
1	CD Audio L
2	Ground
3	Ground
4	CD Audio R

CN8: Speaker Connector

The CN8 connector supports 2W/8ohm stereo audio power amplifier.

Pin #	Signal Name
1	Audio R
2	Ground
3	Ground
4	Audio L

CN9, CN10: Serial ATA Connectors

CN11: Compact Flash Connector

J13: IrDA Connector

Pin #	Signal Name
1	+5V
2	No connect
3	Ir RX
4	Ground
5	Ir TX

PCI1: PCI Slot (supports 2 Master)

AGP1: MicroAGP Socket

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BIOS Setup

This chapter describes the different settings available in the Award BIOS that comes with the board. The topics covered in this chapter are as follows:

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Save & Exit Setup 39
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BIOS Introduction

The Award BIOS (Basic Input/Output System) installed in your computer system's ROM supports Intel/AMD processors. The BIOS provides critical low-level support for a standard device such as disk drives, serial ports and parallel ports. It also adds virus and password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

BIOS Setup

The Award BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the Award BIOS is immediately activated. Pressing the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again. The following message will appear on the screen:

```
Press  <DEL>  to  Enter  Setup
```

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Phoenix - AwardBIOS CMOS Setup Utility

Standard CMOS Features Advanced BIOS Features Advanced Chipset Features Integrated Peripherals Power Management Setup PnP/PCI Configurations PC Health Status	Frequency/Voltage Control Load Fail-Safe Defaults Load Optimized Defaults Set User Password Save & Exit Setup Exit Without Saving
ESC : Quit F10 : Save & Exit Setup	↑ ↓ → ← : Select Item
Time, Date, Hard Disk Type…	

The section below the setup items of the Main Menu displays the control keys for this menu. At the bottom of the Main Menu just below the control keys section, there is another section, which displays information on the currently highlighted item in the list.

***Note**:* *If the system cannot boot after making and saving system changes with Setup, the Award BIOS supports an override to the CMOS settings that resets your system to its default.*

Warning: *It is strongly recommended that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both Award and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could cause the system to become unstable and crash in some cases.*

Standard CMOS Setup

"Standard CMOS Setup" choice allows you to record some basic hardware configurations in your computer system and set the system clock and error handling. If the motherboard is already installed in a working system, you will not need to select this option. You will need to run the Standard CMOS option, however, if you change your system hardware configurations, the onboard battery fails, or the configuration stored in the CMOS memory was lost or damaged.

Phoenix - AwardBIOS CMOS Setup Utility
Standard CMOS Features

		Item Help
Date (mm:dd:yy)	Wed, Apr 28, 2004	Menu Level >
Time (hh:mm:ss)	00 : 00 : 00	
IDE Channel 0 Master	None	Change the day, month,
IDE Channel 0 Slave	None	Year and century
IDE Channel 1 Master	None	
IDE Channel 1 Slave	None	
Drive A	None	
Drive B	None	
Video	EGA/VGA	
Halt On	All Errors	
Base Memory	640K	
Extended Memory	129024K	
Total Memory	130048K	

At the bottom of the menu are the control keys for use on this menu. If you need any help in each item field, you can press the <F1> key. It will display the relevant information to help you. The memory display at the lower right-hand side of the menu is read-only. It will adjust automatically according to the memory changed. The following describes each item of this menu.

Date

The date format is:

Day :	**Sun to Sat**
Month :	**1 to 12**
Date :	**1 to 31**
Year :	**1999 to 2099**

To set the date, highlight the “Date” field and use the PageUp/ PageDown or +/- keys to set the current time.

Time

The time format is: **Hour : 00 to 23**
Minute : 00 to 59
Second : 00 to 59

To set the time, highlight the “Time” field and use the <PgUp>/ <PgDn> or +/- keys to set the current time.

IDE Channel Master/Slave

The onboard PCI IDE connector provides Primary and Secondary channels for connecting up to two IDE hard disks or other IDE devices.

Press <Enter> to configure the hard disk. The selections include Auto, Manual, and None. Select ‘Manual’ to define the drive information manually. You will be asked to enter the following items.

CYLS :	Number of cylinders
HEAD :	Number of read/write heads
PRECOMP :	Write precompensation
LANDING ZONE :	Landing zone
SECTOR :	Number of sectors

The Access Mode selections are as follows:

CHS	(HD < 528MB)
LBA	(HD > 528MB and supports Logical Block Addressing)
Large	(for MS-DOS only)
Auto	

Remarks: The main board supports two serial ATA ports and are represented in this setting as IDE Channel 2 or 3.

Drive A / Drive B

These fields identify the types of floppy disk drive A or drive B that has been installed in the computer. The available specifications are:

360KB	1.2MB	720KB	1.44MB	2.88MB
5.25 in.	5.25 in.	3.5 in.	3.5 in.	3.5 in.

Video

This field selects the type of video display card installed in your system. You can choose the following video display cards:

EGA/VGA	For EGA, VGA, SEGA, SVGA or PGA monitor adapters. (default)
CGA 40	Power up in 40 column mode.
CGA 80	Power up in 80 column mode.
MONO	For Hercules or MDA adapters.

Halt On

This field determines whether or not the system will halt if an error is detected during power up.

No errors	The system boot will not be halted for any error that may be detected.
All errors	Whenever the BIOS detects a non-fatal error, the system will stop and you will be prompted.
All, But Keyboard	The system boot will not be halted for a keyboard error; it will stop for all other errors
All, But Diskette	The system boot will not be halted for a disk error; it will stop for all other errors.
All, But Disk/Key	The system boot will not be halted for a keyboard or disk error; it will stop for all others.

Advanced BIOS Features

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Phoenix - AwardBIOS CMOS Setup Utility
Advanced BIOS Features

		ITEM HELP
Hard Disk Boot Priority	Press Enter	
Virus Warning	Disabled	Menu Level >
CPU Internal Cache	Enabled	
Quick Power On Self Test	Enabled	
First Boot Device	CD-ROM	
Second Boot Device	Hard Disk	
Third Boot Device	LS120	
Boot Other Device	Enabled	
Swap Floppy Drive	Disabled	
Boot Up Floppy Seek	Disabled	
Boot Up NumLock Status	On	
Gate A20 Option	Fast	
Typematic Rate Setting	Disabled	
Typematic Rate (Chars/Sec)	6	
Typematic Delay (Msec)	250	
Security Option	Setup	
APIC Mode	Enabled	
MPS Version Control for OS	1.4	
OS Select For DRAM>64MB	Non-OS2	
HDD S.M.A.R.T. Capability	Disabled	
Video BIOS Shadow	Enabled	
Small Logo (EPA) Show	Enabled	

Hard Disk Boot Priority

With the field, there is the option to choose, aside from the hard disks connected, “Bootable add-in Cards” which refers to other external devices.

Virus Warning

If this option is enabled, an alarm message will be displayed when trying to write on the boot sector or on the partition table on the disk, which is typical of the virus.

CPU Internal Cache

Cache memory is additional memory that is much faster than conventional DRAM (system memory). CPUs from 486-type on up contain internal cache memory, and most, but not all, modern PCs have additional (external) cache memory. When the CPU requests data, the system transfers the requested data from the main DRAM into cache memory, for even faster access by the CPU. These items allow you to enable (speed up memory access) or disable the cache function. By default, these items are enabled.

Quick Power On Self Test

When enabled, this field speeds up the Power On Self Test (POST) after the system is turned on. If it is set to *Enabled*, BIOS will skip some items.

First/Second/Third Boot Device

These fields determine the drive that the system searches first for an operating system. The options available include *Floppy*, *LS120*, *Hard Disk*, *CDROM*, *ZIP100*, *USB-Floppy*, *USB-ZIP*, *USB-CDROM*, *LAN* and *Disable*.

Boot Other Device

These fields allow the system to search for an OS from other devices other than the ones selected in the First/Second/Third Boot Device.

Swap Floppy Drive

This item allows you to determine whether or not to enable Swap Floppy Drive. When enabled, the BIOS swaps floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A. By default, this field is set to ***Disabled.***

Boot Up Floppy Seek

This feature controls whether the BIOS checks for a floppy drive while booting up. If it cannot detect one (either due to improper configuration or its absence), it will flash an error message.

Boot Up NumLock Status

This allows you to activate the NumLock function after you power up the system.

Gate A20 Option

This field allows you to select how Gate A20 is worked. Gate A20 is a device used to address memory above 1 MB.

Typematic Rate Setting

When disabled, continually holding down a key on your keyboard will generate only one instance. When enabled, you can set the two typematic controls listed next. By default, this field is set to ***Disabled.***

Typematic Rate (Chars/Sec)

When the typematic rate is enabled, the system registers repeated keystrokes speeds. Settings are from 6 to 30 characters per second.

Typematic Delay (Msec)

When the typematic rate is enabled, this item allows you to set the time interval for displaying the first and second characters. By default, this item is set to ***250msec.***

Security Option

This field allows you to limit access to the System and Setup. The default value is ***Setup***. When you select *System*, the system prompts for the User Password every time you boot up. When you select *Setup,* the system always boots up and prompts for the Supervisor Password only when the Setup utility is called up.

APIC Mode

APIC stands for Advanced Programmable Interrupt Controller. The default setting is ***Enabled***.

MPS Version Control for OS

This option is specifies the MPS (Multiprocessor Specification) version for your operating system. MPS version 1.4 added extended configuration tables to improve support for multiple PCI bus configurations and improve expandability. The default setting is ***1.4***.

OS Select for DRAM > 64MB

This option allows the system to access greater than 64MB of DRAM memory when used with OS/2 that depends on certain BIOS calls to access memory. The default setting is ***Non-OS/2***.

HDD S.M.A.R.T. Capability

By default, this field is disabled. SMART stands for Self-Monitoring Analysis and Reporting Technology.

Video BIOS Shadow

This parameter, when enabled, turns on BIOS ROM shadowing for the block of memory normally used for standard VGA video ROM code, which is C0000 to C7FFF (32K). See here for a full description of what ROM shadowing does; in short, it speeds up your system by copying the contents of your video BIOS code from the slow ROM in which it resides into faster RAM

Small Logo (EPA) Show

The EPA logo appears at the right side of the monitor screen when the system is boot up. The default setting is ***Enabled***.

Advanced Chipset Features

This Setup menu controls the configuration of the chipset.

Phoenix - AwardBIOS CMOS Setup Utility
Advanced Chipset Features

		ITEM HELP
DRAM Clock/Timing Control	Press Enter	Menu Level >
Advanced Host Control	Press Enter	
AGP & P2P Bridge Control	Press Enter	
OnChip AGP Control	Press Enter	
System BIOS Cacheable	Enabled	
Video RAM Cacheable	Enabled	

DRAM Clock Timing Control

The fields in this option and their respective default settings are as follows:

Current CPU Frequency
Current DRAM Frequency
DRAM Frequency (By SPD)
Auto Configuration (Normal)
DDR Input Terminate Ctrl (OFF)

Advanced Host Control

The fields in this option and their respective default settings are as follows:

Memory Hole at 15M-16M (Disabled)
C1 State Disconnect (Disabled)
C2 State Disconnect (Disabled)
C3 State Disconnect (Disabled)
C1 State Self-Refresh (Disabled)
C2 State Self-Refresh (Disabled)
C3 State Self-Refresh (Disabled)
CPU Command ACK Limit (8)

AGP & P2P Bridge Control

The fields in this option and their respective default settings are as follows:

AGP Aperture Size (64MB)
AGP Fast Write Support (Disabled)
AGP Data Transfer Rate (Auto)

OnChip AGP Control

The fields in this option and their respective default settings are as follows:

Dual Display Support (Disabled)
VGA Share Memory Size (32MB)
Display Device Setting (Disabled); default is CRT1+LVDS for the Display Device when the setting is enabled.
LCD Setting (Enabled); to set the display type and resolution.
TV Setting (Disabled); to set the mode (NTSC), Type and YpbPr mode.
Graphics Engine Clock (133MHz)

System BIOS Cacheable

The setting of *Enabled* allows caching of the system BIOS ROM at F000h-FFFFFh, resulting in better system performance. However, if any program writes to this memory area, a system error may result.

Video BIOS Cacheable

The Setting *Enabled* allows caching of the video BIOS ROM at C0000h-F7FFFh, resulting in better video performance. However, if any program writes to this memory area, a system error may result.

Memory Hole At 15M-16M

In order to improve performance, certain space in memory can be reserved for ISA cards. This memory must be mapped into the memory space below 16 MB. The choices are *Enabled* and *Disabled*.

Integrated Peripherals

This section sets configurations for your hard disk and other integrated peripherals. The first screen shows three main items for user to select. Once an item selected, a submenu appears. Details follow.

Phoenix - AwardBIOS CMOS Setup Utility
Integrated Peripherals

		ITEM HELP
SIS OnChip IDE Device	Press Enter	Menu Level >
SIS OnChip PCI Device	Press Enter	
Onboard SuperIO Device	Press Enter	
IDE HDD Block Mode	Enabled	
Init Display First	PCI Slot	
USB0 Access Interface	EDB Bus	
USB1 Access Interface	EDB Bus	
USB2 Access Interface	EDB Bus	
USB2,0 Access Interface	EDB Bus	
MAC Access Interface	EDB Bus	
Audio Access Interface	EDB Bus	

Phoenix - AwardBIOS CMOS Setup Utility
SIS OnChip IDE Device

		ITEM HELP
Internal PCI/IDE	Both	Menu Level >
IDE Primary Master PIO	Auto	
IDE Primary Slave PIO	Auto	
IDE Secondary Master PIO	Auto	
IDE Secondary Slave PIO	Auto	
Primary Master UltraDMA	Auto	
Primary Slave UltraDMA	Auto	
Secondary Master UDMA	Auto	
Secondary Slave UDMA	Auto	
Secondary Slave UDMA	Auto	
IDE DMA transfer access	Enabled	
IDE Burst Mode	Enabled	

Phoenix - AwardBIOS CMOS Setup Utility
SIS OnChip PCI Device

		ITEM HELP
SIS USB Controller	Enabled	Menu Level >
USB Ports Number	6 Ports	
USB 2.0 Supports	Enabled	
USB Keyboard Support	Disabled	
USB Mouse Support	Disabled	
SIS AC97 Audio	Enabled	
SIS 10/100M Ethernet	Enabled	
SIS Serial ATA Controller	Enabled	
SIS Serial ATA Mode	IDE	

Phoenix - AwardBIOS CMOS Setup Utility
SIS OnChip PCI Device

Onboard FDC Controller	Enabled	ITEM HELP
Onboard Serial Port 1	3F8/IRQ4	Menu Level >
Onboard Serial Port 2	2F8/IRQ3	
UART Mode Select	Normal	
UR2 Duplex Mode	Half	

IDE HDD Block Mode

This field allows your hard disk controller to use the fast block mode to transfer data to and from your hard disk drive.

Init Display First

The default setting is ***PCI Card***.

IDE DMA Transfer Access

This field, by default, is enabled

IDE Primary/Secondary Master/Slave PIO

These fields allow your system hard disk controller to work faster. Rather than have the BIOS issue a series of commands that transfer to or from the disk drive, PIO (Programmed Input/Output) allows the BIOS to communicate with the controller and CPU directly.

The system supports five modes, numbered from 0 (default) to 4, which primarily differ in timing.

Primary/Secondary Master/Slave UltraUDMA

These fields allow your system to improve disk I/O throughput to 33Mb/sec with the Ultra DMA/33 feature.

Onboard FDC Controller

Select *Enabled* if your system has a floppy disk controller (FDC) installed on the motherboard and you wish to use it. If you install an add-in FDC or the system has no floppy drive, select Disabled in this field. This option allows you to select the onboard FDD port.

Onboard Serial Port

These fields allow you to select the onboard serial ports and their addresses. The default values for these ports are:

Serial Port 1	3F8/IRQ4
Serial Port 2	2F8/IRQ3

Power Management Setup

Phoenix - AwardBIOS CMOS Setup Utility
Power Management Setup

		ITEM HELP
ACPI Function	Enabled	
ACPI Suspend	S1(POS)	
Power Management	User Define	Menu Level >
Suspend Type	Disabled	
Video Off Option	Susp, Stby ->Off	
Video Off In Suspend	Yes	
Switch Function	Break/Wake	
Modem Use IRQ	NA	
Hot Key Function As	Power Off	
HDD Off After	Disabled	
Power Button Override	Instant-Off	
Power State Resume Control	Always Off	
PM Wake Up Events	**Press Enter**	

ACPI Function

Enable this function to support ACPI (Advance Configuration and Power Interface).

ACPI Suspend Type

The default setting of the ACPI Suspend mode is ***S1(POS)***.

Power Management

This field allows you to select the type of power saving management modes. There are four selections for Power Management.

Min. Power Saving	Minimum power management
Max. Power Saving	Maximum power management.
User Define	Each of the ranges is from 1 min. to 1hr. Except for HDD Power Down which ranges from 1 min. to 15 min.

Suspend Mode

The default setting is ***Disabled***.

Video Off Option

This field defines the Video power saving features.

- Always on: System BIOS will never turn off the screen.
- Suspend => Off: Screen off when system is in SUSPEND mode.
- Susp, Stby => Off: Screen off when system is in STANDBY or SUSPEND mode.
- All modes => Off: Screen off when system is in DOZE, STANDBY or SUSPEND mode.

Video Off Method

This field defines the Video Off features. There are three options.

V/H SYNC + Blank	Default setting, blank the screen and turn off vertical and horizontal scanning.
DPMS	Allows BIOS to control the video display.
Blank Screen	Writes blanks to the video buffer.

Switch Function

The default setting is ***Break/Wake***.

Modem Use IRQ

This field sets the IRQ used by the Modem. By default, the setting is ***3***.

Hot Key Function As

The default setting is ***Power Off***.

HDD Off After

The default setting is ***Disabled***.

Power Button Override

The default setting is ***Off***. This field determines the state of the computer after a power failure. If set to Off, the system will not boot when power returns. If set to On, the system will restart when power returns.

Power State Resume Control

The default setting is ***Always Off***.

PM Wake Up Events

Users can enable system events (IRQ, Ring Power Up, MACPME Power Up, PCIPME Power Up, PS2KB Wakeup, PS2MS Wakeup, Power up by Alarm) to wake up the system.

PNP/PCI Configurations

This option configures the PCI bus system. All PCI bus systems on the system use INT#, thus all installed PCI cards must be set to this value.

Phoenix - AwardBIOS CMOS Setup Utility
PnP/PCI Configurations

Reset Configuration Data	Disabled	Menu Level
Resources Controlled By	Auto (ESCD)	
IRQ Resources	Press Enter	
PCI/VGA Palette Snoop	Disabled	

Reset Configuration Data

This field allows you to determine whether to reset the configuration data or not. The default value is ***Disabled.*** Select Enabled to reset Extended System Configuration Data when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the OS cannot boot.

Resources Controlled by

This PnP BIOS can configure all of the boot and compatible devices with the use of a PnP operating system such as Windows 95.

PCI/VGA Palette Snoop

Some non-standard VGA display cards may not show colors properly. This field allows you to set whether or not MPEG ISA/VESA VGA cards can work with PCI/VGA. When this field is enabled, a PCI/VGA can work with an MPEG ISA/VESA VGA card. When this field is disabled, a PCI/VGA cannot work with an MPEG ISA/VESA card.

PC Health Status

This section shows the parameters in determining the PC Health Status. These parameters include temperatures, fan speeds and voltages.

Phoenix - AwardBIOS CMOS Setup Utility
PC Health Status

		ITEM HELP
Shutdown Temperature	Disabled	
Vcore(V)	1.02 V	Menu Level >
2.6V		
Vcc3.3V		
Vcc5V		
+12V		
SB 3.3V		
-12V		
SB 5V		
Voltage Battery		
CPU TEMP		
SYSTEM TEMP		
POWER TEMP		
SYSTEM FAN Speed		
CPU FAN Speed		
SmartFAN	Disabled	

Temperatures/Voltages

These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.

Shutdown Temperature

This field allows the user to set the temperature by which the system automatically shuts down once the threshold temperature is reached. This function can help prevent damage to the system that is caused by overheating.

Frequency/Voltage Control

This section shows the user how to configure the processor frequency.

Phoenix - AwardBIOS CMOS Setup Utility
Frequency/Voltage Control

		ITEM HELP
Auto Detect DIMM/PCI Clk	Disabled	Menu Level >
Spread Spectrum	Disabled	

Auto Detect PCI Clk

This field enables or disables the auto detection of the PCI clock.

Spread Spectrum

This field sets the value of the spread spectrum. The default setting is ***Disabled***. This field is for CE testing use only.

Load Fail-Safe Defaults

This option allows you to load the troubleshooting default values permanently stored in the BIOS ROM. These default settings are non-optimal and disable all high-performance features.

Load Optimized Defaults

This option allows you to load the default values to your system configuration. These default settings are optimal and enable all high performance features.

Set Password

User Password sets a password that will be used exclusively on the system. To specify a password, highlight the type you want and press <Enter>. The Enter Password: message prompts on the screen. Type the password, up to eight characters in length, and press <Enter>. The system confirms your password by asking you to type it again. After setting a password, the screen automatically returns to the main screen.

To disable a password, just press the <Enter> key when you are prompted to enter the password. A message will confirm the password to be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

Save & Exit Setup

This option allows you to determine whether or not to accept the modifications. If you type “Y”, you will quit the setup utility and save all changes into the CMOS memory. If you type “N”, you will return to Setup utility.

Exit Without Saving

Select this option to exit the Setup utility without saving the changes you have made in this session. Typing “Y” will quit the Setup utility without saving the modifications. Typing “N” will return you to Setup utility.

This page is intentionally left blank.

Drivers Installation

This section describes the installation procedures for software and drivers under the Windows 2000 and Windows XP. The software and drivers are included with the motherboard. If you find the items missing, please contact the vendor where you made the purchase. The contents of this section include the following:

SIS 741CX Chipset VGA Driver 42
SIS Chipset Ethernet Driver 45
Realtek Gigabit Ethernet Driver 46
Realtek AC97 Codec Driver 47

SIS 741CX Chipset VGA Driver

1. Insert the CD that comes with the board. Click ***TI/ALi/SiS Chipset*** and then ***SiS741CX/SiS964 Chipset Drivers***.

2. When the welcome screen to the InstallShield Wizard appears, click Next.

3. Click Next. (Select Typical setup, as default.).

4. Click Next, when asked to select the Program Folder listed.

5. Click Next for Setup to start the copying process.

6. When prompted, click ***Finish*** to restart the computer and for changes to take effect.

.

SIS Chipset Ethernet Driver

1. Insert the CD that comes with the board. Click ***TI/Ali/SiS Chipset*** and then ***SiS PCI Fast Ethernet Adapter Driver***.

2. When the InstallShield Wizard appears, click Next to continue with the Ethernet drivers installation.

3. After the drivers are installed succesfully, you will be promted to restart the computer. Restart the computer for changes to take effect.

Realtek Gigabit Ethernet Driver

1. Insert the CD that comes with the board. Click ***LAN Card*** on the left side and then ***Realtek Network Interface Controller Drivers*** to execute the REALTEK Gigabit and Fast Ethernet NIC Driver Setup.

2. When the maintenance is complete, click Finish to complete the drivers setup.

Realtek AC97 Codec Driver

1. Insert the CD that comes with the board. Click ***TI/Ali/SiS Chipset*** and then ***Realtek AC'97 Codec Audio Driver***.

2. When the welcome screen to the InstallShield Wizard appears, click Next to proceed with the Realtek AC97 Audio Setup.

3. InstallShield Wizard is not complete and you are prompted to restart your computer. Restart the computer for changes to take effect.

Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
278 - 27F	Parallel Port #2(LPT2)
2F8h - 2FFh	Serial Port #2(COM2)
2B0 - 2DF	Graphics adapter Controller
378h - 3FFh	Parallel Port #1(LPT1)
360 - 36F	Network Ports
3B0 - 3BF	Monochrome & Printer adapter
3C0 - 3CF	EGA adapter
3D0 - 3DF	CGA adapter
3F0h - 3F7h	Floppy Disk Controller
3F8h - 3FFh	Serial Port #1(COM1)

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Reserved
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1
IRQ8	Real Time Clock
IRQ9	Reserved
IRQ10	Reserved
IRQ11	Reserved
IRQ12	PS/2 Mouse
IRQ13	80287
IRQ14	Primary IDE
IRQ15	Secondary IDE

C. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODES:

```
File name:Main.CPP
//==========================================================
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT
// WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
// TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A
// PARTICULAR PURPOSE.
//
//==========================================================
#include <stdio.h>
#include <stdlib.h>
#include "ITE8705.H"
//==========================================================
int main (int argc, char *argv[]);
void copyright(void);
void EnableWDT(int);
void DisableWDT(void);
//==========================================================
int main (int argc, char *argv[])
{
        unsigned char bTime;
        char **endptr;

        copyright();

        if (argc != 2)
        {
                printf(" Parameter incorrect!!\n");
                return 1;
        }

if (Init_ITE8705() == 0)
{
        printf(" ITE8705 is not detected, program abort.\n");
        return 1;
}
        bTime = strtol (argv[1], endptr, 10);
        printf("System will reset after %d seconds\n", bTime);

        EnableWDT(bTime);

        return 0;
}
//==========================================================
void copyright(void)
```

```
{
        printf("\n  ITE8705 Watch Timer Tester (AUTO DETECT)  \n"\
                        "       Usage : ITE8705 reset_time\n"\
                        "       Ex : ITE8705 3  => reset system after 3 second\n"\
                        "           ITE8705 0  => disable watch dog timer\n");
}
//==========================================================



void EnableWDT(int interval)
{

        Set_ITE8705_LD( 0x05);                          //Set Logic Device 5
        Set_ITE8705_Reg( 0xFB, 0x88);                   //Enable WDT

        Set_ITE8705_Reg( 0xFC, 0x36);                    //Set GPIO Mapping
        Set_ITE8705_Reg( 0xFD, interval);                //set timer

}
//==========================================================
void DisableWDT(void)
{
        Set_ITE8705_LD(0x05);                                   //switch to logic device 8
        Set_ITE8705_Reg(0xFB, 0x00);                            //clear watchdog timer
        Set_ITE8705_Reg(0xFD, 0x00);                            //watchdog disabled
}
//==========================================================
→


File name: ITE8705.CPP
//==========================================================
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT
// WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
// TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A
// PARTICULAR PURPOSE.
//
//==========================================================
#include "ITE8705.H"
#include <dos.h>
//==========================================================
unsigned int ITE8705_BASE;
void Unlock_ITE8705 (void);
void Lock_ITE8705 (void);
//==========================================================
unsigned int Init_ITE8705(void)
{
        unsigned int result;    //0=NA,1=ITE8705

        ITE8705_BASE = 0x2E;
        result = Get_ITE8705_Reg(0x21);
        if (result == 0x05)
        {
                result = 1;
                goto Init_Finish;
        }

        ITE8705_BASE = 0x4E;
        result = Get_ITE8705_Reg(0x21);
        if (result == 0x05)
        {
```

```
                result = 1;
                goto Init_Finish;
        }

        ITE8705_BASE = 0x00;
        result = 0;

Init_Finish:
        return (result);
}
//==========================================================
void Unlock_ITE8705 (void)
{
        outportb(ITE8705_INDEX_PORT, ITE8705_UNLOCK1);
        outportb(ITE8705_INDEX_PORT, ITE8705_UNLOCK2);
        outportb(ITE8705_INDEX_PORT, ITE8705_UNLOCK3);

if (ITE8705_BASE == 0x2E)
        outportb(ITE8705_INDEX_PORT, ITE8705_UNLOCK3);
else
        outportb(ITE8705_INDEX_PORT, ITE8705_UNLOCK4);
}
//==========================================================
void Lock_ITE8705 (void)

{
      outportb(ITE8705_INDEX_PORT, ITE8705_LOCK);
}
//==========================================================
void Set_ITE8705_LD( unsigned char LD)
{
        Unlock_ITE8705();
        outportb(ITE8705_INDEX_PORT, ITE8705_REG_LD);
        outportb(ITE8705_DATA_PORT, LD);
        Lock_ITE8705();
}
//==========================================================
void Set_ITE8705_Reg( unsigned char REG, unsigned char DATA)
{
        Unlock_ITE8705();
        outportb(ITE8705_INDEX_PORT, REG);
        outportb(ITE8705_DATA_PORT, DATA);
        Lock_ITE8705();
}
//==========================================================
unsigned char Get_ITE8705_Reg(unsigned char REG)
{
        unsigned char Result;
        Unlock_ITE8705();
        outportb(ITE8705_INDEX_PORT, REG);
        Result = inportb(ITE8705_DATA_PORT);
        Lock_ITE8705();
        return Result;
}
//==========================================================→
```

File name:ITE8705.H

```
//=============================================================
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT
// WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
// TO THE   IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A
// PARTICULAR  PURPOSE.
//
//=============================================================
#ifndef __ITE8705_H
#define __ITE8705_H                    1
//=============================================================
#define        ITE8705_INDEX_PORT          (ITE8705_BASE)
#define        ITE8705_DATA_PORT           (ITE8705_BASE+1)
//=============================================================
#define        ITE8705_REG_LD              0x07
//=============================================================
#define        ITE8705_IO_PORT             0x0803
//=============================================================
#define ITE8705_UNLOCK1                    0x87
#define ITE8705_UNLOCK2                    0x01
#define ITE8705_UNLOCK3                    0x55
#define ITE8705_UNLOCK4                    0xAA
#define ITE8705_LOCK                   0xFF
//=============================================================
unsigned int Init_ITE8705(void);
void Set_ITE8705_LD( unsigned char);
void Set_ITE8705_Reg( unsigned char, unsigned char);
unsigned char Get_ITE8705_Reg( unsigned char);
//=============================================================
#endif  //__ITE8705_H
```

D. Digital I/O Sample Code

File name: Main.CPP

```
//-----------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT
// WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
// TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A
// PARTICULAR
// PURPOSE.
//-----------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "ITE8705.H"
//-----------------------------------------------------------------------------
void ClrKbBuf(void);
int main (int argc, char *argv[]);
void SetDioOutput(unsigned char);
unsigned char GetDioInput(void);

//-----------------------------------------------------------------------------
int main (int argc, char *argv[])
{
        if (Init_ITE8705() == 0)
        {

                printf("Can not detect ITE8705, program abort.\n");
                return(1);
        }

<!--[if !supportEmptyParas]--> <!--[endif]-->

        printf("Current DIO input is 0%X\n", GetDioInput());

<!--[if !supportEmptyParas]--> <!--[endif]-->

        printf("Set DIO output to high\n");
        SetDioOutput(0x0F);

<!--[if !supportEmptyParas]--> <!--[endif]-->

        printf("Set DIO output to low\n");
        SetDioOutput(0x00);

<!--[if !supportEmptyParas]--> <!--[endif]-->

        return 0;
}
//-----------------------------------------------------------------------------
void SetDioOutput(unsigned char data)
{
        Set_ITE8705_LD( 0x05);                                  //switch to logic device 7
      outportb(ITE8705_IO_PORT, ((data & 0x0F) << 4));
}
//-----------------------------------------------------------------------------
unsigned char GetDioInput(void)
```

```
{
        unsigned char result;

        Set_ITE8705_LD(0x05);                                   //switch to logic device 7
      result = inportb(ITE8705_IO_PORT) & 0x0F;
        return (result);
}
//-----------------------------------------------------------------------
void ClrKbBuf(void)
{
        while(kbhit())
        {       getch();        }
}
//-----------------------------------------------------------------------

→
File name:ITE8705.CPP

//==============================================================
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT
// WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
// TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A
// PARTICULAR
// PURPOSE.
//
//==============================================================
#include "ITE8705.H"
#include <dos.h>
//==============================================================
unsigned int ITE8705_BASE;
void Unlock_ITE8705 (void);
void Lock_ITE8705 (void);
//==============================================================
unsigned int Init_ITE8705(void)
{
        unsigned int result;    //0=NA,1=ITE8705

        ITE8705_BASE = 0x2E;
        result = Get_ITE8705_Reg(0x21);
        if (result == 0x05)
        {
                result = 1;
                goto Init_Finish;
        }

        ITE8705_BASE = 0x4E;
        result = Get_ITE8705_Reg(0x21);
        if (result == 0x05)
        {
                result = 1;
                goto Init_Finish;
        }

        ITE8705_BASE = 0x00;
        result = 0;

Init_Finish:
        return (result);
}
//==============================================================
void Unlock_ITE8705 (void)
{
        outportb(ITE8705_INDEX_PORT, ITE8705_UNLOCK1);
```

```
        outportb(ITE8705_INDEX_PORT, ITE8705_UNLOCK2);
        outportb(ITE8705_INDEX_PORT, ITE8705_UNLOCK3);
if (ITE8705_BASE == 0x2E)
        outportb(ITE8705_INDEX_PORT, ITE8705_UNLOCK3);
else
        outportb(ITE8705_INDEX_PORT, ITE8705_UNLOCK4);
}
//=============================================================
void Lock_ITE8705 (void)
{
        outportb(ITE8705_INDEX_PORT, ITE8705_LOCK);
}
//=============================================================
void Set_ITE8705_LD( unsigned char LD)
{
        Unlock_ITE8705();
        outportb(ITE8705_INDEX_PORT, ITE8705_REG_LD);
        outportb(ITE8705_DATA_PORT, LD);
        Lock_ITE8705();
}
//=============================================================
void Set_ITE8705_Reg( unsigned char REG, unsigned char DATA)
{
        Unlock_ITE8705();
        outportb(ITE8705_INDEX_PORT, REG);
        outportb(ITE8705_DATA_PORT, DATA);
        Lock_ITE8705();
}
//=============================================================
unsigned char Get_ITE8705_Reg(unsigned char REG)
{
        unsigned char Result;
        Unlock_ITE8705();
        outportb(ITE8705_INDEX_PORT, REG);
        Result = inportb(ITE8705_DATA_PORT);
        Lock_ITE8705();
        return Result;
}
//=============================================================→
```

File name: ITE8705.H

```
//=============================================================
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT
// WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
// TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A
// PARTICULAR
// PURPOSE.
//
//=============================================================
#ifndef __ITE8705_H
#define __ITE8705_H                     1
//=============================================================
#define     ITE8705_INDEX_PORT          (ITE8705_BASE)
#define     ITE8705_DATA_PORT           (ITE8705_BASE+1)
//=============================================================
#define     ITE8705_REG_LD              0x07
//=============================================================
#define     ITE8705_IO_PORT             0x0803
//=============================================================
#define ITE8705_UNLOCK1                 0x87
#define ITE8705_UNLOCK2                 0x01
```

```
#define ITE8705_UNLOCK3                 0x55
#define ITE8705_UNLOCK4                 0xAA
#define ITE8705_LOCK                                    0xFF
//==========================================================
unsigned int Init_ITE8705(void);
void Set_ITE8705_LD( unsigned char);
void Set_ITE8705_Reg( unsigned char, unsigned char);
unsigned char Get_ITE8705_Reg( unsigned char);
//==========================================================
#endif  //__ITE8705_H
→
```