

**33MHz Zero-Wait 80386  
Turbo Main Board**

MB

-1333C-CH

-1340C-CH



(B)

*Users  
Manual*



**Thanks for your  
smart choice for the product**

**\***

**From now on you will enjoy the  
highest quality**

**&**

**sound after-service**

**Date: 10-18-1991**

Product of the  
United States of America

It is the policy of the  
United States of America

to support the  
free world

# Contents

## Preface

About This Manual

<b>1. Introduction</b>	<b>1</b>
<b>2. Features</b>	<b>3</b>
<b>3. Installation</b>	
3.1-1 Check Point	5
3.1-2 Whole Assemble	12
3.1-3 Keyboard Speed Select	13
<b>4. AMI BIOS SETUP</b>	<b>14</b>
4.1 Stand CMOS Setup	24
4.2 Advance CMOS Setup	30
4.3 Advance Chipset Setup	41
4.4 Change Password	42
4.5 Hard Disk Utility	48
<b>5. System Board Technical Reference</b>	
5.1 System Board Block Diagram..	61
5.2 Description	62
5.3 System Hardware Configuration	
5.3-1 System Memory Map	64
5.3-2 System I/O Address Map	65
5.3-3 DMA Channels	67
5.3-4 Interrupt	67
5.3-5 CMOS RAM Address Map	68
5.3-6 Real Time Clock (RTC) Information.	69
5.3-7 I/O Channel	70
5.4 System Function Control- Index Register	76
<b>6. Trouble Shooting</b>	<b>100</b>

# Preface

## About This Manual

The purpose of this manual is to introduce you the Main Board. This manual is divided into six chapters.

- Chapter 1 will introduce you this Main Board.
- Chapter 2 will introduce you this Main Board's features.
- Chapter 3 provides you the correct installation methods when you want to assemble it by yourself.
- Chapter 4 gives you a overview of SETUP program.
- Chapter 5 provides detail technical reference.
- Chapter 6 Trouble Shooting

*The information in this document is subject to change without notice*

### Trademarks

IBM, IBM PC, IBM PC/XT, IBM/AT, and PC-DOS are registered trademarks of International Business Machines Corp.

80286, 386, 387, iAPX and Intel are registered trademarks of Intel Corporation.

MS-DOS is a registered trademark of Microsoft Corporation.

AMD is a registered trademark of Advanced Micro Devices, Inc.

Award is a registered trademark of Award Software Inc.

AMI is a registered trademark of American Megatrends Inc.

CHIP, PEAK and PEAK/DM are trademarks of Chips and Technologies Incorporated.

Lotus is a registered trademark of Lotus Development Corporation.

Motorola is a registered trademark of Motorola.

# Introduction

---

## 1. Introduction

The system board is approximately 21.8 by 33 centimeters (8.6 by 13 inches) and uses three chips VLSI implementation of the system logic required to implement a cache based 386 DX system. This chip set is designed to offer a 100% PCAT compatible integrated solution. It has the following components:

1. Controller enhances 80386 CPU and memory system performance due to simultaneous activation of cache and DRAM access

Near Zero Wait State memory access

Zero Wait State non-pipelined read hit access

Buffered write through DRAM update scheme to minimize write cycle-penalty

Supports 64KB, and 256KB direct mapped cache

Supports 4 blocks (of variable size 4KB to 4MB) of main memory as non-cacheable address space

7 channel Direct Memory Access (DMA)

16 level interrupt

System clock

Three programmable times

2. 80387 and Weitek 3167 co-processor interface logic

3. Flexible memory architecture-Supports up to 64 MB of local memory programmable wait states and RAS pre-charge time for each block or pair of banks

Supports staggered RAS during refresh

Supports hidden and burst refresh

Supports single 512K EPROMS

4. Supports shadowing of BIOS EPROMS
5. High Cache Hit Rate
6. Integrated high speed cache tag comparator
7. Programmable write 0 or 1 wait state, posted or non-posted writes
8. Rechargeable battery backup for CMOS configuration table and real-time clock
9. 8 Input/Output (I/O) slots:
  - 5 with a 36 and a 62 pin card-edge socket
  - 3 with only the 62 pin card-edge socket

# Features

---

## 2. Features

This Main Board has the following features:

- \* INTEL 80386 32-BIT Operation at 33/40 MHz. Chip Sets by C&T Inc.
- \* PGA socket for INTEL 80387 or WEITEK 3167 co-processor
- \* AMI Legal BIOS and C&T Legal BIOS
- \* Page Interleave memory supports single bank page mode, 2/4 way Interleave mode.
- \* Shadow RAM for BIOS & Video ROM to improve system performance.
- \* CPU speed can be switched by both Hardware/Software
- \* I/O bus clock is fixed at 8.33 MHz operation for compatibility with a lot of I/O cards
- \* Memory subsystem
  - C&T BIOS ROM alternatively available with built-in SETUP utilities
  - Supporting memory up to 32MB on board, expandable up to 100MB
  - DRAM type support 256K & 1M SIMM Module and 4M SIMM Module speed 80ns.

## Features

---

\* **Bus controller subsystem**

- Three 8-bit I/O channel connectors
- Five 16-bit I/O channel connectors

\* **Front pannel supporting: Power/Turbo Speed, Reset, Keylock**

\* **4 Layer P.C.B design to improve system reliability**

Software under test	33 MHz	40 MHz
Landmark Ver 1.14	55.0	64.6
Power Meter MIPS Ver 1.5	7.79	8.383

\* **Baby size Mainboard (22 x 33 cm or 8.67" x 13")**

\* **Offers the highest performance for DOS, OS/2, Windows, Novell, UNIX System V/386 applications, iRMX, iRMK, Kernels.**

\* **On board cache for 64K, 256K**

\* **SRAM fype support 16K x 4 or 64K x 4**

\* **TAG RAM type support 16K x 4 or 64K x 4 (w/24pin)**

# Installation

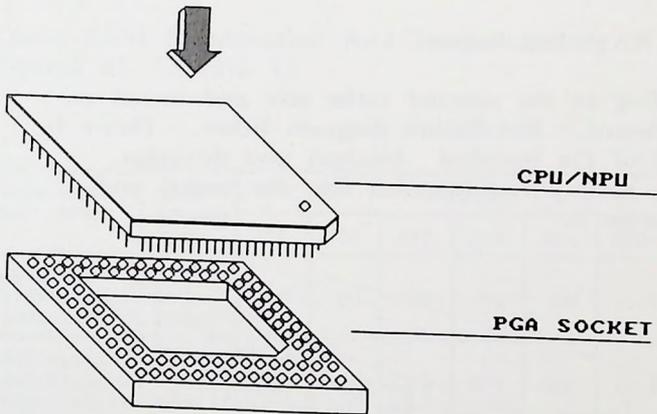
---

## 3. Installation

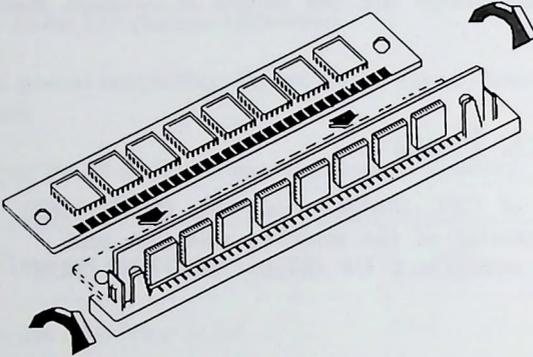
Because computer is composed by complicate components that should be assembled by professionals to avoid any mistakes. Listed below are the simple installation methods.

### 3.1-1 Check Point

- A. Installation of CPU (80386) and NPU (80387/3167).  
Please be careful of the installed direction and location of mainboard U4 (80386) and U13 (80387/3167).

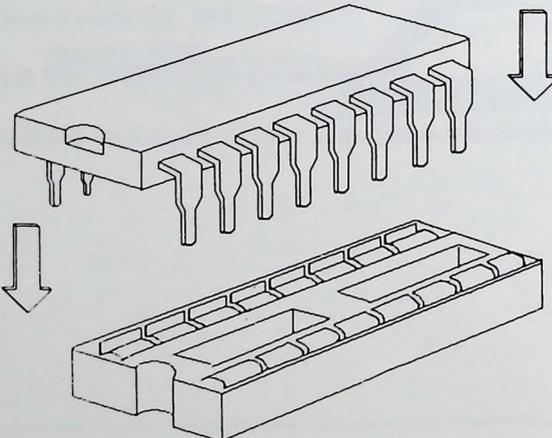


- B. Use 256K , 1MB SIMM DRAM or 4MB SIMM DRAM to install on the Main Board. Please refer to the following diagram.



- C. Cache RAM Installation:

According to the selected cache size and install on main board. Installation diagram below. Please be careful of the installed location and direction. Ensure each pin is installed into the socket and then press it.



## Installation

---

D. Check with all the jumper and connector explanation

Jumper No.	No. of Pin	Description	Default Setting
J21	2	Reserved for factory diagnostics	OFF
J22	2	ON: Enable fast gate A20 OFF: Disable fast gate A20	ON
J23	2	ON: Select color monitor	
J42	3	1-2 Discharge the power of CMOS RAM in real time clock	1-2

2-3 Normal, Operation

E. Cache RAM Combination And Jumper Setting  
Speed at 33 MHz :

Cache TAG	RAM RAM	SRAM Access Time	Jumper						
			J25	J26	J27	J28	J29	J33	J34
64K	Cache (16Kx4)x8pcs (16Kx4)x2pcs	25ns 20ns	ON	ON	ON	ON	ON	(1-2)	(1-2)
256K	Cache (64Kx4)x8pcs (64Kx4)x3pcs	25ns 20ns	OFF	OFF	OFF	OFF	OFF	(2-3)	(2-3)

CPU	Clock	Speed	Cache RAM	TAG RAM
	40 MHz		20 ns	15 ns

ON means short ; OFF means open  
 (1-2) means short Pin 1 and Pin 2  
 (2-3) means short Pin 2 and Pin 3

## F. Memory Combination And Jumper Setting

DRAM Access Time: 80ns

DRAM Type: 256KB/1MB SIMM Module

Memory Size	Bank0	Bank1	Jumper J48
1M	256KBx4pcs	-----	(2-3)
2M	256KBx4pcs	256KBx4pcs	(2-3)
4M	1MBx4pcs	-----	(2-3)
8M	1MBx4pcs	1MBx4pcs	(2-3)
16M	4MBx4pcs	-----	(2-3)
32M	4MBx4pcs	4MBx4pcs	(2-3)

(2-3) means short J48 Pin 2 and Pin 3.

Memory Size	Bank0	Bank1	Jumper J48
5M	256KBx4pcs	1MBx4pcs	(1-2)
	1MBx4pcs	256KBx4pcs	(1-2)
17M	256KBx4pcs	4MBx4pcs	(1-2)
	4MBx4pcs	256KBx4pcs	(1-2)
20M	1MBx4pcs	4MBx4pcs	(1-2)
	4MBx4pcs	1MBx4pcs	(1-2)

(1-2) means short J48 Pin 1 and Pin 2.

## Installation

---

### G. Connectors

Connector Name	Pin Assignments	Function
JP2 External Battery Connector	Pin 1:+6VDC Pin 2:No Connection Pin 3: No Connection Pin 4:Ground	When On-Board rechargeable battery is out work. Connect the 6V external battery to JP2 and take out the On-Board rechargeable battery (BTI).
J50 Turbo Connector	Pin 1:Turbo Input Pin 2:Ground	Off:High Speed (25/33MHz) On:Low Speed (8MHz)
Turbo LED Connector:	Pin 1: Negative End of Turbo LED Pin 2: VCC (+5VDC)	If the connection is correct,the LED will light up.If the system is in the turbo mode others,the LED will turn off.
Reset Connector:	Pin 1: Reset Input Pin 2: Ground	Connect the Reset connector to the Reset switch of the front panel of chassis. Press and hold down the Reset button for at least one second to reset the system.

Connector No.	Pin Assignments	Function
J19 Keylock Connector	Pin 1:LED Power Pin 2:No Connection Pin 3:Ground Pin 4:Keyboard Inhibit Pin 5:Ground	This connector provide the power for LED and the Electrical interlock, such as a key-activated switch on the front panel of the chassis. You can use the switch to lock out the keyboard.
J18 Speaker Connector	Pin 1:Speaker Drive Output Pin 2:Key (Pin Missing) Pin 3:Ground Pin 4:+5 VDC	Connector J18 provides an interface to the speaker for audible tone generation.
J1 Power Connector	Pin 1:Power Good Signal Pin 2:+5VDC Pin 3:+12VDC Pin 4:-12VDC Pin 5-Pin 8:Ground Pin 9:-5VDC Pin 10-Pin 12:+5VDC	This connector is used for connecting the power from power supply to the system board.

## Installation

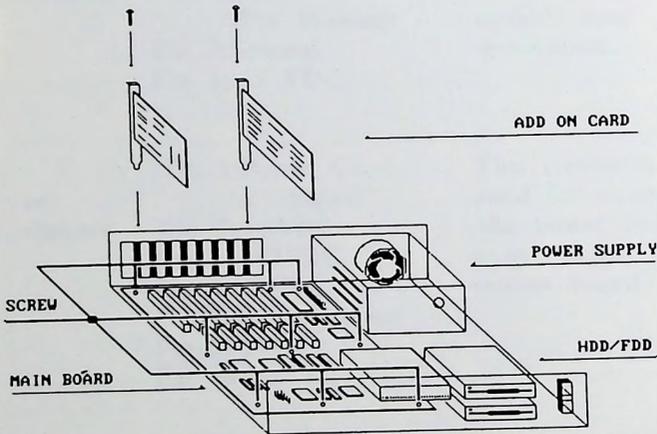
---

J3 Keyboard Connector	Pin 1:Keyboard Clock	This connector is used for connecting the keyboard to the system board.
	Pin 2:Keyboard Data	
	Pin 3:Spare	
	Pin 4:Ground	
	Pin 5:+5VDC	

All other jumpers which are not described in this manual are for factory testing purpose.

## 3.1-2 Whole Assemble

- A. Insert the power supply into Case and fix it.
- B. Insert the floppy, hard disk into Case and fix it.
- C. then insert the main board and fix it with screw.
- D. Install the ADD On Card.
- E. Connected with the LED, keyboard.....etc.
- F. Turn on the power and ready for booting.
- G. Make sure the system is well installed before turning on your system.
- H. Upon booting fail, please make a prompt contact with your dealer or professional engineers.



### 3.1-3 Keyboard Speed Select

System speed switch is selectable via hardware switch or keyboard.

\* via keyboard:

Press <CTRL> <ALT> <+> key for turbo speed selection or press <CTRL> <ALT> <-> key for normal speed selection.

## 4. AMI BIOS SETUP

### Running AMI BIOS:

When the system is powered on, the BIOS will enter the Power-On Self Test (POST) routines.

The AMI BIOS performs the various diagnostic checks at the time the system is powered up; if an error is encountered, the error will be reported in one of two different ways. If the error occurs before the display device is initialized, a series of beeps will be transmitted.

If the error occurs after the display device is initialized, the screen will display the error message. In the case of a non-fatal error, a prompt to press the <F1> key may also appear on the screen.

### **WARNING !**

Please boot up the system periodically , in order to keep CMOS SETUP data correct. Otherwise rechargeable battery power is not enough , CMOS SETUP losses data sometimes.

If a problem occurs with the system, copy these reference numbers down before consulting your system manufacturer.

To "freeze" the screen, power on the system and hold a key down on the keyboard. This will cause a "Keyboard Error" message to appear on the screen and the system will wait for the <F1> key to be pressed. At this point, you may copy the three lines down and then press <F1> to continue the boot procedure.

**NOTE:** If the "Wait for <f1> If any Error option in the Advanced CMOS Setup Program of the BIOS SETUP program is set to "Disabled", it should be set to enabled prior to using this method to freeze the screen.

After the POST routines are completed, the following message appears:

"Hit <DEL> if you want to run SETUP"

To access the AMI BIOS SETUP program, press the <DEL> key.

The screen in Figure 1.2 will be displayed at this time.

A record of the computer's system parameters (such as amount of memory, disk drives, video displays, and numeric coprocessors) is stored in the CMOS (Complementary Metal Oxide Semiconductor) memory. When the computer is turned off, a back-up battery retains the system parameters in the CMOS memory.

Each time the system is powered-on, it is configured with these values, unless the CMOS has been corrupted or is faulty. AMI's SETUP program is resident in the ROM BIOS (Read Only Memory Basic input/Output System) so that it is available each time the computer is turned on.

If, for some reason, the CMOS becomes corrupted, the system is configured with the default values stored in this ROM file. There are two (2) sets of BIOS values stored in the ROM file: the BIOS Setup default values and the Power-On default values.

The BIOS Setup default values are those which should provide optimum performance for the system. They are the best case default values.

The Power-On defaults, which are the worst case defaults, are the stable values for the system. They are to be used if the system is performing erratically because of hardware problems.

Listed below is an explanation of the keys displayed at the bottom of the screens accessed through the BIOS SETUP program:

**ESC:** Exit to previous screen.

**ARROW KEYS:** Use arrow keys to move cursor to desired selection.

**PAGEUP/PAGEDOWN/CTRL-PAGEUP/CTRL-PAGEDOWN:** Modify the default value of the options for the highlighted feature. If there are less than 10 available options, the Ctrl PageU and PageDown keys function the same as the PageUp and PageDown keys.

**F1:** Displays help screen for selected feature.

**F2/F3:** Changes background and foreground colors.

**F5:** Retrieves the values which were resident when current setup session was started. These values will be CMOS values if the CMOS was uncorrupted at the start of the session, or they will be the BIOS Setup default values.

**F6:** Loads all features in the Advanced CMOS Setup/Advanced Chip Set Setup with the BIOS Setup defaults.

**F7:** Loads all features in the Advanced CMOS Setup/Advanced Chip Set Setup with the Power-On defaults.

**F10:** Saves all changes made to Setup and exists program.

# AMI BIOS SETUP

---

**NOTE:** The default value for the prompts which occur when the <F5>, <F6>, and <F7> keys are pressed is always <N> (No). Actually executing these options requires changing the <N> to <Y> (Yes) and pressing <ENTER>.

The generic menu options of the BIOS SETUP Program are shown in Figure 1.2.

Figure 1.2 BIOS Setup Menu

BIOS SETUP PROGRAM - AMI BIOS SETUP UTILITIES (C) 1990 American Megatrends Inc., All Rights Reserved
STANDARD CMOS SETUP ADVANCED CMOS SETUP ADVANCED CHIPSET SETUP AUTO CONFIGURATION WITH BIOS DEFAULTS AUTO CONFIGURATION WITH POWER - ON DEFAULTS CHANGE PASSWORD HARD DISK UTILITY WRITE TO CMOS AND EXIT DO NOT WRITE TO CMOS AND EXIT
Standard CMOS Setup for Changing Time, Date, Hard Disk Type, etc.
ESC:Exit, ↑ ↓ → ← :Select, F2/F3:Color, F10:Save & Exit

A warning message, shown in Figure 1.3, is displayed each time one of the first three options (Standard CMOS Setup, Advanced CMOS Setup, and Advanced Chip Set Setup) is selected, before any changes are allowed to any of the setup parameters.

Figure 1.3 BIOS Setup Warning Message Screen

```
BIOS SETUP PROGRAM - WARNING INFORMATION
(C) 1990 American Megatrends Inc., All Rights Reserved

Improper Use of Setup may Cause Problems!!

If System Hangs. Reboot System and Enter Setup by Pressing the "ESC" key

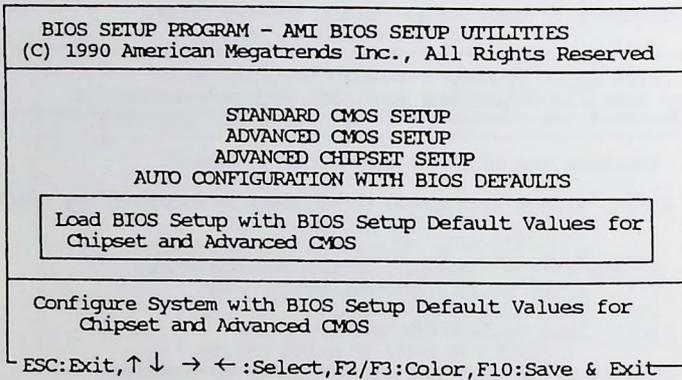
Do any of the following After Entering Setup
(i) After Options to make System Work
(ii) Load BIOS Setup Defaults
(iii) Load Power-On Defaults

Hit <ESC> to stop now any other key to continue
```

## AUTO CONFIGURATION WITH BIOS DEFAULTS

The Auto Configuration With BIOS feature uses the default system values before the user has changed any CMOS values. If the CMOS is corrupted, the BIOS defaults will automatically be loaded.

Figure 1.4 BIOS Default Auto Configuration Screen



If you wish to use the BIOS defaults, change the prompt to <Y> and press <ENTER>. The following message will appear on the screen:

"Default values loaded. Press any key to continue."

## AUTO CONFIGURATION WITH POWER-ON DEFAULTS

This feature uses the default Power-On values. You may wish to use this option as a diagnostic aid if your system is behaving erratically.

Figure 1.5 Power On Default Auto Configuration Screen

```
BIOS SETUP PROGRAM - AMI BIOS SETUP UTILITIES
(C) 1990 American Megatrends Inc., All Rights Reserved

STANDARD CMOS SETUP
ADVANCED CMOS SETUP
ADVANCED CHIPSET SETUP
AUTO CONFIGURATION WITH BIOS DEFAULTS
AUTO CONFIGURATION WITH POWER - ON DEFAULTS
CHANGE PASSWORD
HARD DISK UTILITY
WRITE TO CMOS AND EXIT
DO NOT WRITE TO CMOS AND EXIT

Standard CMOS Setup for Changing Time, Date, Hard Disk
Type, etc.

ESC:Exit,↑↓ → ← :Select,F2/F3:Color,F10:Save & Exit
```

If you wish to use the Power-On defaults, change the prompt to <Y> and press <ENTER>. The following message will appear on the screen:

"Default values loaded. Press any key to continue."

## WRITE TO CMOS AND EXIT

The features selected and configured in the Standard Setup, Advanced CMOS Setup, Advanced Chip Set Setup, and the New Password Setup will be stored in the CMOS when this option is taken. The CMOS checksum is calculated and written to the CMOS. Control is then passed back to BIOS.

Figure 1.6 Write to CMOS Exit Screen

```
BIOS SETUP PROGRAM - AMI BIOS SETUP UTILITIES
(C) 1990 American Megatrends Inc., All Rights Reserved

STANDARD CMOS SETUP
ADVANCED CMOS SETUP
ADVANCED CHIPSET SETUP
AUTO CONFIGURATION WITH BIOS DEFAULTS
Write to CMOS and Exit (Y/N)? N

Write the setting to the CMOS and EXIT
ESC:Exit,↑↓→←:Select,F2/F3:Color,F10:Save & Exit
```

Pressing <N> (No) and <ENTER> will return you to the Main Menu.

Pressing <Y> (Yes) and <ENTER> will save the system parameters and continue with the booting process.

## DO NOT WRITE TO CMOS AND EXIT

This option passes control back to BIOS without writing any changes to the CMOS.

Figure 1.7 CMOS Exit Screen

```
BIOS SETUP PROGRAM - AMI BIOS SETUP UTILITIES
(C) 1990 American Megatrends Inc., All Rights Reserved

STANDARD CMOS SETUP
ADVANCED CMOS SETUP
ADVANCED CHIPSET SETUP
AUTO CONFIGURATION WITH BIOS DEFAULTS
  Want to Quit without Saving (Y/N) ? N

Do Not Write the setting to the CMOS and EXIT
ESC:Exit,↑↓ → ← :Select,F2/F3:Color,F10:Save & Exit
```

Pressing <N> (No) and <ENTER> will return the user to the Main Menu.

Pressing <Y> (Yes) and <ENTER > will continue with the booting process without saving any system parameters.

## 4.1 Standard CMOS Setup

Standard CMOS Setup is the first option on the main setup menu. Press <ENTER> at the highlighted selection to access this option. The screen in Figure 2 will appear.

Figure 2 Standard CMOS Setup Screen

BIOS SETUP PROGRAM - STANDARD CMOS SETUP  
(C) Copyright 1990. American Megatrends Inc. All Rights Reserved

---

Date (mn/date/year): Thu, Jan 31, 1991	Base memory: 640KB
Time (hour/min/sec): 15:23:15	Ext. memory: 0 KB
Daylight saving : Disabled	
Hard disk C: type : 47=User Type	Cylin Head WPcom LZone Sect Size
Hard disk D: type : Not Installed	1314 7 1314 1314 17 76MB
Floppy drive A: : 1.2 MB, 5 1/4"	
Floppy drive B: : Not Install	
Primary display : Not Install	
Keyboard : Not Install	

	Sun	Mon	Tue	Wed	Thu	Fri	Sat
28	29	30	31	1	2	3	
4	5	6	7	8	9	10	
11	12	13	14	15	16	17	
18	19	20	21	22	23	24	
25	26	27	28	29	30	1	
2	3	4	5	6	7	8	

Month: Jan, Feb,.....Dec  
Date : 01,02,03,.....31  
Year : 1901,1902,.....2099

ESC: Exit ↑↓ → ← : Select      F2/F3: Color    PU/PD: Modify

The Standard CMOS Setup utility is used to configure the following features:

- \* **Date:** Month, Date, and Year. Ranges for each value are listed below in prompt box in the lower left corner of the CMOS Setup Screen (Figure 2.1).
- \* **Time:** Hour, Minute, and Second. Uses 24 hour clock format, i.e., for PM numbers, add 12 to the hour. You would enter 4:30 P.M. as 16:30:00.
- \* **Daylight Savings:** Disabled or Enabled.
- \* **Hard Disk C and Hard Disk D:** Hard disk types from 1 to 46 are standard ones; type 47 is user definable. The user must enter the hard disk parameters for each drive.

**NOTE:** The USER definition entry allows you to perform a test on a disk drive not defined in ROM. The USER definition entry is valid only during the period that the test is performed.

The drive types are identified by the following characteristics:

- \* **Type**            This is the number designation for a drive with certain identification parameters.
- \* **Cyl.**            This is the number of cylinders found in the specified drive type .

## AMI BIOS SETUP

---

- \* **Heads**            This is the number of heads found in the specified drive type.
  
- \* **WPcom**            WPcom is the read delay circuitry which takes into account the timing differences between the inner and outer edges of the surface of the disk platter. The number designates the starting cylinder of the signal.
  
- \* **L-zone**            L-zone is the landing zone of the heads. This number determines the cylinder location where the heads will normally park when the system is shut down.
  
- \* **Capacity**        This is the formatted capacity of the drive based on the following formula:

(#of heads)X(#of cylinders)X(17 secs/cyl.)X(512 bytes/sec)

## AMI BIOS SETUP

---

Listed below are the attributes for disk types 1 through 46.

Type	Cyln	Head	WPcom	LZone	Sect	Size
1	306	4	128	305	17	10 MB
2	615	4	300	615	17	20 MB
3	615	6	300	615	17	31 MB
4	940	8	512	940	17	62 MB
5	940	6	512	940	17	47 MB
6	615	4	65535	615	17	20 MB
7	462	8	256	511	17	31 MB
8	733	5	65535	733	17	30 MB
9	900	15	65535	981	17	112 MB
10	820	3	65535	828	17	20 MB
11	855	5	65535	855	17	35 MB
12	855	7	65535	855	17	50 MB
13	306	8	128	319	17	28 MB
14	733	7	65535	733	17	43 MB
16	612	4	0	663	17	20 MB
17	977	5	300	977	17	41 MB
18	977	7	65535	977	17	57 MB
19	1024	7	512	1024	17	60 MB
20	733	5	300	732	17	30 MB
21	733	7	300	732	17	43 MB
22	733	5	300	733	17	30 MB
23	306	4	0	336	17	10 MB
24	925	7	0	925	17	54 MB
25	925	9	65535	925	17	69 MB
26	754	7	754	754	17	44 MB
27	754	11	65535	754	17	69 MB
28	699	7	256	699	17	41 MB
29	823	10	5535	823	17	68 MB
30	918	7	918	918	17	53 MB
31	1024	11	65535	1024	17	94 MB

## AMI BIOS SETUP

---

Type	Cyln	Head	WPcom	LZone	Sect	Size
32	1024	15	65535	1024	17	128 MB
33	1024	5	1024	1024	17	43 MB
34	612	2	128	612	17	10 MB
35	1024	9	65535	1024	17	77 MB
36	1024	8	512	1024	17	68 MB
37	615	8	128	615	17	41 MB
38	987	3	987	987	17	25 MB
39	987	7	987	987	17	57 MB
40	820	6	820	820	17	41 MB
41	977	5	977	977	17	41 MB
42	981	5	981	981	17	41 MB
43	830	7	512	830	17	48 MB
44	830	10	65535	830	17	69 MB
45	917	15	65535	918	17	114 MB
46	1224	15	65535	1223	17	152 MB

"Not installed" is available for use as an option. This option could be used for diskless workstations and SCSI hard disks. Type 47 may be used for both hard disks C: and D:.

The parameters for type 47 under Hard Disk C: and Hard Disk D: may be different, which effectively allows 2 different user-definable hard disk types.

- \* Floppy Drive A and Floppy Drive B: The options are 360 KB 5 1/4", 1.2 MB 5 1/4", 720 KB 3 1/2", 1.44MB 3 1/2", and Not installed. Not installed could be used as an option for diskless workstations.
  
- \* Primary Display: Options are Monochrome, Color 40x25, VGA/PGA/EGA, Color 80x25, and Not installed. The Not Installed option could be used for network file servers.
  
- \* Keyboard: Options are installed or Not installed.

## 4.2 Advanced CMOS Setup

The Advanced CMOS Setup program is equipped with a series of help screens, accessed by the <F1> key, which will display the options available for a particular configuration feature and special help for some of the options.

The options for the following features of the Advanced CMOS setup are either "Disabled or Enabled:"

Typematic Rate Programming  
Extended Memory Test  
Memory Test Tick Sound  
Memory Parity Error Check  
Hit <DEL> Message Display  
Wait for <F1> if Any Error

- \* Fast Gate A20 Option
- \* Video or Adapter ROM Shadow
- \* GA20 Line After System Boot

The options for the following features of the Advanced CMOS setup are either "Present" or "Absent:"

Numeric Processor

The options for Power-On Up Num Lock are "On" or "Off."

The options for System Boot Up Speed are "High" or "Low."

Note: Depending on the particular hardware and chip set combination of each individual system, the options in Figure 3.1 may or may not appear on the Setup Screen or they may not appear in the same order. There may also be more options for your system than those shown on the Setup screen.

Generic Screen

■ Figure 3.1 Advanced CMOS Setup Screen

BIOS SETUP PROGRAM - ADVANCED CMOS SETUP			
(C) 1990 American Megatrends Inc., All Rights Reserved			
Typematic Rate Programming	: Disabled	Password Checking Option	: Disabled
Typematic Rate Delay (msec)	: 500	Video ROM Shadow C000,16K	: Enabled
Typematic Rate (Chars/Sec)	: 15	Video ROM Shadow C400,16K	: Enabled
Above 1MB Memory Test	: Enabled	Adapter ROM Shadow C800,16K	: Disabled
Memory Test Tick Sound	: Enabled	Adapter ROM Shadow CC00,16K	: Disabled
Memory Parity Error Check	: Enabled	Adapter ROM Shadow D000,16K	: Disabled
Hit <DEL> Message Display	: Enabled	Adapter ROM Shadow D400,16K	: Disabled
Hard Disk Type 47 RAM Area	: 0:300	Adapter ROM Shadow D800,16K	: Disabled
Wait For <F1> Key If Any Error	: Enabled	Adapter ROM Shadow DC00,16K	: Disabled
System Boot Up Num Lock	: On	Adapter ROM Shadow E000,16K	: Disabled
Numeric Processor Test	: Enabled	Adapter ROM Shadow E400,16K	: Disabled
Waitk Processor	: Absent	Adapter ROM Shadow E800,16K	: Disabled
Floppy Driver Seek At Boot	: Enabled	Adapter ROM Shadow EC00,16K	: Disabled
System Boot Up Sequence	: A:, C:	System ROM Shadow F000,64K	: Enabled
System Boot Up CPU Speed	: High		
External Cache Memory	: Enabled		
Internal Cache Memory	: Enabled		
Fast Gate A20 Option	: Enabled		
ESC: Exit     — — :Sel, (Ctrl)Pu/Pd: Modify, F1: Help, F2/F3: Color F5: Old Vales, F6: BIOS Setup Defaults, F7: Power-on Defaults			

## AMI BIOS SETUP

---

A short description follows for each of the options on the Advanced CMOS Setup Screen. In addition, Figures 3.2 through 3.6 display the options which will appear on the Advanced CMOS Setup screen when the F1 Help key is pressed.

**Typematic Rate Programming:** By enabling this option, the user can adjust the rate at which a keystroke is repeated. The options "Typematic Rate Delay" and "Typematic Rate" affect this rate. When a key is pressed and held down, the character appears on the screen and after a delay set by the Typematic Rate Delay, it keeps on repeating at a rate set by the Typematic Rate value. When two or more keys are pressed and held down simultaneously, only the last key pressed will be repeated at the typematic rate. This stops when the last key pressed is released, even if other keys are depressed.

See figures 3.2 and 3.3 for the values for these rates.

# AMI BIOS SETUP

Figure 3.2 Typematic Rate Delay Help Screen

BIOS SETUP PROGRAM - ADVANCED CMOS SETUP (C) 1990. American Megatrends Inc. All Rights Reserved	
Typematic Rate Programming : Disabled	Password Checking Option : Disabled
Typematic Rate Delay(msec) : 500	Vj led
Typematic Rate (Chars/Sec) : 15.0	Vi led
Above 1 MB Memory Test : Disabled	Ac Typematic Rate Delay (msec)
Memory Test Tick Sound : Enabled	Ac led
Memory Parity Error Check : Disabled	Ac Available Options are : -
Hit <DEL> Message Display : Enabled	Ac 250
Hard Disk Type 47 RAM Area : 0:300	Ac 500
Wait for <F1> If Any Error : Enabled	Ac 750
System Boot Up Num Lock : On	Ac 1000
Numeric Processor Test : Enabled	Ac Press any key to continue
Weitek Processor : Absent	Sy led
Floppy Drive Seek At Boot : Enabled	Adaptor ROM Shadow EC00, 16K : Disabled
System Boot Up Sequence : A; C:	System ROM Shadow F000, 64K : Enabled
System Boot Up CPU Speed : High	
External Cache Memory : Enabled	
Internal Cache Memory : Disabled	
Fast Gate A20 Option : Enabled	
ESC: Exit, ↑ ↓ → ← :Sel, (Ctrl)PU/PD: Modify, F1: Help, F2/F3: Color	
F5: Old Values, F6: BIOS Setup Defaults, F7: Power-On Defaults	

# AMI BIOS SETUP

Figure 3.3 Typematic Rate Help Screen

BIOS SETUP PROGRAM - ADVANCED CMOS SETUP		(C) 1990. American Megatrends Inc. All Rights Reserved	
Typematic Rate Programming	: Disabled	Password Checking Option	: Disabled
Typematic Rate Delay(msec)	: 500	V	
Typematic Rate (Chars/Sec)	: 15,0	V	Typematic Rate (Chars/Sec)
Above 1 MB Memory Test	: Disabled	A	
Memory Test Tick Sound	: Enabled	A	Available Options are :-
Memory Parity Error Check	: Disabled	A	6
Hit <DEL> Message Display	: Enabled	A	8
Hard Disk Type 47 RAM Area	: 0:300	A	10
Wait for <F1> If Any Error	: Enabled	A	12
System Boot Up Num Lock	: On	A	15
Numeric Processor Test	: Enabled	A	20
Weitek Processor	: Absent	S	24
Floppy Drive Seek At Boot	: Enabled	A	30
System Boot Up Sequence	: A, C:	S	
System Boot Up CPU Speed	: High		
External Cache Memory	: Enabled		
Internal Cache Memory	: Disabled		
Fast Gate A20 Option	: Enabled		
Press any key to continue			

ESC: Exit, ↑↓ → ←:Sel, (Ctrl)PU/PD: Modify, F1: Help, F2/F3: Color  
 F5: Old Values, F6: BIOS Setup Defaults, F7: Power-On Defaults

**Extended Memory Test:** This feature, when enabled, will invoke the POST memory routines on the RAM above 1 MB (if present on the system). If disabled, the BIOS will only check the first 1 MB of RAM.

**Memory Test Tick Sound:** This option will enable (turn on) or disable (turn off) the "ticking" sound during the memory test.

**Memory Parity Error Check:** If the system board does not have parity RAM, the user may disable the memory parity error checking routines in the BIOS. The user should check with the manufacturer regarding the proper setting of this option.

**Hit <DEL> Message Display:** Disabling this option will prevent the message:

"Hit <DEL> if you want to run SETUP"  
 from appearing on the screen when the system boots-up.

**Hard Disk Type 47 Data Area:** The AMI BIOS SETUP features two user-definable hard disk types. Normally, the data for these disk types are stored at 0:300 in lower system RAM. If a problem occurs with other software, this data can be located at the upper limit of the DOS shell (640 KB). If the option is set to "DOS 1 KB," the DOS Shell is shortened to 639 KB, and the top KB is used for the hard disk data storage. Please refer to Figure 3.4 for this option.

Figure 3.4 Hard Disk Type 47 Data Area Help Screen

BIOS SETUP PROGRAM - ADVANCED CMOS SETUP (C) 1990. American Megatrends Inc. All Rights Reserved																							
Typematic Rate Programming : Disabled Typematic Rate Delay(msec) : 500 Typematic Rate (Chars/Sec) : 15.0 Above 1 MB Memory Test : Disabled Memory Test Tick Sound : Enabled Memory Parity Error Check : Disabled Hit <DEL> Message Display : Enabled Hard Disk Type 47 RAM Area : 0:300 Wait for <F1> If Any Error : Enabled System Boot Up Num Lock : On Numeric Processor Test : Enabled Weitek Processor : Absent Floppy Drive Seek At Boot : Enabled System Boot Up Sequence : A, C System Boot Up CPU Speed : High Internal Cache Memory : Enabled External Cache Memory : Disabled Fast Gate A20 Option : Enabled	<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%; padding: 2px;">Password Checking Option</td> <td style="width: 20%; text-align: right; padding: 2px;">: Disabled</td> </tr> <tr> <td colspan="2" style="border: 1px solid black; padding: 5px;"> <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%; padding: 2px;">Hard Disk Type 47 RAM Area</td> <td style="width: 20%; text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">If BIOS Shadow RAM is disabled,</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">RAM will be used for hard disk</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">type 47 parameter table.</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">Available Options are :-</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">0:300</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">DOS 1KB</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">Press any key to continue</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> </table> </td> </tr> <tr> <td colspan="2" style="padding: 2px;">System ROM Shadow F000, 64K : Enabled</td> </tr> </table>	Password Checking Option	: Disabled	<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%; padding: 2px;">Hard Disk Type 47 RAM Area</td> <td style="width: 20%; text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">If BIOS Shadow RAM is disabled,</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">RAM will be used for hard disk</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">type 47 parameter table.</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">Available Options are :-</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">0:300</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">DOS 1KB</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">Press any key to continue</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> </table>		Hard Disk Type 47 RAM Area	bled	If BIOS Shadow RAM is disabled,	bled	RAM will be used for hard disk	bled	type 47 parameter table.	bled	Available Options are :-	bled	0:300	bled	DOS 1KB	bled	Press any key to continue	bled	System ROM Shadow F000, 64K : Enabled	
Password Checking Option	: Disabled																						
<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%; padding: 2px;">Hard Disk Type 47 RAM Area</td> <td style="width: 20%; text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">If BIOS Shadow RAM is disabled,</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">RAM will be used for hard disk</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">type 47 parameter table.</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">Available Options are :-</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">0:300</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">DOS 1KB</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> <tr> <td style="padding: 2px;">Press any key to continue</td> <td style="text-align: right; padding: 2px;">bled</td> </tr> </table>		Hard Disk Type 47 RAM Area	bled	If BIOS Shadow RAM is disabled,	bled	RAM will be used for hard disk	bled	type 47 parameter table.	bled	Available Options are :-	bled	0:300	bled	DOS 1KB	bled	Press any key to continue	bled						
Hard Disk Type 47 RAM Area	bled																						
If BIOS Shadow RAM is disabled,	bled																						
RAM will be used for hard disk	bled																						
type 47 parameter table.	bled																						
Available Options are :-	bled																						
0:300	bled																						
DOS 1KB	bled																						
Press any key to continue	bled																						
System ROM Shadow F000, 64K : Enabled																							
<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%; border-right: 1px solid black; padding: 2px;">ESC: Exit, ↑ ↓ → ← : Sel, (Ctrl)PU/PD: Modify, F1: Help, F2/F3: Color</td> <td style="width: 50%; padding: 2px;">F5: Old Values, F6: BIOS Setup Defaults, F7: Power-On Defaults</td> </tr> </table>		ESC: Exit, ↑ ↓ → ← : Sel, (Ctrl)PU/PD: Modify, F1: Help, F2/F3: Color	F5: Old Values, F6: BIOS Setup Defaults, F7: Power-On Defaults																				
ESC: Exit, ↑ ↓ → ← : Sel, (Ctrl)PU/PD: Modify, F1: Help, F2/F3: Color	F5: Old Values, F6: BIOS Setup Defaults, F7: Power-On Defaults																						

**Wait for F1 If any Error:** Before the system boots-up, the BIOS will execute the POST routines, a series of system diagnostic routines. If any of these tests fail, but a non-fatal error has occurred and the system can still function, the BIOS will respond with an appropriate error message followed by the following statement:

"Press <F1> to continue."

If this option is disabled, any non-fatal error which occurs will not generate the above statement, but the BIOS will still display the appropriate error message. This will eliminate the need for any user response to a non-fatal error condition message.

**System boot Up Num Lock:** The user may turn off the "numlock" option on his Enhanced Keyboard when the system is powered on. This will allow him to use the arrow keys on the numeric keypad instead of using the other set of arrow keys on the Enhanced Keyboard. The BIOS will default to turning the "numlock" on.

**Numeric Processor(s):** These options allow the user to mark the numeric processor (Intel 80X87 or compatible) as present or absent.

**Floppy Drive Seek At Boot:** The default for this option is "disabled" to allow a fast boot and to decrease the possibility of damage to the heads.

**System Boot Up Sequence:** The AMI BIOS will normally attempt a boot from floppy drive A: ( if present), and if unsuccessful, it will attempt to boot from hard disk C: This sequence can be switched using this option. If the option is set to "C:, A:," the system will attempt to boot from the hard drive C:, and then A:. If the option is set to "A:, C:," the sequence is reversed. Please refer to Figure 3.5 for this option.

Figure 3.5 System Boot Up Sequence Help Screen

BIOS SETUP PROGRAM - ADVANCED CMOS SETUP (C) 1990. American Megatrends Inc. All Rights Reserved	
Typematic Rate Programming : Disabled Typematic Rate Delay(msec) : 500 Typematic Rate (Chars/Sec) : 15.0 Above 1 MB Memory Test : Disabled Memory Test Tick Sound : Enabled Memory Parity Error Check : Disabled Hit <DEL> Message Display : Enabled Hard Disk Type 47 RAM Area : 0:300 Wait for <F1> If Any Error : Enabled System Boot Up Num Lock : On Numeric Processor Test : Enabled Weitek Processor : Absent Floppy Drive Seek At Boot : Enabled System Boot Up Sequence : A:, C: System Boot Up CPU Speed : High External Cache Memory : Enabled Internal Cache Memory : Disabled Fast Gate A20 Option : Enabled	Password Checking Option : Disabled V led System Boot Up Sequence : led A: bled Available Options are :- bled C:, A: bled A:, C: bled A: bled Press any key to continue bled A: bled Adaptor ROM Shadow E400, 15K : Disabled System ROM Shadow E800, 64K : Disabled Adaptor ROM Shadow EC00, 16K : Disabled System ROM Shadow F000, 64K : Enabled
ESC: Exit, ↑ ↓ → ← : Sel, (Ctrl)PU/PD: Modify, F1: Help, F2/F3: Color F5: Old Values, F6: BIOS Setup Defaults, F7: Power-On Defaults	

**System Boot Up CPU Speed:** The speed at which the system will boot up is determined with this option. Choices for this option are "high" or "low." The default speed is "low."

## AMI BIOS SETUP

**Password Check Option:** Controlled by the system manufacturer's preferences, the password feature can be used to prevent unauthorized system boot-up or unauthorized use of BIOS SETUP. The option in the BIOS SETUP only allows the user to enable the password check option every time the system boots or upon entering SETUP only. A third option is to disable the password option entirely. See Figure 3-6.

Figure 3.6 Password Checking Option Screen

BIOS SETUP PROGRAM - ADVANCED CMOS SETUP (C) 1990. American Megatrends Inc. All Rights Reserved	
Typematic Rate Programming : Disabled Typematic Rate Delay(msec) : 500 Typematic Rate (Chars/Sec) : 15.0 Above 1 MB Memory Test : Disabled Memory Test Tick Sound : Enabled Memory Parity Error Check : Disabled Hit <DEL> Message Display : Enabled Hard Disk Type 47 RAM Area : 0:300 Wait for <F1> If Any Error : Enabled System Boot Up Num Lock : On Numeric Processor Test : Enabled Weitek Processor : Absent Floppy Drive Seek At Boot : Enabled System Boot Up Sequence : A; , C: System Boot Up CPU Speed : High External Cache Memory : Enabled Internal Cache Memory : Disabled Fast Gate A20 Option : Enabled	Password Checking Option : Disabled <div style="border: 1px solid black; padding: 5px; margin: 5px 0;">                         Password Checking Option                          Available Options are :-                          Disabled                          Setup                          Always                          Press any key to continue                     </div> System ROM Shadow E800, 64K : Disabled Adaptor ROM Shadow EC00, 16K : Disabled System ROM Shadow F000, 64K : Enabled
ESC: Exit, ↑ ↓ → ← : Sel, (Ctrl)PU/PD: Modify, F1: Help, F2/F3: Color F5: Old Values, F6: BIOS Setup Defaults, F7: Power-On Defaults	

The default option is "Disabled." The prompt for the password will not appear when the system is re-booted.

If the "Always" option is chosen at Setup, each time the system is turned on, i.e. "booted," the prompt for user password will appear.

If the "Setup" option is chosen at Setup, the password prompt will not appear when the system is turned on, but will appear if the user attempts to enter the Setup program.

The program allows three attempts to key in the correct password. After each incorrect attempt, the prompt to enter the current password will appear, followed by an "X." After the third incorrect attempt, the system will lock and it will be necessary to reboot. The screen will not display the characters entered.

See Section 5 for instructions on changing the user password.

**Fast Gate A20:** This option uses the fast gate A20 line, supported in some chip sets, to access any memory above 1 MB. Normally, all RAM access above 1 MB is handled through the keyboard controller chip. Using this option will make the access faster than the normal method. This option is very useful in networking operating systems.

**Video or Adaptor ROM Shadow:** ROM shadow is a procedure in which BIOS code is copied from slower ROM to faster RAM. The BIOS is then executed from the RAM. These options are chip set specific and are dependent on the system hardware. They may or may not appear on the BIOS screen. Each option, when it does appear, allows for a segment of 16 KB to be shadowed from ROM to RAM. If one of these options is enabled, and there is BIOS present in that particular 16 KB segment, the BIOS will be shadowed.

**System ROM Shadow:** The same concept applies here as above, except that in this case, the system BIOS (64 KB in length) is shadowed.

**Gate A20 Line After System Boot:** This option will enable or disable the use of Gate A20 after the system has booted. Gate A20 is an alternate method for accessing system RAM above 1 MB.

### 4.3 Advanced Chipset Setup

This portion of the BIOS Setup is entirely chip set specific and requires knowledge about the particular chip set in use. This option is used to change the register values for the chip set registers. These registers control most of the system options in the computer.

The screens and options will vary according to the particular BIOS chip set. See Figure 4.1 for the actual screens and options applicable to your system.

■ Figure 4.1 Advanced Chipset Setup Screen

BIOS SETUP PROGRAM - ADVANCED CMOS SETUP			
(C) 1990 American Megatrends Inc., All Rights Reserved			
Read/Write Cycle Wait State	: 3 W/S	RAS Compare Test Mode 1	: Enabled
16-bit DMA Wait States	: 1 W/S	Duble RAS Mode	: Enabled
8-bit DMA Wait States	: 1 W/S	Early LDBEN Mode	: Disabled
Extended DMA Memory Read	: Enabled	Addition Wait States	: Disabled
DMA Clock	: Bclk/2	Early MA Signal Release	: Enabled
Command Delay, 16-bit Cycle	: 0 Bclk	Eary CAS Mode	: Disabled
Command Delay, 8-bit Cycle	: 1 Bclk	Read Extra Wait State	: Disabled
AT Bus I/O Command Delay	: 1 Bclk	7CLK2 CAS Pulse Width	: Disabled
16-bit I/O Wait States	: 3 Bclk	Late RAS Mode	: Disabled
8-bit I/O Wait States	: 5 Bclk	RAS To Cas Delay	: Disabled
AT Bus Address Hold Time	: Disabled	Alter RAS Percharge	: 3.6 CLK2
Bus Clock Divider	: ATCLK	Force RAS High	: Disabled
Refresh Pulse Width	: 6 CLK2s	RAS Active Position	: Middle
RAS Precharge Time (Blk0)	: 6 CLK2s	Refresh type	: Hidden
RAS Precharge Time (Blk1)	: 6 CLK2s	Back To Back Memory Cycles	: 1 W/S
RAS Precharge Time (Blk2)	: 6 CLK2s	Posted Write Wait States	: 0 W/S
RAS Precharge Time (Blk3)	: 6 CLK2s	Posted Write Enable	: Enabled
Page Hit Wait State (Blk0)	: Enabled	Parity Check	: Enabled
Page Hit Wait State (Blk1)	: Enabled	Non-Cacheable Block-0 Base	: 0 KB
Page Hit Wait State (Blk2)	: Enabled	Non-Cacheable Block-0 Size	: Disabled
Page Hit Wait State (Blk3)	: Enabled	Non-Cacheable Block-1 Base	: 0 KB
CAS Pulse Width (Blk0)	: 6 CLK2s	Non-Cacheable Block-1 Size	: Disabled
CAS Pulse Width (Blk1)	: 6 CLK2s	Non-Cacheable Block-2 Base	: 0 KB
CAS Pulse Width (Blk2)	: 6 CLK2s	Non-Cacheable Block-2 Size	: Disabled
CAS Pulse Width (Blk3)	: 6 CLK2s	Non-Cacheable Block-3 Base	: 0 KB
RAS Compare Test Mode 0	: Disabled	Non-Cacheable Block-3 Size	: Disabled

ESC: Exit | | — —:Sel, (Ctrl)Pu/Pd: Modify, F1: Help, F2/F3: Color  
F5: Old Vales, F6: BIOS Setup Defaults, F7: Power-on Defaults

## 4.4 Change Password

The BIOS SETUP program has a new optional password feature. Depending on the particular hardware manufacturer or system integrator, the system may be configured so that the user is required to enter a password every time the system boots, or whenever an attempt is made to enter the SETUP programs. The password function may also be disabled, which means that the prompt will not appear under any circumstances.

This section of the manual deals with changing the user password. The password check function is enabled or disabled in Advanced CMOS Setup (refer to Section 3 for a more detailed view). The password check function is enabled by choosing either "Always" or "Setup."

The password, which will be stored in the CMOS, cannot exceed 6 characters in length. A default password, to be used if the CMOS is corrupted, is stored in the ROM. The default password is <AMI>. Check your system documentation in the event the default password has been changed by the manufacturer.

To change the user password, select the Change Password option from the main Setup screen, by using the arrow keys to move the cursor to this selection and pressing <ENTER>. The screen in Figure 5.1 will appear.

Figure 5.1 Password Opening Screen

BIOS SETUP PROGRAM - ADVANCED CMOS SETUP (C) Copyright 1990. American Megatrends Inc. All Rights Reserved	
<table border="1"><tr><td>Enter CURRENT Password:</td></tr></table>	Enter CURRENT Password:
Enter CURRENT Password:	
Use Maximum 6 ASCII Characters, ESC: Exit	

The first time you select this option, enter the default password <AMI>, or the default password specified in your system documentation, then press <ENTER> to complete your selection.

The screen will not display the characters entered. After the current password has been correctly entered, the screen in Figure 5.2 will appear, prompting you for the new password.

Figure 5.2 New Password Screen

BIOS SETUP PROGRAM - ADVANCED CMOS SETUP (C) Copyright 1990. American Megatrends Inc. All Rights Reserved	
Enter NEW Password:	
Use Maximum 6 ASCII Characters, ESC: Exit	

After the new password is entered, the prompt in Figure 5.3 will appear. Rekey the new password and press <ENTER>.

Figure 5.3 Password Confirmation Screen

BIOS SETUP PROGRAM - ADVANCED CMOS SETUP (C) Copyright 1990. American Megatrends Inc. All Rights Reserved
<input type="text"/>
Re-Enter NEW Password:
Use Maximum 6 ASCII Characters, ESC: Exit

If the password confirmation is miskeyed, the error screen in Figure 5.4 will appear. If the new password confirmation is entered without error, the screen in Figure 5.5 will appear. Press <ESC> to return to the Main Setup menu.

# AMI BIOS SETUP

---

Figure 5.4 Password Error Screen

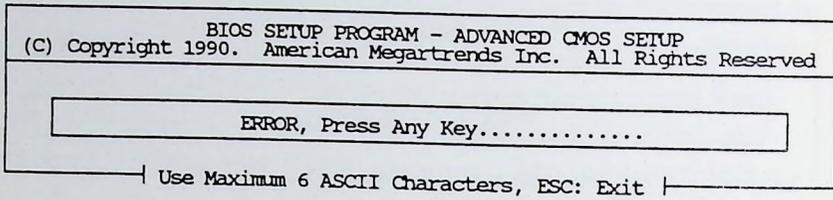
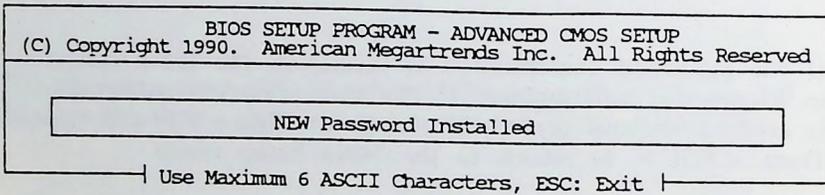


Figure 5.5 Password Installation Confirmation Screen



Once Setup is completed and the changed values have been stored in the CMOS, when the system next boots, the user will be prompted for the password if the password function is present and has been enabled.

When and if the prompt appears is dependent upon the options chosen in Advanced CMOS Setup:

If the "Always" option was chosen in Advanced CMOS Setup, the prompt will appear each time the system is powered on.

If the "Setup" option was chosen in Advanced CMOS Setup, the prompt will not appear when the system is powered on, but will appear each time an attempt is made to enter the Setup program.

If the "Disabled" option was chosen in Advanced CMOS Setup, the password prompt will never appear.

When the password prompt appears, the new password, which is now stored in the CMOS, should be entered and the <Enter> key pressed. If the CMOS is corrupted, e.g., the batteries fall out or are loosened, the default ROM password mentioned above should be used instead.

**NOTE:** When the password is changed, however, it is important that a record of the change be kept in a safe place. In the event the password check has been enabled in Setup and the user forgets or loses the new password, the default password stored in the ROM cannot be used unless the CMOS is disabled. A relatively safe way to do this would be to disconnect the CMOS batteries.

## 4.5 Hard Disk Utility

### **!! WARNING !!**

Performing the Hard Disk Format, Auto Interleave, and/or Media Analysis will destroy any data on the hard disk being tested. Back up the hard disk(s) before actually performing any of these routines.

**NOTE:** These routines are not valid for a SCSI Disk Drive.

The **Hard Disk Format** option performs a "low level" format of the hard drive(s). The user should check with the system or hard drive manufacturer to determine if this option should be taken.

The **Auto Interleave** option determines the optimum interleave factor prior to the format of the hard drive(s).

The **Media Analysis** option performs an analysis of each track of the hard drive to determine whether it is usable. If it is not usable, the track is marked as "bad" so that data cannot be stored there in the future.

A more detailed explanation of the above options is found in the individual sections on the options. See Appendix D for a list of error messages which may occur during these procedures.

If you are installing a brand new hard disk (drive), the manufacturer of the hard drive usually provides a list of "bad tracks" with the hard drive. Your system documentation might also include the optimum interleave factor.

In this case, assuming that you have a list of bad tracks and know the interleave factor, it will not be necessary to take the auto interleave and media analysis options. Simply follow the instructions in the Hard Disk Format section below. If you have a bad track list but have not been provided with the optimum interleave factor, follow the instructions in the Auto Interleave section.

If you are installing a used hard disk or reformatting an existing hard disk, perform the Media Analysis and then follow the instructions in the Auto Interleave section.

Once the Hard Disk Diagnostics option is taken by pressing <Enter> at the Main Setup Menu, the screen in Figure 6.1 will appear.

Figure 6.1 Hard Disk Utility Setup Screen

BIOS SETUP PROGRAM - STANDARD CMOS SETUP (C) Copyright 1990. American Megatrends Inc. All Rights Reserved						
Hard Disk C: Type	: 17	Cylin	Head	WPcom	LZone	Sect Size(MB)
Hard Disk D: Type	: Not Installed	977	5	300	977	17 41
Hard Disk Type can be changed from the STANDARD SETUP option in Main Menu						
Hard Disk Format Auto Interleave Media Analysis						
ESC: Exit			↑ ↓ → ← : Select		F2/F3: Color	

Use the Arrow Keys to select one of the three options and press <ENTER>.

## Hard Disk Format Utility

### **!! WARNING !!**

Performing the Hard Disk Format, Auto Interleave, and/or Media Analysis will destroy any data on the hard disk being tested. Back up the hard disk(s) before actually performing any of these routines.

**NOTE:** This routine is not valid for a SCSI Disk Drive.

Use the Hard Disk Format option to integrate a new hard disk to the system, or to reformat a used hard disk which has developed some bad patches as a result of aging or poor handling. To find these bad patches on a used drive, you may select the Media Analysis option.

When you press <ENTER> at the Hard Disk Format option, the screen in Figure 6.2 appears.

Figure 6.2 Hard Disk Format Screen

BIOS SETUP PROGRAM - STANDARD CMOS SETUP						
(C) Copyright 1990. American Megatrends Inc. All Rights Reserved						
Hard Disk C: Type	:	47=User Type	Cylin	Head	WPcom	LZone
Hard Disk D: Type	:	Not Installed	1314	7	1314	1314
			Sect	Size(MB)		
			17	76		

Hard Disk Format	
Disk Drive (C/D)	? C
Disk Drive Type	? 47
Interleave (1-16)	? 3
Mark Bad Tracks (Y/N)	?
Proceed (Y/N)	?

ESC: Exit   ↑   ↓   →   ← : Select   F2/F3: Color

The box on the left of the screen contains a series of questions (prompts) which must be answered before performing the Hard Disk Format. The first two questions may already have been answered for you if the value was previously entered for one disk only at the Standard CMOS Setup screen.

The value for Disk Drive is C for a C: Drive or D for a D: Drive. If two disk drives have been previously entered at the Standard CMOS Setup Screen, then The ID (C/D) will appear to the right of the question mark following the Disk Drive field. Choose which drive you wish to format by selecting the appropriate letter and pressing <ENTER>. If only one drive was selected at the Standard CMOS Setup screen, the cursor will automatically be placed at the interleave prompt.

# AMI BIOS SETUP

The Disk Drive Type is read from the CMOS. The interleave factor can be selected manually, or can be determined with the Auto interleave feature of the SETUP program.

The manufacturer of the hard drive usually provides a list of "bad tracks" with the hard drive. These tracks should be entered with this option, and they will then be marked as "bad" in order to prevent data from being stored there in the future.

The screen in Figure 6.3 is displayed when the prompt to Mark Bad Tracks is changed to <Y> and the <ENTER> key is pressed and an option to add, delete, revise, or clear is selected from the Bad Track Edit Menu.

Figure 6.3 Hard Disk Utility Options

BIOS SETUP PROGRAM - STANDARD CMOS SETUP			
(C) Copyright 1990. American Megatrends Inc. All Rights Reserved			
Hard Disk C: Type	: 47	Cylin Head	WPcom LZone Sect Size(MB)
Hard Disk D: Type	: Not Installed	1314 7	1314 1314 17 76
<b>Auto Interleave</b> Disk Drive (C/D) ? C Disk Drive Type ? 17 Mark Bad Track (Y/N) ? N Proceed (Y/N) ?		<b>Bad Track Edit Menu</b> Add an Entry Revise an Entry Delete an Entry Clear Bad Trk List	
Enter Cylinder # : 0 Enter Head # :		<b>Bad Track # 0</b> No. Cyln. Head	
ESC: Exit    ↑ ↓ → ← : Select    F2/F3: Color			

When the Proceed prompt is changed to <Y> and the <ENTER> key pressed, the warning screen in Figure 6.4 will be displayed.

The default for the Continue prompt is <N> to prevent accidental formatting of the hard drive and subsequent loss of data. Once this prompt is changed to <Y> and the <ENTER> key pressed, any data residing on the hard drive will be irrevocably lost.

Figure 6.4 Hard Disk Format Warning Screen

BIOS SETUP PROGRAM - STANDARD CMOS SETUP (C) Copyright 1990. American Megatrends Inc. All Rights Reserved			
Hard Disk C: Type	: 47	Cylin Head	WPCom LZone Sect Size(MB)
Hard Disk D: Type	: Not Installed	1314 7	1314 1314 17 76
Auto Interleave		WARNING INFORMATION	
Disk Drive (C/D) ? C Disk Drive Type ? 17 Interleave (1-16) ? 3 Mark Bad Track (Y/N) ? Y Proceed (Y/N) ? Y		All Data on Specified Harddisk will be LOST Want to Continue (Y/N)?N	
ESC: Exit ↑ ↓ → ← : Select F2/F3: Color			

## Media Analysis Utility

### **!! WARNING !!**

Performing the Hard Disk Format, Auto Interleave, and/or Media Analysis will destroy any data on the hard disk being tested. Back up the hard disk(s) before actually performing any of these routines.

**NOTE:** These routines are not valid for a SCSI Disk Drive.

The Media Analysis utility performs a series of tests to locate bad or damaged patches on the hard disk as a result of aging or poor handling. This utility locates all bad tracks on the hard disk and lists them in the Bad Track List Box. Since this test writes to all cylinders and heads on the hard disk to verify any bad tracks, the test may require several minutes to complete. For best results, run this test in its entirety.

To run the Media Analysis utility, use your arrow keys to select the option from the main Hard Disk Utility Menu and press <ENTER>. The following screen (Figure 6.5) will appear.

# AMI BIOS SETUP

Figure 6.5 Media Analysis Screen

BIOS SETUP PROGRAM - STANDARD CMOS SETUP	
(C) Copyright 1990. American Megatrends Inc. All Rights Reserved	
Hard Disk C: Type	: 47=User Type      Cylin Head WPCam LZone Sect Size(MB)
Hard Disk D: Type	: Not Installed      1314 7 1314 1314 17 76
Hard Disk Format	
Disk Drive (C/D)	? C
Disk Drive Type	? 47
Proceed (Y/N)	? N

ESC: Exit    ↑ ↓ → ← : Select      F2/F3: Color

The cursor will appear at the Proceed prompt. When you press <ENTER>, the warning screen in Figure 6.6 will appear.

# AMI BIOS SETUP

Figure 6.6 Media Analysis Warning Screen

BIOS SETUP PROGRAM - STANDARD CMOS SETUP						
(C) Copyright 1990. American Megatrends Inc. All Rights Reserved						
Hard Disk C: Type	: 47	Cylin	Head	WPcom	LZone	Sect Size(MB)
Hard Disk D: Type	: Not Installed	1314	7	1314	1314	17 76

Auto Interleave	
Disk Drive (C/D)	? C
Disk Drive Type	? 47
Interleave (1-16)	? 3
Mark Bad Track (Y/N)?	Y
Proceed (Y/N)	? Y

WARNING INFORMATION
All Data on Specified Harddisk will be LOST
Want to Continue (Y/N)?N

ESC: Exit ↑ ↓ → ← : Select F2/F3: Color

If you do not wish to proceed at this point, press the <Enter> key and you will be returned to the main Hard Disk Utility screen. If you wish to proceed with the analysis, change the prompt to <Y> and press <ENTER>.

## Auto Interleave Utility

### **!! WARNING !!**

Performing the Hard Disk Format, Auto Interleave, and/or Media Analysis will destroy any data on the hard disk being tested. Back up the hard disk(s) before actually performing any of these routines.

**NOTE:** These routines are not valid for a SCSI Disk Drive.

The Auto interleave utility calculates the optimum interleave value through trial and error by measuring the transfer rate for four different interleave values. To determine the best interleave factor, the system will format a portion of the hard disk for each transfer rate calculated. The cylinders, heads and sectors formatted for each value will be displayed in the activity box on the screen.

To begin the Auto interleave process, use your arrow keys to select this function on the main Hard Disk Utility Screen (Figure 6.1). Press <ENTER> to select this option. The screen in Figure 6.7 will appear.

Figure 6.7 Interleave Utility Options

BIOS SETUP PROGRAM - STANDARD CMOS SETUP					
(C) Copyright 1990. American Megatrends Inc. All Rights Reserved					
Hard Disk C: Type	: 47	Cylin	Head	WPcom	LZone
Hard Disk D: Type	: Not Installed	1314	7	1314	1314
				17	76
					Size(MB)

<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th colspan="2" style="text-align: center;">Auto Interleave</th> </tr> <tr> <td>Disk Drive (C/D)</td> <td>? C</td> </tr> <tr> <td>Disk Drive Type</td> <td>? 47</td> </tr> <tr> <td>Mark Bad Track (Y/N)</td> <td>? N</td> </tr> <tr> <td>Proceed (Y/N)</td> <td>?</td> </tr> </table>	Auto Interleave		Disk Drive (C/D)	? C	Disk Drive Type	? 47	Mark Bad Track (Y/N)	? N	Proceed (Y/N)	?	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="text-align: center;">Bad Track # 0</td> </tr> <tr> <td style="text-align: center;">No. Cyl. Head</td> </tr> </table>	Bad Track # 0	No. Cyl. Head
Auto Interleave													
Disk Drive (C/D)	? C												
Disk Drive Type	? 47												
Mark Bad Track (Y/N)	? N												
Proceed (Y/N)	?												
Bad Track # 0													
No. Cyl. Head													

ESC: Exit    ↑ ↓ → ← : Select                      F2/F3: Color

The cursor will be placed at the Mark Bad Tracks prompt. The default for this prompt is <N>. To mark additional bad tracks, change the prompt to <Y> and press <ENTER>. The screen in Figure 6.8 will appear.

# AMI BIOS SETUP

Figure 6.8 Interleave Bad Track Option Screen

BIOS SETUP PROGRAM - STANDARD CMOS SETUP (C) Copyright 1990. American Megatrends Inc. All Rights Reserved														
Hard Disk C: Type	: 47	Cylin Head WPCoom LZone Sect Size(MB)												
Hard Disk D: Type	: Not Installed	1314 7 1314 1314 17 76												
<table border="1"><tr><td>Auto Interleave</td></tr><tr><td>Disk Drive (C/D) ? C</td></tr><tr><td>Disk Drive Type ? 47</td></tr><tr><td>Mark Bad Track (Y/N) ? Y</td></tr><tr><td>Proceed (Y/N) ?</td></tr></table>	Auto Interleave	Disk Drive (C/D) ? C	Disk Drive Type ? 47	Mark Bad Track (Y/N) ? Y	Proceed (Y/N) ?	<table border="1"><tr><td>Bad Track Edit Menu</td></tr><tr><td>Add an Entry</td></tr><tr><td>Revise an Entry</td></tr><tr><td>Delete an Entry</td></tr><tr><td>Clear Bad Trk List</td></tr></table>	Bad Track Edit Menu	Add an Entry	Revise an Entry	Delete an Entry	Clear Bad Trk List	<table border="1"><tr><td>Bad Track # 0</td></tr><tr><td>No. Cyl. Head</td></tr></table>	Bad Track # 0	No. Cyl. Head
Auto Interleave														
Disk Drive (C/D) ? C														
Disk Drive Type ? 47														
Mark Bad Track (Y/N) ? Y														
Proceed (Y/N) ?														
Bad Track Edit Menu														
Add an Entry														
Revise an Entry														
Delete an Entry														
Clear Bad Trk List														
Bad Track # 0														
No. Cyl. Head														
<table border="1"><tr><td>Enter Cylinder # : 0</td></tr><tr><td>Enter Head # :</td></tr></table>		Enter Cylinder # : 0	Enter Head # :											
Enter Cylinder # : 0														
Enter Head # :														
ESC: Exit ↑ ↓ → ← : Select F2/F3: Color														

After you have made the desired selections at the Bad Tracks Edit Menu, press <ESC>. The cursor will be moved to the Proceed prompt.

To Proceed with the Auto interleave process, change the prompt to <Y> and press <ENTER>. The following warning screen in Figure 6.9 will appear.

# AMI BIOS SETUP

Figure 6.9 Auto Interleave Warning Screen

BIOS SETUP PROGRAM - STANDARD CMOS SETUP						
(C) Copyright 1990. American Megatrends Inc. All Rights Reserved						
Hard Disk C: Type	: 47	Cylin Head	WPcom	LZone	Sect	Size(MB)
Hard Disk D: Type	: Not Installed	1314	7	1314	1314	17 76

Auto Interleave	
Disk Drive (C/D)	? C
Disk Drive Type	? 47
Interleave (1-16)	? 3
Mark Bad Track (Y/N)?	Y
Proceed (Y/N)	? Y

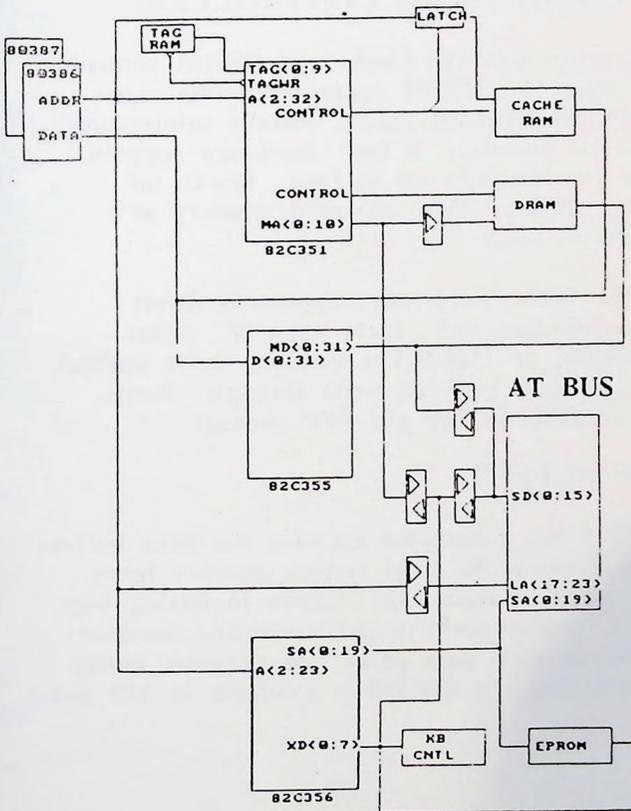
WARNING INFORMATION	
All Data on Specified Harddisk will be LOST	
Want to Continue (Y/N)?N	

ESC: Exit ↑ ↓ → ← : Select F2/F3: Color

If you do not wish to proceed, press <ENTER> and you will return to the main Hard Disk Utility screen. To proceed, change the warning prompt to <Y> and press <ENTER>.

# 5. System Board Technical Reference

## 5.1 System Board Block Diagram



## 5.2 Description

This Main Board allows it to be used in any iAPX 386 based system designs such as CAD/CAE workstations, office systems, industrial and financial transaction systems. The Main Board consists of one 82C351 CPU/CACHE/DRAM controller, one 82C355 Data Buffer and 82C356 peripherals controller.

### 82C351 CPU/CACHE/DRAM CONTROLLER

By integrating both the Cache and DRAM control function in one chip, the 82C351 supports simultaneous activation of cache and DRAM access, thereby minimizing the cache miss cycle penalty. It has hardware support to allow the user to designate up to four blocks (of variable size from 4KB to 4MB) of main memory as non-cacheable address space.

The 82C351 Cache Controller supports a direct mapped cache architecture and cache sizes of either 32KB, 64KB, 128KB, or 256KB. The memory write updates are implemented using a buffered write through scheme. The 82C351 is available in 160 pin PFP package.

### 82C355 DATA BUFFER

The 82C355 Bus Controller contains the data buffers used to interface between the local system memory buses and a path for AT data buses. In addition to having high current bus drive, it also perform the conversion necessary between the different sized data paths and provides parity generation and checking. The 82C355 is available in 120 pin PFP package.

### 82C356 PERIPHERAL CONTROLLER

The 82C356 Peripheral Controller contains the address buffers used to interface between most address buses. It also contains an equivalent 82C206 Integrated Peripheral Controller which incorporates two 8237 DMA controllers, two 8259 Interrupt controllers, one 8254 Timer/Counter, one MC146818 Real Time Clock, a 74LS612 memory mapper, and several other TTL/SSI interface logic chips. The 82C356 is available in 144 pin PFP package.

## 5.3 System Hardware Configuration

### 5.3-1 System Memory Map

Address	Name	Function
000000 to 07FFFF	512Kb system board	System board memory
080000 to 09FFFF	128Kb	I/O channel memory-IBM Personal Computer AT 128KB Memory Expansion Option
0A0000 to 0BFFFF	128Kb video RAM	Reserved for graphics display buffer
0C0000 to 0DFFFF	128Kb I/O expansion ROM	Reserved for ROM on I/O adapters
0E0000 to 0EFFFF	64Kb Reserved on system board	Duplicated code assignment at address FE0000
0F0000 to 0FFFFF	64Kb ROM on the system board	Duplicated code assignment at address FF0000
100000 to FDFFFF	Maximum memory 15Mb	I/O channel memory-IBM Personal Computer AT 512KB Memory Expansion Option
FE0000 to FEFFFF	64Kb Reserved on the system board	Duplicated code assignment at address 0E0000
FF0000 to FFFFFF	64Kb ROM on the system board	Duplicated code assignment at address 0F0000

## Hardware Configuration

---

### 5.3-2 System I/O Address Map

Hex Range	Device
000-01F	DMA Controller 1, 8237A-5
020-03F	Interrupt controller 1, 8259A, Master
040-05F	Timer, 8254.2
060-06F	8042 (Keyboard)
070-07F	Real-time clock,NMI (non-maskable interrupt) mask
080-09F	DMA page register, 74LS612
0A0-0BF	Interrupt controller 2, 8259A
0C0-0DF	DMA controller 2, 8237A-5
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel printer port 2
2F8-2FF	Serial port 2
300-31F	Prototype card

## Hardware Configuration

---

360-36F	Reserved
378-37F	Parallel printer port 1
380-38F	SDLC, bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome Display and Printer Adapter
3C0-3CF	Reserved
3D0-3DF	Color/Graphics Monitor Adapter
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1

---

# Hardware Configuration

---

## 5.3-3 DMA Channels

CTLR 1	CTLR 2
Ch 0 - Spare	Ch 4 - Cascade for Ctlr 1
Ch 1 - SDLC	Ch 5 - Spare
Ch 2 - Diskette (IBM Personal Computer)	Ch 6 - Spare
Ch 3 - Spare	Ch 7 - Spare

---

## 5.3-4 Interrupt

Interrupt Controllers  
CTLR 1      CTLR 2

IRQ 0	Timer Output 0
IRQ 1	Keyboard (Output Buffer Full)
IRQ 2	Interrupt from CTLR 2
	Realtime Clock Interrupt
	IRQ 8 Software Redirected to
	IRQ 9 INT 0 AH (IRQ 2)
	IRQ 10 Reserved
	IRQ 11 Reserved
	IRQ 12 Reserved
	IRQ 13 Coprocessor
	IRQ 14 Fixed Disk Controller
	IRQ 15 Reserved
IRQ 3	Serial Port 2
IRQ 4	Serial Port 1
IRQ 5	Parallel Port 2
IRQ 6	Diskette Controller
IRQ 7	Parallel Port 1

---

## 5.3-5 CMOS RAM Address Map

Addresses	Description
00-0D	*Real-time clock information
0E	*Diagnostic status byte
0F	*Shutdown status byte
10	Diskette drive type byte-drives A and B
11	Reserved
12	Fixed disk type byte-drives C and D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	*Low expansion memory byte
31	*High expansion memory byte
32	*Date century byte
33	*Information flags (set during power on)
34-3F	Reserved

---

## Hardware Configuration

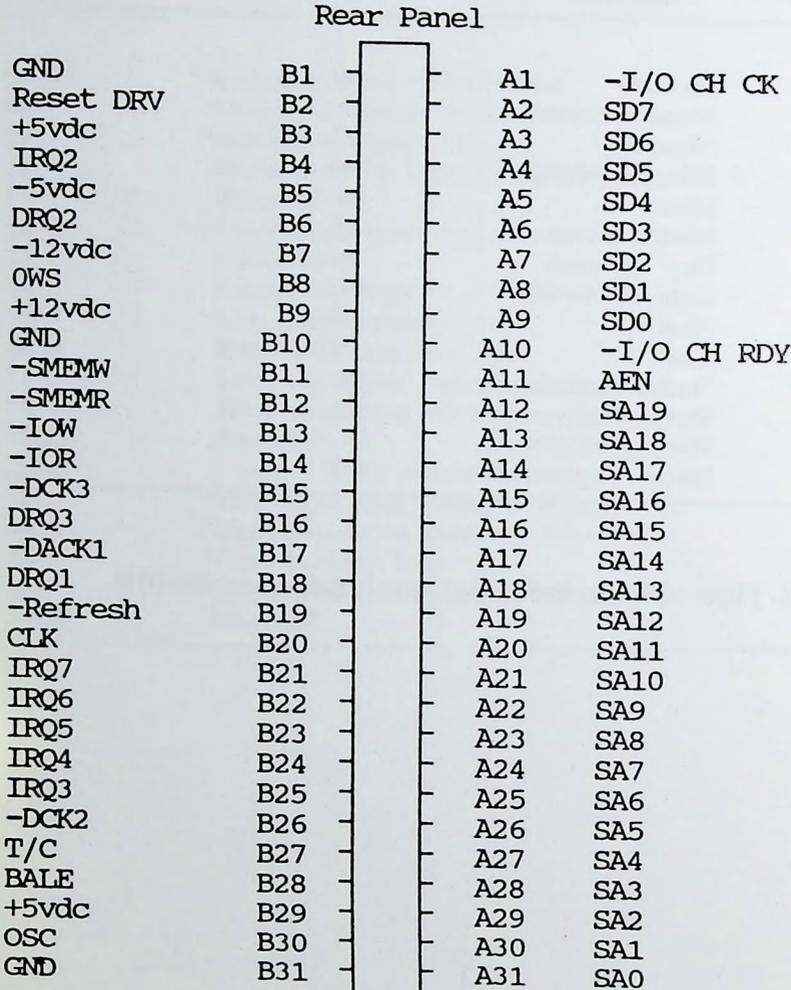
---

### 5.3-6 RTC Information

Byte	Function	Address
0	Seconds	00
1	Second alarm	01
2	Minutes	02
3	Minutes alarm	03
4	Hours	04
5	Hours alarm	05
6	Day of week	06
7	Date of month	07
8	Month	08
9	Year	09
10	Status Register A	0A
11	Status Register B	0B
12	Status Register C	0C
13	Status Register D	0D

Real-Time Clock Information (addresses 00-0D)

## 5.3-7 I/O Channel



I/O Channel Pin Numbering (J1-J8)

# Hardware Configuration

---

-MEM CS16	D1	C1	SBHE
I/O CS16	D2	C2	LA23
IRQ16	D3	C3	LA22
IRQ11	D4	C4	LA21
IRQ12	D5	C5	LA20
IRQ15	D6	C6	LA19
IRQ14	D7	C7	LA18
-DACK0	D8	C8	LA17
DRQ0	D9	C9	-MEMR
-DACK5	D10	A10	-MEMW
DRQ5	D11	A11	SD08
-DACK6	D12	A12	SD09
DRQ6	D13	A13	SD10
-DACK7	D14	A14	SD11
DRQ7	D15	A15	SD12
+5vdc	D16	A16	SD13
-MASTER	D17	A17	SD14
GND	D18	A18	SD15

I/O Channel Pin Numbering (J10-J14 and J16)

## Hardware Configuration

---

### I/O Channel (A-Side,U102 through U108)

I/O Pin	Signal Name	I/O
A 1	-I/O CH CK	I
A 2	SD7	I/O
A 3	SD6	I/O
A 4	SD5	I/O
A 5	SD4	I/O
A 6	SD3	I/O
A 7	SD2	I/O
A 8	SD1	I/O
A 9	SD0	I/O
A 10	-I/O CH CK	I
A 11	AEN	O
A 12	SA19	I/O
A 13	SA18	I/O
A 14	SA17	I/O
A 15	SA16	I/O
A 16	SA15	I/O
A 17	SA14	I/O
A 18	SA13	I/O
A 19	SA12	I/O
A 20	SA11	I/O
A 21	SA10	I/O
A 22	SA9	I/O
A 23	SA8	I/O
A 24	SA7	I/O
A 25	SA6	I/O
A 26	SA5	I/O
A 27	SA4	I/O
A 28	SA3	I/O
A 29	SA2	I/O
A 30	SA1	I/O
A 31	SA0	I/O

---

## Hardware Configuration

---

### I/O Channel (B-Side J1, through J8)

I/O Pin	Signal Name	I/O
B 1	GND	Ground
B 2	RESET DRV	O
B 3	+5 Vdc	Power
B 4	IRQ 9	I
B 5	-5 Vdc	Power
B 6	DRQ2	I
B 7	-12 Vdc	Power
B 8	OVS	I
B 9	+12 Vdc	Power
B 10	GND	Ground
B 11	-SMEMW	O
B 12	-SMEMR	O
B 13	-IOW	I/O
B 14	-IOR	I/O
B 15	-DACK3	O
B 16	DRQ3	I
B 17	-DACK1	O
B 18	DRQ1	I
B 19	-Refresh	I/O
B 20	CLK	O
B 21	IRQ7	I
B 22	IRQ6	I
B 23	IRQ5	I
B 24	IRQ4	I
B 25	IRQ3	I
B 26	-DACK2	O
B 27	T/C	O
B 28	BALE	O
B 29	+5 Vdc	Power
B 30	OSC	O
B 31	GND	Ground

---

## Hardware Configuration

---

### I/O Channel (C-Side J10 through J14 and J16)

I/O Pin	Signal Name	I/O
C1	SBHE	I/O
C2	LA23	I/O
C3	LA22	I/O
C4	LA21	I/O
C5	LA20	I/O
C6	LA19	I/O
C7	LA18	I/O
C8	LA17	I/O
C9	-MEMR	I/O
C10	-MEMW	I/O
C11	SD08	I/O
C12	SD09	I/O
C13	SD10	I/O
C14	SD11	I/O
C15	SD12	I/O
C16	SD13	I/O
C17	SD14	I/O
C18	SD15	I/O

---

## Hardware Configuration

---

### I/O Channel (D-Side, J10 through J14 and J16)

I/O Pin	Signal Name	I/O
D1	-MEM CS16	I
D2	-I/O CS16	I
D3	IRQ10	I
D4	IRQ11	I
D5	IRQ12	I
D6	IRQ15	I
D7	IRQ14	I
D8	-DACK0	O
D9	DRQ0	I
D10	-DACK5	O
D11	DRQ5	I
D12	-DACK6	O
D13	DRQ6	I
D14	-DACK7	O
D15	DRQ7	I
D16	+5Vdc	Power
D17	-MASTER	I
D18	GND	Ground

---

## 5.4 System Function Control- Index Registers

The 82C351 has index registers for various system control functions. These registers are accessed through ports 22H and 23H. An indexing scheme is used to reduce the number I/O addresses required to access all registers needed to configure and control the CHIP set. Each access (either read or write) to an internal register is done by first writing its index into port 22H. Then read port 23H (if reading of the register is required) or write to port 23H (if writing of the selected index register is required.) Every access to port 23 should be preceded by writing index value to port 22H even if the same data port is being accessed again.

Port 92H can be accessed directly without going through indexing.

### Port 92H Fast GATE A20 and RESET Register

This port is active only if Index 2B bit 6 is a 1  
NOTE: This port is used by OS/2 and can be disabled by writing a 0 to index register 2B bit 6.

<i>Address</i>	<i>Bits</i>	<i>Description</i>
92H	7-2	<i>Reserved</i>
	1	<i>Fast GATEA20</i> <i>0:Force CPU A20 low</i> <i>(1):Enable CPU A20</i> <i>Fast CPU enable</i> <i>(0):A 0 to 1 transition</i> <i>causes a CPU reset.</i>

## Index Registers

---

Index Registers (accesses are through IO ports 22 and 23).

---

### Name: Revision Registers (READ ONLY)

Index	Bits	Values and Functions
04H	7-4	: Undefined
	3-0	: Revision Level

---

### AT Bus Command Delays (READ/WRITE)

Index	Bits	Values and Functions
05H	7:6	(00) : Reserved
	5:4	AT bus 16 bit memory command delay (00):0 BCLK delay (01):1 BCLK delay 10 :2 BCLK delay 11 :3 BCLK delay
	3:2	AT bus 8 bit memory command delay 00 :0 BCLK delay (01):1 BCLK delay 10 :2 BCLK delay 11 :3 BCLK delay
	1:0	AT bus I/O command delay 00 :0 BCLK delay (01):1 BCLK delay 10 :2 BCLK delay 11 :3 BCLK delay

## Name: AT bus Wait States (READ/WRITE)

Index Bits Values and Functions

- 06H 7:6 (00) : Reserved
- 5:4 16 bit AT bus wait states
    - (00):3 BUSCLK wait states
    - 01:2 BUSCLK wait states
    - 10:1 BUSCLK wait states
    - 11:0 BUSCLK wait states
  - 3:2 8 bit AT bus wait states
    - (00):5 BUSCLK wait states
    - 01:4 BUSCLK wait states
    - 10:3 BUSCLK wait states
    - 11:2 BUSCLK wait states
  - 1 AT bus address hold time. (Provides extra address time for adapter cards that require it for reliable operation)
    - (0):Disable extra address hold time on AT bus
    - 1:Enable extra address hold time on AT bus (delays next cycle by one  $T_r$  state and holds current address valid.
  - 0 Reserved

## Name: AT Clock Source Select (READ/WRITE)

Index Bits Values Functions

- 07H 7:3 (0000) : Reserved
- 2:0 Bus Clock Source Select (BCLK).  $BUSCLK = BCLK/2$ 
    - (000):CLK2IN/5
    - 001:CLK2IN/4
    - 010:CLK2IN/3
    - 011:CLK2IN/2
    - 100:ATCLK

## Index Registers

---

### Name: Initial Memory, CPU Speed (READ/WRITE)

Index	Bits	Values and Functions
08H	7:4	(00000) :Reserved
	3	486 MODE (0): Default 1 = EADS on VRAMSEL output KEN on HLDA2 output
	2	-AF32 assertion control (0): Does not generate-AF32 for addresses above 16MB.Should only be used if external logic can recognize address above 16MB. 1 : Generates-AF32 for address above 16 MB. Unless real physical memory is installed for that address range, no memory cycles starts and no -READY is given to the CPU.
	1	Initial memory (0): Only 512 K memory enabled.Registers 0C to 0F are ignored.Register 2A can also affect the bottom 512K . 1: Registers 0C-0F can enable the memory above 512K .
	0	CPUCLK (CPU Clock) select (0): Selects CLK2IN 1: Selects AT control logic clock (BCLK)

Bits 7 to 4 write protect RAM located in the BIOS area in 64KB blocks.Bits 3 to 0 enable the substitution of the BIOS ROM located below 1MB with RAM at the same location in 64KB blocks. This should be done after BIOS code is copied from the ROM and the RAM locations have been protected using bits 7 to 4. Make sure registers 0C-0F are enabled if RAM accesses are required.

Index	Bits	Values and Functions
09H	7	64KB RAM at 768K C0000-CFFFFH(VIDEO) (0): 64KB of RAM at 768K is read/write 1: 64KB of RAM at 768K is read only
	6	64KB RAM type at 832K D0000-DFFFFH (0): 64KB of RAM at 832K is read/writ 1: 64KB of RAM at 832K is read only
	5	64KB RAM at 896K E0000-EFFFFH (0): 64KB of RAM at 896K is read/write 1: 64KB of RAM at 896K is read only
	4	64KB RAM type at 960K F0000-EFFFFH(SYSTEM) (0): 64KB of RAM at 960K is read/writ 1: 64KB of RAM at 960K is read only
	3	64KB ROM at 768K C0000-CFFFFH (VIDEO) (0): 64KB of ROM at 768K is disabled 1: 64KB of ROM at 768K is enabled
	2	64KB ROM at 832K D0000-DFFFFH (0): 64KB of ROM at 832K is disabled 1: 64KB of ROM at 832K is enabled
	1	64KB ROM at 896K E0000-EFFFFH (0): 64KB of ROM at 896K is disabled 1: 64KB of ROM at 896K is enabled
	0	64KB ROM type at 960K F0000-FFFFFH (SYSTEM) (0): 64KB of ROM at 960K is disabled 1: 64KB of ROM at 960K is enabled

Index registers 0CH through 0FH control whether memory is located or controlled by the system board or the AT bus. Each bit controls a 16KB block. Bit 0 enables the lowest and bit 7 the highest 16K block in each 128KB memory area. For example, bit 0 of index register 0CH controls the 16K block from 08000H to 083FFFH (512KB to 528KB). This permits selective 16K blocks of memory to be disabled, allowing ROMs, memory expansion schemes (EMS, EEMS or XMA) or memory mapped I/O devices to reside within the lower 1MB address space.

## Index Registers

---

### Index Bits Values and Functions

0CH	7:0	Memory enable map - 080000-09FFFFH (Read/Write)
0DH	7:0	Memory enable map - 0A0000-0BFFFFH (Read/Write)
0EH	7:0	Memory enable map - 0C0000-0DFFFFH (Read/Write)
0FH	7:0	Memory enable map - 0E0000-0FFFFH(Read/Write)

Enable bits for eight 16K blocks of memory  
0: Address is on or controlled by the system board; 16K block enabled  
(1): Address is on the I/O channel;16K block disable

---

### Name: Bank 0/1 Type and Starting address (READ/ WRITE)

### Index Bits Values and Functions

10H	7:6	DRAM type in bank 0/1 00:Bank0/1 disabled (01):1Mx1 or 1Mx4 DRAMs 10 : 1Mx1 or 1Mx4 DRAMs 11:4Mx1 or 4Mx4 DRAMs
	5:0	(000000) : Starting address for Block 0 A26 to A21. 256K usage A <26:21 > (1MB per block, interleaved) (2MB per block, non-interleaved) 1M usage A <26:23 > (4MB per block) (8MB per block, non-interleaved) 4M usage A <26:25 > (16MB per block) (32MB per block, non-interleaved)

**Name: Bank 0/1 RAM timing (READ/WRITE)**

Index	Bits	Values and Functions
11H	7:5	(000) : Reserved - write 000 00:3 wait states 01:4 wait states (10):5 wait states 11:Reserved
	4:3	RAS precharge time, RAS <0:1> non-interleaved, RAS <0> interleave 00:3 CPUCLKIN cycles 01:4 CPUCLKIN cycles 10:5 CPUCLKIN cycles (11)6 CPUCLKIN cycles
	2:1	-RAS Refresh pulse width (for all banks) 00:4 CPUCLKIN cycles 01:5 CPUCLKIN cycles 10:6 CPUCLKIN cycles (11):7 CPUCLKIN cycles
	0	(0):Reserved - write 0

---

**Name: Bank 2/3 Type and Starting address (READ/WRITE)**

Index	Bits	Values and Functions
12H	7:6	DRAM type 1 in block 1 00:Block 1 disabled (01):256Kx1 or 256Kx4 DRAMs 10:1Mx1 or 1Mx4 DRAMs 11:4Mx1 or 4Mx4 DRAMs
	5:0	(000000) Starting address for block 1  256K usage A <26:21> (1MB per block, interleaved) (2MB per block, non-interleaved) 1M usage A <26:23> (4MB per block) (8MB per block, non-interleaved) 4M usage A <26:25> (16MB per block) (32MB per block, non-interleaved)

---

## Index Registers

---

### Name: Bank 2/3 RAM timing (READ/WRITE)

Index	Bits	Values and Functions
13H	7:5	(000) Reserved - write 000
	4:3	RAS percharge time (RAS <2:3 > non-interleaved) (RAS <2 > interleaved)
	00:3	CPUCLKIN cycles
	01:4	CPUCLKIN cycles
	10:5	CPUCLKIN cycles
	(11):6	CPUCLKIN cycles
	2:0	(000) : Reserved - write 0

---

### Name: Bank 4/5 Type and Starting address (READ/ WRITE)

Index	Bits	Values and Functions
14H	7:6	DRAM type block 2 00:Bank0/1 disabled (01):256Kx1 or 256Kx4 DRAMs 10:1Mx1 or 1Mx4 DRAMs 11:4Mx1 or 4Mx4 DRAMs
	5:0	(000000) : Starting address for Block 2  256K usage A <26:21 > (2MB per block, interleaved) (2MB per block, non-interleaved) 1M usage A <26:23 > (8MB per block) (8MB per block, non-interleaved) 4M usage A <26:25 > (32MB per block) (32MB per block, non-interleaved)

### Name: Bank 4/5 RAM timing (READ/WRITE)

Index Bits Values and Functions

- 15H 7:5 (000) : Reserved - Write 000
- 4:3 RAS percharge time RAS <4:5> non-interleaved  
RAS <4> interleaved  
00:3 CPUCLKIN cycles  
01:4 CPUCLKIN cycles  
10:5 CPUCLKIN cycles  
(11):6 CPUCLKIN cycles
- 2:0 (000) : Reserved - write 0
- 

### Name: Bank 6/7 Type and Starting address (READ/WRITE)

Index Bits Values and Functions

- 16H 7:6 DRAM type in Block 3  
00:Block 3 disabled  
(01):256Kx1 or 256Kx4 DRAMs  
10:1Mx1 or 1Mx4 DRAMs  
11:4Mx1 or 4Mx4 DRAMs
- 5:0 Starting address for Block 3
- 256K usage A <26:21> (1MB per bank )  
(2MB per block, non-interleaved)
- 1M usage A <26:23> (4MB per bank )  
(8MB per block, non-interleaved)
- 4M usage A <26:25> (16MB per bank )  
(32MB per block, non-interleaved)
-

## Index Registers

---

### Name: Bank 6/7 RAM timing (READ/WRITE)

Index	Bits	Values and Functions
17H	7:5	(000) : Reserved - write 000
4:3		RAS precharge time, RAS <6:7> non-interleaved, RAS <6> interleaved
00:3		CPUCLKIN cycles
01:4		CPUCLKIN cycles
10:5		CPUCLKIN cycles
(11)6		CPUCLKIN cycles
0	(0)	: Reserved - write 0
2:0	(000)	

---

### Name: Cache size (READ/WRITE)

Index	Bits	Values and Functions
18H	7:4	(0000) : Reserved
3		Block 3 (Bank 6/7) (0) : Bank 6 populated only 1 : Banks 6 and 7 populated
2		Block 2 (Bank 4/5) (0) : Bank 4 populated only (used for single bank and interleaved configurations) 1 : Banks 4 and 5 populated
1		Block 1 (Bank 2/3) (0): Bank 2 populated only(used for single bank and interleaved configurations) 1. Banks 2 and 3 populated
0		Block 0 (Bank 0/1) (0): Bank 0 populated only(used for single bank and interleaved configurations) 1: Banks 0 and Bank 1 populated

---

## Name: Cache and tag test (READ/WRITE)

Index	Bits	Values and Functions
19H	7	RAS compare test mode (0) : Disabled 1 : Enabled
	6	Double CAS mode (2 or 4 CLK2 CAS) 0 : Disabled (1) : Enabled
	5	RAS compare test mode (0) : Disabled 1 : Enabled
	4	Early LDBEN (1) : LDBEN transistions high to low during first T2 (0) : Normal
	3	Additional wait-states for all but consective write DRAM cycles (0) : 0 wait-state 1 : 1 wait-state added
	2	Early MA signal release (0) : Enable 1 : Disable
	1	Early CAS mode (0) : Disable 1 : Enable
	0	Page Interleave Mode RAS 1,3,5,7 used as CASEN <0:3 > (0) : Disable 1 : Enable

# Index Registers

---

Index	Bits	Values and Functions
1AH	7	Read extra wait-state for page hit (0) : No extra wait-state 1 : Add 1 wait-state
	6	Read page hit wait-state state selection (block 1). Note : Add one wait-state if non-pipeline mode is used. 0 : 0 wait-state (pipeline mode) (1) : 1 wait-state (pipeline mode)
	5:4	CAS low pulse width for READ RAS high Page Misses (block 1) 00 : 3 CPUCLKIN cycles 01 : 4 CPUCLKIN cycles 10 : 3 CPUCLKIN cycles (11) : 6 CPUCLKIN cycles
	3	(0) : Reserved write 0
	2	Read page hit wait-state selection (block 2). Note : Add one wait-state if non-pipeline mode is used. 0 : 0 wait-state (pipeline mode) (1) : 1 wait-state (pipeline mode)
	1:0	CAS low pulse width for READ RAS high or Page miss (block 2) 00 : 3 CPUCLKIN cycles 01 : 4 CPUCLKIN cycles 10 : 5 CPUCLKIN cycles (11) : 6 CPUCLKIN cycles

Index	Bits	Values and Functions
1BH	7	7 CLK2 CAS pulse width (0) : Normal 1 : 7 CLK CAS pulse width all banks
	6	Read page hit wait-state (block 3) selection Note : Add one wait-state if non-pipeline mode is used. 0 : 0 wait-state (pipeline mode) (1) : 1 wait-state (pipeline mode)
	5:4	CAS low pulse width for READ RAS high Page Misses (block 3) 00 : 3 CPUCLKIN cycles 01 : 4 CPUCLKIN cycles 10 : 5 CPUCLKIN cycles (11) : 6 CPUCLKIN cycles
	3	(0) : Reserved write 0
	2	Read page hit wait-state selection (block 2). Note : Add one wait-state if non-pipeline mode is used. 0 : 0 wait-state (pipeline mode) (1) : 1 wait-state (pipeline mode)
	1:0	CAS low pulse width for READ RAS high or Page miss (block 2) 00 : 3 CPUCLKIN cycles 01 : 4 CPUCLKIN cycles 10 : 5 CPUCLKIN cycles (11) : 6 CPUCLKIN cycles

# Index Registers

---

## Index Bits Values and Functions

- 1CH**
- 7** Late, late mode for all blocks for write miss and RAS High
    - 0 : Normal CAS mode
    - (1): Late CAS mode (adds 1 wait-state to write page miss write cycles)
  
  - 6** RAS to CAS delay section
    - 0 : 2 CLK2 cycles
    - (1) : 3 CLK2 cycles
  
  - 5** Alternate RAS precharge values, defined by registers 11,13,15,17 bits <4:3> for Blocks A,B,C,D
    - 0 : RAS precharge values = 3,4,5,6 CLK2s
    - (1) : RAS precharge values 4,6,6,6
  
  - 4** Force RAS high enable bit
    - (0) : Normal page mode operation
    - 1 : Force RAS high after each cycle
  
  - 3** RAS active position
    - 1 : Assert RAS at beginning of T1P/T2
    - (0) : Assert RAS in the middle of T1P/T2
  
  - 2:0** Interleave selection
    - (000) : non-interleave mode
    - 001 : 2-waypage interleave; blocks 0 and 1
    - 010 : 2-waypage interleave; blocks 2 and 3
    - 011 : 2-waypage interleave; blocks 0 and 1 as well as banks 2 and 3 but separately
    - 100 : 4-way page interleave; blocks 0,1,2 and 3
    - 101-111 : Reserved combinations

Index	Bits	Values and Functions
20H	7	Cache enable bit (0) : cache is disabled 1 : cache is enabled
	6	Force Read miss cycle. This bit is used for initializing the data and tag SRAMs. When set to 1, all accesses are to DRAM, but the tag and data SRAMs are still updated for cacheable areas as if the cache is fully operating. Any block of 256KB (or size of the cache) consecutive locations are then read, followed by setting this bit to 0. The 256KB block used to initialize the tag must not be made non-cacheable afterward. (0) : No force read miss cycle (normal operation) 1 : Forced read miss cycle enabled
	5	Freeze cache directory. A cache read miss will not cause a tag RAM update and change of data in the cache data RAM. Instead, a normal DRAM read operation will be performed. A cache write hit will update the cache data RAM.
	4	(0) : Reserved
	3	Refresh type selection 0 : Hidden refresh (1) : AT style refresh
	2:0	(000) : Reserved

## Index Registers

---

The following register controls the Ready Timeout option. If any device accessed by the CPU does not respond with -READY within 128 clock cycles, the 83C351 AT control logic will generate -READY itself.

### Index Bits Values and Functions

- 26H 7:3 Reserved (See Volume IV: 82C356 Peripheral Controller, Section 2 : 356 Configuration Registers)
- 2 -READY Timeout  
(0) : -READY Timeout disabled  
1 : -READY Timeout disabled
- 1:0 Reserved (See Volume IV: 82C356 Peripheral Controller, Section 2 : 356 Configuration Registers)
- 

### Name: Parity error status register (READ/WRITE)

#### Index Bits Values and Functions

- 28H 7 Parity check enable  
(0):Parity check enabled (PEN is low)  
1:Parity is disabled (PEN is high)
- 6:3 (0000): Reserved
- 2:0 Parity error address bits A26:A24. When a local parity error occurs the address A26-A24 is latched into bits 2:0. These bits are read only.
-

### Name: Parity error address register (READ ONLY)

When a local parity error occurs address A23-A16 are latched into this register.

Index Bits Values and Functions

- 29 7:0 Parity error address bits A <24:A16> .  
When a local parity error occurs, the address A <26:16> is latched into this register. These bits are read only.
- 

### Name: Memory Enable Map 0-07FFFFH (READ/ WRITE)

Index Bits Values and Functions

- 2AH 7 Ready Timeout Flag (R/W)  
(0): Default  
1 : RDY Timeout has occurred
- 6 CWE Pulse Width  
(0): Default  
1 : Increase PW by 3ns (TYP)
- 5 Reserved  
(0) : Default  
1 : Write (1)
- 4 Enables internal hidden refresh logic. Enable only if external work around is not present.  
(0) : Disabled : external work around present  
1 : Enable
- 3 SLODRD for 25 MHz Pipeline mode  
(0) : Default (non-pepeline mode)  
1 : Delay LBEN by 1/2 CLK2 for DRAM reads
- 2 Reserved  
(0) : Default  
1 : Write (1)
- 1 DMA Cycles  
(0) : Default  
1 : Drive A24-31 low for DMA cycles (HLDA1 active)
-

## Index Registers

---

### Name: Miscellaneous Control (READ/WRITE)

Index Bits Values and Functions

2BH 7 (0) : Reserved

6 Enable port 92H  
(0):Disable port 92H  
1:Enable port 92H

5:4 Ready generation for 387DX cycles  
(00):82C351 generates ready after 1 wait-state  
01:82C351 runs AT cycle for all NPX cycles  
10:82C351 does not generate ready at all  
11:Reserved

3 Weitek Present bit (READ ONLY)  
1:Weitek coprocessor present  
(0):Weitek coprocessor not present

2:1 (000) : Reserved

---

### Name: Middle Boot Space RAM/ROM Configuration (READ/WRITE)

Index Bits Values and Functions

2CH 7 Type of 64KB RAM at 0FC0000H  
(0):64KB of RAM at 0FC0000H is R/W  
1:64KB of RAM at 0FC0000H is read only

6 Type of 64KB RAM at 0FD0000H  
(0):64KB of RAM at 0FD0000H is R/W  
1:64KB of RAM at 0FD0000H is read only

---

— Continued —

- 5 Type of 64KB RAM at 0FE0000H  
 (O):64KB of RAM at 0FE0000H is R/W  
 1:64KB of RAM at 0FE0000H is read only
  
- 4 Type of 64KB RAM at 0FF0000H  
 (O):64KB of RAM at 0FF0000H is R/W  
 1:64KB of RAM at 0FF0000H is read only
  
- 3 Type of 64KB RAM at 0FC0000H  
 (O):64KB of RAM at 0FC0000H is disable  
 1:64KB of RAM at 0FC0000H is enable
  
- 2 Type of 64KB RAM at 0FD0000H  
 (O):64KB of RAM at 0FD0000H is disable  
 1:64KB of RAM at 0FD0000H is enable
  
- 1 Type of 64KB RAM at 0FE0000H  
 (O):64KB of RAM at 0FE0000H is disable  
 1:64KB of RAM at 0FE0000H is enable
  
- 0 Type of 64KB RAM at 0FE0000H  
 (O):64KB of RAM at 0FE0000H is disable  
 1:64KB of RAM at 0FE0000H is enable

---

## Name: DRAM timing control (READ/WRITE)

Index    Bits    Values and Functions

- 2FH    7:5 (000) : Reserved
  
- 4    Additional wait-state on consecutive cycles  
 (0):0 additional wait states  
 1: 1 additional wait-state
  
- 3    (0) Reserved write 0
  
- 2    Posted write wait-states. Determines the number of wait-states for posted CPU write cycles. If a posted write is already in progress wait-states are added until the cycle is finished.  
 0 : zero wait-state posted writes  
 (1) : one wait-state posted writes
  
- 1    Posted DRAM write enable  
 0 : Enable posted writes  
 (1) : Disable posted writes
  
- 0    (0) : Reserved

## Index Registers

---

**Non cacheable blocks:** the 82C351 provides programmable registers for defining a area of memory as non cacheable. For example the BIOS ROM area needs to be non cached. Four such areas can be declared non cacheable. The index registers 30 to 39 are used to set the starting address and the amount of memory for to be non cached. Block 0 to 3 are the four non cacheable blocks. Each block has three registers which define the starting address and the amount of memory. For example block 0 has register 30H, 31H and 38H. The register 31 contains the non cacheable size. The non cacheable size is 4K to 4MB.

**Name: Block 0 Non-Cacheable address A23 to A16  
(READ/WRITE)**

**Index    Bits    Values and Functions**

**30H    7:0    (00000000) Block 0 Non-Cacheable address A23 to A16**

---

**Name: Block 0 Non-Cacheable address A15 to A12  
and Size (READ/WRITE)**

**Index    Bits    Values and Functions**

**31H    7:4    (0000) : Block 0 Non-Cacheable address A15 to A12  
3:0    Non-Cacheable Size  
(0000):Disabled  
0001:4KB  
0010:8KB  
0011:16KB  
0100:32KB  
0101:64KB  
0110:128KB  
0111:256KB  
1000:512KB  
1001:1MB  
1010:2MB  
1011:4MB**

---

### Name: Block 1 Non-Cacheable address A23 to A16 (READ/WRITE)

Index Bits Values and Functions

32H 7:0 (00000000) : Block 1 Non-Cacheable address A23 to A16

---

### Name: Block 1 Non-Cacheable address A15 to A12 and Size (READ/WRITE)

Index Bits Values and Functions

33H 7:4 (0000) : Block 1 Non-Cacheable address A15 to A12

3:0 Non-Cacheable Size

(0000):Disabled

0001:4KB

0010:8KB

0011:16KB

0100:32KB

0101:64KB

0110:128KB

0111:256KB

1000:512KB

1001:1MB

1010:2MB

1011:4MB

---

### Name: Block 2 Non-Cacheable address A23 to A16 (READ/WRITE)

Index Bits Values and Functions

34H 7:0 (00000000) : Block 2 Non-Cacheable address A23 to A16

---

## Index Registers

---

### Name: Block 2 Non-Cacheable address A15 to A12 and Size (READ/WRITE)

Index	Bits	Values and Functions
-------	------	----------------------

35H	7:4	(0000) : Block 2 Non-Cacheable address A15 to A12
	3:0	Non-Cacheable Size
		(0000):Disabled
		0001:4KB
		0010:8KB
		0011:16KB
		0100:32KB
		0101:64KB
		0110:128KB
		0111:256KB
		1000:512KB
		1001:1MB
		1010:2MB
		1011:4MB

---

### Name: Block 3 Non-Cacheable address A23 to A16 (READ/WRITE)

Index	Bits	Values and Functions
-------	------	----------------------

36H	7:0	(00000000) : Block 3 Non-Cacheable address A23 to A16
-----	-----	-------------------------------------------------------

---

### Name: Block 3 Non-Cacheable address A15 to A12 and Size (READ/WRITE)

Index	Bits	Values and Functions
-------	------	----------------------

37H	7:4	(0000) : Block 3 Non-Cacheable address A15 to A12
	3:0	Non-Cacheable Size
		(0000):Disabled
		0001:4KB
		0010:8KB
		0011:16KB
		0100:32KB
		0101:64KB
		0110:128KB
		0111:256KB
		1000:512KB
		1001:1MB
		1010:2MB
		1011:4MB

---

**Name: Non-Cacheable address A26 to A24  
(READ/WRITE)**

**Index    Bits    Values and Functions**

**38H    7:6    (00) : Reserved**

**5:3    (000) : Block 1 Non-Cacheable address A26 to A24**

**2:0    (000) : Block 0 Non-Cacheable address A26 to A24**

---

**Name: Non-Cacheable address A26 to A24 to A12  
(READ/WRITE)**

**Index    Bits    Values and Functions**

**39H    7:6    (00) : Reserved**

**5:3    (000) : Block 3 Non-Cacheable address A26 to A24**

**2:0    (000) : Block 2 Non-Cacheable address A26 to A24**

---

**Index    Bits    Values and Functions**

**60H    7:6    (00) : Reserved**

**5    Alemate CPU reset. A low to high transition activates a CPU reset (RESET3)**

**4:0    (00000) : Reserved**

---

## Index Registers

---

### Name: Fast Reset Control Register

Direct Port Bits Values and Functions  
Access

92H 7:2 (000000) Reserved

- 1 Fast GATE A20
  - (0) : Force CPU A20 low
  - (1) : Enable CPU A20
- 0 (1) : Enable CPU reset
  - (0) : A 0 to 1 transition causes a CPU reset

Note : This port is used by OS2 and is disabled by writing a 0 to register 2B bit 6.

## 6. Trouble Shooting

The simple inspection methods for end user

---

Situation	Solution
No screen No light for "Power LED" No fan	<b>*Ensure your computer plug on and the power under the normal condition.</b> <b>*Ensure the connector of computer back site without unconnecting.</b>
No screen No light for "Power LED" Have voice of fan	<b>*Ensure power on the monitor and adjust to appropriate light of screen to avoid too dark to identify signal.</b>
Disability of booting for floppy disk & hard disk	<b>*Confirm disk can be booted the "DOS".</b> <b>*Make sure disk is clean.</b>  <b>*Make disk has been inserted at right site.</b>
No way to key-in	<b>*Please examine the power code of keyboard if connected with the printer. Besides, nothing put upon the keyboard while trun on to avoid misdiagnosis of keyboard status.</b>
For new equipment installation	<b>*Please contact with your local agency if you want to move the computer or add any new equipments.</b>



