M9N System

Service Guide

100% Recycled Paper

Copyright

Disclaimer

Acer Incorporated makes no representations or warranties, either expressed or implied, with respect to the contents hereof and specifically disclaims any warranties of merchantability or fitness for any particular purpose. Any Acer Incorporated software described in this manual is sold or licensed "as is". Should the programs prove defective following their purchase, the buyer (and not Acer Incorporated, its distributor, or its dealer) assumes the entire cost of all necessary servicing, repair, and any incidental or consequential damages resulting from any defect in the software. Further, Acer Incorporated reserves the right to revise this publication and to make changes from time to time in the contents hereof without obligation of Acer Incorporated to notify any person of such revision or changes.

About this Manual

Purpose

This service guide aims to furnish technical information to the service engineers and advanced users when upgrading, configuring, or repairing the M9N system.

Manual Structure

This service guide contains technical information about the M9N system. It consists of three chapters and five appendices.

Chapter 1 System Introduction

This chapter describes the system features and major components. It contains the M9N system board layout, block diagrams, cache and memory configurations, power management and mechanical specifications, and operation theory.

Chapter 2 Major Chipsets

This chapter describes the features and functions of the major chipsets used in the system board, including the Pentium II processor. It also includes chipset block diagrams, pin diagrams, and pin descriptions.

Chapter 3 BIOS Setup Utility

This chapter describes the parameters in the BIOS Utility screens.

Appendix A Model Definition

This appendix shows the different configuration options for the M9N system.

Appendix B Spare Parts List

This appendix lists the spare parts for the M9N system with their part numbers and other information.

Appendix C Schematics

This appendix contains the schematic diagrams for the system board.

Appendix D Silk Screens

This appendix illustrates the system board and CPU silk screens.

Appendix E BIOS POST Check Points

This appendix lists and describes the BIOS POST check points.

Conventions

The following are the conventions used in this manual:

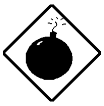
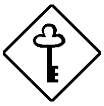
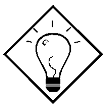
`Text entered by user`	Represents text input by the user.
`Screen messages`	Denotes actual messages that appear onscreen.
ALT, ENTER, F8, etc.	Represent the actual keys that you have to press on the keyboard.
	**NOTE** Gives bits and pieces of additional information related to the current topic.
	**WARNING** Alerts you to any damage that might result from doing or not doing specific actions.
	**CAUTION** Gives precautionary measures to avoid possible hardware or software problems.
	**IMPORTANT** Reminds you to do specific actions relevant to the accomplishment of procedures.
	**TIP** Tells how to accomplish a procedure with minimum steps through little shortcuts.

Table of Contents

Chapter 1 System Introduction

1.1 Overview 1-1
1.1.1 System Board 1-1
1.1.2 CPU Board 1-1
1.1.3 Features 1-2
1.2 Board Layouts 1-3
1.2.1 System Board 1-3
1.2.2 CPU Board 1-4
1.3 Jumpers and Connectors 1-5
1.3.1 System Board 1-5
1.3.2 CPU Board 1-8
1.4 Specifications 1-10
1.4.1 System 1-10
1.4.2 CPU 1-11
1.4.3 BIOS 1-11
1.4.4 System Memory 1-12
1.4.5 Memory Configurations 1-12
1.4.6 Video Interface 1-13
1.4.7 Video Memory 1-13
1.4.8 Video Display Modes and Refresh Rates 1-13
1.4.9 Parallel Port 1-14
1.4.10 Serial Port 1-14
1.4.11 HDD (IDE) Interface 1-14
1.4.12 HDD (SCSI) Interface 1-15
1.4.13 Memory Address Map 1-15
1.4.14 PCI INTx# Map 1-16
1.4.15 Interrupt Channels Map 1-16
1.4.16 I/O Address Map 1-17
1.4.17 DMA Channels Map 1-18

Chapter 2 Major Chipsets

2.1 Pentium II Processor....2-1

2.1.1 Features....2-1

2.1.2 Slot Pin Diagram....2-2

2.1.3 BIOS Update Code....2-3

2.1.4 Pentium II Processor Card Edge Signal List....2-4

2.2 Intel 440FX PCIsets (82441FX and 82442FX)....2-11

2.2.1 Features....2-13

2.2.2 Block Diagrams....2-15

2.2.3 Pin Diagrams....2-16

2.2.4 Signal Descriptions....2-18

2.3 Intel 82371SB....2-30

2.3.1 Features....2-30

2.3.2 Block Diagram....2-31

2.3.3 Pin Diagram....2-32

2.3.4 Signal Descriptions....2-33

2.4 DEC 21152....2-45

2.4.1 Features....2-45

2.4.2 Block Diagram....2-46

2.4.3 Pin Diagram....2-47

2.4.4 Signal Descriptions....2-48

2.5 ATI 264VT....2-60

2.5.1 Features....2-60

2.5.2 Block Diagram....2-61

2.5.3 Pin Diagram....2-62

2.5.4 Signal Descriptions....2-63

2.6 Adaptec AIC 7880....2-68

2.6.1 Features....2-68

2.6.2 Block Diagram....2-71

2.6.3 Pin Diagram....2-72

2.6.4 Signal Descriptions....2-73

2.7 Intel S82093....2-84

2.7.1 Features....2-85

2.7.2 Block Diagram....2-85

2.7.3 Pin Diagram 2-86

2.7.4 Signal Descriptions 2-87

2.8 Intel S82557 2-91

2.8.1 Features 2-91

2.8.2 Block Diagram 2-92

2.8.3 Pin Diagram 2-93

2.8.4 Signal Descriptions 2-94

2.9 NS DP83223 2-100

2.9.1 Features 2-100

2.9.2 Block Diagram 2-101

2.9.3 Pin Diagram 2-101

2.9.4 Signal Descriptions 2-102

2.10 NS DP83840 2-104

2.10.1 Features 2-104

2.10.2 Block Diagram 2-105

2.10.3 Pin Diagram 2-105

2.10.4 Signal Descriptions 2-106

2.11 NS LM78CCVF 2-116

2.11.1 Features 2-116

2.11.2 Block Diagram 2-117

2.11.3 Pin Diagram 2-118

2.11.4 Signal Descriptions 2-119

2.12 SMC 37C935 2-121

2.12.1 Features 2-121

2.12.2 Block Diagram 2-123

2.12.3 Pin Diagram 2-124

2.12.4 Signal Descriptions 2-125

Chapter 3 BIOS Setup Utility

3.1 Entering Setup 3-1

3.2 Basic System Configuration 3-2

3.2.1 Date and Time 3-3

3.2.2 Diskette Drives 3-4

3.2.3 Onboard IDE 3-4

3.2.4 IDE Drives 3-4

3.2.5 Total Memory 3-5

3.2.6 Enhanced IDE Features 3-5

3.2.7 Num Lock After Boot 3-6

3.2.8 Memory Test 3-6

3.2.9 Quiet Boot 3-6

3.2.10 Configuration Table 3-7

3.3 Advanced System Configuration 3-8

3.3.1 Internal Cache (CPU Cache) 3-8

3.3.2 External Cache (CPU Cache) 3-8

3.3.3 Cache Scheme 3-8

3.3.4 ECC/Parity Mode Selection 3-9

3.3.5 Memory at 15MB-16MB 3-9

3.3.6 MP Fault Tolerance 3-9

3.4 PCI System Configuration 3-10

3.4.1 PCI IRQ Setting 3-11

3.4.2 VGA Palette Snoop 3-12

3.4.3 PCI Slot Latency Time 3-12

3.4.4 Onboard LAN 3-12

3.4.5 USB Host Controller 3-12

3.4.6 Onboard SCSI 1 3-12

3.4.7 Onboard SCSI 2 3-12

3.4.8 RAID Port Boot 3-13

3.4.9 PCI IRQ Sharing 3-13

3.4.10 Plug & Play OS 3-13

3.4.11 Reset Resource Assignments 3-13

3.5 System Security 3-14
3.5.1 Disk Drive Control 3-15
3.5.2 Onboard Communication Ports 3-15
3.5.3 Onboard PS/2 Mouse (IRQ12) 3-17
3.5.4 Setup Password 3-18
3.5.5 Power On Password 3-20
3.6 Remote Diagnostic Configuration 3-21
3.7 Load Setup Default Settings 3-22
3.8 Leaving Setup 3-22

Appendices

Appendix A Model Definition

Appendix B Spare Parts List

Appendix C Schematics

Appendix D Silk Screens

Appendix E BIOS POST Check Points

List of Figures

1-1 System Board Layout ... 1-3
1-2 CPU Board Layout ... 1-4
1-3 System Board Jumper and Connector Locations ... 1-5
1-4 Pentium II CPU Board Jumper Locations ... 1-8
2-1 Pentium II Second-Level Cache Implementation ... 2-2
2-2 Pentium II Slot 1 Pin Diagram ... 2-2
2-3 82441FX (PMC) Block Diagram ... 2-15
2-4 82442FX (DBX) Block Diagram ... 2-15
2-5 82441FX (PMC) Pin Diagram ... 2-16
2-6 82441FX (DBX) Pin Diagram ... 2-17
2-7 82371SB (PIIX3) Block Diagram ... 2-31
2-8 82371SB (PIIX3) Pin Diagram ... 2-32
2-9 DEC 21152 Block Diagram ... 2-46
2-10 DEC 21152 Pin Diagram ... 2-47
2-11 ATI 264VT Block Diagram ... 2-61
2-12 ATI 264VT Pin Diagram ... 2-62
2-13 AIC 7880 Block Diagram ... 2-71
2-14 AIC 7880 Pin Diagram ... 2-72
2-15 S82093 Block Diagram ... 2-85
2-16 S82093 Pin Diagram ... 2-86
2-17 82557 Block Diagram ... 2-92
2-18 82557 Pin Diagram ... 2-93
2-19 DP83223 Block Diagram ... 2-101
2-20 DP83223 Pin Diagram ... 2-101
2-21 DP83840 Block Diagram ... 2-105
2-22 DP83840 Pin Diagram ... 2-105
2-23 LM78CCVF Block Diagram ... 2-117
2-24 LM78CCVF Pin Diagram ... 2-118
2-25 SMC 37C935 Block Diagram ... 2-123
2-26 SMC 37C935 Pin Diagram ... 2-124

List of Tables

1-1 System Board Jumper Settings 1-6
1-2 System Board Connector Functions 1-7
1-3 Settings for CPU Core/Bus Frequency Ratio (JP1) 1-8
1-4 Settings for CPU Clock Speed (JP5) 1-9
1-5 CPU Board Connector Functions 1-9
1-6 System Specifications 1-10
1-7 CPU Specifications 1-11
1-8 BIOS Specifications 1-11
1-9 System Memory Specifications 1-12
1-10 Memory Configurations 1-12
1-11 Video Interface Specifications 1-13
1-12 Video Memory Specifications 1-13
1-13 Display Modes and Refresh Rates for EDO DRAM 1-13
1-14 Parallel Port Interface 1-14
1-15 Serial Port Interface 1-14
1-16 HDD Interface 1-14
1-17 HDD Interface 1-15
1-18 Memory Address Map 1-15
1-19 PCI INTx# Map 1-16
1-20 Interrupt Channels Map 1-16
1-21 I/O Address Map 1-17
1-22 DMA Channels Map 1-18
2-1 Pentium II Processor Card Edge Signal List 2-4
2-2 82440FX PCIset Signal Type Descriptions 2-18
2-3 82440FX PCIset Buffer Types Descriptions 2-18
2-4 82441FX (PMC) Signal Descriptions 2-19
2-5 82442FX (DBX) Signal Descriptions 2-27
2-6 82371SB (PIIX3) Signal Descriptions 2-33
2-7 DEC 21152 Signal Type Descriptions 2-48
2-8 DEC 21152 Signal Descriptions 2-48
2-9 ATI 264VT Signal Descriptions 2-63
2-10 AIC 7880 Signal Type Descriptions 2-73
2-11 AIC 7880 Signal Descriptions 2-73
2-12 S82093 Signal Descriptions 2-87

2-13 S82093 Signal Descriptions..2-87
2-14 82557 Signal Descriptions 2-94
2-15 DP83223 Signal Descriptions 2-102
2-16 DP83840 Signal Descriptions 2-106
2-17 LM78CCVF Signal Descriptions..2-119
2-18 SMC 37C935 Signal Type Descriptions..2-125
2-19 SMC 37C935 Signal Descriptions...2-125
3-1 Drive Control Settings 3-15
3-2 Serial Port 1 Settings 3-15
3-3 Serial Port 2 Settings 3-16
3-4 Parallel Port Settings...3-16
3-5 Parallel Port Operation Mode Settings..3-17

Chapter 1

System Introduction

1.1 Overview

The M9N is a dual-processor system board that supports the Intel Pentium II CPU. It contains an exclusive connector for the CPU board that carries two slots for the Pentium II CPU modules.

1.1.1 System Board

This high-performance 64-bit system board utilizes both the ISA and the PCI local bus architecture. Two ISA and five PCI bus slots reside on the board to allow installation of either master or slave devices.

One 50-pin Fast SCSI-II interface and two 68-pin Wide SCSI interfaces come with the system board to connect SCSI devices. External I/O interfaces include a parallel port and a video port, RJ-45 and USB connectors, and keyboard and mouse ports.

The system board supports two optional features, the ASM Pro and the remote diagnostic management (RDM), that allow better server management. The ASM Pro detects problems in CPU thermal condition, system and CPU working voltage detection (±12V/±5V/3.3V/1.5V), and PCI bus utilization calculation. It also detects if the CPU fan or the chassis fan malfunctions. The RDM allows execution of the RDM diagnostic program from a remote RDM station to fix detected problems or to reboot the system.

1.1.2 CPU Board

The CPU board carries two sockets to support a powerful dual-CPU configuration. The sockets accommodate the new Intel Pentium II CPU running at 233/266 MHz. The Pentium II CPU incorporates the first-level cache and boasts a new generation of power.

The board comes with four DRAM banks composed of four 168-pin dual-inline memory module (DIMM) sockets that accommodate extended data output (EDO) DIMMs.

Designed to work with Intel 440FX PCIset, the board includes the PCI bridge/memory controller (PMC) and the data bus accelerator (DBX) chipsets. The PMC provides bus control signals and address paths for transfers between the host bus, PCI bus, and the main memory. The DBX supports multiple-bit error detection and single-bit error correction through the ECC/parity feature.

1.1.3

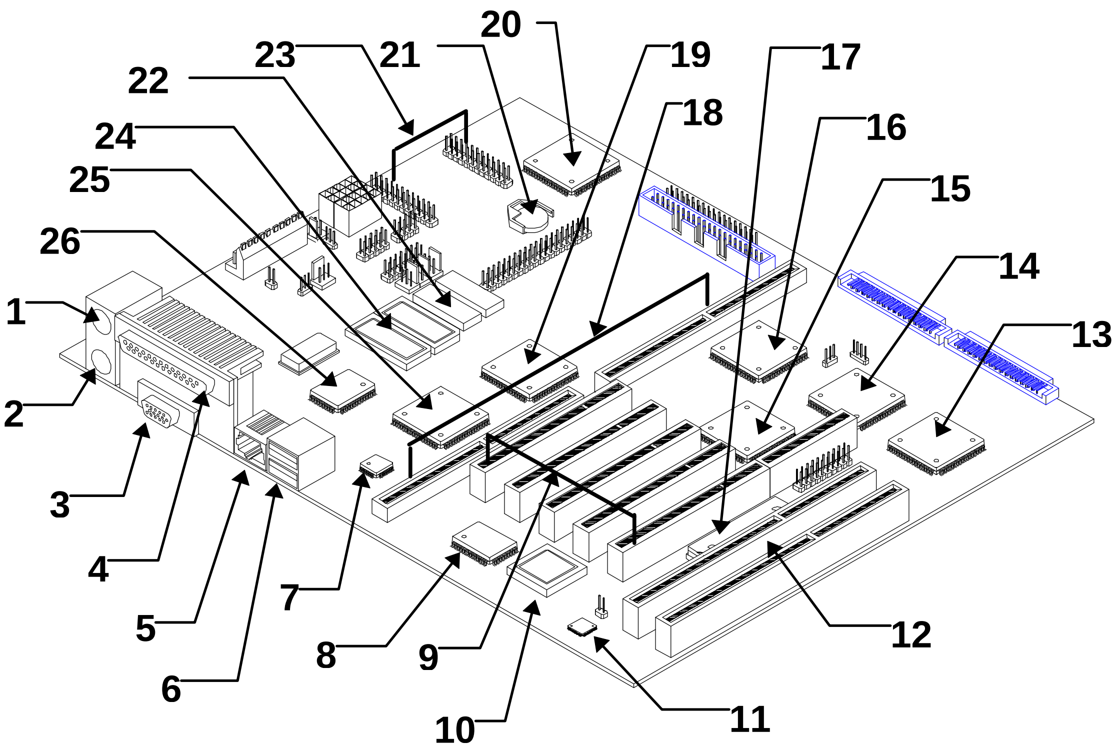
Features

The M9N system has the following features:

- Two ISA and five PCI bus slots (one PCI slot may include an optional RAID port)
- Four DIMM banks composed of four 168-pin DIMM sockets that support 32/64/128-MB, 60ns, EDO-type DIMMs
- One 50-pin Fast SCSI-II and two 68-pin Wide SCSI interfaces
- One E-IDE hard disk and one diskette drive interface
- Standard 1-MB video EDO RAM onboard plus two upgrade sockets for up to 2-MB video memory
- 256-KB flash ROM BIOS for system, video and SCSI
- System clock/calendar with battery backup
- ASM Pro and remote diagnostic management (RDM) features
- External ports:
  - PS/2 keyboard and mouse ports
  - Two buffered high-speed serial headers (NS16C550-compatible UARTs with 16-byte FIFOs)
  - One ECP/EPP high-speed parallel port (IEEE 1284-compliant)
  - Two Universal Serial Bus (USB) ports
  - Ethernet RJ-45 port
  - Video port
- Onboard controller chipsets
  - PCI bridge/memory controller (PMC 82441FX)
  - Data bus accelerator (DBX 82442FX)
  - PCI-ISA Xelerator (PIIX3, 82371SB)
  - SCSI controller (AIC 7880)
  - PCI-to-PCI Bridge (DEC 21152)
  - Super I/O controller (SMC 37C935)
  - 10/100 Base-T Ethernet controller (Intel S82557)
  - 10/100 Base-T Ethernet twisted pair transceiver (NS DP83223)
  - Ethernet decoder (NS DP83840)
  - PCI local bus VGA with enhanced GUI acceleration (ATI 264VT)
  - I/O APIC (Intel S82093)
  - System hardware monitor (NS LM78CCVF)

1.2 Board Layouts

1.2.1 System Board

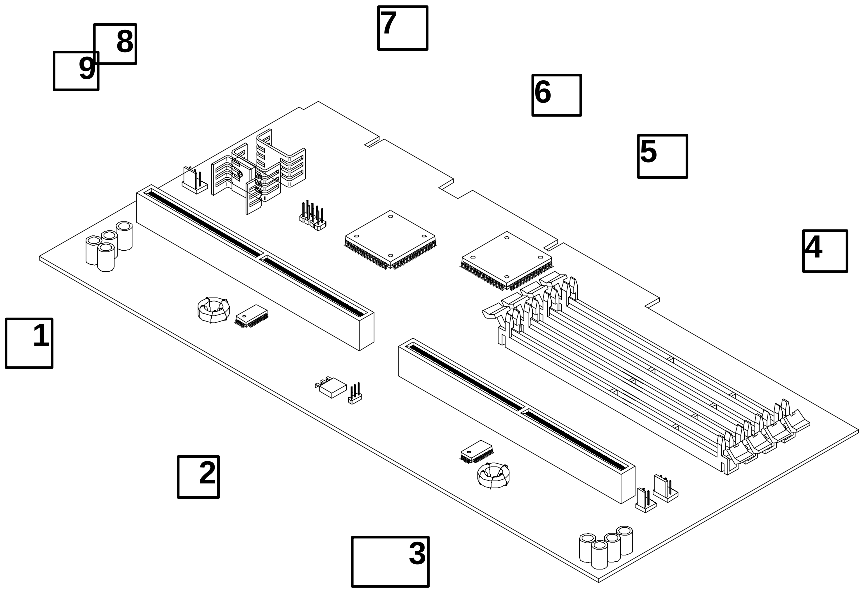


1 *Mouse port*
2 *Keyboard port*
3 *Video port*
4 *Parallel port*
5 *Ethernet connector*
6 *USB connectors*
7 *Ethernet transceiver (DP83223)*
8 *I/O APIC (S82093)*
9 *PCI slots*
10 *PLD, ASM IRQ mapper*
11 *Hardware monitor (LM78CCVF)*
12 *ISA slots*
13 *SCSI controller (AIC7880)*
14 *SCSI controller (AIC 7880)*
15 *PCI-to-PCI bridge (DEC21152)*
16 *PCI-ISA Xelerator (PIIX3, 82371SB)*
17 *Flash ROM BIOS*
18 *Pentium II CPU board slots*
19 *VGA controller (ATI 264VT)*
20 *Super I/O controller (SMC37C935)*
21 *RTC battery*
22 *Video memory*
23 *RDM daughter board connectors*
24 *Video memory upgrade sockets*
25 *Ethernet controller (S82557)*
26 *Ethernet decoder (DP83840)*

Figure 1- 1 System Board Layout

1.2.2

CPU Board

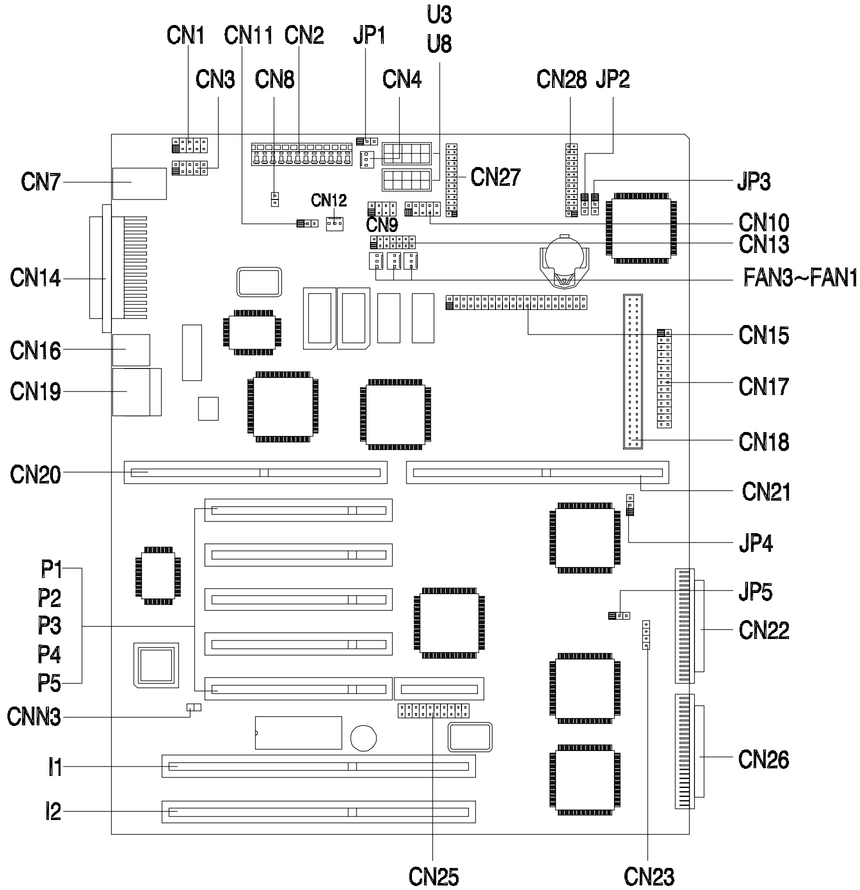


1 *CPU 2 slot*
2 *CPU voltage regulator (2.5V)*
3 *CPU 1 slot*
4 *DIMM sockets*
5 *PCI/memory controller (82441FX)*
6 *Data bus accelerator (82442FX)*
7 *CPU voltage regulator (3.3V)*
8 *CPU voltage regulator (3.3V)*
9 *CPU voltage regulator (1.5V)*

Figure 1- 2 CPU Board Layout

1.3 Jumpers and Connectors

1.3.1 System Board



Jumpers are prefixed "JP". Connectors are prefixed "CN". The blackened pin of a jumper represents pin 1.

Figure 1- 3 System Board Jumper and Connector Locations

1.3.1.1

System Board Jumper Settings

Table 1-1 lists the system board jumpers with their corresponding settings and functions.

Table 1- 1 System Board Jumper Settings

Jumper	Setting	Function
Software Shutdown Power Supply Type Select JP1	1-2 2-3*	If **CN4** is connected to the standby power of power supply. If **CN12** is connected to the standby power of power supply.
BIOS Type JP2	1-2 2-3*	Branded Generic
Password Security JP3	1-2 2-3*	Check password Bypass password
SCSI Channel 1 High-Byte Termination JP4	1-2* 2-3 Open	Terminator always set to ON SCSI terminator sets to ON or OFF by SCSI Setup Utility[1] Terminator always set to OFF
VGA Feature JP5	1-2* 2-3	Normal (auto-detect) Onboard VGA always disabled

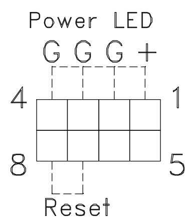
1.3.1.2

* Default setting

[1] Press Ctrl+A during system boot to enter the SCSI Setup Utility.

System Board Connector Functions

Table 1- 2 System Board Connector Functions

Connector	Function
CN1	COM 1
CN2	Power connectors
U3, U8	Power connectors (optional)
CN3	COM 2
CN4, CN12	Standby power connector, connect to power supply. **Important**: This connector may very in different type of power supply, select either CN4 or CN12 to connect.
CN7	Upper: PS/2 mouse connector Lower: Keyboard connector
CN8	Power switch
CN9	 Power LED and reset connector
CN10	Monitor signal connector for redundant power supply
CN11	Test connector, to generate NMI signal
CN13	Backplane board LED connector
CN14	Upper: Printer port Lower: Video port
CN15	IDE connector
CN16	LAN connector
CN17	Diskette drive connector
CN18	Channel 1 narrow SCSI connector
CN19	Universal serial bus (USB) port
CN20, CN21	CPU board slots
CN22	Channel 1 wide SCSI connector
CN23	IDE Hard disk LED connector
CN25	SMM connector
CN26	Channel 2 wide SCSI connector
CN27, CN28	RDM daughter board connectors
CNN3	Connector for chassis intrusion prevention
FA1, FA2, FA3	Fan connectors
I1, I2	ISA bus slots
P1, P2, P3, P4	PCI bus slots
P5	PCI bus slot with optional SCSI RAID port support

1.3.2 CPU Board

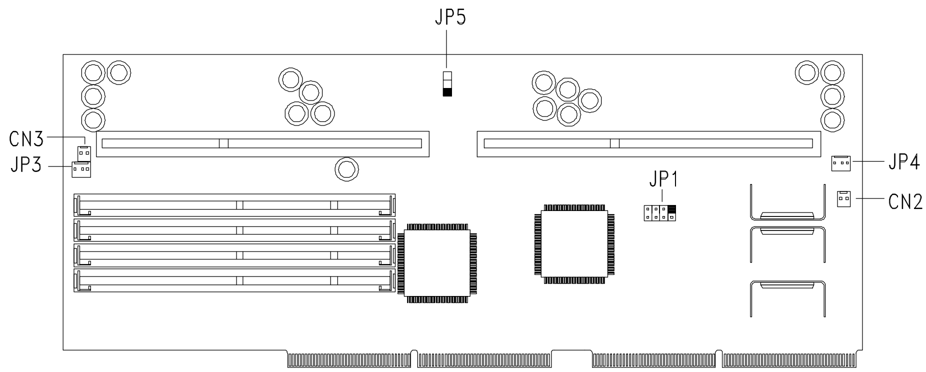
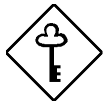


Figure 1- 4 Pentium II CPU Board Jumper Locations



The system is designed to support either one or two processors. However, if you install only one processor, make sure to install a termination board into the empty processor slot to avoid signal emission. If you intend to install two processors, make sure that the processors have the same speed.

Table 1- 3 Settings for CPU Core/Bus Frequency Ratio and CPU Clock Frequency

JP1 Settings				
1-2	**3-4**	**5-6**	**7-8**	**CPU Core/Bus Freq.**
1	1	1	1	2
1	1	0	1	3
1	1	1	0	4
1	1	0	0	2.5
1	0	0	1	3.5*
JP5 Settings				
1-2		**2-3**		**CPU Clock Speed**
1		0		66 MHz*
0		1		60 MHz

Note: 0 - Pins open 1 - Pins closed

Jumpers JP1 and JP5 set the CPU core/bus frequency ratio and the CPU clock for the two processor slots.

Table 1- 4 CPU Board Connector Functions

Connector	Function
JP3, JP4	Thermal detection from CPU heatsinks
CN2, CN3	Fan connectors for CPU heatsinks

1.4

* Default setting

Specifications

1.4.1 System

Table 1- 5 System Specifications

Item	Description
CPU	Single or dual Intel Pentium II
System Memory	Four DIMM sockets on CPU board that supports up to 512 MB of system memory using 60ns EDO type, 32/64/128-MB DIMMs
Video Memory	Onboard 1-MB (256K*16x2) EDO memory upgradable to 2-MB by installing another two pieces of 256K*16, 60ns SOJ chip to the upgrade sockets (U36, U37).
BIOS[2]	256-KB Flash ROM for system, video and SCSI BIOS
Video Interface	Onboard ATI264VT PCI accelerator that supports a resolution of 1024x768, 65536-color interlaced with 2-MB video RAM installed.
Hard Disk Interface	One PCI bus master type E-IDE interface supports up to two IDE devices. Two PCI bus master type wide SCSI interfaces support up to thirty (fifteen on each channel) SCSI devices.
Diskette Drive Interface	One diskette drive interface that supports 2.88/1.44/1.2-MB diskette drives Supports three-mode diskette type
Network	One RJ11 Ethernet connector
Onboard I/O	One PS/2 keyboard port (6-pin, mini-din type x1) One PS/2 mouse port (6-pin, mini-din type x1) Two NS16C550-compatible serial ports (9-pin header) One ECP/EPP parallel port (15-pin D-type x1) Two USB ports
Real-time Clock	System clock/calendar with 128 bytes extended CMOS RAM and battery backup
Expansion Slot	Two Pentium II S.E.C. cartridge board slots (Slot 1) Five secondary level PCI bus slots Two ISA bus slots
Power Supply	200/250/420-watt switching power supply
Housing	IDUR, IDT, or IDATX

1.4.2

[2] Supports PCI v2.1 and PnP v1.0a protocols.

CPU

Table 1- 6 CPU Specifications

Item	Specification
Type	Intel Pentium II in single-edge contact (S. E. C.) cartridge package. The system is designed to support either one or two processors. However, if you install only one processor, make sure to install a termination board into the empty processor slot to avoid signal emission. If you intend to install two processors, make sure that the processors have the same speed.
Slot package	Slot 1[3]
Speed	233 MHz, 266 MHz
Minimum operating speed	0 MHz (when the system is in suspend mode)
Voltage	Processor voltage can be detected by the system without setting any jumper.

1.4.3 BIOS

Table 1- 7 BIOS Specifications

Item	Specification
Program vendor	Acer
Version	V2.0
ROM type	Bulk mode (29EE020) Flash ROM without boot block protection.
ROM size[4]	256KB
ROM package type	32-pin DIP package
Contents	System, video and SCSI
Boot from CD-ROM feature	No
Support protocols	PCI BIOS specification revision 2.1 MP specification 1.4 PCI to PCI bridge version 1.0 PnP BIOS specification revision 1.0A ESCD specification version 1.03 E-IDE
Password control	Check/bypass by jumper setting (JP3)
Acer logo display control during POST	Enable/disable by jumper setting (JP2)

1.4.4

[3] Slot 1 defines mechanical and electrical specification for Pentium II processor slot. It is defined and developed by Intel®.

[4] Set JP7 for the appropriate Flash ROM size.

System Memory

Table 1- 8 System Memory Specifications

Item	Specification
Onboard memory size	0 MB
DIMM socket number	Four DIMM sockets on CPU board
Support per DIMM memory size	32MB / 64MB / 128MB
Support maximum memory size	512MB (128MB x4)
Support DIMM speed (access time)	60ns
Support DIMM voltage	3.3V
Support DIMM package	168-pin DIMM
Support DIMM type	EDO

1.4.5 Memory Configurations

Table 1- 9 Memory Configurations

DIMM1	DIMM2	DIMM3	DIMM4	Total Memory
32 MB				32 MB
32 MB	32 MB			64 MB
32 MB	32 MB	32 MB		96 MB
32 MB	32 MB	32 MB	32 MB	128 MB
32 MB	32 MB	64 MB	64 MB	192 MB
64 MB				64 MB
64 MB	64 MB			128 MB
64 MB	64 MB	64 MB		192 MB
64 MB	64 MB	64 MB	64 MB	256 MB
64 MB	64 MB	128 MB	128 MB	384 MB
128 MB				128 MB
128 MB	128 MB			256 MB
128 MB	128 MB	128 MB		384 MB
128 MB	128 MB	128 MB	128 MB	512 MB

The above configurations are only some of the available memory combinations. When upgrading memory, simply install DIMMs into any of the empty sockets.

1.4.6

Video Interface

Table 1- 10 Video Interface Specifications

Item	Specification
Video controller	ATI 264VT
Video controller resident bus	PCI bus
Video function control	Enable/disable video by either jumper setting (JP5) or auto-detect.

1.4.7 Video Memory

Table 1- 11 Video Memory Specifications

Item	Specification	
Size	1MB	2MB
Type	EDO RAM	
Configuration	256K*16 x 2	256K*16 x 4
Upgrade	1st MB is fixed onboard, 2nd MB is upgradeable	
Speed	60ns	
Voltage	5V	
Package	SOJ 40-pin	

1.4.8 Video Display Modes and Refresh Rates

Table 1- 12 Display Modes and Refresh Rates for EDO DRAM

Resolution	256 colors		64K colors		16.7M colors	
	1 MB	2 MB	1 MB	2 MB	1 MB	2 MB
640 x 480	100	100	100	100	90	100
800 x 600	100	100	90	100	—	100
1024 x 768	100	100	—	100	—	—
1152 x 864	80	80	—	80	—	—
1280 x 1024	*	75	—	—	—	—

* - The resolution 1280 x 1024 @ 16 colors is available at 75 Hz.

1.4.9

Parallel Port

Table 1- 13   Parallel Port Interface

Item	Specification
Parallel port controller	SMC 37C935
Parallel port controller resident bus	ISA bus
Number of parallel ports	1
ECP/EPP support	Yes
Selectable ECP DMA channel (through BIOS Setup)	DMA channel 1 DMA channel 3
Connector type	15-pin D-type female connector
Selectable parallel port (through BIOS Setup)	3BCh (IRQ 7) 378h (IRQ 7) 278h (IRQ 5) Disabled

1.4.10 Serial Port

Table 1- 14   Serial Port Interface

Item	Specification
Serial port controller	SMC 37C935
Serial port controller resident bus	ISA bus
Number of serial ports	2
16550 UART support	Yes
Connector type	9-pin header
Selectable serial port (by BIOS Setup)	3F8h 2F8h 3E8h 2E8h Disabled

1.4.11 HDD (IDE) Interface

Table 1- 15   HDD Interface

Item	Specification
IDE controller	Built-in of PIIX3 (Bus master type)
IDE controller resident bus	PCI bus
Number of IDE channel	One (CN15)
Support IDE interface	E-IDE (up to PIO mode 5 and DMA mode 2), ANSIS ATA rev.3.0, ATAPI

1.4.12

HDD (SCSI) Interface

Table 1- 16 HDD Interface

Item	Specification
SCSI controller	Two AIC7880
SCSI controller resident bus	PCI bus (Bus master type)
Number of SCSI channel	Three (one narrow SCSI CN18 and two wide SCSI CN22,CN26)
Support SCSI interface	8-bit Narrow SCSI 16-bit fast wide SCSI

1.4.13 Memory Address Map

Table 1- 17 Memory Address Map

Address	Size	Function
0000000 ~ 009FFFF	640 KB system memory	Onboard DRAM
00A0000 ~ 00BFFFF	128 KB video RAM	Reserved for graphics display buffer, non-cacheable
00C0000 ~ 00C7FFF	32 KB for VGA BIOS	Reserved for onboard VGA
00C8000 ~ 00CFFFF	32 KB I/O expansion ROM	Reserved for ROM on I/O adapters
00D0000 ~ 00D3FFF	16 KB I/O expansion ROM	Reserved for ROM on I/O adapters
00D4000 ~ 00D7FFF	16 KB I/O expansion ROM	Reserved for ROM on I/O adapters
00D8000 ~ 00DBFFF	16 KB I/O expansion ROM	Reserved for ROM on I/O adapters
00DC000 ~ 00DFFFF	16 KB I/O expansion ROM	Reserved for ROM on I/O adapters
00E0000 ~ 00E7FFF	32 KB for SCSI BIOS	Reserved SCSI BIOS
00E8000 ~ 00EFFFF	32 KB	Reserved onboard (video RAM BIOS)
00F0000 ~ 00FFFFF	64 KB BIOS	System ROM BIOS (ROM) System RAM BIOS (DRAM)
0100000 ~ 0F9FFFF	System memory	Onboard DRAM
0FA0000 ~ 0FFFFFF	384 KB I/O card memory	Reserved for memory map I/O card, non-cacheable
1000000 ~ Upper limit[5]	System memory	Onboard DRAM

1.4.14

[5] Upper limit means the maximum size of main memory.

PCI INTx# Map

Table 1- 18   PCI INTx# Map

PCI Bus#	PCI INTx	PCI Device
PCI Bus 0	INTA	PCI slot s1, 2, 3
	INTB	PCI slots 1, 2, 3
	INTC	PCI slots 1, 2, 3
	INTD	PCI slots 1, 2, 3; LAN
PCI Bus 1	INTA	PCI slots 4, 5
	INTB	PCI slots 4, 5
	INTC	PCI slots 4, 5, SCSI channel 1
	INTD	PCI slots 4, 5, SCSI channel 2

1.4.15 Interrupt Channels Map

Table 1- 19   Interrupt Channels Map

IRQ	System Device
IRQ0	Timer output 0
IRQ1	Keyboard
IRQ2	Reserved
IRQ3	Serial port 2
IRQ4	Serial port 1
IRQ5	Reserved
IRQ6	Diskette drive
IRQ7	Parallel port
IRQ8	Real-time clock
IRQ9	Reserved
IRQ10	Reserved
IRQ11	Reserved
IRQ12	PS/2 mouse
IRQ13	Math coprocessor
IRQ14	IDE hard disk
IRQ15	Reserved

1.4.16

I/O Address Map

Table 1- 20 I/O Address Map

Hex Range	Device
Standard I/O Addresses	
000 ~ 01F	DMA controller 1, (8237)
020 ~ 027	Interrupt controller 1, (8259)
030 ~ 037	Interrupt controller 1, (8259)
040 ~ 047	System timer (8254-1)
050 ~ 057	System timer (8254-1)
060 ~ 06F	Keyboard controller (8742)
070 ~ 07F	Real-time clock, NMI mask
080 ~ 09F	DMA page register 74LS612, speed status register
0A0 ~ 0BF	Interrupt controller 2, (8259)
0C0 ~ 0DF	DMA controller 2, (8237)
0F0	Clear math coprocessor busy
0F1	Reset math coprocessor
0F8 ~ 0FF	Math coprocessor
0CF8	PCI configuration address regulation
0CFC	PCI configuration data regulation
1F0 ~ 1F7	Hard disk
278 ~ 27F	Parallel port 2
2F8 ~ 2FF	Serial port 2
378 ~ 37F	Parallel port 1
3B0 ~ 3BF	Monochrome display
3C0 ~ 3CF	EGA, VGA, SVGA
3D0 ~ 3DF	CGA, VGA, SVGA
3F0 ~ 3F7	Diskette drive controller
3F7 ~ 3FF	Serial port 1

Table 1- 20   I/O Address Map

Hex Range	Device
Special I/O Addresses	
4A0*	Software power down Software reset RAID port card detect Onboard VGA enabled/disable Flash ROM programming RDM reset
4A1*	Fan status VRM ID
4A2*	PCI utilization counter
4A3*	PCI utilization counter
4A4*	Redundant power supply status
4A5*	LAN disabled Keyboard/mouse power status Housing fan enabled USB power status PCI counter stop control SCSI termination power status PCI counter clear CPU MUX select I^2C clock I^2C data
4A6*	RDM I/O ports
4A7*	Backplane board hard disk failed indicator
4A7~4AF*	ASM controller Secondary PCI device IRQ select

1.4.17 DMA Channels Map

Table 1- 21   DMA Channels Map

Channel	Function
0	Available
1	Available
2	Diskette drive controller
3	Available
4	Cascaded
5	Available
6	Available
7	Available

* Special I/O port

Chapter 2

Major Chipsets

2.1 Pentium II Processor

The Pentium® II processor, known until now by the code name Klamath, integrates the benefits of the Pentium II processor with Intel's MMX™ media enhancement technology. It is offered in an innovative packaging design called Single Edge Contact package, or S.E.C. package. This new package design paves the way for future processors of higher performance.

2.1.1 Features

Similar to the Pentium II processor, the Pentium II processor implements a Dynamic Execution micro-architecture which is a unique combination of multiple-branch prediction, data flow analysis and speculative execution. This enables the Pentium II processor to deliver higher performance than the Pentium II processor while maintaining binary compatibility with all previous Intel architecture processors.

Increasing clock frequencies and silicon density complicates system designs. As with the Pentium Pro processor, the Pentium II processor integrates several system components which alleviate some of the previous system burdens. This integration results in the system bus more closely resembling a symmetric multiprocessing (SMP) bus rather than the previous generation processor-to-cache bus. The added level of integration and improved performance (compared to Pentium processor-based systems) results in higher power consumption and a new bus technology. It is very important to ensure adherence to this specification.

From a system perspective, a significant feature of the Pentium II processor is the built-in direct multiprocessing support. In order to achieve multiprocessing and maintain memory and I/O bandwidth to support them, new system designs are needed. The Pentium II processor supports both uni-processor and dual-processor implementations, as well as caching up to 512 MB of addressable memory space. Memory above 512 MB must be set as uncacheable in the processor MTRs.

The Pentium II processor system bus operates in the same manner as the Pentium Pro processor system bus. It uses the GTL+ signal technology. The Pentium II processor deviates from the Pentium Pro processor by using individual components for the second-level cache. The second-level cache (the tag RAM and the burst pipelined synchronous static RAM (BSRAM)) are now separate components). Transfer rates between the Pentium II processor and the second-level cache components are just half of the processor core clock frequency. Both the tag RAM and the BSRAM components receive clocked data directly from the Pentium II processor. As with the Pentium Pro processor, the second level cache does not connect to the Pentium II processor system bus (see Figure 2-1).

The Pentium II processor utilizes the Single Edge Contact (S.E.C.) cartridge packaging technology. The S.E.C. cartridge allows the second-level (L2) cache to remain tightly coupled to the processor, while maintaining flexibility when implementing high-performance processors into OEM systems. The L2 cache performance is optimized and tested at the cartridge level. The S.E.C. cartridge utilizes surface-mount core components and a printed circuit board with an edge-finger connection. This packaging type introduced on the Pentium II processor will also be used in the Deschutes and future slot 1 processors.

The S.E.C. cartridge has the following features: a thermal plate, a cover and a PCB with an edge-finger connector. The thermal plate allows standardized heatsink attachment or customized thermal solutions. The thermal plate enables a reusable heatsink to minimize fit issues for serviceability, upgradability and replacement. The full enclosure also protects the surface-mount components. The edge-finger connection maintains flexibility for system configuration. The edge-finger connector is noted as slot 1 connector in this manual, as well as in the other related documentation.

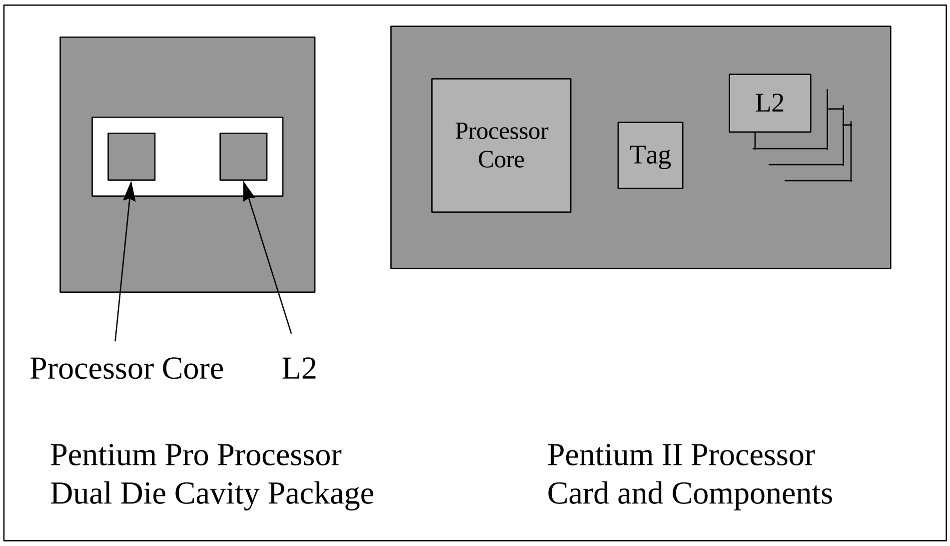


Figure 2- 1 Pentium II Second-Level Cache Implementation

2.1.2 Slot Pin Diagram

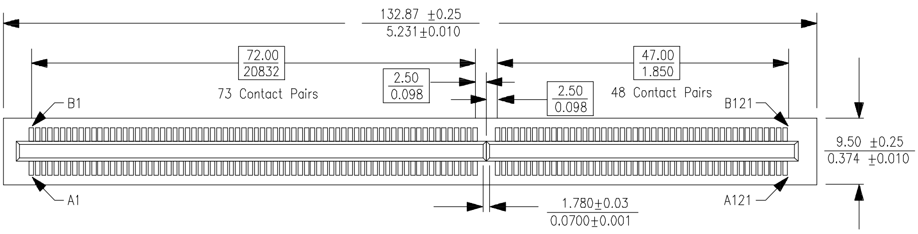


Figure 2- 2 Pentium II Slot 1 Pin Diagram

2.1.3 BIOS Update Code

In order to support Pentium II and Pentium Pro processors to correct specific errata through the loading of an Intel-supplied block, an update loader integrated within the BIOS uses data from the update where BIOS is responsible for loading the update on all processors during system initialization. Each BIOS update (BU) code is tailored for a particular stepping of the Pentium II and Pentium Pro processors which can be obtained from CPUID. BIOS should load each processor with the appropriate update code for its CPUID.

For testing convenience, the Acer BIOS loads as many sets of update code as possible, if the ROM size permits. It can load as much as ten sets of BIOS update code. However, this process still cannot avoid the possibility of another update of BIOS code at QT, UCC, dealer site, and even customer site especially with the purchase a new Pentium Pro processor. To avoid the inconsistency between different models, the Acer BIOS keeps two sets of BIOS update code (see Note 1). Once BIOS detects a BU code mismatch, a mismatch message appears on the screen. In this case, the user can use the utility provided by Intel to load the BIOS update code (see Note 2). The QT, UCC, dealer and service site are responsible for loading the correct BIOS update code. All the updates can be accessed through Intel Web site. Acer also maintains its own service BIOS update code in order to provide consistent service.

Currently, Acer strongly recommends that the user to install only the same stepping of the Pentium II and Pentium Pro processors in the multiprocessor system. Future BIOS versions may incorporate support to multiple steppings of the Pentium II and Pentium Pro processors. This feature will allow operation under mixed stepping environment on an MP system to enable upgrades to later versions of the processor. The Acer BIOS contains two sets of BIOS update code for dual Pentium Pro processors and four sets for quad Pentium Pro processors. The default case is two sets of BU code.

The utility provided by Intel is SETUP1.EXE. This utility can only load the update for booting Pentium II and Pentium Pro processors. Under mixed stepping environment on MP system, the user must load the update for each Pentium II and Pentium Pro processor one at a time. Currently, Intel is still developing a new utility that can support the one-time loading of updates for mixed stepping processors.

2.1.4 Pentium II Processor Card Edge Signal List

Table 2- 1 Pentium II Processor Card Edge Signal List (by Pin Number List)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A1	VCC_VTT	GTL+VTT Supply	B1	EMI	EMI Management
A2	GND	VSS	B2	FLUSH#	CMOS Input
A3	VCC_VTT	GTL+VTT Supply	B3	SMI#	CMOS Input
A4	IERR#	CMOS Output	B4	INIT#	CMOS Input
A5	A20M#	CMOS Input	B5	VCC_VTT	GTL+VTT Supply
A6	GND	VSS	B6	STPCLK#	CMOS Input
A7	FERR#	CMOS Output	B7	TCK	JTAG Input
A8	IGNNE#	CMOS Input	B8	SLP#	CMOS Input
A9	TDI	JTAG Input	B9	VCC_VTT	GTL+VTT Supply
A10	GND	VSS	B10	TMS	JTAG Input
A11	TDO	JTAG Output	B11	TRST#	JTAG Input
A12	PWRGOOD	CMOS Input	B12	Reserved	Reserved
A13	TESTHI	CMOS Test Input	B13	VCC_CORE	CPU Core VCC
A14	GND	VSS	B14	THRMDP	Thermal Diode P Junction(+)
A15	THERMTRIP#	CMOS Output	B15	THRMDN	Thermal Diode N Junction(-)
A16	Reserved	Reserved	B16	LINT[1]/NMI	CMOS Input
A17	LINT[0]/INTR	CMOS Input	B17	VCC_CORE	CPU Core VCC
A18	GND	VSS	B18	PICCLK	APIC Clock Input
A19	PICD[0]	CMOS I/O	B19	BP#[2]	GTL+ I/O
A20	PREQ#	CMOS Input	B20	Reserved	Reserved
A21	BP#[3]	GTL+ I/O	B21	100/66#	BCLK Frequency Select
A22	GND	VSS	B22	PICD[1]	CMOS I/O
A23	BPM#[0]	GTL+ I/O	B23	PRDY#	GTL+ Output
A24	BINIT#	GTL+ I/O	B24	BPM#[1]	GTL+ I/O
A25	DEP#[0]	GTL+ I/O	B25	VCC_CORE	CPU Core VCC
A26	GND	VSS	B26	DEP#[2]	GTL+ I/O
A27	DEP#[1]	GTL+ I/O	B27	DEP#[4]	GTL+ I/O
A28	DEP#[3]	GTL+ I/O	B28	DEP#[7]	GTL+ I/O
A29	DEP#[5]	GTL+ I/O	B29	VCC_CORE	CPU Core VCC
A30	GND	VSS	B30	D#[62]	GTL+ I/O
A31	DEP#[6]	GTL+ I/O	B31	D#[58]	GTL+ I/O
A32	D#[61]	GTL+ I/O	B32	D#[63]	GTL+ I/O
A33	D#[55]	GTL+ I/O	B33	VCC_CORE	CPU Core VCC
A34	GND	VSS	B34	D#[56]	GTL+ I/O
A35	D#[60]	GTL+ I/O	B35	D#[50]	GTL+ I/O
A36	D#[53]	GTL+ I/O	B36	D#[54]	GTL+ I/O

Table 2- 1 Pentium II Processor Card Edge Signal List (by Pin Number List)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A37	D#[57]	GTL+ I/O	B37	VCC_CORE	CPU Core VCC
A38	GND	VSS	B38	D#[59]	GTL+ I/O
A39	D#[46]	GTL+ I/O	B39	D#[48]	GTL+ I/O
A40	D#[49]	GTL+ I/O	B40	D#[52]	GTL+ I/O
A41	D#[51]	GTL+ I/O	B41	EMI	EMI Management
A42	GND	VSS	B42	D#[41]	GTL+ I/O
A43	D#[42]	GTL+ I/O	B43	D#[47]	GTL+ I/O
A44	D#[45]	GTL+ I/O	B44	D#[44]	GTL+ I/O
A45	D#[39]	GTL+ I/O	B45	VCC_CORE	CPU Core VCC
A46	GND	VSS	B46	D#[36]	GTL+ I/O
A47	Reserved	Reserved	B47	D#[40]	GTL+ I/O
A48	D#[43]	GTL+ I/O	B48	D#[34]	GTL+ I/O
A49	D#[37]	GTL+ I/O	B49	VCC_CORE	CPU Core VCC
A50	GND	VSS	B50	D#[38]	GTL+ I/O
A51	D#[33]	GTL+ I/O	B51	D#[32]	GTL+ I/O
A52	D#[35]	GTL+ I/O	B52	D#[28]	GTL+ I/O
A53	D#[31]	GTL+ I/O	B53	VCC_CORE	CPU Core VCC
A54	GND	VSS	B54	D#[29]	GTL+ I/O
A55	D#[30]	GTL+ I/O	B55	D#[26]	GTL+ I/O
A56	D#[27]	GTL+ I/O	B56	D#[25]	GTL+ I/O
A57	D#[24]	GTL+ I/O	B57	VCC_CORE	CPU Core VCC
A58	GND	VSS	B58	D#[22]	GTL+ I/O
A59	D#[23]	GTL+ I/O	B59	D#[19]	GTL+ I/O
A60	D#[21]	GTL+ I/O	B60	D#[18]	GTL+ I/O
A61	D#[16]	GTL+ I/O	B61	EMI	EMI Management
A62	GND	VSS	B62	D#[20]	GTL+ I/O
A63	D#[13]	GTL+ I/O	B63	D#[17]	GTL+ I/O
A64	D#[11]	GTL+ I/O	B64	D#[15]	GTL+ I/O
A65	D#[10]	GTL+ I/O	B65	VCC_CORE	CPU Core VCC
A66	GND	VSS	B66	D#[12]	GTL+ I/O
A67	D#[14]	GTL+ I/O	B67	D#[7]	GTL+ I/O
A68	D#[9]	GTL+ I/O	B68	D#[6]	GTL+ I/O
A69	D#[8]	GTL+ I/O	B69	VCC_CORE	CPU Core VCC
A70	GND	VSS	B70	D#[4]	GTL+ I/O
A71	D#[5]	GTL+ I/O	B71	D#[2]	GTL+ I/O
A72	D#[3]	GTL+ I/O	B72	D#[0]	GTL+ I/O
A73	D#[1]	GTL+ I/O	B73	VCC_CORE	CPU Core VCC
A74	GND	VSS	B74	RESET#	GTL+ Input
A75	BCLK	CPU Clock	B75	BRT#	GTL+ Input

Table 2- 1 Pentium II Processor Card Edge Signal List (by Pin Number List)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A76	BR0#	GTL+ I/O	B76	FRCERR#	GTL+ I/O
A77	BERR#	GTL+ I/O	B77	VCC_CORE	CPU Core VCC
A78	GND	VSS	B78	A#[35]	GTL+ I/O
A79	A#[33]	GTL+ I/O	B79	A#[32]	GTL+ I/O
A80	A#[34]	GTL+ I/O	B80	A#[29]	GTL+ I/O
A81	A#[30]	GTL+ I/O	B81	EMI	EMI Management
A82	GND	VSS	B82	A#[26]	GTL+ I/O
A83	A#[31]	GTL+ I/O	B83	A#[24]	GTL+ I/O
A84	A#[27]	GTL+ I/O	B84	A#[28]	GTL+ I/O
A85	A#[22]	GTL+ I/O	B85	VCC_CORE	CPU Core VCC
A86	GND	VSS	B86	A#[20]	GTL+ I/O
A87	A#[23]	GTL+ I/O	B87	A#[21]	GTL+ I/O
A88	Reserved	Reserved	B88	A#[25]	GTL+ I/O
A89	A#[19]	GTL+ I/O	B89	VCC_CORE	CPU Core VCC
A90	GND	VSS	B90	A#[15]	GTL+ I/O
A91	A#[18]	GTL+ I/O	B91	A#[17]	GTL+ I/O
A92	A#[16]	GTL+ I/O	B92	A#[11]	GTL+ I/O
A93	A#[13]	GTL+ I/O	B93	VCC_CORE	CPU Core VCC
A94	GND	VSS	B94	A#[12]	GTL+ I/O
A95	A#[14]	GTL+ I/O	B95	A#[8]	GTL+ I/O
A96	A#[10]	GTL+ I/O	B96	A#[7]	GTL+ I/O
A97	A#[5]	GTL+ I/O	B97	VCC_CORE	CPU Core VCC
A98	GND	VSS	B98	A#[3]	GTL+ I/O
A99	A#[9]	GTL+ I/O	B99	A#[6]	GTL+ I/O
A100	A#[4]	GTL+ I/O	B100	EMI	EMI Management
A101	BNR#	GTL+ I/O	B101	SLOTOCC#	Slot Occupied
A102	GND	VSS	B102	REQ#[0]	GTL+ I/O
A103	BPRI#	GTL+ Input	B103	REQ#[1]	GTL+ I/O
A104	TRDY#	GTL+ Input	B104	REQ#[4]	GTL+ I/O
A105	DEFER#	GTL+ Input	B105	VCC_CORE	CPU Core VCC
A106	GND	VSS	B106	LOCK#	GTL+ I/O
A107	REQ#[2]	GTL+ I/O	B107	DRDY#	GTL+ I/O
A108	REQ#[3]	GTL+ I/O	B108	RS#[0]	GTL+ Input
A109	HITM#	GTL+ I/O	B109	VCC5	Other VCC
A110	GND	VSS	B110	HIT#	GTL+ I/O
A111	DBSY#	GTL+ I/O	B111	RS#[2]	GTL+ Input
A112	RS#[1]	GTL+ Input	B112	Reserved	Reserved
A113	Reserved	Reserved	B113	VCC_L2	Other VCC
A114	GND	VSS	B114	RP#	GTL+ I/O

Table 2- 1 Pentium II Processor Card Edge Signal List (by Pin Number List)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A115	ADS#	GTL+ I/O	B115	RSP#	GTL+ Input
A116	Reserved	Reserved	B116	AP#[1]	GTL+ I/O
A117	AP#[0]	GTL+ I/O	B117	VCC_L2	Other VCC
A118	GND	VSS	B118	AERR#	GTL+ I/O
A119	VID[2]	Voltage Identification	B119	VID[3]	Voltage Identification
A120	VID[1]	Voltage Identification	B120	VID[0]	Voltage Identification
A121	VID[4]	Voltage Identification	B121	VCC_L2	Other VCC

Table 2- 1 Pentium II Processor Card Edge Signal List (by Pin Name List)

Pin Name	Pin No.	Signal Buffer Type	Pin Name	Pin No.	Signal Buffer Type
100/66#	B21	BCLK Frequency Select	A#[21]	B87	GTL+ I/O
A#[3]	B98	GTL+ I/O	A#[22]	A85	GTL+ I/O
A#[4]	A100	GTL+ I/O	A#[23]	A87	GTL+ I/O
A#[5]	A97	GTL+ I/O	A#[24]	B83	GTL+ I/O
A#[6]	B99	GTL+ I/O	A#[25]	B88	GTL+ I/O
A#[7]	B96	GTL+ I/O	A#[26]	B82	GTL+ I/O
A#[8]	B95	GTL+ I/O	A#[27]	A84	GTL+ I/O
A#[9]	A99	GTL+ I/O	A#[28]	B84	GTL+ I/O
A#[10]	A96	GTL+ I/O	A#[29]	B80	GTL+ I/O
A#[11]	B92	GTL+ I/O	A#[30]	A81	GTL+ I/O
A#[12]	B94	GTL+ I/O	A#[31]	A83	GTL+ I/O
A#[13]	A93	GTL+ I/O	A#[32]	B79	GTL+ I/O
A#[14]	A95	GTL+ I/O	A#[33]	A79	GTL+ I/O
A#[15]	B90	GTL+ I/O	A#[34]	A80	GTL+ I/O
A#[16]	A92	GTL+ I/O	A#[35]	B78	GTL+ I/O
A#[17]	B91	GTL+ I/O	A20M#	A5	CMOS Input
A#[18]	A91	GTL+ I/O	ADS#	A115	GTL+ I/O
A#[19]	A89	GTL+ I/O	AERR#	B118	GTL+ I/O
A#[20]	B86	GTL+ I/O	AP#[0]	A117	GTL+ I/O

Table 2- 1 Pentium II Processor Card Edge Signal List (by Pin Name List)

Pin Name	Pin No.	Signal Buffer Type	Pin Name	Pin No.	Signal Buffer Type
AP#[1]	B116	GTL+ I/O	D#[26]	B55	GTL+ I/O
BCLK	A75	CPU Clock	D#[27]	A56	GTL+ I/O
BERR#	A77	GTL+ I/O	D#[28]	B52	GTL+ I/O
BINIT#	A24	GTL+ I/O	D#[29]	B54	GTL+ I/O
BNR#	A101	GTL+ I/O	D#[30]	A55	GTL+ I/O
BP#[2]	B19	GTL+ I/O	D#[31]	A53	GTL+ I/O
BP#[3]	A21	GTL+ I/O	D#[32]	B51	GTL+ I/O
BPM#[0]	A23	GTL+ I/O	D#[33]	A51	GTL+ I/O
BPM#[1]	B24	GTL+ I/O	D#[34]	B48	GTL+ I/O
BPRI#	A103	GTL+ Input	D#[35]	A52	GTL+ I/O
BR0#	A76	GTL+ I/O	D#[36]	B46	GTL+ I/O
BR1#	B75	GTL+ Input	D#[37]	A49	GTL+ I/O
D#[0]	B72	GTL+ I/O	D#[38]	B50	GTL+ I/O
D#[1]	A73	GTL+ I/O	D#[39]	A45	GTL+ I/O
D#[2]	B71	GTL+ I/O	D#[40]	B47	GTL+ I/O
D#[3]	A72	GTL+ I/O	D#[41]	B42	GTL+ I/O
D#[4]	B70	GTL+ I/O	D#[42]	A43	GTL+ I/O
D#[5]	A71	GTL+ I/O	D#[43]	A48	GTL+ I/O
D#[6]	B68	GTL+ I/O	D#[44]	B44	GTL+ I/O
D#[7]	B67	GTL+ I/O	D#[45]	A44	GTL+ I/O
D#[8]	A69	GTL+ I/O	D#[46]	A39	GTL+ I/O
D#[9]	A68	GTL+ I/O	D#[47]	B43	GTL+ I/O
D#[10]	A65	GTL+ I/O	D#[48]	B39	GTL+ I/O
D#[11]	A64	GTL+ I/O	D#[49]	A40	GTL+ I/O
D#[12]	B66	GTL+ I/O	D#[50]	B35	GTL+ I/O
D#[13]	A63	GTL+ I/O	D#[51]	A41	GTL+ I/O
D#[14]	A67	GTL+ I/O	D#[52]	B40	GTL+ I/O
D#[15]	B64	GTL+ I/O	D#[53]	A36	GTL+ I/O
D#[16]	A61	GTL+ I/O	D#[54]	B36	GTL+ I/O
D#[17]	B63	GTL+ I/O	D#[55]	A33	GTL+ I/O
D#[18]	B60	GTL+ I/O	D#[56]	B34	GTL+ I/O
D#[19]	B59	GTL+ I/O	D#[57]	A37	GTL+ I/O
D#[20]	B62	GTL+ I/O	D#[58]	B31	GTL+ I/O
D#[21]	A60	GTL+ I/O	D#[59]	B38	GTL+ I/O
D#[22]	B58	GTL+ I/O	D#[60]	A35	GTL+ I/O
D#[23]	A59	GTL+ I/O	D#[61]	A32	GTL+ I/O
D#[24]	A57	GTL+ I/O	D#[62]	B30	GTL+ I/O
D#[25]	B56	GTL+ I/O	D#[63]	B32	GTL+ I/O

Table 2- 1 Pentium II Processor Card Edge Signal List (by Pin Name List)

Pin Name	Pin No.	Signal Buffer Type	Pin Name	Pin No.	Signal Buffer Type
DBSY#	A111	GTL+ I/O	GND	A74	VSS
DEFER#	A105	GTL+ Input	GND	A78	VSS
DEP#[0]	A25	GTL+ I/O	GND	A82	VSS
DEP#[1]	A27	GTL+ I/O	GND	A86	VSS
DEP#[2]	B26	GTL+ I/O	GND	A90	VSS
DEP#[3]	A28	GTL+ I/O	GND	A94	VSS
DEP#[4]	B27	GTL+ I/O	GND	A98	VSS
DEP#[5]	A29	GTL+ I/O	GND	A102	VSS
DEP#[6]	A31	GTL+ I/O	GND	A106	VSS
DEP#[7]	B28	GTL+ I/O	GND	A110	VSS
DRDY#	B107	GTL+ I/O	GND	A114	VSS
EMI	B1	EMI Management	GND	A118	VSS
EMI	B41	EMI Management	HIT#	B110	GTL+ I/O
EMI	B61	EMI Management	HITM#	A109	GTL+ I/O
EMI	B81	EMI Management	IERR#	A4	CMOS Output
EMI	B100	EMI Management	IGNNE#	A8	CMOS Input
FERR#	A7	CMOS Output	INIT#	B4	CMOS Input
FLUSH#	B2	CMOS Input	LINT[0]/INTR	A17	CMOS Input
FRCERR#	B76	GTL+ I/O	LINT[0]/NMI	B16	CMOS Input
GND	A2	VSS	LOCK#	B106	GTL+ I/O
GND	A6	VSS	PICCLK	B18	APIC Clock Input
GND	A10	VSS	PICD[0]	A19	CMOS I/O
GND	A14	VSS	PICD[1]	B22	CMOS I/O
GND	A18	VSS	PRDY#	B23	GTL+ Output
GND	A22	VSS	PREQ#	A20	CMOS Input
GND	A26	VSS	PWRGOOD	A12	CMOS Input
GND	A30	VSS	REQ#[0]	B102	GTL+ I/O
GND	A34	VSS	REQ#[1]	B103	GTL+ I/O
GND	A38	VSS	REQ#[2]	A107	GTL+ I/O
GND	A42	VSS	REQ#[3]	A108	GTL+ I/O
GND	A46	VSS	REQ#[4]	B104	GTL+ I/O
GND	A50	VSS	Reserved	A16	Reserved for Future Use
GND	A54	VSS	Reserved	A47	Reserved for Future Use
GND	A58	VSS	Reserved	A88	Reserved for Future Use
GND	A62	VSS	Reserved	A113	Reserved for Future Use
GND	A66	VSS	Reserved	A116	Reserved for Future Use
GND	A70	VSS	Reserved	B12	Reserved for Future Use

Table 2- 1 Pentium II Processor Card Edge Signal List (by Pin Name List)

Pin Name	Pin No.	Signal Buffer Type	Pin Name	Pin No.	Signal Buffer Type
Reserved	B20	Reserved for Future Use	VCC_CORE	B37	CPU Core VCC
Reserved	B112	Reserved for Future Use	VCC_CORE	B45	CPU Core VCC
RESET#	B74	GTL+ Input	VCC_CORE	B49	CPU Core VCC
RP#	B114	GTL+ I/O	VCC_CORE	B53	CPU Core VCC
RS#[0]	B108	GTL+ Input	VCC_CORE	B57	CPU Core VCC
RS#[1]	A112	GTL+ Input	VCC_CORE	B65	CPU Core VCC
RS#[2]	B111	GTL+ Input	VCC_CORE	B69	CPU Core VCC
RSP#	B115	GTL+ Input	VCC_CORE	B73	CPU Core VCC
SLOTOCC#	B101	Slot Occupied	VCC_CORE	B77	CPU Core VCC
SLP#	B8	CMOS Input	VCC_CORE	B85	CPU Core VCC
SMI#	B3	CMOS Input	VCC_CORE	B89	CPU Core VCC
STPCLK#	B6	CMOS Input	VCC_CORE	B93	CPU Core VCC
TCK	B7	JTAG Input	VCC_CORE	B97	CPU Core VCC
TDI	A9	JTAG Input	VCC_CORE	B105	CPU Core VCC
TDO	A11	JTAG Output	VCC_L2	B113	Other VCC
TESTHI	A13	CMOS Test Input	VCC_L2	B117	Other VCC
THERMTRIP#	A15	CMOS Output	VCC_L2	B121	Other VCC
THRMDN	B15	Thermal Diode N Junction(-)	VCC_VTT	A1	GTL+VTT Supply
THRMDP	B14	Thermal Diode P Junction(+)	VCC_VTT	A3	GTL+VTT Supply
TMS	B10	JTAG Input	VCC_VTT	B5	GTL+VTT Supply
TRDY#	A104	GTL+ Input	VCC_VTT	B9	GTL+VTT Supply
TRST#	B11	JTAG Input	VCC5	B109	Other VCC
VCC_CORE	B13	CPU Core VCC	VID[0]	B120	Voltage Identification
VCC_CORE	B17	CPU Core VCC	VID[1]	A120	Voltage Identification
VCC_CORE	B25	CPU Core VCC	VID[2]	A119	Voltage Identification
VCC_CORE	B29	CPU Core VCC	VID[3]	B119	Voltage Identification
VCC_CORE	B33	CPU Core VCC	VID[4]	A121	Voltage Identification

2.2 Intel 440FX PCIsets (82441FX and 82442FX)

The Intel 440FX PCIset is composed of 82441FX, the PCI and memory controller (PMC), and 82442FX, the data bus accelerator (DBX).

The 440FX PClset consists of a host-to-PCI bridge and memory controller, and an I/O subsystem core that allows an optimized price/performance path for the next generation of personal computers based on the Pentium II Processor. The host-to-PCI bridge consists of two components; the PCI bridge/memory controller (PMC) and the data bus accelerator (DBX). The PMC and the DBX include the following functions.

- Support for single and two Pentium II processors at bus frequencies up to 66 MHz
- 64-bit GTL+ based host bus data interface
- 32-bit host address support
- 32-bit PCI bus interface
- 64/72-bit main memory interface
- Extensive data buffering between all interfaces for high throughput and concurrent operations

The PMC and the DBX interface with the Pentium II processor host bus. A maximum of two Pentium II processors are supported on the Pentium II host bus in a two processor symmetrical multiprocessing configuration. A 16-bit private data bus PD[15:03] operating at host frequency between the DBX and the PMC provides a high throughput indirect interface between the DBX and PCI bus.

The PMC and the DBX host bus interfaces are designed based on the GTL+ specification. The PMC and DBX also provide a 5.0V tolerant 3.3V main memory interface that allows support of either 5V or 3V DRAMs. The PMC connects directly to the 5V PCI bus. The PMC includes an internal PCI arbiter, the PIIX3. The PIIX3 provides the PCI-to-ISA bridge functions along with the universal serial bus (USB) support. The PIIX3 also includes a local bus master IDE interface and an interface for the I/O APIC component required to support a second Pentium II processor. The PIIX3 is compliant to the PCI Rev. 2.1 specification.

Host Interface

The PMC provides bus control signals and address paths for transfers between the host bus, PCI bus, and main memory. It also supports an optimized in-order queue that allows for pipelining of outstanding transaction requests on the host bus. During host-to-PCI cycles, the PMC controls the PCI protocol and data flows through the DBX and PMC via the 16-bit private data (PD) bus. The PD operates at the host bus clock frequency.

The PMC also receives addresses from PCI bus initiators for PCI-to-DRAM transfers. It then translates these addresses to the appropriate memory addresses and provide them to the host bus for snoop cycles. The PMC sends PCI master cycles to the main memory with data moving over the PD bus to the DBX, which subsequently forwards the data to the DRAM.

DRAM Interface

The PMC integrates a main memory controller that supports a 64/72-bit DRAM interface. The PMC DRAM controller interface supports the following features:

- DRAM type: Standard fast page mode (FPM), extended data output (EDO), sometimes referred to as Hyper Page mode, and burst EDO (BEDO) memory
- Memory size: 8 MB to 1 GB with eight RAS lines available
- Addressing type: Symmetrical and asymmetrical addressing
- Memory modules supported: Single- and double-density DIMMs
- DRAM device technology: 4 Mbit, 16 Mbit, and 64 Mbit
- DRAM speeds: 50, 60, and 70 ns

The memory controller supports auto-detection capability for BEDO/EDO/FPM DRAM type installed in the system during the system configuration and initialization. This provides a Plug-and-Play DRAM interface to the user. The PMC/DBX also supports data integrity features including ECC in the memory array and parity error detection. During host and PCI reads of the DRAM, the DBX provides error checking and data correction. The DBX supports multiple-bit error detection and single-bit error correction when the ECC mode is enabled, and parity error detection when parity mode is enabled. During host or PCI master writes to the DRAM, the DBX generates ECC/Parity for the data.

DBX

A single DBX creates the data path for the 64-bit CPU to the main memory. The DBX also interfaces with the 16-bit private data bus for PCI transactions and PMC configuration register set access. The private bus operating at host frequency provides enough throughput to sustain the PCI bandwidth. The DBX allows for a cost-effective solution providing optimal CPU-to-DRAM performance while maintaining a relatively small footprint (208 pins).

PCI Interface

The PCI interface is 5V rev. 2.1 compliant and supports up to five PCI bus masters in addition to the PIIX3 components. The PMC supports a “divide-by-2” synchronous PCI coupling to the host bus frequency.

I/O APIC

I/O APIC supports dual processors as well as enhanced interrupt processing in a single processor environment. No special interface is required on the PMC in this case. The PMC furnishes an external status output signal to the standalone I/O APIC component that deals with buffer flushing during synchronization events for the PIIX3.

2.2.1 Features

- Supports Pentium II processors at bus frequencies up to 66 MHz
  - Supports 32 bit addressing
  - Optimized in-order and request queue
  - Full symmetric multiprocessor (SMP) protocol for up to two processors
  - Dynamic deferred transaction support
  - GTL+ compliant host bus
  - Supports USWC cycles
- Integrated DRAM controller
  - 8 MB to 1 GB main memory
  - 64/72-bit non-interleaved path to memory
  - FPM (fast page mode), EDO (extended data out page mode), BEDO (extended data out burst mode) DRAMs providing x-222 to x-44 4 burst capability
  - Supports auto-detection of memory type: BEDO, EDO or FPM
  - 8 RAS lines available
  - Support for 4-,16- and 64-Mbit DRAM devices
  - Support for symmetrical and asymmetrical DRAM addressing
  - Configurable support for ECC or parity
  - ECC with single-bit error correction and multiple-bit error detection
  - Read-around-write support for host and PCI DRAM read accesses
  - Supports 3.3V or 5V DRAMs
- PCI bus interface
  - PCI rev. 2.1, 5V interface compliant
  - Greater than 100 Mbps data streaming for PCI to DRAM accesses enables Native Signal Processing (NSP) on systems designed with the Pentium II processor
  - Integrated arbiter with multi-transaction PCI arbitration accelerator hooks
  - Five PCI bus masters are supported in addition to the host and PCI-to-ISA I/O bridge
  - Delayed transaction support
  - PCI parity checking and generation support
  - Supports concurrent Pentium II and PCI transactions to main memory

- Data buffering for increased performance
  - Extensive CPU-to-DRAM and PCI-to-DRAM write data buffering
  - Write combining support for CPU-to-PCI burst writes
- System Management Mode (SMM) compliant
- 208-pin PQFP PCI Bridge/Memory Controller (PMC), 208-pin PQFP for the 440FX PCIset data bus accelerator (DBX)

2.2.2 Block Diagrams

2.2.2.1 PMC

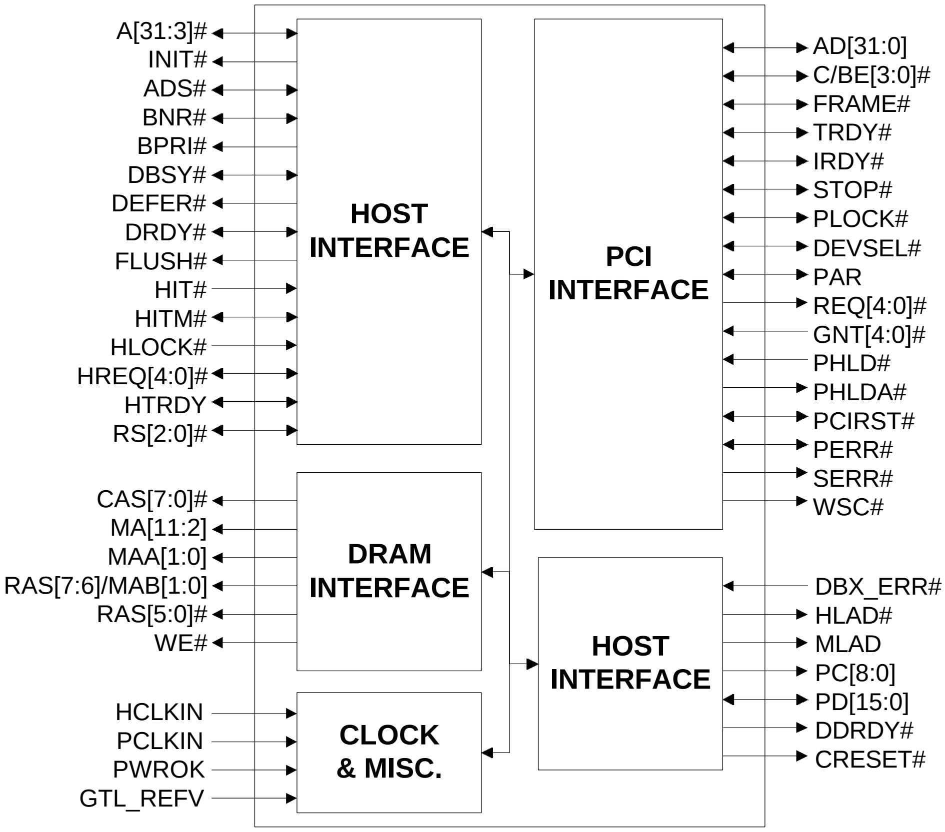


Figure 2- 3 82441FX (PMC) Block Diagram

2.2.2.2 DBX

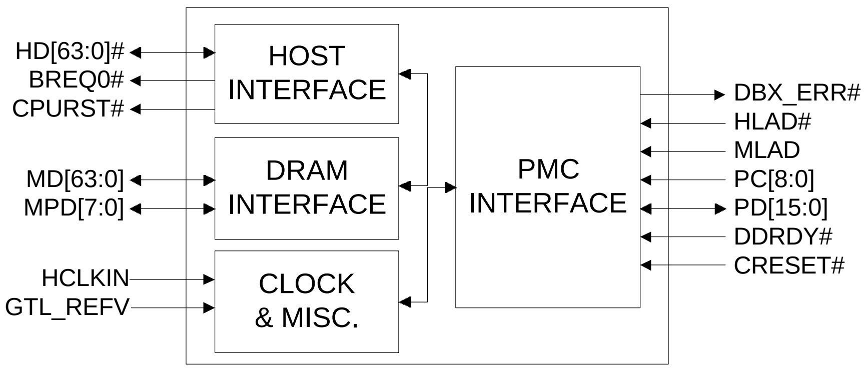


Figure 2- 4 82442FX (DBX) Block Diagram

2.2.3 Pin Diagrams

2.2.3.1 PMC

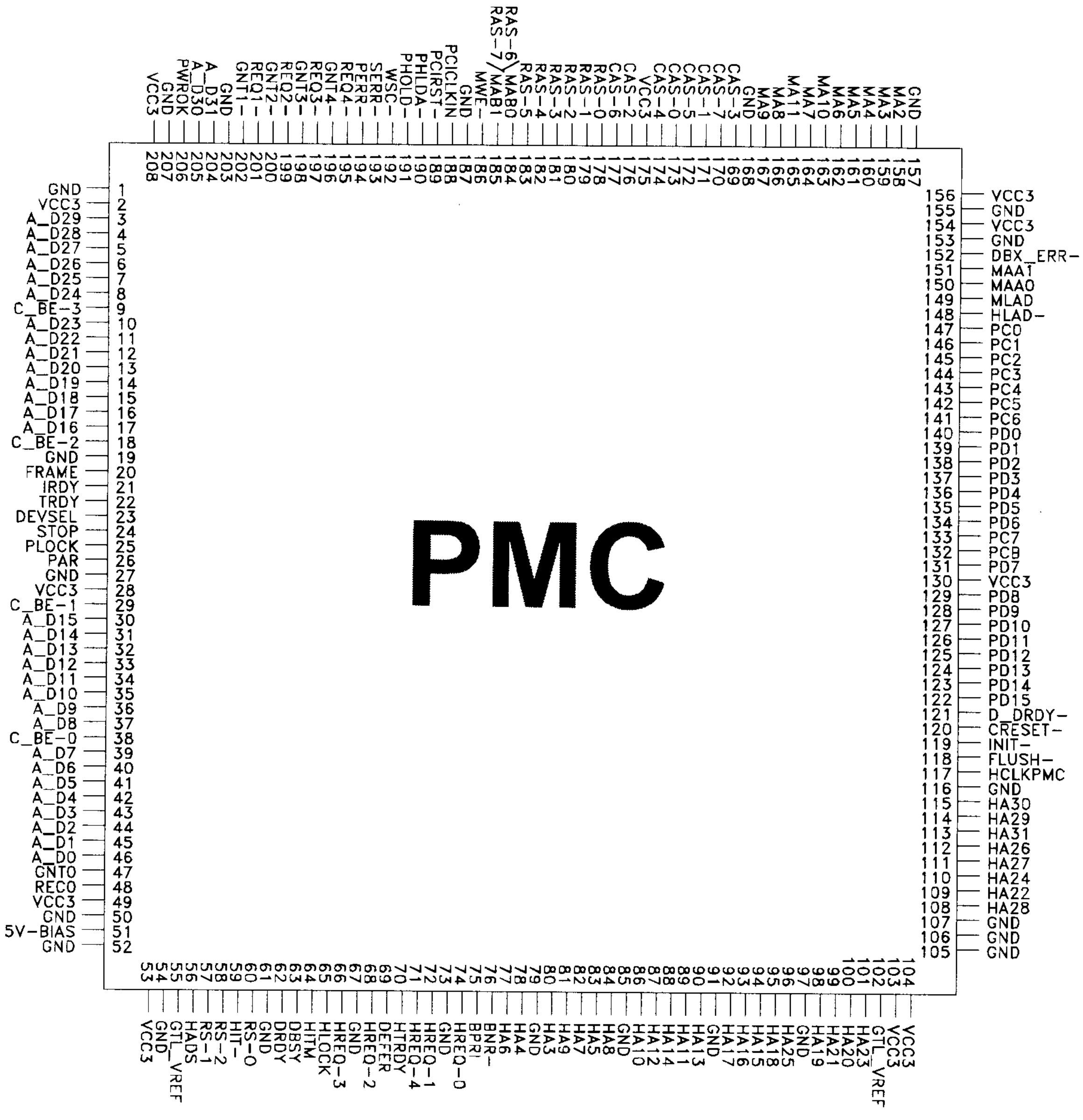


Figure 2- 5 82441FX (PMC) Pin Diagram

2.2.3.2 DBX

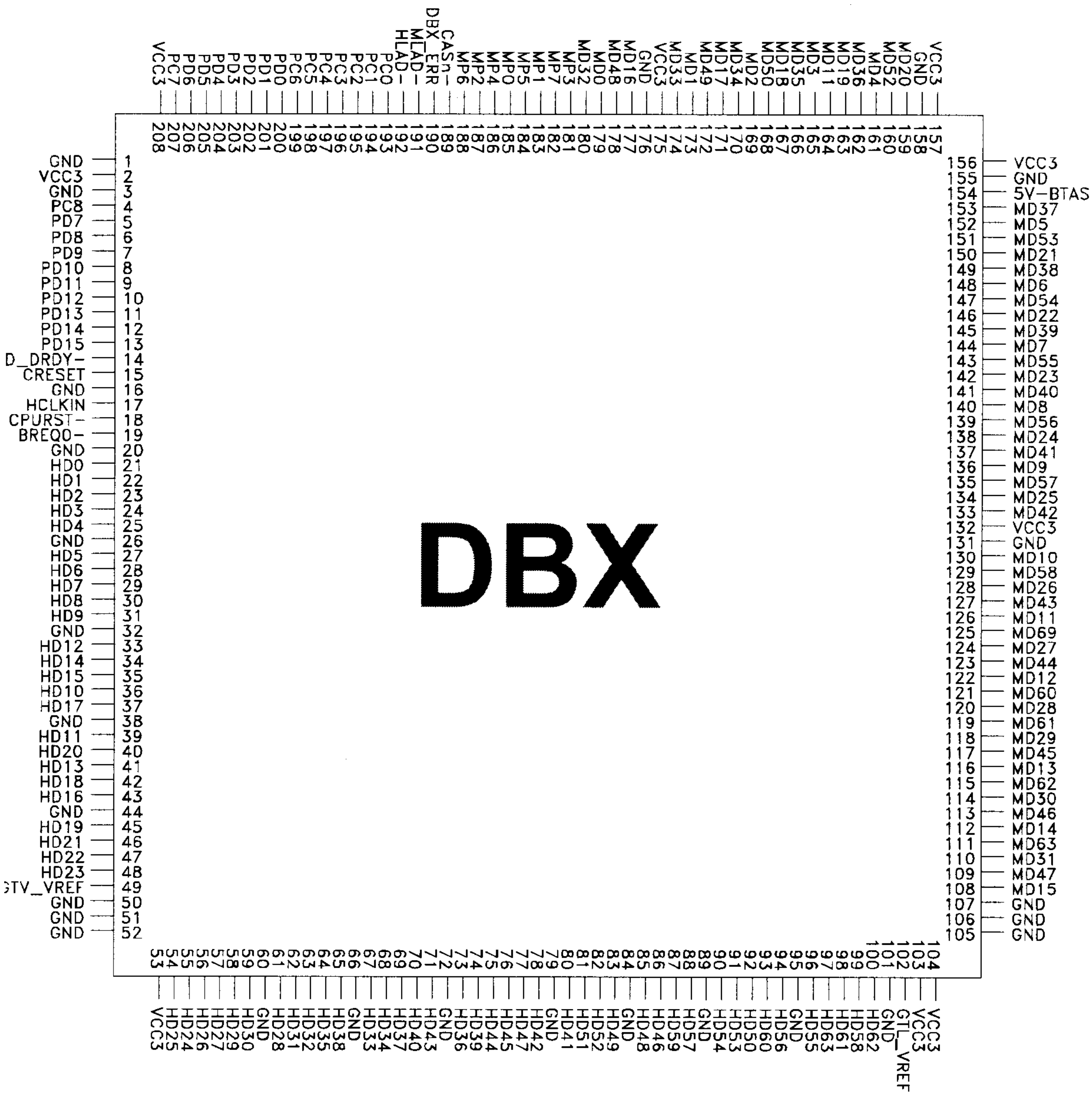


Figure 2- 6 82441FX (DBX) Pin Diagram

2.2.4 Signal Descriptions

The "#" symbol at the end of a signal indicates that the active, or asserted state, occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted at a high-voltage level.

The following notations describe the signal type:

Table 2- 2 82440FX PCIset Signal Type Descriptions

Signal Type	Descriptions
I	Input pin
O	Output pin
OD	Open drain output pin. This requires a pull-up to the VCC of the processor core.
I/O	Bidirectional input/output pin

The signal description also includes the type of buffer used for the particular signal:

Table 2- 3 82440FX PCIset Buffer Types Descriptions

Buffer Type	Descriptions
GTL+	Open Drain GTL+ interface signal. Refer to the GTL+ I/O specification for complete details.
PCI	PCI bus interface signals. These signals are compliant with the PCI 5.0V signaling environment DC and AC specifications
LVTTL	Low Voltage TTL compatible signals. These are also 3.3V outputs with 5V tolerant inputs.

2.2.4.1 PMC Signal Descriptions

Table 2- 4 82441FX (PMC) Signal Descriptions

Signal	Pin	Type	Description
Host Interface			
INIT#	119	O, LVTTL	**Initialization.** This is the soft reset output pin generated by the PMC during a CPU shutdown bus cycle, or after the writing to the reset control register to initiate a soft reset.
A[31:3]#	113, 115, 114, 108, 111, 112, 96, 110, 101, 109, 99, 100, 98, 95, 92, 93, 94, 88, 90, 87, 89, 86, 81, 84, 82, 77, 83, 78, 80	I/O, GTL+	**Address Bus.** A[31:3]# connects to the CPU address bus. During CPU cycles the A[31:3]# are inputs. The PMC drives A[31:3]# during snoop cycles on behalf of PCI initiators. Note that the CPU address bus is an inverted bus.
ADS#	56	I/O, GTL+	**Address Strobe.** The CPU bus owner asserts ADS# to indicate the first of two cycles of a request phase.
BNR#	76	O, GTL+	**Block Next Request.** Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the CPU bus pipeline depth.
BPRI#	75	O, GTL+	**Priority Agent Bus Request.** The owner of this signal is always the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted. The PMC drives this signal to gain control of the CPU bus.
DBSY#	63	I/O, GTL+	**Data Bus Busy.** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	69	O, GTL+	**Defer.** The PMC uses a dynamic deferring policy to optimize system performance. The PMC also uses the DEFER# signal to indicate a CPU retry response.
DRDY#	62	I/O, GTL+	**Data Ready.** Asserted for each cycle that data is transferred.
FLUSH#	118	OD, GTL+	**Flush.** Issued to CPU(s) for L1/L2 cache to do a write back of all cache lines in modified state then invalidate all cache lines. This signal is asserted by the PMC to throttle the CPU bus in the de-turbo mode of operation.
HIT#	59	I/O, GTL+	**HIT#.** Indicates that a caching agent holds an unmodified version or the requested line, and driven in conjunction with HITM# by the target to extend the snoop window.

Table 2- 4   82441FX (PMC) Signal Descriptions

Signal	Pin	Type	Description
Host Interface			
HITM#	64	I/O, GTL+	**Hit Modified.** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. This is driven in conjunction with HIT# to extend the snoop window.
HLOCK#	65	I, GTL+	**Host Lock.** All CPU bus cycles sampled with the assertion of HLOCK# and ADS# must be atomic until the negation of HLOCK#. This means that no PCI activity to DRAM is allowed and the locked cycle must be translated to PCI if targeted for the PCI bus.
HREQ[4:0]#	71, 66, 68, 72, 74	I/O, GTL+	**Request Command.** This is asserted during both clocks of the request phase. In the first clock, the signals define the transaction type in details sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type.
HTRDY#	70	I/O, GTL+	**Host Target Ready.** Indicates that the target of the CPU transaction is able to enter the data transfer phase.
RS[2:0]#	58, 57, 60	I/O, GTL+	**Response Signals.** Indicates the type of response following the table below: **RS[2:0]** **Response Type** 000 Idle state 001 Retry response 010 Defer response 011 Reserved 100 Hard failure 101 Normal without data 110 Implicit write back 111 Normal with data
DRAM Interface			
CAS[7:0]#	170, 177, 172, 174, 169, 171, 173	O, LVTTL	**Column Address Strobe.** The CAS[7:0]# signals are used to latch the column address on the MA[11:0] lines into the DRAMs. These are active low signals that drive the DRAM array directly without external buffering. CAS3# supports BEDO DRAM as connection to the CASn# signal on the DBX. When this signal connects to DBX, the drive strength should be increased to 16 mA by correctly programming the MBSC register.
MA[11 :2]	165, 163, 167, 166, 164, 162, 161, 160, 159, 158	O, LVTTL	**Memory Address.** MA[11:2] provides multiplexed row and column address to the DRAM. MA[11:2] are externally buffered to drive the address lines of the DRAM.

Table 2- 4 82441FX (PMC) Signal Descriptions

Signal	Pin	Type	Description
DRAM Interface			
MAA[1 :0]	151, 150	O, LVTTL	**Lower Memory Address Set A.** MAA[1:0] are the lower two bits of the memory address used to complete the row and column address to the DRAM. These two bits are toggled during the burst phase.
RAS[7:0]# / MAB[1:0]	185, 184	O, LVTTL	**Row Address Strobes RAS7# and RAS6# or Lower Memory Address Set B.** MAB[1:0] are the lower two bits of the memory address used to complete the row and column address to the DRAM. These signals are toggled during the burst phase. RAS[7:6]# signals are used to latch the row address on the MA[11:0] lines into the DRAMs. These signals should be used to select the upper two rows in the memory array. These signals drive the DRAM array directly without external buffers. The strapping on PC[8] signal selects the function of these pins.
RAS[5:0]#	183~178	O, LVTTL	**Row Address Strobe.** The RAS[5:0]# signals are used to latch the row address on the MA[11:0] lines into the DRAMs. Each signal is used to select one DRAM row. These signals drive the DRAM array directly without any external buffers.
WE#	186	O, LVTTL	**Write Enable Signal.** WE# is asserted during writes to main memory. During burst writes to main memory, the WE# is externally buffered to drive the WE# inputs of the DRAM.
AD[31:0]	204, 205, 3~8, 10~17, 30~37, 39~46	I/O, PCI	**PCI Address/Data.** These signals connect to the PCI address/data bus. The PMC drives the address with FRAME# assertion and data is driven or received in the following clocks. When the PMC acts as a target on the PCI bus, the AD[31:0] signals are inputs and contain the address during the first clock of FRAME# assertion and data on subsequent clocks.
DEVSEL#	23	I/O, PCI	**Device Select.** Device select, when asserted, indicates that a PCI target device has decoded its address as the target of the current access. The PMC asserts DEVSEL# based on the DRAM address range being accessed by a PCI initiator, or if it decodes the current configuration cycle, it is targeted to the PMC.

Table 2- 4 82441FX (PMC) Signal Descriptions

Signal	Pin	Type	Description
DRAM Interface			
FRAME#	20	I/O, PCI	**Frame.** FRAME# is an output when the PMC acts as an initiator on the PCI bus. FRAME# is asserted by the PMC to indicate the beginning and duration of an access. The PMC asserts FRAME# to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is negated, the transaction is in the final data phase. FRAME# is an input when the PMC acts as a PCI target. As a PCI target, the PMC latches the C/BE[3:0]# and the AD[31:0] signals on the first clock edge on which it samples FRAME# active.
IRDY#	21	I/O, PCI	**Initiator Ready.** IRDY# is an output when PMC acts as a PCI initiator and an input when the PMC acts as a PCI target. The assertion of IRDY# indicates the current PCI bus initiator's ability to complete the current data phase of the transaction.
PLOCK#	25	I/O, PCI	**Plock.** PLOCK# indicates an exclusive bus operation and may require multiple transactions to complete. When PLOCK# is asserted, non-exclusive transactions may proceed. A grant to start a transaction on the PCI bus does not guarantee control of the PLOCK# signal. Control of the PLOCK# signal is obtained under its own protocol in conjunction with the GNT# signal. The PMC supports bus lock mode of operation.
TRDY#	22	I/O, PCI	**Target Ready.** TRDY# is an input when the PMC acts as a PCI initiator and an output when the PMC acts as a PCI target. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction.

Table 2- 4 82441FX (PMC) Signal Descriptions

Signal	Pin	Type	Description
DRAM Interface			
C/BE[3:0]#	9, 18, 29, 38	I/O, PCI	**Command/Byte Enable.** PCI bus command and byte enable signals are multiplexed on the same pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase, C/BE[3:0]# are used as byte enables. The byte enables determine which byte lanes carry meaningful data. The PCI bus command encoding and types follows. **C/BE[3:0]# Command Type** 0000 Interrupt Acknowledge 0001 Special Cycle 0010 I/O Read 0011 I/O Write 0100 Reserved 0101 Reserved 0110 Memory Read 0111 Memory Write 1000 Reserved 1001 Reserved 1010 Configuration Read 1011 Configuration Write 1100 Memory Read Multiple 1101 Reserved (Dual/Address Cycle) 110 Memory Read Line 1111 Memory/Write and invalidate
PAR	26	I/O, PCI	**Parity.** The PMC drives PAR when the former acts as a PCI initiator during address and data phases for a write cycle, and during the address phase for a read cycle. The PMC drives PAR when the former acts as a PCI target during each data phase of a PCI memory read cycle. Even parity is generated across AD[31:0] and C/BE[3:0]#.
PERR#	194	I/O, PCI	**PCI Parity Error.** Pulsed by an agent receiving data with bad parity one clock after PAR is asserted. The PMC generates PERR# active if it detects a parity error on the PCI bus and the PERR# enable bit is set.
SERR#	193	O, PCI	**System Error.** The PMC can be programmed to assert SERR# when the DBX_ERR# signal is sampled active. The DBX_ERR# can be driven active for two types of error conditions: 1. Main memory single-bit ECC error 2. Main memory (DRAM) parity or multiple-bit ECC error The PMC asserts can be programmed to assert SERR# when it detects a target abort on a PMC initiated PCI cycle and when PERR# is sampled active.

Table 2- 4 82441FX (PMC) Signal Descriptions

Signal	Pin	Type	Description
DRAM Interface			
PCIRST#	189	O, PCI	**PCI Reset.** PCI bus reset forces the PCI interfaces of each device to a known state. The PMC generates a minimum 1 ms pulse for PCIRST#.
STOP#	24	I/O, PCI	**Stop.** STOP# is an input when the PMC acts as a PCI initiator and an output when the PMC acts as a PCI target. STOP# indicates that the bus initiator must immediately terminate its current PCI bus cycle at the next clock edge and release control of the PCI bus. STOP# is used to disconnect, retry, or abort sequences on the PCI bus.
PCI Sideband Interface			
PHOLD#	191	I, PCI	**PCI Hold.** This signal comes from the PIIX3. It is the PIIX3 request for PCI.
PHLDA#	190	O, PCI	**PCI Hold Acknowledge.** The PMC drives this signal to grant PCI bus ownership to the PIIX3.
WSC#	192	O, PCI	**Write Snoop Complete.** This signal is asserted active to indicate that all that the snoop activity on the CPU bus on the behalf of the last PCI-DRAM write transaction is complete.
REQ[4:0]#	195, 197, 199, 201, 48	I, PCI	**PCI Bus Request.** REQ[4:0]# are the PCI bus request signals used by the PMC for PCI initiator arbitration.
GNT[4:0]#	196, 198, 200, 202, 47	O, PCI	**PCI Grant.** GNT[4:0]# are the PCI bus grant signals used by the PMC for PCI initiator arbitration.
DBX_ERR#	152	I, PCI	**DBX Error.** The DBX generates this signal if an ECC or parity error occurred during a memory cycle. DBX_ERR# is held low (active) for five host clocks to indicate a single-bit ECC error and six host clocks to indicate a parity or multiple-bit ECC error.
HLAD#	148	O, LVTTL	**Host Latch and Advance.** During CPU reads (both from DRAM and PCI), this signal controls the latching of the read data into the DBX CPU interface output latch.

Table 2- 4 82441FX (PMC) Signal Descriptions

Signal	Pin	Type	Description
PCI Sideband Interface			
MLAD	149	O, LVTTL	**Memory Latch and Advance.** During DRAM reads, asserting this signal latches memory read data into the DBX. During DRAM writes, asserting this signal latches write data out of the DBX.
PC[8:0]	132, 133, 141~147	I/O, LVTTL	**PMC Control Signals.** PC[8:0] are control signals between the PMC and DBX.
PD[15:0]	122~129, 131, 134~140	I/O, LVTTL	**Private Data Bus.** This is a 16-bit private data path between the PMC and DBX. This bus runs at the host clock rate and is used to transfer data during CPU to PCI cycles and PCI to DRAM cycles
DDRDY	121	O, LVTTL	**Delayed Data Ready.** This delayed version of the DRDY# signal is asserted by the PMC to the DBX.
Clock			
HCLKIN	117	I, 2.5V, LVTTL	**Host Clock In.** This pin receives a host clock input from an external clock source. The input is configurable via the PD[1] strap. If the PD[1] is sampled low at reset (default), 3.3V buffer mode is enabled. During normal operation, this is enabled by internal pulldowns. If the PD[1] is sampled high, then the buffer is enabled in 2.5V mode.
PCLKIN	188	I, LVTTL	**PCI Clock In.** This pin receives a PCI clock reference synchronous with respect to the host clock. This is the PCI clock reference that can be synchronously derived by an external clock synthesizer component from the host clock (divide-by-2). This clock is used by all of the PMC logic that is in the PCI clock domain.
Miscellaneous			
CRESET#	120	O, LVTTL	**Chip Reset.** This is a reset output signal driven by the PMC to the DBX. CRESET# is driven active for 2 ms. The CBX drives CPURST# to the CPUs, which is a two-host clock delayed version of the CRESET#. The PMC can also activate CRESET# under software control by writing to the internal reset configuration register to initiate a hard reset or CPU BIST.
GTL_REFV	55, 102	I	**GTL+ Reference Voltage.** This is the reference voltage derived from the termination voltage to the pullup resistors which determine the noise margin for the signals. This signal goes to the reference input of the GTL+ sense amp on each GTL+ input or I/O pin.

Table 2- 4 82441FX (PMC) Signal Descriptions

Signal	Pin	Type	Description
Miscellaneous			
PWROK	206	I, LVTTL	**Power OK.** This input goes active after all the power supplies in the system have reached their specified values. PWROK forces all of the PMC internal state machines to their default values. PWROK inactive generates CPURST# and PCIRST# active. The rising edge of PWROK is asynchronous, but must meet setup and hold specifications for recognition on any specific clock. The PMC holds CPURST# for 2 ms and PCIRST# active for 1 ms after the rising edge of PWROK.
Vcc3	2, 28, 49, 53, 103, 104	–	
Vcc5	130, 154, 156, 175, 208, 51	–	**+5V Power Supply Input**
GND	1, 19, 27, 50, 52, 54, 61, 67, 73, 79, 85, 91, 97, 105, 106, 107, 116, 153, 155, 157, 168, 187, 203, 207	–	**Ground**

2.2.4.2 DBX Signal Descriptions

Table 2- 5 82442FX (DBX) Signal Descriptions

Signal	Pin	Type	Description
DRAM Interface Signals			
MD[63:0]	111, 115, 119, 121, 125, 129, 135, 139, 143, 147, 151, 160, 164, 168, 172, 178, 109, 113, 117, 123, 127, 133, 137, 141, 145, 149, 153, 162, 166, 170, 174, 180, 110, 114, 118, 120, 124, 128, 134, 138, 142, 146, 150, 159, 163, 167, 171, 177, 108, 112, 116, 122, 126, 130, 136, 140, 144, 148, 152, 161, 165, 169, 173, 179	I/O, LVTTL	**Memory Data.** These signals connect to the DRAM data bus. These signals have weak internal pulldowns.
MPD[7:0]	182, 188, 184, 186, 181, 187, 183, 185	I/O, LVTTL	**Memory Parity Data.** These signals connect to the parity or ECC bits or the DRAM data bus. These signals have weak internal pulldowns.
PMC Interface Signals			
DBX_ERR#	190	O, LVTTL	**DBX Error.** DBX_ERR# is generated for ECC or parity errors during a memory read cycle. DBX_ERR# is held low (active) for five host clocks to indicate a single-bit ECC error and six host clocks to indicate a parity or multiple-bit ECC error.
HLAD#	192	I, LVTTL	**Host Latch and Advance Signal.** During CPU reads this signal is used to control the latching read data into the DBX CPU interface output latch (i.e. flip-flop).
MLAD	191	I, LVTTL	**Memory Latch and Advance Signal.** During DRAM reads, asserting this signal latches memory read data into the DBX DRAM interface input latch. During DRAM writes, asserting this signal latches write data out of the DBX DRAM interface output
PC[8:0]	4, 207, 199~193	I, LVTTL	**PMC/DBX Control Signals.** PC[8:0] are control signals between the PMC and DBX.
DDRDY#	14	I, LVTTL	**Delayed Data Ready.** This is a delayed version of DRDY# for the DBX that is asserted by the PMC.

Table 2- 5 82442FX (DBX) Signal Descriptions

Signal	Pin	Type	Description
PMC Interface Signals			
PC[15:0]	13~5, 206~200, 4, 207, 199~193	I/O, LVTTL	**Private Data Bus.** These signals connect to the PD data bus on the PMC. This is the data path for the PCI-DRAM and CPU-PCI cycles. During PCI to DRAM reads and CPU to PCI writes, the DBX drives data onto these pins. During CPU to PCI reads and PCI to DRAM writes, the DBX receives data on this bus.
Host Interface Signals			
HD[63:0]#	97, 100, 98, 93, 87, 99, 88, 94, 96, 90, 91, 82, 81, 92, 83, 85, 77, 86, 76, 75, 71, 78, 80, 70, 74,65, 69, 73, 64, 68, 67, 63, 62, 59, 58, 61, 57, 56, 54, 55, 48, 47, 46, 40, 45, 42, 37, 43, 35, 34, 41, 33, 39, 36, 31, 29, 30, 28, 27, 25, 24, 23, 22, 21	I/O, GTL+	**Host Data.** These signals connect to the CPU data bus. Note that the data signals are inverted on the CPU bus.
CPURST#	18	O, GTL+	**CPU Reset.** The CPURST# pin is an output from the DBX that is driven directly from the CRESET#. It allows the CPUs to begin execution at a known state.
Miscellaneous Signals			
HCLKIN	17	I, 2.5V, LVTTL	**Host Clock In.** This pin receives a host clock input from an external source. The input is configurable via the PD[1] strap. If the PD[1] is sampled low at reset (default), 3.3V buffer mode is enabled. During normal operation, this is enabled by internal pulldowns. If the PD[1] is sampled high, then the buffer is enabled in 2.5V mode.
CRESET#	15	I, LVTTL	**Chip Reset.** This is a reset input signal driven by the PMC to the DBX. It forces the DBX to begin execution in a known state. This signal is also used to drive the CPURST# to the CPUs.
GTL_REFV	102	I	**GTL Reference Voltage.** This is the reference voltage derived from the termination voltage to the pullup resistors and determines the noise margin for the signals. This signal goes the reference input of the GTL+ sense amp on each GTL+ input or I/O pin.

Table 2- 5 82442FX (DBX) Signal Descriptions

Signal	Pin	Type	Description
Miscellaneous Signals			
BREQ0#	19	O, GTL+	**Symmetric Agent Bus Request.** The DBX drives this signal during CPURST# to configure the symmetric bus agents.
Vcc3	2, 53, 103, 104, 132, 156, 157, 175, 208		**+3V Power Supply Input**
Vcc5	154		**+5V Power Supply Input**
GND	1, 3, 16, 20, 26, 32, 38, 44, 50, 51, 52, 60, 66, 72, 79, 84, 89, 95, 101, 105, 106, 107, 131, 155, 158, 176		**Ground**

2.3 Intel 82371SB

2.3.1 Features

- Supports PCI and ISA bus bridge
- PCI and ISA master/slave interface
  - PCI: from 25 - 33 MHz
  - ISA: from 7.5 - 8.33 MHz
  - Four ISA slots
- Fast IDE interface
  - Supports PIO and bus master IDE interface
  - Supports up to Mode 4 timings
  - 22-MB/s transfer rates
  - 8 x 32-bit buffer for bus master IDE PCI burst transfers
  - Separate master/slave IDE mode support
- Plug-and-Play port for motherboard devices
  - Support one steerable interrupt line
  - One programmable chip select
- Steerable PCI interrupts for PCI Plug-and-Play device
- Compliant with PCI specification rev. 2.1
- Single 82C54 functionality
  - System timer
  - Refresh request
  - Speaker tone output
  - Dual 82C59 interrupt controllers functionality
  - Supports 14 interrupts
  - Independently programmable for edge/level sensitivity
- Enhanced DMA functions
  - Two 8237 DMA controllers
  - Fast Type F DMA
  - Compatible DMA transfers
  - Seven independently programmable channels
- X-bus peripheral support
  - Chip-select decode

- Controls the lower X-bus data byte transceiver

- I/O advanced programmable interrupt controller(I/O APIC) support
- Universal Serial Bus (USB) controller
  - Host/Hub controller
  - Two USB ports
- Non-maskable interrupts (NMI)
  - PCI system error reporting
- NAND tree for board-level ATE testing
- 208-pin QFP

2.3.2 Block Diagram

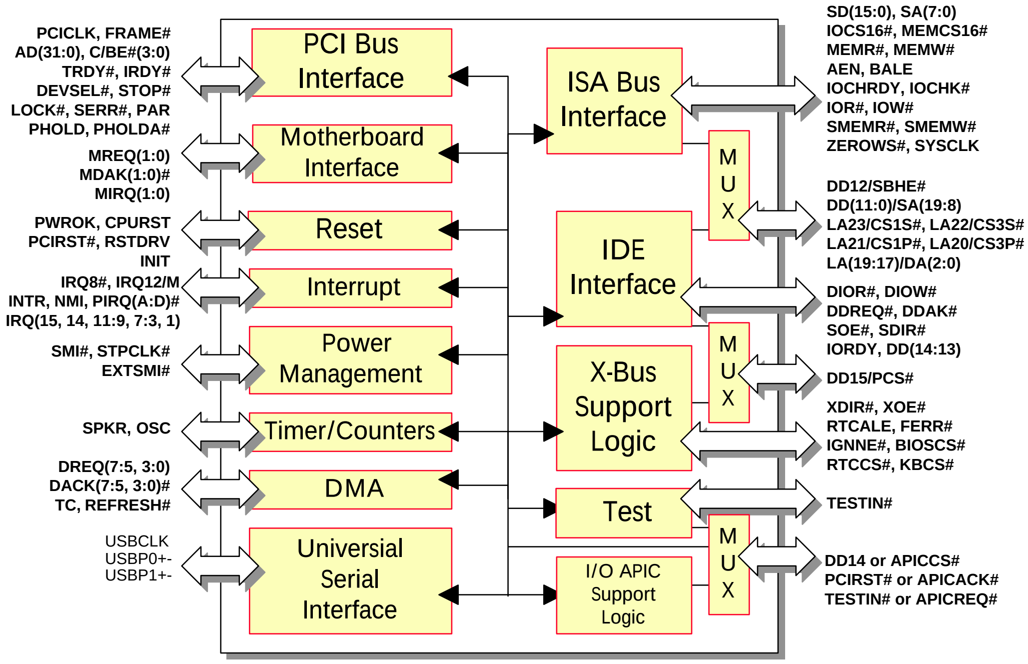


Figure 2- 7 82371SB (PIIX3) Block Diagram

2.3.3 Pin Diagram

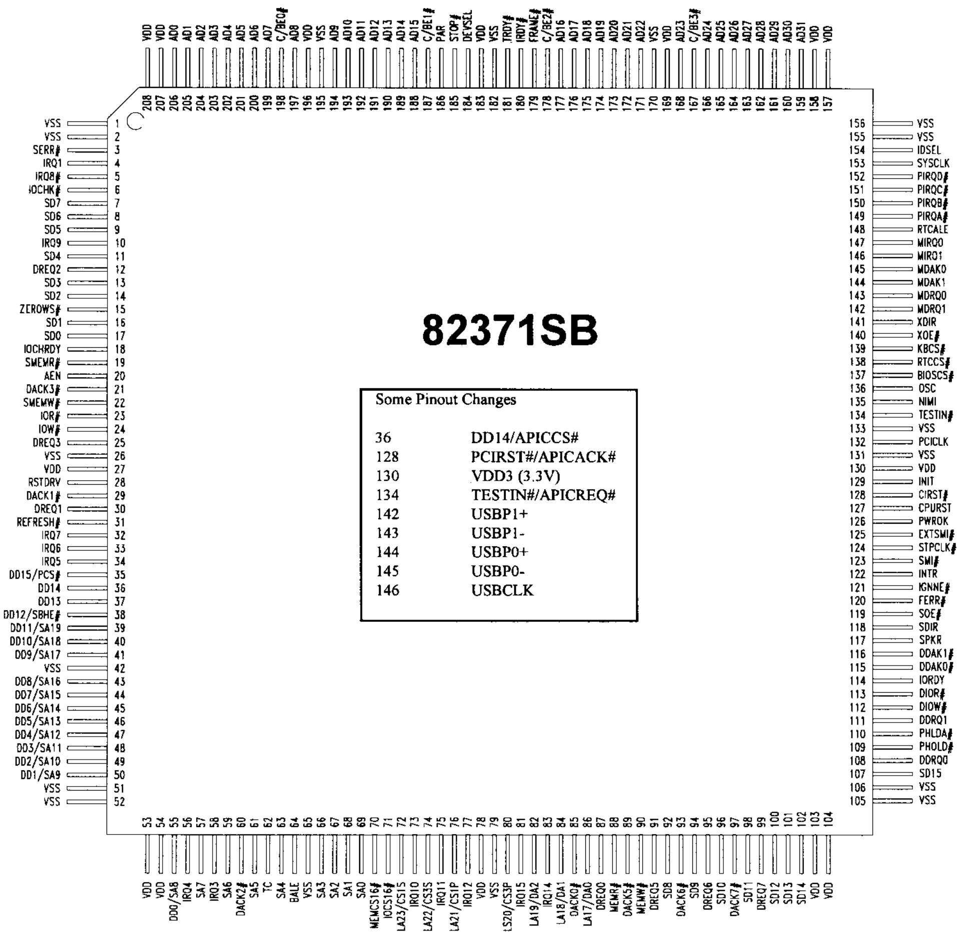


Figure 2- 8 82371SB (PIIX3) Pin Diagram

2.3.4 Signal Descriptions

Table 2- 6 82371SB (PIIX3) Signal Descriptions

Signal	Pin	Type	Description
PCI Interface			
PCICLK	132	I	**PCI Clock.** PCICLK supports timing for all transactions on the PCI bus. All other PCI signals are sampled on the rising edge of the PCICLK, and all timing parameters are defined with respect to this edge. It also supports PCI frequencies of 25-33 MHz.
AD[31:0]	159-166, 168, 171-177, 188-194, 197, 199-206	I/O	**PCI Address/Data.** The standard PCI address and data line. The address is driven with FRAME# assertion and data is driven or received in following clocks.
C/BE[3:0]#	167, 178	I/O	**Bus Command and Byte Enables.** The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on the following clocks.
FRAME#	179	I/O (s/t/s)	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one or more data transfer is desired by the cycle initiator.
TRDY#	181	I/O (s/t/s)	**Target Ready.** Asserted when the target is ready for a data transfer.
IRDY#	180	I/O (s/t/s)	**Initiator Ready.** Asserted when the initiator is ready for a data transfer.
STOP#	185	I/O (s/t/s)	**Stop.** Asserted by the target to request the master to stop the current transaction.
IDSEL	154	I	**Initialization Device Select.** IDSEL is used as a chip select during configuration read and write transactions.
DEVSEL	184	I/O (s/t/s)	**Device Select.** The PIIX asserts DEVSEL# to claim a PCI transaction through positive and subtractive decoding.
PAR	186	O	**Calculated Parity Signal.** PAR is an "even" parity and is calculated on 36 bits – AD[31:0] plus C/BE[3:0]#.
SERR#	3	I	**System Error.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the PIIX can be programmed to generate a non-maskable interrupt (NMI) to the CPU.
PHOLD#	109	O	**PCI Hold.** The chip asserts this signal to request the PCI bus. This chip implements the passive release mechanism by toggling PHOLD# inactive for one PCICLK.
PHLDA#	110	I	**PCI Hold Acknowledge.** This signal is asserted to grant the PCI bus to this chip.

Table 2- 6 82371SB (PIIX3) Signal Descriptions

Signal	Pin	Type	Description
Motherboard I/O Device Interface			
MIRQ0[1:0]	146-147	I	**Motherboard Device Interrupt Request.** The MIRQ signals can be internally connected to the interrupts IRQ[15, 14, 12:9, 7:3]. Each MIRQx line has a separate Route Control register. If MIRQx and PIRQx are steered to the same ISA interrupt, the device connected to the MIRQx should produce active high-level interrupts. If the bus master mode of the IDE interface and the secondary IDE channel is used, the interrupt for that channel must be connected to MIRQ0. If MIRQ is steered to a given IRQ input to the internal 8259, the corresponding ISA IRQ is masked - unless the Route Control register is programmed to allow the interrupts to be shared. This should only be done if the device connected to the MIRQ line and the device connected to the ISA IRQ line both produce active high-level interrupts.
IDE Interface			
DD[15:0]/ PCS#, SBHE#, SA[19:8] APICCS#	35-41, 43-50, 55	I/O O I/O I/O O	**Disk Data.** These signals directly drive the corresponding signals on the two IDE connectors (primary and secondary). In addition, these signals are buffered (using 2xALS245's on the motherboard) to produce the SA[19:8] and PCS# and SBHE# signals. DD14 is buffered to produce APICCS#
DIOR#	113	O	**Disk I/O Read.** This signal directly drives the corresponding signal on the two IDE connectors (primary and secondary).
DIOW#	112	O	**Disk I/O Write.** This signal directly drives the corresponding signal on the two IDE connectors (primary and secondary).
DDRQ[1:0]	111, 108	I	**Disk DMA Request.** These input signals are directly driven from the DRQ signals on the primary (DDRQ0) and secondary (DDRQ1) IDE connectors. They are used in conjunction with the PCI bus master IDE function and are not associated with any ISA-compatible DMA channel.
DDAK[1:0]#	116, 115	O	**Disk DMA Acknowledge.** These signals directly drive the DAK# signals on the primary (DDAK0#) and secondary (DDAK1#) IDE connectors. These signals are used in conjunction with the PCI bus master IDE function and are not associated with any ISA-compatible DMA channel.
IORDY	114	I	**IO Channel Ready.** This input signal is directly driven by the corresponding signal on the two IDE connectors (primary and secondary).

Table 2- 6 82371SB (PIIX3) Signal Descriptions

Signal	Pin	Type	Description
IDE Interface			
SOE#	119	O	**System Address Transceiver Output Enable.** This signal controls the output enables of the '245 transceivers that interface the DD[15:0] signals to the SA[9:8], SBHE# and PCS# signals.
SDIR	118	O	**System Address Transceiver Direction.** This signal controls the direction of the '245 transceivers that interface the DD[15:0] signals to the SA[19:8], SBHE# and PCS# signals. Default condition is high (transmit). When an ISA bus master is granted use of the bus, the transceivers are turned around to drive the ISA address [19:8] on D[D[15:3]. The address can then be latched by the PIIX. In this case, the SDIR signal is low (receive). The SOE# and SDIR signals taken together as a group can assume one of three states: **SOE# SDIR State** 0 1 PCI to ISA transaction 1 1 PCI to IDE 0 0 ISA bus master
Buffered From LA[23:17]			
LA23/ CS1S#	72	I/O	**Chip Select.** CS1S# is the ATA Command register block and corresponds to CS1FX# on the secondary IDE connector. CS1S is inverted externally (see PCI Local Bus IDE section).
LA22/ CS3S#	74	I/O	**Chip Select.** CS3S# is the ATA Control register block and corresponds to CS3FX# on the secondary IDE connector. CS3S is inverted externally (see PCI Local Bus IDE section).
LA21/ CS1P#	76	I/O	**Chip Select.** CS1P# is the ATA Command register block and correspond to CS1FX# on the primary IDE connector. CS1P is inverted externally (see PCI Local Bus IDE section).
LA20/ CS3P#	80	I/O	**Chip Select.** CS3P# is the ATA Control register block and corresponds to the CS3FX# on the primary connector. CS3P is inverted externally (see PCI Local Bus IDE section).
LA[19:17] DA[2:0]	82, 84, 86	I/O	**Disk Address.** DA[2:0] are used to indicate which byte in either the ATA command block or control block is being addressed.

Table 2- 6 82371SB (PIIX3) Signal Descriptions

Signal	Pin	Type	Description
ISA Interface			
BALE	64	O	**Bus Address Latch Enable.** BALE is an active high signal asserted by this chip to indicate that the address SA[19:0], LA[23:17] and SBHE# signal lines are valid.
AEN	20	O	**Address Enable.** AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMSA cycles as valid I/O cycles. This signal is also driven high during this chip initiated refresh cycles. When TC is sample low on the assertion of PWORK (External DMA mode), the chip tri-states this signal.
SYSCLK	153	O	**ISA System Clock.** SYSCLK is the reference clock for the ISA bus and drives the bus directly. SYSCLK is generated by dividing PCICLK by 3 or 4. The SYSCLK frequencies supported are 7.5 MHz and 8.33 MHz. SYSCLK is a divided down version of PCICLK. **Hardware strapping option.** SYSCLK is tri-stated when PWROK is negated. The value of SYSCLK is sampled on the assertion of PWROK. If sampled high, the ISA clock divisor is 3 (for 25 MHz PCI). If sampled low, the divisor is 4 (for 30 and 33 MHz PCI)
IORCHDY	18	I/O	**I/O Channel Ready.** Resources on the ISA bus negate IORCHDY to indicate that additional time (wait states) is required to complete the cycle. This owns the ISA bus and the CPU or a PCI agent accesses an ISA slave during DMA transfers. IORCHDY is an output when an external ISA bus master owns the ISA bus and is accessing DRAM or the chip register.
IOCS16#	71	I	**16-bit I/O Chip Select.** This signal is driven by I/O devices on the ISA bus to indicate that they support 16-bit I/O bus cycles.
IOCHK#	6	I	**I/O Channel Check.** IOCHK# can be driven by any resource on the ISA bus. When asserted, it indicates that a parity or an uncorrectable error has occurred for a device or memory on the ISA bus. If enabled, a NMI is generated to the CPU.
IOR#	23	I/O	**I/O Read.** IOR# is the command to an ISA I/O device that the slave may drive data on to the ISA data bus (SD[15:0]).
IOW#	24	I/O	**I/O Write.** IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus (SD[15:0]).

Table 2- 6 82371SB (PIIX3) Signal Descriptions

Signal	Pin	Type	Description
ISA Interface			
LA[23:17]/ CS1S#, CS3S#, CS1P#, CS3P#, DA[2:0]	72, 74, 76, 80, 82, 84, 86	I/O O O O O O	**Unlatched Address.** The LA[23:17] address lines are bidirectional. These address lines allow accesses to physical memory on the ISA bus up to 16 MB. The LA[23:17] are also used to drive the IDE interface chip selects and address lines via an external ALS244 buffer.
SA[7:0], SA[19:8], DD[11:0]	57, 59, 61, 63, 66,67, 68, 69 SA[19:8]/ DD[11:0], 39-41, 43-50, 55	I/O I/O I/O	**System Address Bus.** These bidirectional address lines define the selection with the granularity of one byte within the 1-MB section of memory defined by the LA[23:17] address lines. The address lines SA[A(:17] that are coincident with LA[19:17] are defined to have the same values as LA[19:17] for all memory cycles. For I/O accesses, only SA[15:0] are used.
SBHE#/ DD12	38	I/O I/O	**System Byte High Enable.** When asserted, SBHE# indicates that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles.
MEMCS16#	70	od	**Memory Chip Select 16.** MEMCS16# is a decode of LA[23:17] without any qualification of the command signal lines. ISA slaves that are 16-bit memory devices drive this signal low. During refresh cycles, the PIIX drives this signal low.
MEMR#	88	I/O	**Memory Read.** MEMR# is the command to a memory slave that it may drive data onto the ISA data bus. This signal is also driven by the PIIX during refresh cycles.
MEMW#	90	I/O	**Memory Write.** MEMW# is the command to a memory slave that it may latch data from the ISA data bus.
SMEMR#	19	O	**Standard Memory Read.** The PIIX asserts SMEMRQ# to request an ISA memory slave to accept data from the data lines. If the access is below 1 MB (000000000-000FFFFFh) during DMA compatible, the PIIX master or ISA master cycles, the PIIX asserts SMEMW#. SMEMW# is a delayed version of MEMW#.
ZEROWS#	15	I	**Zero Wait States.** An ISA slave asserts ZEROWS# after its address and command signals have been decoded to indicate that the current cycle can be shortened. A 16-bit ISA memory cycle can be reduced to two SYSCLKs. An 8-bit memory or I/O cycle can be reduced to three SYSCLKs. ZEROWS# has no effect during 16-bit I/O cycles.

Table 2- 6 82371SB (PIIX3) Signal Descriptions

Signal	Pin	Type	Description
ISA Interface			
SD[15:0]	107, 102-100, 98, 96, 94, 92, 7-9, 11, 13-14, 16-17	I/O	**System Data.** SD[15:0] support the 16-bit data path for devices residing on the ISA bus. SD[15:8] correspond to the high-order byte and SD[7:0] correspond to the low-order byte. SD[15:0] are undefined during refresh.
DMA			
DREQ[7:5, 3:0]	99, 95, 91, 87, 25, 12, 30	I	**DMA Request.** The DREQ lines are used to request DMA service from the chip DMA controller or for a 16-bit master to gain control of the ISA expansion bus. The active level (high or low) is programmed via the DMA command register. The request must remain active until the appropriate DACKx# signal is asserted.
DACK[7:5, 3:0]	97, 93, 89, 21, 60, 29, 85	O	**DMA Acknowledge.** The DAK output lines indicate that a request for DMA service has been granted by the chip or that a 16-bit master has been granted the bus. The active level (high or low) is programmed via the DMA command register. These lines should be used to decode the DMA slave device with the IOR# or IOW# line to indicate the selection. If used to signal acceptance of a bus master request, this signal indicates when it is legal to assert MASTER#. When TC is sampled low on the assertion of PWORK (External DMA mode), the chip tri-states these signals.
TC	62	O	**Terminal Count.** The PIIX asserts TC to DMA slaves as a terminal count indicator. When all the DMA channels are not in use, TC is negated (low). **Hardware Strapping Option.** This strapping option selects between the internal ISA DMA mode and External DMA mode. When TC is sampled high on the assertion of PWROK (ISA DMA mode), the chip drives the AEN, TC, and DACK[7:5, 3:0]# signals, and also forwards PCI masters I/O accesses to location 0000h to ISA. TC has an internal pull-up resistor. To tie TC low, an external 1KOhm pull-down resistor should be used.

Table 2- 6   82371SB (PIIX3) Signal Descriptions

Signal	Pin	Type	Description
DMA			
REFRESH#	31	I/O	**Refresh.** As an output, REFRESH# indicates when a refresh cycle is in progress. It should be used to enable the SA[15:0] address to the row address inputs of all banks of dynamic memory on the ISA bus. Thus, when MEMRW# is asserted , the entire expansion bus dynamic memory is refreshed. Memory signal is driven directly onto the ISA bus. This signal is an output only when the chip DMA refresh controller is a master on the bus responding to an internally generated request for refresh. As an input, REFRESH# is driven by 16-bit ISA bus masters to initiate refresh cycles.
SPKR	117	O	**Speaker Drive.** The SPKR signal is the output of counter 2.
OSC	136	I	**Oscillator.** OSC is the 14.31818-MHz ISA clock signal. It is used by the internal 8253 Timer.
Interrupt Controller			
IRQ[15., 14, 11:9, 7:3, 1]	81, 83, 75, 73, 10, 32, 33,34, 56, 58, 4	I	**Interrupt Request.** The IRQ signals support both system board components and ISA bus I/O devices with a mechanism for asynchronously interrupting the CPU. The assertion mode of these inputs depends on the programming of the two ELCR registers. IRQ14 is assumed by the bus master IDE interface function to be used to signal interrupts on the primary IDE channel.
IRQ8	5	I	**Interrupt Request Eight Signal.** IRQ8# is always an active low edge triggered interrupt input (i.e., software cannot modify this interrupt). Upon PCIRST#, IRQ8# is placed in active low edge-sensitive mode.
IRQ12	77	I	**Interrupt Request/Mouse Interrupt.** In addition to supporting the standard interrupt function signal, this pin can be programmed (via X-Bus chip select register) to grant a mouse interrupt function.
PIRQ[D:A]#	152-149	I I/O for PIRQD#	**Programmable Interrupt Request.** The PIRQx# signals can be shared with interrupts IRQ[15, 14, 12:9, 7:3] as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control register. These signals require external pull-up resistors. For the chip, when the APIC is enabled (via the XBCS Register), the USB interrupt is an output on PIRQD#.

Table 2- 6 82371SB (PIIX3) Signal Descriptions

Signal	Pin	Type	Description
Interrupt Controller			
INTR	122	od	**CPU Interrupt.** The 82371 drives the INTR to signal the CPU that an interrupt request is pending and needs to be serviced. The interrupt controller must be programmed following PCIRST# to ensure that INTR is at a known state.
NMI	135	od	**Non-maskable Interrupt.** NMI is used to force a non-maskable interrupt to the CPU. The 82371 generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control register is programmed.
System Power Management (SMM)			
SMI#	123	od	**System Management Interrupt.** SMI# is an active low synchronous output that is asserted by the chip in response to one of many enabled hardware or software events.
STPCLK#	124	od	**Stop Clock.** STPCLK# is an active low synchronous output that is asserted by the chip in response to one of the many hardware or software events. STPCLK# connects directly to the CPU and is synchronous to PCICLK.
EXTSMI#	125	I	**External System Management Interrupt.** EXTSMI# is a falling edge triggered input to the chip indicating that an external device is requesting the system to enter the SMM mode. An external pull-up resistor should be placed on this signal if it is not used or if it is not guaranteed to be always driven.
X-Bus			
XDIR#	141	O	**X-Bus Direction.** XDIR# is tied directly to the direction control of a 74F245 that buffers the X-Bus data (XD[7:0]). XDIR# is asserted for all I/O read cycles regardless if the accesses are to the chip supported device. XDIR# is only asserted for memory cycles if BIOS space has been decoded. For PCI master and ISA master-initiated read cycles, XDIR# is asserted from the falling edge of either IOR# or MEMR# (from MEMR# only if BIOS space has been decoded), depending on the cycle type. When the rising edge of IOR# or MEMR# occurs, the PIIX negates XDIR#. For DMA read cycles from the X-Bus, XDIR# is asserted from DACKx# falling and negated from DACKx# rising. At all other times, XDIR# is negated.

Table 2- 6 82371SB (PIIX3) Signal Descriptions

Signal	Pin	Type	Description
X-Bus			
XOE#	140	O	**X-Bus Output Enable.** XOE# is tied directly to the output enable of a 74F245 that buffers the X-Bus data (XD[7:0]) from the system data bus (SD[7:0]). XOE# is asserted when a PIIX supported X-Bus device is decoded, and the decoded device is enabled in the X-Bus Chip Select Enable Register (XBCS Register). XOE# is asserted from the falling edge of the ISA commands (IOR#, IOW#, MEMR#, or MEMW#) for PCI master and ISA master-initiated cycles. XOE# is negated from the rising edge of the ISA command signals for CPU and PCI master-initiated cycles and the SA[16:0] and LA[23:17] address for ISA master-initiated cycles. XOE# is not generated during any access to an X-Bus peripheral in which its decode space has been disabled.
DD15/PCS#	35	O	**Programmable Chip Select.** PCS# is asserted for ISA I/O cycles that are generated by PCI masters and subtractively decoded to ISA, if the access hits the address and programmed into the PCSC register. The X-bus buffer signals are enabled when the chip select is asserted assuming that the selected peripheral via this pin resides on the X-Bus.
BIOSCS#	137	O	**BIOS Chip Select.** BIOSCS# is asserted during read or write accesses to BIOS. BIOSCS# is driven in combination from the ISA addresses SA[16:0] and LA[23:17], except during DMA. During DMA cycles, BIOSCS# is not generated.
KBCS#	139	O	**Keyboard Controller Chip Select.** LBCS# is during I/O read or write accesses to KBC locations 60h and 64h. This signal is driven in combination from the ISA addresses SA[16:0] and LA[23:17]. For DMA cycles, KBCS# is never asserted.
RTCCS#	138	O	**Real Time Clock Chip Select.** RTCCS# is asserted during read or write accesses to RTC location 71h. RTCCS# can be tied to a pair of external OR gates to generate the real time clock read and write command signals.
RTCALE	148	O	**Real Time Clock Address Latch.** RTCALE is used to latch the appropriate memory address into the RTC. A write to port 70h with the appropriate RTC memory address that will be written to or read from causes the RTCALE assertion. RTCALE is asserted based on IOW# falling and remains asserted for two SYSCLKs.

Table 2- 6 82371SB (PIIX3) Signal Descriptions

Signal	Pin	Type	Description
X-Bus			
FERR#	130	od	**Numeric Coprocessor Error.** This signal is tied to the coprocessor error signal on the CPU. IGNNE# is only used if the chip coprocessor error reporting function is enabled in the XBCSA register. If FERR# is asserted, the chip generates an internal IRQ13 to this interrupt controller unit. The chip then asserts the INTR output to the CPU. FERR# is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the CPU unless FERR# is active. FERR# has a weak internal pull-up used to ensure a high level when the coprocessor error function is disabled.
IGNNE#	121	od	**Ignore Error.** This signal is connected to the ignore error pin on the CPU. IGNNE# is only used if the chip coprocessor error reporting function is enabled in the XBCSA register. If FERR# is asserted, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR is not asserted when the Coprocessor Error register is written, the IGNNE# signal is not asserted.
APIC Bus			
DD14/APICCS#	36	I/O O	**APIC Chip Select.** This active low output signal is asserted when the APIC chip select is enabled and a PCI originated cycle is positively decoded within the programmed I/O APIC address space. The default addresses of the I/O APIC are Memory FECO_0000h and FECO_0010h. *System Design Note:* The DD[14]/APICCS# signal is de-mixed externally with a 245 transceiver. The output of the transceiver drives the I?O APIC's CS# signal. At certain times the transceiver floats its outputs; therefore' a pull-up resistor on the output of the transceiver is required to keep this signal negated.

Table 2- 6 82371SB (PIIX3) Signal Descriptions

Signal	Pin	Type	Description
TESTIN#/ APICREQ#	134		**APIC Request.** This signal has two functions, depending on the programming of the APIC chip select bit (XBCS register) (see the test signal description for the TESTIN# function). APICREQ# is asserted by an external APIC device prior to sending an interrupt over the APIC serial bus. When the chip samples this pin active, it flushes its F-type DMA buffers pointing towards PCI. Once the buffers are flushed, the chip asserts APICACK# to inform the external APIC that it can proceed to send the APIC interrupt. APICREQ# must be synchronous to PCICLK.
APIC Bus			
PCIRST#/ APICACK#	128	O O	**APIC Acknowledge.** This signal has two functions, depending on the programming of the APIC chip select bit (XBCS register) (see the System reset signal description for the PCIRST# function). The chip asserts APICACK# after its internal buffers are flushed and that it can proceed to send the APIC interrupt. The signal is driven from the rising edge of PCICLK and is de-asserted while PCIRST# is asserted.
Universal Serial Bus (USB)			
USBCLK	146	I	**Universal serial bus clock.** This signal clocks the universal serial bus clock.
USBP0+ USBP0-	144, 145	I/O	**Universal serial bus port 0.** These signal are the differential data pair for serial port 0.
USBP1+ USBP1-	142, 143	I/O	**Universal serial bus port 1.** These signals are the differential data pair for serial port 1.
System Reset			
PWROK	126	I	**Power OK.** When asserted, PWROK is an indication to the PIIX that power and PCICLK have been stable for at least 1ms. PWROK can be driven asynchronously. When PWROK is negated the chip asserts CPURST, PCIRST# and RSTDRV. When PWROK is asserted, the PIIX negates CPURST, PCIRST# and RSTDRV.
CPURST	127	od	**CPU Reset.** During power-up and when a hard reset sequence is initiated through the RC register, the chip asserts CPURST to reset the CPU. CPURST is driven synchronously to the rising edge of the PCICLK. If a hard reset is initiated through the RC register, the chip resets its internal registers to the default state.

Table 2- 6 82371SB (PIIX3) Signal Descriptions

Signal	Pin	Type	Description
PCIRST#	128	O	**PCI Reset.** The chip asserts PCIRST# to reset devices that reside on the PCI bus. The chip asserts PCRST# during power-up and when a hard reset sequence is initiated through the RC register. PCIRST# is driven inactive in a minimum of 1ms after PWROK is driven active. PCIRST# is driven active for a minimum of 1ms when initiated through the RC register. PCIRST# is driven asynchronously relative to PCICLK.
System Reset			
INIT	129	od	**Initialization.** The chip asserts INIT if it detects a shutdown special cycle on the PCI bus or if a soft reset is initiated via RC register.
RSTDRV	28	O	**Reset Drive.** The chip asserts this signal during a hard reset and during power-up to reset ISA bus devices. RSTDRV is also asserted for a minimum of 1 ms if a hard reset has been programmed in the RC register.
Test			
TESTIN#	134	I	**Test Input.** The Test signal is used to tri-state all of the chip outputs. This input contains an internal pull-up resistor.

2.4 DEC 21152

Digital Semiconductor's 21152 is a second-generation PCI-to-PCI bridge and is fully compliant with PCI Local Bus Specification, revision 2.1. The 21152 is pin-to-pin compatible with Digital Semiconductor's 21052, which is fully compliant with PCI Local Bus Specification, revision 2.0. The 21152 provides full support for delayed transactions, which enables the buffering of memory read, I/O, and configuration transactions. The 21152 has separate posted write, read data, and delayed transaction queues with significantly more buffering capability than first-generation bridges. In addition, the 21152 supports buffering of simultaneous multiple posted write and delayed transactions in both directions. Among the features provided by the 21152 are a programmable 2-level secondary bus arbiter, individual secondary clock software control, and enhanced address decoding. The 21152 has sufficient clock and arbitration pins to support four PCI bus master devices directly on its secondary interface.

The 21152 allows the two PCI buses to operate concurrently. This means that a master and a target on the same PCI bus can communicate while the other PCI bus is busy. This traffic isolation may increase system performance in applications such as multimedia.

2.4.1 Features

- Complies fully with Revision 2.1 of the PCI Local Bus Specification
- Complies fully with Revision 1.1 of the PCI-to-PCI Bridge Architecture Specification
- Implements delayed transactions for all PCI configuration, I/O, and memory read commands–up to three transactions simultaneously in each direction
- Allows 88 bytes of buffering (data and address) for posted memory write commands in each direction–up to five posted write transactions simultaneously in each direction
- Allows 72 bytes of read data buffering in each direction
- Provides concurrent primary and secondary bus operation to isolate traffic
- Provides five secondary clock outputs:
  - Low skew, permitting direct drive of option slots
  - Individual clock control through configuration space
- Provides arbitration support for four secondary bus devices:
  - A programmable 2-level arbiter
  - Hardware disable control, permitting use of an external arbiter
- Provides enhanced address decoding:
  - A 32-bit I/O address range
  - A 32-bit memory-mapped I/O address range
  - A 64-bit pre-fetched memory address range
  - ISA-aware mode for legacy support in the first 64KB of I/O address range
  - VGA addressing and VGA palette snooping support

- Supports PCI transaction forwarding for the following commands:
  - All I/O and memory commands
  - Type 1 to Type 1 configuration commands
  - Type 1 to Type 0 configuration commands (downstream only)
  - All Type 1 to special cycle configuration commands
- Includes downstream lock support
- Supports both 5-V and 3.3-V signaling environments

2.4.2 Block Diagram

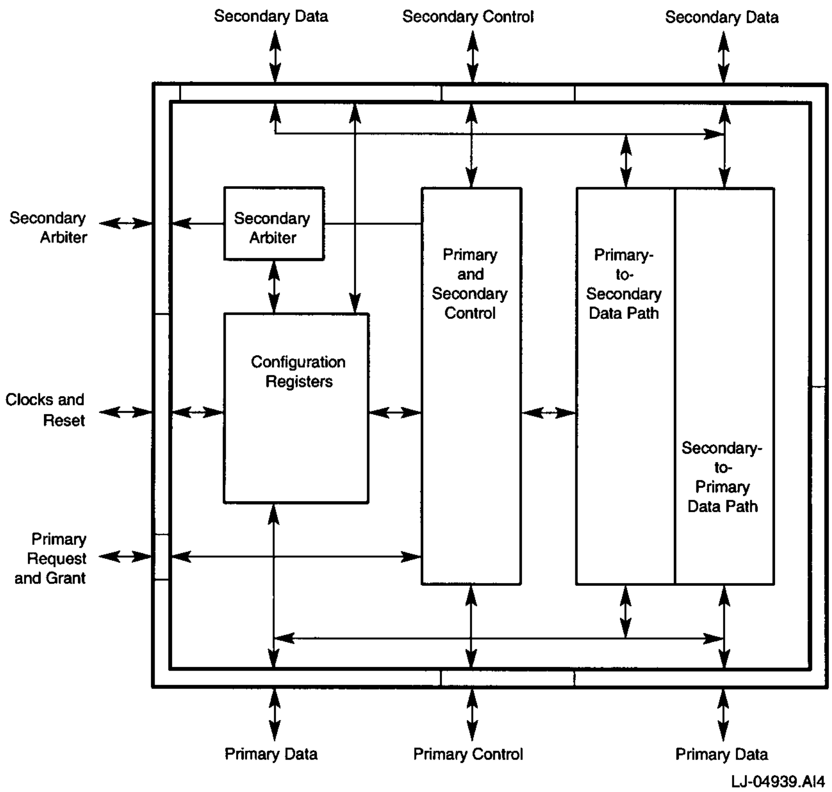


Figure 2- 9 DEC 21152 Block Diagram

2.4.3 Pin Diagram

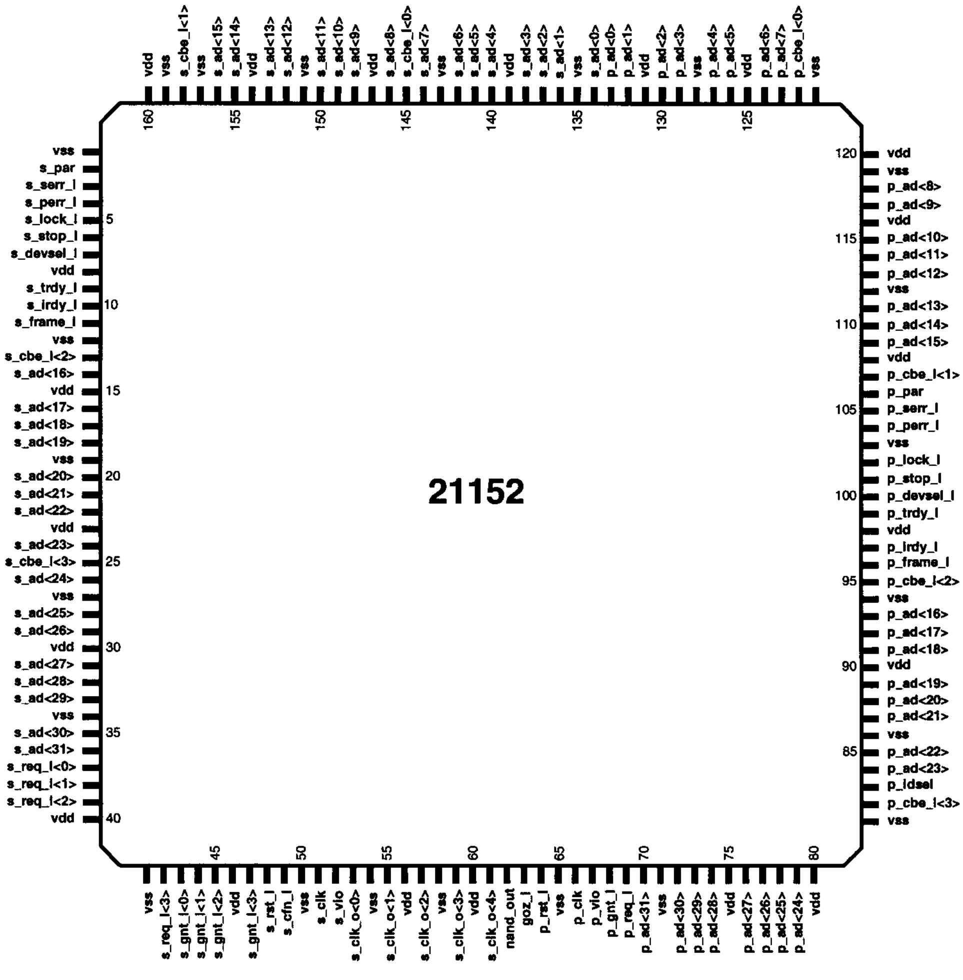


Figure 2- 10 DEC 21152 Pin Diagram

2.4.4 Signal Descriptions

Table 2- 7 DEC 21152 Signal Type Descriptions

Signal Type	Description
I	Standard input only.
O	Standard output only.
TS	Tristate bidirectional.
STS	Sustained tristate. Active low signal must be pulled high for one cycle when deasserting.
OD	Standard open drain.

Table 2- 8 DEC 21152 Signal Descriptions

Signal	Pin	Type	Description
Primary PCI Bus Interface Signals			
p_ad<31:0>	70, 72, 73, 74, 76, 77, 85, 87, 88, 89, 91, 92, 93, 109, 110, 111, 113, 114, 115, 117, 118, 123, 124, 126, 127, 129, 130, 132, 133	TS	**Primary PCI interface address/data.** These signals are a multiplexed address and data bus. During the address phase or phases of a transaction, the initiator drives a physical address on **p_ad<31:0>**. During the data phases of a transaction, the initiator drives write data, or the target drives read data, on **p_ad<31:0>.** When the primary PCI bus is idle, the 21152 drives **p_ad** to a valid logic level when **p_gnt_l** is asserted.
p_cbe_l<3:0>	82, 95, 107, 122	TS	**Primary PCI interface command/byte enables.** These signals are a multiplexed command field and byte enable field. During the address phase or phases of a transaction, the initiator drives the transaction type on **p_cbe_l<3:0>.** When there are two address phases, the first address phase carries the dual address command and the second address phase carries the transaction type. For both read and write transactions, the initiator drives byte enables on **p_cbe_l<3:0>** during the data phases. When the primary PCI bus is idle, the 21152 drives **p_cbe_l** to a valid logic level when **p_gnt_l** is asserted.

Table 2- 8 DEC 21152 Signal Descriptions

Signal	Pin	Type	Description
Primary PCI Bus Interface Signals			
p_par	106	TS	**Primary PCI interface parity.** Signal **p_par** carries the even parity of the 36 bits of **p_ad<31:0>** and **p_cbe_l<3:0>** for both address and data phases. Signal **p_par** is driven by the same agent that has driven the address (for address parity) or the data (for data parity). Signal **p_par** contains valid parity one cycle after the address is valid (indicated by assertion of **p_frame_l**), or one cycle after data is valid (indicated by assertion of **p_irdy_l** for write transactions and **p_trdy_l** for read transactions). Signal **p_par** is driven by the device driving read or write data one cycle after **p_ad** is driven. Signal **p_par** is tristated one cycle after the **p_ad** lines are tristated. Devices receiving data sample **p_par** as an input to check for possible parity errors. When the primary PCI bus is idle, the 21152 drives **p_par** to a valid logic level when **p_gnt_l** is asserted (one cycle after the **p_ad** bus is parked).
p_frame_l	96	STS	**Primary PCI interface FRAME#.** Signal **p_frame_l** is driven by the initiator of a transaction to indicate the beginning and duration of an access on the primary PCI bus. Signal **p_frame_l** assertion (falling edge) indicates the beginning of a PCI transaction. While **p_frame_l** remains asserted, data transfers can continue. The deassertion of **p_frame_l** indicates the final data phase requested by the initiator. When the primary PCI bus is idle, **p_frame_l** is driven to a deasserted state for one cycle and then is sustained by an external pull-up resistor.
p_irdy_l	97	STS	**Primary PCI interface IRDY#**. Signal **p_irdy_l** is driven by the initiator of a transaction to indicate the initiator's ability to complete the current data phase on the primary PCI bus. During a write transaction, assertion of **p_irdy_l** indicates that valid write data is being driven on the **p_ad** bus. During a read transaction, assertion of **p_irdy_l** indicates that the initiator is able to accept read data for the current data phase. Once asserted during a given data phase, **p_irdy_l** is not deasserted until the data phase completes. When the primary bus is idle, **p_irdy_l** is driven to a deasserted state for one cycle and then is sustained by an external pull-up resistor.

Table 2- 8 DEC 21152 Signal Descriptions

Signal	Pin	Type	Description
Primary PCI Bus Interface Signals			
p_trdy_l	99	STS	**Primary PCI interface TRDY#.** Signal **p_trdy_l** is driven by the target of a transaction to indicate the target's ability to complete the current data phase on the primary PCI bus. During a write transaction, assertion of **p_trdy_l** indicates that the target is able to accept write data for the current data phase. During a read transaction, assertion of **p_trdy_l** indicates that the target is driving valid read data on the **p_ad** bus. Once asserted during a given data phase, **p_trdy_l** is not deasserted until the data phase completes. When the primary bus is idle, **p_trdy_l** is driven to a deasserted state for one cycle and then is sustained by an external pull-up resistor.
p_devsel_l	100	STS	**Primary PCI interface DEVSEL#**. Signal **p_devsel_l** is asserted by the target, indicating that the device is accepting the transaction. As a target, the 21152 performs positive decoding on the address of a transaction initiated on the primary bus to determine whether to assert **p_devsel_l**. As an initiator of a transaction on the primary bus, the 21152 looks for the assertion of **p_devsel_l** within five cycles of **p_frame_l** assertion; otherwise, the 21152 terminates the transaction with a master abort. When the primary bus is idle, **p_devsel_l** is driven to a deasserted state for one cycle and then is sustained by an external pull-up resistor.
p_stop_l	101	STS	**Primary PCI interface STOP#**. Signal **p_stop_l** is driven by the target of the current transaction, indicating that the target is requesting the initiator to stop the current transaction on the primary bus. When **p_stop_l** is asserted in conjunction with **p_trdy_l** and **p_devsel_l** assertion, a disconnect with data transfer is being signaled. When **p_stop_l** and **p_devsel_l** are asserted, but **p_trdy_l** is deasserted, a target disconnect without data transfer is being signaled. When this occurs on the first data phase, that is, no data is transferred during the transaction, this is referred to as a target retry. When **p_stop_l** is asserted and **p_devsel_l** is deasserted, the target is signaling a target abort. When the primary bus is idle, **p_stop_l** is driven to a deasserted state for one cycle and then is sustained by an external pull-up resistor.

Table 2- 8   DEC 21152 Signal Descriptions

Signal	Pin	Type	Description
Primary PCI Bus Interface Signals			
p_lock_l	102	I	**Primary PCI interface LOCK#**. Signal **p_lock_l** is deasserted during the first address phase of a transaction and is asserted one clock cycle later by an initiator attempting to perform an atomic operation that may take more than one PCI transaction to complete. The 21152 samples **p_lock_l** as a target and can propagate the lock across to the secondary bus. The 21152 does not drive **p_lock_l** as an initiator; that is, the 21152 does not propagate locked transactions upstream. When released by an initiator, **p_lock_l** is driven to a deasserted state for one cycle and then is sustained by an external pull-up resistor.
p_idsel	83	I	**Primary PCI interface IDSEL#**. Signal **p_idsel** is used as the chip select line for Type 0 configuration accesses to 21152 configuration space. When **p_idsel** is asserted during the address phase of a Type 0 configuration transaction, the 21152 responds to the transaction by asserting **p_devsel_l**.
p_perr_l	104	STS	**Primary PCI interface PERR#**. Signal **p_perr_l** is asserted when a data parity error is detected for data received on the primary interface. The timing of **p_perr_l** corresponds to **p_par** driven one cycle earlier and **p_ad** and **p_cbe_l** driven two cycles earlier. Signal **p_perr_l** is asserted by the target during write transactions, and by the initiator during read transactions. When the primary bus is idle, **p_perr_l** is driven to a deasserted state for one cycle and then is sustained by an external pull-up resistor.

Table 2- 8 DEC 21152 Signal Descriptions

<table>
<tr><th>Signal</th><th>Pin</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">Primary PCI Bus Interface Signals</td></tr>
<tr><td>p_serr_l</td><td>105</td><td>OD</td><td>Primary PCI interface SERR#. Signal p_serr_l can be driven low by any device on the primary bus to indicate a system error condition. The 21152 can assert p_serr_l for the following reasons:
• Address parity error
• Posted write data parity error on target bus
• Secondary bus s_serr_l assertion
• Master abort during posted write transaction
• Target abort during posted write transaction
• Posted write transaction discarded
• Delayed write request discarded
• Delayed read request discarded
• Delayed transaction master timeout
Signal p_serr_l is pulled up through an external resistor.</td></tr>
<tr><td>p_req_l</td><td>69</td><td>TS</td><td>Primary PCI bus REQ#. Signal p_req_l is asserted by the 21152 to indicate to the primary bus arbiter that it wants to start a transaction on the primary bus. When the 21152 receives a target retry or disconnect in response to initiating a transaction, the 21152 deasserts p_req_l for at least two PCI clock cycles before asserting it again.</td></tr>
<tr><td>p_gnt_l</td><td>68</td><td>I</td><td>Primary PCI bus GNT#. When asserted, p_gnt_l indicates to the 21152 that access to the primary bus is granted. The 21152 can start a transaction on the primary bus when the bus is idle and p_gnt_l is asserted. When the 21152 has not requested use of the bus and p_gnt_l is asserted, the 21152 must drive p_ad, p_cbe_l, and p_par to valid logic levels.</td></tr>
</table>

Table 2- 8 DEC 21152 Signal Descriptions

Signal	Pin	Type	Description
Secondary PCI Bus Interface Signals			
s_ad<31:0>	36, 35, 33, 32, 31, 29, 28, 26, 24, 22, 21, 20, 18, 17, 16, 14, 156, 155, 153, 152, 150, 149, 148, 146, 144, 142, 141, 140, 138, 84, 136, 134	TS	**Secondary PCI interface address/data**. These signals are a multiplexed address and data bus. During the address phase or phases of a transaction, the initiator drives a physical address on **s_ad<31:0>**. During the data phases of a transaction, the initiator drives write data, or the target drives read data, on **s_ad<31:0>**. When the secondary PCI bus is idle, the 21152 drives **s_ad** to a valid logic level when its secondary bus grant is asserted.
s_cbe_l<3:0>	25, 13, 158, 145	TS	**Secondary PCI interface command/byte enables**. These signals are a multiplexed command field and byte enable field. During the address phase or phases of a transaction, the initiator drives the transaction type on **s_cbe_l<3:0>**. When there are two address phases, the first address phase carries the dual address command and the second address phase carries the transaction type. For both read and write transactions, the initiator drives byte enables on **s_cbe_l<3:0>** during the data phases. When the secondary PCI bus is idle, the 21152 drives **s_cbe_l** to a valid logic level when its secondary bus grant is asserted.
s_par	2	TS	**Secondary PCI interface parity**. Signal **s_par** carries the even parity of the 36 bits of **s_ad<31:0>** and **s_cbe_l<3:0>** for both address and data phases. Signal **s_par** is driven by the same agent that has driven the address (for address parity) or the data (for data parity). Signal **s_par** contains valid parity one cycle after the address is valid (indicated by assertion of **s_frame_l**), or one cycle after data is valid (indicated by assertion of **s_irdy_l** for write transactions and **s_trdy_l** for read transactions). Signal **s_par** is driven by the device driving read or write data one cycle after **s_ad** is driven. Signal **s_par** is tristated one cycle after the **s_ad** lines are tristated. Devices receive data sample **s_par** as an input to check for possible parity errors. When the secondary PCI bus is idle, the 21152 drives **s_par** to a valid logic level when its secondary bus grant is asserted (one cycle after the **s_ad** bus is parked).

Table 2- 8 DEC 21152 Signal Descriptions

Signal	Pin	Type	Description
Secondary PCI Bus Interface Signals			
s_frame_l	11	STS	**Secondary PCI interface FRAME#**. Signal **s_frame_l** is driven by the initiator of a transaction to indicate the beginning and duration of an access on the secondary PCI bus. Signal **s_frame_l** assertion (falling edge) indicates the beginning of a PCI transaction. While **s_frame_l** remains asserted, data transfers can continue. The deassertion of **s_frame_l** indicates the final data phase requested by the initiator. When the secondary PCI bus is idle, **s_frame_l** is driven to a deasserted state for one cycle and then is sustained by an external pull-up resistor.
s_irdy_l	10	STS	**Secondary PCI interface IRDY#**. Signal **s_irdy_l** is driven by the initiator of a transaction to indicate the initiator's ability to complete the current data phase on the secondary PCI bus. During a write transaction, assertion of **s_irdy_l** indicates that valid write data is being driven on the **s_ad** bus. During a read transaction, assertion of **s_irdy_l** indicates that the initiator is able to accept read data for the current data phase. Once asserted during a given data phase, **s_irdy_l** is not deasserted until the data phase completes. When the secondary bus is idle, **s_irdy_l** is driven to a deasserted state for one cycle and then is sustained by an external pull-up resistor.
s_trdy_l	9	STS	**Secondary PCI interface TRDY#**. Signal **s_trdy_l** is driven by the target of a transaction to indicate the target's ability to complete the current data phase on the secondary PCI bus. During a write transaction, assertion of **s_trdy_l** indicates that the target is able to accept write data for the current data phase. During a read transaction, assertion of **s_trdy_l** indicates that the target is driving valid read data on the **s_ad** bus. Once asserted during a given data phase, **s_trdy_l** is not deasserted until the data phase completes. When the secondary bus is idle, **s_trdy_l** is driven to a deasserted state for one cycle and then is sustained by an external pull-up resistor.

Table 2- 8 DEC 21152 Signal Descriptions

Signal	Pin	Type	Description
Secondary PCI Bus Interface Signals			
s_devsel_l	7	STS	**Secondary PCI interface DEVSEL#**. Signal **s_devsel_l** is asserted by the target, indicating that the device is accepting the transaction. As a target, the 21152 performs positive decoding on the address of a transaction initiated on the secondary bus in order to determine whether to assert **s_devsel_l**. As an initiator of a transaction on the secondary bus, the 21152 looks for the assertion of **s_devsel_l** within five cycles of **s_frame_l** assertion; otherwise, the 21152 terminates the transaction with a master abort. When the secondary bus is idle, **s_devsel_l** is driven to a deasserted state for one cycle and then is sustained by an external pull-up resistor.
s_stop_l	6	STS	**Secondary PCI interface STOP#.** Signal **s_stop_l** is driven by the target of the current transaction, indicating that the target is requesting the initiator to stop the current transaction on the secondary bus. • When **s_stop_l** is asserted in conjunction with **s_trdy_l** and **s_devsel_l** assertion, a disconnect with data trans-fer is being signaled. • When **s_stop_l** and **s_devsel_l** are asserted, but **s_trdy_l** is deasserted, a target disconnect without data transfer is being signaled. When this occurs on the first data phase, that is, no data is transferred during the transaction, this is referred to as a target retry. • When **s_stop_l** is asserted and **s_devsel_l** is deasserted, the target is signaling a target abort. When the secondary bus is idle, **s_stop_l** is driven to a deasserted state for one cycle and then is sustained by an external pull-up resistor.
s_lock_l	5	STS	**Secondary PCI interface LOCK#**. Signal **s_lock_l** is deasserted during the first address phase of a transaction and is asserted one clock cycle later by the 21152 when it is propagating a locked transaction downstream. The 21152 does not propagate locked transactions upstream. The 21152 continues to assert **s_lock_l** until the address phase of the next locked transaction, or until the lock is released. When the lock is released, **s_lock_l** is driven to a deasserted state for one cycle and then is sustained by an external pull-up resistor.

Table 2- 8 DEC 21152 Signal Descriptions

Signal	Pin	Type	Description
Secondary PCI Bus Interface Signals			
s_perr_l	4	STS	**Secondary PCI interface PERR#.** Signal **s_perr_l** is asserted when a data parity error is detected for data received on the secondary interface. The timing of **s_perr_l** corresponds to **s_par** driven one cycle earlier and **s_ad** driven two cycles earlier. Signal **s_perr_l** is asserted by the target during write transactions, and by the initiator during read transactions. When the secondary bus is idle, **s_perr_l** is driven to a deasserted state for one cycle and then is sustained by an external pull-up resistor.
s_serr_l	3	I	**Secondary PCI interface SERR#.** Signal **s_serr_l** can be driven low by any device except the 21152 on the secondary bus to indicate a system error condition. The 21152 samples **s_serr_l** as an input and conditionally forwards it to the primary bus on **p_serr_l**. The 21152 does not drive **s_serr_l**. Signal **s_serr_l** is pulled up through an external resistor.
Secondary Bus Arbitration Signals			
s_req_l<3:0>	37	I	**Secondary PCI interface REQ#s**. The 21152 accepts four request inputs, **s_req_l<3:0>**, into its secondary bus arbiter. The 21152 request input to the arbiter is an internal signal. Each request input can be programmed to be in either a high priority rotating group or a low priority rotating group. An asserted level on an **s_req_l** pin indicates that the corresponding master wants to initiate a transaction on the secondary PCI bus. If the internal arbiter is disabled (**s_cfn_l** tied high), **s_req_l<0>** is reconfigured to be an external secondary grant input for the 21152. In this case, an asserted level on **s_req_l<0>** indicates that the 21152 can start a transaction on the secondary PCI bus if the bus is idle.
s_gnt_l<3:0>	47, 45, 44, 43	TS	**Secondary PCI interface GNT#s**. The 21152 secondary bus arbiter can assert one of four secondary bus grant outputs, **s_gnt_l<3:0>**, to indicate that an initiator can start a transaction on the secondary bus if the bus is idle. The 21152's secondary bus grant is an internal signal. A programmable 2-level rotating priority algorithm is used. If the internal arbiter, **s_cfn_l**, is disabled (tied high), **s_gnt_l<0>** is reconfigured to be an external secondary bus request output for the 21152. The 21152 asserts this signal whenever it wants to start a transaction on the secondary bus.

Table 2- 8 DEC 21152 Signal Descriptions

Signal	Pin	Type	Description
Secondary Bus Arbitration Signals			
s_cfn_l	49	I	**Secondary PCI central function enable**. When tied low, **s_cfn_l** enables the 21152 secondary bus arbiter. When tied high, **s_cfn_l** disables the internal arbiter. An external secondary bus arbiter must then be used. Signal **s_req_l<0>** is reconfigured to be the 21152 secondary bus grant input, and **s_gnt_l<0>** is reconfigured to be the 21152 secondary bus request output, when an external arbiter is used. Secondary bus parking is done when **s_req_l<0>** is asserted, the secondary bus is idle, and the 21152 does not want to initiate a transaction.
Clock Signals			
p_clk	66	I	**Primary interface PCI CLK**. Provides timing for all transactions on the primary PCI bus. All primary PCI inputs are sampled on the rising edge of **p_clk**, and all primary PCI outputs are driven from the rising edge of **p_clk**. Frequencies supported by the 21152 range from 0 MHz to 33 MHz.
s_clk	51	I	**Secondary interface PCI CLK**. Provides timing for all transactions on the secondary PCI bus. All secondary PCI inputs are sampled on the rising edge of **s_clk**, and all secondary PCI outputs are driven from the rising edge of **s_clk**. Frequencies supported by the 21152 range from 0 MHz to 33 MHz.
s_clk_o<4:0>	61, 59, 57, 55, 53	O	**Secondary interface PCI CLK outputs**. Signals **s_clk_o<4:0>** are 5 clock outputs generated from the primary interface clock input, **p_clk**. These clocks operate at the same frequency of **p_clk**. When these clocks are used, one of the clock outputs must be fed back to the secondary clock input, **s_clk**. Unused clock outputs can be disabled by writing the secondary clock disable bits in configuration space; otherwise, terminate them electrically.

Table 2- 8 DEC 21152 Signal Descriptions

Signal	Pin	Type	Description
Reset Signals			
p_rst_l	64	I	**Primary PCI bus RST#**. Signal **p_rst_l** forces the 21152 to a known state. All register state is cleared, and all primary PCI bus outputs are tristated. Signal **p_rst_l** is asynchronous to **p_clk**.
s_rst_l	48	O	**Secondary PCI bus RST#**. Signal **s_rst_l** is driven by the 21152 and acts as the PCI reset for the secondary bus. The 21152 asserts **s_rst_l** when any of the following conditions is met: • Signal **p_rst_l** is asserted. • The secondary reset bit in the bridge control register in configuration space is set. • The chip reset bit in the diagnostic control register in configuration space is set. When the 21152 asserts **s_rst_l**, it tristates all secondary control signals and drives zeros on **s_ad**, **s_cbe_l**, and **s_par**. Signal **s_rst_l** remains asserted until **p_rst_l** is deasserted, and the secondary reset bit is clear. Assertion of **s_rst_l** by itself does not clear register state, and configuration registers are still accessible from the primary PCI interface.
Miscellaneous Signals			
p_vio	67	I	**Primary interface I/O voltage**. This signal must be tied to either 3.3 V or 5 V, corresponding to the signaling environment of the primary PCI bus as described in the *PCI Local Bus Specification*, *Revision 2.1*. When any device on the primary PCI bus uses 5-V signaling levels, tie **p_vio** to 5 V. Signal **p_vio** is tied to 3.3 V only when all the devices on the primary bus use 3.3-V signaling levels.
s_vio	52	I	**Secondary interface I/O voltage**. This signal must be tied to either 3.3 V or 5 V, corresponding to the signaling environment of the secondary PCI bus as described in the *PCI Local Bus Specification, Revision 2.1*. When any device on the secondary PCI bus uses 5-V signaling levels, tie **s_vio** to 5 V. Signal **s_vio** is tied to 3.3 V only when all the devices on the secondary bus use 3.3-V signaling levels.

Table 2- 8 DEC 21152 Signal Descriptions

Signal	Pin	Type	Description
Nand Tree Signals			
goz_l	63	I	**Diagnostic tristate control.** This signal, when asserted, tristates all bidirectional and tristatable output pins.
nand_out	62	O	**Nand tree diagnostic output**. This signal is dedicated to the diagnostic Nand tree. The Nand tree starts at **s_cfn_l** and runs clockwise. All inputs, except **p_clk** and **s_clk,** are used in the Nand tree. The **goz_l** signal should be asserted when the Nand tree mechanism is used.
Power / Ground			
vdd	8, 15, 23, 30, 40, 46, 56, 60, 75, 80, 90, 108, 116, 120, 125, 131, 139,		**Power pins.**
Vss	34, 41, 50, 54, 58, 65, 71, 81, 86, 94, 103, 112, 119, 121, 128, 135, 145, 151, 157, 159		**Ground pins.**

2.5 ATI 264VT

The ATI 264VT is a highly integrated multimedia graphics and video controller for both multiplexed VESA Local Bus (VLB) and PCI bus systems. The VT achieves unprecedented performance with an "all-in-one" design that integrates a video scaler, a color space converter, a true-color palette DAC, and a triple-clock synthesizer with ATI's proven mach64 graphics engine.

Active power management techniques are used to monitor activity levels within these graphics controllers and to perform real-time power reductions such as dynamic clock control and graphics engine shutdown. Because full-speed operation can be restored without delay, these techniques do not have impact on performance.

The VT is register-compatible with ATI's *mach64* accelerator series and provides immediate compatibility with a wide range of application drivers.

The VT is backward compatible with ATI's family of integrated controllers, providing OEM with a low-cost path to additional features and performance.

2.5.1 Features

- High integration results hl a low cost and small footprint graphics subsystem ideal for motherboard implementations.
- PCI revision 2.0 bus for Plug-and-Play ease of use.
- True-color palette DAC supporting pixel clock rates up to 135 MHz for 1280 x 1024 resolution at 75 Hz.
- YUV to RGB conversion with support for both packed-pixel and planar YUV formats
- DDC1 and DDC2B Plug-and-Play monitor support.
- Support for 26-pin VESA compatible feature com1ector that supports up to 1024 x 768 resolution
- Flexible memory configurations: 1 MB to 4 MB DRAM, 256K x 4, 256K x 8, or 256K x l6 with support for either dual CAS or dual write.

2.5.2 Block Diagram

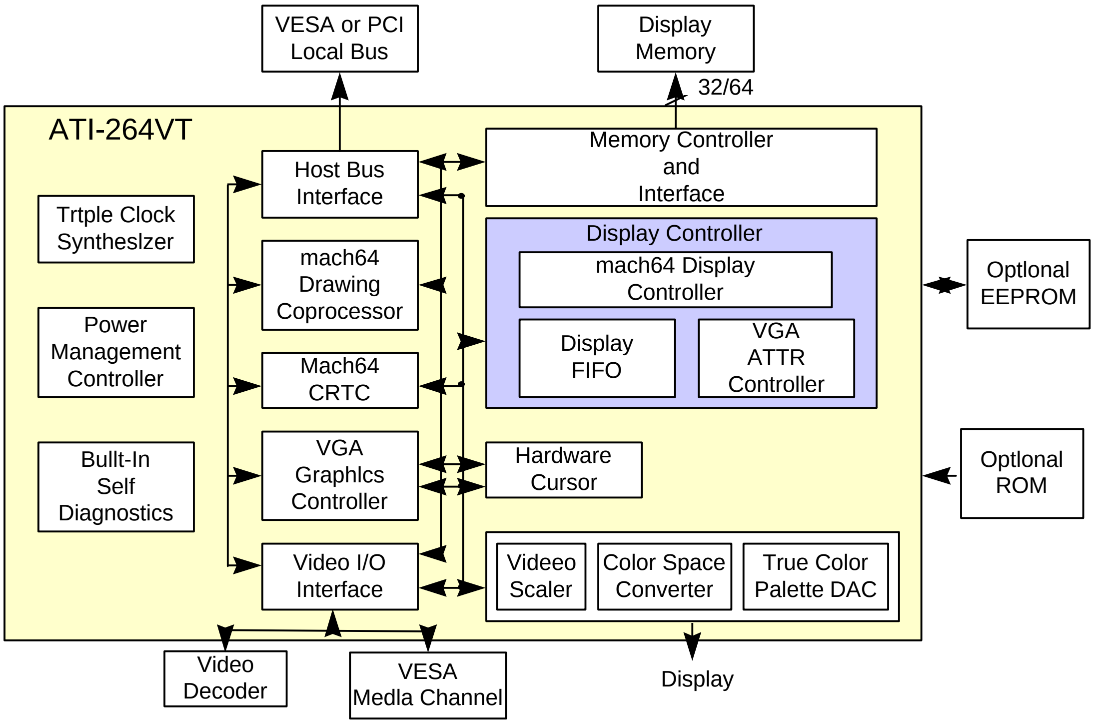


Figure 2- 11 ATI 264VT Block Diagram

2.5.3 Pin Diagram

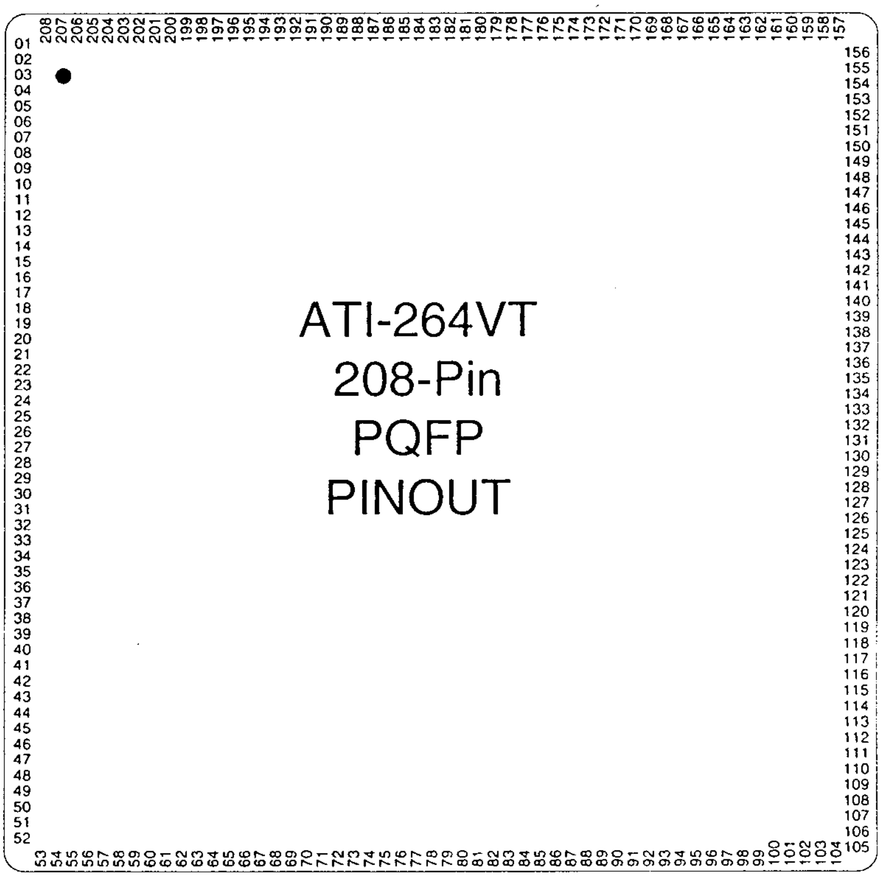


Figure 2- 12 ATI 264VT Pin Diagram

2.5.4 Signal Descriptions

Table 2- 9 ATI 264VT Signal Descriptions

Signal	Pin	Type	Description
Bus Interfaces / PCI Local Bus Implementation			
AD[31:0]	143: 150 153: 154 158: 163 174: 181 185: 192	I/O	System Address or Data bits (31:0)
C/BE#[3:0]	151, 164, 173, 184	I	Bus Command or Byte Enable bits 3:0. BE# are active low.
CPUCLK	142	I	Bus Clock
DEVSEL#	169	O	Device Select. When actively driven, it indicates that the controller has decoded its address.
FRAME#	165	I	FRAME. Frame is driven by the current bus master to indicate the beginning and duration of an access.
IDSEL	152	I	Initialization Device Select. Used as a chip select during configuration read and write transactions.
INTR#	140	O	Interrupt Request. Level triggered, active low by default
IRDY#	166	I	Initiator Ready. Indicates the bus master is able to complete the current data phase of transaction.
PAR	172	O	Parity. Even parity used
RESET#	141	I	Bus Reset
STOP#	171	O	Stop. Indicates the current target us requesting the master to stop the current transaction.
TRDY#	167	O	Target Ready. Indicates the target agent is able to complete the current data phase of the transaction.
AD[31:0]	143:150, 153:154. 158:163, 174:181, 185:192	I/O	System Address or Data bits [31:0]
BE#3 [IDSEL]	152	I	BE#[3]
BE#0 [TRDY#]	167	I	BE#[0]
BE#1 [DEVSEL#]	169	I	BE#[1]
BE#2 [STOP#]	171	I	BE#[2]
RESET	141	I	Reset
LCLK [CPUCLK]	142	I	CPUCLK
RDYRTN [IRDY]	166	O	RDYRTN#
LRDY# [FRAME#]	165	I	LRDY#

Table 2- 9 ATI 264VT Signal Descriptions

Signal	Pin	Type	Description
ADS# [PAR]	172	O	ADS#
Bus Interfaces / PCI Local Bus Implementation			
DIR [C/BE3]	151	O	DIR
DEN3	164	O	DEN#
AEN# [C/BE1]	173	O	AEN#
LDEV# [C/BE0]	184	O	LDEV#
INTR	140	I	INTR
Memory Interfaces / Dual-write Memory 256x4, 256x8, 256x16			
CAS0#/WE#0	29	O	Column Address Strobe for first and second MB of memory
CAS1#/WE#1	28	O	Column Address Strobe for third and fourth MB of memory
MA[9:0]	204, 198, 196, 194:193	O	Memory Address bits 9:0
MD[31:0]	55: 54 50: 40 38 36: 30 24: 14	I/O	Data bits 31:0 for first and third MB of memory
MD[63:32]	92: 90 88: 80 77: 65 63, 61: 56	I/O	Data bits 63 and 32 of second and fourth MB of memory
OE#0	205	O	Output Enable for first and second MB of memory
OE#1	207	O	Output Enable for third and fourth MB of memory
RAS#0	3	O	Row Address Strobe for first and second MB of memory
RAS#1	206	O	Row Address Strobe for third and fourth MB of memory
WE#/CAS# [7:0]	4:9, 11, 13	I/O	Write Enable bits 7:0
Memory Interfaces / Dual-CAS Memory 256x4, 256x8, 256x16			
WE#/CAS# [7:0]	4:9, 11, 13	I/O	Column Address Strobe
MA[9:0]	204, 198 196 194: 193	O	Memory Address bits 9:0
MD[31:0]	55:54 50: 40 38 36: 30 24: 14	I/O	Data bits 63 and 32 of second and fourth MB of memory
MD[63:32]	92:90, 88:80, 77:65, 63, 61:56	I/O	Data bits 63 and 32 of second and fourth MB of memory

Table 2- 9　　ATI 264VT Signal Descriptions

Signal	Pin	Type	Description
RAS#0	3	O	Row Address Strobe for first and second MB of memory
Memory Interfaces / Dual-CAS Memory 256x4, 256x8, 256x16			
RAS#1	206	O	Row Address Strobe for the third and fourth MB of memory
CAS#/WE#0	29	O	Write Strobe for first and second MB of memory
CAS#/WE#1	28	O	Write Strobe for the third and fourth MB of memory
OE#0	205	O	Output enable for the first and second MB of memory
OE#1	207	O	Output enable for third and fourth MB of memory
Memory Interfaces / SDRAM Memory 128x16x2			
CAS# [1:0]	28, 29	O	CAS[1:0]
RAS# [1:0]	3,206	O	RAS[1:0]
WE# [7:0]	4, 9, 11, 13	O	DQM[7:0]
OE#1	205	O	WE#
OE#0	207	O	CLK
MA[9:0]	204:198, 196, 194, 193	O	MA[9:0]
MD[63:0]	55, 54, 50:40, 38, 36:30, 24:14, 92:90, 88:80, 77:65, 63, 61:56	I/O	AD[63:0]
DAC and Monitor Interface			
R	120	O	Red analog pixel data output to monitor
G	121	O	Green analog pixel data output to monitor
B	122	O	Blue analog pixel data output to monitor
COMP	124	A	Compensation pin for the DAC
RSET	123	A	Current setting resistor for the DAC
VREF	125	A	DAC reference voltage
HSYNC	129	O	Horizontal sync
VSYNC	128	O	Vertical sync
Frequency Synthesizer Interface			
MLOOP	111	A	Memory clock loop filter
PLOOP	114	A	Pixel clock loop filter
XTALIN[1]	102	A	14.31818 MHz crystal or TTL oscillator connection

[1] For designs using an external clock source (instead of a crystal), the input XTALIN is CMOS inverter C_{in}=0.5pF, and XTALOUT is not connected.

Table 2- 9 ATI 264VT Signal Descriptions

Signal	Pin	Type	Description
XTALOUT[1]	103	A	14.31818 MHz crystal connection
Feature Connector Interface			
EDCLK	107	I	Auxiliary Pixel Clock Select
ESYNC	133	I	Auxiliary Pixel Clock Select
EVIDEO	132	I	Auxiliary Pixel Data Select
BLANK#	135	O	Blank Signal
DCLK	134	O	Pixel Clock Output
PIXEL[7:0]	93:100	O	Pixel Data Output
EEPROM Interface			
GIO2	135	I/O	EEPROM Data I/O
GIO3	136	O	EEPROM Chip Select
GIO1	109	I/O	EEPROM Clock
EPROM Interface			
ROMCS#	113	O	ROM Chip Select
MD [46:32]	72:56	I/O	EPROM Address Bus
MD [63:56]	92:84	I/O	EPROM Data Bus
Monitor ID Interface			
GIO0	108	I/O	DDC Serial Data
GIO4	138	I/O	DDC Serial Clock
VMC Interface			
SA#	117		Serial I/O Interrupt Request
SB# [EDCLK]	107		Serial I/O Interrupt Request
BS#0 [BLANK#]	135		Bus Size
BS#1 [EVIDEO#]	133		Bus Size
VMCCTRL [ESYNC]	133		VMC Control Cycle Flag
VMCMASK	25		Pixel Mask
VMCCLK [DCLK]	134		VMC CLock
SNRDY#	137		Slave Not Ready
DATA [7:0]	100:93		Data Bits

Table 2- 9 ATI 264VT Signal Descriptions

Signal	Pin	Type	Description
Power and Ground Pins			
VCC	10, 27, 37, 53, 62, 78, 89, 104, 127, 130, 170, 195, 208	PWR	3.3V Power
VSS	1, 2, 12, 26, 39, 51, 52, 64, 79, 101, 105, 118, 131, 155, 156, 168, 182, 197	GND	Ground
PVDD	110, 115	PWR	PLL Power
PVSS	112	GND	PLL Ground
QVSS	106	GND	PLL Ground
AVDD	126	PWR	DAC Analog Power
AVSS	119	GND	DAC Analog Ground
VEE	139, 157, 183	PWR	5.0V Power

2.6 Adaptec AIC 7880

The AIC-7880 provides advanced host adapter features in a single chip with a SCSI-2 bus controller and a full featured PCI 32-bit bus master with zero wait state transfer capability including PCI enhanced data transfer commands. The AIC-7880 chip incorporates a dedicated processor, the SCSI PhaseEngine™ (RISC Sequencer), which executes a SCSI command described by a Sequencer Control Block (SCB). Sixteen SCBs may be stored in the internal SCB Array and with the addition of an external SRAM, a maximum of 256 SCBs may be stored for execution. These SCBs are executed independently of the SCSI target ID in the order that they are received. The SCB is a data structure which contains all information necessary for the execution of the command. The sequencer in the chip handles all phases of the SCSI bus, including the Disconnect/ Reconnect and Command Complete message. On the PCI host side, bus master transfers are made in a 64-bit address space at up to the maximum burst rate of 133 MBytes/ sec with data buffering of 256 bytes.

The AIC-7880 also provides a memory port for external access, an 8-bit ROM/EEPROM (for add-in card local BIOS support), a serial 1-bit EEPROM (for nonvolatile SCSI bus device and parameter storage, and/or adapter board assembly/serial/revision information), an 8/9-bit SRAM (for SCB expansion), and external board logic control.

2.6.1 Features

- Automatic data threshold selection
- Power-down modes
- Scatter/Gather operations supported
- Extremely low SCSI command overhead
- Data residue reported on underruns
- One interrupt per command completion, multiple command completion may be queued on a single interrupt
- Queued commands per Target/LUN
- Overlapped command execution
- Modify Data Pointers message handled
- Tagged Queuing supported
- SCSI Configured AutoMagically (SCAM level 1 support)
- Data path from PCI bus to SCSI bus internally byte parity protected
- Hardware address breakpoint capability for software debug
- External BIOS ROM option with in-place BIOS update (EEPROM) capability
- Device ID option for exchanging internal default value with an external value
- External Board Control option for controlling host adapter logic external to the AIC-7880 from the PCI bus

SCSI Features

- Fast (10 MHz) data transfers
- Wide data transfers
- Differential controls
- Flexible configuration
    - One 8-bit Single-ended, Fast
    - One 8-bit Differential, Fast
    - One 16-bit Single-ended, Fast
    - One 16-bit Differential, Fast
- Auto SCSI bus PIO
- Wide data connector indicator
- LED indicator control (SCSI busy, diagnostics, external ID clock) or general purpose control
- Selectable SCSI output active negation
- SCSI termination power down control or general purpose control
- SCAM level 1 support
- Digital filtering for incoming REQ and ACK signals

PCI 32-bit Interface

- Direct pin out connection to PCI 32-bit bus interface
- PCI bus master with zero wait state 32-bit memory data transfers at 133 MBytes/sec, capable of leading and trailing 32-bit boundary offset bytes, with a 32-bit address range within a selected 64-bit address page
- Supports both PCI single and dual address cycles
- PCI bus master/slave timing referenced to PCI signal PCLK (33.3 MHz max)
- Buffered PCI signal PCLK output for adapter card logic usage
- PCI bus master programmable Latency Timer, Cache Size, and Interrupt Line Select registers
- PCI bus access of AIC-7880 device registers from both PCI I/O and memory address spaces
- Supports exchange of internal device ID default value with an external value
- Supports medium PCI target device-select response time
- Supports enhanced PCI system memory data Read and Write commands
- Cache line streaming capability

- Supports PCI bus address and data parity generation and checking
- Supports PCI PERR and SERR requirements
- Supports 32-bit external ROM read access
- Data transfers may be selected to be initiated by CACHESIZE or data level thresholds
- Data FIFO data flush for transfers to system memory
- IRQA# interrupt generation .from hardware, firmware and software controlled sources
- Supports reduced power requirements when not performing master data transfers

Data Buffer

- Data FIFO provides 256 bytes of storage, dual-ported RAM, with parity per byte
- Programmable data and cache size threshold levels to initiate PCI bus master requests
- Early FIFO full status
- Multi byte-width data ports: 8 (PCI), 2 (SCSI), 1 (sequencer or driver) byte with byte parity
- Byte write parity generation and byte read parity checking
- Read/write capable address counters
- Partial quad-word detection and adjustment
- Starting address byte offset capable

Scratch RAM

- 64 bytes of dual-ported SRAM, accessible by sequencer and host drivers
- Byte parity protected

Sequencer (SCSI PhaseEngine)

- RISC instruction per clock design
- Clock rate selectable for 8 or 10 MHz operation
- SRAM microcode storage, 512 29-bit words plus byte parity
- Sixteen instruction group types
- Operation may be paused by maskable interrupt condition or software driver
- Diagnostic single-step and address breakpoint
- SLEEP mode for chip power reduction

2.6.2 Block Diagram

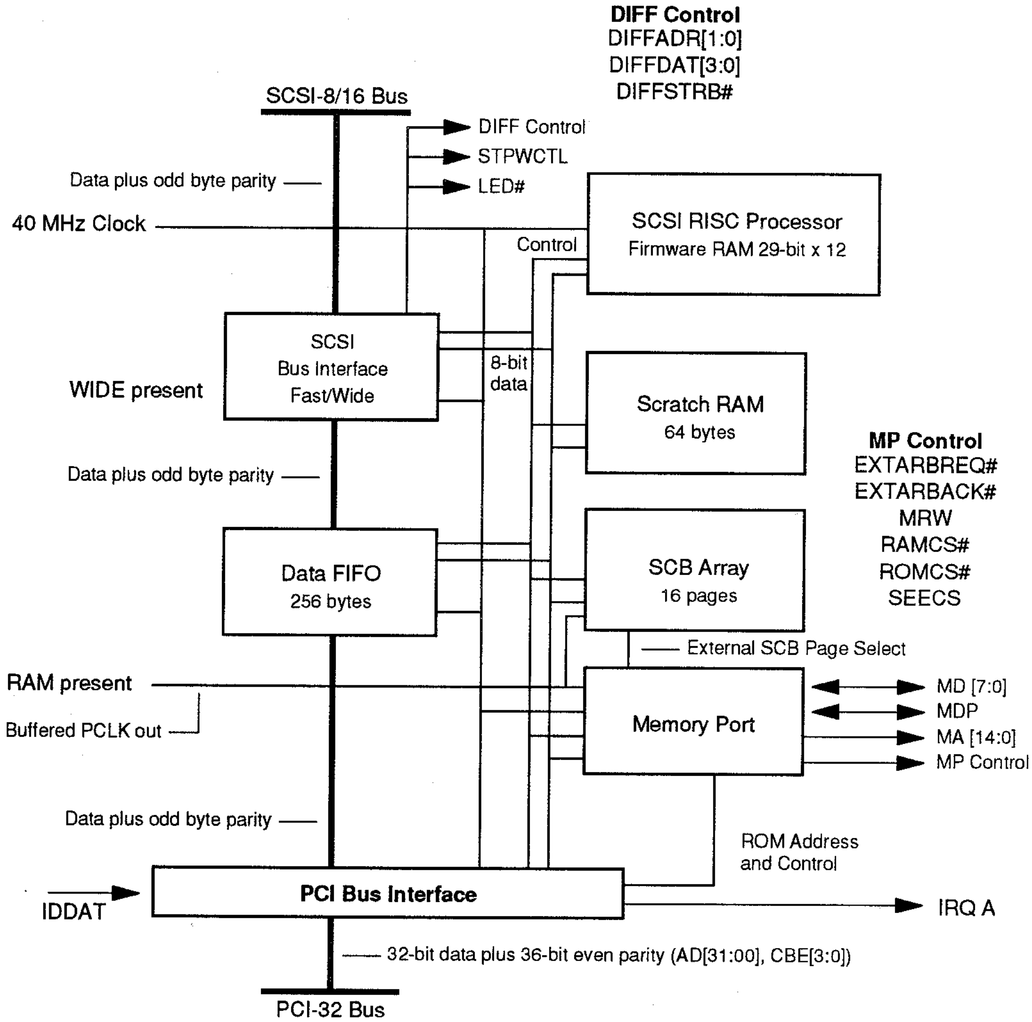


Figure 2- 13 AIC 7880 Block Diagram

2.6.3 Pin Diagram

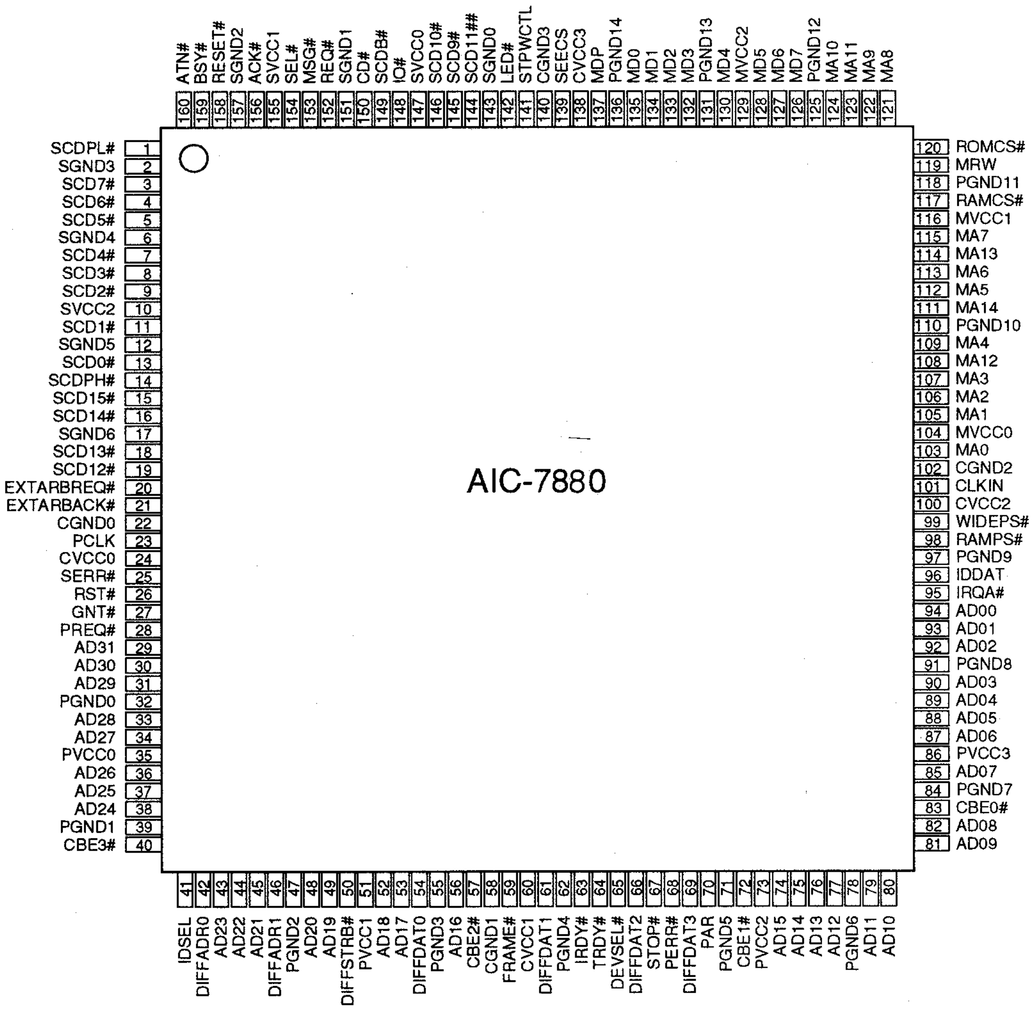


Figure 2- 14 AIC 7880 Pin Diagram

2.6.4 Signal Descriptions

The following notations describe the signal types.

Table 2- 10 AIC 7880 Signal Type Descriptions

Signal Type	Description
I	Input
3ST/#	Tristate output/minute drive current in mA
OD/#	Open drain output/minute drive current in mA
NOD/#	Negation capable open drain output/minute sink current in mA

Table 2- 11 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
Host Interface[1]			
AD[31:00]	29-31, 33, 34, 36-38, 43-45, 48, 49, 52, 53, 56, 74-77, 79-82, 85, 87-90, 92-94	I, 3ST/6	**Address and Data.** These are multiplexed on the same PCI bus pin. During the first clock of a transaction, AD[31:00] signals contain 32-bit physical byte address called low address [31:00] for Single Address Cycles (SAC). During subsequent clocks, AD[31:00] contain 32-bit data called low data 31:00 except for Dual Address Cycle (DAC) where both the first and the second (high address 63:32) clocks of a transaction contain address and the remaining clocks contain data (low data 31:00). The turn-around PCLK period for AD[31:00] is the idle cycle between transactions.
CBE[3:0]#	40, 57, 72, 83	I, 3ST/6	**Bus Command and Byte Enables.** These signals are multiplexed on the same PCI pins. During the address phase of a transaction, CBE[3:0]# may assert concurrently and indicate a command to PCI.
DEVSEL#	65	I; 3ST/6	**Device Select.** When this signal is asserted, it indicates that the driving device has decoded its address as the selected target of the current bus transaction. DEVSEL# cannot be de-asserted once it is asserted unless FRAME# is sampled de-asserted except for the target abort case. Also, DEVSEL# must be asserted for one or more PCLKs before a target-abort condition may be signaled.

[1] Host interface signals separated by semi-colon (;) are for I/O PCI Master and I/O PCI Target, respectively.

Table 2- 11 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
Host Interface			
FRAME#	59	I, 3ST/6	**Frame.** The FRAME# signal is asserted by the current master to indicate the duration of a bus transaction. The assertion of FRAME# identifies an address phase of a transaction. De-assertion of this signal identifies the final data phase of the transaction.
GNT#	27	I	**Grant.** An asserted GRANT# signal indicates to master that a bus transaction may be performed. This is a point-to-point signal with every master having its own GNT# signal. Only one GNT# may be asserted by the PCI System Board Central Source Arbitrator at a time.
PAR	70	I, 3ST/6	**Parity.** This is an even-parity bit that protects both AD[31:00] and C\BE[3:0]# signals. PAR is generated by the agent that is sourcing the 32-bit address of the transaction and/or the data of the transaction, including the CBE[3:0] values.
IDSEL	41	I	**Initialization Device Select.** The signal is used in lieu of the upper 24 ADn address signals and is valid only during configuration read and write transactions. This signal is validated with FRAME# assertion and valid CBEn# values. IDSEL is a point-to-point signal with each agent having its own IDSEL. PCI convention is to connect a different AD[31:11] line to IDSEL input of each device on the bus. Dagger respond to all accesses in its configuration address range.
IRDY#	63	I, 3ST/6	**Initiator Ready#.** This signal is asserted to indicate the current master's ability to complete the current data phase of a transaction. During a write, IRDY# indicates that the master is prepared to accept data on AD[31:00]. It is used in conjunction with TRDY#. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. A data phase is completed on any PCLK when IRDY# and TRDY# are both sampled asserted. An idle cycle (PCI bus free) occurs when both FRAME# and IRDY# are de-asserted. The turn-around PCLK period for IRDY# is the address phase of a transaction.
PCLK	23	I	**PCI Bus Clock Input.** This input supports timing for all transactions on the PCI bus. All other PCI signals are sampled on the rising edge of PCLK and all other parameters are defined with respect to this edge. PCLK is a controlled skew, point-to-point signal to each agent and is only driven by the PCI System Board Central Resource. The PCLK signal for the Dagger is a maximum rate of 33.3 MHz.

Table 2- 11 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
Host Interface			
PREQ#	28	3ST/6	**PCI Request.** Once asserted, this pin indicates to the PCI System Board Arbitrator that a master desires use of the bus. This is a point-to-point signal with every master having its own PREQ#. Arbitration for the PCI bus is performed either when the bus is idle or in parallel with the transaction in process.
PERR#	68	I, 3ST/6	**Parity Error#.** This signal may be asserted (Pulsed for one PCLK period for each detected error, provided that the Parity Error Response bit, PERRESPEN, is active in the Configuration Command register) only by the agent receiving the data. Also, a target cannot assert PERR# until it has claimed the access by asserting DEVSEL# and completing the data transfer. The turn-around PCLK for PERR# is the third PCLK period after the last address PAR period for an agent. PERR# is asserted for detected errors after two PCLK periods.
RST#	26	I	**Reset#.** When this signal is asserted, it forces agents to a known initialization state. RST# may be synchronous to PCLK when asserted or de-asserted.
SERR#	25	I, OD/6	**System Error#.** This signal may be asserted by a PCI agent that detects an address parity error (provided that PERRESPEN and SERRESPEN are active) during the address phase of a transaction of for data parity errors on special cycles and for any other system error where the result is a catastrophic error. The transaction master is solely responsible for reporting master or target aborts. Targets do not assert SERR# when using target-abort termination.
STOP#	67	I, 3SR/6	**Stop.** An asserted STOP# signal indicates that the current target is requesting the master to stop the current data phase of a transaction in process. STOP#, once asserted, must remain asserted until FRAME# is de-asserted and data may or may not be transferred in the final data phase of the transaction. The turn-around PCLK period for STOP# is the address phase of a transaction.

Table 2- 11 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
Host Interface			
TRDY#	64	I, 3ST/6	**Target Ready#.** When this signal is asserted, this indicates that the current slave's ability to complete the current data phase of a transaction. During a read, TRDY# indicates that the slave is asserting valid data on AD[31:00]. During a write, it indicates that the slave is prepared to accept data. It is used in conjunction with IRDY#. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. Wait cycles should be minimized when more than eight are expected. Except for the first transfer, the transaction should be disconnected by the target and retried by the master. A data phase is completed on any PCLK when IRDY# and TRDY# are both sampled asserted. The turn-around PCLK period for TRDY# is the address phase of a transaction.
IRQA#	95	3ST/4	**Interrupt Request A.** IRQA# assertion state changes are synchronized to PCLK for PCI type errors and parity errors. Dagger interrupt conditions cannot assert IRQA when the INTEN bit is not active or the POWRDN bit is active in the HCNTRL register. For IRQA# assertion conditions, see INSTAT register. Note that IRQA output is floated when RST# is asserted.
SCSI Interface			
SCD(15:0)#	15, 16, 18, 19, 144, 145 146, 149, 3-5, 7-9, 11,13	I, NOD/48	**SCSI Data [15:0]#.** The SCSI data lines drive the ID during arbitration and selection, command and data information, as well as status and messages.
SCDPH#	14	I, NOD/48	**SCSI High Byte Parity.** This bit supports odd parity for SCD[15:8]#.
SCDPL#	1	I, NOD/48	**SCSI Low Byte Parity.** This bit supports odd parity for SCD[7:0].
CD#	150	I, NOD/48	**Command Data.** This control line is received when in Initiator mode or driven when in Target mode. It indicates Command or Message phase when asserted, and Data phase when de-asserted. This control signal is used for 8 or 16 bit transfers.
IO#	148	I, NOD/48	**In/Out.** This control line is received when in Initiator mode or driven when in Target mode. It indicates the In direction when asserted, and the Out direction when de-asserted. This control signal is used for 8 or 26 bit transfers.

Table 2- 11 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
SCSI Interface			
MSG#	153	I, NOD/48	**Message#.** This control line is received when in Initiator mode or driven when in Target mode. It indicates a Message phase when asserted, and a Command or Data phase when de-asserted. This control signal is used for 8 or 16 bit transfers.
REQ#	152	I, NOD/48	**Request#.** This control line is received by the device when in Initiator mode and driven when in Target mode. A Target asserts REQ# to indicate that a byte is ready or is needed by the Target. This control signal is used for 8 or 16 bit transfers.
ACK#	156	I, NOD/48	**Acknowledge#.** This control line is received by the device when in Target mode, and driven when in Initiator mode. An Initiator asserts ACK# to indicate that a byte is ready for or is received from the target. This control signal is used for 8 or 16 bit transfers.
RESET#	158	I, NOD/48	**Reset#.** This line is received and/or driven. It is interpreted as a hard reset and clears all commands pending on the SCSI bus. This control signal is used for 8 or 16 bit transfers.
SEL#	154	I, NOD/48	**Select#.** This line is driven after a successful arbitration to select as an Initiator or re-select as a Target, and otherwise it is received. This control signal is used for 8 or 16 bit transfers.
BSY#	159	I, NOD/48	**Busy#.** This line is driven by the Initiator as a handshake during arbitration and received for the rest of the transfer. As a target, it is driven also as a handshake during arbitration and then is driven for the rest of the transfer.
ATN#	160	I, NOD/48	**Attention#.** This line is driven as an Initiator when a special condition occurs. It is received by the target. This control signal is also used for 16 bit transfers.
DIFFADR[1:0]	43, 42	3ST/4	**Differential Control Address.** This line determines the meaning of DIFFDAT[3:0]. This control signal is used for 8- or 16-bit data transfers.
DIFFDAT[3:0]	69, 66, 61, 54	3ST/4	**Differential Control Data.** These lines contain information latched by outside circuitry to control differential drivers. The definition of these bits depends on the value of DIFFADR[1:0]. This control signal is used for 8- or 16-bit data transfers.

Table 2- 11 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
SCSI Interface			
DIFFSTRB#	50	3ST/4	**Differential Control Strobe.** This signals clocks the data from DIFFDAT into the addressed latch specified by DIFFADR on the rising edge. Both DIFFDAT and DIFFADR are stable for the duration of DIFFSTRB#. This control signal is used for 8- or 16-bit transfers.
LED#	142	3ST/4	**LED#.** The LED# output has three functions: 1. To indicate that AIC-7880 is actively connected to the SCSI bus. LED asserted state is latched with the ORrf result of active bits SELINGO, SELDI, and SELDO in the SSTAT0 register and de-asserted by the following SCSI bus free condition. LED# may be used to supply the system status of AIC-7880 SCSI bus activity and may directly drive an indicator (LED) provided that the current is limited to a maximum of 20 Ma. 2. As a clock to shift in an external device ID value from input IDDAT, to replace the internal default device ID value. This use of LED# is triggered as a result of RST# assertion. 3. For diagnostic support or general purpose output control bit. Note that LED# output is floated when RST# is asserted.
WIDEPS#	99	I	**Wide Present#.** Then asserted (=0), this signal indicates that a wide (16-bit) cable connector is present. WIDEPS# input contains an internal pullup and only needs to be connected for 16-bit operations.
STPWCTL	141	3ST/4	**SCSI Termination Power Down Control.** This supports the capability to enable or disable the external SCSI bus termination power source. The enable/disable polarity of STPWCTL may be selected with the STPWLEVEL bit in the Configuration DEVCONFIG register and the actual enable/disable state is selected with the STPWEN bit in the device SXFRCTL1 register. CHIPRST forces STPWCTL to the selected disabled state and STPWEN to the inactive state. RST# assertion forces STPWCL to be floated and both STPWLEVEL and STPWEN to be inactive. STPWCL may also be used for a general purpose output control bit.

Table 2- 11 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
Memory Port Interface			
EXTARBACK#	21	I	**External Arbitration Acknowledge** is a status input to AIC-7880 with an internal pullup. When EXTARBACK# is asserted low in response to AIC-7880's asserted EXTARBREQ# output, it indicates to the AIC-7880 that it may drive its memory port outputs and access external memory devices. EXTARBACK# remains asserted until some other user needs access to the memory port external shared memory devices which is detected by the external memory port arbitrator.
MDP	137	I, 3ST/8	**Memory Data Parity** is optionally used for parity protection of SCB data stored in the external SRAM 99-bit device). Odd parity data are always generated and parity checking is enabled when EXTSCBPEN is active in the configuration DEVCONFIG register. MDP is in a float condition and become driven only after EXTARBACK# is asserted due to AIC-7880 EXTARBREQ# being asserted or when MPORTMODE is active. It is driven when a write access is to be performed. MDP output is floated during and following assertion of RST#. When the external SRAM is an 8-bit device, EXTSCBPEN must be inactive.
MRW	119	3ST/24	**Memory Port Read Write** is driven when AIC-7880 has been granted the arbitration for an access to the external SRAM/ROM/EEPROM memory devices. A read cycle results when output MRW is at a high level (=1), while RAMCS# or RMCS# is asserted. A write cycle results when output MRW is a t low (=0), while RAMCS/ROMCS# is asserted. A read cycle, a write cycle, or a read-modify-write cycle may be performed by the sequencer with memory port timed control of MRW and RAMCS# in a single sequencer instruction cycle access of the memory port. AIC-7880 as a target may only perform a read or a write cycle access through the memory port with timing following the source of the access time. MRW is in a float condition and is driven only after EXTARBACK# is asserted due to AIC-7880 EXTARBREQ# being asserted or when MPORTMODE is active. MRW is floated during and flowing assertion of RST# or a write to CHIPRESET=1.

Table 2- 11 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
Memory Port Interface			
RAMCS#	117	3ST/24	**RAM Chip Select#** is driven when ACI-7880 has been granted the arbitration for an access to the external memory SRAM device and is asserted (=0) for an access to the external SRAM. RAMCS# is in a float condition and is driven only after EXTARBACK# is asserted due to AIC-7880 EXTARBREQ# being asserted or when MPORTMODE is active. RAMCS# is floated during and following assertion of RST# or a write to CHIPRESET=1. The SRAM cycle access time is 20 nanoseconds.
ROMCS#	120	3ST/4	**ROM Chip Select#** is driven when AIC-7880 has been granted the arbitration for an access to the external ROM/EEPROM and is asserted (=0) for access of the external memory ROM/EEPROM device. ROMCS# is in a float condition and is driven only after EXTARBACK# is asserted due to AIC-7880 EXTARBREQ# being asserted or when MPORTMODE is active. ROMCS# is floated during and following assertion of RST# or a write to CHIPRESET=1. The cycle access time is hardware controlled for a 150-ns device. The external ROM control interface should be such that when MRW is low (write access) and ROMCS# is asserted, ROM data outputs are not enabled, then the cycle becomes a NOP with no contention with AIC-7880 driven MD[7:0] outputs.
SEECS	139	3ST/4	**Serial EEPROM Chip Select** output is asserted (=1) if SEEMS is active and AIC-7880 has been granted arbitration for an access to the external memory SEEPROM device. SEECS output may now be controlled by the state stored in bit SEECS in the SEECTL register. SEECS is in a float condition and is driven only after EXTARBACK# is asserted due to AIC-7880 EXTARBREQ# being asserted or when MPORTMODE is active. SEECS is floated while RST# is asserted or POR is active.

Table 2- 11 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
Memory Port Interface			
EXTARBREQ#	20	3ST/8	**External Arbitrator Request.** When asserted, this status output indicates to an external arbitrator that AIC-7880 requires access to the memory port external devices such as SRAM (SCB), ROM/EEPROM, SEEPROM, and other board control devices. All requests for the memory port access is delayed until access is initially granted with EXTARBACK# assertion. EXTARBREQ# remains asserted until EXTARBACK# is de-asserted and AIC-7880 is not performing an access before being de-asserted. When EXTREQLCK is active, it will not affect the assertion of EXTARBREQ#, but once EXTARBREQ# is asserted, it extends its assertion until EXTREQLCK is inactive. EXTARBREQ# output has high impedance during assertion of RST#.
MA[14:0]	111, 114, 108, 123, 124, 122, 121, 115, 113, 112, 109, 107, 106, 105, 103	3ST/8	**Memory Address [14:0]** are address bus outputs to the external memory devices. They are in a float condition and become driven only after EXTARBACK# is asserted due to AIC-7880 EXTARBREQ# being asserted or when MPORTMODE is active. They are driven continuously until EXTARBREQ# is de-asserted. MA[14:0] outputs have high impedance during assertion of RST#.
MD[7:0]	126-128, 130, 132-135	I, 3ST/8	**Memory Data [7:0]** is the memory port data bus. It is used to read or write external ROM/EEPROM byte data when AIC-7880 is a target, to read or write external SRAM SCB page byte data by the sequencer or by the driver when AIC-7880 is a target, to read or write external SEEPROM bit data or board control device data by the sequencer or by the driver when AIC-7880 is a target. The are in a float condition and become driven only after EXTARBACK# is asserted or when MPORTMODE is active due to AIC-7880 EXTARBREQ# being asserted and a write process is to be performed. MD[7:0] outputs have high impedance during assertion of RST#.

Table 2- 11 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
Memory Port Interface			
RAMPS#	98	I, 3ST/4	**RAM Present#** is asserted (=0) to enable access of an external SRAM for expanded SCB array data storage. When RAMPS# is de-asserted the internal AIC-7880 SCB array RAM is used for SCB storage of 16 SCBs (0-15), the SCBPTR register maximum stored value is restricted to 1Fh, and the QINFIFO/QINCNT/ QOUTFIFO/QOUTCNT storage and count (0=empty, 16=full) supports only 16 SCBs. When RAMPS# is asserted, an external SRAM is required. The size of the SRAM is 4 KB for 128 SCBs and 8 KB for 256 SCBs. The software driver must scan to determine the actual installed SRAM size.
Miscellaneous			
IDDAT	96	I	**Identification Data.** This input signal performs the shifting-in of an external device ID value to replace the internal default device ID value readable from the DEVICEID1 configuration register or the DSDEVID1 device register. The external IDDAT data source should be initialized with the desired identification data to be shifted-in when RST# is asserted. The loaded data will be shifted with the rising edge of 8 IDDAT shift clocks supplied on LED# commencing (2 to 3 CLKINs) after sampling RST# is de-asserted. LED# transitions after the 8 IDDAT shift clocks are ignored by the IDDAT data load logic.
CLKIN	101	I	**Input Clock Frequency.** Standard input (Dagger) - 40 MHz nominal input frequency. This is used internally by the SCSI, sequencer, DFIFO, memory port, and the PCI host blocks for timing.
Power Distribution / Core Logic Power Pins			
Only pin 23 is connected to and utilizes power supplied by the Core Logic pins.			
CVCC[3:0]	138, 100, 60, 24	PWR	**Core Logic Positive Voltage Supply, +5V**
CGND[3:0]	140, 102, 58, 22	PWR	**Core Logic Ground**
Power Distribution / SCSI Interface Power Pins			
The following external pins are connected to and utilize power supplied by these power pins: SCD[15:0]#, SCDPH#, SCDPL#, CD#, IO#, MSG#, REQ#, ACK#, RESET#, SEL#, BSY#, ATN#, LED#, STPWCTL.			
SVCC [2:0]	10, 155, 147	PWR	**SCSI Bus Driver Positive Voltage Supply**
SGND [5:1]	17, 12, 6, 2, 157, 151, 143	PWR	**SCSI Bus Driver Ground**

Table 2- 11 AIC 7880 Signal Descriptions

Signal	Pin	Type	Description
Power Distribution / PCI Interface Power Pins			
The following external pins are connected to and utilize power supplied by the PVCC power pins: AD[31:00], CBE[3:0]#, CLKIN, DEVSEL#, FRAME#, GNT#, IDSEL#, IRDY#, PAR#, PCLK, PERR#, PREQ#, RST#, SERR#, STOP#, TRDY#, IRQA#, DIFFDAT[3:0], DIFFADR[1:0], DIFFSTRB#, EXTARBREQ#, EXTARBACK#.			
PVCC[3:0]	86, 73, 51, 35	PWR	**PCI Bus Driver Positive Voltage Supply**
The following external pins are connected to and utilize power supplied by the PGND power pins: AD[31:00], CBE[3:0]#, CLKIN, DEVSEL#, FRAME#, GNT#, IDSEL#, IRDY#, PAR#, PCLK, PERR#, PREQ#, RST#, SERR#, STOP#, TRDY#, IRQA#, DIFFDAT[3:0], DIFFADR[1:0], DIFFSTRB#, WIDEPS#, MD[7:0], MDP, MA[14:0], ROMCS#, RAMCS#, MRW, RAMPS#, SEECS, IDDAT, EXTARBREQ#, EXTARBACK#.			
PGND [14:0]	136, 131, 125, 118, 110, 97, 91, 84, 78, 71, 62, 55, 47, 39, 32	PWR	**PCI Bus Driver Ground**
Power Distribution / Memory Port Interface Power Pins			
The following external pins are connected to and utilize power supplied by this power pin: IRQA#, WIDEPS#, MD[7:0], MDP, MA[14:0], ROMCS#, RAMCS#, MRW, RAMPS#, SEECS, IDDAT.			
MVCC[2:0]	129, 116, 104	PWR	**Memory Port Bus Driver Positive Voltage Supply**

2.7 Intel S82093

While the standard ISA Compatible interrupt controller (located in the PIIX3) is intended for use in a uni-processor system, the I/O Advanced Programmable Interrupt Controller (IOAPIC) can be used in either a uni-processor or multiprocessor system. The IOAPIC provides multiprocessor interrupt management and incorporates both static and dynamic symmetric interrupt distribution across all processors. In systems with multiple I/O subsystems, each subsystem can have its own set of interrupts.

In a uni-processor system, the IOAPIC's dedicated interrupt bus can reduce interrupt latency over the standard interrupt controller (i.e., the latency associated with the propagation of the interrupt acknowledge cycle across multiple busses using the standard interrupt controller approach). Interrupts can be controlled by the standard ISA Compatible interrupt controller in the PIIX3, the IOAPIC unit, or mixed mode where both the standard ISA Compatible Interrupt Controller and IOAPIC are used. The selection of which controller responds to an interrupt is determined by how the interrupt controllers are programmed. Note that it is the programmer's responsibility to make sure that the same interrupt input signal is not handled by both interrupt controllers.

At the system level, APIC consists of two parts (Figure 2.0)—one residing in the I/O subsystem (called the IOAPIC) and the other in the CPU (called the Local APIC). The local APIC and the IOAPIC communicate over a dedicated APIC bus. The IOAPIC bus interface consists of two bi-directional data signals (APICD[1:0]) and a clock input (APICCLK).

The CPU's Local APIC Unit contains the necessary intelligence to determine whether or not its processor should accept interrupts broadcast on the APIC bus. The Local Unit also provides local pending of interrupts, nesting and masking of interrupts, and handles all interactions with its local processor (e.g., the INTR/INTA/EOI protocol). The Local Unit further provides inter-processor interrupts and a timer, to its local processor. The register level interface of a processor to its local APIC is identical for every processor.

The IOAPIC Unit consists of a set of interrupt input signals, a 24-entry by 64-bit Interrupt Redirection Table, programmable registers, and a message unit for sending and receiving APIC messages over the APIC bus. I/O devices inject interrupts into the system by asserting one of the interrupt lines to the IOAPIC. The IOAPIC selects the corresponding entry in the Redirection Table and uses the information in that entry to format an interrupt request message. Each entry in the Redirection Table can be individually programmed to indicate edge/level sensitive interrupt signals, the interrupt vector and priority, the destination processor, and how the processor is selected (statically or dynamically). The information in the table is used to transmit a message to other APIC units (via the APIC bus).

The IOAPIC contains a set of programmable registers. Two of the registers (I/O Register Select and I/O Window Registers) are located in the CPU's memory space and are used to indirectly access the other APIC registers as described in Section 3.0, Register Description. The Version Register provides the implementation version of the IOAPIC. The IOAPIC ID Register is programmed with an ID value that serves as a physical name of the IOAPIC. This ID is loaded into the ARB ID Register when the IOAPIC ID Register is written and is used during bus arbitration.

The interrupt number or the vector does not imply a particular priority for being sent. The IOAPIC continually polls the 24 interrupts in a rotating fashion, one at a time. The pending interrupt polled first is the one sent.

2.7.1 Features

- Provides Multiprocessor Interrupt Management
  - Dynamic Interrupt Distribution-Routing Interrupt to the Lowest Priority Processor
  - Software Programmable Control of Interrupt Inputs
  - Off Loads Interrupt Related Traffic From the Memory Bus
- 24 Programmable Interrupts
  - 13 ISA Interrupts Supported
  - 4 PCI Interrupts
  - 1 Interrupt/SMI# Rerouting
  - 2 Motherboard Interrupts
  - 1 Interrupt Used for INTR Input
  - 3 General Purpose Interrupts
  - Independently Programmable for Edge/Level Sensitivity Interrupts
  - Each Interrupt Can Be Programmed to Respond to Active High or Low Inputs
- X-Bus Interface
  - CS For Flexible Decode of the IOAPIC Device.
  - Index Register Interface for Optimum Memory Usage
  - Registers are 32-Bit Wide to Match the PCI to Host Bridge Architecture
- Package 64-Pin PQFP

2.7.2 Block Diagram

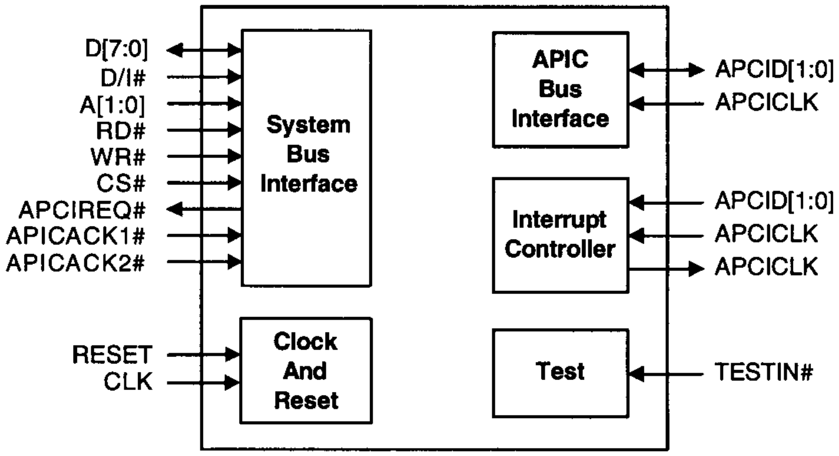


Figure 2- 15 S82093 Block Diagram

2.7.3 Pin Diagram

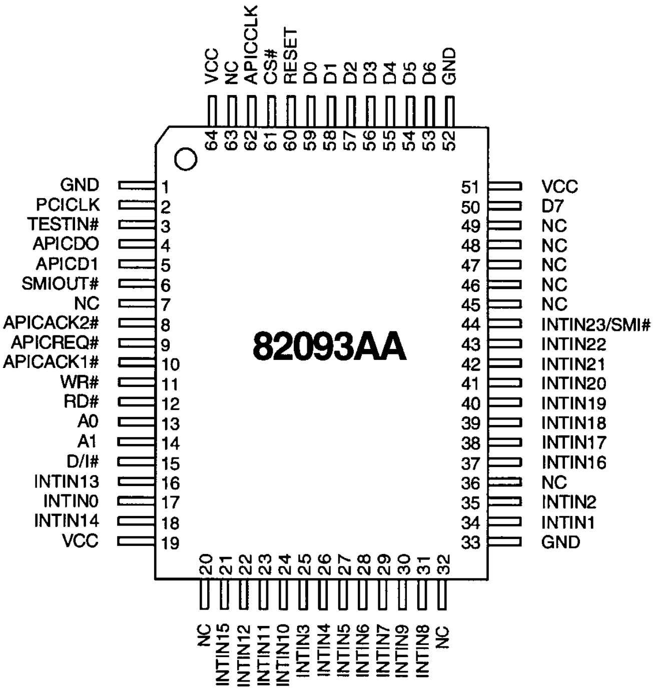


Figure 2- 16 S82093 Pin Diagram

2.7.4 Signal Descriptions

Table 2- 12 S82093 Signal Descriptions

Pin Type	Description
I	Input pin
O	Output pin
ST	Schmitt Trigger Input pin
OD	Open Drain Output pin. This requires a pull-up to the VCC of the processor core
I/OD	Bi-directional Input withOpen Drain Output pin.
I/O	Bi-directional Input/Output pin

Table 2- 13 S82093 Signal Descriptions

Signal	Pin	Type	Description
System Bus Signals			
D[7:0]	50, 53, 54, 55, 56, 57, 58, 59	I/O	DATA: D[7:0] contain the data when writing to or reading from internal IOAPIC registers. These signals are outputs when reading data from the IOAPIC and they are inputs when writing data to the IOAPIC. These signals are tri-stated during reset.
D/I#	15	I	DATA/INDEX#: This input selects whether the I/O Register Select (IOREGSEL) Register or I/O Window (IOWIN) Register is accessed. All internal IOAPIC registers are accessed with an indexing scheme. When the D/I# pin is low, the IOREGSEL Register is accessed. When the D/I# pin is high, the data becomes available from the register pointed to by the index register. Typically, this signal is connected to SA4 on the ISA bus (i.e., IOREGSEL Register is at 00h and IOWIN Register is at 10h).
A[1:0]	14, 13	I	ADDRESS: The IOAPIC is a 32 bit device with an 8 bit ISA interface. A[1:0] steer the data byte to the correct 8 bit location within the 32 bit register. Typically, these input signals are connected to SA[1:0] of the ISA bus.
RD#	12	I	READ STROBE: RD# causes the IOAPIC to respond by driving internal register data onto the D[7:0] pins. Typically this pin is connected to the MEMRD# signal on the ISA bus.
WR#	11	I	WRITE STROBE: When this signal transitions from low to high, the data present on the IOAPIC's D[7:0] signals are written to an internal register. Typically, this signal is connected to the MEMWR# signal on the ISA bus.
CS#	61	I	CHIP SELECT: This active low input selects the IOAPIC as the target of the current read or write transaction.

Table 2- 13 S82093 Signal Descriptions

Signal	Pin	Type	Description
System Bus Signals			
APICREQ#	9	O	APIC REQUEST: APICREQ# is asserted prior to the APIC sending an interrupt message over the APIC data bus. This is the request part of a handshake that insures system level buffer coherency prior to sending an interrupt over the APIC bus. This signal is tri-stated during reset. This signal has an internal pull-up resistor.
APICACK1#	10	I	APIC ACKNOWLEDGE 1: This signal is the acknowledge part of the handshake indicating that the APIC can send the interrupt message over the APIC bus. This signal is typically connected to the PIIX3.
APICACK2#	8	I	APIC ACKNOWLEDGE 2: This signal is the second half of the acknowledge handshake indicating that the APIC can send the interrupt message over the APIC bus. This signal is typically connected to the host-to-PCI bridge and along with APICREQ# and APICACK1# makes up the complete buffer coherency protocol cycles. If the system does not have a host-to-PCI bridge, this signal can be tied low.
Clock and Reset Signals			
PCICLK	2	I	PCI CLOCK: This signal is used to synchronize and strobe the data buffer status signals (APICREQ#, APICACK1#, and APICACK2#). This signal is typically connect to the PCI clock.
RESET	60	I	RESET: RESET initializes the IOAPIC’s internal logic and sets the register bits to their default value.
APIC Bus Interface			
APICD[1:0]	5, 4	I/OD	APIC DATA: These signals are used to send and receive data over the APIC bus. These signals are tri-stated during reset and must be pulled up to the appropriate VCC levels of the CPU.
APICCLK	62	I	APIC CLOCK: The input signal is used to determine when valid data is being sent over the APIC bus.
Interrupt Signals			
INTIN0	17	ST	Interrupt Input 0: This signal is connected to the redirection table entry 0. Typically, this signal may be connected to the INTR on the PIIX3 to communicate the status of IRQ0 and IRQ13 interrupts. Note that the IRQ0 and IRQ13 interrupts are embedded in the PIIX3 and are not available to the rest of the system.
INTIN1	34	ST	Interrupt Input 1: INTIN1 is connected to the redirection table entry 1. Typically, this signal will be connected to the keyboard interrupt (IRQ1).

Table 2- 13 S82093 Signal Descriptions

Signal	Pin	Type	Description
Interrupt Signals			
INTIN2	35	ST	Interrupt Input 2: This signal is connected to the redirection table entry 2. If IRQ0 interrupt is available in hardware, it is connected to this pin.
INTIN[3:11, 14,15]	25, 26, 27, 28, 29, 31, 30, 24, 23, 18, 21	ST	Interrupt Inputs 3 through 11, 14 and 15: These signals are connected to the redirection table entries 3:11, 14 & 15. Typically, these signals are connected to the ISA interrupts IRQ[3:7,8#,9:11,14:15] respectively.
INTIN12	22	ST	Interrupt Input 12: This signal is connected to the redirection table entry 12. Typically, this signal will be connected to the mouse interrupt (IRQ12/M).
INTIN13	16	ST	Interrupt input 13: This signal is connected to the redirection table entry 13. If IRQ13 interrupt is available in hardware, it is connected to this signal. If IRQ13 is not available, it is routed through the INTR interrupt and this signal becomes INTIN13 (redirection table entry 13).
INTIN[16:19]	37, 38, 39, 40	ST	Interrupt inputs 16 through 19: These signals are connected to the redirection table entries [16:19]. Typically, these signals are connected to the PCI interrupts (PIRQ[0:3]). The steering of the PCI IRQs to the ISA IRQs is accomplished in the IOAPIC by setting the PCI redirection table entry to the correct ISA interrupt vector.
INTIN[20:21]	41, 42	ST	Interrupt inputs 20 and 21: These signals are connected to the redirection table entries 20 and 21. Typically, these signals are connected to the motherboard interrupts (MIRQ[0:1]). These pins could be used for the NMI and INIT signals or just general purpose interrupts.
INTIN22	43	ST	Interrupt input 22: This signal is connect to the redirection table entry 22. This signal is a general purpose interrupt.
INTIN23/SMI#	44	ST	Interrupt input 23: This signal is connected to the redirection table entry 23. This input has a special feature for the SMI# interrupt routing. If the Mask bit is not set, the signal is a normal interrupt input that is sent over the APIC bus just like all the other interrupts. When the Mask bit is set, the INTIN23/SMI# input is routed through the IOAPIC to the SMIOUT# output signal.
SMIOUT#	6	OD	SMI OUTPUT: This signal is an output in response to the SMI# input when the MASK bit for the redirection table entry number 23 is set. If the MASK bit is not set, the redirection table can be setup to deliver an SMI# over the APIC bus.

Table 2- 13 S82093 Signal Descriptions

Signal	Pin	Type	Description
Test and Power Signals			
TESTIN#	3	I	TEST INPUT: This active-low input is used to invoke test modes. TESTIN# should be pulled high during normal operation.
VCC	19, 51, 64		VCC POWER PIN: 5V ± 10%.
GND	1, 33, 52		GROUND POWER PINS
NC	7, 20, 32, 36, 45, 46, 47, 48, 49, 63		NON-CONNECTED PINS

2.8 Intel S82557

The 82557 is Intel's first highly-integrated 32-bit PCI LAN controller for 10 Mbps or 100 Mbps Fast Ethernet networks. The 82557 offers a high-performance LAN solution while maintaining low-cost through its high-integration. It contains a 32-bit PCI bus master interface to fully utilize the high bandwidth available (up to 132 Mbs) to masters on the PCI bus. The bus master interface can eliminate the intermediate copy step in Receive (RCV) and Transmit (XMT) frame copies, resulting in faster processing of these frames. Though the 82557 maintains a similar memory structure to the Intel 82596 LAN coprocessor, its memory structures have been streamlined for better network operating system (NOS) interaction and improved performance.

The 82557 contains two large receive and transmit FIFOs that prevent data overruns or underruns while waiting for access to the PCI bus, as well as enabling back-to-back frame transmission within the minimum 960 ns interframe spacing. Full support for up to 1 MB of Flash enables network management support via Intel FlashWorks utilities as well as remote boot capability (a BIOS extension stored in the Flash which could allow a node to boot itself off of a network drive). For 100 Mbps applications, the 82557 contains an IEEE MII compliant interface to the Intel 82553 serial interface device (or other MII compliant PHYs) which will allow connection to 100 Mbps/10 Mbps networks. For 10 Mbps networks, the 82557 can be interfaced to a standard ENDEC device (such as the Intel 82503 Serial Interface), while maintaining software compatibility with 100 Mbps solutions.

The 82557 is designed to implement cost-effective, high-performance PCI add-in adapters, PC mother boards, or other interconnect devices such as a hubs or bridges. Its combination of high integration and low cost make it ideal for these applications.

The 82557 has two interfaces: the host system PCI bus interface and the serial or network interface. The network interface complies to the IEEE standard for 10Base-T, TX, and T4 Ethernet interfaces. The 82557 also complies to the PCI Bus Specification, Revision 2.1.

2.8.1 Features

The following list summarizes the main features of the Intel 82557 controller:

- Glueless 32-bit PCI bus master interface (Direct Drive of Bus), compatible with PCI Bus Specification, Revision 2.1
- 82596-like chained memory structure
- Improved dynamic transmit chaining for enhanced performance
- Programmable transmit threshold for improved bus utilization
- Early receive interrupt for concurrent processing of receive data
- Flash support up to 1 MB
- Large on-chip receive and transmit FIFOs
- On-chip counters for network management
- Back-to-back transmit at 100 Mbps EEPROM support

- Support for both 10 Mbps and 100 Mbps networks
- Interface to MII-compliant PHY devices, including Intel 82553 Physical interface component for 10 Mbps/100 Mbps designs
- IEEE 802.3 100Base-T, TX, and T4 compatible
- Interface to Intel 82503 or other serial device for 10 Mbps designs: IEEE 802.3 10Base-T compatible
- Auto-detect and auto-switching for 10 Mbps or 100 Mbps network speeds
- Full- or half-duplex capabilities at 10 Mbps and 100 Mbps
- 160-lead QFP package

2.8.2 Block Diagram

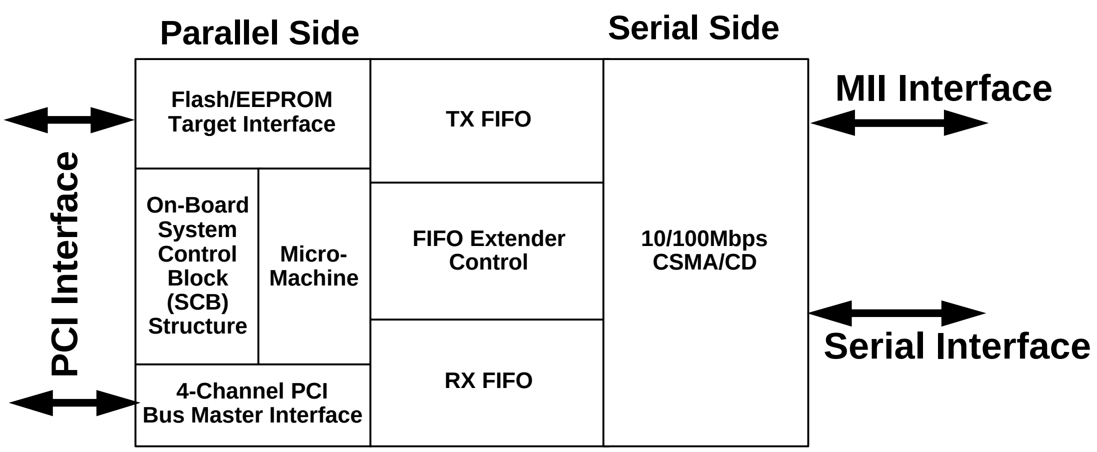


Figure 2- 17   82557   Block Diagram

2.8.3 Pin Diagram

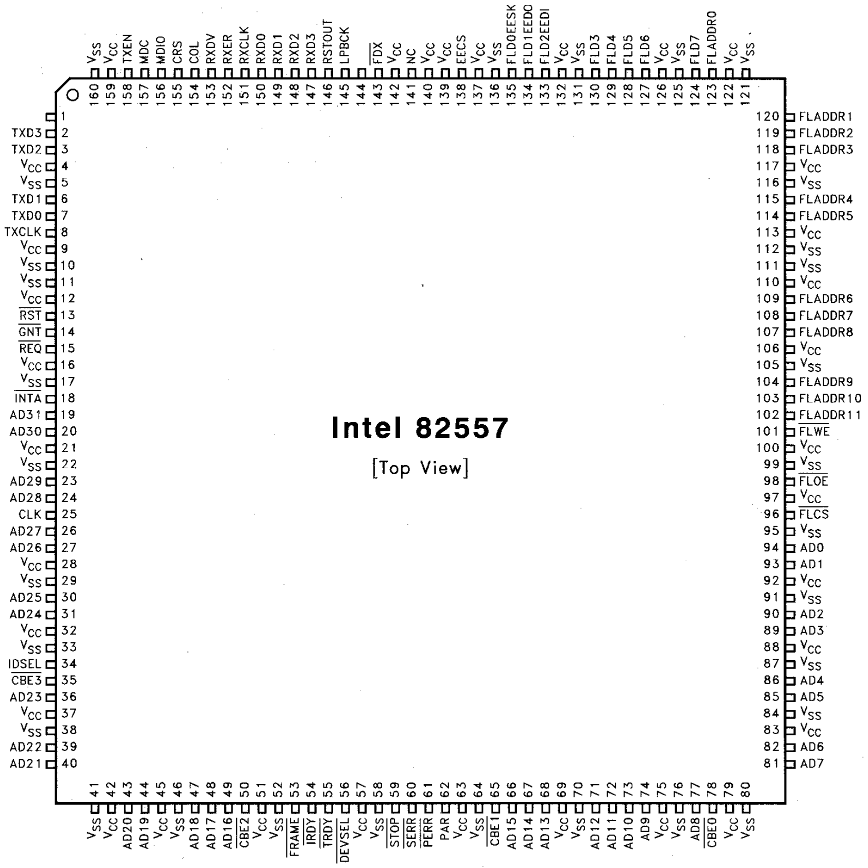


Figure 2- 18 82557 Pin Diagram

2.8.4 Signal Descriptions

Table 2- 14 82557 Signal Descriptions

Signal	Pin	Type	Description
Address and Data Signals			
ADO AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 |AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31	94 93 90 89 86 85 82 81 77 7473 72 7168 67 66 49 48 47 44 43 40 39 36 31 30 27 26 24 23 20 19	TS	Address and Data are multiplexed on the same PCI pins by the 82557. A bus transaction consists of an address phase followed by one or more data phases. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD0-31 contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory it is a DWORD address. The 82557 used "Little Endian" byte ordering. During data phases AD0-7 contain the least significant byte (LSB) and AD24-31 contain the most significant byte (MSB).
CBE0# CBE1# CBE2# CBE3#	78 65 50 35	TS	Bus Command and Byte Enables are multiplexed on the same PCI pins by the 82557. During the address phase of a transaction, C/BE0-3# define the bus command. During the data phase C/BE0-3# are used as Byte Enables. The Byte Enables are valid for the entire data phase and capable of determining which byte lanes carry meaningful data. The C/BE0# applies to byte 0 (LSB) and C/BE3# applies to byte 3 (MSB).

Table 2- 14 82557 Signal Descriptions

Signal	Pin	Type	Description
Address and Data Signals			
PAR	62	TS	Parity is even parity across AD0-31 and C/BE0-3#. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. When the 82557 is a bus master, it drives PAR for address and write data phases. As a slave, it drives PAR for read data phases.
Interface Control Signals			
FRAME#	53	STS	FRAME# is driven by the 82557 to indicate the beginning and duration of an access. FRAME# is asserted to indicate that a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase.
IRDY#	54	STS	Initiator Ready# indicates the ability of the 82557 (as a bus mastering device) to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock in which both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD0-31. During a read, it indicates that the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. The 82557 drives IRDY# when acting as a master and samples it when acting as a slave.
TRDY#	55	STS	Target Ready# indicates the ability of the 82557 (as a selected device) to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock in which both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD0-31. During a write, it indicates that the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. The 82557 drives TRDY# when acting as a slave and samples it when acting as a master.

Table 2- 14 82557 Signal Descriptions

Signal	Pin	Type	Description
Interface Control Signals			
STOP#	59	STS	STOP# indicates the current target is requesting the master to stop the current transaction. As a slave, the 82557 drives STOP# to inform the bus master to stop the current transaction. As a bus master, the 82557 receives STOP# from the slave and stops the current transaction.
IDSEL	34	IN	Initialization Device Select is used by the 82557 as a chip select during configuration read and write transactions.
DEVSEL#	56	STS	Device Select#, when actively driven by the 82557 as a slave, indicates to the bus master that it has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
Error Reporting Signals			
SERR#	60	OD	System Error# is used by the 82557 to report address parity errors. SERR# is open drain and is actively driven for a single PCI clock when reporting the error.
PERR	61	STS	Parity Error# is used by the 82557 for reporting data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the 82557 receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected.
Interrupt Signal			
INTA#	18	OD	Interrupt A# is used to request an interrupt by the 82557. This is an active low, level-triggered interrupt signal.
Arbitration Signals			
REQ#	15	TS	Request# indicates to the arbiter that the 82557 desires use of the bus. This is a point-to-point signal. Every master has its own REQ.
GNT#	14	IN	Grant indicates to the 82557 that access to the bus has been granted. This is a point-to-point signal.

Table 2- 14 82557 Signal Descriptions

Signal	Pin	Type	Description
System Signals			
CLK	25	IN	Clock provides timing for all transactions on the PCI bus and is an input to the 82557 All other PCI signals, except RST and the INT lines are sampled on the rising edge of CLK and all other timing parameters are defined with respect to this edge.
RST#	13	IN	Reset# is used to bring PCI-specific registers, sequencers and signals to a consistent state. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be tri-stated and SERR# (open drain) is floated. To prevent AD, C/BE# and PAR signals from floating during reset, the central device may drive these lines during reset (bus parking). But to a logic low-level, these signals may not be driven high.
Local Memory Interface			
EECS	138	OUT	The EEPROM Chip Select is an active high signal used to assert Chip Select to the Serial EEPROM.
FLD0EESK	135	TS	Multiplexed pin. During flash access, this signal acts as Flash Data 0 input/output. During EEPROM access, it acts as EEPROM SHIFT.CLOCK output to shift data into and out of the serial EEPROM.
FLD1EEDO	134	TS	Multiplexed pin. During flash access, this signal acts as Flash Data 1 input/output. During EEPROM access, it acts as the input EEPROM DATA OUT.
FLD2EEDI	133	TS	Multiplexed pin. During flash access, this signal acts as Flash Data 2 input/output. During EEPROM access, it acts as the output EEPROM DATA IN.
FLD3 FLD4 FLD5 FLD6 FLD7	130 129 128 127 124	TS	Flash Data 7 to 3 input/outputs
FLCS#	96	OUT	Flash CS is normally high to disable access to the Flash. Whenever a Flash high address is to be latched, FLCS# goes low, thus latching the data in the latch and enabling the Flash. FLCS# should be connected to both the ENABLE pin on the external address latch and the CE# pin on the Flash.

Table 2- 14 82557 Signal Descriptions

Signal	Pin	Type	Description
Local Memory Interface			
FLOE#	98	OUT	This output provides the active low Output Enable control to the Flash.
FLWE#	101	OUT	This output provides the active low Write Enable control to the Flash.
FLADDR0 FLADDR1 FLADDR2 FLADDR3 FLADDR4 FLADDR5 FLADDR6 FLADDR7 FLADDR8 FLADDR9 FLADDR10 FLADDR11	123 120 119 118 115 114 109 108 107 104103102	OUT	Flash Address 11 to 0. These signals work in conjunction with an external 8-bit Address Latch to control the Flash addressing up to 1 MB. The 8 most significant Flash address pins (FLADDR11 to 4) should be connected to both the Address Latch and to Address Pins 11 to 4 of the Flash. The Address Latch provides the upper 8 bits, 19 to 12, of address to the Flash and is loaded by assertion of the FLCS# pin.
MII/Serial Interface Signals			
RXCLK	151	IN	Receive Clock input operates at either 25 MHz, 2.5 MHz (MII Mode), or 10 MHz (10 Mbps-only mode).
RXD0 RXD1 RXD2 RXD3	150 149 148 147	IN	Receive Data signals are the nibble wide receive data inputs in MII mode. In 10 Mbps only mode, RXD0 is the serial receive data input.
RXDV	153	IN	Receive Data Valid indicates that valid data is present on the RXD lines. This is used for MII mode only. When this signal is inactive (low), receive data is not sampled by the 82557.
RXER	152	IN	Receive Data Error indicates that an invalid symbol has been detected inside a receive packet. MII mode only.
Reserved	1	-	No connection
CRS	155	IN	Carrier Sense signal indicates traffic on the wire.
TXCLK	8	IN	Transmit Clock input that operates at either 25 MHz, 2.5 MHz (MII Mode), or 10 MHz (10 Mbps-only mode).
TXD0 TXD1 TXD2 TXD3	7 6 3 2	OUT	Transmit Data signals are the nibble wide transmit data outputs in MII mode. However, in 10 Mbps mode, only the TXD0 is the serial transmit data output signal.
RTS/TXEN	158	OUT	Request To Send signal indicates that the 82557 has a frame pending for transmission (10 Mbps-only mode). Transmit Enable signal indicates that the 82557 is transferring data to the PHY (MII mode).

Table 2- 14 82557 Signal Descriptions

Signal	Pin	Type	Description
MII/Serial Interface Signals			
COL	154	IN	Collision Detect signal indicates that a collision has been detected on the wire. In Full Duplex mode, assertion of COL indicates a Congestion condition has occurred.
Reserved	144	IN	Ties high with a 3.3-Kohm pull-up resistor
RSTOUT	146	OUT	This is the Reset Out signal to the PHY. This signal is driven high during H/W reset of the 82557.
LPBCK	145	OUT	Loopback controls the PHY into loopback mode
FDX#	143	IN	Full Duplex is an input from the physical layer component that indicates if it has switched into or out of full duplex mode. FDX# is active low.
FULHAL	6	OUT	When active, this signal indicates that 82557 is in full duplex mode. This is multiplexed with the TXD1 pin and operates only when in 10 Mbps mode.
MDIO	156	TS	Management Data Input / Output. Bidirectional signal between the 82557 and an MII-compatible PHY. It is used to transfer control information and status between the 82557 and the PHY. Control information is driven by the 82557 on the MDIO synchronously to MDC and sampled synchronously by PHY. The status information is driven synchronously by PHY and sampled synchronously by 82557.
MDC	157	OUT	Management Data Clock. This is the timing reference for transfer of control information and status on the MDIO signal. The frequency of this clock is up to 2.5 MHz.
Power and Ground			
V_{CC}	4, 9, 12, 16, 21, 28, 32, 37, 42, 45, 51, 63, 69, 75, 79, 83, 88, 92, 97, 100, 110, 113, 117, 122, 126, 132, 137, 159	IN	Power: +5v +-5%
V_{SS}	5, 10, 11, 17, 22, 29, 33, 38, 41, 46, 52, 58, 64, 70, 76, 80, 84, 87, 91, 95, 99, 105, 111, 112, 116, 121, 125, 131, 136	IN	Ground: 0V

2.9 NS DP83223

The DP83223 Twisted Pair Transceiver is an integrated circuit capable of driving and receiving three-level (MLT-3) encoded data streams. The DP83223 Transceiver is designed to interface directly with National Semiconductor's Fast Ethernet and FDDI Chip Sets or similar Physical Layer silicon allowing low cost data links over copper based media. The DP83223 allows links of up to 100 meters over Shielded Twisted Pair (Type-1A STP) and Category-5 data grade Unshielded Twisted Pair (Cat-5 UTP) or equivalent. The DP83223 is available in a 28 pin PLCC package and a 32 pin PQFP package.

2.9.1 Features

- Compatible with ANSI X3.263 TP-PMD draft standard
- Allows use of Type 1 STP and Category 5 UTP cables
- Requires a single +5V supply
- Integrated transmitter and receiver with adaptive equal-ization circuit
- Isolated TX and RX power supplies for minimum noise coupling
- Loop back feature for board diagnostics
- Digitally Synthesized transmit signal transition time control for reduced EMI
- Programmable transmit voltage amplitude
- Suitable for 100BASE-TX Fast Ethernet and Twisted
- Pair FDDI applications

2.9.2 Block Diagram

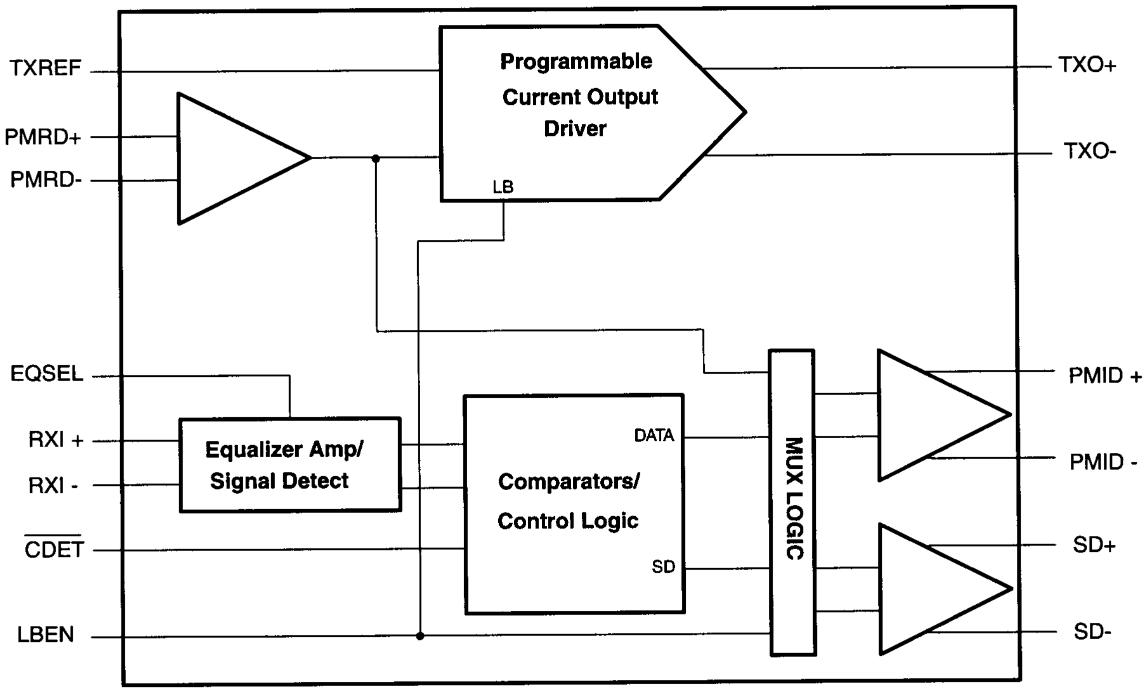


Figure 2- 19 DP83223 Block Diagram

2.9.3 Pin Diagram

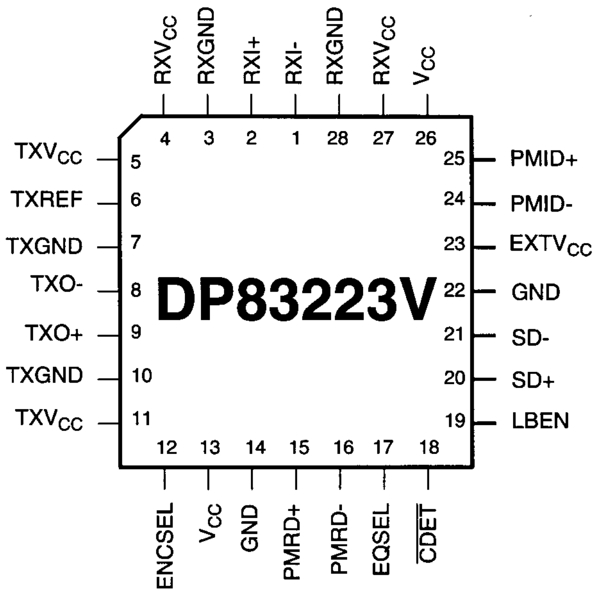


Figure 2- 20 DP83223 Pin Diagram

2.9.4 Signal Descriptions

Table 2- 15 DP83223 Signal Descriptions

Signal	Pin	Type	Description
Vcc	13,26	Supply	**Vcc:** Positive power supply for the ECL compatible circuitry. The Transceiver operates from a single +5VDC power supply.
GND	14, 22	Supply	**GND:** Return path for the ECL compatible circuitry power supply.
RXVcc	4, 27	Supply	**Receive Vcc:** Positive power supply for the small signal receive circuitry. This power supply is intentionally separated from others to eliminate receive errors due to coupled supply noise.
RXGND	3, 28	Supply	**Receive GND:** Return path for the receive power supply circuitry. This power supply return is intentionally separated from others to eliminate receive errors due to coupled supply noise.
TXVcc	5, 11	Supply	**Transmit Vcc:** Positive power supply required by the analog portion of the transmit circuitry. This power supply is intentionally separated from the others to prevent supply noise from coupling to the transmit outputs.
TXGND	7, 10	Supply	**Transmit GND:** Return path for the analog transmit power supply circuitry. This supply return is intentionally separated from others to prevent supply noise from being coupled to the transmit outputs.
EXTVcc	23	Supply	**External Vcc:** Positive power supply for ECL output circuitry.
RXI+/-	2, 1	Differential Voltage In	**Receive Data Inputs:** Balanced differential line receiver inputs.
PMID+/-	25, 24	ECL Out	**Physical Media Indicate Data:** Differential ECL compatible outputs source the recovered receive data back to the Physical Layer device or to a separate clock recovery device.
PMRD+/-	15, 16	ECL In	**Physical Media Request Data:** Differential ECL compatible inputs which receive data from Physical Layer Device.
TXO+/-	9, 8	Differential Current Out	**Transmit Data Outputs:** Differential current driver outputs which drive MLT-3 encoded data over twisted pair cable. These outputs provide controlled rise and fall times designed to filter the transmitters output which helps to reduce associated EMI.
SD+/-	20, 21	ECL Out	**Signal Detect Outputs:** Differential ECL compatible Signal Detect outputs indicating that either a signal with the proper amplitude is present at the RXI+/- inputs or that loop back mode has been selected.

Table 2- 15 DP83223 Signal Descriptions

Signal	Pin	Type	Description
TXREF	6	Current Out	**Transmit Amplitude Reference:** Reference current pin allowing adjustment of TXO+/- transmit amplitude. By placing a resistor between this pin and GND, a reference current is setup which results in a given transmit amplitude for a given application.
ENCSEL	12	CMOS In	**Encode Select Input:** The TTL compatible CMOS Encode Select input controls the encoded state of the signal at the TXO+/- outputs. A logic low level at this input causes the TXO outputs to become MLT-3 encoded with the receiver programmed to accept MLT-3 encoded data. This is the recommended mode of operation. A logic high level causes the TXO pins to output standard two-level binary code and the receiver is conditioned to receive a two-level binary signal. The DP83223V does not guarantee this mode(binary) of operation.
LBEN	19	CMOS In	**Loopback Enable:** TTL compatible CMOS loopback Enable input pin selects the internal loopback path which routes the PMRD+/- data to the PMID+/- differential outputs and forces Signal Detect true. During loopback, data present at the RXI+/- inputs is ignored. However, binary data is still transmitted by the TXO+/- outputs (regardless of the state of the ENCSEL input). Loopback mode is selected when LBEN is forced high. Normal operation occurs when LBEN is forced low.
EQSEL	17	3-Level Select	**Equalization Select:** This three level Equalization Select input controls the mode of receiver equalization. Forcing a median voltage level, accomplished by allowing EQSEL to float, selects the adaptive equalization mode which automatically regulates the equalization effects based on signal degradation caused by the media. The other two levels are intended as test modes and are not a guaranteed mode of operation. Forcing a voltage less than 1.5V, selects full equalization which provides fixed equalization for a maximum length of cable. Forcing a voltage greater than 3.0V turns the receive equalizer off.
CDET	18	CMOS In	**Cable Detect Bar:** The active low Cable Detect CMOS input is provided to support the option of external Cable Detection circuitry (wire fault). With CDET low, the transceiver functions normally. With CDET high, the signal detect output is forced low which inhibits data reception by the PHY and the PMID outputs are forced to ECL static levels. The exception is in the case of loopback when the Signal Detect output is forced high regardless of all other conditions.

2.10 NS DP83840

The DP83840 is a physical layer device for Ethernet 10Base-T and 100Base-X using Category 5 Unshielded, Type 1 Shielded, and Fiber Optic cables. This VLSI device is designed for easy implementation of the 10/100 Mbs Ethernet LANs. It interfaces with the PMD sub-layer through the DP83223 twisted-pair transceiver from National Semiconductor (NS), and with the MAC layer through a media independent interface (MII), ensuring compatibility between products from different vendors. The DP83840 is designed with BiCMOS process. Its' system architecture is based on the integration of the company's industry-proven core technologies as follows:

- 10Base-T ENDEC/transceiver module to support the10 Mbs IEEE 802.3 functions
- Clock recovery/generator modules from National Semiconductor's leading FDDI product
- FDDI Stream Cipher (Cyclone)
- 100Base-X physical coding sub-layer (PCS) and control logic that integrate the core modules into a dual-speed Ethernet physical layer controller

2.10.1 Features

- IEEE 802.3 10Base-T compatible—built-in ENDEC and UTP/STP transceivers and filters
- IEEE 802.3u 100Base-X compatible—support for 2-pair Category 5 UTP (100m), Type 1 STP and Fiber Optic Transceivers. This connects directly to the DP83223 twisted-pair transceiver
- ANSI X3T12 TP-PMD compatible
- IEEE 802.3u Auto-negotiation for automatic speed selection
- IEEE 802.3u compatible Media Independent Interface (MII) with Serial Management Interface
- Integrated high-performance 100 Mbs clock recovery circuitry requiring no external filters
- Full-duplex support for 10 and 100 Mbs
- MII Serial 10 Mbs output mode fully-configurable node and repeater modes—allows operation in either application
- Programmable loop back modes for easy system diagnostics
- Flexible LED support
- I EEE 1149.1 Standard Test Access Port and Boundary-Scan compatible
- Small footprint 100-pin PQFP package

2.10.2 Block Diagram

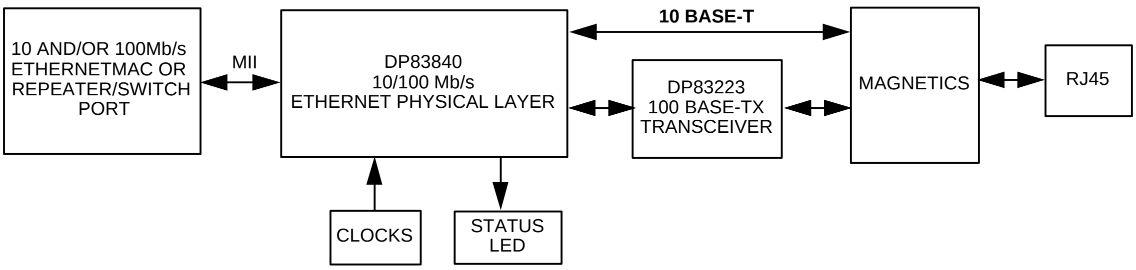


Figure 2- 21 DP83840 Block Diagram

2.10.3 Pin Diagram

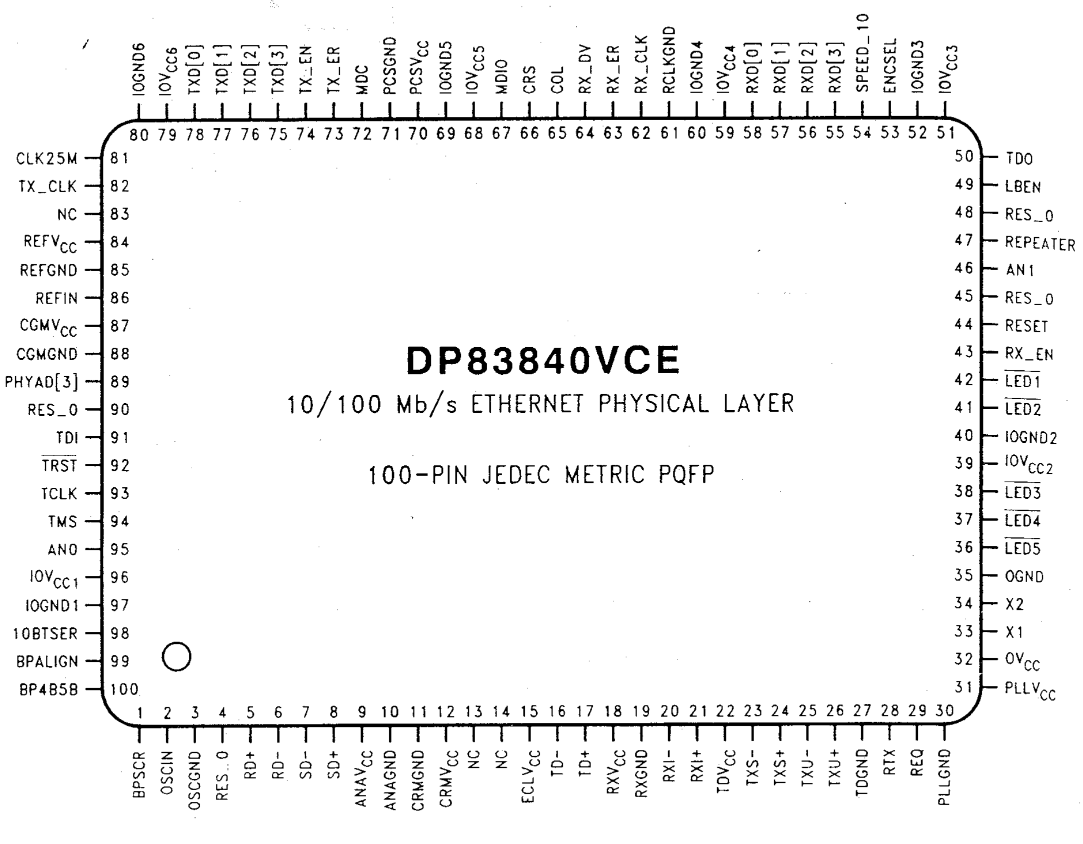


Figure 2- 22 DP83840 Pin Diagram

2.10.4 Signal Descriptions

Table 2- 16 DP83840 Signal Descriptions

Signal	Pin	Type	Description
TX_CLK	82	O, Z	**Transmit Clock.** This is the transmit clock output from the DP83840: - 25 MHz nibble transmit clock derived from Clock Generator Module's (CGM) PLL in 100 BASE-TX mode - 2.5 MHz transmit clock in 10BASE-T nibble mode - 10 MHz transmit clock in 10BASE-T serial mode
TXD[3] TXD[2] TXD[1] TXD[0]	75 76 77 78	I, J	**Transmit Data.** These are the transmit data input pins for nibble data from the MII in 100 Mbs or 10 Mbs nibble mode (25 MHz for 100 Mbs mode, 2.5 MHz for 10 Mbs nibble mode). In 10 Mbs serial mode, the TXD[0] pin is used as the serial data input pin. The TXD[3: 1] are ignored
TX_EN	74ss	I, J	**Transmit Enable.** An active high input that indicates the presence of valid nibble data on TXD[3:0] for both 100 Mbs or 10 Mbs nibble mode. In 10 Mbs serial mode, active high indicates the presence of valid 10 Mbs data on TXD[0].
TX_ER	73	I, J	**Transmit Error.** In 100 Mbs mode, when this signal is high and TX_EN is active, the HALT symbol is substituted for the actual data nibble. In 10 Mbs mode, this input is ignored. In encoder bypass mode (BP_4B5B or BP_ALIGN) TX_ER becomes the TXD[4] pin, the fifth TXD data bit.
MDC	72	I, J	**Management Data Clock.** This is the synchronous clock to the MDIO management data input/output serial interface which may be asynchronous to transmit and receive clocks. The maximum clock rate is 2.5 MHz.
MDIO	67	I/O, J	**Management Data I/O.** This is the bidirectional management instruction/data signal that may be sourced by the station management entity or the PHY. This pin requires a 4.7 Kohm pull-up resistor.
CRS (PHYAD[2])	66	I/O, Z, J	**Carrier Sense.** This signal is asserted high to indicate the presence of carrier due to receive or transmit activities in 10Base-T or 100Base-X Half-duplex modes. In Repeater, Full-duplex, or Loop back mode, a logic 1 indicates presence of carrier due only to receive activity. This is also the PHY address sensing (PHYAD[2]) signal for multiple PHY applications.

Table 2- 16 DP83840 Signal Descriptions

Signal	Pin	Type	Description
COL	65	O, Z, J	**Collision Detect.** This signal is asserted high to indicate detection of collision conditions in 10 Mbs and 100 Mbs Half-duplex modes. In 10Base-T Half-duplex mode with Heartbeat asserted (bit 4, register 1 Ch). It is also asserted for a duration of approximately 1 µs at the end of transmission to indicate CD heartbeat. In Full-duplex mode, this signal is always logic 0. There is no heartbeat function in this mode.
RX_DV	64	O, Z, J	**Receive Data Valid.** This signal is asserted high to indicate that valid data is present on RXD[3:0].
RX_CLK	62	O, Z	**Receive Clock.** This signal supplies the recovered receive clock for different modes of operation: -25 MHz nibble clock in 100 Mbs mode -2.5 MHz nibble clock in 10 Mbs nibble mode -10 MHz receive clock in 10 Mbs serial mode
RX_ER (PHYAD[4])	63	O, Z, J	**Receive Error.** This signal is asserted high to indicate that an invalid symbol has been detected inside and received packet in 100 Mbs mode. In a 5B/4B decoder bypass mode (BP_4B5B or BP_ALIGN modes), RX_ER becomes RXD[4], the fifth RXD data bit of the 5B symbol. This is also the PHY address sensing (PHYAD[4]) signal for multiple PHY applications.
RXD[3] RXD[2] RXD[1] RXD[0]	55 56 57 58	O, Z, J	**Receive Data.** These are the nibble wide receive data (synchronous to RX_CLK-25 MHz for 100Base-X mode, 2.5 MHz for 10Base-T nibble mode). Data is driven to the falling edge of RX_CLK. In 10 Mbs serial mode, the RXD[0] pin is used as the data output pin. The RXD[3:1] are not used.
RX_EN	43	I, J	**Receive Enable.** This is the active high enable for receive signals RXD[3:0], RX_CLK, RX_DV and RX_ER. A low on this input tri-states these output pins. For normal operation in a node application this pin should be pulled high.
100 Mbs Serial PMD Interface			
SPEED_10	54	O, J	**Speed 10 Mb/s.** Indicates 10 Mbs operation when high, and 100 Mbs operation when low. This signal is used to drive a low current LED to indicate 100 Mbs speed if required.
ENCSEL (PHYAD[1])	53	I/O, J	**Encode Select.** This signal is used to select binary or MLT-3 coding scheme in the PMD transceiver (at , J the DP83223, logic high selects binary coding scheme and logic low selects MLT-3 coding scheme). This is also the PHY address sensing (PHYAD[1]) signal for multiple PHY applications.

Table 2- 16 DP83840 Signal Descriptions

Signal	Pin	Type	Description
LBEN (PHYAD[0])	49	I/O, J	**Loop back Enable.** The corresponding pin for this signal should be connected to the Loopback Enable pin of a DP83223 100 Mbs Transceiver: 1 = Loopback enabled 0 = Loopback disabled In 10 Mb/s modes, this output has no meaning. This is also the PHY address sensing (PHYAD[0]) signal for multiple PHY applications.
TD- TD+	16 17	O(ECL)	**Transmit Data.** These are the differential ECL 125 Mbs serialized transmit data outputs to the DP83223 Twister.
SD- SD+	7 8	I(ECL)	**Signal Detect.** These are the differential ECL signal detect inputs and indicate that a signal is present at the DP83223 receive inputs as specified by the TP-PMD ANSI standard.
RD- RD+	6 5	I(ECL)	**Receive Data.** These are the differential ECL 125 Mbs receive data inputs.
10 Mbs Interface			
REQ	29	I	**Equalization Resistor.** A resistor connected between the signal pin and GND or Vcc adjusts the equalization step amplitude on the 10Base-T Manchester encoded transmit data (TXU + / - or TXS + /—). Typically, no resistor is required for operation with cable lengths less than 100 m. Great care must be taken to ensure system timing integrity when using cable lengths greater than 100 m. Refer to the IEEE 802.3u standard, Clause 29 for more details on system topology issues. The equations to calculate this resistor value are still under investigation. Currently, this value must be determined empirically.
10 Mbs Interface			
RTX	28	I	**Extended Cable Resistor.** A resistor connected between this signal pin and GND or Vcc adjusts the amplitude of the differential transmit outputs (TXU + / - or TXS + /—). Typically, no resistor is required for operation with cable lengths less than 100 m. Great care must be taken to ensure system timing integrity when using cable lengths greater than 100 m. Refer to the IEEE 802.3u standard, Clause 29 for more details on system topology issues. The equations to calculate this resistor value are still under investigation. Currently, this value must be determined empirically.
TXU- TXU+	25 26	O	**Unshielded Twisted Pair Output.** This differential output pair is the filtered 10Base-T transmit data for UTP cable.

Table 2- 16 DP83840 Signal Descriptions

Signal	Pin	Type	Description
TXS- TXS+	23 24	O	**Shielded Twisted Pair Output.** This differential output pair is the filtered 10Base-T transmit data for STP cable.
RXI- RXI+	20 21	I	**Twisted Pair Receive Input.** These are the differential 10Base-T receive data inputs for either STP or UTP.
Clock Interface			
REFIN	86	I	**Reference Input.** This is the 25 MHz TTL reference clock input that can be supplied from an external oscillator module or from the CLK25M output.
CLK25M	81	O, Z	**25 MHz Clock Output.** Derived from the 50 MHz OSCIN input.
Device Configuration Interface			
OSCIN	2	I	**Oscillator Input.** This is the 50 MHz + 50 ppm external TTL oscillator input. If not used, this is the pull-down GND with a 4.7-Kohm resistor.
X2	34	O	**Crystal Oscillator Output.** This is the external 20 MHz + 0.005% crystal connection and is used for 10Base-T timing. When using an external 20 MHz oscillator connected to X1, it is recommended to leave the signal pin unconnected.

Table 2- 16 DP83840 Signal Descriptions

Signal	Pin	Type	Description
Device Configuration Interface			
AN0	95	I	**AN0.** This is a three level input pin (i.e.,1, M,0) that works in conjunction with the AN1 pin to control the forced or advertised operating mode of the DP83840 according to the following table. The pin value is set by either connecting the input to GND or Vcc (0 or 1) or leaving it unconnected (M). The unconnected state, M, refers to the mid level (Vcc - 2) set by internal resistors (~ 3 Kohm). This value is latched into the DP83840 at power-up/reset. **AN1 / AN0 / Forced Mode** 0 / M / 10Base-T, Half-duplex without Auto-Negotiation 1 / M / 10Base-T, Full-duplex without Auto-Negotiation M / 0 / 100Base-TX, Half-duplex without Auto-Negotiation M / 1 / 100Base-TX, Full-duplex without Auto-Negotiation **AN1 / AN0 / Advertised Mode** M / M / All capable (i.e. Full-duplex for 100Base-TX and 100Base-TX) advertised via Auto-Negotiation 0 / 0 / 10Base-T, Half-duplex advertised via Auto-Negotiation 0 / 1 / 10Base-T, Full-duplex advertised via Auto-Negotiation 1 / 0 / 100Base-TX, Half-duplex advertised via Auto-Negotiation 1 / 1 / 100Base-TX, Full-duplex advertised via Auto-Negotiation
X1	33	I	**Crystal Oscillator Input.** This is the external 20 MHz + 0.005% crystal connection and is used for 10Base-T timing and Auto-Negotiation. If not used, the signal pin should be tied to Vcc either directly via a pull-up resistor-typically 4.7 Kohm. The DP83840 detects this condition, enables the internal - 2.5 divider and switches the 10 Mbs and Auto-Negotiation circuitry to the internally derived 20 MHz clock.
REPEATER	47	I, J	**Repeater/Node Mode.** Selects REPEATER mode when set high and NODE mode when set low. In REPEATER mode or NODE mode with Full-duplex configured. The Carrier Sense (CRS) output from the DP83840 is asserted due to receive activity only. In NODE mode, and not configured for Ful-duplex operation, CRS is asserted due to either receive and transmit activity. At power-up/reset, the pin value (set by a pull-up or pull-down resistor, typically 4.7 Kohm) is latched to bit 12 of the PCS Configuration Register, address 17h.

Table 2- 16 DP83840 Signal Descriptions

Signal	Pin	Type	Description
Device Configuration Interface			
AN1	46	I	**AN1.** This is a three-level input pin (i.e.,1, M,0) that works in conjunction with the AN0 pin to control the forced or advertised operating mode of the DP83840 according to the table given in the AN0 pin description above. The pin value is set by either connecting the input to GND or Vcc (0 or 1) or leaving it unconnected (M). This value is latched into the DP83840 at power-up/ reset.
10BTSER	98	I, J	**Serial/Nibble Select.** **10 Mbs Serial Operation:** When set high, this input selects serial data transfer mode. Manchester encoded transmit and receive data is exchanged serially with a 10 MHz clock rate on the least significant bits of the nibble-wide MII data buses, pins TXD[0] and RXD[0] respectively. This mode is intended for use with the DP83840 connected to a device (MAC or Repeater) that has a 10 Mbs serial interface. Serial operation is not supported in 100 Mbs mode, so for 100 Mbs, this input is ignored. **10 and 100 Mbs Nibble Operation:** When set low, this input selects the MII compliant nibble data transfer mode. Transmit and receive data is exchanged in nibbles on the TXD[3:0] and RXD[3:0] pins, respectively. At power-up/reset, the pin value (set by a pull-up or pull-down resistor, typically 4.7 Kohm) is latched to bit 9 of the 10Base-T Status Register, address 1Bh.
BPALIGN	99	I, J	**Bypass Alignment.** The corresponding signal pin allows 100 Mbs transmit and receive data streams to bypass all of the transmit and receive operations when set high. At power-up/reset, the pin value (set by a pull-up or pull-down resistor, typically 4 7 Kohm) is latched into bit 12 of the Loopback, Bypass and Receiver Error Mask Register, address 18h.
BP4B5B	100	I, J	**Bypass 4B5B Encoder/Decoder.** The corresponding pin allows 100 Mbs transmit and receive data streams to bypass the 4B to 5B encoder and 5B to 4B decoder circuits when set high. At power-up/reset, the pin value (set by a pull-up or pull-down resistor, typically 4.7 Kohm) is latched into bit 14 of the Loopback, Bypass and Receiver Error Mask Register, address 1 8h.

Table 2- 16 DP83840 Signal Descriptions

Signal	Pin	Type	Description
Device Configuration Interface			
BPSCR	1	I, J	**Bypass Scrambler/Descrambler.** The corresponding pin allows 100 Mb/s transmit and receive data streams to bypass the scrambler and descrambler circuits when set high. At power-up/reset, the pin value (set by a pull-up or pull-down resistor, typically 4.7 Kohm) is latched into bit 13 of the loop back, Bypass and Receiver Error Mask Register, address 1 8h.
LED Interface			
These outputs can be used to drive LEDs directly, or can be used to provide status information to a network management '2 for the LED connection diagram. A LED indication of 100 Mbs operation can be obtained by LED (and its associated resistor) to the SPEED_10 pin (54).			
LED1#	42	O, J	**Transmit LED.** This active low signal indicates the presence of transmit activity for 10 Mbs and 100 Mbs operation. If bit 2 (LED1_MODE) of the PCS Configuration Register (address 1 7h) is set high, then the LED1# pin function is changed to indicate the status of the Disconnect Function as defined by the state of bit 5 (CON_STATUS) in the PHY address register (address 1 9h). The DP83840 incorporates a "monostable" function on the LED1# output. This ensures that even minimum size packets generate adequate LED ON time to be visible.
LED2#	41	O, J	**Receive LED.** This active low signal indicates the presence of any receive activity (CRS active) for 10 Mbs and 100 Mbs operation. The DP83840 incorporates a "monostable" function on the LED2# output. This ensures that even minimum size packets generate adequate LED ON time to be visible.
LED3#	38	O, J	**Link LED.** This active low signal indicates Good Link status for 10 Mbs and 100 Mbs operation.
LED4#	37	O, J	**Polarity/Full-duplex LED.** This active low signal indicates Good Polarity status for 10 Mbs operation and Full-duplex mode status for 100 Mbs operation. If bit 1 (LED4_MODE) in the PCS Configuration Register (address 1 7h) is set high, the LED4# pin function is changed to indicate Full-duplex mode status for 10 Mbs and 100 Mbs operation.
LED5#	36	O, J	**Collision LED.** This active low signal indicates the presence of collision activity for 10 Mbs and 100 Mbs operation. This LED has no meaning for 10 Mbs or 100 Mbs Full-duplex operation.

Table 2- 16 DP83840 Signal Descriptions

Signal	Pin	Type	Description
IEEE 1149.1 Interface			
Test Access Port and Boundary Scan (sometimes referred to as JTAG) interface signals allowed to be performed.			
TDO	50	O, Z	**Test Data Output.** This is the serial instruction/test output data for the IEEE 1 149.1 scan chain. If Boundary-Scan is not implemented, the corresponding pin should be left unconnected (NC).
TDI	91	I	**Test Data Input.** This is the serial instruction/test input data for the IEEE 1149.1 scan chain.
TRST#	92	I	**Test Reset.** An asynchronous low going pulse that will reset and initialize the IEEE 1 149.1 test circuitry. If Boundary-Scan is not implemented, the corresponding pin should be left unconnected (NC) since it has an internal pull-up resistor (10 Kohm).
The IEEE 1149.1 Standard Test Access Port and Boundary Scan (sometimes referred to as JTAG) interface signals allow stem-level boundary scan to be performed.			
TCLK	93	I	**Test Clock.** This is the test clock for the IEEE 1149.1 circuitry. Its corresponding pin should be pulled to GND with an appropriate resistor (10 Kohm).
TMS	94	I	**Test Mode Select.** This is the control input to the IEEE 1149.1 test circuitry. If Boundary-Scan is not implemented, the corresponding signal pin should be left unconnected (NC) since it has an internal pull-up resistor (10 Kohm).
PHY Address Interface			
It should be noted that while PHYAD[4:0] provides up to 32 unique PHY address options, an address selection of all zeros (00000) results in a PHY isolation condition. See the Isolate bit description in the BMCR, address 00h.			
LBEN (PHYAD[0])	49	I/O, J	**PHY Address [0].** HY address sensing pin (bit 0) for multiple PHY applications. PHY address sensing is achieved by strapping a pull-up/pull-down resistor (typically 10 Kohm) to the corresponding pin as required. The pull-up/pull-down status of the signal pin is latched into the PHYAD address register (address 19h) during power up/reset. It is also the Loopback Enable output pin (LBEN) for the 100 Mbs Serial PMD Interface.

Table 2- 16 DP83840 Signal Descriptions

Signal	Pin	Type	Description
PHY Address Interface			
It should be noted that while PHYAD[4:0] provides up to 32 unique PHY address options, an address selection of all zeros (00000) results in a PHY isolation condition. See the Isolate bit description in the BMCR, address 00h.			
ENCSEL (PHYAD[1])	53	I/O, J	**PHY Address [1].** PHY address sensing pin (bit 1) for multiple PHY applications. PHY address sensing is achieved by strapping a pull-up/pull-down resistor (typically 10 Kohm) to the corresponding pin as required. The pull-up/pull-down status of the signal pin is latched into the PHYAD address register (address 19h) during power up/reset. It is also the Encode Select output pin (ENCSEL) for the 100 Mbs Serial PMD Interface.
CRS (PHYAD[2])	66	I/O, J	**PHY Address [2].** PHY address sensing pin (bit 2) for multiple PHY applications. PHY address sensing is achieved by strapping a pull-up/pull-down resistor (typically 10 Kohm) to the corresponding pin as required. The pull-up/pull-down status of the signal pin is latched into the PHYAD address register (address 19h) during power up/reset. It is also the Carrier Sense output pin (CRS) for the MII Interface.
PHYAD[3]	89	I	**PHY Address [3.** PHY address-sensing pin (bit 3) for multiple PHY applications. PHY address sensing is achieved by strapping a pull-up/pull-down resistor (typically 10 Kohm) to the corresponding pin as required. The pull-up/pull-down status of the signal pin is latched into the PHYAD address register (address 19h) during power up/reset. Since this input does not have a dual function, it is a good choice for providing a non-zero PHY address to the DP83840.
RX_ER (PHYAD[4])	23	I/O, Z, J	**PHY Address [4].** PHY address sensing pin (bit 4) for multiple PHY applications. PHY address sensing is achieved by strapping a pull-up/pull-down resistor (typically 10 Kohm) to the corresponding pin as required. The pull-up/pull-down status of the signal pin is latched into the PHYAD address register (address 19h) during power up/reset. It is also the Receive Error output pin (RX_ER) for the MII Interface.
RESET	44	I, J	**Reset.** This is an active high input that initializes the DP83840.

Table 2- 16 DP83840 Signal Descriptions

Signal	Pin	Type	Description
Power and Ground Pins			
The power (Vcc) and ground (GND) pins of the DP83840 are grouped in pairs into four categories- TTL/CMOS Input pairs, TTL/CMOS Output and I/O pairs, 10 Mbs pairs. Great care must be taken with the layout of the power and ground supplies to this device. Each of the four categories of pairs should have its own isolated supplies.			
Group A-TTL/CMOS Input Supply Pairs			
IOV$_{CC1}$, IOGND1		96, 97	TTL Input / Output Supply #1
IOV$_{CC2}$, IOGND2		39, 40	TTL Input / Output Supply #2
IOV$_{CC3}$, IOGND3		51, 52	TTL Input / Output Supply #3
PCSV$_{CC}$, PCSGND		70, 71	Physical Coding Sub-layer supply
Group B-TTL/CMOS Output and I/O Supply Pairs			
IOV$_{CC4}$, IOGND4		59, 60	TTL Input / Output Supply #4
RCLKGND		61	Receive Clock Ground, No Paired Vcc
IOV$_{CC5}$, IOGND4		68, 69	TTL Input / Output Supply #5
IOV$_{CC6}$, IOGND4		79, 80	TTL Input / Output Supply #6
REFV$_{CC}$, REFGND		84, 85	25 MHz Clock Supply
Group C-10 Mbs Supply Pairs			
RXV$_{CC}$, RXGND		18, 19	Receive Section Supply
TDV$_{CC}$, TDGND		22, 27	Transmit Section Supply
PLLV$_{CC}$, PLLGND		31, 30	Phase Locked Loop Supply
OV$_{CC}$, OGND		32, 35	Internal Oscillator Supply
Group C-100 Mbs Supply Pairs			
OSCGND		3	External Oscillator Input Ground-No Paired Vcc
ANAV$_{CC}$, ANAGND		9, 10	Analog Section Supply
CRMV$_{CC}$, CRMGND		12, 11	Clock Recovery Module Supply
ECLV$_{CC}$		15	ECL Outputs Supply
CGMV$_{CC}$, CGMGND		87, 88	Clock Generator Module Supply

2.11 NS LM78CCVF

The LM78 is a highly integrated Data Acquisition system for hardware monitoring of servers, Personal Computers, or virtually any microprocessor based system. In a PC, the LM78can be used to monitor power supply voltages, temperatures, and fan speeds. Actual values for these inputs can be read at any time, and programmable WATCHDOG™ limits in the LM78 activate a fully programmable and maskable interrupt system with two outputs. The LM78 has an on-chip temperature sensor, 5 positive analog inputs, two inverting inputs (for monitoring negative voltages), and an 8-bit ADC. An input is provided for the over temperature outputs of additional temperature sensors and this is linked to the interrupt system. The LM78 provides inputs for three fan tachometer outputs. Additional inputs are provided for Chassis Intrusion detection circuits, VID monitor inputs, and chainable interrupt. The LM78 provides both ISA and Serial Bus interfaces. A 32-byte auto-increment RAM is provided for POST (Power On Self Test) code storage.

2.11.1 Features

- Temperature sensing
- 5 positive voltage inputs
- 2 op amps for negative voltage monitoring
- 3 fan speed monitoring inputs
- Input for additional temperature sensors
- Chassis Intrusion Detector input
- WATCHDOG comparison of all monitored values
- POST code storage RAM
- ISA and I^2C Serial Bus interfaces

2.11.2 Block Diagram

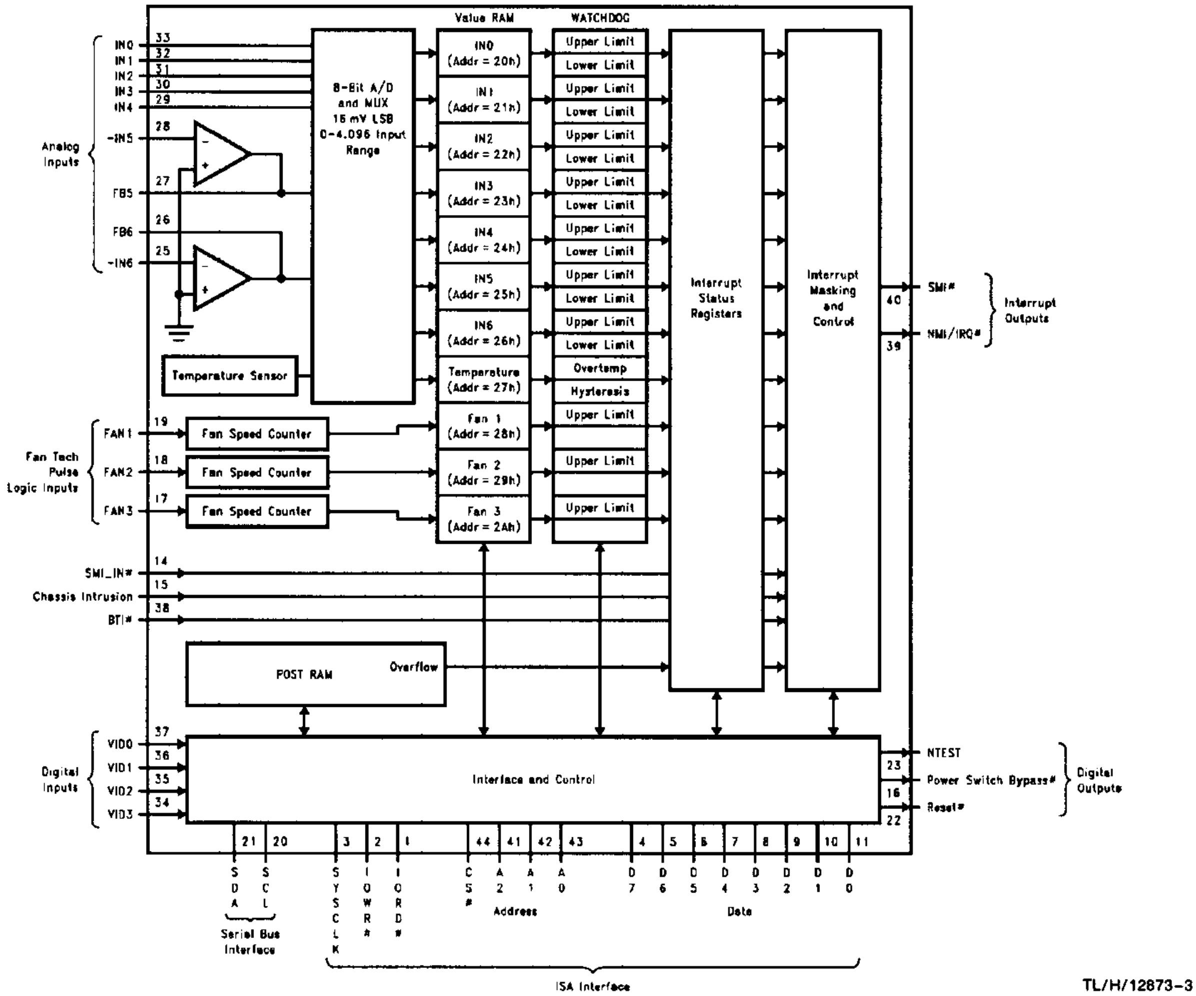


Figure 2- 23 LM78CCVF Block Diagram

2.11.3 Pin Diagram

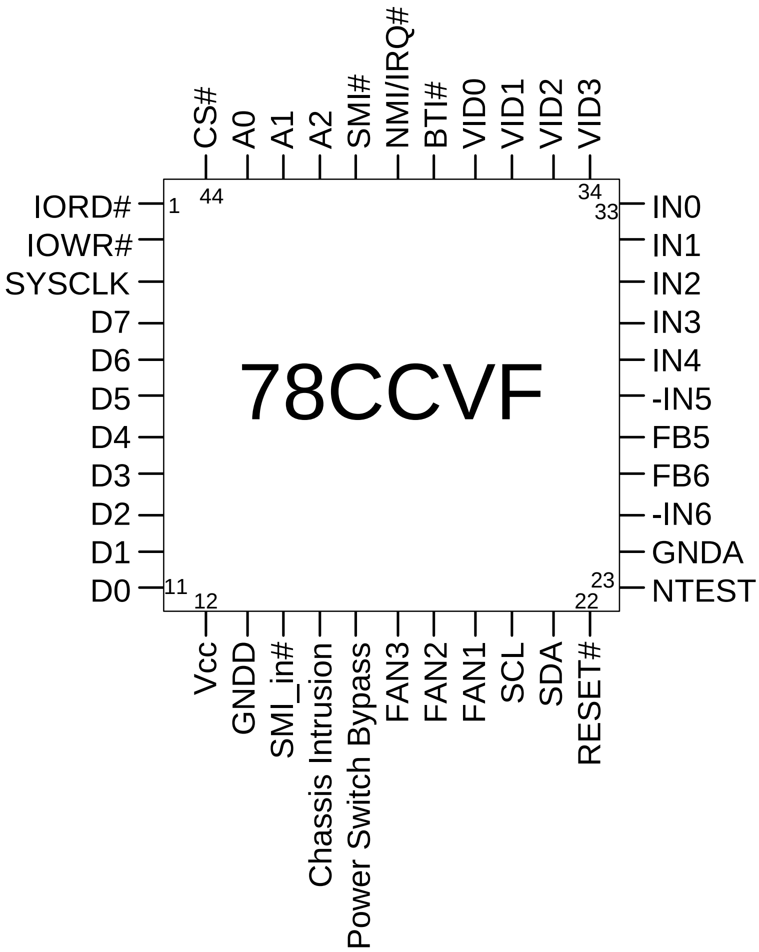


Figure 2- 24 LM78CCVF Pin Diagram

2.11.4 Signal Descriptions

Table 2- 17 LM78CCVF Signal Descriptions

Signal	Pin	Type	Description
IORD#	1	Digital Input	An active low standard ISA bus I/O Read Control.
IOWR#	2	Digital Input	An active low standard ISA bus I/O Write Control.
SYSCLK	3	Digital Input	The reference clock for the ISA bus. Typically ranges from 4.167 MHz to 8.33 MHz. The minimum clock frequency this input can handle is 1 Hz.
D7-D0	4-11	Digital I/O	Bi-directional ISA bus Data lines. D0 corresponds to the low order bit, with D7 the high order bit.
Vcc (+5V)	12	POWER	+5V Vcc power. Bypass with the parallel combination of 10 mF (electolytic or tantalum) and 0.1 mF (ceramic) bypass capacitors.
GNDD	13	GROUND	Internally connected to all digital circuitry.
SMI_IN#	14	Digital Input	Chainable SMI# (System Management Interrupt) Input. This is an active low input that propagates the SMI# signal to the SMI# output of the LM78 via SMI# Mask Register Bit 6 and SMI# enable Bit 1 of the Configuration Register.
Chassis	15	Digital I/O	An active high input from an external circuit which latches a Chassis Intrusion event. This line can go high without any clamping action Intrusion regardless of the powered state of the LM78. The LM78 provides an internal open drain on this line, controlled by Bit 7 of NMI Mask Register 2, to provide a minimum 20 ms reset of this line.
Power Switch Bypass#	16	Digital Output	An active low output intended to drive an external P-channel power MOSFET for software power control.
FAN3±FAN1	17-19	Digital Input	0V to +5V amplitude fan tachometer input.
SCL	20	Digital Input	Serial Bus Clock.
SDA	21	Digital I/O	Serial Bus bidirectional Data.
RESET#	22	Digital Output	Master Reset, 5 mA driver (open drain), active low output with a 20 ms minimum pulse width. Available when enabled via Bit 7 in SMI# Mask Register 2.
NTEST	23	Test Output	NAND Tree totem-pole output that provides board-level connectivity testing.
GNDA	24	GROUND	Internally connected to all analog circuitry. The ground reference for all analog inputs.
-IN6	25	Analog Input	Ground-referred inverting op amp input.
FB6	26	Analog Output	Output of inverting op amp for Input 6.

Table 2- 17 LM78CCVF Signal Descriptions

Signal	Pin	Type	Description
FB5	27	Analog Output	Output of inverting op amp for Input 5.
-IN5	28	Analog Input	Ground-referred inverting op amp input.
IN4-IN0	29-33	Analog Input	0V to 4.096V FSR Analog Inputs.
VID3-VID0	34-37	Digital Input	Voltage Supply readouts from P6. This value is read in the VID/Fan Divisor Register.
BTI#	38	Digital Input	Board Temperature Interrupt driven by O.S. outputs of additional temperature sensors such as LM75. Provides internal pull-up of 10 kΩ.
NMI#/IRQ#	39	Digital Output	Non-Maskable Interrupt (open source)/Interrupt Request# (open drain). The mode is selected with Bit 5 of the Configuration Register and the output is enabled when Bit 2 of the Configuration Register is set to 1. The default state is disabled and IRQ# mode. SMI# 40 1 Digital Output System Management Interrupt (open drain). This output is enabled when Bit 1 in the Configuration Register is set to 1. The default state is disabled. A2±A0 41±43 3 Digital Input The three lowest order bits of the 16-bit ISA Address Bus. A0 corresponds to the lowest order bit.
CS#	44	Digital Input	Chip Select input from an external decoder which decodes high order address bits on the ISA Address Bus. This is an active low input.

2.12 SMC 37C935

The SMC 37C935 is an advanced high-performance multi-mode parallel port super I/O floppy disk controller.

2.12.1 Features

- Compatible with ISA Plug-and-Play standard (version 1.0a)
- 8042 keyboard controller
  - 2-K Program ROM
  - 256-byte Data RAM
  - Asynchronous access to two data registers and one status register
  - Supports interrupt and pollinq access
  - 8-bit timer counter
- Real time clock
  - MC146818 and DS1287 compatible
  - 256 bytes of battery-backed CMOS in two banks of 128 bytes
  - 128 bytes of CMOS RAM lockable in 4 x 32 byte blocks
  - 12- and 24-hour time format
  - Binary and BCD format
  - <1µa standby current (typ)
- Intelligent auto-power management
- 2.88-MB super I/O floppy disk controller
  - Relocatable to 480 different addresses
  - 13 IRQ options
  - 3 DMA Options
  - Licensed CMOS 765B floppy disk controller
  - Advanced digital data separator
  - Software and register compatible with SMC's proprietary 82077AA compatible core
  - Sophisticated Power Control Circuitry (PCC) including multiple power-down modes for reduced power consumption
  - Game port select logic
  - Directly supports two floppy drives
  - 24 mA AT bus drivers
  - Low-power CMOS design

- Licensed CMOS 765B floppy disk controller core
    - Supports vertical recording format
    - 16-byte data FIFO
    - 100% IBM compatibility
    - Detects all overrun and underrun conditions
    - 48-mA drivers and Schmitt Trigger inputs
    - DMA enable logic
    - Data rate and drive control registers
- Enhanced digital data separator
    - Low-cost implementation
    - No filter components required
    - 2-Mbps, 1-Mbps, 500-Kbps, 300-Kbps, 250-Kbps data rates
    - Programmable pre-compensation modes
- Serial ports
    - Relocatable to 480 different addresses
    - 13 IRQ options
    - Two high-speed NS16C550 Compatible UARTs with send/receive 16-byte FIFOs
    - Programmable baud rate generator
    - Modem control circuitry including 230-K and 460-K baud
    - IrDA, HP-SIR, ASK-IR support
- IDE interface
    - Can be relocated to 480 different addresses
    - 13 IRQ options
    - 6 DMA Options
    - Two-channel/four-drive support
    - On-chip decode and select logic compatible with IBM PC/Xr and PC/A? embedded hard disk drives
- Multi-mode parallel port with ChiProtect
    - Can be relocated to 480 different addresses

2.12.2 Block Diagram

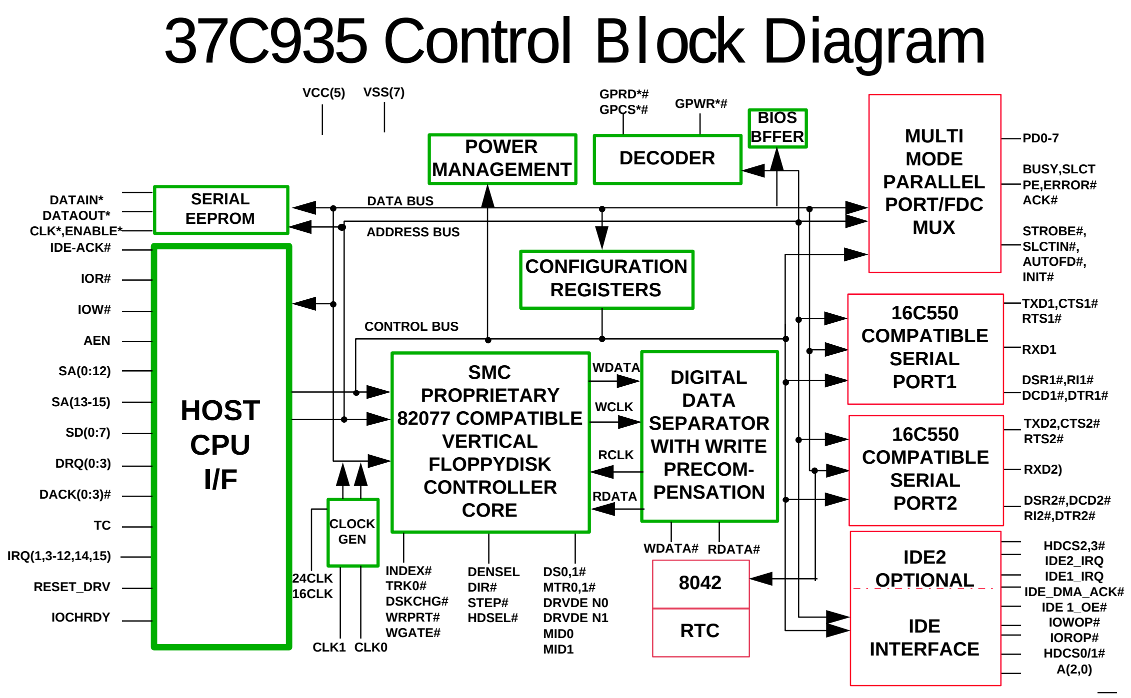


Figure 2- 25 SMC 37C935 Block Diagram

2.12.3 Pin Diagram

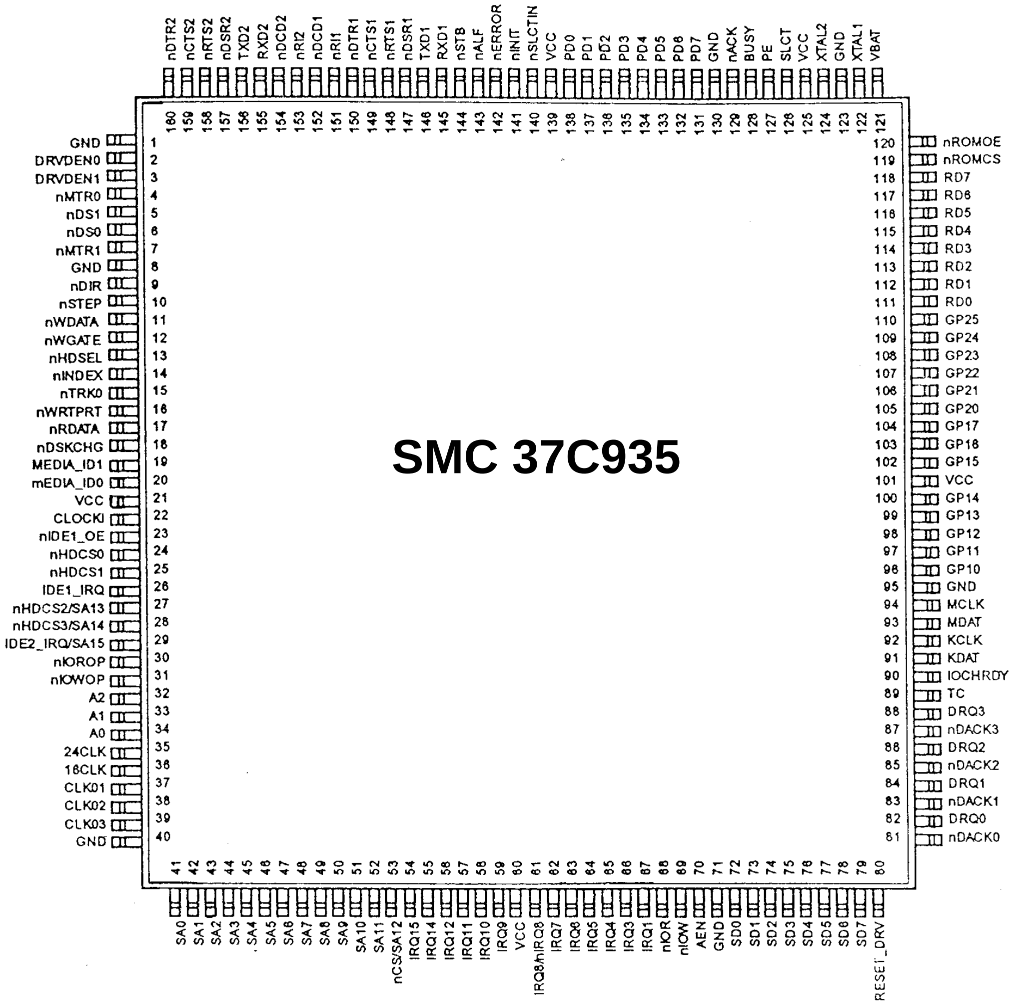


Figure 2- 26 SMC 37C935 Pin Diagram

2.12.4 Signal Descriptions

Table 2- 18 SMC 37C935 Signal Type Descriptions

Signal Type	Description
I	Input TTL compatible
IS	Input with Schmitt Trigger
I/OD16P	Input/output, 19-mA sink, 90-uA pull-up
I/O24	Input/output pin. 24-mA sink; 12-mA source
O4	Output, 4-mA sink; 2.0-mA source
O8SR	Output, 8-mA sink; 4.0-mA source with Slew Rate Limiting
O24	Output, 24-mA sink; 12-mA source
OD24	Output, open drain; 24-mA sink
OD48	Output, open drain; 48-mA sink
OD24P	Output, open drain; 24-mA sink, 4-mA source pull up
OP24	Output; 24-mA sink, 12-mA source
OCLK	Clock output
ICLK	Clock input

Table 2- 19 SMC 37C935 Signal Descriptions

Signal	Pin	Type	Description
Host Processor Interface			
SD0 - SD7	72:79	I/O24	System Data Bus
SA0 - SA11	41:52	I	System Address Bus
CS#	53	I	Chip Select / SA12
AEN	70	I	Address Enable
IOCHRDY	90	OD24	I/O Channel Ready
RESET_DRV	80	IS	Reset Drive
IRQ[1, 3:12, 14, 15]	67:61, 59:54	OD24	Interrupt Requests
DRQ[0:3]	82,84,86,88	O24	DMA Request
DACK[0:3]#	81, 83, 85, 87	I	DMA Acknowledge
TC	89	I	Terminal Count
IOR#	68	I	I/O Read
IOW#	69	I	I/O Write
24CLK	35	O8SR	Serial Clock Out (24 MHz)
16CLK	36	O8SR	16-MHz Out
CLOCKI	22	ICLK	14.318-MHz Clock Input
CLOCK1	37	O8SR	14.318-MHz Clock Output 1
CLOCK2	38	O8SR	14.318-MHz Clock Output 2
CLOCK3	39	O8SR	14.318-MHz Clock Output 3

Table 2- 19   SMC 37C935 Signal Descriptions

Signal	Pin	Type	Description
Diskette Drive Interface			
RDATA#	17	IS	Read Disk Data
WGATE#	12	OD48	Write Gate
WDATA#	11	OD48	Write Data
HDSEL#	13	OD48	Head Select (1 = side 0)
DIR#	9	OD48	Direction Control (1 = out)
STEP#	10	OD48	Step Pulse
DSKCHG#	18	IS	Disk Change
DS[0:1]#	5,6	OD48	Drive Select 0, 1
MTR[0:1]#	7,4	OD48	Motor on Lines
WPROT#	16	IS	Write Protected
TR0#	15	IS	Track 00
INDEX#	14	IS	Index Pulse Input
DRVDEN[1:0]	3,2	OD48	Drive Density Select [1:0]
MID[1:0]	19,20	IS	Media ID Inputs
Serial Port Interface			
RXD1, RXD2	145, 155	I	Receive Data
TXD1, TXD2	146, 156	O4	Transmit Data
RTS1#, RTS2#	148, 158	O4	Request to Send
CTS1#, CTS2#	149, 159	I	Clear to Send
DTR1#, DTR2#	150, 160	O4	Data Terminal Ready
DSR1#, DSR2#	147, 157	I	Data Set Ready
DCD1#, DCD2#	152, 154	I	Data Carrier Select
RI1#, RI2#	151, 153	I	Ring Indicator
Parallel Port Interface			
PD0-PD7	138:131	I/OP24	Port Data
SLCTIN#	140	OD24/OP24	Printer Select
INIT#	141	OD24/OP24	Initiate Output
AUTOFD#	143	OD24/OP24	Autofeed Signal
STROBE#	144	OD24/OP24	Strobe Signal
BUSY	128	I	Busy Signal
ACK#	129	I	Acknowledge Handshake
PE	127	I	Paper End
SLCT	126	I	Printer Selected
ERR#	142	I	Error at Printer
IDE			

Table 2- 19 SMC 37C935 Signal Descriptions

Signal	Pin	Type	Description
IDE1_OE#	23	O4	IDE1 Enable
HDCS0#	24	O24	IDE1 Chip Select0
HDCS1#	25	O24	IDE1 Chip Select1
IOROP#	30	O24	IOR Output
IOWOP#	31	O24	IOW Output
A[2:0]	32:34	O24	Address [2:0] Output
IDE1_IRQ	26	I	IDE Interrupt Request
HDCS2	27	O24	IDE2 Chip Select 2 / SA13
HDCS3	28	O24	IDE2 Chip Select 3 / SA14
IDE2_IRQ	29	I	IDE2 Interrupt Request / SA15
Real Time Clock			
XTAL1	122	ICLK	32-KHz Crystal Input
XTAL2	124	OCLK	32-KHz Crystal Output
Vbat	121		Battery Voltage
Keyboard / Mouse			
KDAT	91	I/OD16P	Keyboard Data
KCLK	92	I/OD16P	Keyboard Clock
MDAT	93	I/OD16P	Mouse Data
MCLK	94	I/OD16P	Mouse Clock
General Purpose I/O			
GP10	96	I/O4	IRQ In
GP11	97	I/O4	IRQ In
GP12	98	I/O4	WD Timer Output / IRRX
GP13	99	I/O24	Power LED Output / IRTX
GP14	100	I/O4	General Purpose Read Strobe
GP15	102	I/O4	General Purpose Write Strobe
GP16	103	I/O4	Joy Stick Read Strobe / JOYCS
GP17	104	I/O4	Joy Stick Write Strobe
GP20	105	I/O4	IDE2 Output Enable
GP21	106	I/O4	Serial EEPROM Data In
GP22	107	I/O4	Serial EEPROM Data Out
GP23	108	I/O4	Serial EEPROM Clock
GP24	109	I/O4	Serial EEPROM Enable
GP25	110	I/O4	8042 P21
BIOS Buffers			

Table 2- 19 SMC 37C935 Signal Descriptions

Signal	Pin	Type	Description
RD[0:7]	111:118	I/O4	ROM Bus (I/O to the SD bus)
DOMCS#	119	I	ROM Chip Select (only used for ROM)
ROMOE#	120	I	ROM Output Enable (DIR) (only used for ROM)
Power			
VCC	21, 60, 101, 125, 139		+ 5V Supply Voltage
GND	1, 8, 40, 71, 95, 123, 130		Ground

Chapter 3

BIOS Setup Utility

Most systems are already configured by the manufacturer or the dealer. There is no need to run Setup when starting the computer unless you get a Run Setup message.

If you repeatedly receive Run Setup messages, the battery may be bad. In this case, the system cannot retain configuration values in CMOS. Ask a qualified technician for assistance.

Before you run Setup, make sure that you have saved all open files. The system reboots immediately after you exit Setup.

3.1 Entering Setup

To enter Setup, press the key combination CTRL+ALT+ESC.

You must press CTRL+ALT+ESC while the system is booting. This key combination does not work during any other time.

The BIOS Utility main menu then appears:

```
                         BIOS Utility

                Basic System Configuration
               Advanced System Configuration
                 PCI System Configuration
                     System Security
              Remote Diagnostic Configuration
                Load Setup Default Settings

↑↓ = Move Highlight Bar,  ↵  = Select,  Esc = Exit and Reboot
```

The parameters on the following screens show default values. These values may not be the same as those in your system.

The grayed items (denoted with asterisks) on the following screens have fixed settings and are non-configurable.

3.2 Basic System Configuration

Select Basic System Configuration to input configuration values such as date, time, and disk types.

The following screen shows the Basic System Configuration menu.

```
                  Basic System Configuration         Page 1/2

   Date  .....................[MM/DD/YY]
   Time  .....................[HH:MM:SS]
   Diskette Drive A  .........[xx-MB     xx-inch]
   Diskette Drive B  .........[xx-MB     xx-inch]

   Onboard IDE  ..............[Enabled ]

                                  Cylinder  Head   Sector

   IDE Drive 0  (xxx MB) .....[Auto]    xx       xx     xx
   IDE Drive 1  (xxx MB) .....[Auto]    xx       xx     xx



   Total Memory  .............[ xxx]  MB

   ↑↓ = Move Highlight Bar,    → ← = Change Setting
   PgDn/PgUp = Move Screen,    F1 = Help,   Esc  =  Exit
```

The command line at the bottom of the menu tells you how to highlight items, change settings, and move from one screen to another.

Press [↑] or [↓] on the cursor-edit keypad to highlight the desired parameter.

Press [→] or [←] to select the desired option for a parameter.

Press [PGDN] to move to the next page or [PGUP] to return to the previous page.

Press [ESC] to exit the configuration menu.

The following screen shows page 2 of the Basic System Configuration menu.

```
                 Basic System Configuration          Page 2/2

   Enhanced IDE Features
      Hard Disk Block Mode  .......... [Enabled ]
      Advanced PIO Mode  ............. [Enabled ]
      Hard Disk Size > 504MB  ........ [Enabled ]
      Hard Disk 32-bit Access  ....... [Enabled ]

   Num Lock After Boot  .............. [Enabled ]
   Memory Test  ...................... [Disabled]
   Quiet Boot  ....................... [Disabled]
   Configuration Table  .............. [Enabled ]

  ↑↓ = Move Highlight Bar,    → ← = Change Setting
  PgDn/PgUp = Move Screen,    F1 = Help,   Esc  =  Exit
```

The following sections explain the different parameters and their settings.

3.2.1 Date and Time

The real-time clock keeps the system date and time. After setting the date and time, you need not enter them every time you turn on the system. As long as the internal battery remains good (approximately seven years) and connected, the clock continues to keep the date and time accurately even when the power is off.

3.2.1.1 Date

Highlight the items on the date parameter and press → or ← to set the date following the month-day-year format.

Valid values for month, day, and year are:

- Month **1** to **12**
- Day **1** to **31**
- Year **00** to **99**

3.2.1.2 Time

Highlight the items on the time parameter and press → or ← to set the time following the hour-minute-second format.

The valid values for hour, minute, and second are:

- Hour **00** to **23**
- Minute **00** to **59**
- Second **00** to **59**

3.2.2 Diskette Drives

To enter the configuration value for the first diskette drive (drive A), highlight the Diskette Drive A parameter. Press → or ← key to view the options and select the appropriate value.

Possible settings for the Diskette Drive parameters:

- `[        None        ]`
- `[360  KB,   5.25-inch]`
- `[1.2  MB,   5.25-inch]`
- `[720  KB,    3.5-inch]`
- `[1.44 MB,    3.5-inch]`
- `[2.88 MB,    3.5-inch]`

Follow the same procedure for Diskette Drive B. Choose **None** if you do not have a second diskette drive.

3.2.3 Onboard IDE

When set to **Enabled**, this parameter enables the IDE drives installed in the system. Setting to **Disabled** deactivates the IDE drives and grays the IDE Drive parameters.

3.2.4 IDE Drives

Move the highlight bar to the IDE Drive 0 parameter to configure the first IDE drive (drive C). Press → or ← to display the IDE hard disk types with their respective values. Select the type that corresponds to your drive. Follow the same procedure for the other drives, if any. Choose **None** if you do not have other drives.

3.2.4.1 Selecting the "Auto" Option

If you do not know the exact type of your IDE drive, select the option **Auto**. During the power-on self-test (POST), when the system performs self-testing and self-initialization before loading the operating system and applications, the BIOS utility automatically determines your IDE drive type. You can see the drive type and its values when you enter the BIOS Utility.

```
                                          Cylinder   Head     Sector
IDE Drive 0 (xx MB) ......[Auto]             xx        xx       xx
```

If desired, you can save the values under the option **User**.

```
                                          Cylinder   Head     Sector
IDE Drive 0 (xx MB) ......[User]             xx        xx       xx
```

The next time you boot the system, the BIOS utility does not have to auto-configure your IDE drive as it detects the saved disk information during POST. Follow the same procedure to auto-configure other IDE drives.

Copy the IDE disk drive values and keep them in a safe place in case you have to reconfigure the disk in the future.

3.2.4.2 Selecting the "User" Option

There are cases when you cannot use the option **`Auto`**, instead you have to select **`User`**. Choose the **`User`** option when you have installed an hard disk that was previously formatted but does not use the disk native parameters or structure, that is, the disk type may be in the hard disk types list but the number of cylinders, heads, and sectors differ.

Follow these steps to configure a hard disk with the **`User`** option:

1. Highlight an hard disk parameter.

2. Select the option **`User`** and press ENTER .

3. Type in the number of cylinders, heads, and sectors of the drive under the appropriate columns.

Be sure to have the correct hard disk information beforehand.

4. Choose **`Yes`** when asked if you want to save CMOS data.

3.2.5 Total Memory

The system automatically detects the total amount of onboard memory during the POST and sets the memory parameters accordingly. If you install additional memory, the system automatically adjusts this parameter to display the new memory size.

3.2.6 Enhanced IDE Features

3.2.6.1 Hard Disk Block Mode

This function enhances disk performance depending on the hard disk in use. If you set this parameter to **`Enabled`**, it allows data transfer in block (multiple sectors) by increasing the data transfer rate to 256 bytes per cycle. If your system does not boot after enabling this parameter, change the setting to **`Disabled`**. This parameter is normally set to **`Enabled`** .

3.2.6.2 Advanced PIO Mode

Enabling this parameter improves system performance by allowing the use of faster hard drives. If your hard disk does not support this function, set this parameter to **Disabled**. The default if **Enabled**.

3.2.6.3 Hard Disk Size > 504 MB

If enabled, BIOS allows you to use a hard disk with a capacity of more than 504 MB. This is made possible through the Logical Block Address (LBA) mode translation. Other operating systems require this parameter to be set to **Disabled**.

To prevent data loss, set this parameter set to **Enabled** if you are using a hard disk with more than 504 MB capacity that was previously configured through LBA mode. If you use a hard disk configured through cylinder-head-sector (CHS) mode, set this parameter to **Disabled**. The default is **Enabled**.

3.2.6.4 Hard Disk 32-bit Access

Enabling this parameter improves system performance by allowing the use of the 32-bit hard disk access. This enhanced IDE feature only works under DOS, Windows 3.x, Windows 95, and Novell NetWare. If your software or hard disk does not support this function, set this parameter to **Disabled**. The default is **Enabled**.

3.2.7 Num Lock After Boot

This parameter allows you to activate the Num Lock function upon booting. The default setting is **Enabled**.

3.2.8 Memory Test

When set to **Enabled**, this parameter allows the system to perform a RAM test during the POST routine. When set to **Disabled**, the system detects only the memory size and bypasses the test routine. The default setting is **Disabled**.

3.2.9 Quiet Boot

This parameter enables or disables the quiet boot function. When set to **Enabled**, BIOS is in graphical mode and displays only an identification logo during POST and while booting. After which the screen displays the operating system prompt (such as DOS) or logo (such as Windows 95). If any error occurred while booting, the system automatically switches to text mode.

Even if your setting is **Enabled**, you may also switch to the text mode while booting by pressing F9 after you hear a beep that indicates the activation of the keyboard.

When set to **Disabled**, BIOS is in the conventional text mode where you see the system initialization details on the screen.

3.2.10 Configuration Table

This parameter allows you to display the configuration table after POST but before booting. The configuration table gives a summary of the hardware devices and settings that BIOS detected during POST. Following is a sample configuration table.

```
CPU ID           : Pentium II          Base Memory      : xxx KB
CPU Clock        : xxx MHz             Extended Memory  : xxxx KB
Math Coprocessor : Installed           Shadow RAM       : xxx KB
IDE Drive 0      : xxx MB              Internal Cache   : xxx KB, Enabled
IDE Drive 1      : xxx MB              External Cache   : xxx KB, Enabled
Diskette Drive A : xx-MB, xx-inch      Serial Port(s)   : 3F8h, 2F8h
Diskette Drive B : None                Parallel Port    : 378h
ECC/Parity Mode  : ECC                 Pointing Device  : None
USB HC           : Disabled            CPU L2 ECC       : None
```

3.3 Advanced System Configuration

The Advanced System Configuration option allows you to configure the advanced system memory functions.

Do not change any settings in the Advanced Configuration if you are not a qualified technician to avoid damaging system.

The following screen shows page one of the Advanced System Configuration parameters.

```
              Advanced System Configuration         Page 1/1

   Internal Cache (CPU Cache) .......... [Enabled ]
   External Cache (CPU Cache)........... [Enabled ]
   Cache Scheme......................... [Write back]

   ECC/Parity Mode Selection ........... [   ECC   ]
     Operation of ECC................... [Correction Enabled]

   Memory at 15MB-16MB Reserved for..... [     System    ] Use


   MP Fault Tolerance................... [Enabled ]



   ↑↓ = Move Highlight Bar,    → ← = Change Setting
   PgDn/PgUp = Move Screen,    F1 = Help,   Esc  =  Exit
```

3.3.1 Internal Cache (CPU Cache)

This parameter enables or disables the first-level cache memory integrated in the Pentium II CPU.

3.3.2 External Cache (CPU Cache)

This parameter enables or disables the second-level cache memory.

3.3.3 Cache Scheme

This parameter allows you to select **Write back** or **Write through** for the cache mode. **Write back** updates the cache but not the memory when there is a write instruction. It updates the memory only when there is an inconsistency between the cache and the memory. **Write through** updates both the cache and the memory whenever there is a write instruction.

3.3.4 ECC/Parity Mode Selection

This parameter allows you to select **ECC**, **Parity**, or **Disabled** . The **ECC** option allows single-bit error detection and automatic correction. The automatic correction depends on the setting of the parameter Operation of ECC. See section 3.3.4 for details.

ECC also detects multiple-bit errors but does not correct them. Instead, it issues a non-maskable interrupt (NMI) signaling the operating system of the multiple-bit error detection.

The **Parity** option allows parity check. If it detects any parity errors, it sets up the parity error flag in the chipset. This signals the operating system of the parity error detection.

3.3.4.1 Operation of ECC

This parameter allows you to enable or disable the error correction function. In the option **Correction Enabled**, ECC automatically corrects any single-bit errors detected. For multiple-bit errors detected, ECC only issues an NMI to signal the operating system of the multiple-bit error detection.

In the option **Correction Disabled**, ECC detects both single-bit and multiple-bit errors but does not correct either one. It only issues an NMI to signal the operating system of the error detection.

This parameter is grayed if the ECC/Parity Mode Selection parameter is set to either **Parity** or **Disabled** . Refer to section 3.3.3.

3.3.5 Memory at 15MB-16MB

To prevent memory address conflicts between the system and expansion boards, reserve this memory range for the use of either the system or an expansion board. Before setting this parameter, check your add-on card manual to determine if your add-on card needs this memory space. If not, set this parameter to **System Use**.

3.3.6 MP Fault Tolerance

This parameter is only applicable to single processor condition. Enable it allows system interrupts pass through I/O APIC (Advanced Programmable Interrupt Controller). If it's disabled, interrupts will pass through a traditional PIC(8259).

Enabling this parameter allows single-processor system to create a multiprocessor (MP) table for multiprocessor OS use. In a single-processor system running Windows NT, you may disable this parameter to enhance system performance.

If you plan to install second processor later, enable this parameter before installing OS (here the OS must be a multiprocessor OS; i.e. Windows NT, with multiprocessor system architecture) in a single-processor system, then you may upgrade to a dual-processor system without reinstalling OS.

3.4 PCI System Configuration

The PCI System Configuration allows you to specify the settings for your PCI devices.

```
                PCI System Configuration          Page 1/2

   PCI IRQ Setting ...........[  Auto  ]
                              INTA   INTB   INTC   INTD
      PCI Slot 1 .............  [--]   [--]   [--]   [--]
      PCI Slot 2 .............  [--]   [--]   [--]   [--]
      PCI Slot 3 .............  [--]   [--]   [--]   [--]
      PCI Slot 4 .............  [--]   [--]   [--]   [--]
      PCI Slot 5 .............  [--]   [--]   [--]   [--]
      Onboard LAN ............  [--]
      Onboard SCSI1 ..........  [--]
      Onboard SCSI2 ..........  [--]

   VGA Palette Snoop ..........[Disabled]

   PCI Slot Latency Time ......[   20   ]

   ↑↓ = Move Highlight Bar,    → ← = Change Setting
   PgDn/PgUp = Move Screen,    F1 = Help,   Esc  =  Exit
```

```
                PCI System Configuration          Page 2/2

   Onboard LAN  ...............[Enabled ]
   USB Host Controller ........[Disabled]
   Onboard SCSI 1  ............[Enabled ]
       Boot SCSI 1 Device .....[Enabled ]
   Onboard SCSI 2  ............[Enabled ]
       Boot SCSI 2 Device .....[Enabled ]

   RAID Port Boot .............[Disabled]

   PCI IRQ Sharing ............[No ]
   Plug & Play OS .............[No ]
   Reset Resource Assignments .[No ]

   ↑↓ = Move Highlight Bar,    → ← = Change Setting
   PgDn/PgUp = Move Screen,    F1 = Help,   Esc  =  Exit
```

3.4.1 PCI IRQ Setting

This parameter allows for **Auto** or **Manual** configuration of PCI devices. If you use plug-and-play (PnP) devices, set this parameter to **Auto**. The system then automatically assigns IRQ to the PnP devices. If your PCI device is not a PnP, you can manually assign the interrupt for each device. Refer to your manual for technical information about the PCI card.

When the PCI IRQ Setting is set to **Auto***, all the IRQ setting fields become gray and non-configurable.*

3.4.1.1 PCI Slots

These parameters allow you to specify the appropriate interrupt for each of the PCI devices. You can assign IRQ3, IRQ4, IRQ5, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, or IRQ15 to the slots.

Make sure that the interrupt you assign in any of the PCI slots are not used by other devices to avoid conflicts.

Press [↑] or [↓] to move between fields. Press [→] or [←] to select options.

3.4.1.2 Onboard LAN

This item allows you to manually assign the interrupt for the onboard LAN when the PCI IRQ Setting parameter is set to **Manual** . This parameter is grayed and not user-configurable when the PCI IRQ Setting is set to **Auto** and when the Onboard LAN parameter is set to **Disabled** .

3.4.1.3 Onboard SCSI 1/Onboard SCSI 2

These items allow you to manually assign the interrupts for the onboard SCSI hard disks when the PCI IRQ Setting parameter is set to **Manual**. These parameters are grayed and not user-configurable when the PCI IRQ Setting is set to **Auto** and when the Onboard SCSI 1 and Onboard SCSI 2 parameters on page 2 are set to **Disabled** .

Make sure to assign an IRQ to this item if you set the PCI IRQ Setting parameter to **Manual***.*

Press [↑] or [↓] to move between fields. Press [→] or [←] to select options.

3.4.2 VGA Palette Snoop

This parameter permits you to use the palette snooping feature if you installed more than one VGA card in the system.

The VGA palette snoop function allows the control palette register (CPR) to manage and update the VGA RAM DAC (Digital Analog Converter, a color data storage) of each VGA card installed in the system. The snooping process lets the CPR send a signal to all the VGA cards so that they can update their individual RAM DACs. The signal go through the cards continuously until all RAM DAC data have been updated. This allows display of multiple images on the screen.

Some VGA cards have required settings for this feature. Consult your VGA card manual before setting this parameter.

3.4.3 PCI Slot Latency Time

This parameter allows you to set the length of time for a PCI device to use the PCI bus.

A PCI master can burst indefinitely as long as the target can source/sink the data, and no other agent requests for the bus. If another PCI device requests for the use of the PCI bus, a PCI bus arbitration takes place, and the tenure of the device currently using the PCI bus cannot go over the PCI latency time set in BIOS. This setting depends on your application. For example, if you install a high bandwidth block I/O card, e.g., FDDI, the longer the latency time the better. This setting only affects the primary PCI components (PCI slots 1, 2, 3, and onboard LAN). The secondary PCI components (PCI slots 4, 5, and onboard SCSI1 and onboard SCSI2) are always set to 20 PCI clocks.

3.4.4 Onboard LAN

This parameter allows you to enable or disable the onboard LAN feature.

3.4.5 USB Host Controller

This parameter allows you to enable or disable the onboard USB host controller and the external USB ports.

3.4.6 Onboard SCSI 1

This parameter allows you to enable or disable the onboard SCSI 1 device.

3.4.6.1 Boot SCSI 1 Device

This parameter allows you to enable or disable the onboard SCSI 1 as a boot device priority.

3.4.7 Onboard SCSI 2

This parameter allows you to enable or disable the onboard SCSI 2 device.

3.4.7.1 Boot SCSI 2 Device

This parameter allows you to enable or disable the onboard SCSI 2 as a boot device priority.

3.4.8 RAID Port Boot

Enabling this parameter allows booting from a RAID hard disk drive. This parameter is currently not user-configurable and is reserved for future use.

3.4.9 PCI IRQ Sharing

When set to **Yes**, this parameter allows you to assign the same IRQ to more than one PCI device installed in the system. When set to **No**, you must assign different IRQs to the PCI devices.

3.4.10 Plug & Play OS

When this parameter is set to **Yes**, BIOS initializes only PnP boot devices such as SCSI cards. When set to **No**, BIOS initializes all PnP boot and non-boot devices such as sound cards.

Set this parameter to **Yes** *only if your operating system is Windows 95.*

3.4.11 Reset Resource Assignments

Set this parameter to **Yes** to avoid IRQ conflict when installing non-PnP or PnP ISA cards. This clears all resource assignments and allows BIOS to reassign resources to all installed PnP devices the next time the system boots. After clearing the resource data, the parameter resets to **No**.

3.5 System Security

The Setup program has a number of security features to prevent unauthorized access to the system and its data.

Enter the Setup program and select System Security to display the following screen.

```
                    System Security              Page 1/1

 Disk Drive Control
   Diskette Drive ................[         Normal        ]
   Hard Disk Drive ...............[         Normal        ]
   System Boot Drive .............[Drive A then C]
 Onboard Communication Ports
   Serial Port 1 Base Address .....[   3F8h   ]
   Serial Port 2 Base Address .....[   2F8h   ]
   Parallel Port Base Address .....[378 (IRQ 7]
      Operation Mode...............[Standard Parallel Port (SPP)] Mode
         *ECP DMA Channel .........[-]
 Onboard PS/2 Mouse (IRQ12)  ...[Enabled ]

 Setup Password....................[  None  ]
 Power On Password.................[  None  ]

    ↑↓ = Move Highlight Bar,    → ← = Change Setting
    PgDn/PgUp = Move Screen,    F1 = Help,   Esc  =  Exit
```

3.5.1 Disk Drive Control

The disk drive control features allow you to enable or disable the read/write functions of a disk drive. These features can also control the diskette drive or the hard disk drive boot function to prevent loading operating systems or other programs from a certain drive while the other drives are operational.

Table 3-1 lists the drive control settings and their corresponding functions.

Table 3- 1 Drive Control Settings

Setting	Description
Diskette Drive	
Normal	Diskette drive functions normally
Write Protect All Sectors	Disables the write function on all sectors
Write Protect Boot Sector	Disables the write function only on the boot sector
Disabled	Disables all diskette functions
Hard Disk Drive	
Normal	Hard disk drive functions normally
Write Protect All Sectors	Disables the write function on all sectors
Write Protect Boot Sector	Disables the write function only on the boot sector
Disabled	Disables all hard disk functions
System Boot Drive	
Drive A then C	The system checks drive A first. If there is a diskette in the drive, the system boots from drive A. Otherwise, it boots from drive C.
Drive C then A	The system checks drive C first. If there is a hard disk (drive C) installed, the system boots from drive C. Otherwise, it boots from drive A.
C:	The system always boots from drive C.
A:	The system always boots from drive A.

3.5.2 Onboard Communication Ports

3.5.2.1 Serial Port 1 Base Address

This parameter allows you to set the serial port 1 logical base address.

Table 3- 2 Serial Port 1 Settings

Setting	Description
3F8h	Serial port 1 with address 3F8h using IRQ4
2F8h	Serial port 1 with address 2F8h using IRQ3
3E8h	Serial port 1 with address 3E8h using IRQ4
2E8h	Serial port 1 with address 2E8h using IRQ3
Disabled	Disables serial port 1

3.5.2.2 Serial Port 2 Base Address

This parameter allows you to set the serial port 2 logical base address.

Table 3- 3 Serial Port 2 Settings

Setting	Description
3F8h	Serial port 2 with address 3F8h using IRQ4
2F8h	Serial port 2 with address 2F8h using IRQ3
3E8h	Serial port 2 with address 3E8h using IRQ4
2E8h	Serial port 2 with address 2E8h using IRQ3
Disabled	Disables serial port 2

If you assign 3F8h to serial port 1, you may only assign 2F8h or 2E8h to serial port 2.

If you assign 2F8h to serial port 1, you may only assign 3F8h or 3E8h to serial port 2.

3.5.2.3 Parallel Port Base Address

The system has one parallel port. Table 3-4 lists the options for selecting the parallel port address. You also have the option to disable the parallel port.

Table 3- 4 Parallel Port Settings

Setting	Function
3BCh (IRQ 7)	Corresponds to the parallel port with address 3BCh
378h (IRQ 7)	Corresponds to the parallel port with address 378h
278h (IRQ 5)	Corresponds to the parallel port with address 278h
Disabled	Disables the parallel port

To deactivate the parallel port, select the **`Disabled`** option. If you install an add-on card with a parallel port whose address conflicts with the onboard parallel port, the system automatically disables the onboard functions.

Check the parallel port address on the add-on card and change the address to one that does not conflict.

OPERATION MODE

This item allows you to set the operation mode of the parallel port. Table 3-5 lists the different operation modes.

Table 3- 5 Parallel Port Operation Mode Settings

Setting	Function
Standard Parallel Port (SPP)	Allows normal speed one-way operation
Standard and Bidirectional	Allows normal speed operation in a two-way mode
Enhanced Parallel Port (EPP)	Allows bidirectional parallel port operation at maximum speed
Extended Capabilities Port (ECP)	Allows parallel port to operate in bidirectional mode and at a speed higher than the maximum data transfer rate

ECP DMA CHANNEL

This item becomes active only if you select **Extended Capabilities Port (ECP)** as the operation mode. It allows you to select DMA channel 1 or DMA channel 3 depending on the available system resource.

3.5.3 Onboard PS/2 Mouse (IRQ12)

This parameter enables or disables the onboard PS/2 mouse. When set to **Enabled**, it allows you to use the onboard PS/2 mouse assigned with IRQ12. When set to **Disabled**, it deactivates the mouse and frees IRQ12 for the use of other devices.

3.5.4 Setup Password

The setup password prevents unauthorized access to the BIOS utility.

3.5.4.1 Setting a Setup Password

1. Make sure that jumper JP3 is set to pins 2-3 (bypass).

> *You cannot enter the BIOS utility if a setup password does not exist and jumper JP3 is set to pins 1-2 (check).*
>
> *The jumper JP3 is set to pins 2-3 (bypass) by default.*

2. Enter BIOS utility and select System Security.

3. Highlight the Setup Password parameter and press the ← or → key. The password prompt appears:

4. Type a password. The password may consist of up to seven characters.

> *Be very careful when typing your password because the characters do not appear on the screen.*

5. Press ENTER. A prompt asks you to retype the password to verify your first entry.

6. Retype the password then press ENTER.

   After setting the password, the system automatically sets the Setup Password parameter to **`Present`**.

7. Press ESC to exit the System Security screen and return to the main menu.

8. Press ESC to exit the BIOS utility. A dialog box appears asking if you want to save the CMOS data.

9. Select Yes to save the changes and reboot the system.

10. While rebooting, turn off the system then open the housing.

11. Set jumper JP3 to pins 1-2 to enable the password function.

The next time you want to enter the BIOS utility, you must key-in your Setup password.

3.5.4.2 Changing or Removing the Setup Password

Should you want to change your setup password, do the following:

1. Enter the BIOS utility and select System Security.

2. Highlight the Setup Password parameter.

3. Press the ← or → key to display the password prompt and key-in a new password.

   or

   Press the ← or → key and select **None** to remove the existing password.

4. Press ESC to exit the System Security screen and return to the main menu.

5. Press ESC to exit the BIOS utility. A dialog box appears asking if you want to save the CMOS data.

6. Select Yes to save the changes and reboot the system.

3.5.4.3 Bypassing the Setup Password

If you forget your setup password, you can bypass the password security feature by hardware. Follow these steps to bypass the password:

1. Turn off and unplug the system.
2. Open the system housing and set JP3 to pins 2-3 to bypass the password checking.
3. Turn on the system and enter the BIOS utility. This time the system does not require you to type in a password.

You can either change the existing Setup password or remove it by selecting **None***. Refer to the previous section for the procedure.*

3.5.5 Power On Password

The power on password secures your system against unauthorized use. Once you set this password, you have to type it whenever you boot the system.

To set a power on password, highlight the Power On Password parameter and follow the same procedure as in setting a setup password. See section 3.5.4.

3.6 Remote Diagnostic Configuration

The Remote Diagnostic Configuration menus allow you to change your RDM settings. For more details on these menus, refer to the RDM user's guide.

```
                Remote Diagnostic Configuration       Page 1/2

    Remote Console  ................ [Enabled ]

    Hidden Partition ............... [Disabled]

    Communication Protocol ......... [ N, 8, 1 ]
    COM Port Baud Rate ............. [57600] BPS
    Telephone Type ................. [Tone ]

    Remote Console Phone No.  .. [                          21]
    Dial Out Retry Times ....... [    2    ]

    Modem Initial Command .......... [                        ]

   ↑↓ = Move Highlight Bar,    → ← = Change Setting
   PgDn/PgUp = Move Screen,    F1 = Help,   Esc  =  Exit
```

```
                Remote Diagnostic Configuration       Page 2/2

    RDM Work Mode  ................. [Waiting ]
    Waiting Mode Password .......... [    1234]

    System Critical Paging No.
                   1.  [                123456]
                   2.  [                      ]
                   3.  [                      ]

    Paging Times ----- [ 1 ]

    RDM SEEPROM Verification ....... [Disabled]

   ↑↓ = Move Highlight Bar,    Esc = Exit
   Number Input, Letter Input, Symbol Input: * , - & % \ "
```

3.7 Load Setup Default Settings

Use this option to load the default settings for the optimized system configuration. When you load the default settings, some of the parameters are grayed-out with their fixed settings. These grayed parameters are not user-configurable.

The following dialog box appears when you select Load Setup Default Settings from the main menu.

```
Load Setup Default Settings
Are you sure?

     [Yes]       [No]
```

Select **[Yes]** to load the default settings.

3.8 Leaving Setup

Examine the system configuration values. When you are satisfied that all the values are correct, write them down. Store the recorded values in a safe place. In the future, if the battery loses power or the CMOS chip is damaged, you will know what values to enter when you rerun Setup.

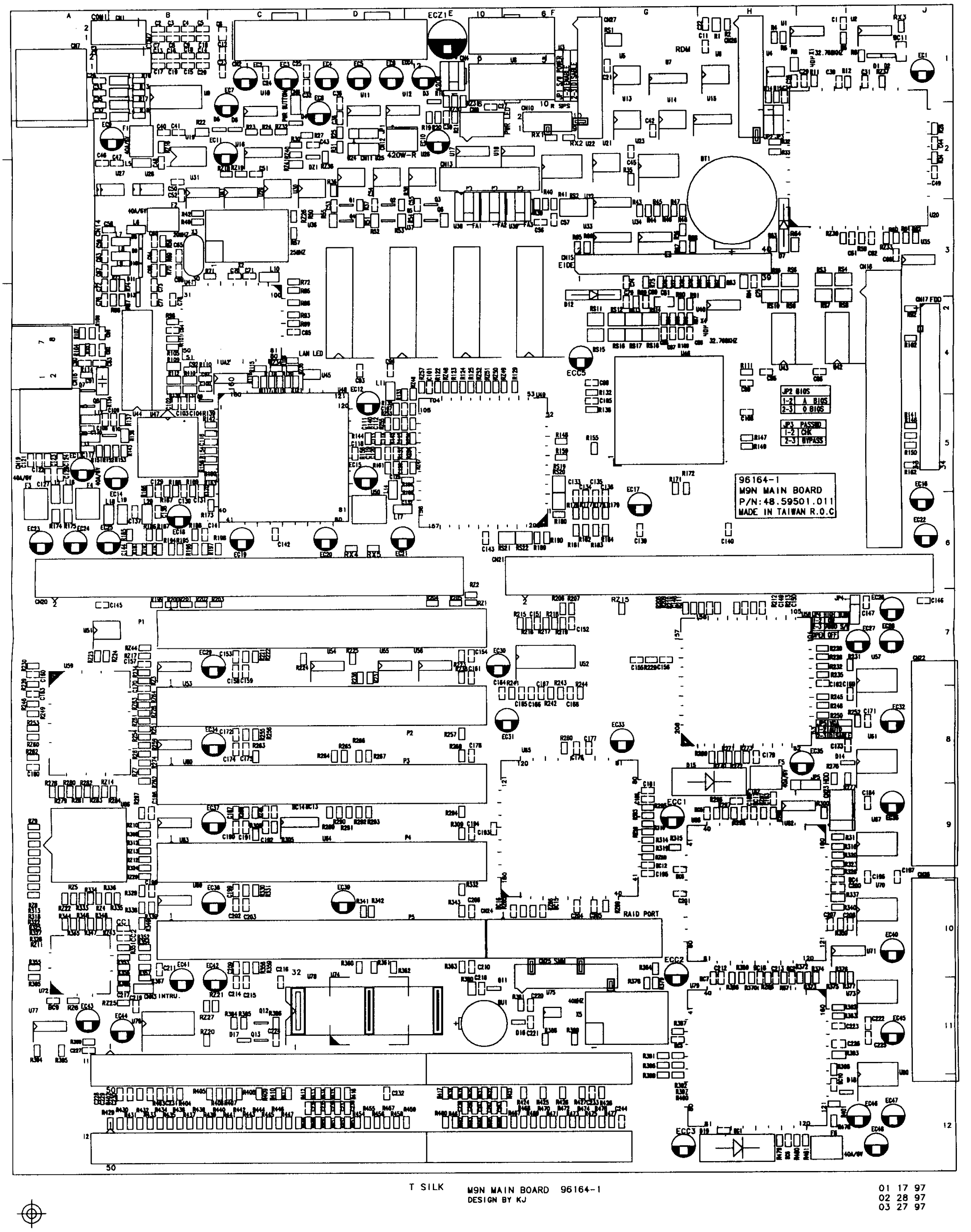
Press [ESC] to leave the system configuration setup. The following screen appears:

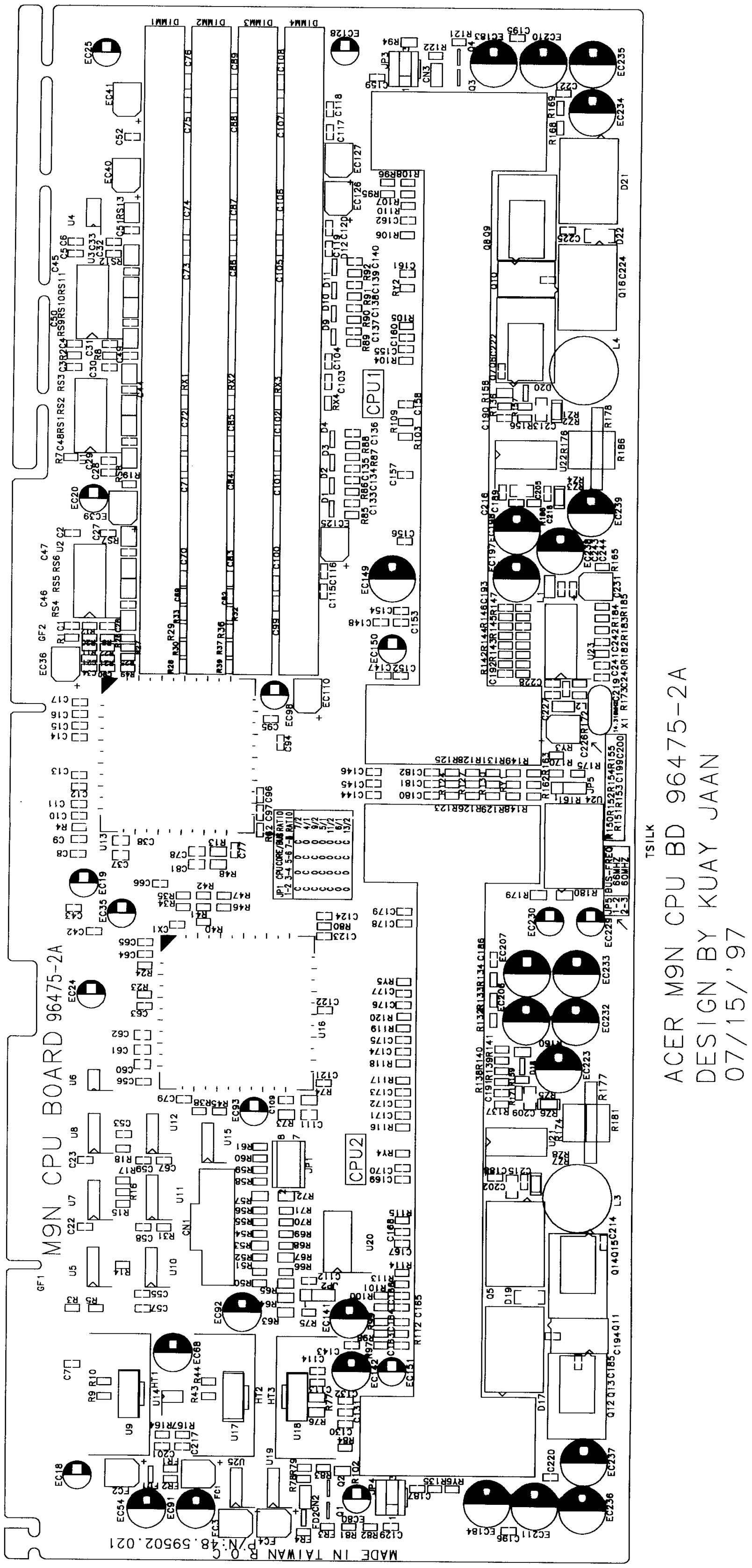
```
Do you want to save CMOS data?

     [Yes]         [No]
```

Use the arrow keys to select your response. Select **Yes** to store the new data in CMOS. Select **No** to retain the old configuration values. Press [ENTER] .

Silk Screens




M9N CPU BOARD 96475-2A
ACER M9N CPU BD 96475-2A
DESIGN BY KUAY JAAN
07/15/'97
MADE IN TAIWAN R.O.C
P/N:48.59502.021

Appendix E

BIOS POST Check Points

E.1 Power-On Self Test (POST)

The power-on self test (POST) is a BIOS procedure that boots the system, initializes and diagnoses the system components, and controls the operation of the power-on password option. If POST discovers errors in system operations at power-on, it displays error messages, generates a check point code at port 80h or halts the system if the error is fatal.

The main components on the system board that must be diagnosed and/or initialized by POST to ensure system functionality are as follows:

- Microprocessor with built-in numeric coprocessor and cache memory subsystem
- Direct memory access (DMA) controller (8237 module)
- Interrupt system (8259 module)
- Three programmable timers (system timer and 8254 module)
- ROM subsystem
- RAM subsystem
- CMOS RAM subsystem and real time clock/calendar with battery backup
- Onboard serial interface controller
- Onboard parallel interface controller
- Embedded hard disk interface and diskette drive interface
- Keyboard and auxiliary device controllers
- I/O ports:
  - RS232 serial ports
  - parallel port
  - PS/2-compatible mouse port
  - PS/2-compatible keyboard port

E.1.1 POST Check Points

When POST executes a task, it uses a series of preset numbers called check points to be latched at port 80h, indicating the stages it is currently running. This latch can be read and shown on a debug board.

Table E-1 describes the Acer common tasks carried out by POST. Each task is denoted by a unique check point. For other unique check points not listed in the following table, refer to the corresponding product service guide.

Table E- 1 Pentium II Processor Card Edge Signal List

Check Point	Description
04H	• Determines if the current booting procedure is from cold boot (press reset button or turn the system on), from warm boot (press b + a + ^), or from exiting BIOS setup. Note: *At the beginning of POST, port 64 bit 2 (8042 system flag) is read to determine whether this POST is caused by a cold or warm boot. If it is a cold boot, a complete POST is performed. If it is a warm boot, the chip initialization and memory test are eliminated from the POST routine.*
08H	• Disables non-maskable interrupt (NMI), alarm interrupt enable (AIE), periodical interrupt enable (PIE), and update-ended interrupt enable (UIE). Note: *These interrupts are disabled to avoid interrupting the POST routine.*
10H	• DMA controller (8237) test and initialization
14H	• System timer (8254) test and initialization
18H	• Memory refresh test; refresh occurrence verification (IRQ0)
1CH	• Verifies CMOS shutdown byte, battery and check sum Note: *Several parts of the POST routine require the system to be in protected mode. When returning to real mode from protected mode, the processor resets and reenters POST. To prevent re-initialization of the system, POST reads the shutdown code stored in location 0Fh in CMOS RAM. Then it jumps around the initialization procedure to the appropriate entry point. The CMOS shutdown byte verification assures that CMOS 0Fh area is fine to execute POST properly.*
1CH continued	• Initializes CMOS default setting • Initializes RTC time base Note: *The RTC has an embedded oscillator that generates 32.768 KHz frequency. To initialize RTC time base, turn on this oscillator and set a divisor to 32768 so that the RTC can count time correctly during POST. The remaining memory area is tested later.*

Table E- 1 Pentium II Processor Card Edge Signal List

Check Point	Description
2CH	• Tests 128K base memory *Note: The 128K base memory area is tested for POST execution. The remaining memory area is tested later.*
20H	• Tests keyboard controller (8041/8042) • Determines keyboard type (AT, XT, PS/2)
24H	• Tests programmable interrupt controller (8259) • Initializes system interrupt
3CH	• Sets interrupt service for POST
4CH	• Checks CPU brand, ID, and frequency
50H	• Initializes video display *Note: If the system has any display card, it should be initialized here via its I/O ROM or the corresponding initialization program.*
58H	• Displays Acer (or OEM) logo (if necessary) • Displays Acer copyright message (if necessary) • Displays BIOS serial number
5CH	• Memory test (except the 128K base memory)
60H	• Initializes SRAM cache capacity • Enables the cache function
64H	• Tests keyboard interface *Note: The keyboard LEDs should flash once.*
68H	• Enables UIE, then checks RTC update cycle *Note: The RTC executes an update cycle per second. When the UIE is set, an interrupt (IRQ8) occurs after every update cycle and indicates that over 999ms are available to read valid time and date information.*
70H	• Initializes parallel port
74H	• Initializes serial port(s)
84H	• Initializes keyboard
88H	• Sets HDD type and features (i.e. transfer speed, mode, ...) • Tests HDD controller
6CH	• Tests and initializes FDD *Note: The FDD LED should flash once and its head should be positioned.*
94H	• Initialize I/O ROM

Table E- 1 Pentium II Processor Card Edge Signal List

Check Point	Description
	Note: I/O ROM is an optional extension of the BIOS located on an installed add-on card as a part of the I/O subsystem. POST detects I/O ROMs and gives them opportunity to initialize themselves and their hardware environment.
96H	• Initializes PCI I/O ROM
A0H	• Sets time and date
B0H	• Checks power-on password • Displays configuration mode table • Booting

E.1.2 POST Error Messages

The power-on self-test (POST) is a program routine performed by the system BIOS. If there is any error during the POST routine, BIOS detects it and shows the corresponding error message on the CRT screen to guide the technical service engineer on the repair procedure.

Table E- 2 POST Error Messages

Error Message	Possible Cause and Corrective Action
Memory Error at MMMM:SSSS:OOOOh (R:xxxxh, W:xxxxh)	• DIMMs or add-on memory card may be defective. ☛ Replace the DRAM chips or the DIMMs
SM RAM Bad	• System Memory Management (SMM) is bad. ☛ Replace the DRAM chips or the DIMMs
Keyboard Interface Error	• POST detects an error in the interface between the system board and the keyboard. The keyboard circuit module may be defective. ☛ Check the keyboard interface circuit or change the keyboard.
Keyboard Error or Keyboard Not Connected	• POST detects an error in the keyboard; or the keyboard is not connected. ☛ Reconnect or replace the keyboard.
Keyboard Locked	• The keyboard lock feature prevents any access to keyboard. ☛ Unlock the keyboard.
Pointing Device Error	• The pointing device installed may be bad or the device is improperly connected. ☛ Reconnect or replace the pointing device.
Pointing Device Interface Error	• POST detects an error in the interface between the system board and the pointing device. ☛ Check the keyboard interface circuit.
Pointing Device IRQ Conflict	• The IRQ setting of add-on card and/or system board conflicted with onboard pointing device. ☛ Enter SETUP and change the setting of IRQ12.
Hard Disk 0 Error Hard Disk 1 Error Hard Disk 2 Error Hard Disk 3 Error	• The hard disk drive may be bad, type mismatched, or not properly installed. ☛ Replace the disk drive or the hard disk drive controller. Check the HDD cable connections and CMOS setup configuration.
Diskette Drive A Type Mismatch	• Diskette A (or B) may be bad, not properly

Table E- 2 POST Error Messages

Error Message	Possible Cause and Corrective Action
Diskette Drive B Type Mismatch	installed, or type mismatched. ☛ Replace diskette drive, checking its cabling and its configuration in Setup.
Diskette Drive A Error Diskette Drive B Error	• Diskette A or B may be bad. ☛ Replace the diskette drive.
Diskette Drive Controller Error	• This error is caused by any of the following: (1) The power supply cable is not connected to the diskette drive connector. (2) The diskette drive cable is not plugged to the diskette drive interface on the system board. (3) The diskette drive controller is defective. ☛ Check the diskette drive cable and its connections. If the cable is good and properly connected, the diskette drive controller may be the problem. Change the diskette drive controller or disable the onboard controller by installing another add-on card with a controller.
Serial Port 1 Conflict Serial Port 2 Conflict	• Onboard serial port address conflicts with the add-on card serial port. ☛ Change the onboard serial port address in Setup or change the add-on card serial port address.
Parallel Port Conflict	• Onboard parallel port address conflicts with the parallel port of add-on card. ☛ Change onboard parallel port address in CMOS SETUP or set the parallel port address of add-on card to others.
Real Time Clock Error	• POST detects a real-time clock error. ☛ Check RTC circuit or replace the RTC.
CMOS Battery Bad	• CMOS battery power lost. ☛ Replace the onboard lithium battery
CMOS Checksum Error	• CMOS RAM error. ☛ Run Setup again and reconfigure the system.

Table E- 2 POST Error Messages

Error Message	Possible Cause and Corrective Action
NVRAM checksum Error	• The NVRAM in the EISA model contains EISA configuration information. Accidental data writes in the NVRAM area causes an error. POST detects the error and displays the corresponding error message. ☛ Run EISA configuration utility (ECU) to restore the original EISA configuration data.
PCI Device Error	• PCI device may be bad. ☛ Check the PCI card. Replace if bad.
System Resource Conflict	• Some system resources conflict with the resources required by the PCI device. ☛ Run Setup to reconfigure the system.
IRQ Setting Error	• Wrong IRQ setting for the PCI device. ☛ Run Setup to reconfigure the system.
Expansion ROM Allocation Fail	• The I/O expansion ROM fails to allocate for the PCI device. ☛ Change the I/O expansion ROM address.

E.1.3 NMI Error Messages and Warning Messages

The non-maskable interrupt (NMI) causes the CPU routines to be interrupted and the system to be halted.

Table E- 3 NMI Error Messages and Warning Messages

Error Message	Possible Cause and Corrective Action
RAM Parity Error	• DIMMs or add-on memory card may be defective. ☛ Replace the DIMMs or the memory card, or disable parity check in Setup if the model supports it.
I/O Parity Error	• The I/O access is not correct. ☛ Check all I/O related circuits (i.e. system I/O controller, memory controller, interrupt controller, DMA controller, etc.)
Press Ctrl_Alt_Esc key to enter SETUP or F1 key to Continue...	• A system configuration error is detected, or the hardware configuration does not match the Setup configuration data in CMOS. ☛ Press b + a + ^ to reconfigure the system.
Press 1 key to enter SETUP or other key to continue...	• This message appears on the screen when a terminal instead of a console monitor is installed. ☛ Press 1 to enter Setup and check the configuration. Pressing any other key prevents entering Setup.
Press ESC to turn off NMI, or any key to reboot	• A non-maskable interrupt (NMI) occurs. ☛ Press ^ to reject NMI error or press any other key to reboot the system.
Insert system diskette and press <Enter> key to reboot	• A non-bootable diskette is detected on the diskette drive when the system boots. ☛ Insert a bootable disk in the diskette drive or remove this disk if a hard disk drive is installed.

Table E- 3 NMI Error Messages and Warning Messages

Error Message	Possible Cause and Corrective Action
Equipment Configuration Error	• The hardware configuration does not match the Setup configuration data. ☛ Run Setup and reconfigure the system.
EISA Configuration Error	• This message appears in any one of the following conditions: (1) An add-on card is plugged into the wrong expansion slot. (2) The ECU was not executed when a new add-on card is installed. (3) A old add-on card was move to another slot. ☛ Run ECU.