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RadiSys®

# **Endura**

## **LS855**

### **Product Manual**

[www.radisys.com](http://www.radisys.com)

World Headquarters

5445 NE Dawson Creek Drive • Hillsboro, OR 97124 USA  
Phone: 503-615-1100 • Fax: 503-615-1121  
Toll-Free: 800-950-0044

International Headquarters

10 Centech Park • Fringe Meadow Road, Redditch  
Worcestershire, B98 9NR • United Kingdom  
Phone: 44 1527 588800 • Fax: 44 1527 588801

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## Revision History

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1.0	First Release	September 2003
1.1	Updated power consumption figures Numerous minor corrections and updates Added mechanical drawing, 1W product SKU, product code information Added section on hard-switched power supply jumper	October 2003

## Notational Conventions

This manual uses the following conventions:

- Screen text and syntax strings appear in this font.
- All numbers are decimal unless otherwise stated ('h' indicates a hexadecimal number).
- Bit 0 is the least-significant bit. If a bit is set to 1, the associated description is true unless otherwise stated.



Warnings indicate situations that may result in physical harm to you or the hardware.



Notes indicate important information about the product.



Cautions indicate situations that may result in damage to data or the hardware.



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## Safety & Approvals Notices

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### Battery

This product contains a lithium cell.



When removing or replacing the lithium cell, do not use a conductive instrument as a short-circuit may cause the cell to explode. Always replace the cell with one of the same type. This product uses a CR2032 cell. Dispose of a spent cell promptly – do not recharge, disassemble or incinerate. Keep cells away from children.



**CAUTION!** Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of batteries according to the manufacturer's instructions.

### LAN (Local Area Network) Connector



This product may include an RJ45 LAN connector (see product options). Do not connect to anything other than an Ethernet LAN.

### Thermal Interface Material



This product may contain thermal interface material between devices and heatsinks. This can cause irritation and can stain clothing. Avoid prolonged or repeated contact with the skin and wash thoroughly with soap and water after handling. Avoid contact with eyes and inhalation of fumes. Do not ingest.

### Anti-static Precautions



This product contains static-sensitive components and should be handled with care. It is recommended that the product be handled in a Special Handling Area (SHA) as defined in EN100015-1:1992. Such an area has working surfaces, floor coverings and chairs connected to a common earth reference point. An earthed wrist strap should be worn whilst handling. Other examples of static-sensitive devices are the memory modules and the processor. Failure to employ adequate anti-static measures can cause irreparable damage to components on the motherboard.

### Safety

This product complies with the American Safety Standard UL60950 when installed in a suitable chassis.

### Electromagnetic Compatibility

This product is designed to meet the following EMC standards when installed in a suitable chassis.

FCC Class B (Title 47 of Code of Federal Regulations, parts 2 & 15, subpart B)  
 EN55022:1998 Class B  
 EN55024:1998

### Legal Directives

This product complies with the relevant clauses of the following European Directives.

Low Voltage Directive	73/23/EEC
EMC Directive	89/336/EEC

## Installation Notes

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When installing this motherboard into a suitable chassis please refer to the following notes.

- Read and save all instructions.
- Always disconnect Cord/Plug before installation or upgrade. Parts of the motherboard can remain powered even when the power supply is switched off unless the cord is disconnected.
- Pay attention to the safety warnings included in this document.
- When installing expansion cards, pay attention to the maximum loads detailed in this document. Use only UL approved peripheral cards.
- Route wiring away from sharp edges, heat sources and cooling fans.
- Pay attention to the thermal issues described in this document. The motherboard requires suitable airflow to maintain an ambient temperature within its operating range.

# Contents

---

1	Overview.....	8
1.1	Motherboard Layout.....	9
1.2	Block Diagram.....	11
1.3	Product Options.....	12
1.4	Product Order Codes.....	12
1.5	Configuration.....	13
1.5.1	Operation Mode Selection.....	13
1.5.2	Riser Control.....	14
1.5.3	BIOS Write Protection.....	14
1.5.4	Hard-switched Power Supply Jumper.....	14
1.5.5	Front Panel Connections.....	14
1.5.6	Alternate Power LED.....	15
2	Motherboard Description.....	16
2.1	Processor.....	16
2.2	System Memory.....	16
2.3	Chipset.....	17
2.4	Video.....	17
2.4.1	Dual Independent Display.....	17
2.4.2	System Memory Allocation.....	17
2.4.3	Video Modes.....	18
2.4.4	LVDS Interface.....	18
2.5	IDE Drives.....	18
2.6	Diskette Drives.....	19
2.7	Audio.....	19
2.8	Network.....	19
2.9	Standard PC I/O.....	19
2.9.1	Serial Ports.....	20
2.9.2	Parallel Port.....	20
2.9.3	Keyboard and Mouse Ports.....	20
2.10	USB Ports.....	20
2.11	General Purpose I/O Lines.....	20
2.12	CMOS RAM & RTC.....	21
2.13	Expansion Cards.....	21
2.14	System management.....	22
2.14.1	Voltage Monitoring.....	22
2.14.2	Temperature Monitoring.....	22
2.14.3	Fan Monitoring.....	22
2.14.4	Fan Control.....	23
2.14.5	Tamper Detection.....	23
2.15	Power management.....	24
2.15.1	ACPI Power States.....	24
2.15.2	ACPI Wake-up Support.....	24
2.16	Indicators.....	25
2.16.1	Power State Indicators.....	25
2.16.2	Network Status Indicators.....	25
2.16.3	I/O Panel Indicators.....	25
2.17	BIOS.....	26
2.18	Operating Systems Support.....	26
3	Specifications.....	27
3.1	Environmental.....	27
3.2	Thermal.....	27

3.3	Regulatory EMC Compliance.....	28
3.4	Regulatory Safety Compliance .....	28
3.5	Industry Compliance .....	28
3.6	Miscellaneous .....	28
3.7	Mechanical.....	29
3.7.1	Motherboard.....	29
3.7.2	I/O Shield.....	30
3.7.3	Fansink.....	30
3.8	Electrical.....	31
3.8.1	Motherboard Power Consumption .....	31
3.8.2	Power Delivery to Expansion Slots .....	32
3.8.3	Power Supply Selection .....	32
3.8.4	Power Budget.....	33
3.8.5	General Purpose I/O Lines.....	33
4	Motherboard BIOS.....	34
4.1	Configuration.....	34
4.2	Update and Recovery .....	35
4.2.1	Creating a BIOS Update Diskette .....	35
4.2.2	Updating the System BIOS .....	35
4.2.3	Creating a BIOS Recovery Diskette.....	36
4.2.4	Recovering the System BIOS .....	36
4.2.5	Updating the Flash Bootblock .....	36
4.3	Customization .....	37
4.4	BIOS Error Indications .....	38
5	Customer Support.....	41
	Appendix A Technical Reference.....	42
A.1.	I/O Map .....	42
A.2.	PCI Interrupt Allocation .....	43
A.3.	PCI Device Assignments .....	44
A.4.	SMBus Resource Allocation .....	44
A.5.	ISA Interrupt Allocation .....	45
A.6.	ISA DMA Channel Allocation .....	45
A.7.	BIOS Organization .....	46
	Appendix B Control Registers.....	47
B.1.	Index Register.....	47
B.2.	Watchdog Control .....	47
B.3.	Watchdog Kick .....	47
B.4.	Watchdog Status.....	48
B.5.	Watchdog Timeout Period .....	48
B.6.	General Purpose I/O Port 1 .....	48
B.7.	General Purpose I/O Port 2 and Control.....	49
B.8.	PWM Control.....	49
B.9.	VRM Status and EDID Control.....	50
B.10.	Controller Part Number .....	50
	Appendix C Connector Descriptions .....	51
C.1.	Connector Part Numbers .....	51
C.2.	AGP Expansion Slot (AGP card mode).....	52
C.3.	AGP Expansion Slot (ADD card mode).....	53
C.4.	PCI Expansion Slot.....	54
C.5.	PCI Slot 2 Riser Extension.....	55
C.6.	PCI Slot 3 Riser Support.....	55
C.7.	PCI Slot 4 Riser Support.....	55

C.8. ATX 12V Power Supply ..... 55  
C.9. ATX Power Supply ..... 55  
C.10. Front Panel Header ..... 55  
C.11. VGA Monitor ..... 56  
C.12. Parallel Port ..... 56  
C.13. Serial Port 1 ..... 56  
C.14. Serial Port 2 ..... 56  
C.15. Ethernet LED Header ..... 56  
C.16. RJ45 Ethernet (10/100) ..... 57  
C.17. RJ45 Ethernet (Gbit) ..... 57  
C.18. USB I/O Panel Ports ..... 57  
C.19. USB Internal Ports ..... 57  
C.20. IDE Drive Headers ..... 57  
C.21. Diskette Drive Header ..... 58  
C.22. GPIO Header ..... 58  
C.23. 30-pin LVDS PanelData (Single channel 24-bit option) ..... 58  
C.24. 30-pin LVDS Panel Data (Dual channel 18-bit option) ..... 58  
C.25. 20-pin LVDS VDL/VCL ..... 59  
C.26. LVDS Backlight Control ..... 59  
C.27. PS/2 Keyboard ..... 59  
C.28. PS/2 Mouse ..... 59  
C.29. Keyboard Header ..... 59  
C.30. Mouse Header ..... 59  
C.31. Internal Audio Headers ..... 59  
C.32. Line In and Out Jacks ..... 60  
C.33. MIC Jack ..... 60  
C.34. Processor and System Fan 1 & 2 ..... 60  
C.35. Remote Thermal Sensor ..... 60  
C.36. SMBus Header ..... 60  
C.37. Alternate Power LED ..... 60

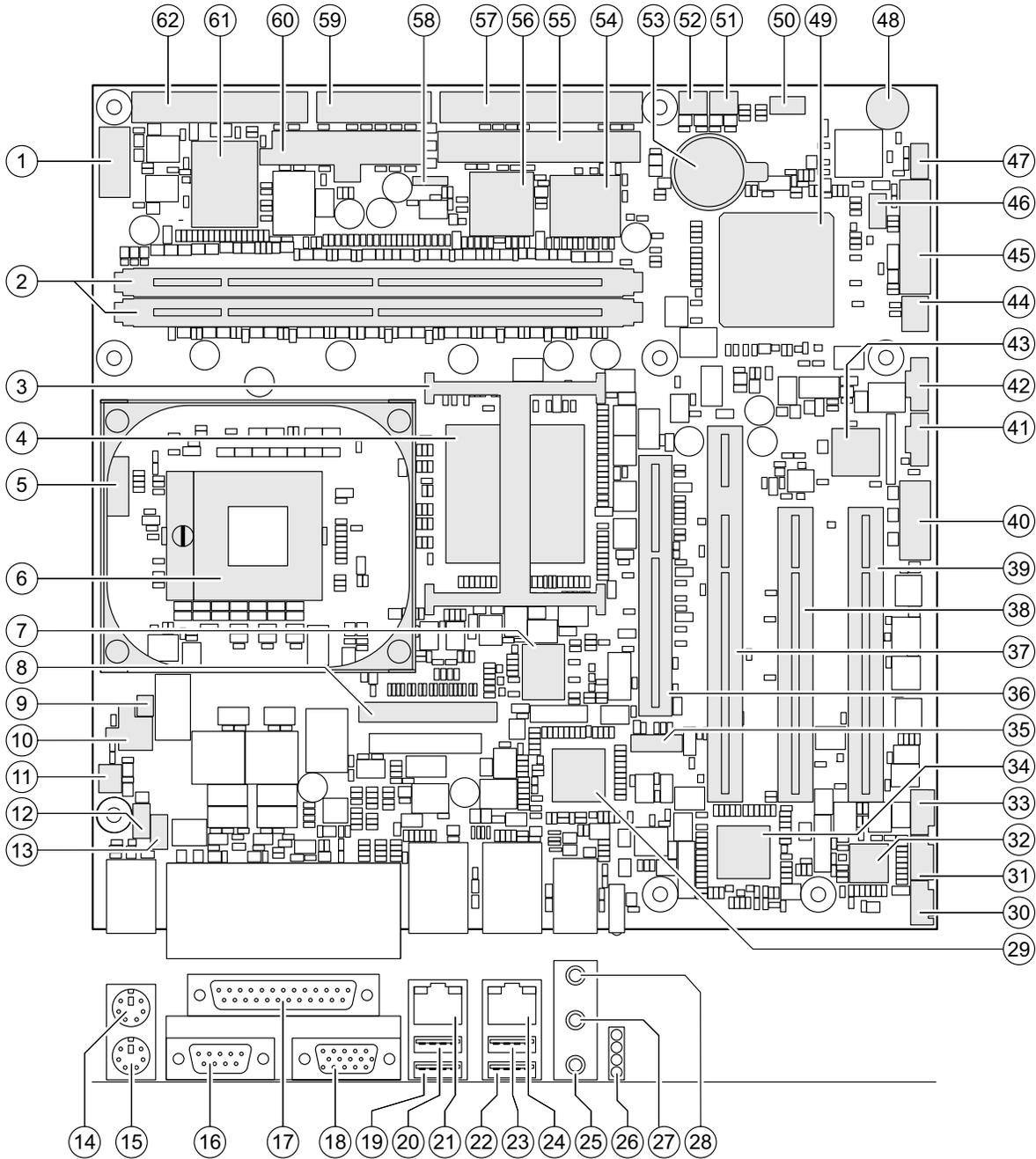
# 1 Overview

The LS855 is a microATX form factor motherboard based around an Intel Pentium M processor and an Intel 855GME chipset. It integrates a video controller supporting dual independent displays, audio, system monitoring and two Ethernet controllers on a 9.6 x 9.6-inch board. The memory controller supports DDR memory at 333MHz with ECC capability.

<b>Form Factor</b>	microATX, 9.6 x 9.6-inches
<b>Processor</b>	Intel Pentium M support 479-pin tool activated PGA socket for $\mu$ FC-PGA processor package 400MHz processor bus speed
<b>Chipset</b>	Intel 855GME GMCH with Intel ICH4 I/O hub
<b>Memory</b>	Two 184-pin DIMM sockets for PC1600/PC2100/PC2700 DDR modules Max 2GB, min 64MB memory; optional ECC
<b>Video</b>	Intel® Extreme Graphics 3D controller integrated within chipset Dual independent displays On-board LVDS flat panel support and analog VGA Support for additional digital display(s) and/or TV-out via ADD card Support for AGP 4X graphics card in lieu of internal graphics controller
<b>Audio</b>	Digital audio controller integrated within chipset AC97 v2.1 CODEC MIC, Line-out and Line-in (optional) jacks on rear panel CD input, AUX input and Line output ATAPI internal connectors On-board PC speaker (beep)
<b>Expansion</b>	Three PCI 2.2 slots, each with 3-slot riser support, one with LPC AGP4X/ADD slot with integrated retention mechanism
<b>Power Management</b>	APM, ACPI, PCI PME
<b>System Management</b>	Voltage, temperature and fan monitoring (3 fans) Lithium cell voltage monitoring Automatic fan speed control (3 fans) Programmable watchdog timer SMBus header Status LED stack on rear panel (4 LEDs)
<b>Security</b>	Optional integrated TCPA compliant TPM
<b>BIOS</b>	Phoenix FirstBIOS™ Notebook Pro-based including video BIOS and network boot (dependent on network controllers) Optionally Socketed ROM with write-protect jumpers
<b>I/O</b>	Six USB 2.0 ports - four on rear panel, two on locking headers Two RS232 serial ports – one on rear panel, one on header Bi-directional/EPP/ECP parallel port on rear panel PS/2 keyboard and mouse on rear panel (and via internal headers) General Purpose I/O lines (13) with LCD character display support
<b>Network</b>	Two Intel-based 10/100Mbps or Gbit Ethernet channels
<b>Disks</b>	Two Ultra ATA/100 interfaces with ATAPI CD, LS120 and ZIP drive support 3-mode floppy interface

## 1.1 Motherboard Layout

The figure below shows the layout of the LS855 motherboard with the major components identified.

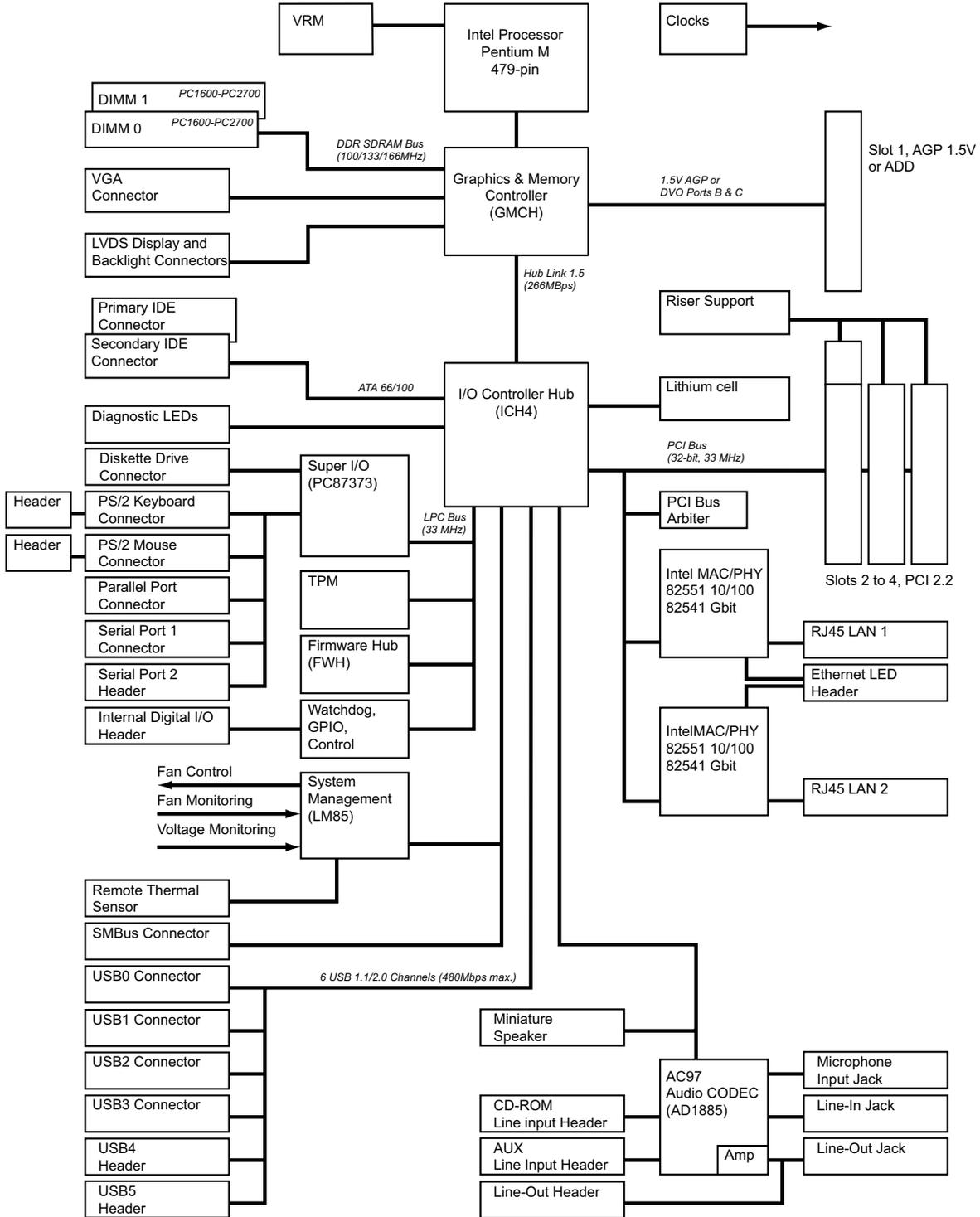


**Component Identification**

1	Serial port 2 header	22	USB 2.0 channel 2	43	PCI bus arbiter
2	PC1600-PC2700 DIMM sockets	23	USB 2.0 channel 3	44	Operating mode and riser enable jumpers
3	Chipset GMCH heatsink clip	24	Ethernet port 2 (RJ45)	45	Front panel connector
4	Chipset GMCH heatsink	25	Audio Microphone input jack	46	SMBus header
5	ITP debug port (prototypes only)	26	Diagnostic LED stack	47	Alternate Power LED header
6	479-pin socket for processor	27	Audio Line output jack	48	Miniature speaker
7	Clock generator	28	Audio Line input jack	49	I/O controller hub (ICH4)
8	LVDS Flat Panel data	29	Ethernet controller 2	50	Hard-switched PSU jumper
9	Remote thermal sensor	30	Audio CD-ROM Line input header	51	System fan 2 power connector
10	12V power connector from PSU	31	Audio AUX Line input header	52	System fan 1 power connector
11	Processor fan power connector	32	AC97 audio CODEC	53	3V Lithium cell – use CR2032
12	Mouse header	33	Audio Line output header	54	BIOS ROM (FWH)
13	Keyboard header	34	Ethernet controller 1	55	Secondary IDE connector
14	PS/2 mouse (green)	35	LVDS Flat Panel backlight control	56	Control logic
15	PS/2 keyboard (purple)	36	Slot 1 - 1.5V AGP or ADD	57	Primary IDE connector
16	Serial port 1	37	Slot 2 - PCI 2.2 with ATX riser extension	58	BIOS ROM write-protect jumper
17	Parallel port	38	Slot 3 - PCI 2.2	59	GPIO header
18	VGA monitor	39	Slot 4 - PCI 2.2	60	Primary power supply connector
19	USB 2.0 channel 0	40	Ethernet ports LED header	61	Super I/O controller
20	USB 2.0 channel 1	41	USB 2.0 channel 5 header	62	Diskette header
21	Ethernet port 1 (RJ45)	42	USB 2.0 channel 4 header		

## 1.2 Block Diagram

The figure below shows a block diagram of the LS855 motherboard.



### 1.3 Product Options

The table below lists the product options available.

Functions	LS855-L	LS855-W
Chipset	855GME	855GME
LAN	Single 10/100 (82551ER)	Single 10/100 (82551QM)
LAN Remote boot	No	No
LAN wake-up	No	Yes
Audio	Yes, 3 jacks	Yes, 3 jacks
AGP	Yes	Yes
ADD	Yes	Yes
Watchdog	Yes	Yes
Riser support	Yes	Yes
Headless	No	No
On-board LVDS	Single channel 30-pin	Single channel 30-pin
Socketed BIOS ROM	No	No
TCPA TPM	No	No

Each of the products is available with a choice of CPU speed. Consult the latest price list for the available options. Other product options are available to special order for high volume customers.

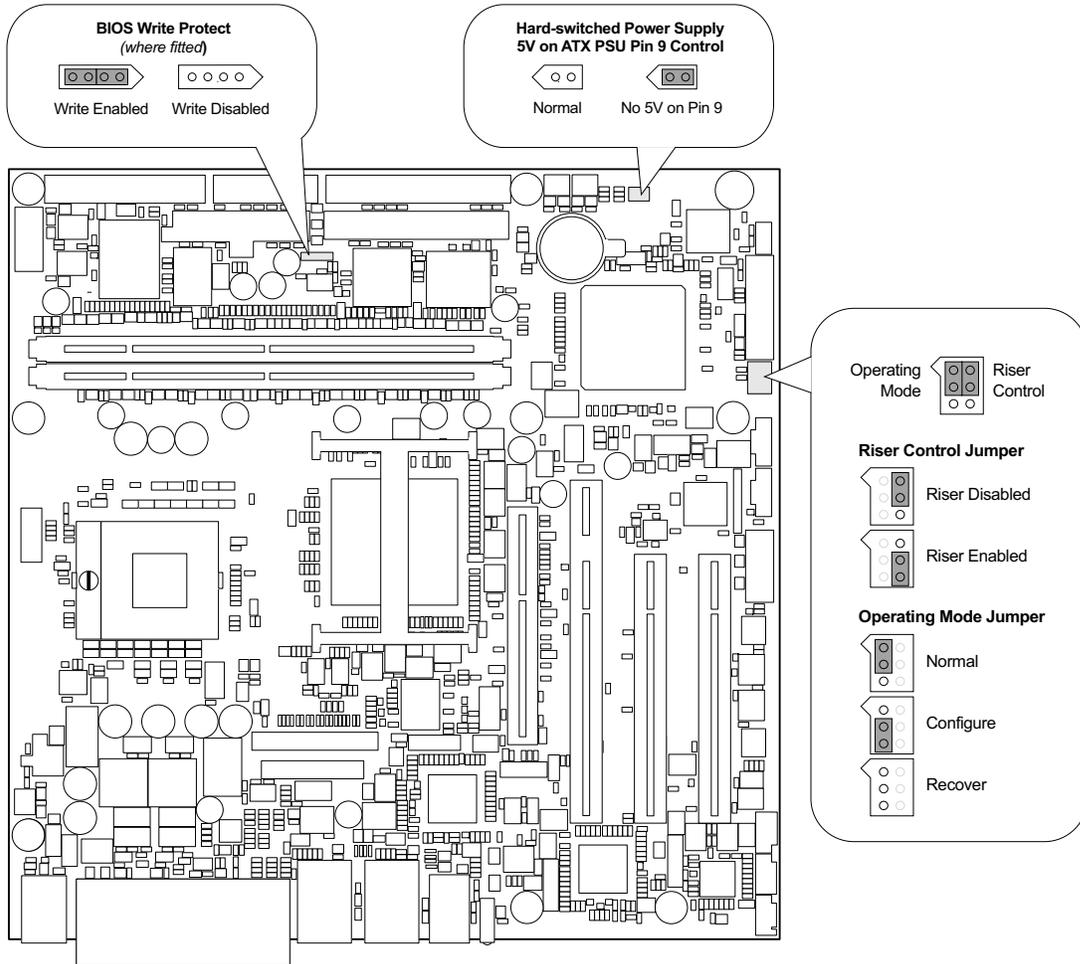
### 1.4 Product Order Codes

Each supported product configuration has an order code and the description below indicates how these codes are created.

<b>LS</b>	<b>2G</b>	<b>00</b>	<b>-</b>	<b>P</b>	<b>16</b>	<b>-</b>	<b>512</b>
<i>i</i>	<i>ii</i>	<i>iii</i>		<i>iv</i>	<i>v</i>		<i>vi</i>
<i>i</i>	Product	LS		LS855 motherboard			
<i>ii</i>	Option	1L		Single 10/100 Ethernet			
		2L		Dual 10/100 Ethernet			
		1W		Single 10/100 Ethernet with wake-up			
		2G		Dual Gbit Ethernet			
		GL		Single 10/100 Ethernet plus single Gbit Ethernet			
<i>iii</i>	Revision	00					
<i>iv</i>	Processor	P		Pentium-M Processor			
<i>v</i>	CPU Speed in 100MHz steps e.g. 16 is 1.6GHz						
<i>vi</i>	Memory capacity e.g. 512 is 512MB, 1G5 is 1.5GB, 1G is 1GB						

## 1.5 Configuration

The majority of the configuration of the motherboard is done through the Setup utility built into the BIOS – discussed later in this document. There are, however, a number of jumpers that control the operation of the motherboard as described below. Some jumpers are not fitted to certain products.



### 1.5.1 Operation Mode Selection

This jumper selects one of three operating modes for the motherboard – Normal, Configure and Recovery modes. The factory default position for this jumper selects ‘Normal’ mode.

**Normal Mode** This is the position the jumper should be in for normal operation of the motherboard. If the motherboard detects corruption in the BIOS ROM, then recovery mode will be entered regardless of the state of the jumper.

**Recovery Mode** If the jumper is in the recovery mode position or if the motherboard detects a corrupted BIOS ROM then recovery mode is entered. The motherboard will not boot and will wait until a valid recovery diskette is detected and will then copy a new BIOS into the ROM. The motherboard must be powered down and then re-powered with the jumper in the normal position before normal operation can resume.

**Configure Mode** With the jumper in this position the motherboard will automatically run the BIOS Setup utility regardless of the state of the Setup disable flag that can be set in the BIOS defaults. Additional BIOS settings are also available within Setup in this mode.

### 1.5.2 Riser Control

Install this jumper in the Enabled position to enable the additional riser support signals to be routed to the normally unused pins of the slot 3 and 4 PCI connectors. Install the jumper in the Disabled position when fitting a PCI card directly into slot 3 or 4. This jumper does not affect risers in slot 2.



*Ensure the jumper is in the Disabled position when a PCI adapter card is fitted directly into slots 3 or 4.*

### 1.5.3 BIOS Write Protection

Some motherboard configurations include a BIOS write protection jumper facility. In this case, the BIOS ROM contents cannot be updated or changed in any way (including CMOS Save/Restore and ESCD) unless the jumpers are fitted. Motherboards without this option have the write protection controlled by software alone.

### 1.5.4 Hard-switched Power Supply Jumper

This motherboard requires a 5V standby supply to operate the power control logic correctly. When a soft-switched power supply is being used, this is provided via pin 9 on the main ATX power connector. When using a hard-switched power supply that does not provide a standby rail, connect pin 9 to the main 5V-power rail. If this is not possible then fit the Hard-switch power supply jumper.



*If the power supply does not provide 5V to pin 9 of the ATX power connector, then fit the hard-switched power supply jumper to enable the motherboard to operate correctly.*



*Never fit the hard-switched power supply jumper if the power supply provides power to pin 9 of the ATX power connector as this can damage the power supply and/or motherboard.*

### 1.5.5 Front Panel Connections

The primary controls and indicators for the motherboard are connected via the front panel connector using either a single ribbon cable to a 'front panel' assembly, or using a number of small PC-standard connectors. The functions are described below. See appendix B for the connector pin-out information.

#### Power LED

This can be used to connect either a single-color LED (usually green) or a two-terminal bi-color LED (usually green/yellow) to indicate the powered status of the motherboard. In both cases, the 'green' anode should be attached to pin 2 of the front panel connector. See the Indicators section later in this document for further information.

#### Power Switch

A momentary switch should be connected between pins 6 and 8 of the power connector if the motherboard is used with a soft-switch power supply. If the switch is closed for greater than approximately 4 seconds, the motherboard will power off immediately, regardless of the state of the operating system, losing any system context information. This input is redundant when using a hard-switch power supply.

#### Reset Switch

If used, a momentary switch connected between pins 5 and 7 will cause the motherboard to restart when closed.

#### Hard Disk LED

A single color LED should be connected between pins 1 (anode) and 3 to indicate hard disk activity on either of the two ATA channels.

**Speaker**

Connect an external speaker between pins 10 and 11 or 10 and 16. This is used only for the PC 'beep' functions. The speaker should typically be 8Ω.

**Tamper Switch**

Connect a momentary switch between pins 18 and 20 to make use of the tamper detection logic of the motherboard. The switch should be open when the chassis is closed.

**1.5.6 Alternate Power LED**

The power LED function on the front panel connector is duplicated on the Alternate Power LED connector for use with LEDs cabled to a 3-pin connector. Do not use both the primary (front panel) and alternate connectors simultaneously.

## 2 Motherboard Description

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### 2.1 Processor

The LS855 motherboard supports Intel Pentium M processors in a 479-pin  $\mu$ FC-PGA package. The table below lists the supported processors. An on-board voltage regulator generates the voltage for the CPU. Both the processor voltage and the operating frequency are automatically adjusted by the motherboard to suit the installed processor.

Processor Type	Processor Speed	CPU bus speed	Cache size	Package
Intel Pentium M	1.3 GHz	400 MHz	1MB	$\mu$ FC-PGA
Intel Pentium M	1.6 GHz	400 MHz	1MB	$\mu$ FC-PGA

### 2.2 System Memory

The LS855 motherboard has two DIMM sockets to accept PC1600, PC2100 or PC2700 modules. The sockets may be populated in any order and each can accept either single or double-sided modules. The minimum total memory size is 64MB and the maximum is 2GB. The BIOS automatically configures the motherboard for the correct size, speed and type. See the Manuals, Drivers & BIOS section on the RadiSys web site at [www.radisys.com](http://www.radisys.com) for a list of memory modules that have been tested with this product.



*When using the on-board video controller, the frame buffer is held within system memory and thus less memory is available to the operating system.*

Each memory module should meet the following requirements

- Compliance with the JEDEC DDR specification
- Speed of either PC1600 (DDR200), PC2100 (DDR266) or PC2700 (DDR333)
- Inclusion of a valid serial presence detect (SPD) ROM
- The module type is 2.5V 184-pin unbuffered DDR SDRAM
- Based on 64Mb, 128Mb, 256Mb or 512Mb devices
- Capacity of between 64MB and 1GB
- 64-bit without ECC or 72-bit with ECC



*When using ECC modules, the BIOS automatically configures the motherboard to use ECC by default although this can be over-ridden via BIOS Setup. With ECC enabled, the bandwidth available to the on-board graphics controller is reduced. It is not recommended to use ECC memory when dual independent displays are required.*

## 2.3 Chipset

The motherboard is based around an Intel 855GME chipset comprising two parts -

- Graphics and memory controller hub (GMCH). This includes the processor interface, a high-performance 3D graphics controller and the system memory controller. The controller includes three digital display ports - two via the ADD/AGP slot and the third is the integrated LVDS panel interface.
- I/O controller hub (ICH4). This provides all the PCAT-compatible devices and the PCI bus interface. In addition, it integrates an Ethernet controller (not used on this product), a USB controller, an SMBus controller, a dual UltraATA/100 disk controller and power management functions.

In addition a firmware hub flash ROM contains the system BIOS, Setup utility and video BIOS and optional remote boot code.

## 2.4 Video

The video controller is integrated within the 855GME chipset GMCH and provides the features listed below.

- Dual independent display pipes
- 2D graphics with full 2D acceleration
- 3D graphics with setup and extensive rendering capabilities
- Hardware motion compensation for software MPEG2 decode
- System memory is used as frame buffer storage
- 15-way D-type for analog RGB output with VESA DDC2B capability
- Support for 1.5V AGP cards at 4X speeds
- Support for ADD cards
- Integrated LVDS flat panel interface

### 2.4.1 Dual Independent Display

The on-board graphics controller provides two data pipes to support two independent displays. The three digital display interfaces (two DVO via ADD card and one LVDS) and one analog display (15-pin VGA CRT) interface must be mapped to the two pipes. The table below shows the supported configurations. Cloned displays have identical resolution and timings.

Display Pipe A	Display Pipe B
CRT or DVO B or DVO C (or any combination as cloned displays)	LVDS
DVO B or DVO C (or both as cloned displays)	CRT
CRT	DVO B or DVO C (or both as cloned displays)

### 2.4.2 System Memory Allocation

The video controller does not have dedicated frame buffer memory but instead makes use of system memory for all its needs. This must be taken into account when the amount of system memory is chosen. When the on-board video controller is not used, it should be disabled completely via BIOS Setup to prevent system memory being allocated to the controller.

The motherboard BIOS allocates 8MB of system memory to the video controller by default to support legacy VGA graphics. The amount of system memory reported by the BIOS will reflect this reduction when the on-board video controller is enabled. Once the operating system loads, the video driver dynamically allocates further system memory dependent on availability and the

application requirement. Systems should have at least 128MB of system memory when using these graphics drivers. The amount of memory allocated is capped to 32MB for systems with between 128MB and 255MB and to 64MB otherwise.

### 2.4.3 Video Modes

The Intel 855GME chipsets and drivers support a wide variety of video modes as indicated by the table below.

Resolution	Color Depth (bpp) *	Refresh Rates (Hz)
640 x 480	8, 16, 32	60, 72, 75, 85, 100, 120
800 x 600	8	60, 70, 75, 85, 100, 120
800 x 600	16, 32	60, 72, 75, 85, 100, 120
1024 x 768	8	60, 75, 85, 100
1024 x 768	16, 32	60, 70, 75, 85, 100, 120
1152 x 864	8, 16, 32	60, 75, 85, 100
1280 x 720	8	60, 75, 85
1280 x 720	16, 32	60, 75, 85, 100
1280 x 960	8, 16, 32	60, 75, 85
1600 x 900	16	60, 75, 85, 100
1600 x 900	8, 32	60, 75, 85
1600 x 1200	8	60, 75
1600 x 1200	16	60, 75, 85
1600 x 1200	8, 16	60

\* Bits per pixel. 8bpp=256 colors, 16bpp=64k colors, 32bpp=16M colors.

### 2.4.4 LVDS Interface

The on-board graphics controller includes an LVDS flat panel interface using either a 20-pin or a 30-pin (standard products) flat cable connector for data and a 7-pin connector for the backlight control. The backlight control supports both PWM and I<sup>2</sup>C modes of operation. The three options for the data channel are shown in the table below. Contact RadiSys for non-standard configurations.

Option	Connector	Channels	Channel width
Standard	30-pin	Single	24-bit
Dual channel option	30-pin	Dual	18-bit
20-pin option	20-pin	Single	18-bit

## 2.5 IDE Drives

Two independent bus-mastering IDE interfaces are provided, each supporting ATA modes up to UltraATA/100. The following drive types are supported.

- ATA hard disks up to UltraATA/100 speeds
- ATAPI devices such as CD-ROMs
- LS120 drives

The BIOS supports logical block addressing (LBA) and extended CHS translation modes for hard disks. When booting from LS120 drives, the correct mode (floppy or hard disk) must be chosen via

the IDE drive type setting in Setup. The BIOS also supports automatic determination of ATA cable type (80- or 40-pin) for UltraATA/66 or ATA/100 drives, and 48-bit addressing for very large capacity hard disk drives (exceeding 137GB).

## 2.6 Diskette Drives

The diskette drive interface supports a single 2- or 3-mode 3.5-inch drive and 720kB, 1.2MB or 1.44MB formats. The controller is located at I/O addresses 3F0-3F7h and uses IRQ6.

## 2.7 Audio

The motherboard audio system comprises the chipset ICH4 digital audio controller and an Analog Devices AD1885 audio CODEC. Three ATAPI headers provide CD-ROM and auxiliary stereo audio Line input, and stereo audio Line output connections. Two or three 3.5mm audio jacks on the I/O panel provide connections for stereo Line output, a monaural microphone input with phantom power suitable for electret microphones and, dependent on build, a stereo Line input. The ATAPI header Line output is a duplicate of the 3.5mm jack output and care must be taken if both connectors are being used simultaneously to ensure that the combined load does not have an adverse effect on the output levels. From either connector, the Line output includes an amplifier capable of driving headphones.

An on-board miniature speaker provides standard PC speaker functionality - error 'beep', for example.

## 2.8 Network

The LS855 provides one or two Ethernet ports based around Intel controllers. Each channel has an RJ45 connector located on the I/O panel with two integrated LED indicators to provide link status information. The list below describes the features provided by each port.

- 10/100 or Gigabit options
  - 10/100 option is IEEE 802.3 10Base-T and 100Base-TX compatible
  - Gigabit option is IEEE 802.3 10Base-T, 100Base-TX and 1000Base-T compatible
- 32-bit bus-mastering PCI device
- RJ45 with two integral LEDs showing line activity, link integrity and line speed

The operation of the two indicators is described in the table below. The motherboard also supports cabling to alternate Ethernet status indicators (to a front panel assembly, for example). See the Indicators section of this document for a description of this header.

LED color	LED state	Indicates
Green/Amber	Off	10Mbps link speed
	Green	100Mbps link speed
	Amber	1Gbps link speed
Yellow	Off	No link is established
	Steady on	Link is established but there is no communication activity
	Blinking	Link is established and communication activity is detected

## 2.9 Standard PC I/O

The standard PC I/O functions serial ports, parallel ports, keyboard and mouse ports and diskette drive controller are provided via a National Semiconductor PC87373 Super I/O (SIO) device attached to the low pin count (LPC) bus from the chipset. In addition, this device provides system control functions and general-purpose I/O lines.

### 2.9.1 Serial Ports

The motherboard supports two 16C550-compatible serial ports that can operate at speeds of up to 115.2kbps. Serial port 1 is located on the I/O panel whilst serial port 2 is via a header. Each port can be assigned as COM1 through COM4 via the BIOS Setup utility.

- I/O addresses 3F8-3FFh, 2F8-2FFh, 3E8-3EFh or 2E8-2EFh
- Interrupts IRQ3 or IRQ4

### 2.9.2 Parallel Port

The motherboard has a 25 way female D-sub parallel port connector located on the rear panel. It supports the following operating modes, configured via the BIOS Setup utility.

- Standard PC-compatible parallel port
- Bi-directional parallel port
- EPP mode
- ECP mode

The I/O locations can be assigned as follows.

- I/O address 378-37Fh & 778-77Fh, IRQ5 or IRQ7
- I/O address 278-27Fh & 678-67Fh, IRQ5 or IRQ7

### 2.9.3 Keyboard and Mouse Ports

Two PS/2 style keyboard and mouse ports are provided on the rear panel. The two ports are interchangeable with the motherboard automatically detecting which peripheral is attached to which port. Both ports provide a resettable fuse protected +5V supply to the peripheral. In addition, both the keyboard and mouse ports are accessible internally via 4-way headers.

The keyboard controller is functionally equivalent to the 8042 standard and is located at I/O addresses 60-64h and uses IRQ1. The mouse shares the same controller and uses IRQ12. The keyboard controller code is from AMI.

## 2.10 USB Ports

The motherboard provides six independent USB 2.0 compliant ports, four on the I/O panel and two via internal headers, all with a resettable fuse protected +5V supply to the peripheral. The chipset includes three 2-channel USB 1.1 controllers, which allow each port to operate in USB1.1 mode, and a single 6-channel USB2.0 controller, which provides USB2.0 support to each port when a high-speed peripheral is detected.

The BIOS supports the use of a USB keyboard and/or mouse in lieu of a PS/2 device via the BIOS customization tools (the feature is disabled by default). This USB legacy support provides emulation of standard keyboards and/or mice and since it causes performance degradation should be enabled only when the operating system being used also supports USB (the emulation is automatically disabled once the operating system is running). The BIOS supports booting from USB devices.

## 2.11 General Purpose I/O Lines

In order to support products that require a small number of internal input or output lines (such as switches or LED indicators), the motherboard provides access to 13 general-purpose lines via a 20-pin header. Ten lines can be programmed as inputs or outputs (in two groups), two are input only and one is output only. It is the responsibility of the customer to provide suitable software to control these lines.

## 2.12 CMOS RAM & RTC

The chipset integrates a Motorola MC146818A compatible real-time clock (RTC) and 256 bytes of CMOS RAM that is used by the BIOS to store configuration information. A replaceable primary lithium coin cell backs up both the RTC and the CMOS RAM and provides for approximately 5 years of unpowered backup. The RTC includes a century byte and is supported by the BIOS to provide year 2000 compliance.

The lithium coin cell is a CR2032 device.

When the +5V standby power is applied to the motherboard, the RTC and the CMOS RAM are powered from that rather than the lithium cell.

## 2.13 Expansion Cards

The motherboard provides 3 bus-master PCI 2.2 compliant slots and one AGP/ADD slot. The motherboard generates the 3.3Vaux supply to these slots using the 5V standby input from the power supply. Always ensure that the 5V standby rail can support the required current when using a PCI card that makes use of the 3.3Vaux supply. The LS855 is designed to support a maximum total power consumption of 60W for all four slots (15W each, on average).

Slot 1 is the AGP/ADD slot that supports digital display adapters, ADD cards, that enable the chipset digital video ports to be used to drive flat panel monitors or to provide TV-out capabilities, dependent on the specification of the card. Motherboards fitted with the Intel 855GME option also support AGP video cards. These must be 1.5V and can operate at 4X speeds – 3.3V AGP cards cannot be used. When an AGP card is in use, the integrated video controller is always disabled.

Slots 2, 3 and 4 (the PCI slots) support 3-slot risers and two risers can be used (usually in back-to-back arrangement) to provide a maximum of 5 PCI slots in the system. Slot 2 supports a riser that meets the ATX Riser Card Specification, using a connector with a 22-pin extension to support the additional signals required. Slots 3 and 4 support 3-slot PCI risers with the additional signals provided via reserved or unused pins on the standard PCI connector. The riser enable jumper must be fitted to enable these additional signals. Do not fit the riser enable jumper when an adapter card is fitted directly into slot 3 or 4. Slot 3 also supports a 2-slot riser with access to the chipset LPC (low pin-count bus). Contact RadiSys for further information.



*Do not fit the riser enable jumper when a PCI adapter card is fitted directly into slot 3 or 4.*

When using risers, the riser slots re-use resources assigned to motherboard slots (although slots 5 and 6 do not physically exist except when risers are used). The table below indicates how the slot resources are allocated. Use risers in slots 2 and 3 or 3 and 4 to support a total of 5 slots. The connector pin-outs in appendix B indicate how the resources are assigned to the different riser slots.

	Riser in Slot 2	Riser in Slot 3	Riser in Slot 4
Slot 2 resources	X	X	
Slot 3 resources		X	
Slot 4 resources	X		X
Slot 5 resources		X	X
Slot 6 resources	X		X

## 2.14 System management

The motherboard includes hardware system management functions via the National Semiconductor LM85 device. They monitor system voltages, motherboard, processor and external temperatures, fan speed and control system fans. The following sections describe this in more detail.

### 2.14.1 Voltage Monitoring

The table below details the motherboard voltage rails monitored and their usage.

Voltage Rail	Usage on Motherboard
+12V	Serial ports, voltage regulators (including processor), fans, expansion slots.
+5.0V	Internal logic, keyboard, mouse, USB and video ports, expansion slots.
+3.3V	Chipset ICH4, firmware hub, SIO, clock generator, system monitor, audio, internal logic, TPM, expansion slots.
VCPU	Processor core voltage.
VBAT	This internal rail is used to power the RTC and the CMOS RAM.

The processor voltage regulator generates the operating voltage automatically based on the processor type jumper and the voltage requirement indicated by the processor (VID).

### 2.14.2 Temperature Monitoring

There are three thermal monitors, two of which are connected to temperature sensors on the motherboard. The first measures the motherboard temperature using a sensor contained within the LM85. This will be a localized reading dominated by the motherboard surface temperature around the component. The second temperature sensor is located on the processor die and thus accurately measures the local die temperature. Since the local die temperature fluctuates rapidly with activity, the controller within the LM85 filters the signal to produce an average temperature. Note that there is temperature deviation across the processor die that cannot be observed by this sensor. Intel provides information on this in the processor datasheet. A third sensor can be connected to the motherboard using the external sensor connector. The sensor should be a silicon diode or transistor connected as a diode, such as a Fairchild MMBT3904.

### 2.14.3 Fan Monitoring

The motherboard supports three fan monitors that check the fan tachometer signals to determine the rotational speed. Fan speeds can be monitored by software to provide early warning of a failing fan, indicated by a slower than normal rotational speed. Note that when a fan is temperature controlled, the speed is determined by the control mechanism and the fan will sometimes be intentionally slowed or stopped – monitoring software must accommodate this.

The three fan tachometer monitors are assigned to fans as follows. Fan monitor 2 is not supported.

	Usage by motherboard
Fan monitor 1	Processor fansink (see motherboard layout section)
Fan monitor 3	System fan 1(see motherboard layout section)
Fan monitor 4	System fan 2 (see motherboard layout section)

#### **2.14.4 Fan Control**

The motherboard supports individual variable speed controls for the processor fansink and the two system fans by pulse-width modulation of the fan drive output voltage. In addition to direct software control, the LM85 supports automatic fan control based on the temperature indicated by the three thermal sensors. Each sensor defines a thermal zone and the fans can then be independently assigned to these zones. Parameters defining PWM frequency, temperature range, spin-up delays etc. are programmed into the LM85 to enable automatic control. The default parameter set programmed by the BIOS can be customized.

#### **2.14.5 Tamper Detection**

The motherboard supports tamper detection security that operates via a chassis tamper switch connected to the front panel connector. When the motherboard detects this signal low the BIOS can be configured to display a warning message or to require a password at the next boot. Since the lithium cell powers the logic, the tamper detection continues to operate even if the board is unpowered.

## 2.15 Power management

The LS855 motherboard implements a number of power management features with software support for APM and ACPI. Where an operating system does not support ACPI, the motherboard defaults to using APM. An APM driver is required by the operating system in order to take advantage of the APM power management features.

### 2.15.1 ACPI Power States

An ACPI-aware operating system directs the power management of the motherboard – causing the various devices within the system to change power state as appropriate. The table below describes the ACPI power states available using the motherboard with a soft-switched power supply.

Global State	Sleep State	Device State	Description
G0	S0	C0, D0	Fully operational, all devices powered.
G1 Sleeping	S1 CPU stopped	C1, D1, D2	Sleep state. CPU is stopped but all devices are powered.
G1 Sleeping	S4 Suspend to disk	D3	All devices are unpowered except wake-up logic. Memory and system context saved to disk.
G2/S5	S5 Soft Off	D3	All devices are unpowered. Memory contents and context are lost. Wake-up possible if enabled.
G3 Mechanical Off	No power	No power	System is unpowered with no standby rails. No wake-up is possible

### 2.15.2 ACPI Wake-up Support

The table below indicates which events can cause an ACPI wake-up and from which sleep states.

Event	Sleep State	Comment
Power switch	S1, S4, S5	
RTC alarm	S1, S4	
PS/2 keyboard or mouse	S1	Ports are unpowered in S4, S5
USB device (any port)	S1	Ports are unpowered in S4, S5
On-board LAN	S1, S4, S5	Not supported on 82551ER or 82541ER-based products. Wake from S5 controlled by BIOS Setup option.
PCI PME signal	S1, S4, S5	Wake from S5 controlled by BIOS Setup option. Requires the card to use 3V3aux supply rail for power.

## 2.16 Indicators

### 2.16.1 Power State Indicators

The motherboard supports a single dual-color LED indicator that is used to show both power and message waiting status. It is possible to use a single-color LED although some functionality is lost. The table below describes how the indicator is driven when operating with both single and dual-color devices and assumes 5V standby power is available.

LED	LED state	Indicates
Single color	Off	The motherboard is powered down or in one of the ACPI sleep states (including S1).
	On	The motherboard is fully powered up (S0).
	Blinking	The motherboard is fully powered up (S0) with a message waiting (as determined by ACPI TAPI).
Dual color (green/yellow)	Off	The motherboard is powered down or in ACPI sleep states S4 or S5 (no +5V supply available).
	Green	The motherboard is fully powered up (S0).
	Yellow	The motherboard is in sleep state S1.
	Blinking Green	The motherboard is fully powered up (S0) with a message waiting (as determined by ACPI TAPI).
	Blinking Yellow	The motherboard is in sleep state S1 with a message waiting (as determined by ACPI TAPI).

### 2.16.2 Network Status Indicators

To support off-board network status indicators, a header is provided that duplicates the functions of the LEDs integrated into the RJ45 connectors. The table below shows how this connector is used.

LED color	LED state	Indicates	Channel 1 Pins	Channel 2 Pins
Green / Amber	Off	10Mbps link speed	11: Green Anode	5: Green Anode
	Green	100Mbps link speed	12: Green Cathode	6: Green Cathode
	Amber <sup>1</sup>	1Gbps link speed		
Yellow	Off	No link is established	8: Anode (+)	2: Anode (+)
	Steady on	Link is established but there is no communication activity	10: Cathode	4: Cathode
	Blinking	Link is established and activity is detected		

### 2.16.3 I/O Panel Indicators

Four software configurable indicators are available on the rear I/O panel and controlled via GPIO signals from the chipset ICH4. See the table below.

LED	GPIO	Default state after boot	Color
1 (bottom)	ICH4 GPIO18	Off	Green
2	ICH4 GPIO19	Off	Green
3	ICH4 GPIO22	On	Green
4 (top)	ICH4 GPIO23	On	Green

<sup>1</sup> Gigabit controllers only, using 2-pin bi-color green/amber LED

## 2.17 BIOS

The system BIOS is held within a flash ROM device called the firmware hub (FWH). The device is an 8Mbit part that contains the following code.

- System BIOS, POST and configuration (Setup) utility
- Video BIOS
- Product configuration information including boot logo and CMOS defaults
- Processor microcode updates
- Customizations
- Network remote boot code, dependent on product

The code is built from a number of software and data modules that can be customized and assembled with a software tool that can be provided by RadiSys. Software to support BIOS updates and crisis recovery is also available - see the Manuals, Drivers & BIOS section on [www.radisys.com](http://www.radisys.com) for BIOS updates and support software.

The configuration of the motherboard is generally automatic with intervention possible via the built-in BIOS Setup utility. The operation and feature set are described in the BIOS chapter of this document.

## 2.18 Operating Systems Support

The following operating systems are validated by RadiSys with the LS855 motherboard. Contact RadiSys for information on the support of other operating systems. See the Manuals, Drivers & BIOS section on [www.radisys.com](http://www.radisys.com) for device drivers.

- Embedded Windows XP
- Windows 2000, Windows XP
- Linux

## 3 Specifications

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### 3.1 Environmental

Parameter	State	Specification
Temperature <sup>2</sup> (ambient)	Operating	0°C to 55°C
	Storage	-40 to 85 °C
Humidity		5% to 95% non-condensing
Vibration	Operating	Random 5Hz to 2kHz, 7.7grms, 10 min. in each of 3 axes: 5Hz to 20Hz: 0.004g <sup>2</sup> /Hz ramping up to 0.04g <sup>2</sup> /Hz; 20Hz to 1000Hz: 0.04g <sup>2</sup> /Hz; 1000Hz to 2000Hz: 0.04g <sup>2</sup> /Hz ramping down to 0.01g <sup>2</sup> /Hz
	Non-operating	Sine 5Hz to 500Hz, 0.15 octave/min up and back, 10 min. dwell at 3 resonances in each of 3 axes: 5 to 50Hz swept – 0.1g; 50 to 500Hz swept – 0.25g
	Packaged	Random 5Hz to 2kHz, 9.7grms, 10 min. in each of 3 axes: 5Hz to 20Hz: 0.006g <sup>2</sup> /Hz ramping up to 0.06g <sup>2</sup> /Hz; 20Hz to 1000Hz: 0.06g <sup>2</sup> /Hz; 1000Hz to 2000Hz: 0.06g <sup>2</sup> /Hz ramping down to 0.02g <sup>2</sup> /Hz
Shock	Non-operating	30g 11ms, half-sine pulse
	Packaged	Drop test, 30 inches free fall, 10-up bulk packaging
Altitude	Operating	To 15000 ft. (4500m)
	Storage	To 40000 ft. (12000m)
ESD	Operating	4kV direct contact, 8kV air

### 3.2 Thermal

The ambient operating temperature range for the motherboard is 0 - 55°C but the selection of processor and heatsink (or fansink) can reduce the system operating range. The processor and fansink combinations normally supplied as standard with the motherboards are tested by RadiSys to the full operating range using software designed to cause maximum power dissipation in the processor. This testing is done in an environmental test chamber with forced-air circulation. The maximum operating temperature of the supplied processor and fansink combination is specified in the Endura Processor Support document, which can be found in the motherboard section of the RadiSys web site.



*Always test the final system configuration to determine if the operating temperature range limits for the motherboard and processor are being met. Failure to do so can lead to unstable operation, motherboard or processor damage and/or shortened life.*

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<sup>2</sup> See Thermal specification section. This specification must be met at all points across the motherboard.

### 3.3 Regulatory EMC Compliance

The table below lists the EMC regulations the LS855 motherboard is designed to meet when correctly installed in a suitable chassis.

Regulation
FCC Class B (Title 47 of Code of Federal Regulations, parts 2 & 15, subpart B)
EN55022:1998 Class B
EN55024:1998

### 3.4 Regulatory Safety Compliance

The table below lists the safety regulations the LS855 motherboard complies with when correctly installed in a suitable chassis.

Regulation
UL60950/07.95
CAN/CSA-C22.2 No. 950-95
IEC60950, 1991 2 <sup>nd</sup> edition with amendments 1, 2, 3, 4

### 3.5 Industry Compliance

The LS855 motherboard implements the following industry specifications.

Specification	Description	Revision
ACPI	Advanced Configuration and Power Interface Specification	1.0b
APM	Advanced Power Management BIOS Specification	1.2
ATAPI	ATA Packet Interface for CD-ROMs	2.5
ATX	ATX Motherboard Form Factor Specification	2.1
microATX	microATX Motherboard Interface Specification	1.1
AGP	Accelerated Graphics Port Interface Specification	2.0
PCI	Peripheral Component Interconnect Local Bus Specification	2.2
	PCI Power Management Interface Specification	1.1
USB	Universal Serial Bus Specification	2.0

### 3.6 Miscellaneous

Parameter	Conditions	Specification
RTC Clock accuracy	25°C, 3.3V	+/- 25 ppm max.
Processor fan drive capability	12.0V	800mA max.
System fan drive capability	12.0V	450mA max.

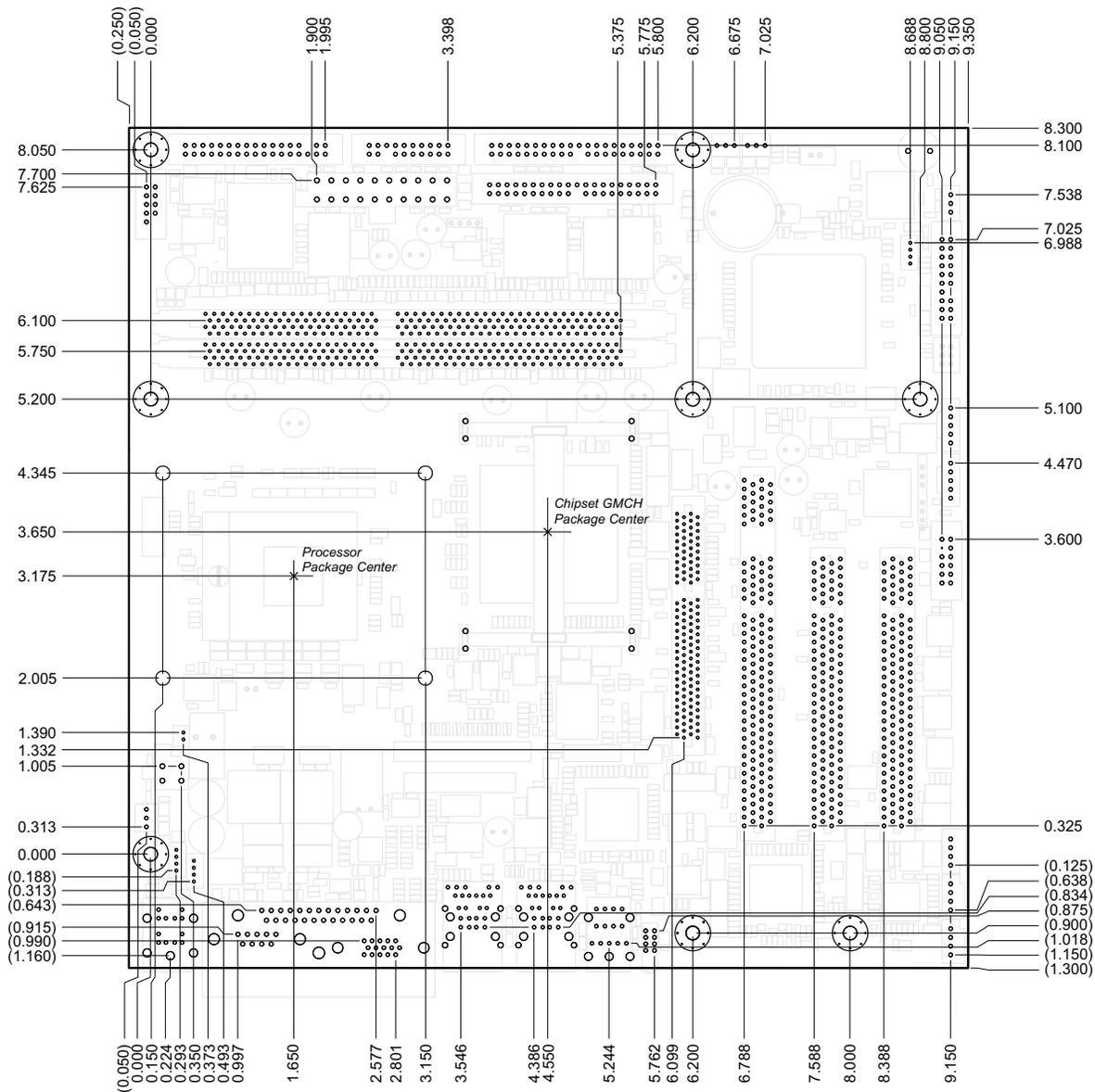
### 3.7 Mechanical

#### 3.7.1 Motherboard

The LS855 motherboard meets the microATX Motherboard Interface Specification, version 1.1 and the ATX Specification, version 2.1. It measures 9.6 x 9.6 inches and is manufactured using an 8-layer PCB with components on the topside only. The screen-printing includes the following.

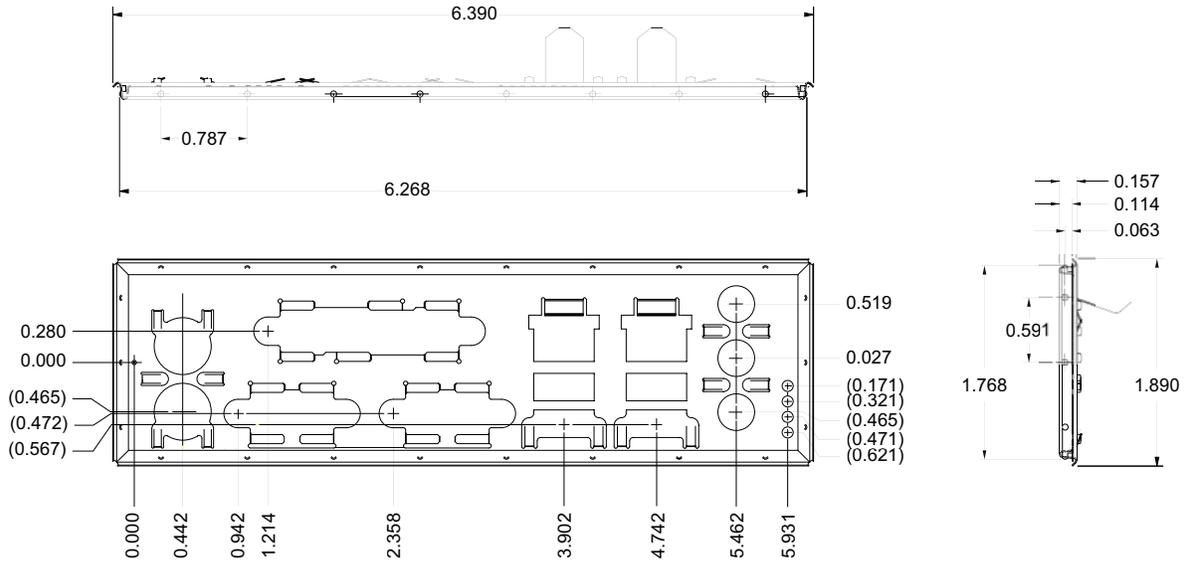
- Product Name, RadiSys part number and RadiSys branding.
- Location for serial number and product labels
- Selected component reference designators

The figure below shows the dimensions of the motherboard and the location of the rear panel connectors (referenced via pin 1 and the location of the processor, memory sockets and expansion slots.



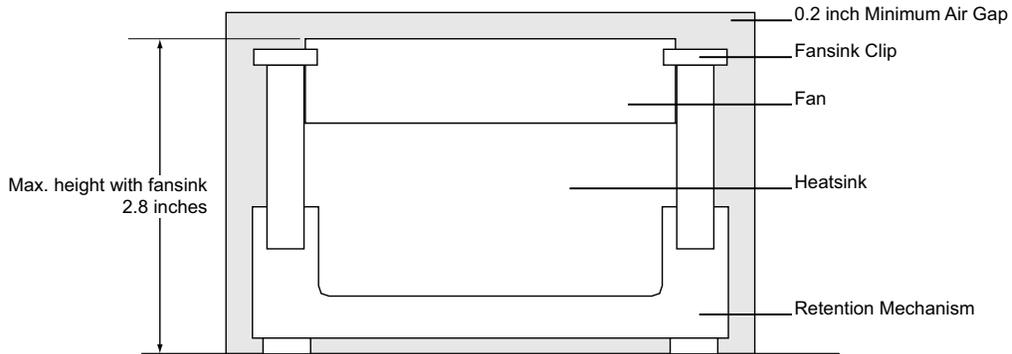
### 3.7.2 I/O Shield

I/O shields are available for the LS855 when used in a standard ATX or microATX chassis and is illustrated below. The shield press-fits into the chassis shield aperture. The drawing below includes all port apertures and is not intended to show a particular shield variant.



### 3.7.3 Fansink

The motherboard can be optionally shipped with a processor fansink, which must have a minimum air space of 0.2 inches around it to function correctly. The standard height fansink is shown in the drawing below. Contact RadiSys for lower profile solutions.



### 3.8 Electrical

#### 3.8.1 Motherboard Power Consumption

The motherboard power consumption is highly dependent on the processor, memory and devices attached and also on the software that is running and the power state that the board is in. The figures given in the table below are designed as a guide to the power requirements that should be expected under selected conditions. They should not be interpreted as maximum requirements.

The figures are based on measurements of a real system configured in the following manner.

Memory	2 off 512MB DDR PC2100 DIMM modules
Drives	Powered independently
Video	On-board
Network	On-board (dual LAN, not operating)

#### Intel Pentium M at 1.3GHz with 400MHz processor bus

Mode	Motherboard Current					Power
	+3.3V	+5V	+12V (combined)	-12V	+5Vsby	Total
MS-DOS Prompt without power management	2.8A	0.2A	0.9A	21mA	4mA	22W
Windows 2000 desktop idle	2.7A	0.1A	0.3A	21mA	4mA	14W
Windows 2000 stress test	5.3A	0.2A	1.2A	21mA	4mA	34W
Windows 2000 standby	2.2A	0.1A	0.2A	21mA	4mA	11W
Windows 2000 hibernate	0A	0A	0A	0A	110mA	0.6W
Windows 2000 shutdown	0A	0A	0A	0A	300mA	1.5W

#### Intel Pentium M at 1.6GHz with 400MHz processor bus

Mode	Motherboard Current					Power
	+3.3V	+5V	+12V (combined)	-12V	+5Vsby	Total
MS-DOS Prompt without power management	2.9A	0.2A	1.3A	21mA	4mA	27W
Windows 2000 desktop idle	2.7A	0.1A	0.4A	21mA	4mA	15W
Windows 2000 stress test	5.5A	0.2A	1.7A	21mA	4mA	40W
Windows 2000 standby	2.2A	0.1A	0.3A	21mA	4mA	12W
Windows 2000 hibernate	0A	0A	0A	0A	110mA	0.6W
Windows 2000 shutdown	0A	0A	0A	0A	300mA	1.5W

### 3.8.2 Power Delivery to Expansion Slots

The table below indicates the maximum current that should be drawn from each PCI or AGP expansion slot or the total for each riser - do not exceed these ratings. PCI slots are limited to 25W in total on the main +5.0V and +3.3V supplies, all of which can be drawn from either voltage rail. The maximum combined power consumption of all slots in the system must not exceed 60W. The figures for the riser are for the total current/power delivered to the riser through the motherboard. If more is required, the riser must draw power from an additional source such as a separate power connector from the PSU.

Maximum Expansion Slot Current						
	+1.5V	+3.3V	+5V	+12V	-12V	+3.3Vaux <sup>3</sup>
AGP	8.0A (3W) <sup>4</sup>	6.0A (20W)	2.0A (10W)	1.0A (12W)	100mA (1.2W)	375mA/20mA (1.3W/0.1W)
PCI	N/A	7.6A (25W) <sup>5</sup>	5.0A (25W) <sup>5</sup>	0.5A (6W)	100mA (1.2W)	375mA/20mA (1.3W/0.1W)
Riser	N/A	7.6A (25W)	8.0A (40W)	0.8A (10W)	300mA (3.6W)	415mA/60mA (1.4W/0.1W)



*Do not exceed the limits for each slot or voltage rail shown in the table above or the limit of 60W for the combined power consumption of all expansion slots in the system.*

### 3.8.3 Power Supply Selection

The motherboard is designed to operate with an ATX compatible power supply, as defined in section 3 of the microATX 1.1 specification. The provision of a 5V standby power rail is optional but, if not provided, the soft-switched power supply control features of the motherboard cannot be used. In this case either the main 5V should be connected in its place or the hard-switched PSU jumper fitted (refer to the Configuration section of this document). Where the standby rail is provided, ensure it is capable of providing sufficient current for the motherboard, particularly for the motherboard LAN controllers and when an adapter card that draws current from the auxiliary 3.3V supply is used. The ATX -5.0V rail is not used by the motherboard.

Voltage Rail	Tolerance	Voltage Rail	Tolerance
+5.0V DC	± 5% <sup>6</sup>	+3.3V DC	± 5%
+12.0V DC	± 5%	+5.0V DC standby	± 5%
-12.0V DC	± 10%		



*When operating with a hard-switched power supply, the BIOS should be customized with the PSU flag in the enclosure data set to 'Hard-Switched' using the tools described in the BIOS Customization section of this document.*



*Ensure the power supply can support the required load current on all rails – failure to meet this can cause damage to the power supply or the motherboard. Pay particular attention to the 5V Standby power requirement – the LAN controllers are powered from this rail.*



*The power supply must be properly approved by a third party agency for use in IEC/EN/UL/CSA 60950 applications.*

<sup>3</sup> One wake-enabled PCI/AGP card at 375mA and the remainder at 20mA.

<sup>4</sup> The 8.0A is a maximum AC (transient) switching current. Average current is 2.0A maximum.

<sup>5</sup> The combined PCI slot power consumption via the +3.3V and +5.0V supplies is a maximum of 25W.

<sup>6</sup> To meet the USB output supply voltage specification, the minimum +5V should be 4.90V.

### 3.8.4 Power Budget

The table below gives an example power budget for the motherboard with processor, memory and expansions cards fitted. The figures are based on the maximum figures from the motherboard power consumption section of this document (measured under stress testing except for the standby rail) and they should not be interpreted as typical values. Before choosing a power supply, always create a power budget for your system. These figures yield a total power requirement of 175W.

	Motherboard Current					Power
	+3.3V	+5V	+12V	-12V	+5Vsby	
Motherboard	5.6A	0.2A	1.3A	0.03A	0.29A	40W
Keyboard		0.3A				1.5W
Mouse		0.1A				0.5W
Six USB ports		3.0A				15.0W
Slots (total)	18.2A*	12.0A*	2.5A	0.3A	0.45A	95.9W
Fans			1.7A			20.4W
Front panel		0.1A				0.5W
Video DDC channel		0.05A				0.3W
<b>Total</b>	<b>23.8A*</b>	<b>15.8A*</b>	<b>5.5A</b>	<b>0.33A</b>	<b>0.74A</b>	<b>175W</b>

\*These cannot be drawn simultaneously - total combined for all slots and both rails power is 60W

### 3.8.5 General Purpose I/O Lines

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>IH</sub>	Input High Voltage		2.0	5.5	V
V <sub>IL</sub>	Input Low Voltage		-0.3	0.8	V
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 3.6V, V <sub>CC</sub> = max		5	μA
		V <sub>IN</sub> = 0V, V <sub>CC</sub> = max		-5	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -3.2mA	2.4		V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 24mA <sup>7</sup>		0.5	V

<sup>7</sup> Total I<sub>OL</sub> of outputs within each port must not exceed 64mA, for ports 1 and 2

## 4 Motherboard BIOS

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### 4.1 Configuration

The motherboard BIOS includes a Setup utility that can be used to both view and modify the board's configuration. The settings are stored in CMOS RAM with the default settings held in the flash ROM. To start the utility, press the F2 key when prompted. If 'silent-boot' is on (logo displayed) then press the ESC key to show the start-up messages.

The display is divided into four areas.

- The top bar shows the five main menus
- The large left area shows the options
- The large right area displays help text specific to the highlighted option or menu
- The bottom bar shows the action of the active keys

The primary menus are briefly described in the table below. The help text describes each option more fully. Many options have sub-menus.

Menu	Options
Main	Product description including processor and memory fitted. Date and time.
Information	Product information Status of system monitors
Configuration	Chipset configuration. Processor cache control. PCI space configuration. I/O devices configuration. Hard disk drive options. Action after AC-reconnect. Power savings modes and timers. Passwords and permissions.
Boot	Selects device boot order. Operating system type (ACPI etc.). Start-up display mode (silent-boot etc.).
Exit	Save with or without changes. Load/save default settings (from flash ROM).

## 4.2 Update and Recovery

This section describes how to update the code and data held in the BIOS ROM. The process should be undertaken with care and must not be interrupted. A recovery mechanism is also described that enables a corrupted BIOS ROM (as a result of an interrupted update, for example) to be repaired.

Updates are available online from the RadiSys site in the form of a compressed image (ZIP) of a number of files. Using the software contained in the ZIP file, you must first create a flash diskette that is then used for the update or recovery process. Included in the ZIP file is a 'Readme.txt' file that contains information on the update and instructions on how to use it. Always read this document before proceeding as it may contain updates to the descriptions below.

The update process assumes you have a PC that can be used to create an update diskette and that the system to be updated or recovered has a diskette drive attached.



*Updating the BIOS is a process that should be undertaken with caution. Always complete the process before powering-down or restarting the motherboard – failure to do this may result in a corrupted BIOS that will require recovery.*

### 4.2.1 Creating a BIOS Update Diskette

Follow the steps below. You need a PC with Microsoft MS-DOS, Windows 95 or Windows 98 and a blank diskette.

1. Obtain the update ZIP file from the Manuals, Drivers & BIOS section on the RadiSys web site, [www.radisys.com](http://www.radisys.com).
2. Unzip the contents to an empty directory on your hard drive.
3. Insert a blank diskette into the floppy drive.
4. Run CRISDISK from the directory created in step 2 to create the update diskette
5. Follow the steps as directed. A copy of MS-DOS 'Format.com' must be available for CRISDISK to complete successfully.

### 4.2.2 Updating the System BIOS

The system BIOS can be updated from MS-DOS without changing jumpers as described below. It is recommended that you create a recovery diskette (described later) before updating the BIOS. This operation does not affect the customization area in the BIOS. If you use the BIOS Setup utility CMOS Save and Restore functions to save a set of defaults, you will need to recreate and re-save these once the update is complete.

1. Create an update diskette as described above.
2. Boot the system to be updated into MS-DOS without memory managers or boot from the update diskette.
3. If you did not boot from the update diskette, do the following.
  - A. Insert the update diskette into the floppy drive.
  - B. Change the MS-DOS directory to match the floppy drive's directory.
  - C. Type UPDATE and press Enter.
4. Follow the instructions to initiate the update. When it is finished, the following message appears:

```
Flash memory has been successfully programmed
PRESS ANY KEY TO RESTART THE SYSTEM
If the system does not restart
TURN THE POWER OFF, THEN ON
```

5. Turn off the system power and re-boot. The motherboard will boot using RadiSys defaults.

If the update operation fails for any reason (if it was interrupted, for example), and the motherboard will no longer operate, then the BIOS must be recovered.

### 4.2.3 Creating a BIOS Recovery Diskette

Follow the steps below. You need a PC with Microsoft MS-DOS, Windows 95, Windows 98 or Windows NT and a blank diskette.

1. Obtain the update ZIP file from the Manuals, Drivers & BIOS section on the RadiSys web site, [www.radisys.com](http://www.radisys.com).
2. Unzip the contents to an empty directory on your hard drive.
3. Insert a blank diskette into the floppy drive.
4. Run CRISDISK /R from the directory created in step 2 and follow the steps as directed to create the recovery diskette. A copy of MS-DOS 'Format.com' must be available for CRISDISK to complete successfully.

### 4.2.4 Recovering the System BIOS

The recovery diskette should be used to recover a system BIOS when the motherboard no longer operates after a failed BIOS update operation. The process is described below.

1. Remove the operating mode selection jumper to place the board into the recover mode (see Configuration section of this document).
  - A. Turn off the power.
  - B. Remove any covers to gain access to the jumper.
  - C. Remove the jumper from the operating mode selection block
2. Insert the recovery diskette into the floppy drive.
3. Power up the motherboard. You will hear the following audio signals from the on-board speaker. If you cannot hear the speaker, wait for approximately 1 minute after all activity has stopped to ensure the operation has completed.

Beep code	Definition
One short beep	BIOS update begins.
One long beep	BIOS update is finished.
Three beeps	This indicates an error.

4. Power down the motherboard.
5. Refit the jumper into the normal operating position and replace the system cover(s).
6. Power up the motherboard. The recovery process is now complete and the product should boot normally.

### 4.2.5 Updating the Flash Bootblock

There is an area of the BIOS ROM, the bootblock, which is normally not updated. It contains code to perform the recovery process and data that identifies the motherboard. Occasionally, a BIOS release may require this bootblock area to be updated and the update disk will do this automatically. However, exercise caution when attempting such an update as a damaged bootblock area means that the motherboard may need to be returned to RadiSys for repair.



*Exercise caution when updating BIOS that includes a bootblock update. If this process is interrupted, the motherboard cannot be recovered and must be returned to RadiSys for repair.*

### 4.3 Customization

There are a number of features of the BIOS that can be customized and the software to accomplish this is contained within the BIOS OEM kit ZIP file that can be obtained from the Manuals, Drivers & BIOS section on the RadiSys web site, [www.radisys.com](http://www.radisys.com). The 'Readme.txt' file also contained in this ZIP provides updated customization information and should be read before proceeding.

The process involves creating a new update disk that contains the customized BIOS. The steps below will guide you through the process.

1. Obtain both the update and OEMKIT ZIP files from the Manuals, Drivers & BIOS section on the RadiSys web site, [www.radisys.com](http://www.radisys.com).
2. Unzip the contents of the update ZIP to an empty directory on your hard drive.
3. Unzip the contents of the OEMKIT ZIP to the same directory as step 2. This may replace some files.
4. Replace the 'P6upd.bin' file with a customized version if required (see description below).
5. Run MAKEBIOS to create the customized binary.
6. Create the update diskette by running CRISDISK /O with a blank diskette in the floppy drive and following the instructions.
8. Using a reference or 'gold' board, update its BIOS with the diskette created in step 6 above using the standard update procedure.
9. Re-boot the board and run the BIOS Setup utility.
10. Configure the board as required.
11. From the Exit menu, save the new settings to flash and re-boot the board with the update disk still in the floppy drive.
12. There should be no reported difference between disk and ROM BIOS versions at this point and you will be prompted to read-back the BIOS. Select this to extract the motherboard ROM image and save it to the update disk, replacing the BIOS binary in the file BIOS.ROM.
13. The diskette is now a fully customized update disk. Save the BIOS.ROM file back to the directory on your hard disk used in step 2, replacing the previous version.
14. Create a new version of the update disk by running CRISDISK (with no switches) with a blank diskette in the floppy drive and following the instructions.

Intel microprocessors allow for their microcode to be updated by the BIOS to workaround some outstanding errata. Each processor type and revision has a unique update image and the BIOS supports a maximum of four contained in the 'P6upd.bin' file. To customize the processor microcode update selections, create a new version of this file by concatenating four microcode updates in binary form - these can be obtained from Intel.

## 4.4 BIOS Error Indications

Once the motherboard powers-up the BIOS code runs Power-On-Self-Test software to check that the motherboard is operating correctly. During this process, the code writes an 8-bit value to an error port at various code checkpoints. If a fatal error is determined, then the error code indicates the last successful checkpoint reached. The BIOS will attempt to write this code to the display. The error port (I/O location 80h) can be read via “off-the-shelf” Debug cards. The table below lists the checkpoint codes.

There are a number of checkpoints that also generate an audible ‘beep’ code on failure using the standard PC speaker (also routed through the motherboard audio system). The beep codes are made up of up to 4 groups of short beeps and are also listed below.

Once the video is enabled further errors generated during and after POST are sent to the video display as text messages. These messages are always displayed unless the motherboard is configured for silent boot or headless (no keyboard, mouse or display) operation.

BIOS POST Checkpoint Codes			
02h	Verify Real Mode	6Ch	Display shadow message
03h	Disable NMI	6Eh	Display non-disposable segments
04h	Get CPU type	70h	Display error messages
06h	Initialize system hardware	72h	Check for configuration errors
08h	Initialize chipset registers with initial POST values	74h	Test real-time clock
09h	Set in POST flag	76h	Check for keyboard errors
0Ah	Initialize CPU registers	7Ah	Test for key lock on
0Bh	Enable CPU cache	7Ch	Set up hardware interrupts vectors
0Ch	Initialize cache to initial POST values	7Eh	Test coprocessor if present
0Eh	Initialize I/O	80h	Disable onboard I/O ports
0Fh	Initialize local bus IDE	81h	Late device initialization
10h	Initialize Power Management	82h	Detect and install external RS232 ports
11h	Load alternate registers with initial POST values	83h	Configure IDE controller
12h	Restore CR0	84h	Detect and install external parallel ports
13h	Reset PCI BM	85h	Initialize PCI PCC devices
14h	Initialize keyboard controller	86h	Re-initialize onboard I/O ports
16h	BIOS ROM checksum	87h	Configure MCD devices
17h	Pre-size DRAM	88h	Initialize BIOS Data Area
18h	8254 timer initialization	89h	Enable NMI
1Ah	8237 DMA controller initialization	8Ah	Initialize Extended BIOS Data Area
1Ch	Reset Programmable Interrupt Controller	8Bh	Initialize mouse
20h	Test DRAM refresh	8Ch	Initialize floppy controller
22h	Test 8742 Keyboard Controller	8Eh	Execute auto-typing
24h	Set ES segment to register to 4GB	8Fh	Hard disk controller fast pre-initialization

<b>BIOS POST Checkpoint Codes</b>			
26h	Enable A20	90h	Initialize hard disk controller
28h	Autosize DRAM	91h	Initialize local bus hard disk controller
29h	Initialize PMM	92h	Disable unused PCI clocks
2Ah	Clear 512KB base RAM	93h	Build MPTABLE for multiprocessor boards
2Ch	Test 512KB base address lines	95h	Install CDROM for boot
2Eh	Test low byte of 512KB base memory	96h	Clear huge ES segment register
2Fh	Pre-System Shadow	97h	Fix up MP table
30h	Test high byte of 512KB base memory	98h	Search for option ROMs (beep for bad checksum)
32h	Test CPU bus-clock frequency	99h	Check for SMART HDD
33h	Initialize PDM	9Ah	Shadow option ROMs
34h	Test CMOS RAM	9Ch	Set up Power Management
35h	Initialize alternate chipset registers	9Dh	Initialize security
36h	Warm start shutdown entry point	9Eh	Enable hardware interrupts
37h	Reinitialize the chipset	9Fh	(Second) HDD fast initialization
38h	Shadow system BIOS ROM	A0h	Set time of day
39h	Reinitialize the cache	A2h	Check keylock
3Ah	Auto-size cache	A4h	Initialize typematic rate
3Ch	Configure advanced chipset registers	A8h	Erase F2 prompt
3Dh	Load alternate registers with CMOS values	AAh	Scan for F2 keystroke
3Eh	Read HW	ACh	Enter SETUP
40h	Set Initial CPU speed	A Eh	Clear in-POST flag
42h	Initialize interrupt vectors	B0h	Check for errors
44h	Initialize BIOS interrupts	B2h	POST done--prepare to boot operating system
45h	Core Device Init	B4h	One beep before boot
46h	Check ROM copyright notice	B5h	Quiet boot end/Display MultiBoot menu
48h	Check video configuration against CMOS	B6h	Check password (optional)
49h	Initialize PCI bus and devices	B8h	Clear global descriptor table
4Ah	Initialize all video adapters in system	B9h	Prepare to boot
4Bh	Display QuietBoot™ screen	BAh	DMI
4Ch	Shadow video BIOS ROM	BBh	Initialize BCVS
4Eh	Display copyright notice	BCh	Clear parity checkers
50h	Display CPU type and speed	BDh	Boot Menu
51h	Initialize EISA board	BEh	Clear screen (optional)
52h	Test keyboard	BFh	Check virus and backup reminders
54h	Set key click if enabled	C0h	Try to boot with INT19

<b>BIOS POST Checkpoint Codes</b>			
56h	Enable keyboard	C1h	Initialize PEM
58h	Test for unexpected interrupts	C2h	PEM log
59h	Initialize PDS	C3h	PEM Display
5Ah	Display prompt "Press F2 to enter SETUP"	C4h	PEM sys error initialization
5Bh	CPU cache off	C5h	Dual CMOS
5Ch	Test RAM between 512KB and 640KB	C6h	Docking initialization
5Eh	Base Address	C7h	Late docking initialization
60h	Test extended memory	D0h	Interrupt handler error
62h	Test extended memory address lines	D2h	Unknown interrupt error
64h	Jump to UserPatch1	D4h	Pending interrupt error
66h	Configure advanced cache registers	D6h	Initialize option ROM error
68h	Enable external and CPU caches	D8h	Shutdown error
69h	PM set up SMM	DAh	Extended Block Move
6Ah	Display external cache size	DCh	Shutdown 10 error
6Bh	Load custom defaults	DFh	A20 Error

<b>Checkpoint Code</b>	<b>Beep Code</b>
16h BIOS ROM checksum	1-2-2-3
20h Test DRAM refresh	1-3-1-1
22h Test 8742 Keyboard Controller	1-3-1-3
28h Autosize DRAM	1-3-3-1
29h Initialize PMM	1-3-3-2
2Ch Test 512KB base address lines	1-3-4-1
2Eh Test low byte of 512KB base memory	1-3-4-3
34h Test CMOS RAM	1-4-3-1
3Ah Auto-size cache	1-4-3-3
46h Check ROM copyright notice	2-1-2-3
58h Test for unexpected interrupts	2-2-3-1
90h Initialize hard disk controller	3-2-1-1
98h Search for option ROMs (beep for bad checksum)	1-2
B4h One beep before boot	1
DFh A20 Error	4-2-4-4

## 5 Customer Support

RadiSys Online Support can be found at [www.radisys.com](http://www.radisys.com) and includes device drivers, BIOS updates, support software and documentation. See the Manuals, Drivers & BIOS section.

RadiSys hotline numbers for the US and Canada are

Support: (800) 438-4769  
 Service: (800) 256-5917



Online specifications and reference material:

Specification	Description	Location
ACPI	Advanced Configuration and Power Interface specification	<a href="http://www.acpi.info">www.acpi.info</a>
AGP	Advanced Graphics Port Interface Specification	<a href="http://www.agpforum.org">www.agpforum.org</a>
APM	Advanced Power Management specification	<a href="http://www.microsoft.com/hwdev/archive/BUSBIOS/amp_12.asp">www.microsoft.com/hwdev/archive/BUSBIOS/amp_12.asp</a>
Intel Pentium M processor	Intel Pentium M processor datasheet	<a href="http://developer.intel.com/design/mobile/pentiumm/pentiummoverview.htm">http://developer.intel.com/design/mobile/pentiumm/pentiummoverview.htm</a>
Intel 855GME GMCH <sup>8</sup>	Intel 855GME chipset	<a href="http://developer.intel.com/design/chipsets/mobile/855GME.htm">http://developer.intel.com/design/chipsets/mobile/855GME.htm</a>
Intel ICH4	Intel ICH4 datasheet	<a href="http://developer.intel.com/design/chipsets/datashts/290744.htm">http://developer.intel.com/design/chipsets/datashts/290744.htm</a>
ATX, microATX	Form factor specifications	<a href="http://www.formfactors.org">www.formfactors.org</a>
PCI	PCI local bus specification	<a href="http://www.pcisig.com">www.pcisig.com</a>
DDR SDRAM DIMMs	Memory module specifications	<a href="http://developer.intel.com/technology/memory/">http://developer.intel.com/technology/memory/</a> <a href="http://www.jedec.org/">http://www.jedec.org/</a>
SMBus	System management bus	<a href="http://www.smbus.org">www.smbus.org</a>
USB	Universal Serial Bus specification	<a href="http://www.usb.org/developers">www.usb.org/developers</a>
VESA	Video Electronics Standards Association	<a href="http://www.vesa.org">www.vesa.org</a>

<sup>8</sup> This Intel link describes the 8255GME chipset using the ICH4-M I/O controller hub but this product uses the ICH4 variant of the I/O controller hub described in the link below.

## Appendix A Technical Reference

### A.1. I/O Map

Address (hex)*	Description
0000 – 000F	DMA controller 1
0020 – 0021	Interrupt controller 1
002E – 002F	SIO control registers
0040 – 0043	Timer counter
0060 – 0064	Keyboard and mouse controller
0062, 0066	Motherboard control registers
0070 – 0071	RTC and CMOS RAM
0080 – 008F	DMA controller page registers (for channels 1 and 2)
0092	PC compatible Port 92 (fast A20 and PIC)
00A0 – 00A1	Interrupt controller 2
00B2 – 00B3	Advanced power management (APM) control registers
00C0 – 00DF	DMA controller 2
00F0	Floating point error control
0170 – 0177	Secondary IDE controller
01F0 – 01F7	Primary IDE controller
0278 – 027F	Parallel port, LPT2
02E8 – 02EF	COM4 serial port
02F8 – 02FF	COM2 serial port
0374 – 0376	Secondary IDE controller
0378 – 037F	Parallel port, LPT1
x3B0 – x3BB	VGA controller
x3C0 – x3CF	EGA controller registers
x3D4 – x3DA	CGA controller registers
03F0 – 03F5	Flexible diskette controller
03F6 – 03F7	Primary IDE controller
03E8 – 03EF	COM3 serial port
03F8 – 03FF	COM1 serial port
04D0 – 04D1	Interrupt controller
0678 – 067A	ECP registers for parallel port LPT2
0778 – 077A	ECP registers for parallel port LPT1
0CF8 – 0CFF	PCI configuration address and data registers
1000 – 105F	ACPI registers
1060 – 107F	TCO controller
1200 – 12FF	AC97 audio mixer

Address (hex)*	Description
1300 – 133F	AC97 audio master
1800 – 182F	SIO GPIO and control logic
FFA0 – FFA7	Primary IDE bus master registers
FFA8 – FFAF	Secondary IDE bus master registers
Dynamically assigned	USB controller (four) (32 locations on 32-byte boundary)
Dynamically assigned	SMBus controller (16 locations on 16-byte boundary)
Dynamically assigned	LAN controllers (two) (4096 locations on a 4096-byte boundary)

\* An 'x' prefix for the address indicates that only the low-order 10 address bits are decoded.

## A.2. PCI Interrupt Allocation

In order to share PCI interrupts efficiently, the routing of the PCI interrupts INTA - INTD to the motherboard PCI interrupts PIRQE – PIRQH are rotated for each slot. Thus the PCI card INTA signals for the PCI slots are spread across these four motherboard inputs. Interrupt routing for the riser slots is determined by the riser design.

Device	PIRQA	PIRQB	PIRQC	PIRQD	PIRQE	PIRQF	PIRQG	PIRQH
Slot 1 (AGP4X)	INTA	INTB	-	-	-	-	-	-
Slot 2 (PCI 2.2)	-	-	-	-	INTA	INTB	INTC	INTD
Slot 3 (PCI 2.2)	-	-	-	-	INTD	INTA	INTB	INTC
Slot 4 (PCI 2.2)	-	-	-	-	INTC	INTD	INTA	INTB
VGA controller	INTA	-	-	-	-	-	-	-
Ethernet controller 1	INTA	-	-	-	-	-	-	-
Ethernet controller 2	-	INTA	-	-	-	-	-	-
USB UHCI controller 1	INTA	-	-	-	-	-	-	-
USB UHCI controller 2	-	-	-	INTB	-	-	-	-
USB UHCI controller 3	-	-	INTC	-	-	-	-	-
USB EHCI controller	-	-	-	-	-	-	-	INTD
SMBus controller	-	INTB	-	-	-	-	-	-
AC97 controller	-	INTB	-	-	-	-	-	-

**Example.** From the table above, the INTA interrupt from a card plugged into slot 2 would be routed to the motherboard PIRQE.

### A.3. PCI Device Assignments

Device	IDSEL	Bus Number	Device Number	Function Number
Chipset host bridge and memory controller	-	0	0	0
AGP bridge	-	0	1	0
Graphics controller, first display pipe, with compatibility support	-	0	2	0
Graphics controller, second display pipe	-	0	2	1
PCI bridge	-	0	30	0
LPC bridge (Includes DMA, timers, PIC, APIC, RTC, power & system management, GPIO)	-	0	31	0
IDE controller	-	0	31	1
SMBus controller	-	0	31	3
AC97 audio controller	-	0	31	5
USB UHCI controller 1	-	0	29	0
USB UHCI controller 2	-	0	29	1
USB UHCI controller 3	-	0	29	2
USB EHCI controller	-	0	29	7
Slot 1 (AGP4X)	AD16	2	0	-
Slot 2 (PCI 2.2)	AD17	2	1	-
Slot 3 (PCI 2.2)	AD18	2	2	-
Slot 4 (PCI 2.2)	AD19	2	3	-
Slot 5 (PCI 2.2, via riser only)	AD20	2	4	-
Slot 6 (PCI 2.2, via riser only)	AD21	2	5	-
Ethernet controller 1	AD23	2	7	0
Ethernet controller 2	AD24	2	8	0

The PCI slots and the Ethernet controller are behind a virtual bridge to PCI bus 2 implemented by the chipset ICH4. An AGP card, when present, resides on PCI bus 1.

### A.4. SMBus Resource Allocation

Address	Description
1010 000X	Memory module 1
1010 001X	Memory module 2
1101 001X	Clock synthesizer

## A.5. ISA Interrupt Allocation

Whilst the motherboard does not include an ISA bus, it includes an ISA-compatible interrupt controller (PIC) in order to be compatible with AT standard architecture. The interrupts are allocated as described in the table below.

Interrupt	Description
IRQ0	System Timer
IRQ1	Keyboard Controller
IRQ2	Cascade interrupt
IRQ3	COM2, COM1 or unassigned
IRQ4	COM1, COM2 or unassigned
IRQ5	Parallel port or unassigned
IRQ6	Floppy
IRQ7	Printer port or unassigned
IRQ8	Real time clock/CMOS RAM
IRQ9	Unassigned
IRQ10	Unassigned
IRQ11	Unassigned
IRQ12	PS/2 mouse or unassigned
IRQ13	Floating point unit
IRQ14	Primary IDE or unassigned
IRQ15	Secondary IDE or unassigned
NMI	PCI PERR and SERR signals

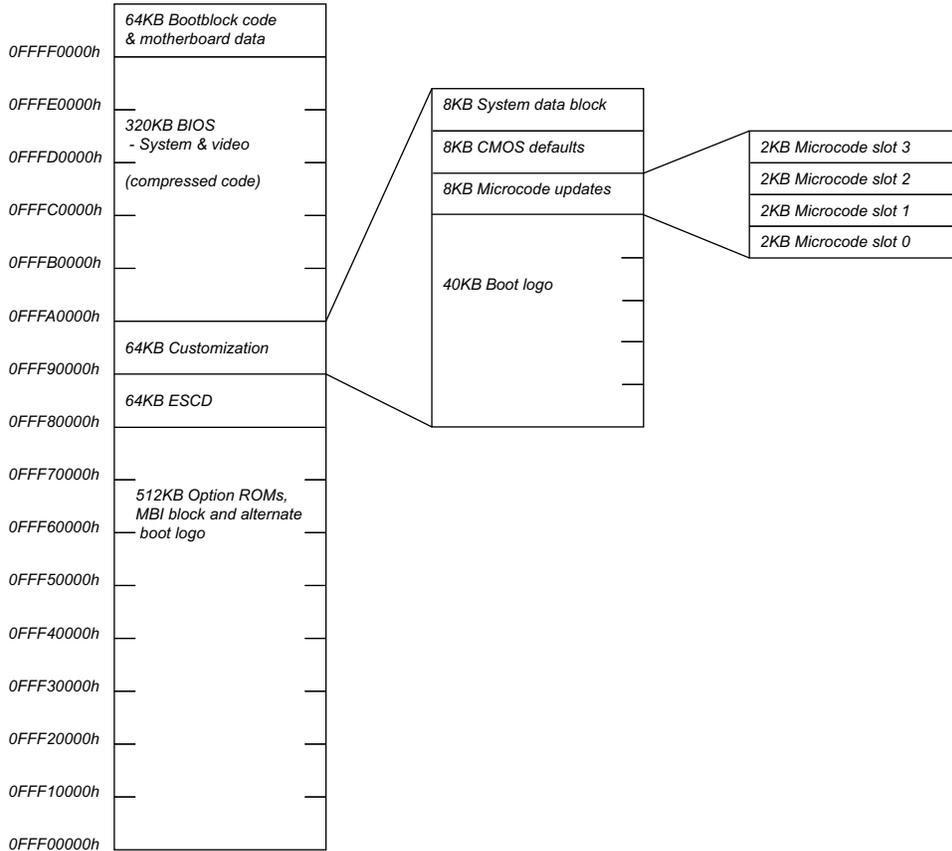
## A.6. ISA DMA Channel Allocation

Whilst the motherboard does not support an ISA bus, it includes an ISA-compatible DMA controller in order to be compatible with AT standard architecture. The DMA channels are allocated as described in the table below.

DMA Channel	Description
Channel 0	Unassigned 8-bit channel
Channel 1	Unassigned 8-bit channel
Channel 2	Floppy controller or unassigned 8-bit channel
Channel 3	ECP parallel port or unassigned 8-bit channel
Channel 4	Cascade channel
Channel 5	Unassigned 16-bit channel
Channel 6	Unassigned 16-bit channel
Channel 7	Unassigned 16-bit channel

## A.7. BIOS Organization

The BIOS ROM is an 8Mbit device containing sixteen symmetrical 64KB blocks. The diagram below shows how the ROM is used to store code and control information. The addresses shown refer to the ROM image at the top of the 4GB-address space. Note that the system BIOS segment is compressed in this image. When the BIOS runs, the code is uncompressed in real-time and the resulting code and data image is found at physical address 0E0000h through 0FFFFFFh.



## Appendix B Control Registers

### B.1. Index Register

<b>Index register</b>								I/O location 062h
7	6	5	4	3	2	1	0	Read only, Read/write
Version				Index				Default vvvv1010b

Version:

A read-only field containing the software version number for the logic

0000 Version 0

Index:

- 0000 Watchdog Control
- 0000 Watchdog Kick
- 0000 Watchdog Status
- 0001 Watchdog Timeout Period
- 0010 General Purpose I/O Port 1
- 0011 General Purpose I/O Port 2 and Control
- 1000 PWM Control
- 1001 Part Number, low digits
- 1010 VRM Status and EDID Control
- 1011 Part Number, high digits

### B.2. Watchdog Control

<b>Watchdog and Power Control</b>								I/O location 066h, WO Index = 0
7	6	5	4	3	2	1	0	Write only
Prescale				RES	SMI	WEN	0	Default 0000000b

Prescale: 4-bit value to set the watchdog counter period  
0..15 16..1s period (a value of 1010b gives a period of 6 seconds)

RES, Reset after second timeout:

- 0 No reset
- 1 Force system reset after second watchdog timeout

SMI, Generate SMI after first timeout:

- 0 No SMI
- 1 Generate SMI after first watchdog timeout

WEN, Watchdog enable:

- 0 Disable watchdog timer
- 1 Enable and start watchdog timer

### B.3. Watchdog Kick

<b>Watchdog and Power Control</b>								I/O location 066h, WO Index = 0
7	6	5	4	3	2	1	0	Write only
Don't care							1	Default 0000000b

### B.4. Watchdog Status

<b>Watchdog and Power Control</b>								I/O location 066h, RO Index = 0
7	6	5	4	3	2	1	0	Read only
Prescale				TO2	TO1	WEN	0	Default N/A

Prescale: 4-bit value to set counter period (copy of data written)

TO1, First timeout:

- 0 First timeout has not occurred
- 1 Timer has expired at least once

TO2, Second timeout:

- 0 Second timeout has not occurred
- 1 Timer has expired twice

WEN, Timer enable:

- 0 Timer is disabled
- 1 Timer is enabled and counting

### B.5. Watchdog Timeout Period

<b>Watchdog timeout period</b>								I/O location 066h, R/W Index = 1
7	6	5	4	3	2	1	0	Read/write
Watchdog timeout period								Default 11111111b

Timeout period:

- 0 Do not use (causes immediate timeout)
- 1-255 Timeout period in units of 1 x prescale value seconds

### B.6. General Purpose I/O Port 1

<b>General purpose I/O port 1</b>								I/O location 066h, R/W Index = 2
7	6	5	4	3	2	1	0	Read/write
P17	P16	P15	P14	P13	P12	P11	P10	Default 00000000b

P17 – P10, GPIO Port 1 data:

When programmed as an output, the GPIO port 1 bit follows the value written into this register and reads reflect the value written. When programmed as inputs, writes are ignored and a read follows the state of the GPIO port 1 signal. Direction control is via the GPIO port 2 and control register.

## B.7. General Purpose I/O Port 2 and Control

<b>General purpose I/O port 2 and control</b>								I/O location 066h, R/W Index = 3
7	6	5	4	3	2	1	0	Read/write
D201	D157	D104	P24	P23	P22	P21	P20	Default 00000000b

P21 – P20, GPIO Port 2 data:

When programmed as an output, the GPIO port 2 bit follows the value written into this register and reads reflect the value written. When programmed as inputs, writes are ignored and a read follows the state of the GPIO port 2 signal. Direction control is via the D201 control.

P22, GPIO Port 2 data:

This bit is output only. GPIO port 2 bit 2 follows the value written into this register and reads reflect the value written.

P24 - P23, GPIO Port 2 data:

These bits are input only. Writes to these bits have no effect, reads reflect the state of the GPIO port 2 bits 4 and 3 respectively.

D104, GPIO Port 1 bits 0 – 4 direction control:

- 0 GPIO bits 10 – 14 are inputs
- 1 GPIO bits 10 – 14 are outputs

D157, GPIO Port 1 bits 5 – 7 direction control:

- 0 GPIO bits 15 – 17 are inputs
- 1 GPIO bits 15 – 17 are outputs

D201, GPIO Port 2 bits 0 – 1 direction control:

- 0 GPIO bits 20 – 21 are inputs
- 1 GPIO bits 20 – 21 are outputs

## B.8. PWM Control

<b>PWM control</b>								I/O location 066h, R/W Index = 8
7	6	5	4	3	2	1	0	Read/write
Reserved				PWM Control				Default 00000000b

PWM Control:

Determines the pulse width of the PWM output.

### B.9. VRM Status and EDID Control

<b>Processor Identification</b>							I/O location 066h, RO Index = 10	
7	6	5	4	3	2	1	0	Read only
EDID	Rsvd	VID5	Reserved					Default N/A

EDID, LVDS port EDID ROM enable:

- 0 On-board LVDS EDID is disabled (EDID via panel)
- 1 On-board LVDS EDID is enabled (panel EDID ignored)

VID5, Processor voltage ID bit 5(selected by processor):

Returns an inverted copy of bit 5 of the voltage identification value presented by the processor.

### B.10. Controller Part Number

<b>Controller Part Number, low digits</b>							I/O location 066h, RO Index = 9	
7	6	5	4	3	2	1	0	Read only
Part Number, byte 1								Default N/A

<b>Controller Part Number, high digits</b>							I/O location 066h, RO Index = 11	
7	6	5	4	3	2	1	0	Read only
Part Number, byte 2								Default N/A

Part number format is 97-xyy-0v where v is version number (top 4 bits of index register), xx is the byte 2 value and yy is the byte 1 value. BCD encoding is used for all digits.

Byte 1 is 69h  
Byte 2 is 42h.

The programmed part number is 97-4269-0v for production motherboards.

## Appendix C Connector Descriptions

Connector views in the following sections are shown from the motherboard side.

### C.1. Connector Part Numbers

The various motherboard connectors are listed in the table below along with the part number of one of the approved vendors. The list is intended to assist in the selection of mating connectors.

Connector	Part Number	Type
I/O panel dual USB	Foxconn UB1112C-81	Dual vertically stacked USB
I/O panel 10/100 RJ45 over dual USB	Bel 0812-1X1T-03	RJ45 with LEDs and transformer over dual USB, 10/100
I/O panel Gbit RJ45 over dual USB	Foxconn JFM31U1C-3401W	RJ45 with LEDs and transformer over dual USB, Gbit
I/O panel PS/2 keyboard and mouse	Foxconn MH11067-PD2	Stacked 6-way mini-DIN
I/O panel VGA monitor	Foxconn DZ11A37-P9	15-way high-density female D-sub
I/O panel parallel port	Foxconn DM11352-PR3	25-way female D-sub
I/O panel serial port	Foxconn DT10122-P5T	9-way male D-sub
Serial port 2 header	Foxconn HL20051-P5	2 by 5-way shrouded header
Fan drive headers	Foxconn HF06030	3-way with locking ramp
Primary and secondary IDE	Foxconn HL20201-D2	40-pin shrouded header
Diskette drive	Foxconn HL20171-P4	34-pin shrouded header
GPIO header	Foxconn HL20101-L7	2 by 10-way shrouded header
Processor socket	Foxconn PZ47903-2741-01	479-pin ZIF PGA, Tool activated
DIMM sockets	Foxconn AT09217-D1	184-pin, 2.5V DDR SDRAM
Keyboard and mouse headers	Foxconn HF55040	4-pin 2mm headers
AGP connector, slot 1	Foxconn EE06217-BUB	1.5V with retention mechanism
PCI connector, slot 2	Foxconn EH07117-DW	5V signaling with riser extension
PCI connector, slots 3, 4	Foxconn EH06007-GU-V	5V signaling
Ethernet LED header	Foxconn HL07061-P7	2 by 6-way shrouded header
Front panel header	Foxconn HC19107-L6	2 by 10-way header
ATAPI CD-ROM header	Foxconn HF14040-P1	4-way header with latch, black
ATAPI Line input header	Foxconn HF14040-NP1	4-way header with latch, white
ATAPI Line output header	Foxconn HF14040-YP1	4-way header with latch, yellow
Triple stack audio jacks	Foxconn JA3333L-G01	Triple vertically stacked 3.5mm
Double stack audio jacks	Foxconn JA23331-G16	Double vertically stacked 3.5mm
Remote thermal sensor	Foxconn HF55020	2-pin 2mm header
Internal USB headers	Foxconn HF01051	5-pin locking ATAPI-style, black
SMBus header	Foxconn HF55040	4-pin 2mm header
Lithium cell holder	Kun Chang KR01-005	Top loading, CR2032
Power Supply, main	Foxconn HM20100-HP1	2 by 10-way ATX power header
Power Supply, 12V	Foxconn HM20020-P1	2 by 2-way ATX power header
Alternate power LED header	Foxconn HB11037	3-pin header
LVDS Panel data	JAE FI-X30S-HF	30-pin 1mm flat cable
LVDS Panel data	JAE FI-SE20P-HF10	20-pin 1.25mm flat cable
LVDS Panel backlight control	Tyco 440372-7	7-pin 1.25mm header

## C.2. AGP Expansion Slot (AGP card mode)

The AGP/ADD slot supports only 1.5V signaling.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	+12V	B1	<i>Not Used</i> <sup>10</sup>	A34	VDDQ1.5	B34	VDDQ1.5
A2	<i>Not Used</i> <sup>9</sup>	B2	+5V	A35	AD22	B35	AD21
A3	<i>Reserved</i>	B3	+5V	A36	AD20	B36	AD19
A4	<i>Not Used</i> <sup>10</sup>	B4	<i>Not Used</i> <sup>10</sup>	A37	GND	B37	GND
A5	GND	B5	GND	A38	AD18	B38	AD17
A6	INTA#	B6	INTB#	A39	AD16	B39	C/BE2#
A7	RST#	B7	CLK	A40	VDDQ1.5	B40	VDDQ1.5
A8	GNT#	B8	REQ#	A41	FRAME#	B41	IRDY#
A9	+3.3V	B9	+3.3V	A42	KEY	B42	KEY
A10	ST1	B10	ST0	A43	KEY	B43	KEY
A11	<i>Reserved</i>	B11	ST2	A44	KEY	B44	KEY
A12	PIPE#	B12	RBF#	A45	KEY	B45	KEY
A13	GND	B13	GND	A46	TRDY#	B46	DEVSEL#
A14	WBF#	B14	<i>Reserved</i>	A47	STOP#	B47	VDDQ1.5
A15	SBA1	B15	SBA0	A48	PME#	B48	PERR#
A16	+3.3V	B16	+3.3V	A49	GND	B49	GND
A17	SBA3	B17	SBA2	A50	PAR	B50	SERR#
A18	SBSTB#	B18	SBSTB	A51	AD15	B51	C/BE1#
A19	GND	B19	GND	A52	VDDQ1.5	B52	VDDQ1.5
A20	SBA5	B20	SBA4	A53	AD13	B53	AD14
A21	SBA7	B21	SBA6	A54	AD11	B54	AD12
A22	<i>Reserved</i>	B22	<i>Reserved</i>	A55	GND	B55	GND
A23	GND	B23	GND	A56	AD9	B56	AD10
A24	<i>Reserved</i>	B24	+3.3VAUX	A57	C/BE0#	B57	AD8
A25	+3.3V	B25	+3.3V	A58	VDDQ1.5	B58	VDDQ1.5
A26	AD30	B26	AD31	A59	ADSTB0#	B59	ADSTB0
A27	AD28	B27	AD29	A60	AD6	B60	AD7
A28	+3.3V	B28	+3.3V	A61	GND	B61	GND
A29	AD26	B29	AD27	A62	AD4	B62	AD5
A30	AD24	B30	AD25	A63	AD2	B63	AD3
A31	GND	B31	GND	A64	VDDQ1.5	B64	VDDQ1.5
A32	ADSTB1#	B32	AD_STB1	A65	AD0	B65	AD1
A33	C/BE3#	B33	AD23	A66	<i>Not Used</i>	B66	VREFCG

<sup>9</sup> This is the TYPEDEF# pin. The function is unused since the motherboard supports only 1.5V signaling and the connector is keyed appropriately.

<sup>10</sup> These pins are reserved for USB channel. This motherboard does not support a USB port via the AGP connector.

### C.3. AGP Expansion Slot (ADD card mode)

The AGP/ADD slot supports only 1.5V signaling.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	+12V	B1	<i>Not Used</i>	A34	VDDQ1.5	B34	VDDQ1.5
A2	<i>Not Used</i>	B2	+5V	A35	DVOCD3	B35	DVOCD2
A3	<i>Not Used</i>	B3	+5V	A36	DVOCD1	B36	DVOCD0
A4	<i>Not Used</i>	B4	<i>Not Used</i>	A37	GND	B37	GND
A5	GND	B5	GND	A38	DVOCBLANK#	B38	DVOCHSYNC
A6	<i>Not Used</i>	B6	<i>Not Used</i>	A39	DVOCVSYNC	B39	<i>Not Used</i>
A7	<i>Not Used</i>	B7	<i>Not Used</i>	A40	VDDQ1.5	B40	VDDQ1.5
A8	<i>Not Used</i>	B8	<i>Not Used</i>	A41	MDVIDATA	B41	MI2CCLK
A9	+3.3V	B9	+3.3V	A42	KEY	B42	KEY
A10	<i>Not Used</i>	B10	<i>Not Used</i>	A43	KEY	B43	KEY
A11	<i>Not Used</i>	B11	<i>Not Used</i>	A44	KEY	B44	KEY
A12	<i>Not Used</i>	B12	<i>Not Used</i>	A45	KEY	B45	KEY
A13	GND	B13	GND	A46	MDVICLK	B46	MI2CDATA
A14	<i>Not Used</i>	B14	<i>Not Used</i>	A47	MDDCDATA	B47	VDDQ1.5
A15	ADDID1	B15	ADDID0	A48	<i>Not Used</i>	B48	<i>Not Used</i>
A16	+3.3V	B16	+3.3V	A49	GND	B49	GND
A17	ADDID3	B17	ADDID2	A50	ADDDetect#	B50	<i>Not Used</i>
A18	<i>Not Used</i>	B18	<i>Not Used</i>	A51	MDDCCLK	B51	DVOBBLANK#
A19	GND	B19	GND	A52	VDDQ1.5	B52	VDDQ1.5
A20	ADDID5	B20	ADDID4	A53	DVOBCLKINT#	B53	DVOBFLDSTL
A21	ADDID7	B21	ADDID6	A54	DVOBD11	B54	DVOBD10
A22	<i>Not Used</i>	B22	<i>Not Used</i>	A55	GND	B55	GND
A23	GND	B23	GND	A56	DVOBD9	B56	DVOBD8
A24	<i>Not Used</i>	B24	+3.3VAUX	A57	DVOBD7	B57	DVOBD6
A25	+3.3V	B25	+3.3V	A58	VDDQ1.5	B58	VDDQ1.5
A26	DVOBCINTR#	B26	DVOCFLDSTL	A59	DVOBCLK#	B59	DVOBCLK
A27	DVOCD11	B27	DVOCD10	A60	DVOBD5	B60	DVOBD4
A28	+3.3V	B28	+3.3V	A61	GND	B61	GND
A29	DVOCD9	B29	DVOCD8	A62	DVOBD3	B62	DVOBD2
A30	DVOCD7	B30	DVOCD6	A63	DVOBD1	B63	DVOBD0
A31	GND	B31	GND	A64	VDDQ1.5	B64	VDDQ1.5
A32	DVOCCLK#	B32	DVOCCLK	A65	DVOBHSYNC	B65	DVOBVSYSYNC
A33	DVOCD5	B33	DVOCD4	A66	VREFGC	B66	VREFGC

### C.4. PCI Expansion Slot<sup>11</sup>

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	TRST# <sup>12</sup>	B1	-12V	A32	AD16	B32	AD17
A2	+12V	B2	TCK <sup>12</sup>	A33	+3.3V	B33	C/BE2#
A3	TMS <sup>13</sup>	B3	GND	A34	FRAME#	B34	GND
A4	TDI <sup>13</sup>	B4	TDO <sup>14</sup>	A35	GND	B35	IRDY#
A5	+5V	B5	+5V	A36	TRDY#	B36	+3.3V
A6	INTA#	B6	+5V	A37	GND	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	GND
A8	+5V	B8	INTD#	A39	+3.3V	B39	LOCK#
A9	CLKRUN# <sup>14</sup>	B9	PRSNT1#	A40	<i>Not Used</i>	B40	PERR#
A10	+5V	B10	<i>Reserved</i>	A41	<i>Not Used</i>	B41	+3.3V
A11	<i>Reserved</i>	B11	PRSNT2#	A42	GND	B42	SERR#
A12	GND	B12	GND	A43	PAR	B43	+3.3V
A13	GND	B13	GND	A44	AD15	B44	C/BE1#
A14	+3.3V AUX	B14	<i>Reserved</i>	A45	+3.3V	B45	AD14
A15	RST#	B15	GND	A46	AD13	B46	GND
A16	+5V	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	GND	A48	GND	B48	AD10
A18	GND	B18	REQ#	A49	AD9	B49	GND
A19	PME#	B19	+5V	A50	KEY	B50	KEY
A20	AD30	B20	AD31	A51	KEY	B51	KEY
A21	+3.3V	B21	AD29	A52	C/BE0#	B52	AD8
A22	AD28	B22	GND	A53	+3.3V	B53	AD7
A23	AD26	B23	AD27	A54	AD6	B54	+3.3V
A24	GND	B24	AD25	A55	AD4	B55	AD5
A25	AD24	B25	+3.3V	A56	GND	B56	AD3
A26	IDSEL	B26	C/BE3#	A57	AD2	B57	GND
A27	+3.3V	B27	AD23	A58	AD0	B58	AD1
A28	AD22	B28	GND	A59	+5V	B59	+5V
A29	AD20	B29	AD21	A60	REQ64#	B60	ACK64#
A30	GND	B30	AD19	A61	+5V	B61	+5V
A31	AD18	B31	+3.3V	A62	+5V	B62	+5V

<sup>11</sup> See following sections for ATX riser extension and slot 3 & 4 pin-out deviations

<sup>12</sup> Not used but pulled low

<sup>13</sup> Not used but pulled high to +5V

<sup>14</sup> Not connected

### C.5. PCI Slot 2 Riser Extension

Pin	Signal	Pin	Signal
A1	GNT4#	B1	GND
A2	GND	B2	CLK4
A3	GNT6#	B3	GND
A4	GND	B4	REQ4#
A5	CLK	B5	GND
A6	ID1	B6	CLK6
A7	<i>Reserved</i>	B7	GND
A8	ID2	B8	REQ6#
A9	NOGO	B9	GND
A10	+12V	B10	DREQ#
A11	SERIRQ	B11	DGNT#

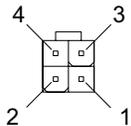
### C.6. PCI Slot 3 Riser Support

Pin	Signal	Pin	Signal
A1	LPCAD0	B2	LPCAD3
A3	LPCAD1	B4	IDSEL2
A4	LPCAD2	B9	CLK5
A11	GNT2#	B10	REQ2#
A40	REQ5#	B11	LPCFRAME#
A41	GNT5#	B14	CLK2
		B60	IDSEL5

### C.7. PCI Slot 4 Riser Support

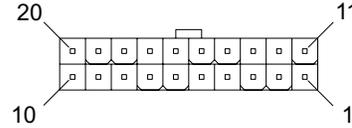
Pin	Signal	Pin	Signal
A4	CLK6	B4	IDSEL5
A11	GNT5#	B10	REQ5#
A40	REQ6#	B14	CLK5
A41	GNT6#	B60	IDSEL6

### C.8. ATX 12V Power Supply



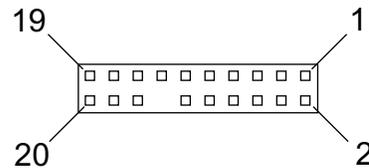
Pin	Signal	Pin	Signal
1	GND	3	+12.0V
2	GND	4	+12.0V

### C.9. ATX Power Supply



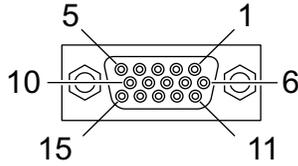
Pin	Signal	Pin	Signal
11	+3.3V	1	+3.3V
12	-12.0V	2	+3.3V
13	GND	3	GND
14	PS_ON#	4	+5.0V
15	GND	5	GND
16	GND	6	+5.0V
17	GND	7	GND
18	<i>Not Used</i>	8	PWR_OK
19	+5.0V	9	+5.0VSBY
20	+5.0V	10	+12.0V

### C.10. Front Panel Header



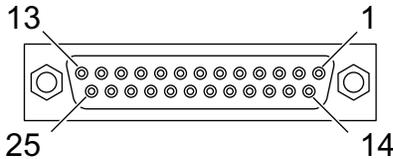
Pin	Signal	Pin	Signal
1	HDLED+	2	GREENLED+
3	HDLED-	4	GREENLED-
5	RESETSW-	6	PWRSW+
7	RESETSW+	8	PWRSW-
9	+5V fused	10	SPKR+
11	<i>Not Used</i>	12	SPKR-
13	GND	14	KEY
15	<i>Not Used</i>	16	SPKR-
17	<i>Not Used</i>	18	TMPSW+
19	<i>Not Used</i>	20	TMPSW-

### C.11. VGA Monitor



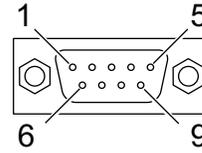
Pin	Signal	Pin	Signal
1	RED	9	+5V
2	GREEN	10	GND
3	BLUE	11	Reserved <sup>15</sup>
4	Reserved <sup>15</sup>	12	SDA
5	GND	13	HSYNC
6	RED RTN	14	VSYNC
7	GREEN RTN	15	SCL
8	BLUE RTN		

### C.12. Parallel Port



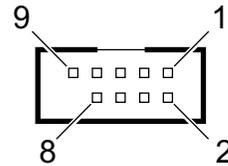
Pin	Signal	Pin	Signal
1	STB#	14	AFD#
2	DB0	15	ERR#
3	DB1	16	INIT#
4	DB2	17	SLIN#
5	DB3	18	GND
6	DB4	19	GND
7	DB5	20	GND
8	DB6	21	GND
9	DB7	22	GND
10	ACK#	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT		

### C.13. Serial Port 1



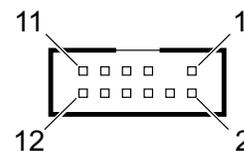
Pin	Signal	Pin	Signal
1	DCD	6	DSR
2	RxD	7	RTS
3	TxD	8	CTS
4	DTR	9	RING
5	GND		

### C.14. Serial Port 2



Pin	Signal	Pin	Signal
1	DCD	2	DSR
3	RxD	4	RTS
5	TxD	6	CTS
7	DTR	8	RING
9	GND	10	KEY

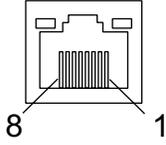
### C.15. Ethernet LED Header



Pin	Signal	Pin	Signal
1	330R Pullup	2	ACTIVITY2#
3	KEY	4	LINK2#
5	1000MB2#	6	100MB2#
7	330R Pullup	8	ACTIVITY1#
9	330R Pullup	10	LINK1#
11	1000MB1#	12	100MB1#

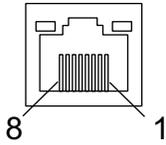
<sup>15</sup> Pulled high to +5V

### C.16. RJ45 Ethernet (10/100)



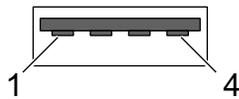
Pin	Signal
1	TxD+
2	TxD-
3	RxD+
4	75Ω AC termination
5	75Ω AC termination
6	RxD-
7	75Ω AC termination
8	75Ω AC termination

### C.17. RJ45 Ethernet (Gbit)



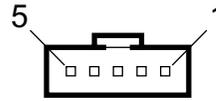
Pin	Signal
1	A+
2	A-
3	B+
4	C+
5	C-
6	B-
7	D+
8	D-

### C.18. USB I/O Panel Ports



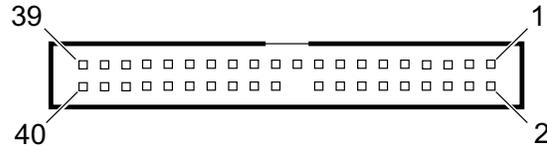
Pin	Signal
1	+5V
2	DATA-
3	DATA+
4	GND

### C.19. USB Internal Ports



Pin	Signal
1	+5V
2	DATA-
3	DATA+
4	GND
5	GND

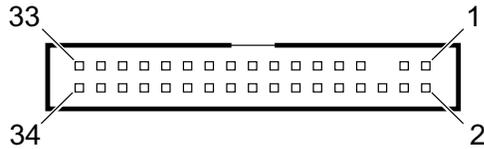
### C.20. IDE Drive Headers



Pin	Signal	Pin	Signal
1	RST#	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	KEY
21	DRQ	22	GND
23	IOW#	24	GND
25	IOR#	26	GND
27	IORDY	28	CSEL
29	DAK#	30	GND
31	IRQ <sup>16</sup>	32	Not Used
33	DA1	34	CBLID#
35	DA0	36	DA2
37	CS1#	38	CS3#
39	HDACT#	40	GND

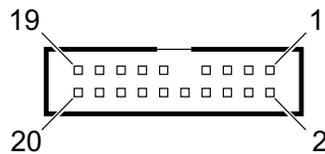
<sup>16</sup> IRQ14 for Primary, IRQ15 for Secondary

### C.21. Diskette Drive Header



Pin	Signal	Pin	Signal
1	GND	2	DENSEL
3	GND	4	<i>Not Used</i>
5	KEY	6	DRATE0
7	GND	8	INDEX#
9	GND	10	MTR0#
11	GND	12	<i>Not Used</i>
13	GND	14	DS0#
15	GND	16	<i>Not Used</i>
17	GND	18	DIR#
19	GND	20	STEP#
21	GND	22	WDATA#
23	GND	24	WGATE#
25	GND	26	TRK0#
27	GND	28	WP#
29	GND	30	RDATA#
31	GND	32	HDSEL#
33	GND	34	DSKCHG#

### C.22. GPIO Header



Pin	Signal	Pin	Signal
1	GND	2	+5V fused
3	PWM	4	GPIO20
5	GPIO21	6	GPO22
7	GPIO10	8	GPIO11
9	GPIO12	10	GPIO13
11	GPIO14	12	GPIO15
13	GPIO16	14	GPIO17
15	<i>Reserved</i>	16	KEY
17	GND	18	GPI23
19	GND	20	GPI24

### C.23. 30-pin LVDS PanelData (Single channel 24-bit option)



Pin	Signal	Pin	Signal
1	GND	16	SHIELD
2	+3.3V	17	CLKAM
3	+3.3V	18	CLKAP
4	+3.3V	19	SHIELD
5	<i>Not Used</i>	20	A3M
6	DDCCLK	21	A3P
7	DDCDATA	22	SHIELD
8	A0M	23	<i>Reserved</i>
9	A0P	24	<i>Reserved</i>
10	SHIELD	25	SHIELD
11	A1M	26	<i>Reserved</i>
12	A1P	27	<i>Reserved</i>
13	SHIELD	28	SHIELD
14	A2M	29	<i>Reserved</i>
15	A2P	30	<i>Reserved</i>

### C.24. 30-pin LVDS Panel Data (Dual channel 18-bit option)



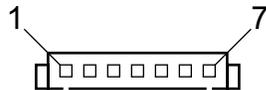
Pin	Signal	Pin	Signal
1	GND	16	SHIELD
2	+3.3V	17	CLKAM
3	+3.3V	18	CLKAP
4	+3.3V	19	SHIELD
5	<i>Not Used</i>	20	B0M
6	DDCCLK	21	B0P
7	DDCDATA	22	SHIELD
8	A0M	23	B1M
9	A0P	24	B1P
10	SHIELD	25	SHIELD
11	A1M	26	B2M
12	A1P	27	B2P
13	SHIELD	28	SHIELD
14	A2M	29	CLKBM
15	A2P	30	CLKBP

### C.25. 20-pin LVDS VDL/VCL



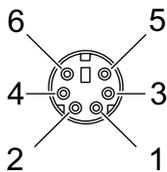
Pin	Signal	Pin	Signal
1	+3.3V	11	A2M
2	+3.3V	12	A2P
3	GND	13	SHIELD
4	GND	14	CLKAM
5	A0M	15	CLKAP
6	A0P	16	GND
7	SHIELD	17	+3.3V
8	A1M	18	Not Used
9	A1P	19	DDCCLK
10	SHIELD	20	DDCDATA

### C.26. LVDS Backlight Control



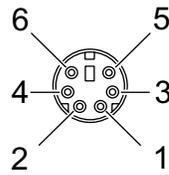
Pin	Signal
1	Inverter Power, +12V
2	GND
3	GND
4	+5V
5	CLK
6	DATA/PWM Control
7	ENABLE

### C.27. PS/2 Keyboard



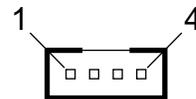
Pin	Signal	Pin	Signal
1	KDATA	4	+5V
2	MDATA	5	KCLOCK
3	GND	6	MCLOCK

### C.28. PS/2 Mouse



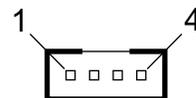
Pin	Signal	Pin	Signal
1	DATA	4	+5V
2	Not Used	5	CLOCK
3	GND	6	Not Used

### C.29. Keyboard Header



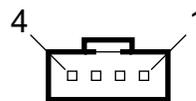
Pin	Signal
1	+5V
2	DATA
3	GND
4	CLOCK

### C.30. Mouse Header



Pin	Signal
1	+5V
2	DATA
3	GND
4	CLOCK

### C.31. Internal Audio Headers



Pin	Signal
1	LEFT
2	GND
3	GND
4	RIGHT

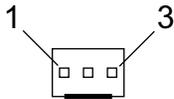
### C.32. Line In and Out Jacks

Pin	Signal
TIP	LEFT
RING	RIGHT
SLEEVE	GND

### C.33. MIC Jack

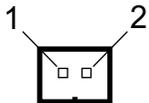
Pin	Signal
TIP	MIC MONO INPUT
RING	BIAS VOLTAGE
SLEEVE	GND

### C.34. Processor and System Fan 1 & 2



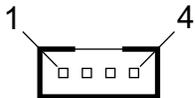
Pin	Signal
1	GND
2	POWER
3	TACH#

### C.35. Remote Thermal Sensor



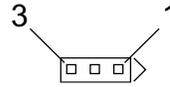
Pin	Signal
1	DIODE+
2	DIODE-

### C.36. SMBus Header



Pin	Signal
1	+3.3V
2	DATA
3	CLOCK
4	GND

### C.37. Alternate Power LED



Pin	Signal
1	GREENLED+
2	KEY
3	GREENLED-