Kaimei Kaimei_KM-V5-V2

Rev. 1.0

JBAT1	
1-2	Retain CMOS data (default)
2-3	Clear CMOS data

JROM1	
1-2	5V Flash ROM
2-3	12V Flash ROM

Clock	JCK1	JCK2	JCK3
50 MHz	2-3	2-3	2-3
55 MHz	2-3	2-3	1-2
60 MHz	1-2	2-3	2-3
66 MHz	2-3	1-2	2-3
75 MHz	1-2	2-3	1-2

CPU	J2
Single supply: Vcore = V_IO and selected by JPW1	1-2, 4-5
Dual supply: V_iO = 3.3V, Vcore selected with the next table	2-3, 5-6

Vcore	No label
3.5V	1-2
3.3V	3-4
3.0V	5-6
2.9V	7-8
2.8V	9-10
2.5V	11-12
2.1V	13-14

Multiplier	JBF1	JBF2	JBF3
1.5	open	open	open
2	**close**	open	open
2.5	**close**	**close**	open
3	open	**close**	open
3.5	open	open	open
4	**close**	open	**close**
4.5	**close**	**close**	**close**

USB 1.0 connectors CN3 and CN4:

Pin	USB-Signal
1	+5V
2	Data(-)
3	Data(+)
4	Ground

CN3 and CN4 are placed opposed. You need a special USB bracket for it.

Other jumpers:	
J1	Fixed to 2-3 with 256kB cache
JV3	Fixed to 1-2
JCK4	Not placed, normaly used for asynchronous PCI bus clock
J3	Ring indicator to wake up the system with a phone call (goes with a pull-up and a series resistor to pin 93 of the VT82C568B)

Additional hints:

128MB single side and 256MB double side are the highest memory capacity which I tested successfully.