CHASSIS PLANS®

Systems Engineered to Perform®

JXT6966 / JXTS6966

S6966-xxx

Revision A

BIOS SETUP

TECHNICAL REFERENCE

Aptio® 4.x Test Setup Environment (TSE)

For use with JXT6966 or JXTS6966

Intel® Xeon® C5500-series

Quad-Core

PROCESSOR-BASED

SHB

PICMG®

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SHB HANDLING PRECAUTIONS

WARNING: This product has components which may be damaged by electrostatic discharge.

To protect your system host board (SHB) from electrostatic damage, be sure to observe the following precautions when handling or storing the board:

- Keep the SHB in its static-shielded bag until you are ready to perform your installation.
- Handle the SHB by its edges.
- Do not touch the I/O connector pins.
- Do not apply pressure or attach labels to the SHB.
- Use a grounded wrist strap at your workstation or ground yourself frequently by touching the metal chassis of the system before handling any components. The system must be plugged into an outlet that is connected to an earth ground.
- Use antistatic padding on all work surfaces.
- Avoid static-inducing carpeted areas.

RECOMMENDED BOARD HANDLING PRECAUTIONS

This SHB has components on both sides of the PCB. Some of these components are extremely small and subject to damage if the board is not handled properly. It is important for you to observe the following precautions when handling or storing the board to prevent components from being damaged or broken off:

- Handle the board only by its edges.
- Store the board in padded shipping material or in an anti-static board rack.
- Do not place an unprotected board on a flat surface.

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Chapter 1 Starting Aptio® TSE

Introduction
The JXT6966 and JXTS6966 feature the Aptio® 4.x BIOS from American Megatrends, Inc. (AMI) with a ROM-resident setup utility called the Aptio® Text Setup Environment or TSE. The TSE allows you to select to the following categories of options:

- Main Menu
- Advanced Setup
- Boot Setup
- Security Setup
- Chipset Setup
- Exit

Each of these options allows you to review and/or change various setup features of your system. Details are provided in the following chapters of this manual. Additional copies of the Chassis Plans JXT6966 / JXTS6966 BIOS and hardware technical reference manuals are available under the **Downloads** tab on the JXT6966 or JXTS6966 web pages.

Aptio Text Setup Environment (TSE) is a text-based basic input and output system. The purpose of Aptio TSE is to empower the user with complete system control at boot. This document explains the basic navigation of Aptio TSE.

NOTE: The contents of this document were provided as a courtesy from American Megatrends, Inc or AMI and describe the standard look and feel of the Aptio TSE interface. Chassis Plans is the manufacturer of the SHB hardware and during production may have made subtle changes to some of the settings described in this document. Therefore, some of the options that are described in this document may not exist or may have been modified for use in the JXT6966 / JXTS6966 implementation of the Aptio TSE BIOS utility. Contact Chassis Plans Technical support for any questions regarding the SHBs' implementation of Aptio TSE.

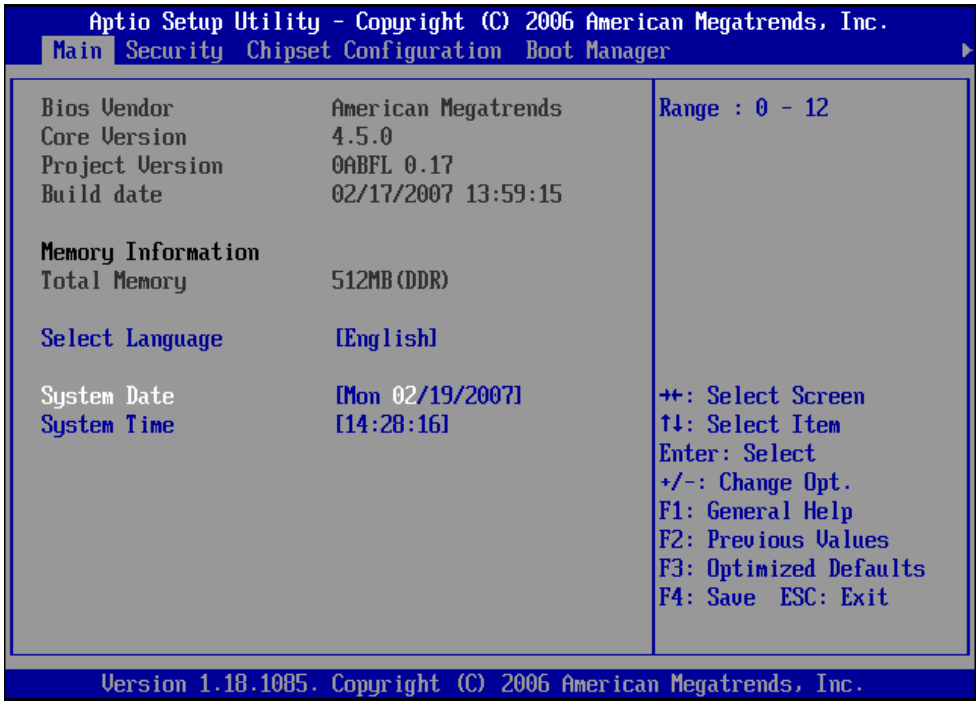
Starting Aptio TSE
To enter the Aptio TSE screens, follow the steps below:

Step	Description
1	Install the SHB in a PICMG 1.3 backplane with the proper system power connections made to the backplane and a mouse, keyboard and monitor connected to the SHB
2	Power on the system with the SHB
3	Press the <Delete> or <F2> key on your keyboard when you see the following text prompt: **Press DEL or F2 to enter Setup**
4	After you press the <Delete>/<F2> key, the Aptio TSE main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as the Chipset and Power menus.

NOTE: In most cases, the <Delete> or <F2> keys are used to invoke the Aptio TSE screen. There are a few cases that other keys are used (<F1>, <F10>, …).

NOTE: The user can press the <TAB> key during boot to switch from the boot splash screen (logo) to see the keystroke messages.

Aptio® TSE Setup Menu
The Aptio TSE BIOS setup menu is the first screen that you can navigate. Each BIOS setup menu option is described in this user's guide.



There may be slight differences in the screen shots illustrated in this manual due to Chassis Plans JXT6966 BIOS modifications. Contact Chassis Plans Technical support for any questions regarding the SHBs' implementation of Aptio TSE.

Navigation
The Aptio® TSE keyboard-based navigation can be accomplished using a combination of the keys.(<FUNCTION> keys, <ENTER>, <ESC>, <ARROW> keys, etc.).

Key	Description
ENTER	The *Enter* key allows the user to select an option to edit its value or access a sub menu.
→← Left/Right	The *Left and Right* <Arrow> keys allow you to select an Aptio TSE screen. For example: Main screen, Advanced screen, Chipset screen, and so on.
↑↓ Up/Down	The *Up and Down* <Arrow> keys allow you to select an Aptio TSE item or sub-screen.
+- Plus/Minus	The *Plus and Minus* <Arrow> keys allow you to change the field value of a particular setup item. For example: Date and Time.
Tab	The <Tab> key allows you to select Aptio TSE fields.
ESC	The <Esc> key allows you to discard any changes you have made and exit the Aptio TSE. Press the <Esc> key to exit the Aptio TSE without saving your changes. The following screen will appear: Press the <Enter> key to discard changes and exit. You can also use the <Arrow> key to select *Cancel* and then press the <Enter> key to abort this function and return to the previous screen.
Function keys	When other function keys become available, they are displayed in the help screen along with their intended function.

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Chapter 2 Advanced Setup

Introduction
Select the *Advanced* menu item from the Aptio TSE screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as System Launch Settings, PCI Sub-System Configuration, ACPI Settings, CPU Configuration, SATA/IDE Configuration, USB Configuration, Info Report Configuration and a SuperIO configuration if the SHB is equipped with an optional IOB33. Selecting on of these set-up items will take you to a configuration sub menu for that item.

Launch PXE OpROM Configuration
With this selection, you can enable or disable the system's Boot From LAN capability of the SHB which allows system ROM storage settings for legacy networks.

Launch Storage OpROM Configuration
With this selection, you can enable or disable the system's ROM storage settings for legacy mass storage devices.

PCI Sub-System Settings
Various device settings are available for configuration with this BIOS parameter. Specific device availability depends on what the BIOS can see during the system boot process.

ACPI Settings
This is where you set up your system for use with the ACPI soft control states available on the SHB. Various system sleep states and recover modes are available for selection on this sub-menu..

CPU Configuration
The parameters for the specific Jasper Forest processors installed on your SHB are displayed on the top portion of this sub-menu. The lower portion of this screen contains processor features that you may elect to enable or disable on the unique requirements of your system. Here is a partial listing of some of these CPU parameters.

Option	Description
Intel® Hyper-Threading	This option allows the user to enable or disable Intel® Hyper-Threading support on the Intel® Xeon® C5000 series (i.e. Jasper Forest) processor. By default, this setting is enabled.
Intel® Virtualization	This option allows the user to enable or disable Intel® Virtualization support on the Intel® Xeon® C5000 series (i.e. Jasper Forest) processor. By default, this setting is enabled.
Execute Disable Bit	This option allows the user to enable or disable Intel® Execute Disable Bit feature of the Intel® Xeon® C5000 series (i.e. Jasper Forest) processor.
Active Processor Cores	With this setting you may us all of the available cores available in the Intel® Xeon® C5000 series (i.e. Jasper Forest) processor or on use a subset of the available CPU execution cores. The default setting for this option is "ALL" and the number of cores to select depends on the specific processor installed on the SHB.

SATA Configuration
This is where you can set the parameters for the SATA devices that have been sensed SHBs' during the boot process.

USB Configuration
This is where you can set the parameters for the USB devices that have been sensed SHBs' during the boot process.

Info Report Configuration
This is where you can set the parameters have the SHB enable selected system BIOS reports.

IDE Configuration
Some of the following IDE configuration parameters will only be available if your Chassis Plans JXT6966 or JXTS6966 has the optional IOB33 installed on the board. Several of these parameters appear as sub-options to the SATA Configuration sub-menu. You can use this screen to select options for the IDE Configuration Settings.

Automatic Mode
This setting allows you to manually configure each controller. Ensure that your operating system allows support for more than two controllers.

Option	Description
Enable	Set this value to allow automatic configuration of the IDE controller(s). This is the default value.
Disable	Set this value to allow manual configuration of the IDE controller(s).

IDE Mode

Option	Description
Legacy	A controller that operates in legacy mode emulates a legacy IDE controller that is a non-standard extension of the ISA-based IDE controller. In legacy mode, the controller requires two ISA-style dedicated IRQs (14 and 15) that cannot be shared with other devices. Because legacy mode requires dedicated resources, the ATA controller for the boot device (which is usually integrated in chipsets on the motherboard) is the only controller on a system that is likely to operate in legacy mode.
Native	A controller that operates in native mode acts as a true PCI device that does not require dedicated legacy resources and can be configured anywhere in the system. ATA controllers running in native mode use their PCI interrupt for both channels and can share this interrupt with other devices in the system, like any other PCI device. Add-in ATA controllers generally operate in native mode.

Serial ATA
The following menu options allow you to turn off or on the onboard SATA ports.

Option	Description
Disabled	Set this value to prevent the computer system from using the onboard SATA controller.
Enabled	Set this value to allow the computer system to detect the onboard SATA controller. This is the default setting.

Serial ATA Port *X*
This item specifies the SATA ports used by the onboard SATA controller.

Option	Description
Disabled	Set this value to prevent the computer system from using the onboard SATA port selected.
Enabled	Set this value to allow the computer system to detect the onboard SATA port selected. This is the default setting.

IDE Configuration (continued)

Onboard Primary/Secondary IDE Controller
This item specifies the IDE channels used by the onboard PCI IDE controller.

Option	Description
Disabled	Set this value to prevent the computer system from using the onboard IDE controller selected.
Enabled	Set this value to allow the computer system to detect the onboard IDE controller selected. This is the default setting.

Super IO Configuration
The only Super IO component available in a system implementation using the JXT6966 or JXTS6966 is located on the optional IOB33 module. An IOB33 can plug into the SHBs' P20 I/O Expansion connector. If an IOB33 is plugged into the SHB then the Super IO Configuration submenu will be displayed. This Advanced Setup sub-menu allows you to configure the system ports connected to the IOB33s' Super I/O component.

NOTE: The following Super IO settings are only valid when an optional Chassis Plans IOB33 I/O Board is installed on the JXT6966 or JXTS6966 SHB.

Floppy Controller
This option allows you to enable or disable the floppy drive controller on your platform.

Option	Description
Disabled	Set this value to prevent the BIOS from detecting the onboard floppy drive controller.
Enabled	Set this value to allow the BIOS to use the onboard floppy drive controller. This is the default setting.

Floppy Write Protect
This option allows you to enable or disable write-protection of floppy disks.

Option	Description
Disabled	Set this value to prevent writing to floppy disks.
Enabled	Set this value to allow writing to floppy disks. This is the default setting.

Floppy Drive A: and B:

Option	Description
Disabled	Set this value to prevent the use of the selected floppy disk drive channel. This option should be set if no floppy disk drive is installed on the specified channel. This is the default setting for *Floppy Drive B*.
360 KB 5 ¼"	Set this value if the floppy disk drive attached to the corresponding channel is a 360 KB 5¼" floppy disk drive.
1.2 MB 5 ¼"	Set this value if the floppy disk drive attached to the corresponding channel is a 1.2 MB 5¼" floppy disk drive.
720 KB 3 ½"	Set this value if the floppy disk drive attached to the corresponding channel is a 720 KB 3½" floppy disk drive.
1.44 MB 3 ½"	Set this value if the floppy disk drive attached to the corresponding channel is a 1.44 MB 3½" floppy disk drive. This is the default setting for *Floppy Drive A*.

Super IO Configuration (continued)

Floppy Drive Seek
Set this option to seek the floppy disk drive during boot up. The Optimal and Fail-Safe setting is *Disabled*.

Option	Description
Disabled	Set this value to prevent the BIOS from seeking the floppy disk drive during boot up. This is the default setting.
Enabled	Set this value to allow the BIOS to seek the floppy disk drive during boot up. This will cause the floppy disk drive to temporarily power on during POST.

PS2 Port Swap

Option	Description
Disabled	Set this value to use the default PS/2 port settings. This is the default setting.
Enabled	Set this value to invert the PS/2 port settings so that the mouse port is switched from the top to the bottom while the keyboard port is switched from the bottom to the top.

Serial Port1 Address
This option specifies the base I/O port address and Interrupt Request address of serial port 1. The Optimal setting is *3F8/IRQ4*. The Fail-Safe default setting is *Disabled.*

Option	Description
Disabled	Set this value to prevent the serial port from accessing any system resources. When this option is set to *Disabled*, the serial port physically becomes unavailable.
3F8/IRQ4	Set this value to allow the serial port to use 3F8 as its I/O port address and IRQ 4 for the interrupt address. This is the default setting. The majority of serial port 1 or COM1 ports on computer systems use IRQ4 and I/O Port 3F8 as the standard setting. The most common serial device connected to this port is a mouse. If the system will not use a serial device, it is best to set this port to *Disabled*.
2F8/IRQ3	Set this value to allow the serial port to use 2F8 as its I/O port address and IRQ 3 for the interrupt address. If the system will not use a serial device, it is best to set this port to *Disabled*.
3E8/IRQ4	Set this value to allow the serial port to use 3E8 as its I/O port address and IRQ 4 for the interrupt address. If the system will not use a serial device, it is best to set this port to *Disabled*.
2E8/IRQ3	Set this value to allow the serial port to use 2E8 as its I/O port address and IRQ 3 for the interrupt address. If the system will not use a serial device, it is best to set this port to *Disabled*.

Super IO Configuration (continued)

Serial Port2 Address
This option specifies the base I/O port address and Interrupt Request address of serial port 2. The Optimal setting is *2F8/IRQ3*. The Fail-Safe setting is *Disabled.*

Option	Description
Disabled	Set this value to prevent the serial port from accessing any system resources. When this option is set to *Disabled*, the serial port physically becomes unavailable.
3F8/IRQ4	Set this value to allow the serial port to use 3F8 as its I/O port address and IRQ 4 for the interrupt address. If the system will not use a serial device, it is best to set this port to Disabled.
2F8/IRQ3	Set this value to allow the serial port to use 2F8 as its I/O port address and IRQ 3 for the interrupt address. This is the default setting. The majority of serial port 2 or COM2 ports on computer systems use IRQ3 and I/O Port 2F8 as the standard setting. The most common serial device connected to this port is an external modem. If the system will not use an external modem, set this port to *Disabled*. **Note:** Most internal modems require the use of the second COM port and use 3F8 as its I/O port address and IRQ 4 for its interrupt address. This requires that the Serial Port2 Address be set to *Disabled* or another base I/O port address and Interrupt Request address.
3E8/IRQ4	Set this value to allow the serial port to use 3E8 as its I/O port address and IRQ 4 for the interrupt address. If the system will not use a serial device, it is best to set this port to Disabled.
2E8/IRQ3	Set this value to allow the serial port to use 2E8 as its I/O port address and IRQ 3 for the interrupt address. If the system will not use a serial device, it is best to set this port to *Disabled*.

Onboard CIR Port
This option specifies the base I/O port address of the onboard CIR port. The Optimal setting is 3E0. The Fail-Safe setting is *Disabled*

Option	Description
Disabled	Set this value to prevent the Onboard CIR Port from accessing any system resources. When the value of this option is set to *Disabled*, the infrared port becomes unavailable.
3E0	Set this value to allow the Onboard CIR Port to use 3E0 as its I/O port address.
2E0	Set this value to allow the Onboard CIR Port to use 2E0 as its I/O port address.

Parallel Port Address
This option specifies the I/O address used by the parallel port. The Optimal setting is *378*. The Fail-Safe setting is *Disabled*.

Option	Description
Disabled	Set this value to prevent the parallel port from accessing any system resources. When the value of this option is set to *Disabled*, the printer port becomes unavailable.
378	Set this value to allow the parallel port to use 378 as its I/O port address. This is the default setting. The majority of parallel ports on computer systems use IRQ7 and I/O Port 378H as the standard setting.
278	Set this value to allow the parallel port to use 278 as its I/O port address.
3BC	Set this value to allow the parallel port to use 3BC as its I/O port address.

Super IO Configuration (continued)

Parallel Port Mode
This option specifies the parallel port mode. The Optimal setting is *Normal*. The Fail-Safe setting is *Disabled*.

Option	Description
Normal	Set this value to allow the standard parallel port mode to be used. This is the default setting.
Bi-Directional	Set this value to allow data to be sent to and received from the parallel port.
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bi-directional data transfer driven by the host device.
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits per second. ECP provides symmetric bi-directional communication.

Parallel Port IRQ
This option specifies the IRQ used by the parallel port. The Optimal and Fail-Safe default setting is *7*.

Option	Description
5	Set this value to allow the serial port to use Interrupt 3.
7	Set this value to allow the serial port to use Interrupt 7. This is the default setting. The majority of parallel ports on computer systems use IRQ7 and I/O Port 378H as the standard setting.

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Chapter 3 Chipset Configuration Setup

Introduction

The term "chipset" is a bit of a misnomer for the Chassis Plans JXT6966 and JXTS6966. The "chipset" on these SHBs is really a single component called a "Platform Controller Hub" or PCH. Specifically, the Chassis Plans JXT6966 and JXTS6966 both feature the Intel® 3420. This new PCH device combines many of the capabilities that were previously contained in individual North Bridge and South Bridge chipset components. The following section covers the set-up parameters of what could thought of as the North Bridge and South Bridge sections of the Intel® 3420 Platform Controller Hub.

North Bridge Configuration

The *North Bridge Configuration* menu item allows the user to do the following:

Option	Description
Jasper Forest I/O Configuration	This option allows the user to view, enable or disable the Intel® Virtualization Technology for Directed I/O feature of the processors. The default setting is Disabled and when Enabled a sub-menu of specific I/O parameters are available for selection.
QPI Link	This option allows the user to view, select or set to auto the frequency of the Intel® Quick Path Interconnect or Intel QPI. The default setting is Auto which allows the system to pick the optimum QPI frequency based on the processor type installed on the SHB. Other link settings are available for the user, but Chassis Plans recommends using the QPI Link defaults.
DIMM Presence & Size Info	This option displays the total memory installed on the SHB as well as the memory size installed in each DDR3 Mini-DIMM socket on the board

South Bridge Configuration

The *South Bridge Configuration* menu item allows the user to do the following:

Option	Description
SMBus Controller	This option allows the user to enable or disable the SMBus Controller in the Intel® 3420
GbE Controller	This option allows the user to enable or disable the Ethernet Controller in the Intel® 3420. Disabling this internal controller shuts down the LAN interface to the PICMG 1.3 backplane. This setting does not affect the operation of the independent Intel 82575 Ethernet Controller that drives the two LAN ports on the SHBs I/O plate.
Wake on LAN from S5	This option allows the user to enable or disable wake on LAN feature derived from an ACPI S5 shutdown event
Restore AC Power Loss Settings	This option allows the user to determine how the system will come back up when power is restored after an unplanned power interruption. The options are Power Off, Power On or Last State.
PCI Express Ports Configuration	This option allows the user to Enable, Disable or Automatically turn on the various PCI Express ports inside the Intel® 3420 PCH. The default setting is set to Auto and Chassis Plans highly recommends leaving this setting alone. These internal PCIe ports drive on-board components and turning them off will disable critical SHB and system functions
USB Configuration	This option allows the user to Enable or Disable the various USB ports inside the Intel® 3420 PCH. The default setting is set to Enable. These internal USB ports drive the USB interface connections to the SHBs I/O plate and down to edge connector C for us on a PICMG 1.3 backplane.

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Chapter 4 Boot Setup

Introduction
Select the *Boot Setup* menu item from the Aptio TSE screen to enter the BIOS Setup screen. The Boot menu option allows you to access the following the following boot setup features.

Quite Boot
Set this value to allow the boot up screen options to be modified between POST messages or OEM logo.

Option	Description
Disabled	Set this default value allows the computer system to display the POST messages.
Enabled	Set this value to allow the computer system to display the OEM logo.

Fast Boot

Option	Description
Disabled	Set this to allow the computer system to a full boot with a full set of devices. In full configuration mode, all devices are detected and initialized. This is the default setting.
Enabled	Set this value to allow the computer system to do a minimal boot. In minimal configuration mode, only the devices that are necessary to boot the system are detected and initialized..

Bootup NumLock State

Option	Description
On	Set this value to allow the Number Lock on the keyboard to be enabled automatically when the computer system is boot up. This allows the immediate use of 10-keys numeric keypad located on the right side of the keyboard. This is the default setting.
Off	This option does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad.

The next four BIOS settings on this screen are:

- Gate20 Active
- Option ROM Messages
- Interrupt 19 Capture
- Non-EDID Monitor Support

These are special purpose BIOS settings and should remain in the default positions. Contact Chassis Plans technical support team if you need to use these BIOS settings.

82575EB LAN1

Option	Description
Enabled	Set this value to enable Ethernet LAN1 on the SHB. This is the default setting.
Disabled	Set this value to disable Ethernet LAN1 on the SHB.

82575EB LAN2

Option	Description
Enabled	Set this value to enable Ethernet LAN2 on the SHB. This is the default setting.
Disabled	Set this value to disable Ethernet LAN2 on the SHB.

Boot Option Priorities

The following settings allow you to set the system boot priority of where to pull the BIOS settings from in order to perform a system boot. You can set three priority levels and the number of available options within each priority is based on the devices connected to the SHB. Here is an example of potential boot options.

Boot Option #1	Boot Option #2	Boot Option #3
SATA Hard Drive [HD type info]	Built-In EFI Shell	USB Flash Hub [USB type info]
Built-In EFI Shell	SATA Hard Drive [HD type info]	SATA Hard Drive [HD type info]
USB Flash Hub [USB type info]	USB Flash Hub [USB type info]	Built-In EFI Shell
Disabled	Disabled	Disabled

Any other devices connected to SHB and the system would show up under each option in the above listing similar to the SATA and USB devices in the example above.

Hard Drive BBS Priorities

BBS means BIOS Boot Specification and this BIOS setting is nearly identical to the Boot Option Priorities. The only difference is that the built-in EFI shell is not a boot option. The options are the devices connected to the system and the disabled option as listed in the example below.

Boot Option #1	Boot Option #2
SATA Hard Drive [HD type info]	USB Flash Hub [USB type info]
USB Flash Hub [USB type info]	SATA Hard Drive [HD type info]
Disabled	Disabled

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Chapter 5 Security

Two Levels of Password Protection
Security Setup provides both a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first.

The system can be configured so that all users must enter a password every time the system boots or when Setup is executed, using either or either the Supervisor password or User password.

The Supervisor and User passwords activate two different levels of password security. If you select password support, you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed. Make sure you write it down. If you forget it, you must drain NVRAM and reconfigure.

Remember the Password
Keep a record of the new password when the password is changed. If you forget the password, you must erase the system configuration information in NVRAM. See (Deleting a Password) for information about erasing system configuration information.

Security Setup
The *Security* setup menu item allows the user to do the following:

Option	Description
User Password	This option allows the user to set a user level password for the BIOS.
Admin Password	This option allows the user to set an administrative level password for the BIOS.

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Chapter 6 Saving and Exiting BIOS Setup and Restoring Defaults

Introduction
There are four methods of saving BIOS changes and leaving Aptio TSE listed at the top of this screen:

1 - **Save Changes & Exit**
When you have completed the system configuration changes, select this option to save your BIOS changes and leave Aptio TSE. You will need to reboot the computer for the new system configuration parameters to take effect.

Select Save Changes & Exit from the Exit menu and press <Enter>.

Save Configuration Changes and Exit Now?

[YES] [NO] appears in the window. Select *YES* to save changes and exit.

2 - **Discard Changes & Exit**
Select this option to quit Aptio TSE without making any permanent changes to the system configuration.

Select Discard Changes & Exit from the Exit menu and press <Enter>.

Discard Changes and Exit Setup Now?

[YES] [NO] Select *YES* to discard changes and exit.

3 - **Save Changes & Reset**
When you have completed the system configuration changes, select this option to save the BIOS changes, leave Aptio TSE and reset the computer so the new system configuration parameters can take effect.

Select Save Changes & Reset from the Exit menu and press <Enter>.

Save Configuration Changes and Exit Now?

[YES] [NO] appears in the window. Select *YES* to save changes and reset.

4 - **Discard Changes & Reset**
Choose this option if you decide to discard your BIOS changes, but what to reset the system upon leaving Aptio TSE.

Select Discard Changes & Reset from the Exit menu and press <Enter>.

Discard Configuration Changes and Exit Now?

[YES] [NO] appears in the window. Select *YES* to discard changes and reset.

The following two screen options allow save or discard BIOS changes without leaving Aptio TSE:

Save Changes	[YES] [NO]
Discard Changes	[YES] [NO]

The following menu options for BIOS defaults are available:

Restore Defaults
Aptio TSE automatically sets all Aptio TSE options to a complete set of factory default settings when you select this option.

Select restore defaults from the Exit menu and press <Enter>.

Restore Defaults?

[YES] [NO] appears in the window. Select *YES* to load restore defaults.

Save as User Defaults
With this option the BIOS changes done so far by the user are saved as User Defaults.

Select save as user defaults from the Exit menu and press <Enter>.

Save as User Defaults?

[YES] [NO] appears in the window. Select *YES* to save user defaults.

Restore User Defaults
Aptio TSE automatically sets all Aptio TSE options to a complete set of user default settings when you select this option.

Select restore user defaults from the Exit menu and press <Enter>.

Restore User Defaults?

[YES] [NO] appears in the window. Select *YES* to load restore user defaults.

Boot Overide
Select this option to allow a system boot override from either a specific device connected to the SHB or from the BIOS' EFI Shell.

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Chapter 7 SMBIOS Event Log

Change SMBIOS Event Log Settings
Use the Aptio TSE menu screen options to set up the system event log reporting format and configuration options for the BIOS.

View SMBIOS Event Log
This read-only menu screen displays the events recorded in the BIOS event log. An event's error code and severity along with the data an time that the event occurred are displayed on this screen.

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Appendix A BIOS Messages

Introduction
A status code is a data value used to indicate progress during the boot phase. These codes are outputted to I/O port 80h on the SHB. Aptio 4.x core outputs checkpoints throughout the boot process to indicate the task the system is currently executing. Status codes are very useful in aiding software developers or technicians in debugging problems that occur during the pre-boot process.

Aptio Boot Flow
While performing the functions of the traditional BIOS, Aptio 4.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI ("the Framework"). The Framework refers the following "boot phases", which may apply to various status code descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization[1]
- Driver Execution Environment (DXE) – main hardware initialization[2]
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, …)

[1] Analogous to "bootblock" functionality of legacy BIOS
[2] Analogous to "POST" functionality in legacy BIOS

BIOS Beep Codes
The Pre-EFI Initialization (PEI) and Driver Execution Environment (DXE) phases of the Aptio BIOS use audible beeps to indicate error codes. The number of beeps indicates specific error conditions.

PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
7	Reset PPI is not available
4	Recovery failed
4	S3 Resume failed

DXE Beep Codes

# of Beeps	Description
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
1	Invalid password
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

BIOS Status Codes

As the POST (Power On Self Test) routines are performed during boot-up, test codes are displayed on Port 80 POST code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LED are located on the top of the SHB, just above the board's battery socket. The POST Code LEDs and are numbered from right (position 1 = LED0) to left (position 8 – LED7).

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following chart is a key to interpreting the POST codes displayed on LEDs 0 through 7 on the JXT6966 and JXTS6966 SHBs. Refer to the board layout in the *Specifications* chapter for the exact location of the POST code LEDs.

The HEX to LED chart in the POST Code LEDs section will serve as a guide to interpreting specific BIOS status codes.

BIOS Status POST Code LEDs

As the POST (Power On Self Test) routines are performed during boot-up, test codes are displayed on Port 80 POST code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LED are located on the top of the SHB, just above the board's battery socket. The POST Code LEDs and are numbered from right (position 1 = LED0) to left (position 8 – LED7).

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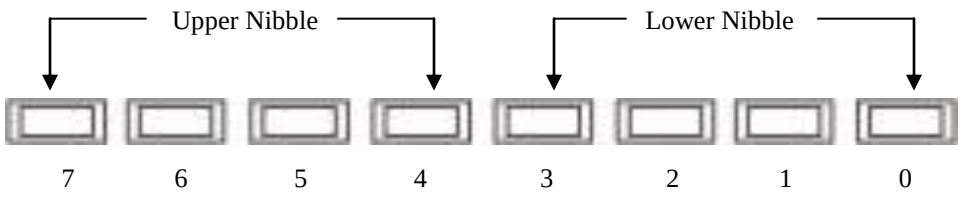
Upper Nibble (UN)				
Hex. Value	LED7	LED6	LED5	LED4
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On

Lower Nibble (LN)				
Hex. Value	LED3	LED2	LED1	LED0
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On



JXT6966 & JXTS6966 POST Code LEDs

Status Code Ranges

Status Code Range	Description
0x01 – 0x0F	SEC Status Codes & Errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0xCF	DXE execution up to BDS
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

SEC Status Codes

Status Code	Description
0x0	Not used
Progress Codes	
0x1	Power on. Reset type detection (soft/hard).
0x2	AP initialization before microcode loading
0x3	North Bridge initialization before microcode loading
0x4	South Bridge initialization before microcode loading
0x5	OEM initialization before microcode loading
0x6	Microcode loading
0x7	AP initialization after microcode loading
0x8	North Bridge initialization after microcode loading
0x9	South Bridge initialization after microcode loading
0xA	OEM initialization after microcode loading
0xB	Cache initialization
SEC Error Codes	
0xC – 0xD	Reserved for future AMI SEC error codes
0xE	Microcode not found
0xF	Microcode not loaded

SEC Beep Codes

There are no SEC Beep codes associated with this phase of the Aptio BIOS boot process.

PEI Status Codes

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started

PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
S3 Resume Error Codes	
0xE8	S3 Resume Failed in PEI
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
7	Reset PPI is not available
4	Recovery failed
4	S3 Resume failed

DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization

0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)

0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

DXE Beep Codes

# of Beeps	Description
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
1	Invalid password
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

ACPI/ASL Status Codes

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

OEM-Reserved Status Code Ranges

Status Code	Description
0x5	OEM SEC initialization before microcode loading
0xA	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes