iEi
IEI Integration Corp.

MODEL:

PICOe-945GSE

Half-size PCIe CPU Card with Intel® Atom™ Processor, 512 MB On-board Memory, VGA/LVDS/HDTV-out Dual GbE, Seven USB 2.0, CF Slot and Two SATA

User Manual

Rev. 1.02 - 23 October, 2013

RoHS Lead Free

Revision

Date	Version	Changes
23 October, 2013	1.02	Modified **Section 2.5.4.1: PCI GbE Controllers**
11 March, 2009	1.01	Changed model name
28 November, 2008	1.00	Initial release

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Manual Conventions

WARNING!

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously. Warnings are easy to recognize. The word "warning" is written as "**WARNING**," both capitalized and bold and is followed by text. The text is the warning message. A warning message is shown below:

WARNING:

This is an example of a warning message. Failure to adhere to warning messages may result in permanent damage to the PICOe-945GSE or personal injury to the user. Please take warning messages seriously.

CAUTION!

Cautionary messages should also be heeded to help reduce the chance of losing data or damaging the PICOe-945GSE. Cautions are easy to recognize. The word "caution" is written as "**CAUTION**," both capitalized and bold and is followed. The italicized text is the cautionary message. A caution message is shown below:

CAUTION:

This is an example of a caution message. Failure to adhere to cautions messages may result in permanent damage to the PICOe-945GSE. Please take caution messages seriously.

![NOTE icon] **NOTE:**

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes. Notes are easy to recognize. The word "note" is written as "**NOTE**," both capitalized and bold and is followed by text. The text is the cautionary message. A note message is shown below:

![NOTE icon] **NOTE:**

This is an example of a note message. Notes should always be read. Notes contain critical information about the PICOe-945GSE. Please take note messages seriously.

Packing List

> ![NOTE] **NOTE:**
>
> If any of the components listed in the checklist below are missing, please do not proceed with the installation. Contact the IEI reseller or vendor you purchased the PICOe-945GSE from or contact an IEI sales representative directly. To contact an IEI sales representative, please send an email to sales@iei.com.tw.

The items listed below should all be included in the PICOe-945GSE package.

- 1 x PICOe-945GSE Single Board Computer
- 1 x Mini Jumper Pack
- 2 x SATA cable
- 1 x Keyboard/Mouse Y cable
- 1 x Dual RS-232 cable
- 1 x USB cable
- 1 x Utility CD
- 1 x QIG

Images of the above items are shown in **Chapter 3**.

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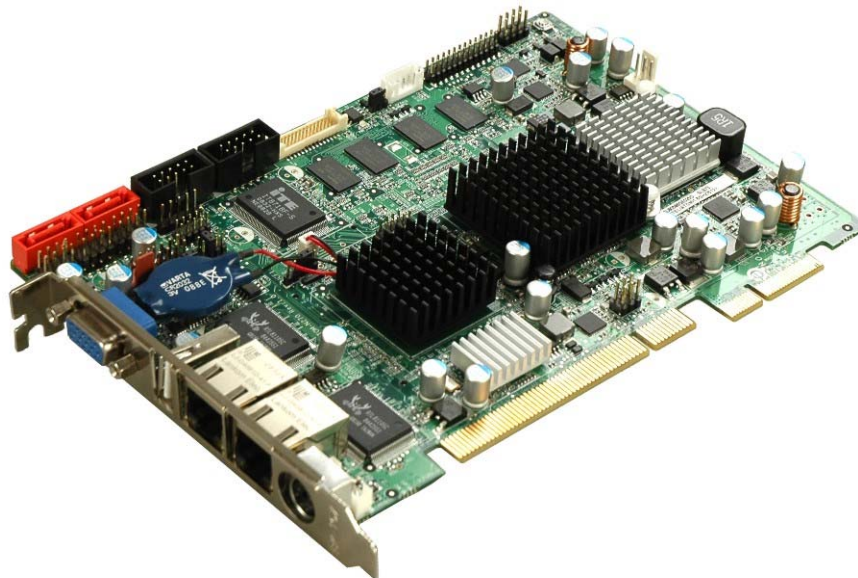
Figure 1-1: PICOe-945GSE

1.1.1 PICOe-945GSE Introduction

The PICOe-945GSE half-size PCIe CPU card is embedded 45 nm Intel® Atom™ processor platform. The Intel® Atom™ processor N270 embedded on the PICOe-945GSE has a 1.60 GHz clock speed, a 533 MHz FSB and a 512 KB L2 cache. The PICOe-945GSE has 512 MB 533 MHz DDR2 memory onboard and also supports one 200-pin 533 MHz 2.0 GB (max.) DDR2 SDRAM SO-DIMM. The board comes with one LVDS connector and supports 18-bit dual-channel LVDS screens. The PICOe-945GSE also comes with two PCI Gigabit Ethernet (GbE) connectors, two SATA connectors and seven USB 2.0 connectors.

1.2 PICOe-945GSE Overview

1.2.1 PICOe-945GSE Overview Photo

The PICOe-945GSE has a wide variety of peripheral interface connectors. **Figure 1-2** is a labeled photo of the peripheral interface connectors on the PICOe-945GSE.
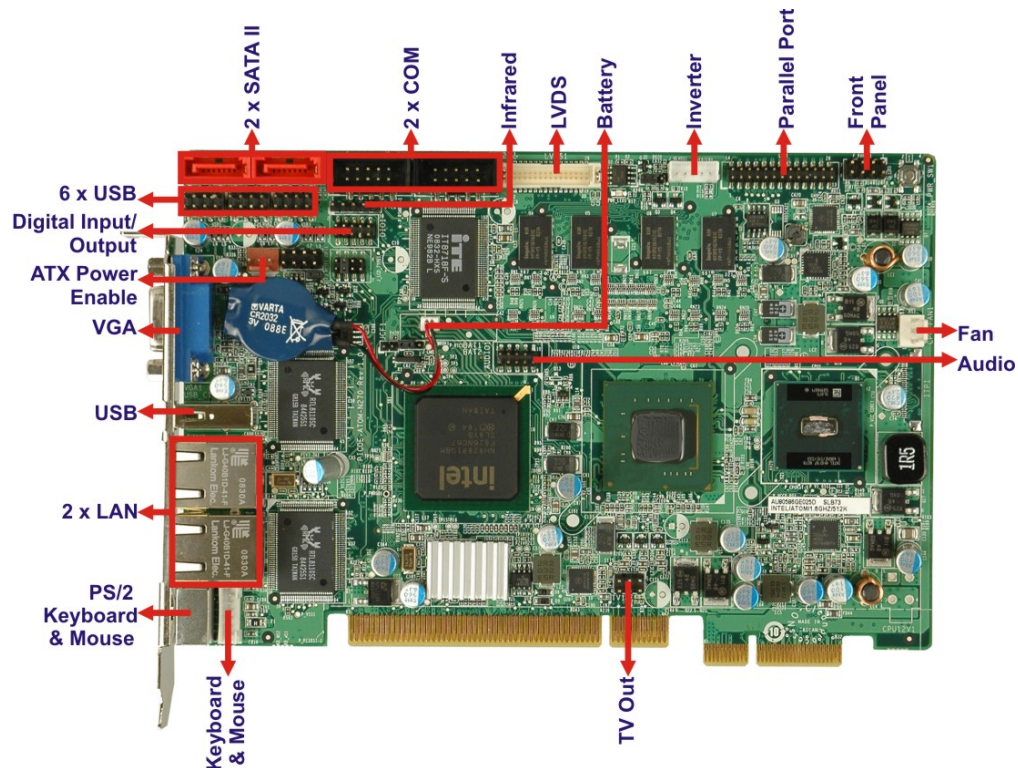
Figure 1-2: PICOe-945GSE Overview [Front View]

Figure 1-3 shows the rear side of the PICOe-945GSE.
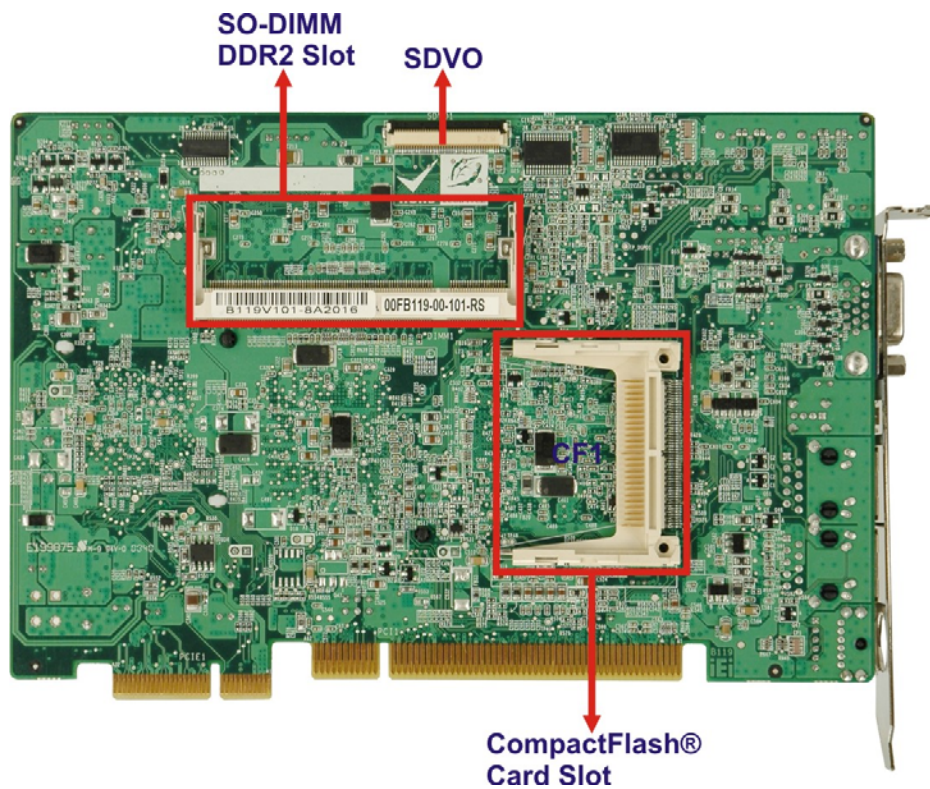
Figure 1-3: PICOe-945GSE Overview [Solder Side]

1.2.2 PICOe-945GSE Peripheral Connectors and Jumpers

The PICOe-945GSE has the following connectors on-board:

- 1 x ATX power supply enable connector
- 1 x Audio connector
- 1 x Backlight inverter connector
- 1 x CompactFlash® socket
- 1 x Digital input/output (DIO) connector
- 1 x Fan connector
- 1 x Front panel connector
- 1 x Infrared interface (IrDA) connector
- 1 x Keyboard connector
- 1 x LVDS connector
- 1 x Parallel port connector
- 2 x Serial ATA (SATA) drive connectors

■ 1 x SDVO connector

■ 2 x RS-232 serial port connectors

■ 1 x TV Out connector

■ 3 x USB 2.0 connectors (supports six USB 2.0 devices)

The PICOe-945GSE has the following external peripheral interface connectors on the board rear panel.

■ 2 x Ethernet connectors

■ 1 x PS/2 connector

■ 1 x USB connector

■ 1 x VGA connector

The PICOe-945GSE has the following on-board jumpers:

■ AT power selection

■ Clear CMOS

■ CF card setup

■ LVDS Voltage Selection

■ LVDS Panel Resolution Selection

■ J_PCIE1

1.2.3 Technical Specifications

PICOe-945GSE technical specifications are listed in **Table 1-1**. See **Chapter 2** for details.

Specification	PICOe-945GSE
System CPU	45 nm 1.6 GHz Intel® Atom™ N270
Front Side Bus (FSB)	533 MHz
System Chipset	Northbridge: Intel® 945GSE Southbridge: Intel® ICH7-M

Memory	One 512 MB 533 MHz DDR2 memory on-board One 200-pin SO-DIMM socket supports one 533/400 MHz 2.0 GB (max.) DDR2 SDRAM SO-DIMM
CompactFlash®	One CompactFlash® Type I/II socket
Super I/O	ITE IT8718F
Display	Intel® Generation 3.5 integrated GFX core (133 MHz) HDTV with 1080i maximum resolution supported 18-bit dual-channel LVDS integrated in Intel® 945GSE
BIOS	AMI BIOS label
Audio	5.1 channel audio kit with Realtek ALC655 AC'97 codec 7.1 channel HD audio kit with Realtek ALC883 codec supports dual audio streams
LAN	Two Realtek RTL8110SC GbE controllers
COM	Two RS-232 serial ports
USB2.0	Seven USB 2.0 devices supported: ■ Six by onboard pin-headers ■ One by external connector
SATA	Two 1.5 Gbps SATA drives supported
Keyboard/mouse	One external PS/2 connector
Parallel Port	One 26-pin parallel port connector
Digital I/O	One 8-bit digital input/output connector; 4-bit input/4-bit output through the ITE IT8718F super I/O
Watchdog Timer	Software programmable 1-255 sec. through the ITE super I/O

Infrared	One infrared connector through the ITE super I/O. Supports: ■ Serial Infrared (SIR) ■ Amplitude Shift Keyed IR (ASKIR)
Power Supply	ATX and AT power supported
Power Consumption	5V @ 2.89A, 12V@0.22A, 5VSB@0.03A (1.6 GHz Intel® Atom™ N270 CPU with one 512 MB 533 MHz DDR2 SO-DIMM)
Temperature	0ºC – 60ºC (32ºF - 140ºF)
Humidity (operating)	5%~95% non-condensing
Dimensions (LxW)	185 mm x 122 mm
Weight (GW/NW)	1000g/250g

Table 1-1: Technical Specifications

Chapter

2

Detailed Specifications

2.1 Dimensions

2.1.1 Board Dimensions

The dimensions of the board are listed below:

- ■ **Length**:   165 mm
- ■ **Width**:   115 mm
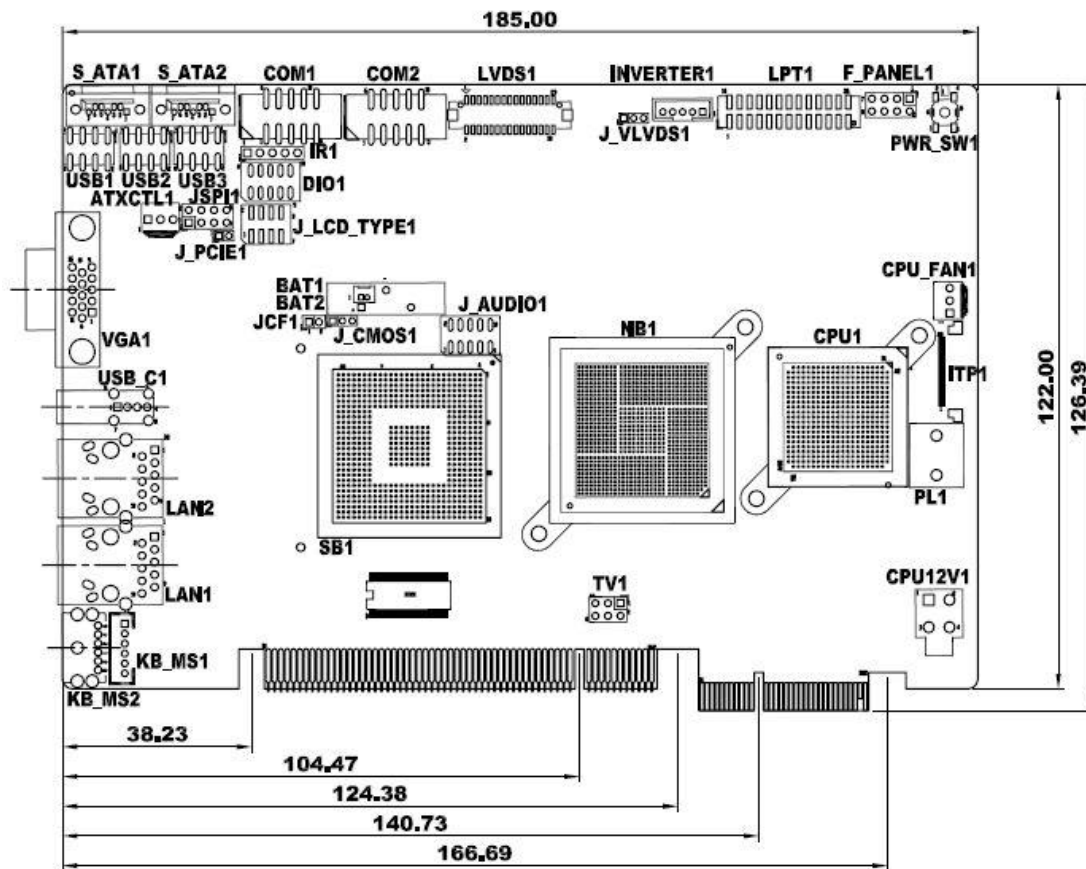
Figure 2-1: PICOe-945GSE Dimensions (mm)

2.1.2 External Interface Panel Dimensions

External peripheral interface connector panel dimensions are shown in **Figure 2-2**.
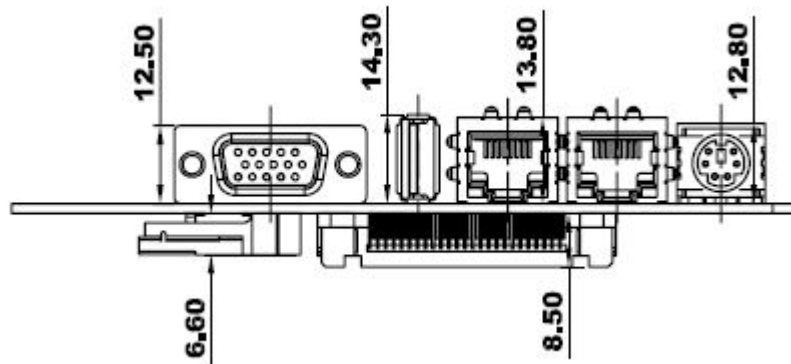
Figure 2-2: External Interface Panel Dimensions (mm)

2.2 Data Flow

Figure 2-3 shows the data flow between the two on-board chipsets and other components installed on the CPU card and described in the following sections of this chapter.
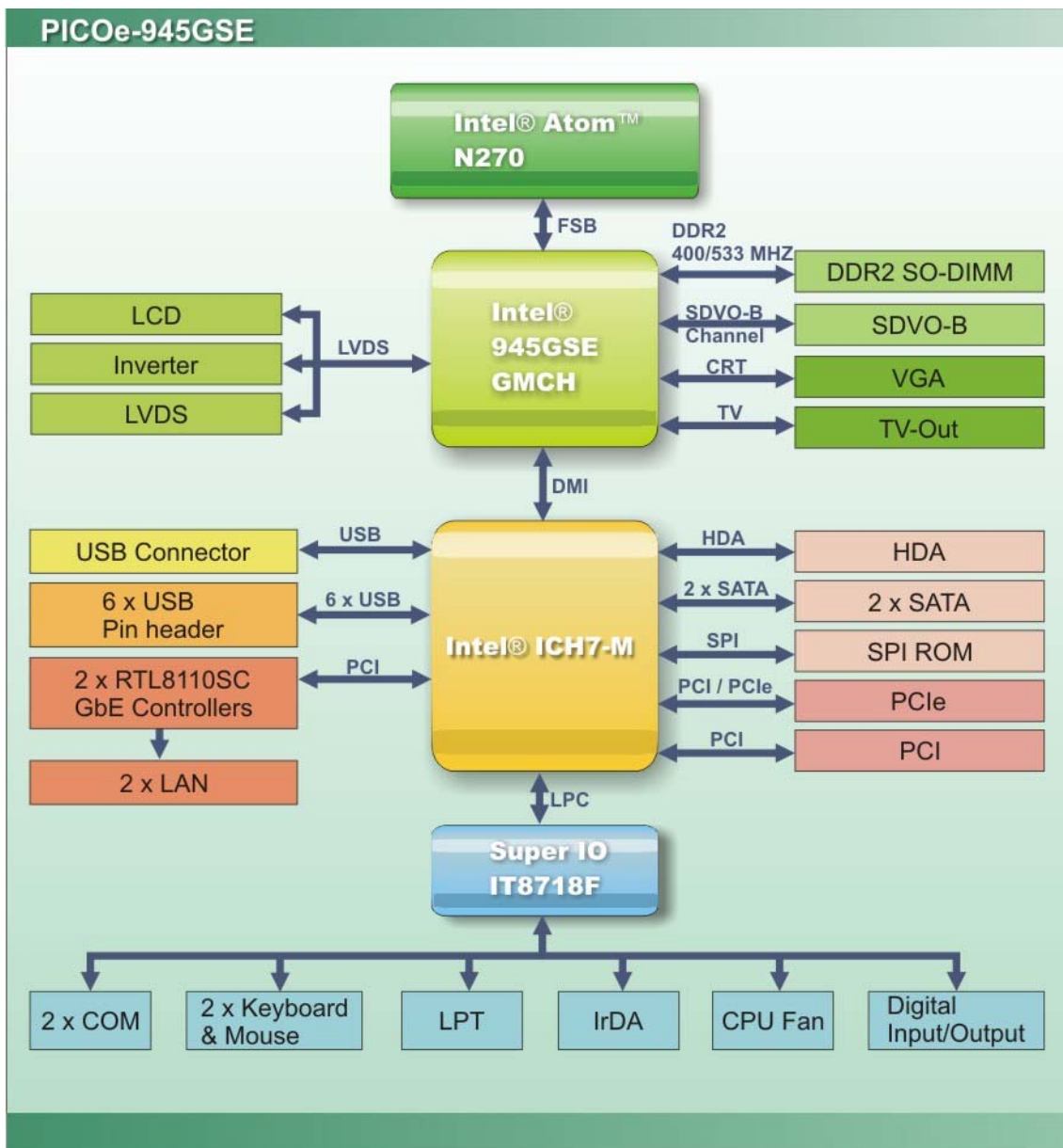
Figure 2-3: Data Flow Block Diagram

2.3 Embedded PICOe-945GSE Processor

2.3.1 Overview

The PICOe-945GSE comes with an embedded 45 nm 1.60 GHz Intel® Atom™ processor N270. The processor supports a 533 MHz FSB and has a 1.6 GHz 512 KB L2 cache. The

low power processor has a maximum power of 2.5 W. The processor is shown in **Figure 2-4** below.
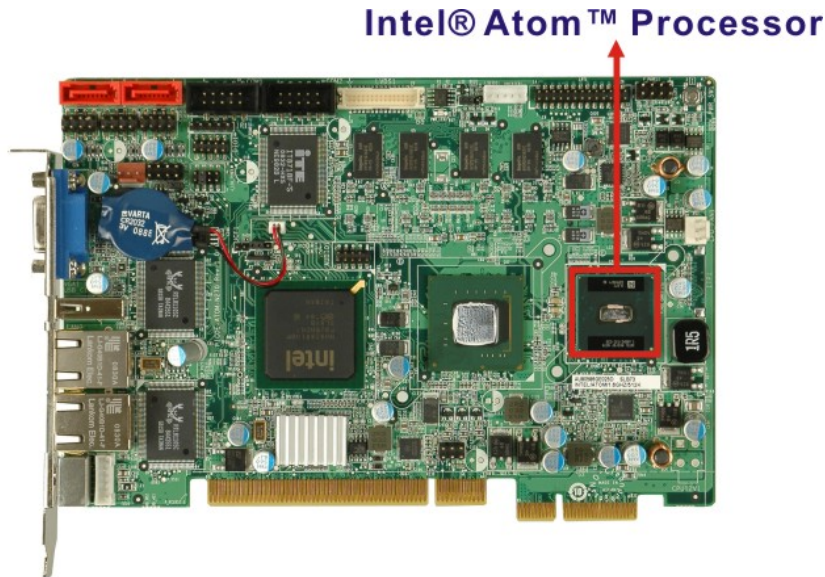
Figure 2-4: Embedded Processor

2.3.2 Features

Some of the features of the Intel® Atom™ processor N270 are listed below

- On-die, primary 32-kB instructions cache and 24-kB write-back data cache
- 533-MHz source-synchronous front side bus (FSB)
- 2-Threads support
- On-die 512-kB, 8-way L2 cache
- Support for IA 32-bit architecture
- Intel® Streaming SIMD Extensions-2 and -3 (Intel® SSE2 and Intel® SSE3) support and Supplemental Streaming SIMD Extension 3 (SSSE3) support
- Micro-FCBGA8 packaging technologies
- Thermal management support via Intel® Thermal Monitor 1 and Intel Thermal Monitor 2
- FSB Lane Reversal for flexible routing
- Supports C0/C1(e)/C2(e)/C4(e)
- L2 Dynamic Cache Sizing

- Advanced power management features including Enhanced Intel SpeedStep® Technology
- Execute Disable Bit support for enhanced security

2.3.3 Front Side Bus (FSB)

The Intel® Atom™ processor on the PICOe-945GSE is interfaced to the Intel® 945GSE through a 533 MHz front side bus (FSB). The FSB is shown in **Figure 2-5** below.
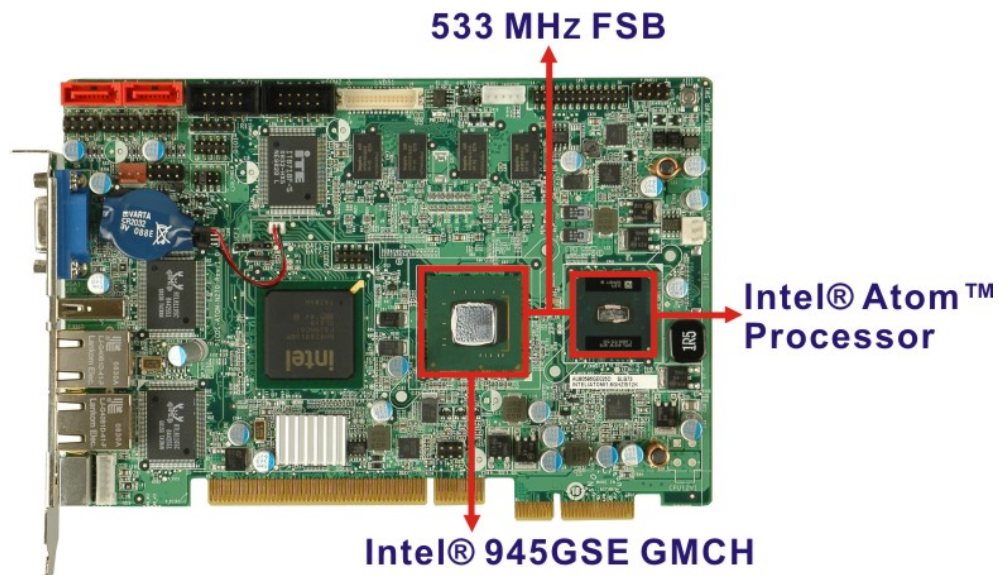
Figure 2-5: Front Side Bus

2.4 Intel 945GSE Northbridge Chipset

2.4.1 Intel® 945GSE Overview

The Intel® 945GSE Graphics and Memory Controller Hub (GMCH) supports the embedded Intel® Atom™ N270 processor. The Intel® 945GSE is interfaced to the processor through a 533 MHz FSB.

2.4.2 Intel® 945GSE DDR2 Controller

2.4.2.1 On-board DDR2 SDRAM

512 MB 533 MHz DDR2 SDRAM is embedded on the PICOe-945GSE. The on-board SDRAM chips are shown in **Figure 2-6**.
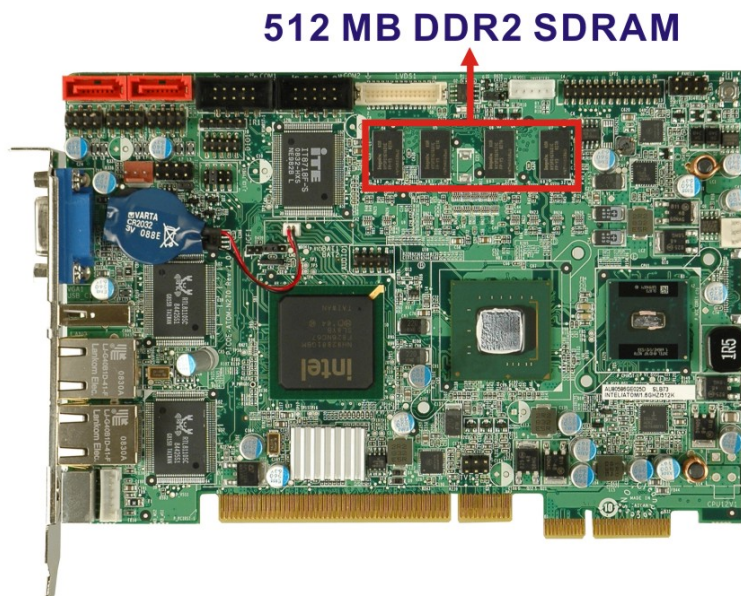
Figure 2-6: On-board DDR2 SDRAM Chips

2.4.2.2 DDR2 SO-DIMM Socket

There is one 200-pin DDR2 SO-DIMM socket on the PICOe-945GSE. The socket supports DDR2 SO-DIMM with the following specifications:

■ Maximum Memory supported 2 GB (1 GB per rank)

■ Support for DDR2 at 400 MHz and 533 MHz

■ No support for Dual-Channel Interleaved mode of operation

■ Enhanced Addressing support (Swap only)

The SO-DIMM socket is shown in **Figure 2-7** below.
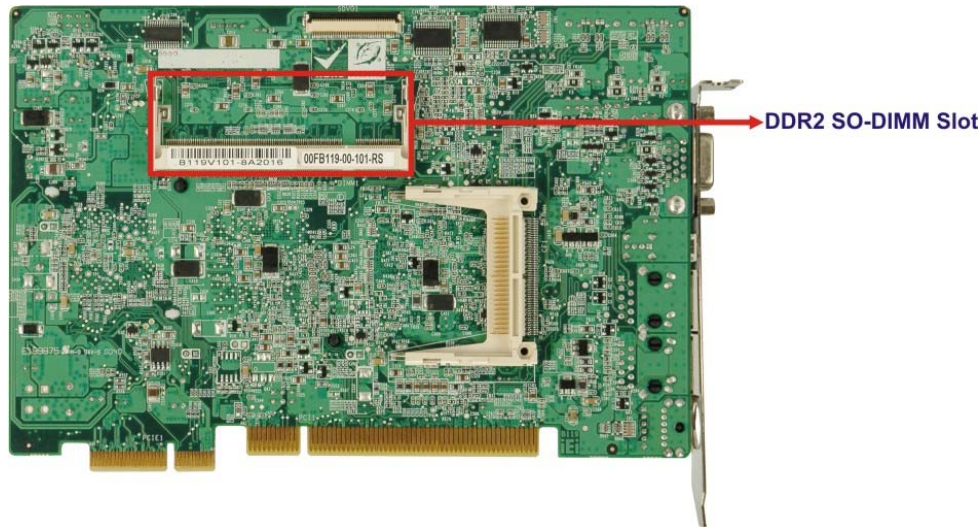
Figure 2-7: DDR2 SO-DIMM Socket

2.4.3 Intel® 945GSE Graphics

The Intel® 945GSE supports CRT, LVDS, TV-Out and SDVO. The internal graphics engine has the following features:

■ Intel® Gen 3.5 Integrated Graphics Engine

■ 250-MHz core render clock and 200 MHz core display clock at 1.05-V core voltage

■ Supports TV-Out, LVDS, CRT and SDVO

■ Dynamic Video Memory Technology (DVMT 3.0)

■ Intel® Display Power Saving Technology 2.0 (Intel® DPST 2.0)

■ Intel® Smart 2D Display Technology (Intel® S2DDT)

■ Intel® Automatic Display Brightness

■ Video Capture via x1 concurrent PCIe port

■ Concurrent operation of PCIe x1 and SDVO

■ 4x pixel rate HWMC

- Microsoft DirectX* 9.1 operating system
- Intermediate Z in Classic Rendering
- Internal Graphics Display Device States: D0, D1, D3
- Graphics Display Adapter States: D0, D3.

2.4.3.1 Analog CRT Graphics Mode

The analog CRT bus is interfaced to an external DB-15 interface connector. The connector is shown below.
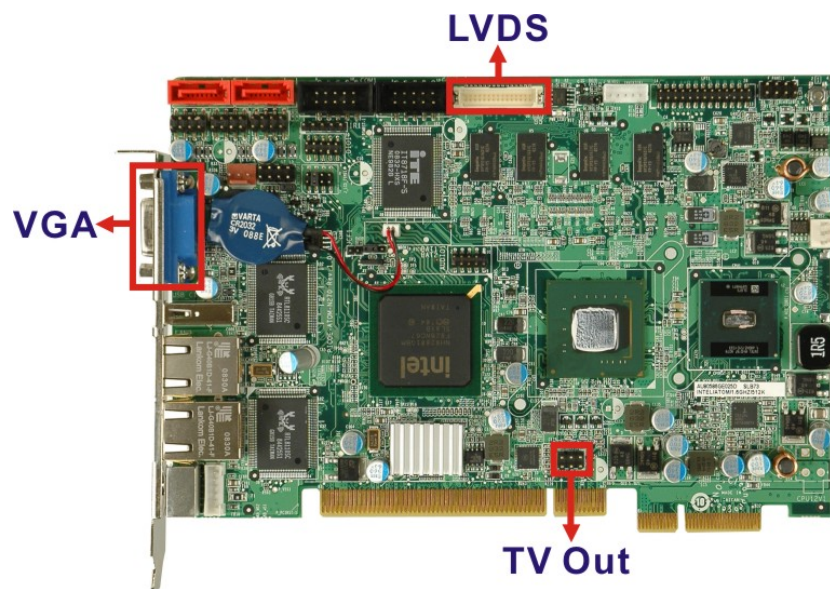
Figure 2-8: VGA Connector

Some of the features of the CRT include:

- Integrated 400-MHz RAMDAC
- Analog Monitor Support up to QXGA
- Support for CRT Hot Plug

2.4.3.2 LVDS Interface

The LVDS interface is connected directly to the LVDS connector on the board. Some of the features of the LVDS interface include:

- Panel support up to UXGA (1600 x 1200)
- 25-MHz to 112-MHz single-/dual-channel; @18 bpp
    ○ TFT panel type supported
- Pixel Dithering for 18-bit TFT panel to emulate 24-bpp true color displays
- Panel Fitting. Panning, and Center Mode Supported
- CPIS 1.5 compliant
- Spread spectrum clocking supported
- Panel Power Sequencing support
- Integrated PWM interface for LCD backlight inverter control

2.4.3.3 TV Out Interface

The TV Out interface has the following features.

- Three integrated 10-bit DACS
- Overscaling
- NTSC/PAL
- Component, S-Video and Composite Output interfaces
- HDTV support
    ○ 480p/720p/1080i/1080p

2.4.3.4 Serial Digital Video Output (SDVO)

Some of the features of the SDVO ports are listed below.

- Concurrent operation of PCIe x1 with SDVO
- Two SDVO ports supported
    ○ SDVO is muxed onto the PCIe pins
    ○ DVI 1.0 support for external digital monitor
    ○ Only Downstream HDCP support
    ○ Supports TV and DVD formats
    ○ Display hot plug support

2.5 Intel® ICH7-M Southbridge Chipset

2.5.1 Intel® ICH7-M Overview

The Intel® ICH7-M chipset is connected to the Intel® 945GSE GMCH through the chip-to-chip Direct Media Interface (DMI). Some of the features of the Intel® ICH7-M are listed below.

- Complies with PCI Express Base Specification, Revision 1.0a
- Complies with PCI Local Bus Specification, Revision 2.3 and supports 33MHz PCI operations
- Supports ACPI Power Management Logic
- Contains:
  - ○ Enhanced DMA controller
  - ○ Interrupt controller
  - ○ Timer functions
- Integrated SATA host controller with DMA operations interfaced to two SATA connectors on the PICOe-945GSE
- Supports the four USB 2.0 devices on the PICOe-945GSE with four UHCI controllers and one EHCI controller
- Complies with System Management Bus (SMBus) Specification, Version 2.0
- Supports Audio Codec '97 (AC'97) Revision 2.3
- Supports Intel® High Definition Audio
- Contains Low Pin Count (LPC) interface
- Supports Firmware Hub (FWH) interface
- Serial peripheral interface support

2.5.2 Intel® ICH7-M Audio Controllers

The Intel® ICH7-M has the following to audio controllers.

- AC'97 controller
- HD Audio controller

The controllers share the same pins and only one can be activated at a time. The controllers are interfaced to the PICOe-945GSE audio connector which is in turn connected to an option audio kit with either an AC'97 codec or an HD Audio codec.

2.5.2.1 Intel® ICH7-M Audio Codec '97 Controller

The Audio Codec '97 (AC'97) controller integrated into the ICH7-M complies with AC'97 Component Specification, Version 2.3. The AC'97 controller is connected to the onboard audio connector. The audio connector is connected to an optional 5.1 channel audio kit with an embedded AC'97 audio codec. The AC'97 controller supports up to six PCM audio output channels. Complete surround sound requires six-channel audio consisting of:

- Front left
- Front right
- Back left
- Back right
- Center
- Subwoofer

2.5.2.2 Intel® ICH7-M High Definition (HD) Audio Controller

The Intel® HD Audio controller on the Intel® ICH7-M shares pins with the AC'97 controller. Only one controller can be used at a time. Intel® HD Audio controller is interfaced through the Intel® High Definition Audio serial link to the audio connector which is in turn connected to an optional 7.1 channel audio kit with an HD audio codec.

2.5.3 Intel® ICH7-M Low Pin Count (LPC) Interface

The ICH7-M LPC interface complies with the LPC 1.1 specifications. The LPC bus from the ICH7-M is connected to the following components:

- BIOS chipset
- Super I/O chipset

2.5.4 Intel® ICH7-M PCI Interface

The PCI interface on the ICH7-M is compliant with the PCI Revision 2.3 implementation. Some of the features of the PCI interface are listed below.

- PCI Revision 2.3 compliant
- 33 MHz
- 5V tolerant PCI signals (except PME#)
- Integrated PCI arbiter supports up to seven PCI bus masters

The PCI bus is connected to an interface gold finger on the bottom of the CPU cards and supports four expansion PCI cards on the backplane.
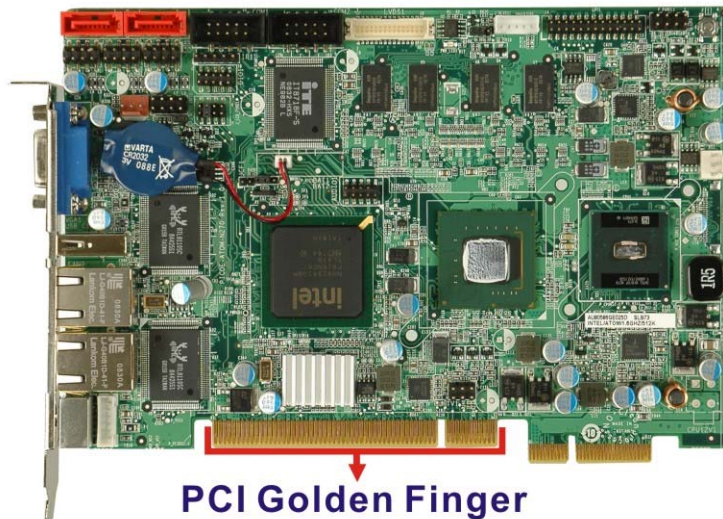
Figure 2-9: PCI Golden Finger

2.5.4.1 PCI GbE Controllers

Two of the PCI lanes are implemented on the PICOe-945GSE through Realtek RTL8110SC PCI GbE controllers and then connected to two RJ-45 Ethernet connectors (**Figure 2-10**).
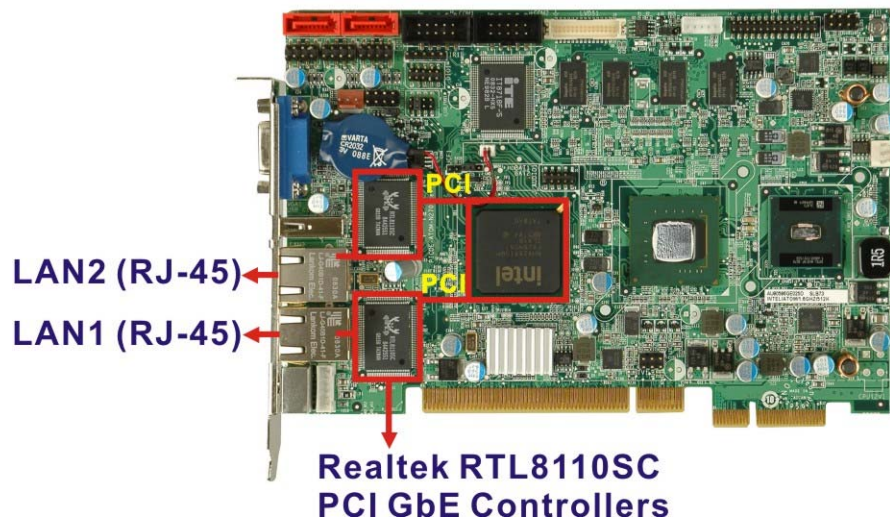
Figure 2-10: RJ-45 Connectors and GbE Controllers

The Realtek RTL8110SC PCI GbE controllers combine a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, 32-bit PCI bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, they offer high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

Some of the features of the Realtek RTL8110SC PCI GbE controllers are listed below.

- Integrated 10/100/1000 transceiver
- Auto-Negotiation with Next Page capability
- Supports PCI rev.2.3, 32-bit, 33 MHz/66 MHz
- Supports pair swap/polarity/skew correction
- Crossover Detection & & Auto-Correction
- Wake-on-LAN and remote wake-up support
- Microsoft® NDIS5, NDIS6 Checksum Offload (IPv4, IPv6, TCP, UDP) and Segmentation Task-offload (Large send and Giant send) support
- Supports Full Duplex flow control (IEEE 802.3x)
- Fully compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab

- ■ Supports IEEE 802.1P Layer 2 Priority Encoding

- ■ Supports IEEE 802.1Q VLAN tagging

- ■ Serial EEPROM

- ■ Transmit/Receive on-chip buffer support

- ■ Supports power down/link down power saving

- ■ Supports PCI MSI (Message Signaled Interrupt) and MSI-X

- ■ Supports Receive-Side Scaling (RSS)

2.5.5 Intel® ICH7-M PCIe Bus

The Intel® ICH7-M chipset has four PCIe lanes. The four PCIe lanes are interfaced through a golden finger on the bottom of the CPU card through a compatible half-size backplane to either four PCIe x1 expansion cards or one PCIe x4 expansion card on. The PCIe x4 golden finger is shown in **Figure 2-11** below.
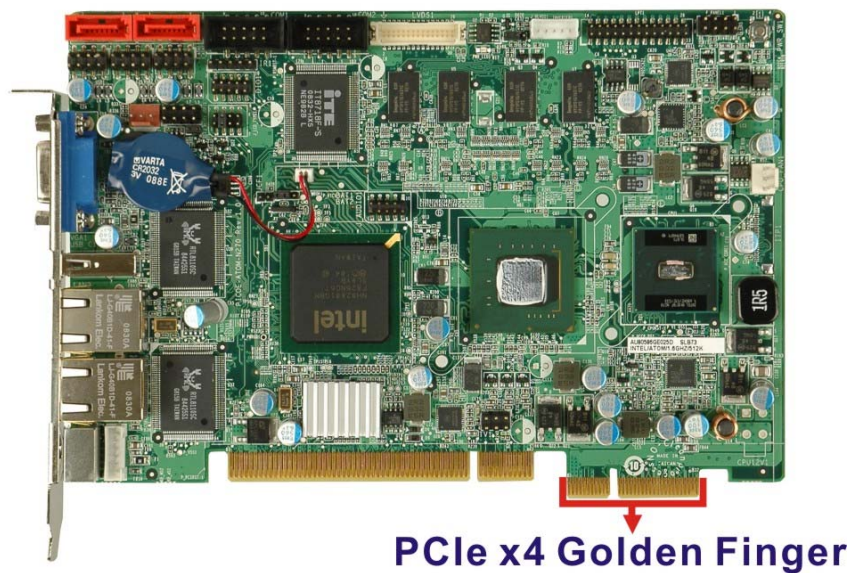
Figure 2-11: PCIe x4 Golden finger

2.5.6 Intel® ICH7-M Real Time Clock

256 bytes of battery backed RAM is provided by the Motorola MC146818A real time clock (RTC) integrated into the ICH7-M. The RTC operates on a 3V battery and 32.768KHz crystal. The RTC keeps track of the time and stores system data even when the system is turned off.

2.5.7 Intel® ICH7-M SATA Controller

The integrated SATA controller on the ICH7-M supports up to two SATA drives with independent DMA operations. Two SATA controllers are connected to two SATA connectors on the PICOe-945GSE. The SATA connectors are shown in **Figure 2-12**.
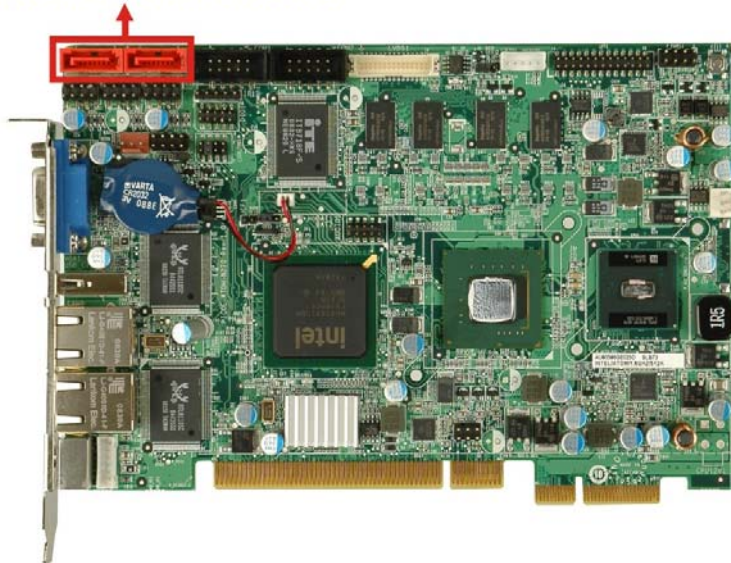
Figure 2-12: SATA Connectors

SATA controller specifications are listed below.

- Supports two SATA drives
- Supports 1.5 Gb/s data transfer speeds
- Supports Serial ATA Specification, Revision 1.0a

2.5.8 Intel® ICH7-M USB Controller

Up to seven high-speed, full-speed or low-speed USB devices are supported by the ICH7-M on the PICOe-945GSE. High-speed USB 2.0, with data transfers of up to 480MB/s, is enabled with the ICH7-M integrated Enhanced Host Controller Interface (EHCI) compliant host controller. USB full-speed and low-speed signaling is supported by the ICH7-M integrated Universal Host Controller Interface (UHCI) controllers.

The seven USB ports implemented on the PICOe-945GSE are connected to three internal connectors and one external connector. See **Figure 2-13**.
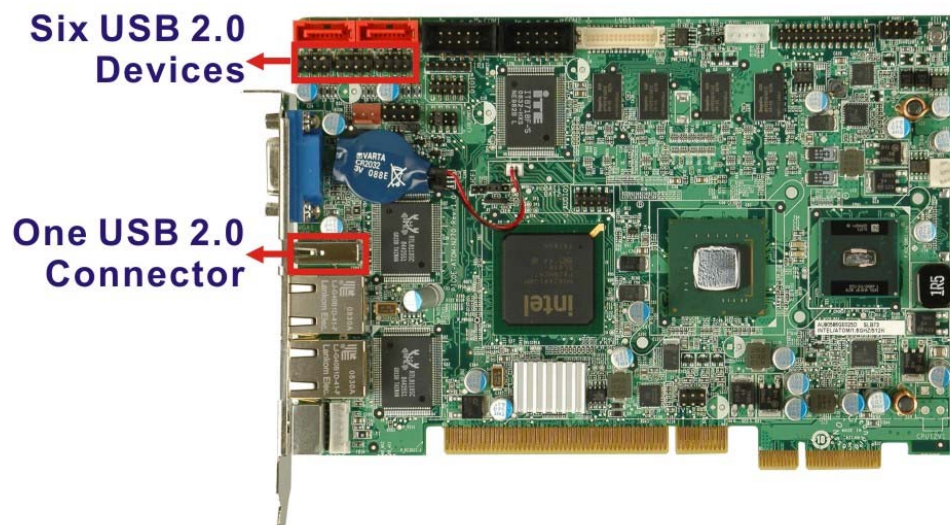
Figure 2-13: Onboard USB Implementation

2.6 LPC Bus Components

2.6.1 LPC Bus Overview

The ICH7-M LPC bus is connected to components listed below:

- Super I/O chipset
- LPC Serial Port Chipset

2.6.2 iTE IT8718F Super I/O Chipset

The iTE IT8718F Super I/O chipset is connected to the ICH7-M through the LPC bus.
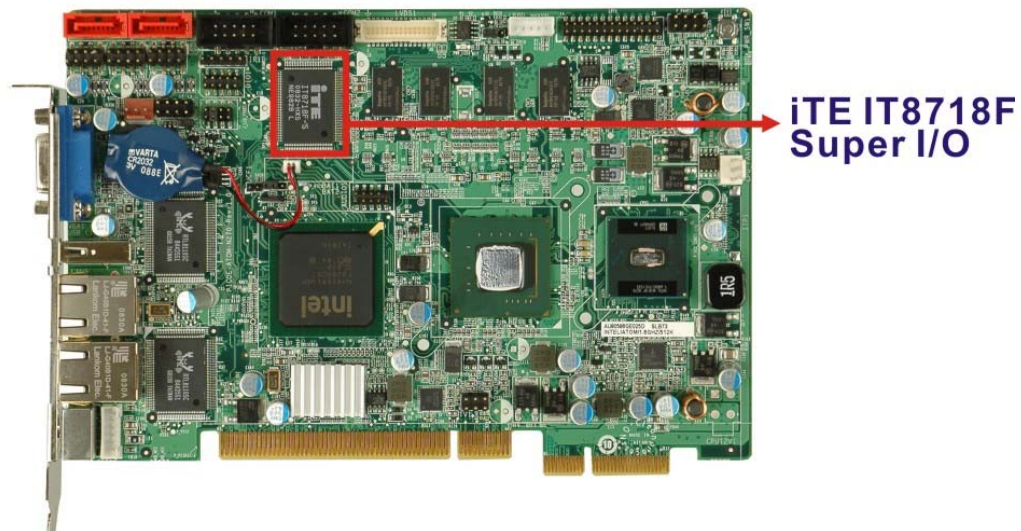
Figure 2-14: Super I/O

The iTE IT8718F is an LPC interface-based Super I/O device that comes with Environment Controller integration. Some of the features of the iTE IT8718F chipset are listed below:

- ACPI and LANDesk Compliant
- Enhanced Hardware Monitor
- Fan Speed Controller
- Two 16C550 UARTs for serial port control
- One IEEE 1284 Parallel Port
- Keyboard Controller
- Watchdog Timer

Some of the Super I/O features are described in more detail below:

2.6.2.1 Super I/O LPC Interface

The LPC interface on the Super I/O complies with the Intel® Low Pin Count Specification Rev. 1.0. The LPC interface supports both LDRQ# and SERIRQ protocols as well as PCI PME# interfaces.

2.6.2.2 Super I/O 16C550 UARTs

The onboard Super I/O has two integrated 16C550 UARTs that can support the following:

- Two standard serial ports (COM1 and COM2)
- IrDa 1.0 and ASKIR protocols

2.6.2.3 Super I/O Digital Input/Output

The input mode supports switch debouncing or programmable external IRQ routing. The output mode supports two sets of programmable LED blinking periods.

2.6.2.4 Super I/O Enhanced Hardware Monitor

The Super I/O Enhanced Hardware Monitor monitors three thermal inputs, VBAT internally, and eight voltage monitor inputs. These hardware parameters are reported in the BIOS and can be read from the BIOS Hardware Health Configuration menu.

2.6.2.5 Super I/O Fan Speed Controller

The Super I/O fan speed controller enables the system to monitor the speed of the fan. One of the pins on the fan connector is reserved for fan speed detection and interfaced to the fan speed controller on the Super I/O. The fan speed is then reported in the BIOS.

2.6.2.6 Super I/O Keyboard/Mouse Controller

The Super I/O keyboard/mouse controller can execute the 8042 instruction set. Some of the keyboard controller features are listed below:

- The 8042 instruction is compatible with a PS/2 keyboard and PS/2 mouse
- Gate A20 and Keyboard reset output
- Supports multiple keyboard power on events

■ Supports mouse double-click and/or mouse move power on events

2.6.2.7 Super I/O Parallel Port

The multi-mode high-performance parallel port supports the bi-directional Standard Parallel Port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP) modes.

2.7 Environmental and Power Specifications

2.7.1 System Monitoring

Two thermal inputs on the PICOe-945GSE Super I/O Enhanced Hardware Monitor monitor the following temperatures:

■ System temperature
■ CPU temperature

Eight voltage inputs on the PICOe-945GSE Super I/O Enhanced Hardware Monitor monitor the following voltages:

■ CPU Core
■ +1.05V
■ +3.30V
■ +5.00V
■ +12.0 V
■ +1.5V
■ +1.8V
■ 5VSB
■ VBAT

The PICOe-945GSE Super I/O Enhanced Hardware Monitor also monitors the following fan speeds:

■ CPU Fan speed

The values for the above environmental parameters are all recorded in the BIOS Hardware Health Configuration menu.

2.7.2 Operating Temperature and Temperature Control

The maximum and minimum operating temperatures for the PICOe-945GSE are listed below.

- Minimum Operating Temperature: 0ºC (32°F)
- Maximum Operating Temperature: 60°C (140°F)

A heat sink must be installed on the CPU. Thermal paste must be smeared on the lower side of the heat sink before it is mounted on the CPU. Heat sinks are also mounted on the Northbridge and Southbridge chipsets to ensure the operating temperature of these chips remain low.

2.7.3 Power Consumption

Table 2-1 shows the power consumption parameters for the PICOe-945GSE running with a 1.6 GHz Intel® Atom™ processor N270 with 512 MB 533 MHz DDR2 memory.

Voltage	Current
+5V	2.89A
+12V	0.22A
5VSB	0.03A

Table 2-1: Power Consumption

Chapter

3

Unpacking

3.1 Anti-static Precautions

WARNING!

Failure to take ESD precautions during the installation of the PICOe-945GSE may result in permanent damage to the PICOe-945GSE and severe injury to the user.

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the PICOe-945GSE. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the PICOe-945GSE, or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- *Wear an anti-static wristband*: - Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- *Self-grounding*:- Before handling the board touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- *Use an anti-static pad*: When configuring the PICOe-945GSE, place it on an antic-static pad. This reduces the possibility of ESD damaging the PICOe-945GSE.
- *Only handle the edges of the PCB*:- When handling the PCB, hold the PCB by the edges.

3.2 Unpacking

3.2.1 Unpacking Precautions

When the PICOe-945GSE is unpacked, please do the following:

- Follow the anti-static precautions outlined in **Section 3.1**.
- Make sure the packing box is facing upwards so the PICOe-945GSE does not fall out of the box.
- Make sure all the components shown in **Section 3.3** are present.

3.3 Unpacking Checklist

> **NOTE:**
>
> If any of the components listed in the checklist below are missing, do not proceed with the installation. Contact the IEI reseller or vendor the PICOe-945GSE was purchased from or contact an IEI sales representative directly by sending an email to sales@iei.com.tw.

3.3.1 Package Contents

The PICOe-945GSE is shipped with the following components:

Quantity	Item and Part Number	Image
1	PICOe-945GSE	
2	SATA cable (**P/N**: 32000-062800-RS)	
1	KB/MS PS/2 Y-cable (**P/N**: 32000-000138-RS)	
1	Dual RS-232 cable (**P/N**: 19800-000051-RS)	
1	Dual USB cable (w bracket) (**P/N**: CB-USB02-RS)	

1	Mini jumper pack (2.0mm) (**P/N**: 33100-000033-RS)	
1	Utility CD	
1	Quick Installation Guide	

3.3.2 Optional Items

The PICOe-945GSE is shipped with the following components:

Item and Part Number	Image
SATA power cable (**P/N**: 32100-088600-RS)	
LPT cable (w/o bracket) (**P/N**: 32200-015100-RS)	
HDTV output cable (**P/N**: HDTVCABLESET-01)	
Audio kit_ 5.1 Channel (**P/N**: AC-KIT08R-R10)	
Audio kit_ 7.1 Channel (**P/N**: AC-KIT-883HD-R10)	

Chapter

4

Connectors

4.1 Peripheral Interface Connectors

Section **4.1.1** shows peripheral interface connector locations. **Section 4.2** lists all the peripheral interface connectors seen in **Section 4.1.1**.

4.1.1 PICOe-945GSE Layout

Figure 4-1 shows the on-board peripheral connectors, rear panel peripheral connectors and on-board jumpers.
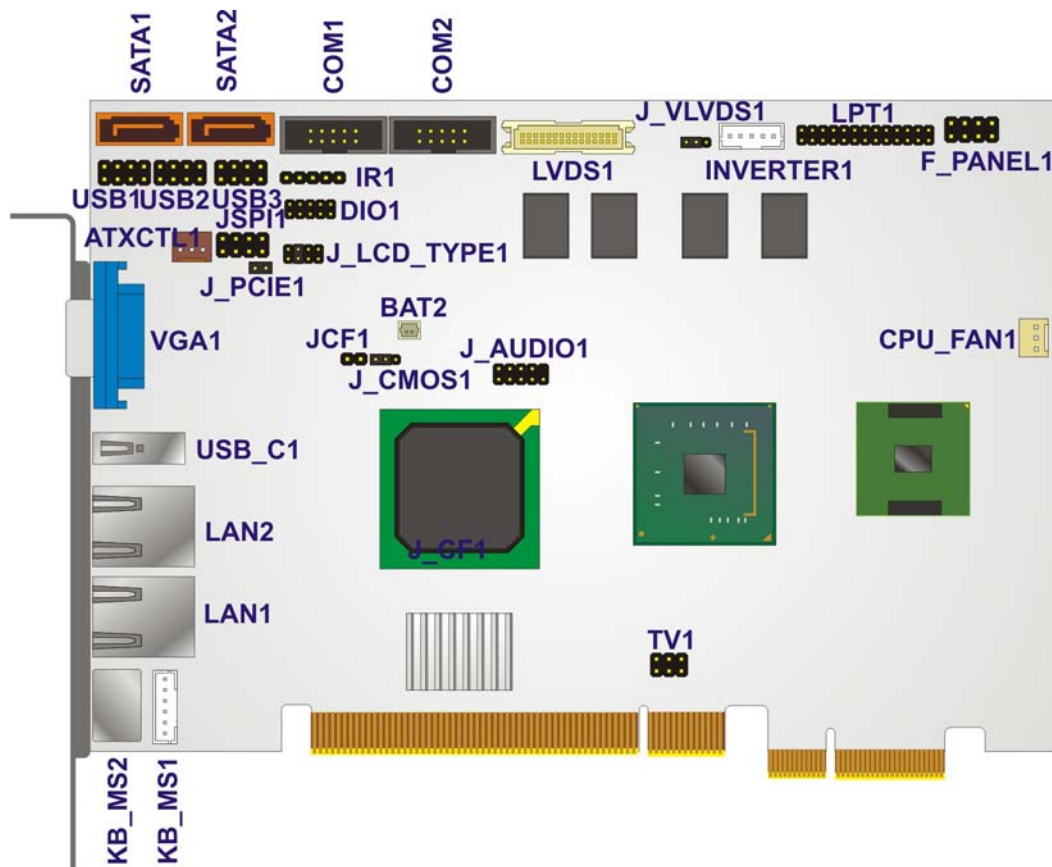
Figure 4-1: Connector and Jumper Locations [Front Side]

Figure 4-2 shows the solder side of the PICOe-945GSE.
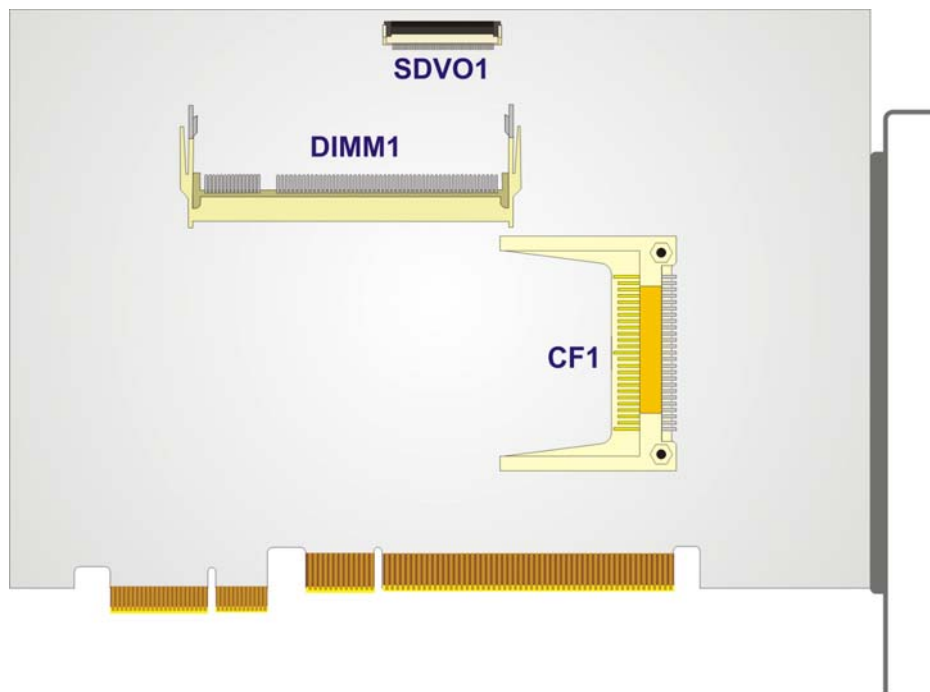
Figure 4-2: Connector and Jumper Locations [Solder Side]

4.1.2 Peripheral Interface Connectors

Table 4-1 shows a list of the peripheral interface connectors on the PICOe-945GSE. Detailed descriptions of these connectors can be found below.

Connector	Type	Label
Audio connector	9-pin header	J_AUDIO1
ATX power control connector	3-pin wafer	ATXCTL1
Backlight inverter connectors	5-pin wafer	INVERTER1
CompactFlash® socket	50-pin CF socket	CF1
Digital input/output (DIO) connector	10-pin header	DIO1
Fan connector	3-pin wafer	CPU_FAN1
Front panel connector	8-pin header	F_PANEL1
Infrared interface (IrDA) connector	5-pin header	IR1

Keyboard connector	6-pin wafer	KB_MS1
LVDS connector	30-pin crimp	LVDS1
Parallel port connector	26-pin header	LPT1
Serial ATA (SATA) drive connectors	7-pin SATA	S_ATA1
Serial ATA (SATA) drive connectors	7-pin SATA	S_ATA2
SDVO connector	48-pin crimp	SDVO1
RS-232 serial port connector	10-pin header	COM1
RS-232 serial port connector	10-pin header	COM2
TV Out connector	6-pin header	TV1
USB 2.0 connector	8-pin header	USB1
USB 2.0 connector	8-pin header	USB2
USB 2.0 connector	8-pin header	USB3

Table 4-1: Peripheral Interface Connectors

4.1.3 External Interface Panel Connectors

Table 4-2 lists the rear panel connectors on the PICOe-945GSE. Detailed descriptions of these connectors can be found in **Section 4.3** on **page 73**.

Connector	Type	Label
Ethernet connector	RJ-45	LAN1
Ethernet connector	RJ-45	LAN2
Keyboard/mouse	PS/2	KB_MS2
USB port	USB port	USB_C1
VGA port connector	15-pin female	VGA1

Table 4-2: Rear Panel Connectors

4.2 Internal Peripheral Connectors

Internal peripheral connectors are found on the CPU card and are only accessible when the CPU card is outside of the chassis. This section has complete descriptions of all the internal, peripheral connectors on the PICOe-945GSE.

4.2.1 ATX Power Supply Enable Connector

CN Label: ATXCTL1

CN Type: 3-pin wafer (1x3)

CN Location: See **Figure 4-3**

CN Pinouts: See **Table 4-3**

The ATX power supply enable connector enables the PICOe-945GSE to be connected to an ATX power supply. In default mode, the PICOe-945GSE can only us an AT power supply. To enable an ATX power supply the AT Power Select jumper must also be configured. Please refer to Chapter 3 for more details.
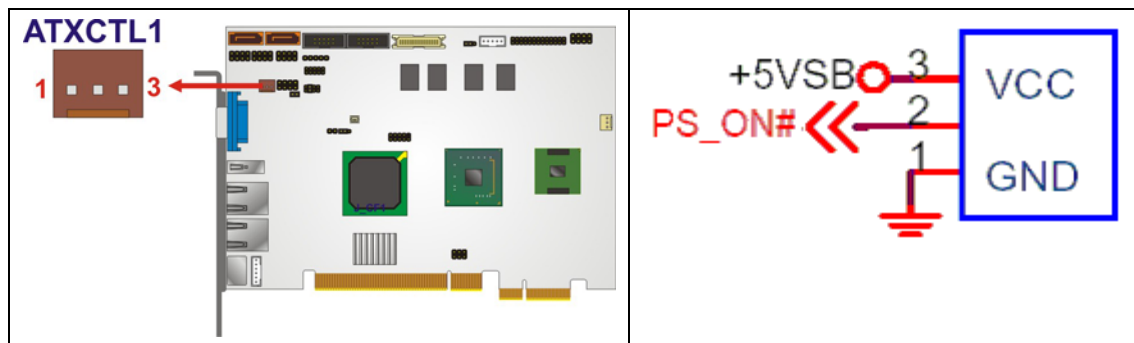
Figure 4-3: ATX Power Supply Enable Connector Location

PIN NO.	DESCRIPTION
1	GND
2	PS-ON
3	+5V Standby

Table 4-3: ATX Power Supply Enable Connector Pinouts

4.2.2 Audio Connector (9-pin)

CN Label: J_AUDIO1

CN Type: 9-pin header (2x5)

CN Location: See **Figure 4-4**

CN Pinouts: See **Table 4-4**

The 9-pin audio connector is connected to external audio devices including speakers and microphones for the input and output of audio signals to and from the system.
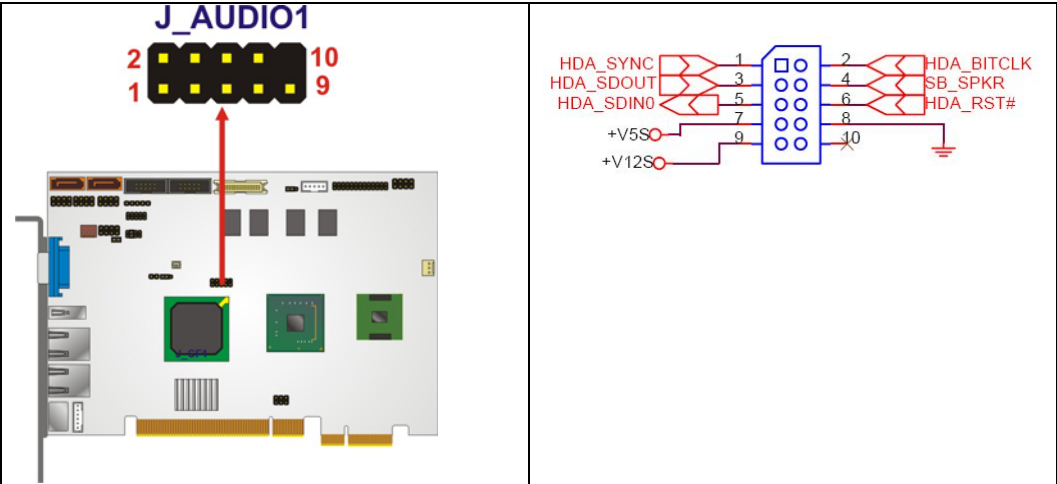
Figure 4-4: Audio Connector Location (9-pin)

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	HDA_SYNC	2	HDA_BITCLK
3	HDA_SDOUT	4	SB_SPKR
5	HDA_SDIN0	6	HDA_RST#
7	VCC	8	GND
9	+12V	10	GND

Table 4-4: Audio Connector Pinouts (9-pin)

4.2.3 Backlight Inverter Connector

CN Label: INVERTER1

CN Type: 5-pin wafer (1x5)

CN Location: See **Figure 4-5**

CN Pinouts: See **Table 4-5**

The backlight inverter connector provides the backlight on the LCD display connected to the PICOe-945GSE with +12V of power.
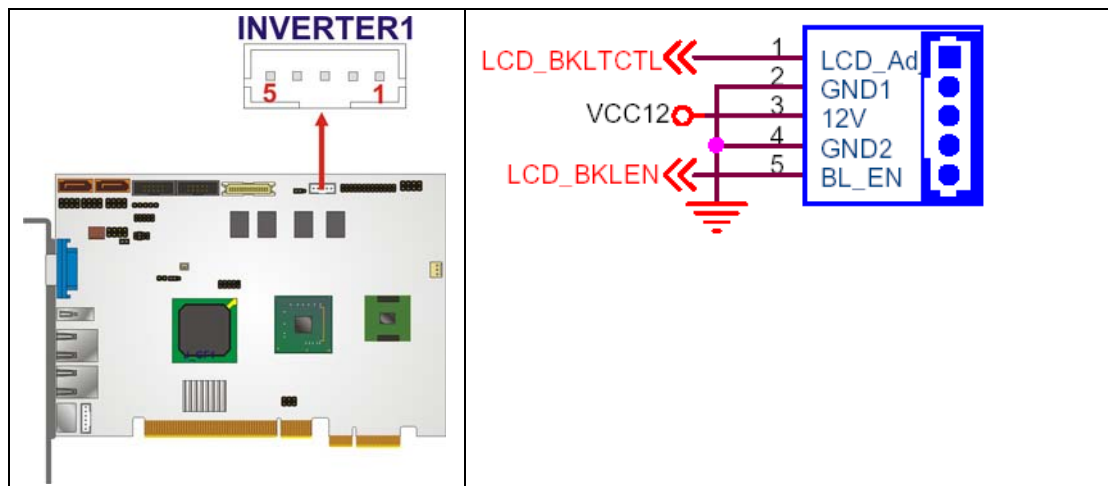
Figure 4-5: Panel Backlight Connector Pinout Locations

PIN NO.	DESCRIPTION
1	LCD Backlight Control
2	GROUND
3	+12V
4	GROUND
5	BACKLIGHT Enable

Table 4-5: Panel Backlight Connector Pinouts

4.2.4 CompactFlash® Socket

CN Label: **CF1** (solder side)

CN Type: 50-pin header (2x25)

CN Location: See **Figure 4-6**

CN Pinouts: See **Table 4-6**

A CF Type I or Type II memory card is inserted to the CF socket on the solder side of the PICOe-945GSE.
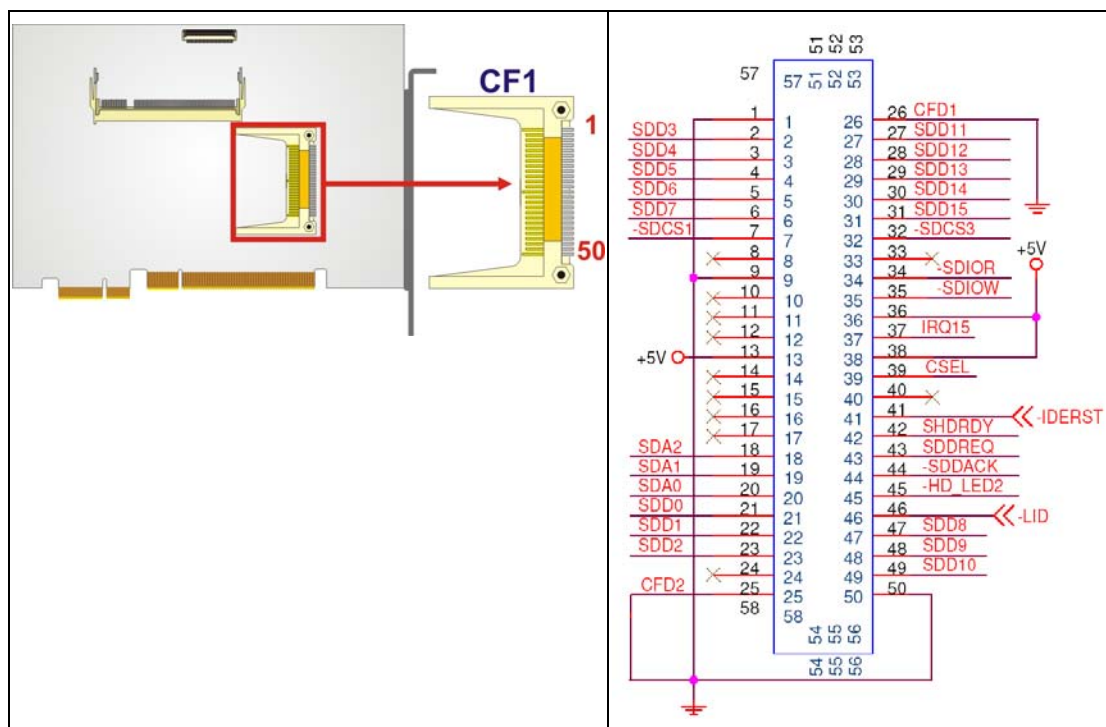
Figure 4-6: CF Card Socket Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GROUND	26	VCC-IN CHECK1
2	DATA 3	27	DATA 11
3	DATA 4	28	DATA 12
4	DATA 5	29	DATA 13

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
5	DATA 6	30	DATA 14
6	DATA 7	31	DATA 15
7	HDC_CS0#	32	HDC_CS1
8	N/C	33	N/C
9	GROUND	34	IOR#
10	N/C	35	IOW#
11	N/C	36	VCC_COM
12	N/C	37	IRQ15
13	VCC_COM	38	VCC_COM
14	N/C	39	CSEL
15	N/C	40	N/C
16	N/C	41	HDD_RESET
17	N/C	42	IORDY
18	SA2	43	SDREQ
19	SA1	44	SDACK#
20	SA0	45	HDD_ACTIVE#
21	DATA 0	46	66DET
22	DATA 1	47	DATA 8
23	DATA 2	48	DATA 9
24	N/C	49	DATA 10
25	VCC-IN CHECK2	50	GROUND

Table 4-6: CF Card Socket Pinouts

4.2.5 Digital Input/Output (DIO) Connector

CN Label: DIO1

CN Type: 10-pin header (2x5)

CN Location: See **Figure 4-7**

CN Pinouts: See **Table 4-7**

The digital input/output connector is managed through a Super I/O chip. The DIO connector pins are user programmable.
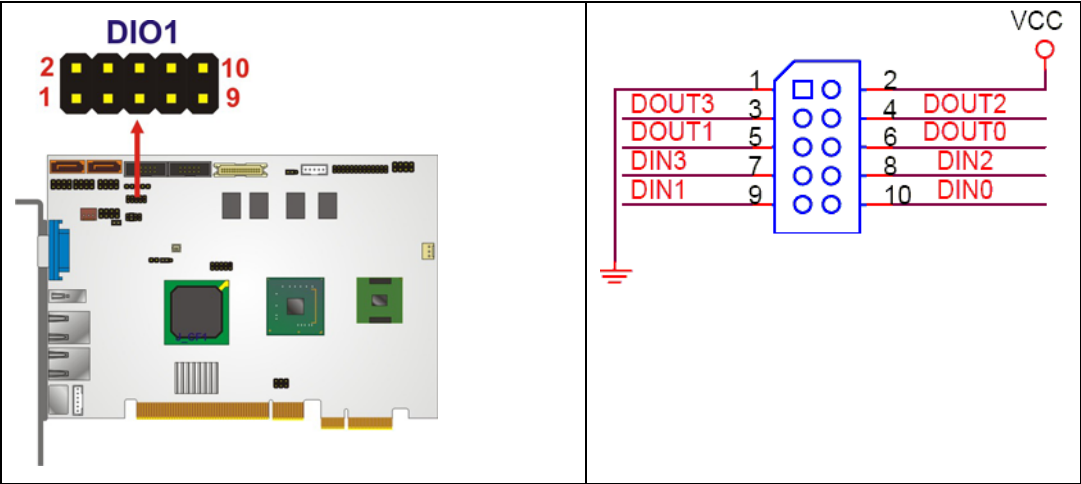
Figure 4-7: DIO Connector Connector Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	VCC
3	Output 3	4	Output 2
5	Output 1	6	Output 0
7	Input 3	8	Input 2
9	Input 1	10	Input 0

Table 4-7: DIO Connector Connector Pinouts

4.2.6 Fan Connector (+12V, 3-pin)

CN Label:　　CPU_FAN1

CN Type:　　3-pin header

CN Location:　See **Figure 4-8**

CN Pinouts:　See **Table 4-8**

The cooling fan connector provides a 12V, 500mA current to the cooling fan. The connector has a "rotation" pin to get rotation signals from fans and notify the system so the

system BIOS can recognize the fan speed. Please note that only specified fans can issue the rotation signals.
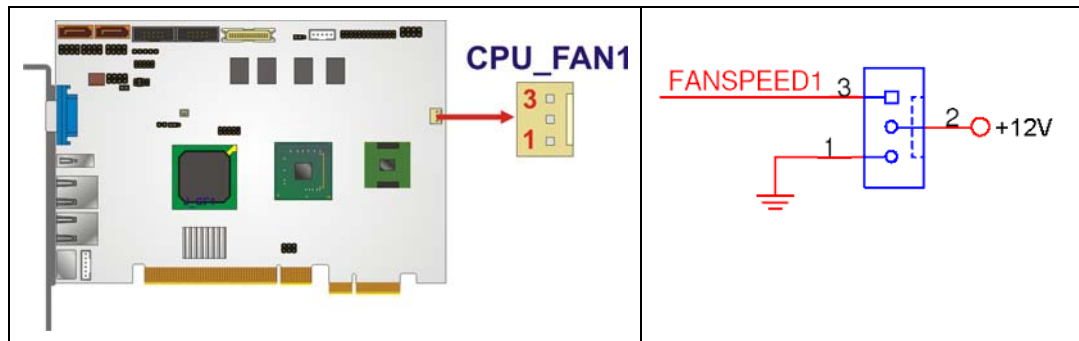
Figure 4-8: +12V Fan Connector Location

PIN NO.	DESCRIPTION
1	GND
2	+12V
3	Fan Speed Detect

Table 4-8: +12V Fan Connector Pinouts

4.2.7 Front Panel Connector (8-pin)

CN Label: F_PANEL1

CN Type: 8-pin header (2x4)

CN Location: See **Figure 4-9**

CN Pinouts: See **Table 4-9**

The front panel connector connects to external switches and indicators to monitor and controls the CPU card. These indicators and switches include:

- Power button
- Reset
- Power LED
- HDD LED
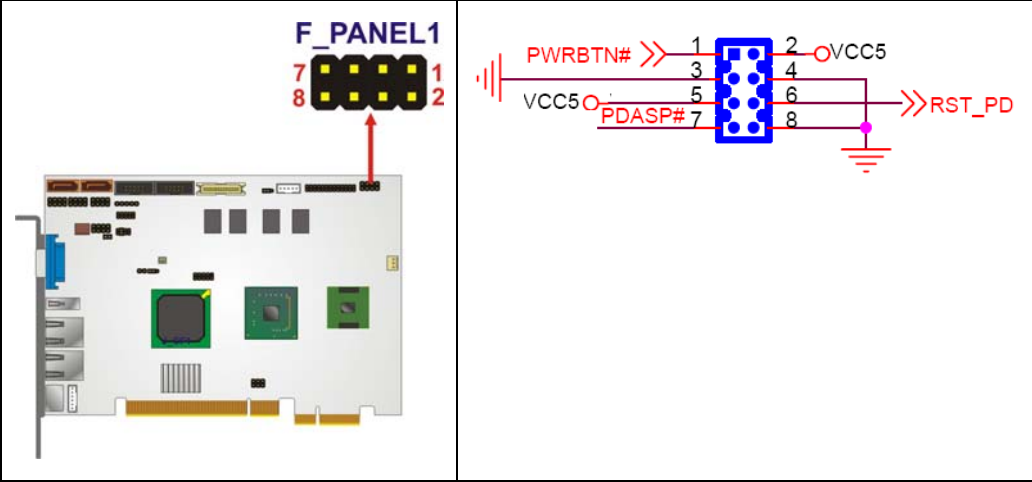
Figure 4-9: Front Panel Connector Pinout Locations (8-pin)

FUNCTION	PIN	DESCRIPTION	FUNCTION	PIN	DESCRIPTION
Power	1	PWR_BTN+	Power LED	2	PWR_LED+
Button	3	PWR_BTN-		4	PWR_LED-
HDD LED	5	HDD_LED+	Reset	6	RESET+
	7	HDD_LED-		8	RESET-

Table 4-9: Front Panel Connector Pinouts (8-pin)

4.2.8 Infrared Interface Connector

CN Label: IR1

CN Type: 5-pin header (1x5)

CN Location: See **Figure 4-10**

CN Pinouts: See **Table 4-10**

The infrared interface connector supports both Serial Infrared (SIR) and Amplitude Shift Key Infrared (ASKIR) interfaces.
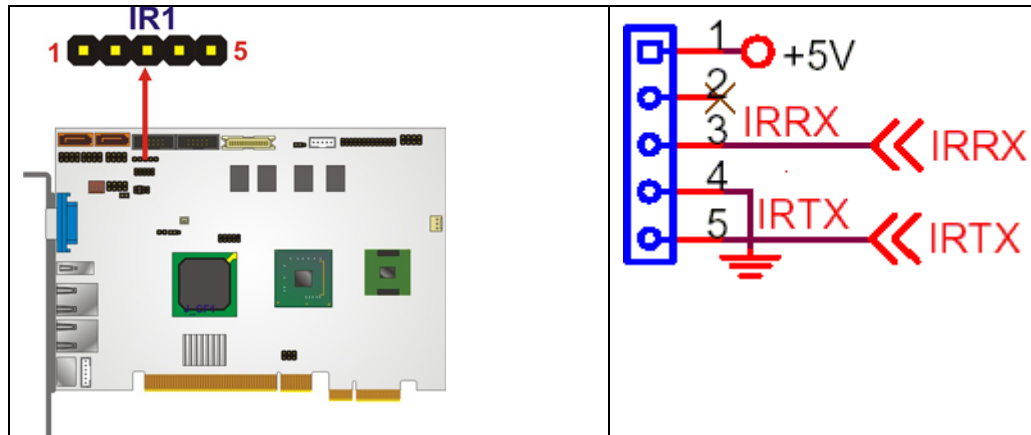
Figure 4-10: Infrared Connector Pinout Locations

PIN NO.	DESCRIPTION
1	VCC
2	NC
3	IR-RX
4	GND
5	IR-TX

Table 4-10: Infrared Connector Pinouts

4.2.9 Keyboard/Mouse Connector

CN Label: KB_MS1

CN Type: 6-pin header (1x6)

CN Location: See **Figure 4-11**

CN Pinouts: See **Table 4-11**

The keyboard and mouse connector can be connected to a standard PS/2 cable or PS/2 Y-cable to add keyboard and mouse functionality to the system.
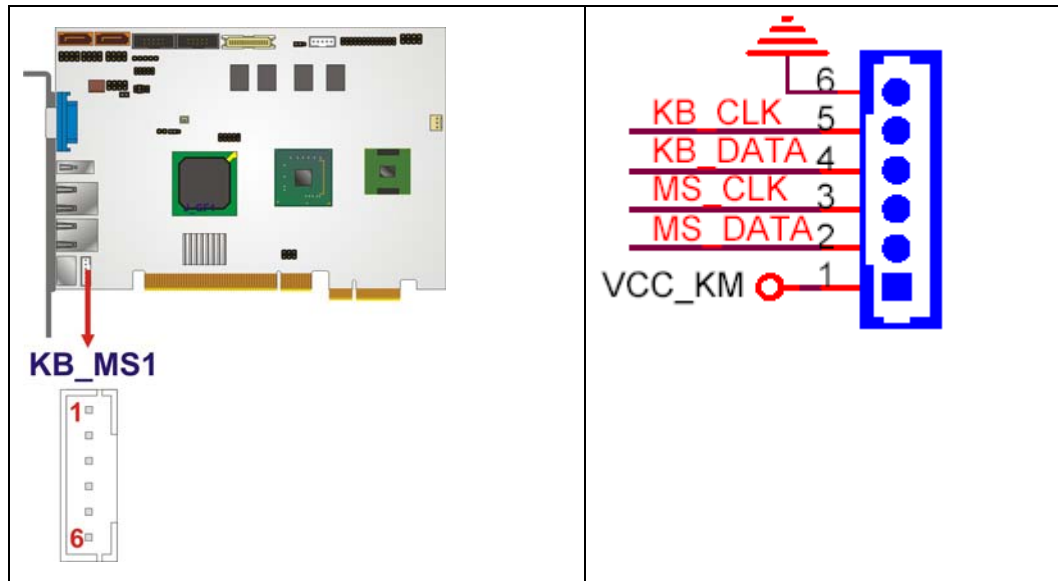
Figure 4-11: Keyboard/Mouse Connector Location

PIN NO.	DESCRIPTION
1	VCC5_KBMS
2	MS DATA
3	MS CLK
4	KB DATA
5	KB CLK
6	GROUND

Table 4-11: Keyboard/Mouse Connector Pinouts

4.2.10 LVDS LCD Connector

CN Label: LVDS1

CN Type: 30-pin crimp (3x10)

CN Location: See **Figure 4-12**

CN Pinouts: See **Table 4-12**

The 30-pin LVDS LCD connectors can be connected to single channel or dual channel, 24-bit or 36-bit LVDS panel.
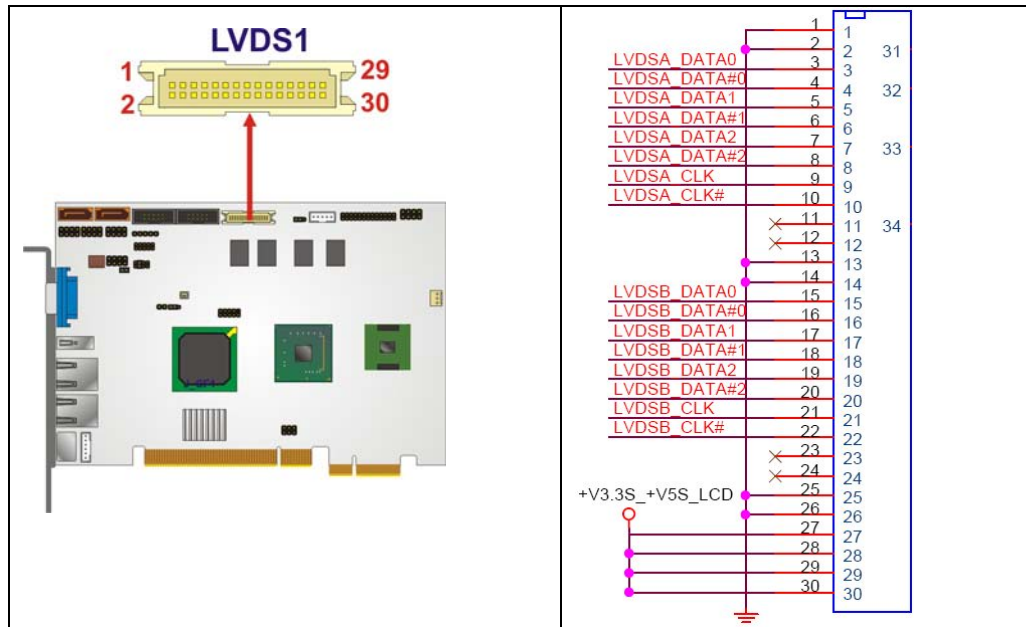
Figure 4-12: LVDS LCD Connector Pinout Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	GND
3	A_Y0	4	A_Y0#
5	A_Y1	6	A_Y1#
7	A_Y2	8	A_Y2#
9	A_CK	10	A_CK#
11	NC	12	NC
13	GND	14	GND
15	B_Y0	16	B_Y0#
17	B_Y1	18	B_Y1#
19	B_Y2	20	B_Y2#
21	B_CK	22	B_CK#
23	NC	24	NC
25	GND	26	GND
27	VCC/VCC3	28	VCC/VCC3
29	VCC/VCC3	30	VCC/VCC3

Table 4-12: LVDS LCD Port Connector Pinouts

4.2.11 Parallel Port Connector

CN Label: LPT1

CN Type: 26-pin header

CN Location: See **Figure 4-13**

CN Pinouts: See **Table 4-13**

The 26-pin parallel port connector connects to a parallel port connector interface or some other parallel port device such as a printer.
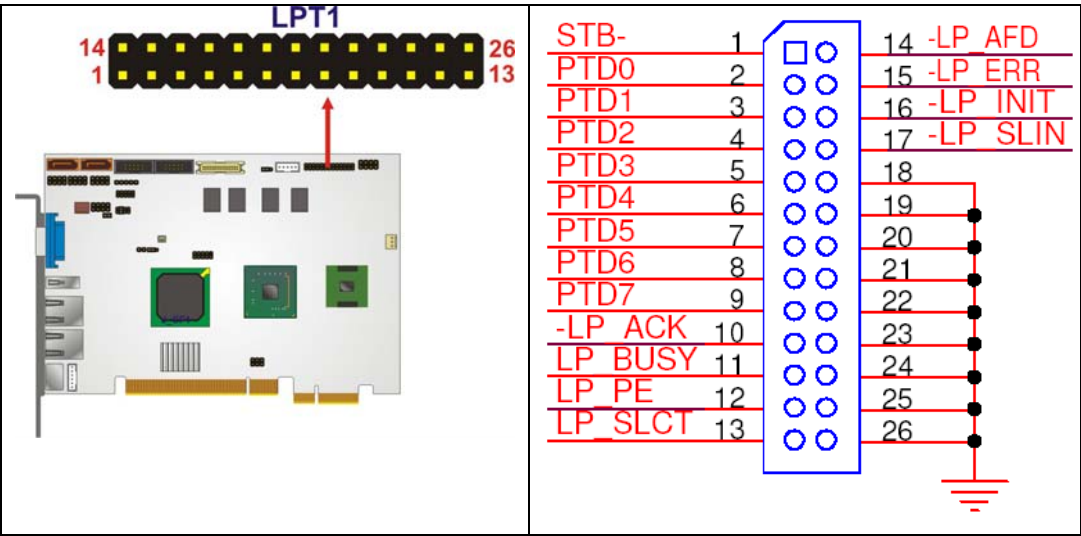
Figure 4-13: Parallel Port Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	STROBE#	2	DATA 0
3	DATA 1	4	DATA 2
5	DATA 3	6	DATA 4
7	DATA 5	8	DATA 6
9	DATA 7	10	ACKNOWLEDGE
11	BUSY	12	PAPER EMPTY
13	PRINTER SELECT	14	AUTO FORM FEED #
15	ERROR#	16	INITIALIZE

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
17	PRINTER SELECT LN#	18	GROUND
19	GROUND	20	GROUND
21	GROUND	22	GROUND
23	GROUND	24	GROUND
25	GROUND	26	NC

Table 4-13: Parallel Port Connector Pinouts

4.2.12 SATA Drive Connectors

CN Label: **S_ATA1** and **S_ATA2**

CN Type: 7-pin SATA drive connectors

CN Location: See **Figure 4-14**

CN Pinouts: See **Table 4-14**

The two SATA drive connectors are each connected to a first generation SATA drive. First generation SATA drives transfer data at speeds as high as 150 Mb/s. The SATA drives can be configured in a RAID configuration.
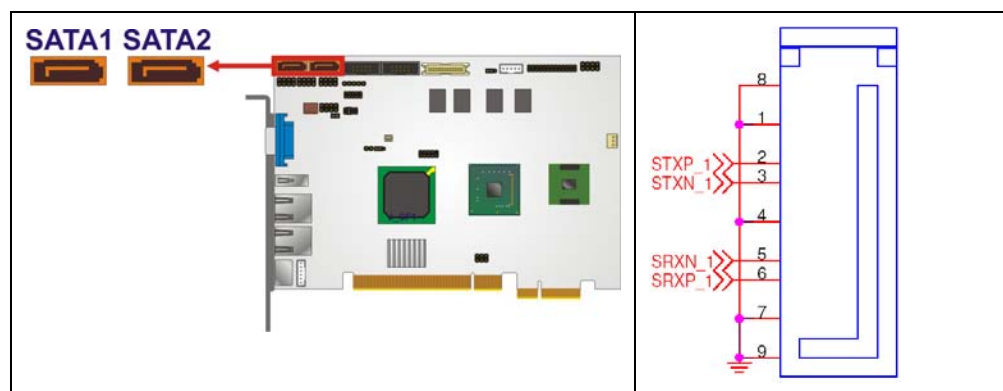
Figure 4-14: SATA Drive Connector Locations

PIN NO.	DESCRIPTION
1	GND
2	TX+

3	TX-
4	GND
5	RX-
6	RX+
7	GND

Table 4-14: SATA Drive Connector Pinouts

4.2.13 Serial Port Connectors (COM 1 and COM 2)

CN Label: **COM1** and **COM2**

CN Type: 10-pin header (2x5)

CN Location: See **Figure 4-15**

CN Pinouts: See **Table 4-15**

The 10-pin serial port connector provides a second RS-232 serial communications channel. The COM serial port connectors can be connected to external RS-232 serial port devices.
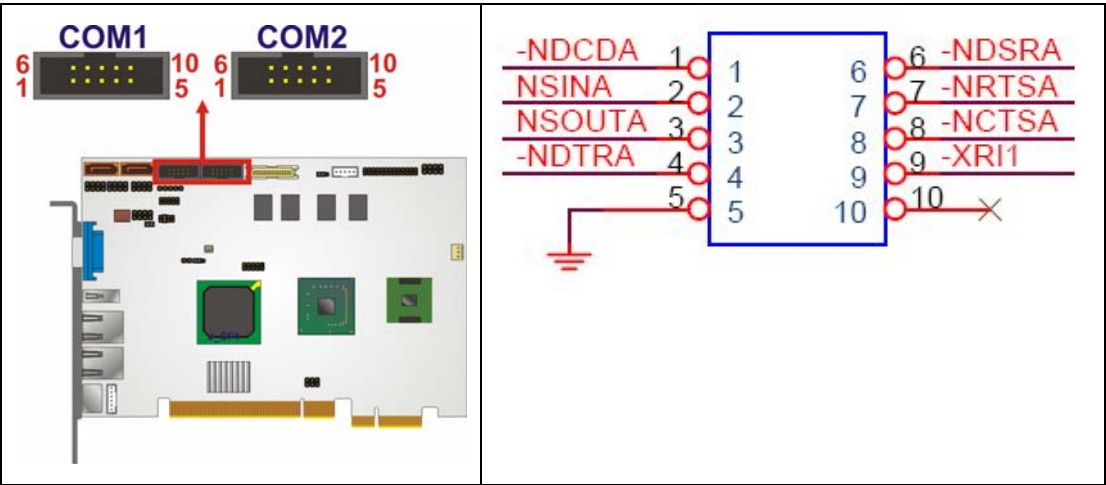
Figure 4-15: COM Connector Pinout Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	Data Carrier Direct (DCD)	2	Receive Data (SIN)
3	Transmit Data (SOUT)	4	Data Terminal Ready (DTR)
5	Ground (GND)	6	DATA Set Ready (DSR)
7	Request To Send (RTS)	8	Clear To Send (CTS)
9	Ring Indicator (XRI)	10	N/C

Table 4-15: COM Connector Pinouts

4.2.14 SDVO Connector

CN Label: SDVO1

CN Type: 47-pin connector (1x47)

CN Location: See **Figure 4-12**

CN Pinouts: See **Table 4-12**

The 47-pin SDVO (Serial Digital Video Out) connector supports additional video signaling interfaces.
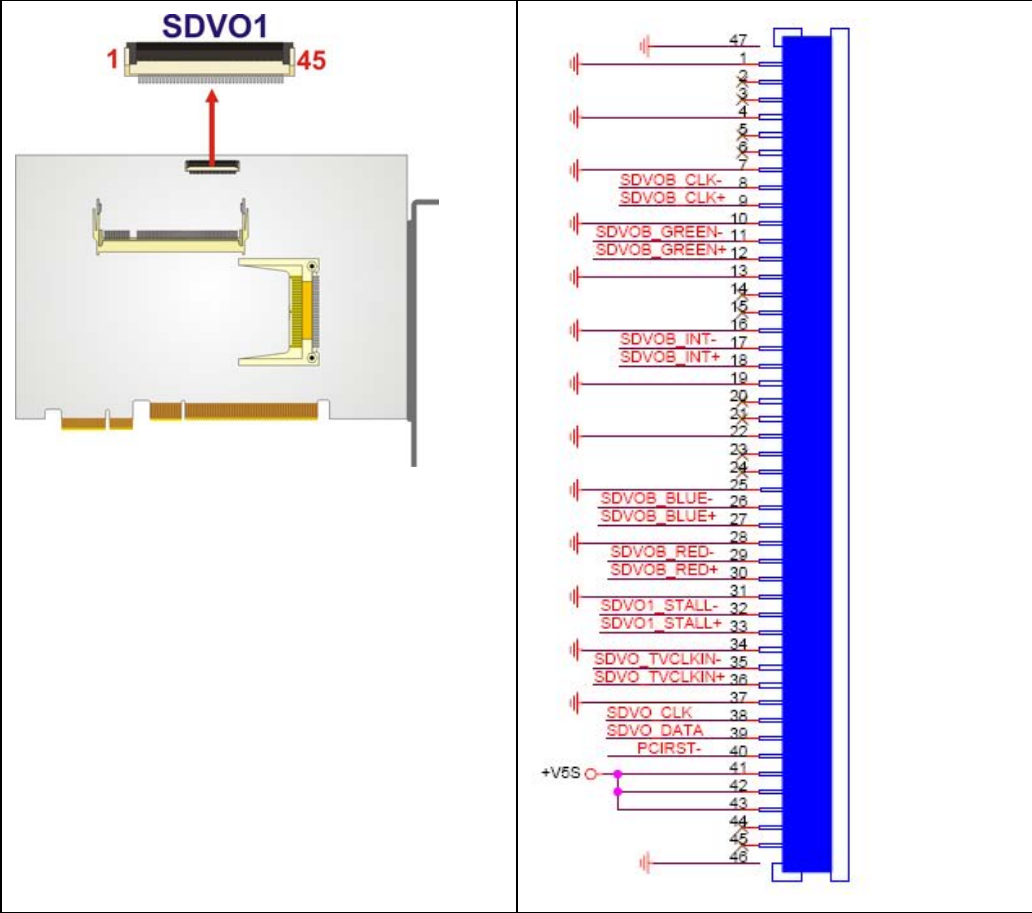
Figure 4-16: SDVO Connector Pinout Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GROUND	25	GROUND
2	NC	26	SDVOB_BLUE-
3	NC	27	SDVOB_BLUE+
4	GROUND	28	GROUND
5	NC	29	SDVOB_RED-
6	NC	30	SDVOB_RED+
7	GROUND	31	GROUND
8	SDVOB_CLK-	32	SDVO1_STALL-
9	SDVOB_ CLK+	33	SDVO1_STALL+
10	GROUND	34	GROUND
11	SDVOB_GREEN-	35	SDVO_TVCLKIN-

12	SDVOB_GREEN+	36	SDVO_TVCLKIN+
13	GROUND	37	GROUND
14	NC	38	SDVO_CLK
15	NC	39	SDVO_DATA
16	GROUND	40	PCIRST
17	SDVOB_INT+	41	+5VS
18	SDVOB_INT+	42	+5VS
19	GROUND	43	+5VS
20	NC	44	NC
21	NC	45	NC
22	GROUND	46	GROUND
23	NC	47	GROUND
24	NC		

Table 4-16: SDVO Connector Pinouts

4.2.15 TV Out Connector

CN Label:	TV1
CN Type:	6-pin header (2x3)
CN Location:	See Figure 4-17
CN Pinouts:	See Table 4-17

The 2x3 pin TV out connector connects to a TV output by using an S-Video or RCA connector. The TV out connector makes displaying media data on a television easier.
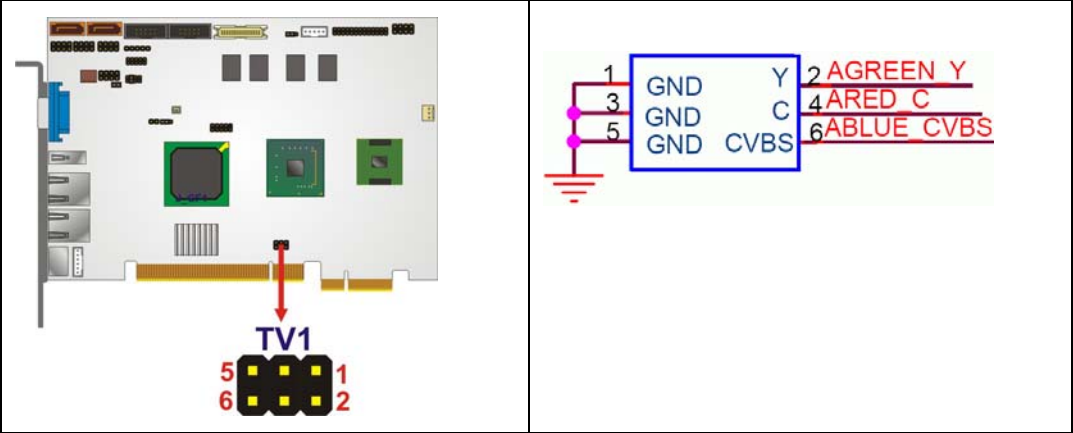
Figure 4-17: TV Connector Pinout Locations

S-Video Connector			
PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	AGREEN_Y
3	GND	4	ARED_C
RCA Connector (only video signal)			
5	GND	6	ABLUE_CVBS

Table 4-17: TV Port Connector Pinouts

4.2.16 USB Connectors (Internal)

CN Label: **USB1**, **USB2** and **USB3**

CN Type: 8-pin header (2x4)

CN Location: See **Figure 4-18**

CN Pinouts: See **Table 4-18**

The 2x4 USB pin connectors each provide connectivity to two USB 1.1 or two USB 2.0 ports. Each USB connector can support two USB devices. Additional external USB ports are found on the rear panel. The USB ports are used for I/O bus expansion.
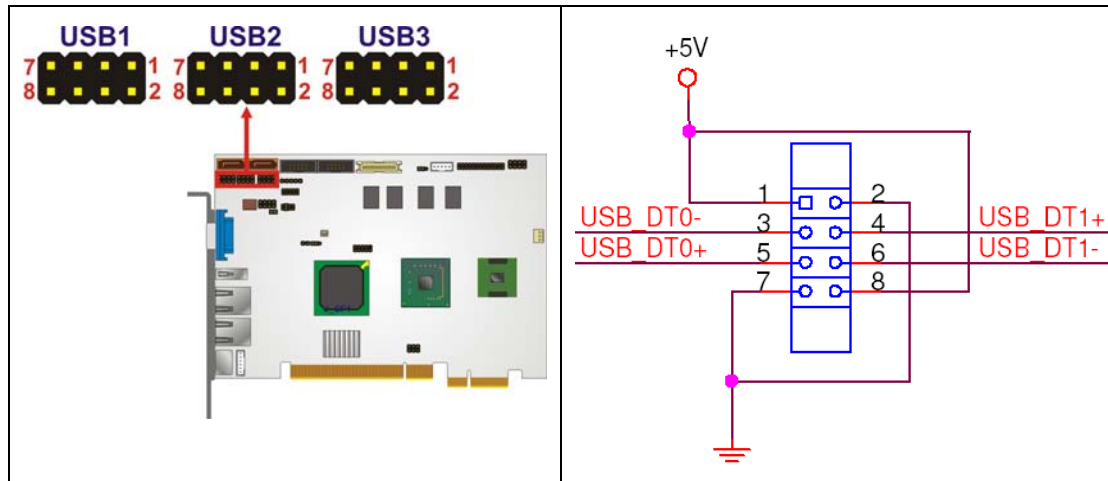
Figure 4-18: USB Connector Pinout Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	VCC	2	GND
3	DATA-	4	DATA-
5	DATA+	6	DATA+
7	GND	8	VCC

Table 4-18: USB Port Connector Pinouts

4.3 External Peripheral Interface Connector Panel

Figure 4-19 shows the PICOe-945GSE external peripheral interface connector (EPIC) panel. The PICOe-945GSE EPIC panel consists of the following:

- 2 x RJ-45 LAN connectors
- 1 x PS/2 connector
- 1 x USB connector
- 1 x VGA connector
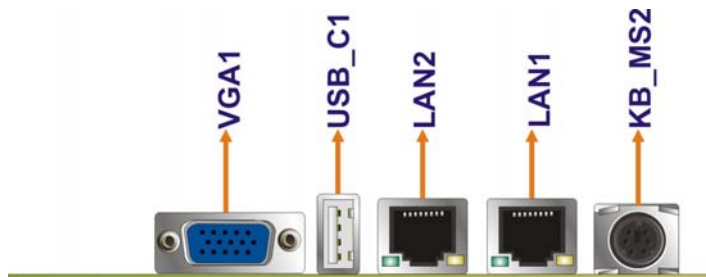
Figure 4-19: PICOe-945GSE External Peripheral Interface Connector

4.3.1 Keyboard/Mouse Connector

CN Label: **KB_MS2**

CN Type: PS/2

CN Location: See **Figure 4-19**

CN Pinouts: See **Figure 4-20, Table 4-19**

The PICOe-945GSE keyboard and mouse connector is a standard PS/2 connector.
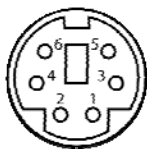
Figure 4-20: PS/2 Pinout and Configuration

PIN	DESCRIPTION
1	KB DATA
2	MS DATA
3	GND
4	VCC
5	KB CLOCK
6	MS CLOCK

Table 4-19: Keyboard Connector Pinouts

4.3.2 LAN Connectors

CN Label: **LAN1** and **LAN2**

CN Type: RJ-45

CN Location: See **Figure 4-19**

CN Pinouts: See **Table 4-20**

The PICOe-945GSE is equipped with two built-in RJ-45 Ethernet controllers. The controllers can connect to the LAN through two RJ-45 LAN connectors. There are two LEDs on the connector indicating the status of LAN. The pin assignments are listed in the following table:

PIN	DESCRIPTION	PIN	DESCRIPTION
1	MDIA3-	5	MDIA1+
2	MDIA3+	6	MDIA2+
3	MDIA2-	7	MDIA0-
4	MDIA1-	8	MDIA0+

Table 4-20: LAN Pinouts
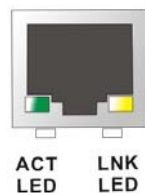
Figure 4-21: RJ-45 Ethernet Connector

The RJ-45 Ethernet connector has two status LEDs, one green and one yellow. The green LED indicates activity on the port and the yellow LED indicates the port is linked. See **Table 4-21**.

STATUS	DESCRIPTION	STATUS	DESCRIPTION
GREEN	Activity	YELLOW	Linked

Table 4-21: RJ-45 Ethernet Connector LEDs

4.3.3 USB Connectors

CN Label: USB_C1

CN Type: USB port

CN Location: See **Figure 4-19**

CN Pinouts: See **Table 4-22**

The PICOe-945GSE has two external USB 2.0 ports. The ports connect to both USB 2.0 and USB 1.1 devices.

PIN NO.	DESCRIPTION
1	VCC
2	DATA-
3	DATA+
4	GND

Table 4-22: USB Port Pinouts

4.3.4 VGA Connector

CN Label: VGA1

CN Type: 15-pin Female

CN Location: See **Figure 4-19**

CN Pinouts: See **Figure 4-22** and **Table 4-23**

The PICOe-945GSE has a single 15-pin female connector for connectivity to standard display devices.
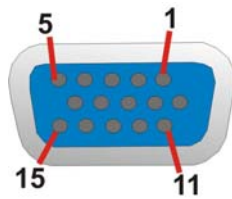
Figure 4-22: VGA Connector

PIN	DESCRIPTION	PIN	DESCRIPTION
1	RED	2	GREEN
3	BLUE	4	NC
5	GND	6	CRT_PLUG-
7	GND	8	GND
9	VCC	10	GND
11	NC	12	DDC DAT
13	HSYNC	14	VSYNC
15	DDCCLK		

Table 4-23: VGA Connector Pinouts

Chapter

5

Installation

5.1 Anti-static Precautions

WARNING:

Failure to take ESD precautions during the installation of the PICOe-945GSE may result in permanent damage to the PICOe-945GSE and severe injury to the user.

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the PICOe-945GSE. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the PICOe-945GSE, or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- *Wear an anti-static wristband*: - Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- *Self-grounding*:- Before handling the board touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- *Use an anti-static pad*: When configuring the PICOe-945GSE, place it on an antic-static pad. This reduces the possibility of ESD damaging the PICOe-945GSE.
- *Only handle the edges of the PCB*:-: When handling the PCB, hold the PCB by the edges.

5.2 Installation Considerations

![NOTE icon] **NOTE:**

The following installation notices and installation considerations should be read and understood before the PICOe-945GSE is installed. All installation notices pertaining to the installation of the PICOe-945GSE should be strictly adhered to. Failing to adhere to these precautions may lead to severe damage of the PICOe-945GSE and injury to the person installing the CPU card.

5.2.1 Installation Notices

![WARNING icon] **WARNING:**

The installation instructions described in this manual should be carefully followed in order to prevent damage to the PICOe-945GSE, PICOe-945GSE components and injury to the user.

Before and during the installation please **DO** the following:

■ Read the user manual:

○ The user manual provides a complete description of the PICOe-945GSE installation instructions and configuration options.

■ Wear an electrostatic discharge cuff (ESD):

○ Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the body and helps prevent ESD damage.

■ Place the PICOe-945GSE on an antistatic pad:

○ When installing or configuring the CPU card, place it on an antistatic pad. This helps to prevent potential ESD damage.

■ Turn all power to the PICOe-945GSE off:

o   When working with the PICOe-945GSE, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

Before and during the installation of the PICOe-945GSE **DO NOT:**

- Remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- Use the product before verifying all the cables and power connectors are properly connected.
- Allow screws to come in contact with the PCB circuit, connector pins, or its components.

5.2.2 Installation Checklist

The following checklist is provided to ensure the PICOe-945GSE is properly installed.

- All the items in the packing list are present
- A compatible memory module is properly inserted into the slot
- The CF Type I or CF Type II card is properly installed into the CF socket
- The jumpers have been properly configured
- The PICOe-945GSE is inserted into a chassis with adequate ventilation
- The correct power supply is being used
- The following devices are properly connected

  o   Primary and secondary IDE device

  o   SATA drives

  o   Power supply

  o   USB cable

  o   Serial port cable

- The following external peripheral devices are properly connected to the chassis:

  o   VGA screen

  o   Keyboard

  o   Mouse

  o   RS-232 serial communications device

  o   USB devices

5.3 Unpacking

When the PICOe-945GSE is unpacked, please check all the unpacking list items listed in Chapter 3 are indeed present. If any of the unpacking list items are not available please contact the PICOe-945GSE vendor reseller/vendor where the PICOe-945GSE was purchased or contact an IEI sales representative.

5.4 SO-DIMM and CF Card Installation

5.4.1 SO-DIMM Installation

![WARNING icon]

WARNING:

Using incorrectly specified SO-DIMM may cause permanently damage the PICOe-945GSE. Please make sure the purchased SO-DIMM complies with the memory specifications of the PICOe-945GSE. SO-DIMM specifications compliant with the PICOe-945GSE are listed in **Chapter 2**.

To install a SO-DIMM into a SO-DIMM socket, please follow the steps below and refer to **Figure 5-1**.
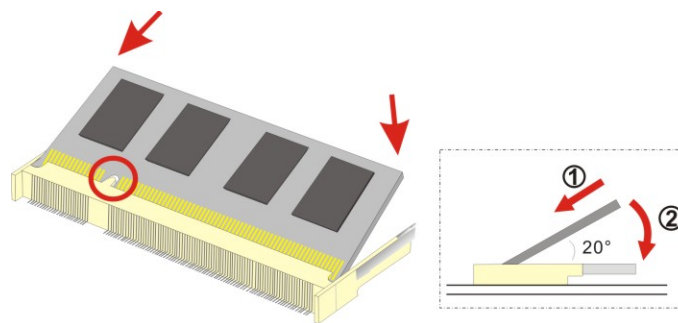
Figure 5-1: SO-DIMM Installation

Step 1: **Locate the SO-DIMM socket**. Place the PICOe-945GSE on an anti-static pad with the solder side facing up.

Step 2: **Align the SO-DIMM with the socket**. The SO-DIMM must be oriented in such a way that the notch in the middle of the SO-DIMM must be aligned with the plastic bridge in the socket.

Step 3: **Insert the SO-DIMM**. Push the SO-DIMM chip into the socket at an angle. (See **Figure 5-1**)

Step 4: **Open the SO-DIMM socket arms**. Gently pull the arms of the SO-DIMM socket out and push the rear of the SO-DIMM down. (See **Figure 5-1**)

Step 5: **Secure the SO-DIMM**. Release the arms on the SO-DIMM socket. They clip into place and secure the SO-DIMM in the socket.

5.4.2 CF Card Installation

![NOTE icon] **NOTE:**

The PICOe-945GSE can support both CF Type I cards and CF Type II cards. For the complete specifications of the supported CF cards please refer to **Chapter 2**.

To install the a CF card (Type I or Type II) onto the PICOe-945GSE, please follow the steps below:

Step 1: **Locate the CF card socket**. Place the PICOe-945GSE on an anti-static pad with the solder side facing up. Locate the CF card.

Step 2: **Align the CF card**. Make sure the CF card is properly aligned with the CF socket.

Step 3: **Insert the CF card**. Gently insert the CF card into the socket making sure the socket pins are properly inserted into the socket. See **Figure 5-2**.
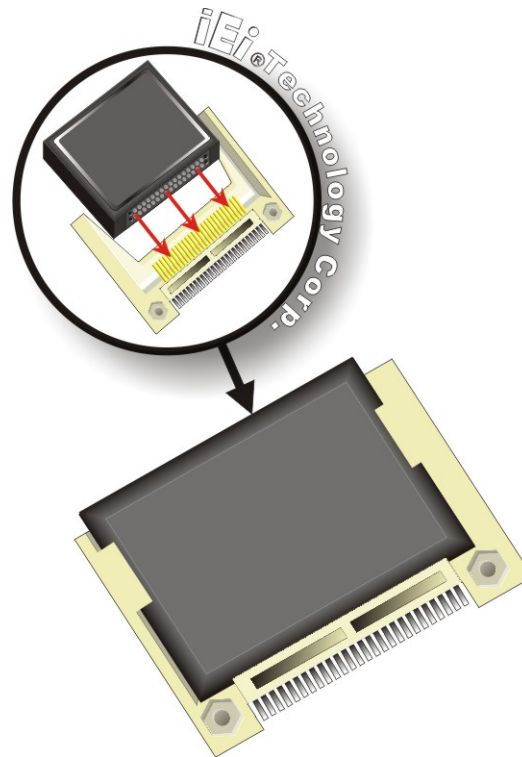
Figure 5-2: CF Card Installation

5.5 Jumper Settings

 NOTE:

A jumper is a metal bridge used to close an electrical circuit. It consists of two or three metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To CLOSE/SHORT a jumper means connecting the pins of the jumper with the plastic clip and to OPEN a jumper means removing the plastic clip from a jumper.
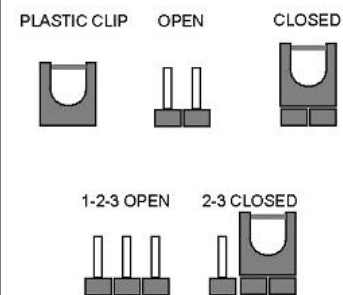
Figure 5-3: Jumper Locations

Before the PICOe-945GSE is installed in the system, the jumpers must be set in accordance with the desired configuration. The jumpers on the PICOe-945GSE are listed in **Table 5-1**.

Description	Label	Type
AT Power Mode Setting	ATXCTL1	2-pin header
CF Card Setting	JCF1	2-pin header
Clear CMOS	J_CMOS1	3-pin header
LVDS Panel Resolution	J_LCD_TYPE1	8-pin header
LVDS Voltage Select	J_VLVDS1	3-pin header
PCIe Status Select	J_PCIE1	2-pin header

Table 5-1: Jumpers

5.5.1 AT Power Select Jumper Settings

 NOTE:

The AT Power Select Jumper is the same as the ATX Enable connector.

Jumper Label: **ATXCTl1**

Jumper Type: 3-pin wafer

Jumper Settings: See **Table 5-2**

Jumper Location: See **Figure 5-4**

The AT Power Select jumper specifies the systems power mode as AT or ATX. Use a jumper cap to short pin 1 - pin 2 on the ATXCTL1 connector to enable the AT Power mode on the system. In the ATX mode use the PS_ON- and 5VSB cable. AT Power Select jumper settings are shown in **Table 5-2**.

AT Power Select	Description	
Short 1 – 2	Use AT power	Default
Open	Use ATX power	

Table 5-2: AT Power Select Jumper Settings

The location of the AT Power Select jumper is shown in **Figure 5-4** below.
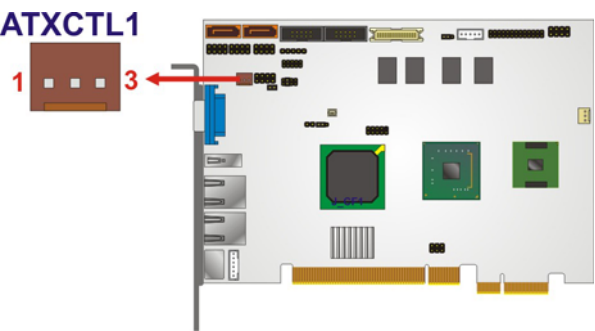
Figure 5-4: AT Power Select Jumper Location

5.5.2 CF Card Setup

Jumper Label: JCF1

Jumper Type: 2-pin header

Jumper Settings: See **Table 5-3**

Jumper Location: See **Figure 5-5**

The CF Card Setup jumper sets the CF Type I card or CF Type II cards as either the slave device or the master device. CF Card Setup jumper settings are shown in **Table 5-3**.

CF Card Setup	Description	
Open	Slave	Default
Closed	Master	

Table 5-3: CF Card Setup Jumper Settings

The CF Card Setup jumper location is shown in **Figure 5-5**.
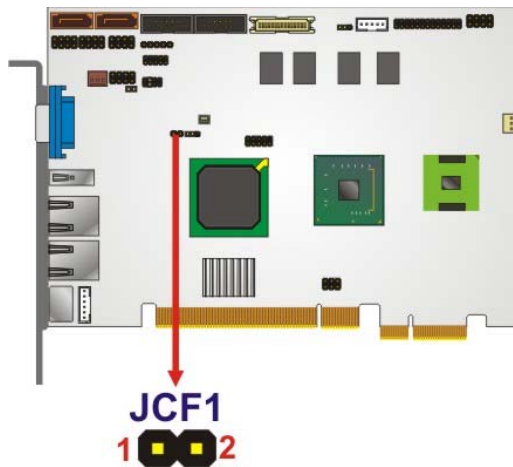
Figure 5-5: CF Card Setup Jumper Location

5.5.3 Clear CMOS Jumper

Jumper Label:	J_CMOS1
Jumper Type:	3-pin header
Jumper Settings:	See **Table 5-4**
Jumper Location:	See **Figure 5-6**

If the PICOe-945GSE fails to boot due to improper BIOS settings, the clear CMOS jumper clears the CMOS data and resets the system BIOS information. To do this, use the jumper cap to close pins 2 and 3 for a few seconds then reinstall the jumper clip back to pins 1 and 2.

If the "CMOS Settings Wrong" message is displayed during the boot up process, the fault may be corrected by pressing the F1 to enter the CMOS Setup menu.   Do one of the following:

- Enter the correct CMOS setting
- Load Optimal Defaults
- Load Failsafe Defaults.

After having done one of the above, save the changes and exit the CMOS Setup menu.

The clear CMOS jumper settings are shown in **Table 5-4**.

Clear CMOS	Description	
Short 1 - 2	Keep CMOS Setup	Default
Short 2 - 3	Clear CMOS Setup	

Table 5-4: Clear CMOS Jumper Settings

The location of the clear CMOS jumper is shown in **Figure 5-6** below.
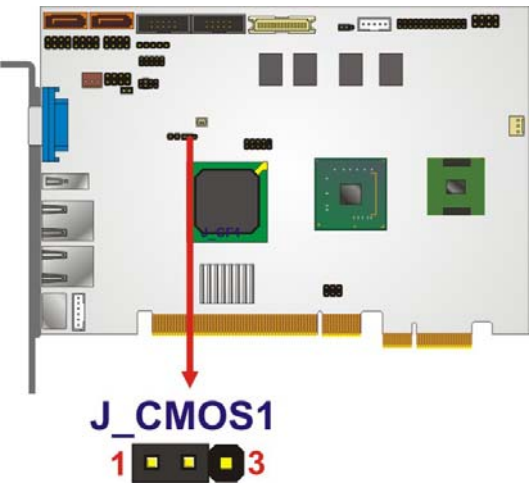
Figure 5-6: Clear CMOS Jumper

5.5.4 LVDS Panel Resolution Jumper

Jumper Label: J_LCD_TYPE1

Jumper Type: 8-pin header

Jumper Settings: See **Table 5-5**

Jumper Location: See **Figure 5-7**

The LVDS Panel Resolution jumper allows the resolution of the LVDS screens connected to the LVDS1 connector to be configured. The LVDS Panel Resolution jumper settings are shown in **Table 5-5**.

J_LCD_TYPE1	Description	
Open	640 x 480 (18-bit)	
Short 1-2	800 x 480 (18-bit)	
Short 3-4	800 x 600 (18-bit)	Default
Short 1-2, 3-4	1024 X 768 (18-bit)	
Short 5-6	1280X1024 (36-bit)	
Short 1-2, 5-6	1400 X 1050 (36-bit)	
Short 3-4, 5-6	1400 x 900 (36-bit)	
Short 1-2, 3-4, 5-6	1600 x 1200 (36-bit)	

Table 5-5: LVDS Panel Resolution Jumper Settings

The LVDS Panel Resolution jumper location is shown in **Figure 5-7**.
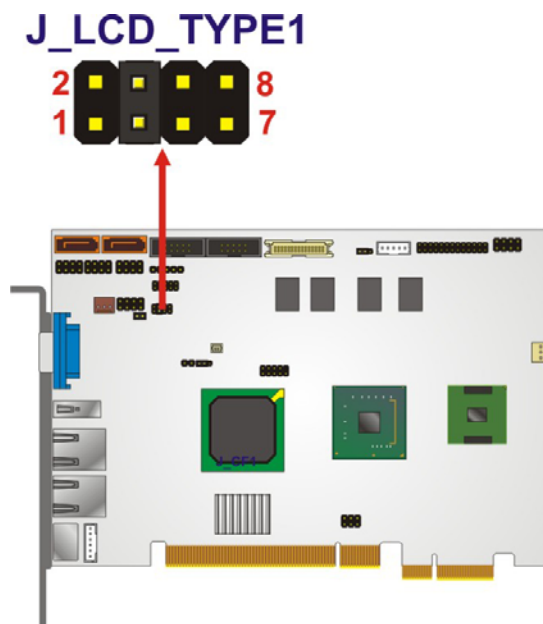
Figure 5-7: LVDS Panel Resolution Jumper Pinout Locations

5.5.5 LVDS Voltage Selection

> ⚠ **WARNING:**
>
> Permanent damage to the screen and PICOe-945GSE may occur if the wrong voltage is selected with this jumper. Please refer to the user guide that cam with the monitor to select the correct voltage.

Jumper Label:	**J_VLVDS1**
Jumper Type:	3-pin header
Jumper Settings:	See **Table 5-6**
Jumper Location:	See **Figure 5-8**

The **LVDS Voltage Selection** jumpers allow the LVDS screen voltages to be set. J_VLVDS1 sets the voltage connected to LVDS1. The **LVDS Voltage Selection** jumper settings are shown in **Table 5-6**.

LCD Voltage Select	Description	
Short 1-2	+3.3V LVDS	Default
Short 2-3	+5V LVDS	

Table 5-6: LVDS Voltage Selection Jumper Settings

The LVDS Voltage Selection jumper location is shown in **Figure 5-8**.
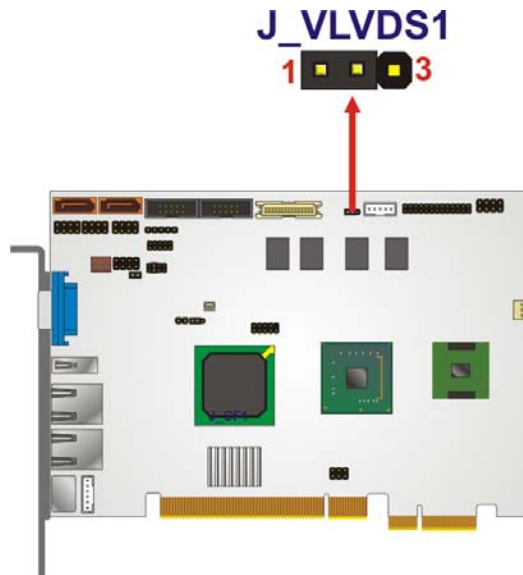
Figure 5-8: LVDS Voltage Selection Jumper Pinout Locations

5.5.6 PCIe Status Select

Jumper Label:	**J_PCIE1**
Jumper Type:	2-pin header
Jumper Settings:	See **Table 5-7**
Jumper Location:	See **Figure 5-9**

The **PCIe Status Select** jumper allows the PCIe status to be configured. The **PCIe Status Select** jumper settings are shown in **Table 5-6**.

PCIe Status Select	Description	
Open	One PCIe x4	
Short	Four PCIe x1	Default

Table 5-7: PCIe Status Select Jumper Settings

The PCIe Status Select jumper location is shown in **Figure 5-8**.
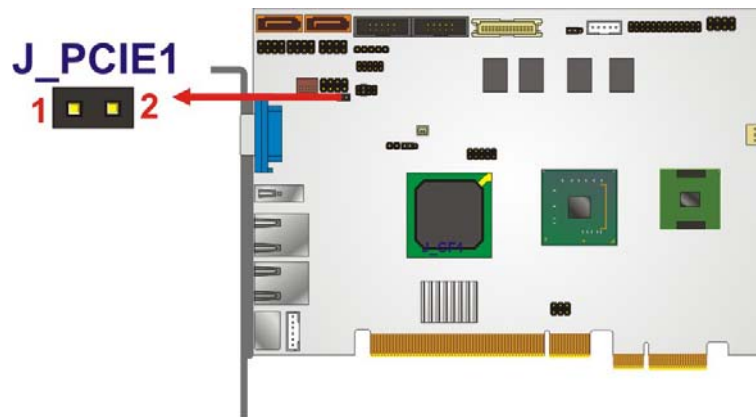
Figure 5-9: PCIe Status Select Jumper Pinout Locations

5.6 Chassis Installation

5.6.1 Airflow

> ⚠️ **WARNING:**
>
> Airflow is critical to the cooling of the CPU and other onboard components. The chassis in which the PICOe-945GSE must have air vents to allow cool air to move into the system and hot air to move out.

The PICOe-945GSE must be installed in a chassis with ventilation holes on the sides allowing airflow to travel through the heat sink surface. In a system with an individual power supply unit, the cooling fan of a power supply can also help generate airflow through the board surface.

5.6.2 Backplane Installation

Before the PICOe-945GSE can be installed into the chassis, a backplane must first be installed. Please refer to the installation instructions that came with the backplane and the chassis to see how to install the backplane into the chassis.

![IEI Integration Corp.]

![NOTE icon] **NOTE:**

> IEI has a wide range of backplanes available. Please contact your
> PICOe-945GSE vendor, reseller or an IEI sales representative at
> sales@iei.com.tw or visit the IEI website (http://www.ieiworld.com.tw)
> to find out more about the available chassis.

5.6.3 CPU Card Installation

To install the PICOe-945GSE CPU card onto the backplane, carefully align the CPU card interface connectors with the corresponding socket on the backplane. To do this, please refer to the reference material that came with the backplane. Next, secure the CPU card to the chassis. To do this, please refer to the reference material that came with the chassis.

5.7 Internal Peripheral Device Connections

5.7.1 Peripheral Device Cables

The cables listed in **Table 5-8** are shipped with the PICOe-945GSE.

Quantity	Type
1	Keyboard and Mouse cable
2	SATA drive cable
1	Dual port USB cable
1	Dual RS-232 cable

Table 5-8: IEI Provided Cables

Some optional items that can be purchased separately and installed on the PICOe-945GSE include:

- SATA power cable
- Parallel port cable

- HDTV out cable
- 5.1 channel audio kit
- 7.1 channel audio kit

5.7.2 5.1 Channel Audio Kit Installation

 NOTE:

This is an optional item that must be ordered separately. For further information please contact the nearest PICOe-945GSE distributor, reseller or vendor or contact an iEi sales representative directly. Send any queries to sales@iei.com.tw.

The optional 5.1 channel audio kit connects to the 10-pin audio connector on the PICOe-945GSE. The audio kit consists of three audio jacks. One audio jack, Mic In, connects to a microphone. The remaining two audio jacks, Line-In and Line-Out, connect to two speakers. To install the audio kit, please refer to the steps below:

Step 1: **Connect the audio kit cable.** The audio kit is shipped with a cable that connects the audio kit to the PICOe-945GSE. Connect the cable to the connector on the back of the audio kit. Make sure the pins are properly aligned (i.e. pin 1 connects to pin 1).

Step 2: **Locate the audio connector**. The location of the 10-pin audio connector is shown in **Chapter 3**.

Step 3: **Align pin 1**. Align pin 1 on the on-board connector with pin 1 on the audio kit cable connector. Pin 1 on the audio kit cable connector is indicated with a white dot. See **Figure 5-10**.
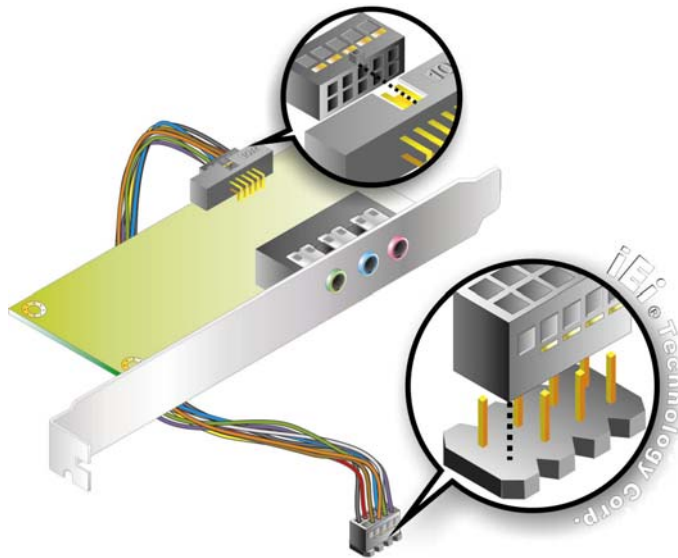
Figure 5-10: 5.1 Channel Audio Kit

Step 4: **Mount the audio kit onto the chassis**. Once the audio kit is connected to the PICOe-945GSE, secure the audio kit bracket to the system chassis.

Step 5: **Connect the audio devices**. Connect one speaker to the line-in audio jack, one speaker to the line-out audio jack and a microphone to the mic-in audio jack.

Step 6: **Install the driver**. If the 5.1 channel audio kit is used, the ALC655 Realtek codec driver must be installed. Refer to **Chapter 7** for driver installation instructions.

5.7.3 7.1 Channel Audio Kit Installation

![NOTE icon] **NOTE:**

This is an optional item that must be ordered separately. For further information please contact the nearest PICOe-945GSE distributor, reseller or vendor or contact an iEi sales representative directly. Send any queries to sales@iei.com.tw.

The optional 7.1 channel audio kit connects to the 10-pin audio connector on the PICOe-945GSE. The audio kit consists of five audio jacks. One audio jack, Mic In, connects to a microphone. The remaining four audio jacks, Line-In, Front-Out, Rear-Out, and Center Subwoofer, connect to speakers. To install the audio kit, please refer to the steps below:

Step 1: **Connect the audio kit cable.** The audio kit is shipped with a cable that connects the audio kit to the PICOe-945GSE. Connect the cable to the connector on the back of the audio kit. Make sure the pins are properly aligned (i.e. pin 1 connects to pin 1).

Step 2: **Locate the audio connector**. The location of the 10-pin audio connector is shown in **Chapter 3**.

Step 3: **Align pin 1**. Align pin 1 on the on-board connector with pin 1 on the audio kit cable connector. Pin 1 on the audio kit cable connector is indicated with a white dot. See **Figure 5-11**.
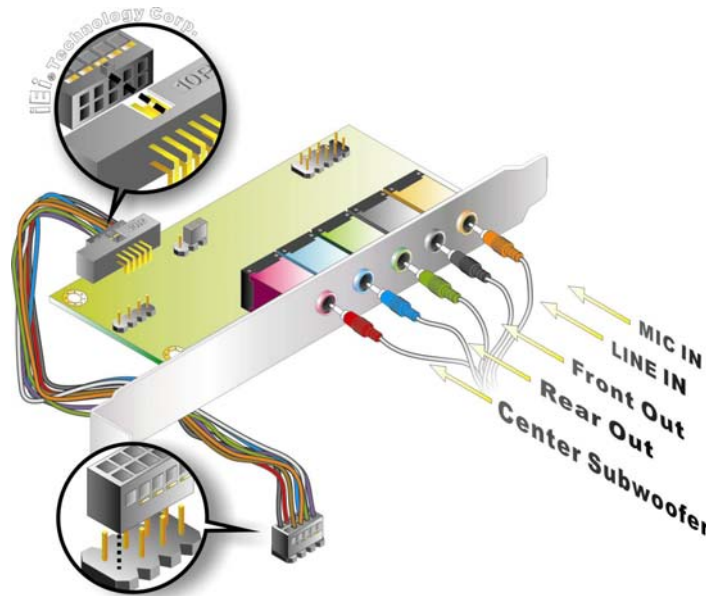
Figure 5-11: 7.1 Channel Audio Kit

Step 4: **Mount the audio kit onto the chassis**. Once the audio kit is connected to the

PICOe-945GSE, secure the audio kit bracket to the system chassis.

Step 5: **Connect the audio devices**. Connect one speaker to the line-in audio jack, one speaker to the line-out audio jack and a microphone to the mic-in audio jack.

Step 6: **Install the driver**. If the 7.1 channel audio kit is used, the ALC883 Realtek codec driver must be installed. Refer to **Chapter 7** for driver installation instructions.

5.7.4 SATA Drive Connection

The PICOe-945GSE is shipped with two SATA drive cables and one SATA drive power cable. To connect the SATA drives to the connectors, please follow the steps below.

Step 1: **Locate the connectors**. The locations of the SATA drive connectors are shown in **Chapter 3**.

Step 2: **Insert the cable connector**. Press the clip on the connector at the end of the SATA cable and insert the cable connector into the onboard SATA drive connector. See **Figure 5-12**.
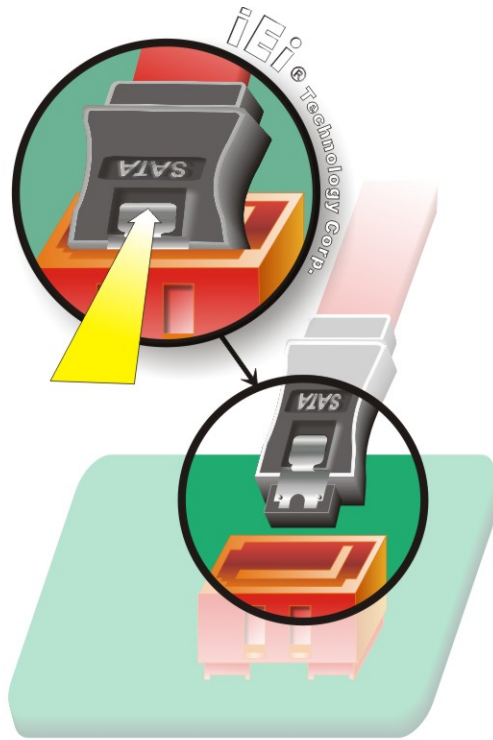
Figure 5-12: SATA Drive Cable Connection

Step 3: **Connect the cable to the SATA disk**. Connect the connector on the other end of the cable to the connector at the back of the SATA drive. See **Figure 5-13**.

Step 4: **Connect the SATA power cable**. Connect the SATA power connector to the back of the SATA drive. See **Figure 5-13**.

Figure 5-13: SATA Power Drive Connection

5.7.5 USB Cable (Dual Port) with Slot Bracket

The PICOe-945GSE is shipped with a dual port USB 2.0 cable. To connect the USB cable connector, please follow the steps below.

Step 1: Locate the connectors. The locations of the USB connectors are shown in **Chapter 3**.

WARNING:

If the USB pins are not properly aligned, the USB device can burn out.

Step 2: Align the connectors. The cable has two connectors. Correctly align pin 1on each cable connector with pin 1 on the PICOe-945GSE USB connector.

Step 3: Insert the cable connectors Once the cable connectors are properly aligned with the USB connectors on the PICOe-945GSE, connect the cable connectors to the on-board connectors. See **Figure 5-14**.
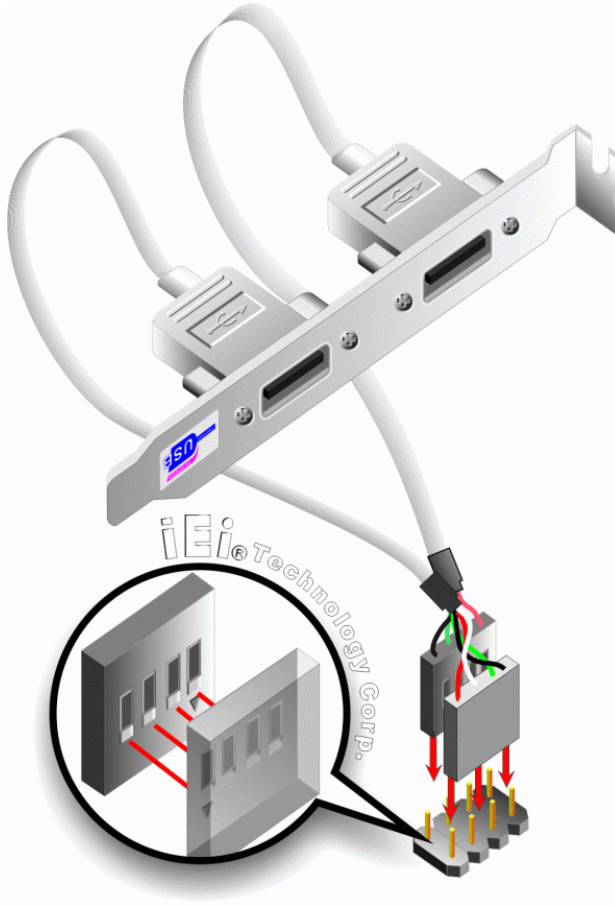
Figure 5-14: Dual USB Cable Connection

Step 4: **Attach the bracket to the chassis**. The USB 2.0 connectors are attached to a bracket. To secure the bracket to the chassis please refer to the installation instructions that came with the chassis.

5.7.6 Parallel Port Cable without Bracket

The optional parallel port (LPT) cable respectively connects the on-board LPT 26-pin box header to an external LPT device (like a printer). The cable comprises a 26-pin female header, to be connected to the on-board LPT box-header, on one side and on the other side a standard external LPT connector. To connect the LPT cable, please follow the steps below.

Step 1: **Locate the connector**. The LPT connector location is shown in **Chapter 4**.

Step 2: **Align the connectors**. Correctly align pin 1 on the cable connector with pin 1 on the PICOe-945GSE LPT box-header connector. See Figure 5-15.

Step 3: **Insert the cable connectors** Once the cable connector is properly aligned with the 26-pin box-header connector on the PICOe-945GSE, connect the cable connector to the on-board connector. See **Figure 5-15.**
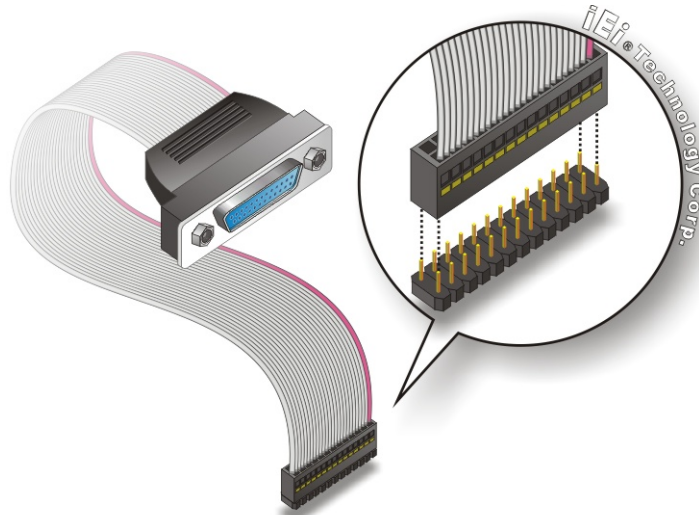
Figure 5-15: LPT Cable Connection

Step 4: **Attach the LPT connector to the chassis**. To secure the LPT interface connector to the chassis please refer to the installation instructions that came with the chassis.

Step 5: **Connect LPT device**. Once the LPT interface connector is connected to the chassis, the LPT device can be connected to the LPT interface connector. See **Figure 5-16**.
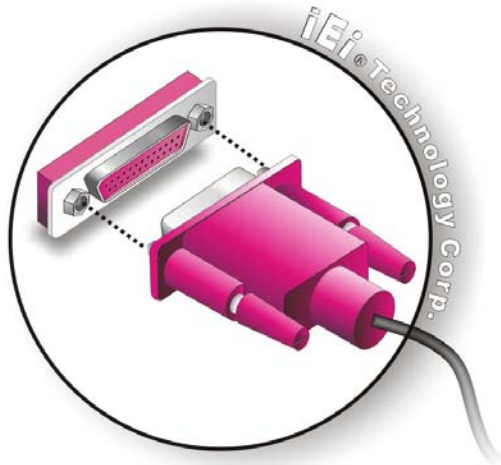
Figure 5-16: Connect the LPT Device

5.7.7 Dual RS-232 Cable with Slot Bracket

The dual RS-232 cable slot connector consists of two connectors attached to two independent cables. Each cable is then attached to a D-sub 9 male connector that is mounted onto a slot. To install the dual RS-232 cable, please follow the steps below.

Step 1: **Locate the connectors**. The locations of the RS-232 connectors are shown in **Chapter 3**.

Step 2: **Insert the cable connectors**. Insert one connector into each serial port box headers. See **Figure 5-17**. A key on the front of the cable connectors ensures the connector can only be installed in one direction.
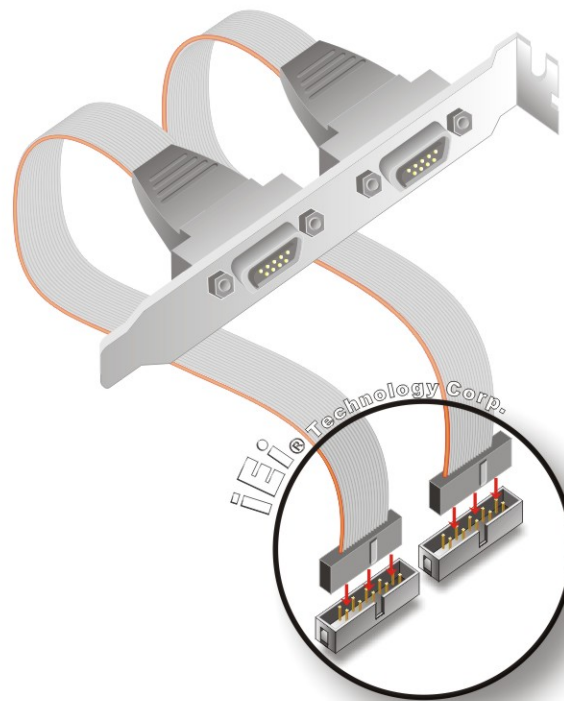
Figure 5-17: Dual RS-232 Cable Installation

Step 3: **Secure the bracket**. The dual RS-232 connector has two D-sub 9 male

connectors secured on a bracket. To secure the bracket to the chassis please

refer to the reference material that came with the chassis

5.8 External Peripheral Interface Connection

The following external peripheral devices can be connected to the external peripheral interface connectors.

- RJ-45 Ethernet cable connectors
- PS/2 devices
- USB devices
- VGA monitors

To install these devices, connect the corresponding cable connector from the actual device to the corresponding PICOe-945GSE external peripheral interface connector making sure the pins are properly aligned.

5.8.1 LAN Connection (Single Connector)

There are two external RJ-45 LAN connectors. The RJ-45 connectors enable connection to an external network. To connect a LAN cable with an RJ-45 connector, please follow the instructions below.

Step 1: **Locate the RJ-45 connectors**. The locations of the USB connectors are shown in **Chapter 4**.

Step 2: **Align the connectors.** Align the RJ-45 connector on the LAN cable with one of the RJ-45 connectors on the PICOe-945GSE. See **Figure 5-18**.
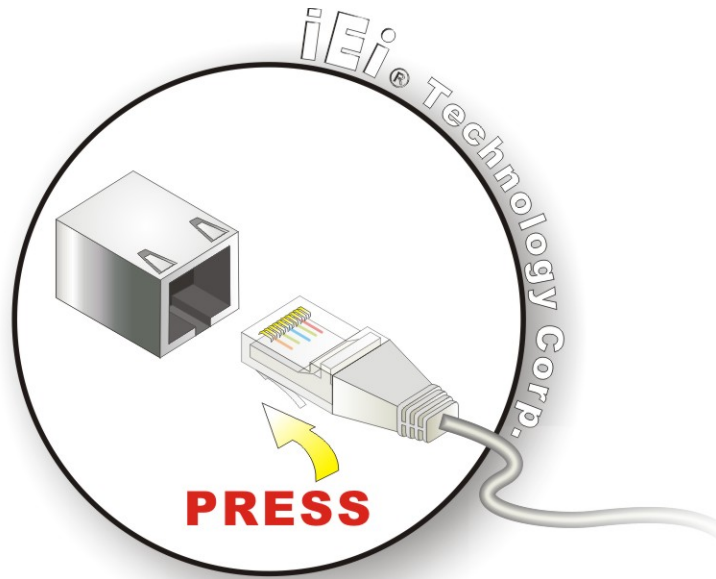
Figure 5-18: LAN Connection

Step 3: **Insert the LAN cable RJ-45 connector.** Once aligned, gently insert the LAN cable RJ-45 connector into the onboard RJ-45 connector.

5.8.2 PS/2 Y-Cable Connection

The PICOe-945GSE has a PS/2 connector on the external peripheral interface panel. The dual PS/2 connector is connected to the PS/2 Y-cable that came with the PICOe-945GSE. One of the PS/2 cables is connected to a keyboard and the other to a mouse to the system. Follow the steps below to connect a keyboard and mouse to the PICOe-945GSE.

Step 1: **Locate the dual PS/2 connector**. The location of the PS/2 connector is shown in **Chapter 3**.

Step 2: **Insert the keyboard/mouse connector**. Insert the PS/2 connector on the end of the PS/2 y-cable into the external PS/2 connector. See **Figure 5-19**.
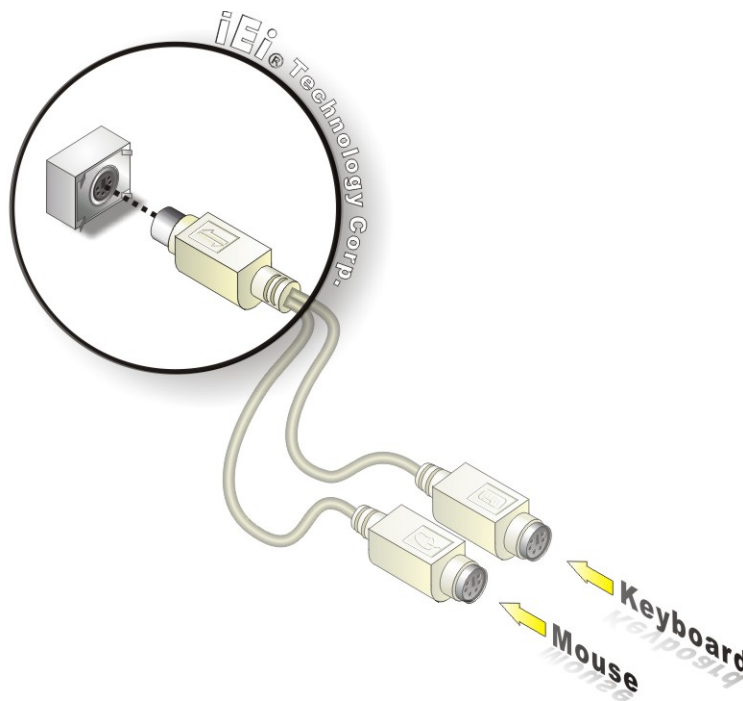
Figure 5-19: PS/2 Keyboard/Mouse Connector

Step 3: **Connect the keyboard and mouse**. Connect the keyboard and mouse to the appropriate connector. The keyboard and mouse connectors can be distinguished from each other by looking at the small graphic at the top of the connector.

5.8.3 USB Connection (Dual Connector)

The external USB Series "A" receptacle connectors provide easier and quicker access to external USB devices. Follow the steps below to connect USB devices to the PICOe-945GSE.

Step 1: **Locate the USB Series "A" receptacle connectors**. The location of the USB

Series "A" receptacle connectors are shown in **Chapter 3**.

Step 2: Insert a USB Series "A" plug. Insert the USB Series "A" plug of a device into the USB Series "A" receptacle on the external peripheral interface. See **Figure 5-20**.
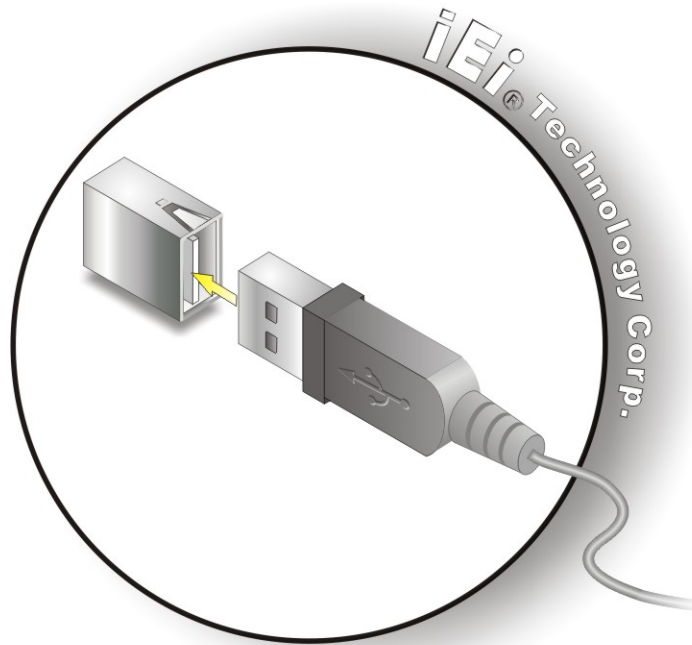
Figure 5-20: USB Connector

5.8.4 VGA Monitor Connection

The PICOe-945GSE has a single female DB-15 connector on the external peripheral interface panel. The DB-15 connector is connected to a CRT or VGA monitor. To connect a monitor to the PICOe-945GSE, please follow the instructions below.

Step 1: Locate the female DB-15 connector. The location of the female DB-15 connector is shown in **Chapter 3**.

Step 2: Align the VGA connector. Align the male DB-15 connector on the VGA screen cable with the female DB-15 connector on the external peripheral interface.

Step 3: Insert the VGA connector. Once the connectors are properly aligned with the

insert the male connector from the VGA screen into the female connector on the

PICOe-945GSE. See **Figure 5-21**.
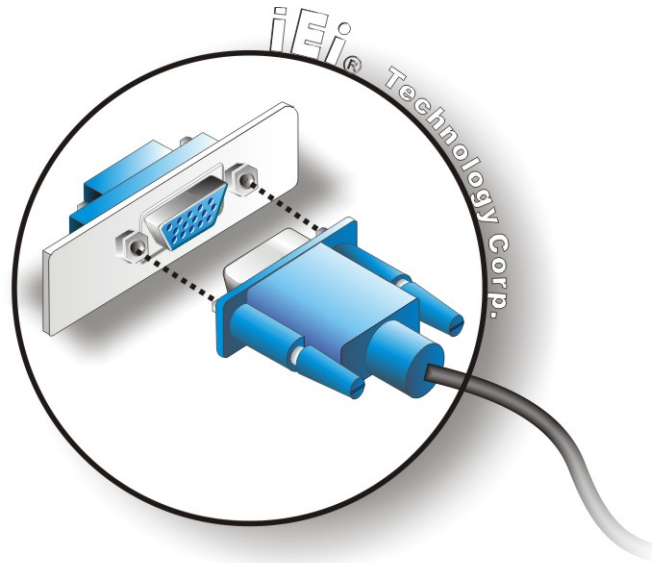
Figure 5-21: VGA Connector

Step 4: **Secure the connector**. Secure the DB-15 VGA connector from the VGA

monitor to the external interface by tightening the two retention screws on either

side of the connector.

Chapter

6

BIOS Screens

6.1 Introduction

A licensed copy of AMI BIOS is preprogrammed into the ROM BIOS. The BIOS setup program allows users to modify the basic system configuration.   This chapter describes how to access the BIOS setup program and the configuration options that may be changed.

6.1.1 Starting Setup

The AMI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. Press the DELETE key as soon as the system is turned on or
2. Press the DELETE key when the "**Press Del to enter SETUP**" message appears on the screen.

If the message disappears before the DELETE key is pressed, restart the computer and try again.

6.1.2 Using Setup

Use the arrow keys to highlight items, press ENTER to select, use the PageUp and PageDown keys to change entries, press **F1** for help and press ESC to quit. Navigation keys are shown in.

Key	Function
Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item on the left hand side
Right arrow	Move to the item on the right hand side
Esc key	Main Menu – Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
Page Up key	Increase the numeric value or make changes
Page Dn key	Decrease the numeric value or make changes

F1 key	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2 /F3 key	Change color from total 16 colors.　F2 to select color forward.
F10 key	Save all the CMOS changes, only for Main Menu

Table 6-1: BIOS Navigation Keys

6.1.3 Getting Help

When **F1** is pressed a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window press **Esc** or the **F1** key again.

6.1.4 Unable to Reboot After Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the jumper described in **Chapter 5**.

6.1.5 BIOS Menu Bar

The **menu bar** on top of the BIOS screen has the following main items:

- **Main** Changes the basic system configuration.
- **Advanced** Changes the advanced system settings.
- **PCIPnP** Changes the advanced PCI/PnP Settings
- **Boot** Changes the system boot configuration.
- **Security** Sets User and Supervisor Passwords.
- **Chipset** Changes the chipset settings.
- **Exit** Selects exit options and loads default settings

The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

6.2 Main

The **Main** BIOS menu (**BIOS Menu 1**) appears when the **BIOS Setup** program is entered.

The **Main** menu gives an overview of the basic system information.

```
                          BIOS SETUP UTILITY
   Main    Advanced    PCIPnP    Boot    Security    Chipset    Exit

  System Overview                                  Use [ENTER], [TAB] or
                                                   [SHIFT-TAB] to select
  AMIBIOS                                          a field.
  Version    :08.00.15
  Build Date:10/07/08                              Use [+] or [-] to
  ID         :B119MR13                             configure system
  0                                                Time.

  Processor
  Genuine Intel® CPU N270  @ 1.60GHz
  Speed      :1600MHz
  Count      :1
                                                   ←→    Select Screen
  System Memory                                    ↑↓    Select Item
  Size       :1016MB                               +-    Change Field
                                                   Tab   Select Field
  System Time              [14:20:27]              F1    General Help
  System Date             [Tue 09/24/2008]         F10   Save and Exit
                                                   ESC   Exit

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```

BIOS Menu 1: Main

➔ **System Overview**

The **System Overview** lists a brief summary of different system components. The fields in **System Overview** cannot be changed. The items shown in the system overview include:

- ■ **AMI BIOS**: Displays auto-detected BIOS information
  - ○ Version: Current BIOS version
  - ○ Build Date: Date the current BIOS version was made
  - ○ ID: Installed BIOS ID
- ■ **Processor**: Displays auto-detected CPU specifications
  - ○ Type: Names the currently installed processor
  - ○ Speed: Lists the processor speed
  - ○ Count: The number of CPUs on the CPU card
- ■ **System Memory**: Displays the auto-detected system memory.

o   Size: Lists memory size

The System Overview field also has two user configurable fields:

➔   **System Time [xx:xx:xx]**

Use the **System Time** option to set the system time. Manually enter the hours, minutes and seconds.

➔   **System Date [xx/xx/xx]**

Use the **System Date** option to set the system date. Manually enter the day, month and year.

6.3 Advanced

Use the **Advanced** menu (**BIOS Menu 2**) to configure the CPU and peripheral devices through the following sub-menus:

⚠ **WARNING:**

Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.

■   CPU Configuration (see **Section 6.3.1**)
■   IDE Configuration (see **Section 6.3.2**)
■   SuperIO Configuration (see **Section 6.3.3**)
■   Hardware Health Configuration (see **Section 6.3.4**)
■   Power Configuration (see **Section 6.3.5**)
■   Remote Access Configuration (see **Section 6.3.6**)
■   USB Configuration (see **Section 6.3.8**)
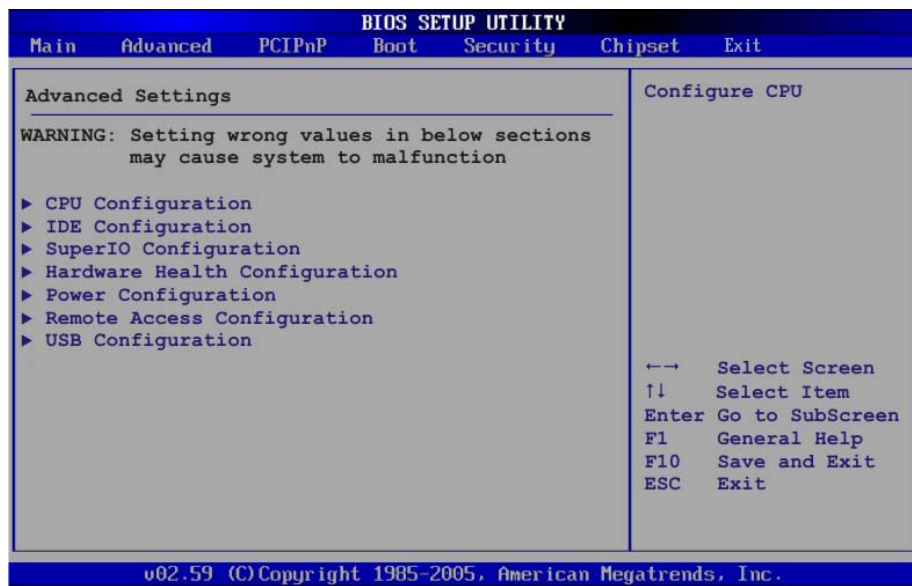
BIOS Menu 2: Advanced

6.3.1 CPU Configuration

Use the **CPU Configuration** menu (**BIOS Menu 3**) to view detailed CPU specifications and configure the CPU.
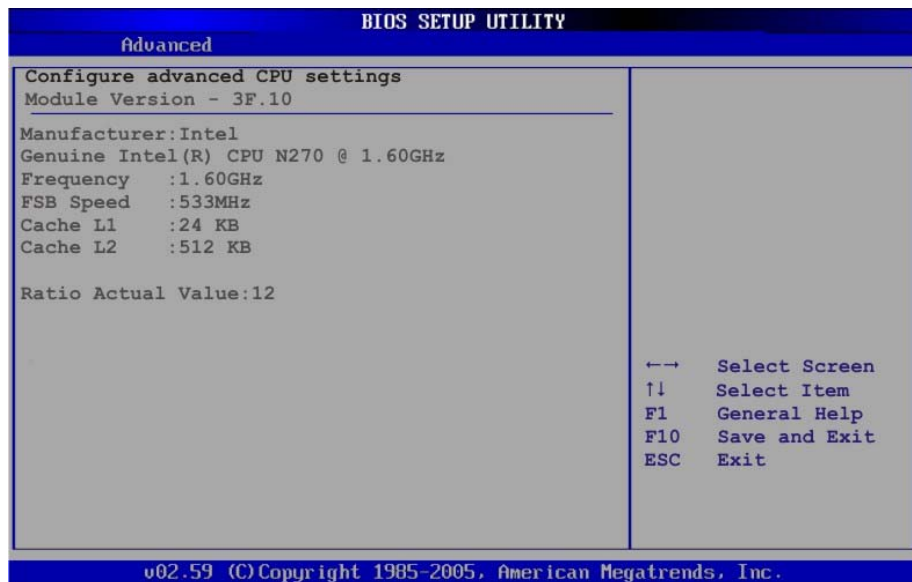
BIOS Menu 3: CPU Configuration

The CPU Configuration menu (**BIOS Menu 3**) lists the following CPU details:

- **Manufacturer**: Lists the name of the CPU manufacturer
- **Brand String**: Lists the brand name of the CPU being used
- **Frequency:** Lists the CPU processing speed
- **FSB Speed**: Lists the FSB speed
- **Cache L1**: Lists the CPU L1 cache size
- **Cache L2**: Lists the CPU L2 cache size

6.3.2 IDE Configuration

Use the **IDE Configuration** menu (**BIOS Menu 4**) to change and/or set the configuration of the IDE devices installed in the system.
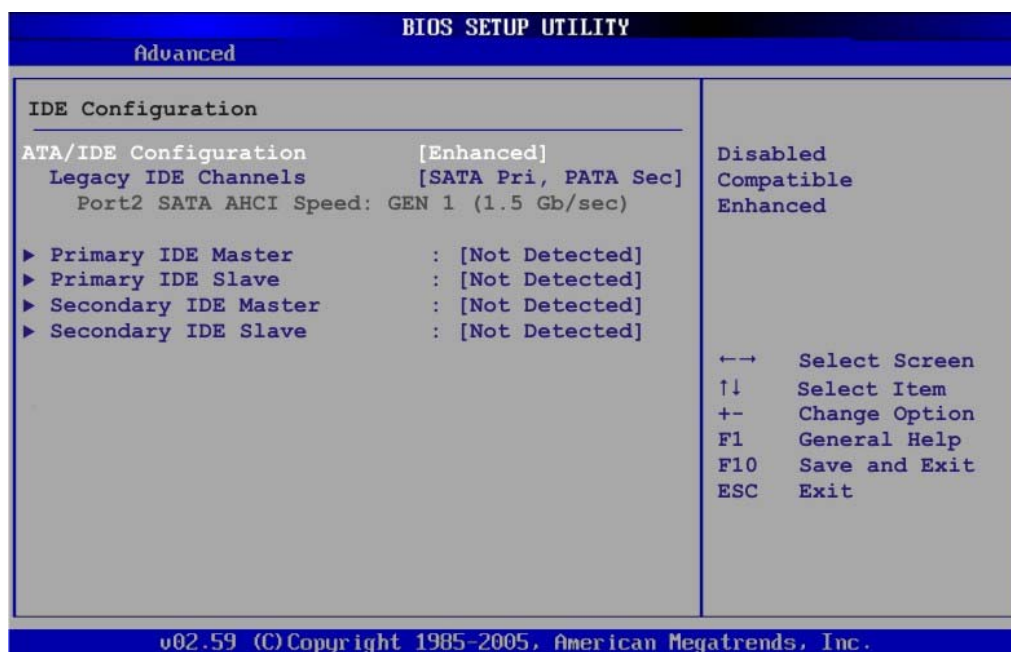
BIOS Menu 4: IDE Configuration

➔ **ATA/IDE Configurations [Compatible]**

Use the **ATA/IDE Configurations** option to configure the ATA/IDE controller.

➔ **Disabled**   Disables the on-board ATA/IDE controller.

➔ **Compatible** DEFAULT Configures the on-board ATA/IDE controller to be in compatible mode. In this mode, a SATA channel will replace one of the IDE channels. This mode supports up to 4 storage devices.

➔ **Enhanced** Configures the on-board ATA/IDE controller to be in Enhanced mode. In this mode, IDE channels and SATA channels are separated. This mode supports up to 6 storage devices. Some legacy OS do not support this mode.

➔ **Legacy IDE Channels [PATA Pri, SATA Sec]**

➔ **SATA Only** Only the SATA drives are enabled.

➔ **SATA Pri, PATA Sec** DEFAULT The IDE drives are enabled on the Primary IDE channel. The SATA drives are enabled on the Secondary IDE channel.

➔ **PATA Only** The IDE drives are enabled on the primary and secondary IDE channels. SATA drives are disabled.

➔ **IDE Master and IDE Slave**

When entering setup, BIOS auto detects the presence of IDE devices. BIOS displays the status of the auto detected IDE devices. The following IDE devices are detected and are shown in the **IDE Configuration** menu:

- Primary IDE Master
- Primary IDE Slave
- Secondary IDE Master
- Secondary IDE Slave

The **IDE Configuration** menu (**BIOS Menu 4**) allows changes to the configurations for the IDE devices installed in the system. If an IDE device is detected, and one of the above listed four BIOS configuration options are selected, the IDE configuration options shown in **Section 6.3.2.1** appear.

6.3.2.1 IDE Master, IDE Slave

Use the **IDE Master** and **IDE Slave** configuration menu to view both primary and secondary IDE device details and configure the IDE devices connected to the system.
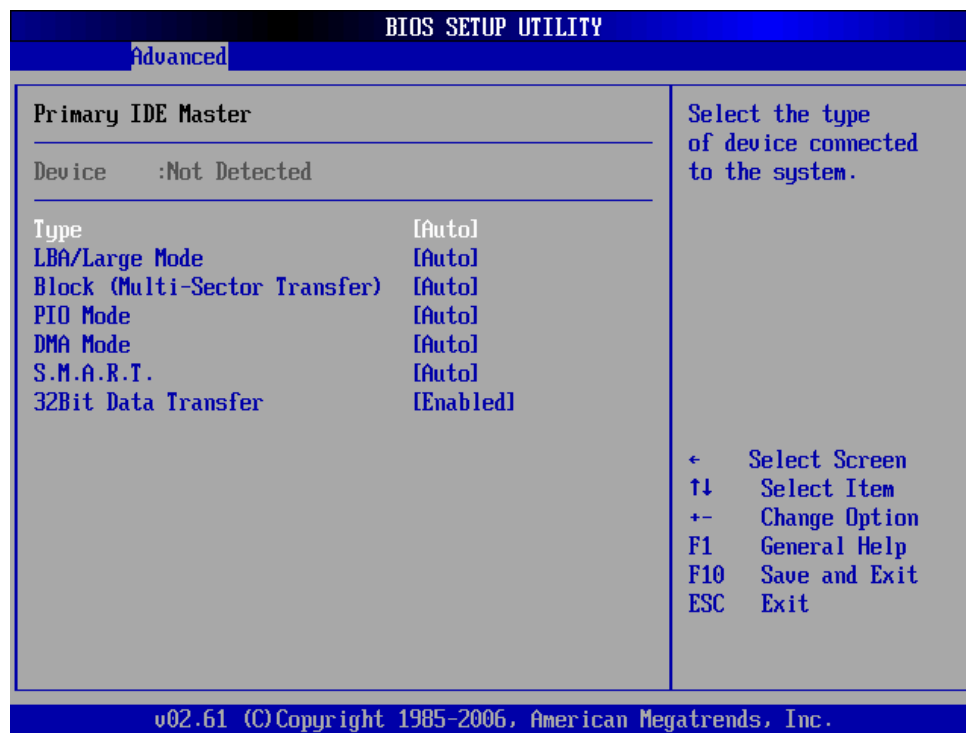
BIOS Menu 5: IDE Master and IDE Slave Configuration

➔ **Auto-Detected Drive Parameters**

The "grayed-out" items in the left frame are IDE disk drive parameters automatically detected from the firmware of the selected IDE disk drive. The drive parameters are listed as follows:

■ **Device**: Lists the device type (e.g. hard disk, CD-ROM etc.)

■ **Type**: Indicates the type of devices a user can manually select

■ **Vendor**: Lists the device manufacturer

■ **Size**: List the storage capacity of the device.

■ **LBA Mode**: Indicates whether the LBA (Logical Block Addressing) is a method of addressing data on a disk drive is supported or not.

■ **Block Mode**: Block mode boosts IDE drive performance by increasing the amount of data transferred. Only 512 bytes of data can be transferred per interrupt if block mode is not used. Block mode allows transfers of up to 64 KB per interrupt.

■ **PIO Mode**: Indicates the PIO mode of the installed device.

■ **Async DMA**: Indicates the highest Asynchronous DMA Mode that is supported.

■ **Ultra DMA**: Indicates the highest Synchronous DMA Mode that is supported.

■ **S.M.A.R.T.**: Indicates whether or not the Self-Monitoring Analysis and Reporting Technology protocol is supported.

■ **32Bit Data Transfer**: Enables 32-bit data transfer.

➔ **Type [Auto]**

Use the **Type** BIOS option select the type of device the AMIBIOS attempts to boot from after the Power-On Self-Test (POST) is complete.

➔ **Not Installed**   BIOS is prevented from searching for an IDE disk drive on the specified channel.

➔ **Auto**   DEFAULT   The BIOS auto detects the IDE disk drive type attached to the specified channel. This setting should be used if an IDE hard disk drive is attached to the specified channel.

➔ **CD/DVD**   The CD/DVD option specifies that an IDE CD-ROM drive is attached to the specified IDE channel. The BIOS does not attempt to search for other types of

IDE disk drives on the specified channel.

➔ **ARMD**　　　　　　　This option specifies an ATAPI Removable Media Device. These include, but are not limited to:

　　　　➔ **ZIP**

　　　　➔ **LS-120**

➔ **LBA/Large Mode [Auto]**

Use the **LBA/Large Mode** option to disable or enable BIOS to auto detects LBA (Logical Block Addressing). LBA is a method of addressing data on a disk drive. In LBA mode, the maximum drive capacity is 137 GB.

➔ **Disabled**　　　　　BIOS is prevented from using the LBA mode control on the specified channel.

➔ **Auto**　　**DEFAULT**　BIOS auto detects the LBA mode control on the specified channel.

➔ **Block (Multi Sector Transfer) [Auto]**

Use the **Block (Multi Sector Transfer)** to disable or enable BIOS to auto detect if the device supports multi-sector transfers.

➔ **Disabled**　　　　　BIOS is prevented from using Multi-Sector Transfer on the specified channel. The data to and from the device occurs one sector at a time.

➔ **Auto**　　**DEFAULT**　BIOS auto detects Multi-Sector Transfer support on the drive on the specified channel. If supported the data transfer to and from the device occurs multiple sectors at a time.

➔ **PIO Mode [Auto]**

Use the **PIO Mode** option to select the IDE PIO (Programmable I/O) mode program timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases.

➔ **Auto**   DEFAULT   BIOS auto detects the PIO mode. Use this value if the IDE disk drive support cannot be determined.

➔ **0**   PIO mode 0 selected with a maximum transfer rate of 3.3MBps

➔ **1**   PIO mode 1 selected with a maximum transfer rate of 5.2MBps

➔ **2**   PIO mode 2 selected with a maximum transfer rate of 8.3MBps

➔ **3**   PIO mode 3 selected with a maximum transfer rate of 11.1MBps

➔ **4**   PIO mode 4 selected with a maximum transfer rate of 16.6MBps

(This setting generally works with all hard disk drives manufactured after 1999. For other disk drives, such as IDE CD-ROM drives, check the specifications of the drive.)

➔ **DMA Mode [Auto]**

Use the **DMA Mode** BIOS selection to adjust the DMA mode options.

➔ **Auto**   DEFAULT   BIOS auto detects the DMA mode. Use this value if the IDE disk drive support cannot be determined.

➔ **SWDMA0**   Single Word DMA mode 0 selected with a maximum data transfer rate of 2.1MBps

➔ **SWDMA1**   Single Word DMA mode 1 selected with a maximum data transfer rate of 4.2MBps

➔ **SWDMA2**   Single Word DMA mode 2 selected with a maximum data transfer rate of 8.3MBps

➔ **MWDMA0**   Multi Word DMA mode 0 selected with a maximum data transfer rate of 4.2MBps

➔ **MWDMA1**   Multi Word DMA mode 1 selected with a maximum data transfer rate of 13.3MBps

➔ **MWDMA2**   Multi Word DMA mode 2 selected with a maximum data transfer rate of 16.6MBps

➔ **UDMA1**   Ultra DMA mode 0 selected with a maximum data transfer rate of 16.6MBps

➔ **UDMA1**   Ultra DMA mode 1 selected with a maximum data transfer rate of 25MBps

➔ **UDMA2**   Ultra DMA mode 2 selected with a maximum data transfer rate of 33.3MBps

➔ **UDMA3**   Ultra DMA mode 3 selected with a maximum data transfer rate of 44MBps (To use this mode, it is required that an 80-conductor ATA cable is used.)

➔ **UDMA4**   Ultra DMA mode 4 selected with a maximum data transfer rate of 66.6MBps (To use this mode, it is required that an 80-conductor ATA cable is used.)

➔ **UDMA5**   Ultra DMA mode 5 selected with a maximum data transfer rate of 99.9MBps (To use this mode, it is required that an 80-conductor ATA cable is used.)

➔ **S.M.A.R.T [Auto]**

Use the **S.M.A.R.T** option to auto-detect, disable or enable Self-Monitoring Analysis and Reporting Technology (SMART) on the drive on the specified channel. **S.M.A.R.T** predicts impending drive failures. The **S.M.A.R.T** BIOS option enables or disables this function.

➔ **Auto** DEFAULT BIOS auto detects HDD SMART support.

➔ **Disabled** Prevents BIOS from using the HDD SMART feature.
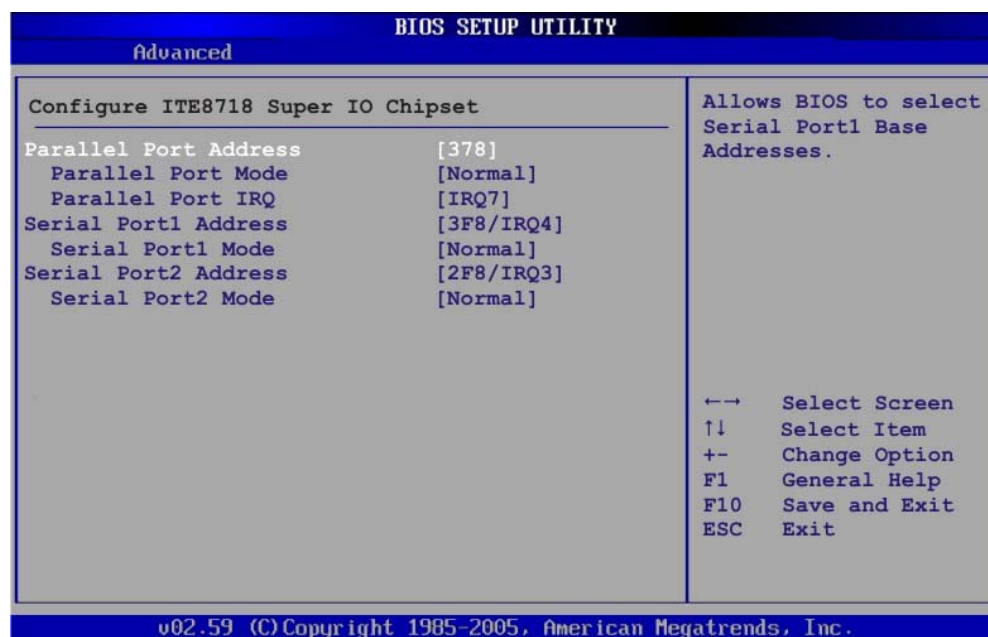
➔ **Enabled** Allows BIOS to use the HDD SMART feature

➔ **32Bit Data Transfer [Enabled]**

Use the **32Bit Data Transfer** BIOS option to enables or disable 32-bit data transfers.

➔ **Disabled** Prevents the BIOS from using 32-bit data transfers.

➔ **Enabled** DEFAULT Allows BIOS to use 32-bit data transfers on supported hard disk drives.

6.3.3 Super IO Configuration

Use the **Super IO Configuration** menu (**BIOS Menu 6**) to set or change the configurations for the FDD controllers, parallel ports and serial ports.

```
                          BIOS SETUP UTILITY
      Advanced

 Configure ITE8718 Super IO Chipset           Allows BIOS to select
 ─────────────────────────────────────        Serial Port1 Base
 Parallel Port Address       [378]            Addresses.
   Parallel Port Mode        [Normal]
   Parallel Port IRQ         [IRQ7]
 Serial Port1 Address        [3F8/IRQ4]
   Serial Port1 Mode         [Normal]
 Serial Port2 Address        [2F8/IRQ3]
   Serial Port2 Mode         [Normal]



                                              ←→    Select Screen
                                              ↑↓    Select Item
                                              +-    Change Option
                                              F1    General Help
                                              F10   Save and Exit
                                              ESC   Exit


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```

BIOS Menu 6: Super IO Configuration

➔ **Parallel Port Address [378]**

Use the **Parallel Port Address** option to select the parallel port base address.

➔ **Disabled** No base address is assigned to the Parallel Port

➔ **378** DEFAULT Parallel Port I/O port address is 378

➔ **278** Parallel Port I/O port address is 278

➔ **3BC** Parallel Port I/O port address is 3BC

➔ **Parallel Port Mode [Normal]**

Use the **Parallel Port Mode** option to select the mode the parallel port operates in.

➔ **Normal** DEFAULT The normal parallel port mode is the standard mode for parallel port operation.

➔ **EPP** The parallel port operates in the enhanced parallel port mode (EPP). The EPP mode supports bi-directional communication between the system and the parallel port device and the transmission rates between the two are much faster than the Normal mode.

➔ **ECP+EPP** The parallel port operates in the extended capabilities port (ECP) mode. The ECP mode supports bi-directional communication between the system and the parallel port device and the transmission rates between the two are much faster than the Normal mode

The parallel port is also be compatible with EPP devices described above

➔ **Parallel Port IRQ [IRQ7]**

Use the **Parallel Port IRQ** selection to set the parallel port interrupt address.

➔ **IRQ5**   IRQ5 is assigned as the parallel port interrupt address

➔ **IRQ7**   DEFAULT   IRQ7 is assigned as the parallel port interrupt address

➔ **Serial Port1 Address [3F8/IRQ4]**

Use the **Serial Port1 Address** option to select the Serial Port 1 base address.

➔ **Disabled**   No base address is assigned to Serial Port 1

➔ **3F8/IRQ4**   DEFAULT   Serial Port 1 I/O port address is 3F8 and the interrupt address is IRQ4

➔ **3E8/IRQ4**   Serial Port 1 I/O port address is 3E8 and the interrupt address is IRQ4

➔ **2E8/IRQ3**   Serial Port 1 I/O port address is 2E8 and the interrupt address is IRQ3

➔ **Serial Port1 Mode [Normal]**

Use the **Serial Port1 Mode** option to select the transmitting and receiving mode for the first serial port.

➔ **Normal**   DEFAULT   Serial Port 1 mode is normal

➔ **IrDA**   Serial Port 1 mode is IrDA

➔ **ASK IR**   Serial Port 1 mode is ASK IR

➔ **Serial Port2 Address [2F8/IRQ3]**

Use the **Serial Port2 Address** option to select the Serial Port 2 base address.

➔ **Disabled**   No base address is assigned to Serial Port 2

➔ **2F8/IRQ3** DEFAULT Serial Port 2 I/O port address is 3F8 and the interrupt address is IRQ3

➔ **3E8/IRQ4**   Serial Port 2 I/O port address is 3E8 and the interrupt address is IRQ4

➔ **2E8/IRQ3**   Serial Port 2 I/O port address is 2E8 and the interrupt address is IRQ3
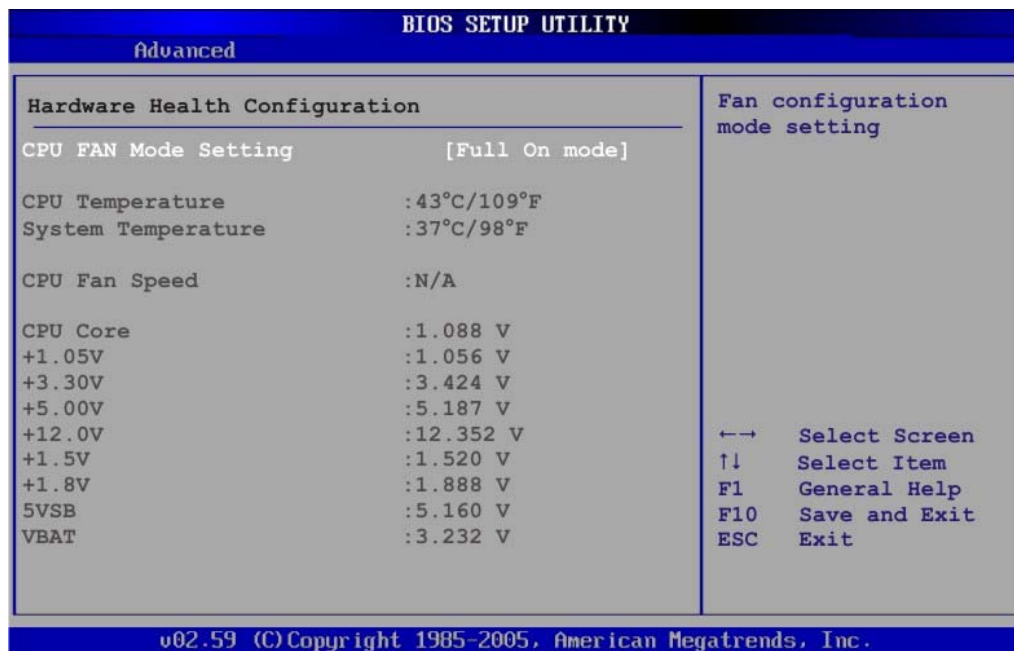
➔ **Serial Port2 Mode [Normal]**

Use the **Serial Port2 Mode** option to select the Serial Port2 operational mode.

➔ **Normal**   DEFAULT Serial Port 2 mode is normal

➔ **IrDA**   Serial Port 2 mode is IrDA

➔ **ASK IR**   Serial Port 2 mode is ASK IR

6.3.4 Hardware Health Configuration

The **Hardware Health Configuration** menu (**BIOS Menu 7**) shows the operating temperature, fan speeds and system voltages.

BIOS Menu 7: Hardware Health Configuration

➔ **CPU FAN Mode Setting [Full On Mode]**

Use the **CPU FAN Mode Setting** option to configure the second fan.

➔ **Full On Mode**   DEFAULT   Fan is on all the time

➔ **Automatic mode**   Fan is off when the temperature is low
                                                          enough. Parameters must be set by the
                                                          user.

➔ **PWM Manual mode**   Pulse width modulation set manually

When the **CPU FAN Mode Setting** option is in the **Automatic Mode**, the following
parameters can be set.

■   CPU Temp. Limit of OFF
■   CPU Temp. Limit of Start
■   CPU Fan Start PWM
■   Slope PWM

When the **CPU FAN Mode Setting** option is in the **PWM Manual Mode**, the following parameters can be set.

- CPU Fan PWM control

➔ **CPU Temp. Limit of OFF [000]**

![Warning icon] **WARNING:**

Setting this value too high may cause the fan to stop when the CPU is at a high temperature and therefore cause the system to be damaged.

The **CPU Temp. Limit of OFF** option can only be set if the **CPU FAN Mode Setting** option is set to **Automatic Mode**. Use the **CPU Temp. Limit of OFF** option to select the CPU temperature at which the cooling fan should automatically turn off. To select a value, select the **CPU Temp. Limit of OFF** option and enter a decimal number between 000 and 127. The temperature range is specified below.

- Minimum Value: 0°C
- Maximum Value: 127°C

➔ **CPU Temp. Limit of Start [020]**

![Warning icon] **WARNING:**

Setting this value too high may cause the fan to start only when the CPU is at a high temperature and therefore cause the system to be damaged.

The **CPU Temp. Limit of Start** option can only be set if the **CPU FAN Mode Setting** option is set to **Automatic Mode**. Use the **CPU Temp. Limit of Start** option to select the CPU temperature at which the cooling fan should automatically turn on. When the fan

starts, it rotates using the starting pulse width modulation (PWM) specified in the **Fan 3 Start PWM** option below. To select a value, select the **CPU Temp. Limit of Start** option and enter a decimal number between 000 and 127. The temperature range is specified below.

- ■ Minimum Value: 0°C
- ■ Maximum Value: 127°C

➔ **CPU Fan Start PWM [070]**

The **Fan 3 Start PWM** option can only be set if the **CPU FAN Mode Setting** option is set to **Automatic Mode**. Use the **Fan 3 Start PWM** option to select the PWM mode the fan starts to rotate with after the temperature specified in the **Temperature 3 Limit of Start** is exceeded. The Super I/O chipset supports 128 PWM modes. To select a value, select the **Fan 3 Start PWM** option and enter a decimal number between 000 and 127. The temperature range is specified below.

- ■ PWM Minimum Mode: 0
- ■ PWM Maximum Mode: 127

➔ **Slope PWM   [0.5 PWM]**

The **Slope PWM 1** option can only be set if the **CPU FAN Mode Setting** option is set to **Automatic Mode**. Use the **Slope PWM 1** option to select the linear rate at which the PWM mode increases with respect to an increase in temperature. A list of available options is shown below:

- ■ 0.125 PWM
- ■ 0.25 PWM
- ■ 0.5 PWM
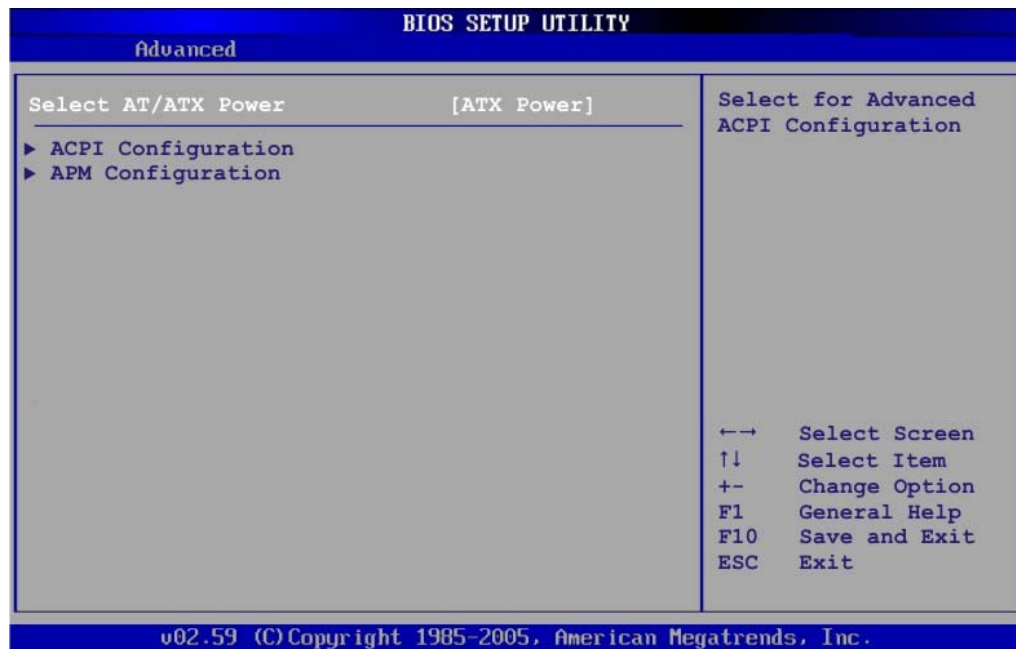- ■ 1 PWM
- ■ 2 PWM
- ■ 4 PWM
- ■ 8 PWM
- ■ 15 PWM

The following system parameters and values are shown. The system parameters that are monitored are:

- ■ **System Temperatures**: The following system temperatures are monitored
  - ○ CPU Temperature
  - ○ System Temperature
- ■ **Fan Speeds**: The CPU cooling fan speed is monitored.
  - ○ CPU Fan Speed
- ■ **Voltages**: The following system voltages are monitored
  - ○ CPU Core
  - ○ +1.05V
 - ○ +3.30V
  - ○ +5.00V
  - ○ +12.0 V
  - ○ +1.5V
  - ○ +1.8V
  - ○ 5VSB
  - ○ VBAT

6.3.5 Power Configuration

The **Power Configuration** menu (**BIOS Menu 8**) configures the Advanced Configuration and Power Interface (ACPI) and Power Management (APM) options.

```
                        BIOS SETUP UTILITY
        Advanced

Select AT/ATX Power           [ATX Power]          Select for Advanced
                                                   ACPI Configuration
▶ ACPI Configuration
▶ APM Configuration




                                                   ←→     Select Screen
                                                   ↑↓     Select Item
                                                   +-     Change Option
                                                   F1     General Help
                                                   F10    Save and Exit
                                                   ESC    Exit


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```

BIOS Menu 8: Power Configuration

6.3.5.1 ACPI configuration

The **ACPI Configuration** menu (**BIOS Menu 9**) configures the Advanced Configuration and Power Interface (ACPI).
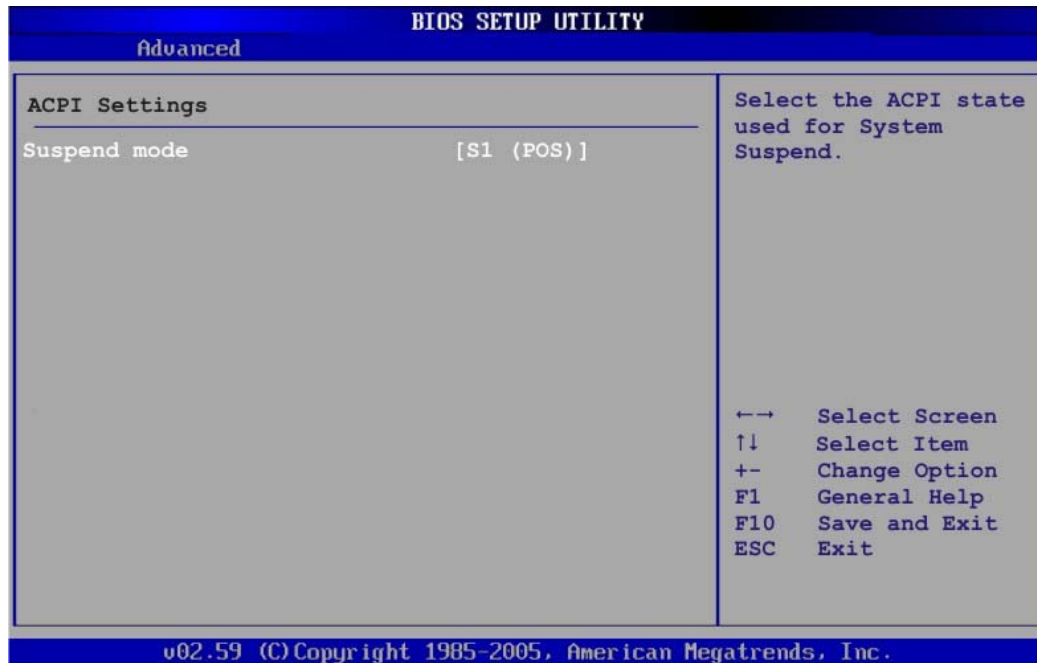
BIOS Menu 9: ACPI Configuration

➔ **Suspend Mode [S1(POS)]**

Use the **Suspend Mode** BIOS option to specify the sleep state the system enters when it is not being used.

➔ **S1 (POS)** DEFAULT System appears off. The CPU is stopped; RAM is refreshed; the system is running in a low power mode.

➔ **S3 (STR)** System appears off. The CPU has no power; RAM is in slow refresh; the power supply is in a reduced power mode.

6.3.6 APM Configuration

The **APM Configuration** menu (**BIOS Menu 10**) allows the advanced power management options to be configured.
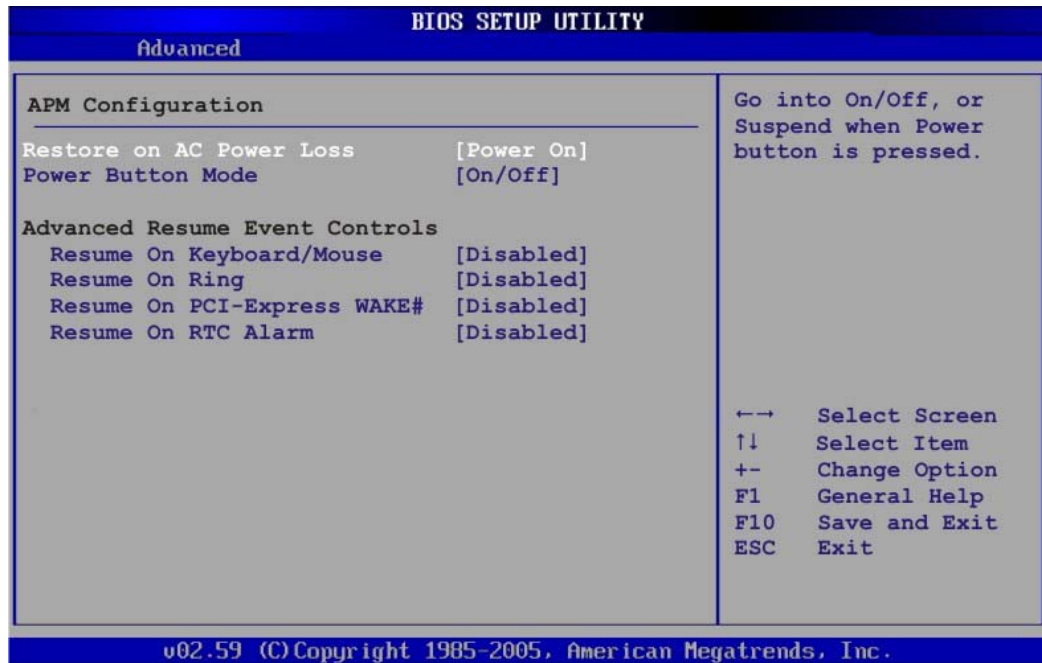
BIOS Menu 10: Advanced Power Management Configuration

➔ **Restore on AC Power Loss [Power On]**

Use the **Restore on AC Power Loss** BIOS option to specify what state the system returns to if there is a sudden loss of power to the system.

➔ **Power Off**　　　　　　The system remains turned off

➔ **Power On**　 DEFAULT 　The system turns on

➔ **Last State**　　　　　　The system returns to its previous state. If it was on, it turns itself on. If it was off, it remains off.

➔ **Power Button Mode [On/Off]**

Use the **Power Button Mode** BIOS to specify how the power button functions.

➔ **On/Off**　 DEFAULT 　When the power button is pressed the system is either turned on or off

➔ **Suspend**　　　　　　When the power button is pressed the system goes into

suspend mode

➔ **Resume on Keyboard/Mouse [Disabled]**

Use the **Resume on Keyboard/Mouse** BIOS option to enable activity on either the keyboard or mouse to rouse the system from a suspend or standby state. That is, the system is roused when the mouse is moved or a button on the keyboard is pressed.

➔ **Disabled** DEFAULT Wake event not generated by activity on the keyboard or mouse

➔ **Resume On KeyBoard** Wake event not generated by activity on the keyboard

➔ **Resume On Mouse** Wake event not generated by activity on the mouse

➔ **Enabled** Wake event generated by activity on the keyboard or mouse

➔ **Resume on Ring [Disabled]**

Use the **Resume on Ring** BIOS option to enable activity on the RI (ring in) modem line to rouse the system from a suspend or standby state. That is, the system will be roused by an incoming call on a modem.

➔ **Disabled** DEFAULT Wake event not generated by an incoming call

➔ **Enabled** Wake event generated by an incoming call

➔ **Resume on PCI-Express WAKE# [Enabled]**

Use the **Resume PCI-Express WAKE#** BIOS option to enable activity on the PCI-Express WAKE# signal to rouse the system from a suspend or standby state.

➔ **Disabled** Wake event not generated by PCI-Express WAKE#

signal activity

➔ **Enabled** 　DEFAULT　 Wake event generated by PCI-Express WAKE# signal activity

➔ **Resume On RTC Alarm [Disabled]**

Use the **Resume On RTC Alarm** option to specify the time the system should be roused from a suspended state.

➔ **Disabled** 　DEFAULT　 The real time clock (RTC) cannot generate a wake event

➔ **Enabled** 　　　　　 If selected, the following appears with values that can be selected:

➔ **RTC Alarm Date (Days)**

➔ **System Time**

After setting the alarm, the computer turns itself on from a suspend state when the alarm goes off.

6.3.7 Remote Configuration

Use the **Remote Access Configuration** menu (**BIOS Menu 11**) to configure remote access parameters. The **Remote Access Configuration** is an AMIBIOS feature and allows a remote host running a terminal program to display and configure the BIOS settings.
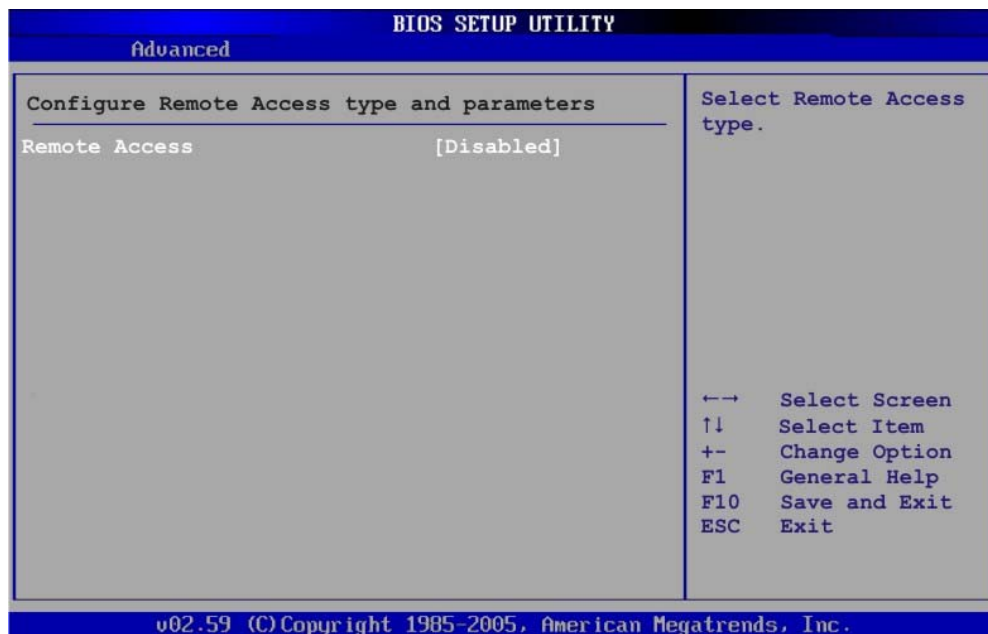
BIOS Menu 11: Remote Access Configuration [Advanced]

➔ **Remote Access [Disabled]**

Use the **Remote Access** option to enable or disable access to the remote functionalities of the system.

➔ **Disabled** **DEFAULT** Remote access is disabled.

➔ **Enabled** Remote access configuration options shown below appear:

➔ **Serial Port Number**

➔ **Serial Port Mode**

➔ **Redirection after BIOS POST**

➔ **Terminal Type**

These configuration options are discussed below.

➔ **Serial Port Number [COM1]**

Use the **Serial Port Number** option allows to select the serial port used for remote access.

➔ **COM1**   DEFAULT   System is remotely accessed through COM1

➔ **COM2**   System is remotely accessed through COM2

NOTE: Make sure the selected COM port is enabled through the Super I/O configuration menu.

➔ **Base Address, IRQ [3F8h,4]**

The **Base Address, IRQ** option cannot be configured and only shows the interrupt address of the serial port listed above.

➔ **Serial Port Mode [115200 8,n,1]**

Use the **Serial Port Mode** option to select baud rate through which the console redirection is made. The following configuration options are available

- 115200 8,n,1 **DEFAULT**
- 57600 8,n,1
- 38400 8,n,1
- 19200 8,n,1
- 09600 8,n,1

NOTE:

Identical baud rate setting musts be set on the host (a management computer running a terminal software) and the slave

➔ **Redirection After BIOS POST [Always]**

Use the **Redirection After BIOS POST** option to specify when console redirection should occur.

➔ **Disabled** The console is not redirected after POST

➔ **Boot Loader** Redirection is active during POST and during Boot Loader

➔ **Always** DEFAULT Redirection is always active (Some OSes may not work if set to Always)

➔ **Terminal Type [ANSI]**

Use the **Terminal Type** BIOS option to specify the remote terminal type.

➔ **ANSI** DEFAULT The target terminal type is ANSI

➔ **VT100** The target terminal type is VT100

➔ **VT-UTF8** The target terminal type is VT-UTF8

6.3.8 USB Configuration

Use the **USB Configuration** menu (**BIOS Menu 12**) to read USB configuration information and configure the USB settings.

```
                        BIOS SETUP UTILITY
     Advanced

  USB Configuration                            Enables USB 1.1 host
                                               controllers.
  Module Version - 2.24.3-13.4

  USB Devices Enabled :
            None

  USB Functions                 [Enabled]
  USB 2.0 Controller            [Enabled]
  Legacy USB Support            [Enabled]
  USB 2.0 Controller Mode       [HiSpeed]


                                               ←→     Select Screen
                                               ↑↓     Select Item
                                               +-     Change Option
                                               F1     General Help
                                               F10    Save and Exit
                                               ESC    Exit


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```

BIOS Menu 12: USB Configuration

➔ **USB Functions [Enabled]**

Use the **USB Function** option to enable or disable the USB controllers.

➔ **Disabled**   USB controllers are enabled

➔ **Enabled**   DEFAULT   USB controllers are disabled

➔ **USB 2.0 Controller [Enabled]**

The **USB 2.0 Controller** BIOS option enables or disables the USB 2.0 controller

➔ **Enabled**   DEFAULT   USB function enabled

➔ **Disabled**   USB function disabled

➔ **Legacy USB Support [Enabled]**

Use the **Legacy USB Support** BIOS option to enable USB mouse and USB keyboard support.

Normally if this option is not enabled, any attached USB mouse or USB keyboard does not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there is no USB driver loaded onto the system.

➔ **Disabled**   Legacy USB support disabled

➔ **Enabled**   DEFAULT   Legacy USB support enabled

➔ **Auto**   Legacy USB support disabled if no USB devices are connected

➔ **USB2.0 Controller Mode [HiSpeed]**

The **USB2.0 Controller Mode** BIOS option sets the speed of the USB2.0 controller.

➔ **FullSpeed**   The controller is capable of operating at full speed 12 Mb/s

➔ **HiSpeed**   DEFAULT   The controller is capable of operating at high speed 480 Mb/s

6.4 PCI/PnP

Use the PCI/PnP menu (BIOS Menu 13) to configure advanced PCI and PnP settings.

⚠️ **WARNING:**

Setting wrong values for the BIOS selections in the PCIPnP BIOS menu may cause the system to malfunction.

```
                        BIOS SETUP UTILITY
   Main     Advanced    PCIPnP    Boot    Security    Chipset    Exit

   Advanced PCI/PnP Settings                          Available: Specified
                                                      IRQ is available to
   WARNING: Setting wrong values in below sections    be use by PCI/PnP
            may cause system to malfunction           devices.
   IRQ3                          [Reserved]           Reserved: Specified
   IRQ4                          [Reserved]           IRQ is reserved for
   IRQ5                          [Available]          use by legacy ISA
   IRQ7                          [Reserved]           devices.
   IRQ9                          [Available]
   IRQ10                         [Available]
   IRQ11                         [Available]
   IRQ14                         [Available]
   IRQ15                         [Available]          ←→    Select Screen
                                                      ↑↓    Select Item
   DMA Channel 0                 [Available]          +-    Change Option
   DMA Channel 1                 [Available]          F1    General Help
   DMA Channel 3                 [Available]          F10   Save and Exit
   DMA Channel 5                 [Available]          ESC   Exit
   DMA Channel 6                 [Available]
   DMA Channel 7                 [Available]

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```

BIOS Menu 13: PCI/PnP Configuration

➔ **IRQ#   [Available]**

Use the **IRQ#** address to specify what IRQs can be assigned to a particular peripheral device.

➔ **Available**   D_{EFAULT}   The specified IRQ is available to be used by PCI/PnP devices

➔ **Reserved**   The specified IRQ is reserved for use by Legacy ISA devices

Available IRQ addresses are:

- IRQ3
- IRQ4
- IRQ5
- IRQ7
- IRQ9
- IRQ10
- IRQ 11
- IRQ 14
- IRQ 15

➔ **DMA Channel# [Available]**

Use the **DMA Channel#** option to assign a specific DMA channel to a particular PCI/PnP device.

➔ **Available**   D_{EFAULT}   The specified DMA is available to be used by PCI/PnP devices

➔ **Reserved**   The specified DMA is reserved for use by Legacy ISA devices

Available DMA Channels are:

- DM Channel 0
- DM Channel 1

- DM Channel 3
- DM Channel 5
- DM Channel 6
- DM Channel 7

6.5 Boot

Use the Boot menu (**BIOS Menu 14**) to configure system boot options.

```
                        BIOS SETUP UTILITY
  Main    Advanced    PCIPnP    Boot    Security    Chipset    Exit

  Boot Settings                              Configure Settings
  ─────────────────────────────             during System Boot
  ▶ Boot Settings Configuration

  ▶ Boot Device Priority
  ▶ Hard Disk Drives




                                            ←→     Select Screen
                                            ↑↓     Select Item
                                            Enter  Go to SubScreen
                                            F1     General Help
                                            F10    Save and Exit
                                            ESC    Exit

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```
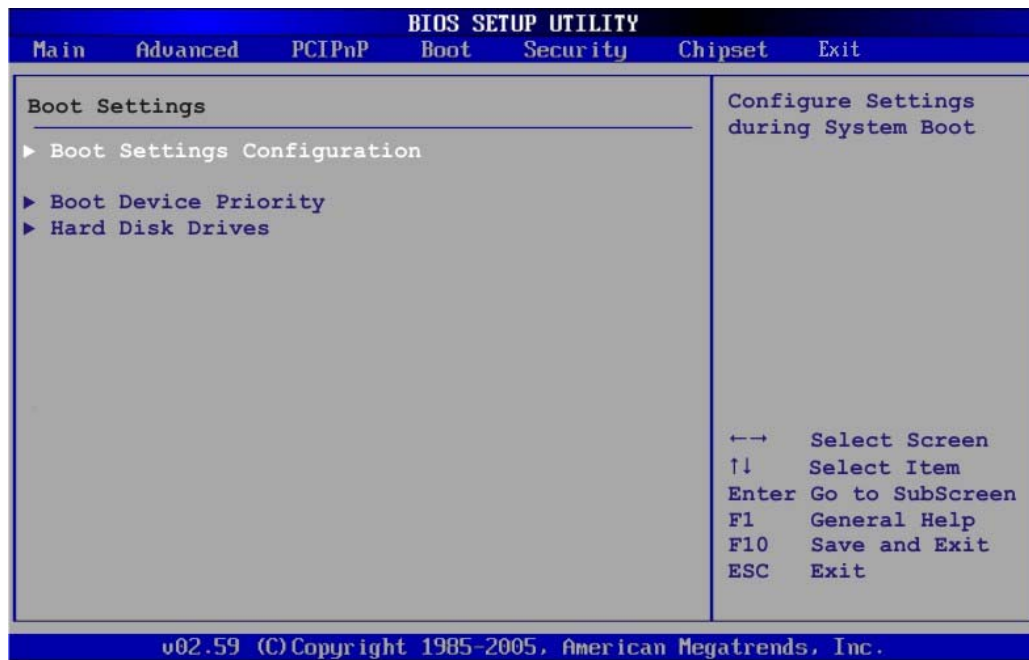
BIOS Menu 14: Boot

6.5.1 Boot Settings Configuration

Use the Boot Settings Configuration menu (BIOS Menu 14) to configure advanced system boot options.
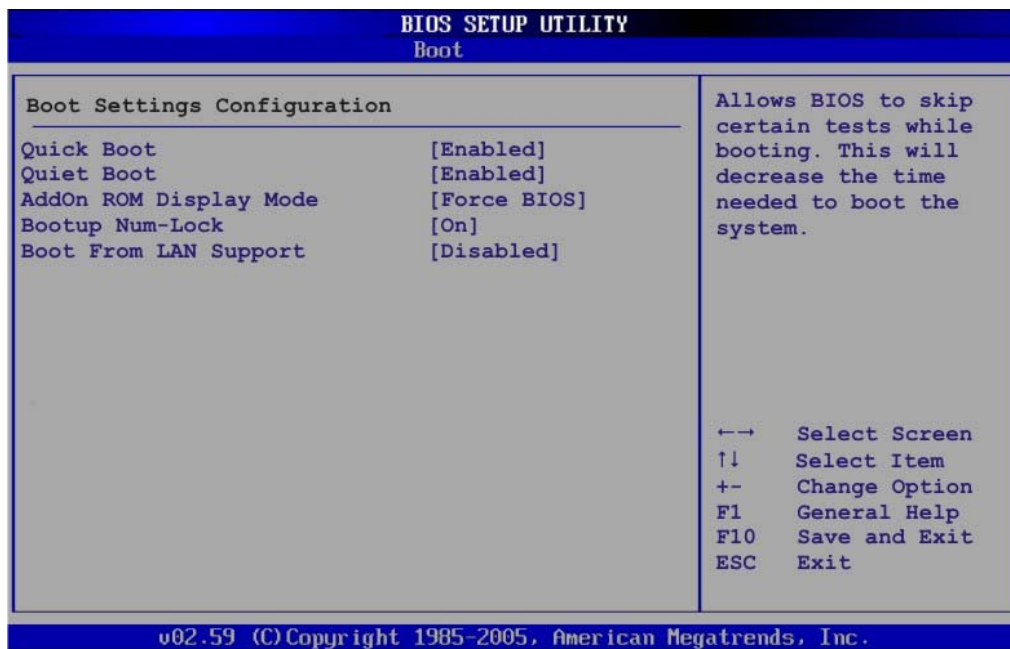
BIOS Menu 15: Boot Settings Configuration

➔ **Quick Boot [Enabled]**

Use the **Quick Boot** BIOS option to make the computer speed up the boot process.

➔ **Disabled** No POST procedures are skipped

➔ **Enabled** DEFAULT Some POST procedures are skipped to decrease the system boot time

➔ **Quiet Boot [Disabled]**

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

➔ **Disabled** DEFAULT Normal POST messages displayed

➔ **Enabled** OEM Logo displayed instead of POST messages

➔ **AddOn ROM Display Mode [Force BIOS]**

The **AddOn ROM Display Mode** option allows add-on ROM (read-only memory) messages to be displayed.

➔ **Force BIOS** DEFAULT Allows the computer system to force a third party BIOS to display during system boot.

➔ **Keep Current** Allows the computer system to display the information during system boot.

➔ **Bootup Num-Lock [On]**

The **Bootup Num-Lock** BIOS option allows the Number Lock setting to be modified during boot up.

➔ **Off** Does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard lights up when the Number Lock is engaged.

➔ **On** DEFAULT Allows the Number Lock on the keyboard to be enabled automatically when the computer system boots up. This allows the immediate use of the 10-key numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard is lit.

➔ **Boot From LAN Support [Disabled]**

The **BOOT From LAN Support** option enables the system to be booted from a remote system.

→ **Enabled**   Can be booted from a remote system through the LAN

→ **Disabled**   DEFAULT   Cannot be booted from a remote system through the LAN

6.5.2 Boot Device Priority

Use the **Boot Device Priority** menu (**BIOS Menu 16**) to specify the boot sequence from the available devices. The following options are available:

- 1st Boot Device
- 2nd Boot Device
- 3rd Boot Device

```
                          BIOS SETUP UTILITY
                               Boot

 Boot Device Priority                                  Specifies the boot
                                                       sequence from the
 1st Boot Device             [USB:Generic Flash ]      available devices.
 2nd Boot Device             [CD/DVD:PS-TEAC DV-]
 3rd Boot Device             [Network:MBA v9.0.1]      A device enclosed in
                                                       parenthesis has been
                                                       disabled in the
                                                       corresponding type
                                                       menu.



                                                       ←    Select Screen
                                                       ↑↓   Select Item
                                                       +-   Change Option
                                                       F1   General Help
                                                       F10  Save and Exit
                                                       ESC  Exit

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```

BIOS Menu 16: Boot Device Priority Settings

6.6 Security

Use the Security menu (BIOS Menu 17) to set system and user passwords.

```
                      BIOS SETUP UTILITY
  Main    Advanced   PCIPnP    Boot   Security   Chipset   Exit

  Security Settings                             Configure Settings
                                                during System Boot
  Supervisor Password :Not Installed
  User Password       :Not Installed

  Change Supervisor Password
  Change User Password




                                                ←→    Select Screen
                                                ↑↓    Select Item
                                                Enter Change
                                                F1    General Help
                                                F10   Save and Exit
                                                ESC   Exit

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```

BIOS Menu 17: Security

➔ **Change Supervisor Password**

Use the **Change Supervisor Password** to set or change a supervisor password. The default for this option is **Not Installed**. If a supervisor password must be installed, select this field and enter the password. After the password has been added, **Install** appears next to **Change Supervisor Password**.

➔ **Change User Password**

Use the **Change User Password** to set or change a user password. The default for this option is **Not Installed**. If a user password must be installed, select this field and enter the password. After the password has been added, **Install** appears next to **Change User Password**.

6.7 Chipset

Use the **Chipset** menu (**BIOS Menu 18**) to access the NorthBridge and SouthBridge configuration menus

WARNING!

Setting the wrong values for the Chipset BIOS selections in the Chipset BIOS menu may cause the system to malfunction.
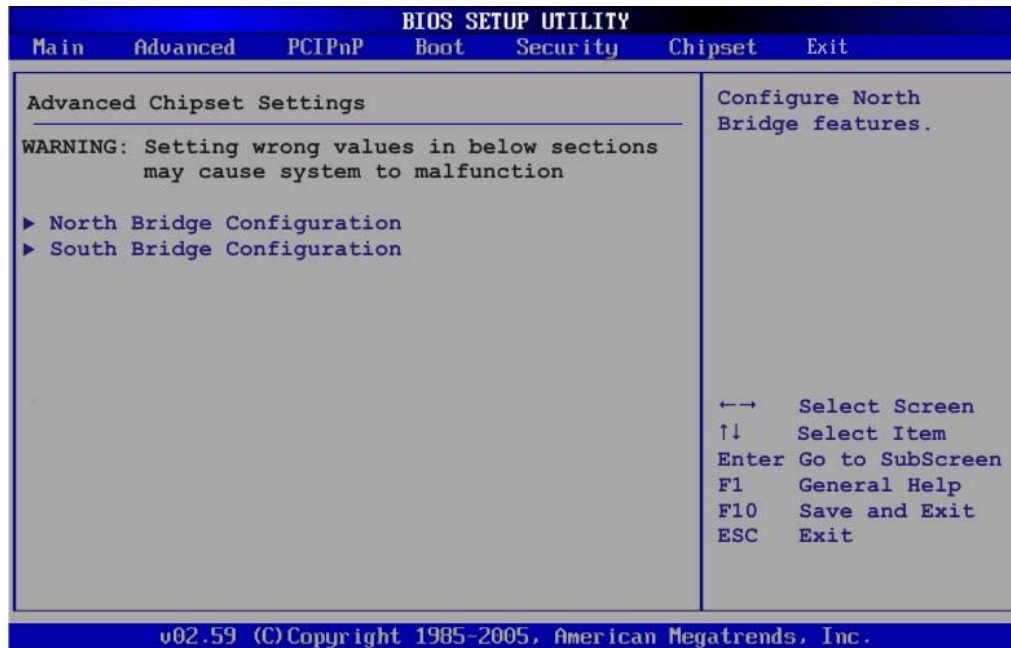
BIOS Menu 18: Chipset

6.7.1 North Bridge Chipset Configuration

Use the **North Bridge Chipset Configuration** menu (BIOS Menu 18) to configure the Northbridge chipset settings.
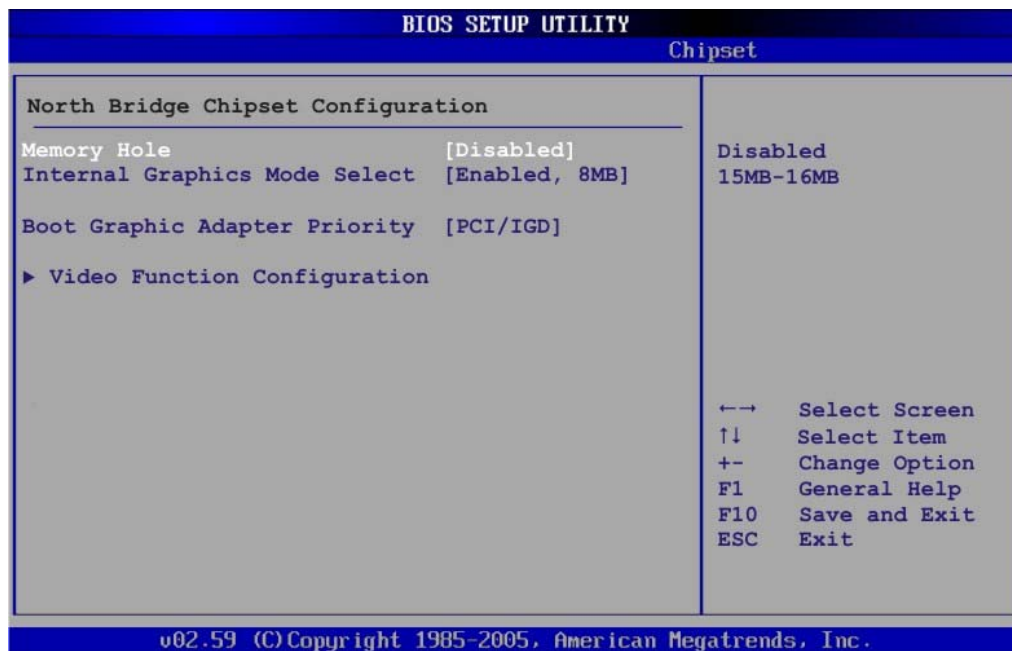
BIOS Menu 19:North Bridge Chipset Configuration

➔ **Memory Hole [Disabled]**

The **Memory Hole** reserves the memory space between 15MB and 16MB for ISA expansion cards that require a specified area of memory to work properly. If an older ISA expansion card is used, please refer to the documentation that came with the card to see if it is necessary to reserve the space.

➔ **Disabled** **DEFAULT** Memory is not reserved for ISA expansion cards

➔ **Enabled** Memory is reserved for ISA expansion cards

➔ **Internal Graphics Mode Select [Enable, 8MB]**

The **Internal Graphic Mode Select** option determines the amount of system memory that can be used by the Internal graphics device.

➔ **Disable**

➔ **Enable, 1MB** 1MB of memory used by internal graphics device

➔ **Enable, 8MB**   DEFAULT   8MB of memory used by internal graphics device

➔ **Boots Graphics Adapter Priority [PCI/IGD]**

Use the **Boots Graphics Adapter** option to select the graphics controller used as the primary boot device. Select either an integrated graphics controller (IGD) or a combination of PCI graphics controller, a PCI express (PEG) controller or an IGD. Configuration options are listed below:

- IGD
- PCI/IGD   DEFAULT

6.7.1.1 Video Function Configuration

Use the **Video Function Configuration** menu to configure the video device connected to the system.

➔ **DVMT Mode Select [DVMT Mode]**

Use the **DVMT Mode Select** option to select the Intel Dynamic Video Memory Technology (DVMT) operating mode.

➔ **Fixed Mode**   A fixed portion of graphics memory is reserved as graphics memory.

➔ **DVMT Mode** DEFAULT   Graphics memory is dynamically allocated according to the system and graphics needs.

➔ **Combo Mode**   A fixed portion of graphics memory is reserved as graphics memory. If more memory is needed, graphics memory is dynamically allocated according to the system and graphics needs.

➔ **DVMT/FIXED Memory**

Use the **DVMT/FIXED Memory** option to specify the maximum amount of memory that can be allocated as graphics memory. This option can only be configured for if **DVMT Mode** or **Fixed Mode** is selected in the **DVMT Mode Selec**t option. If **Combo Mode** is selected, the maximum amount of graphics memory is 128MB. Configuration options are listed below.

- 64MB
- 128MB   **DEFAULT**
- Maximum DVMT

➔ **Boot Display Device [CRT]**

Use the **Boot Display Device** option to select the display device used by the system when it boots. Configuration options are listed below.

- CRT   **DEFAULT**
- TV
- LVDS

6.7.2 SouthBridge Configuration

The **SouthBridge Configuration** menu (**BIOS Menu 20**) the southbridge chipset to be configured.

```
                        BIOS SETUP UTILITY
                                        Chipset

South Bridge Chipset Configuration
                                            Azalia
Audio Controller              [All Disabled]     Ac'97 Audio Only
Spread Spectrum Mode          [Disabled]         All Disabled




                                         ←→    Select Screen
                                         ↑↓    Select Item
                                         +-    Change Option
                                         F1    General Help
                                         F10   Save and Exit
                                         ESC   Exit



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```
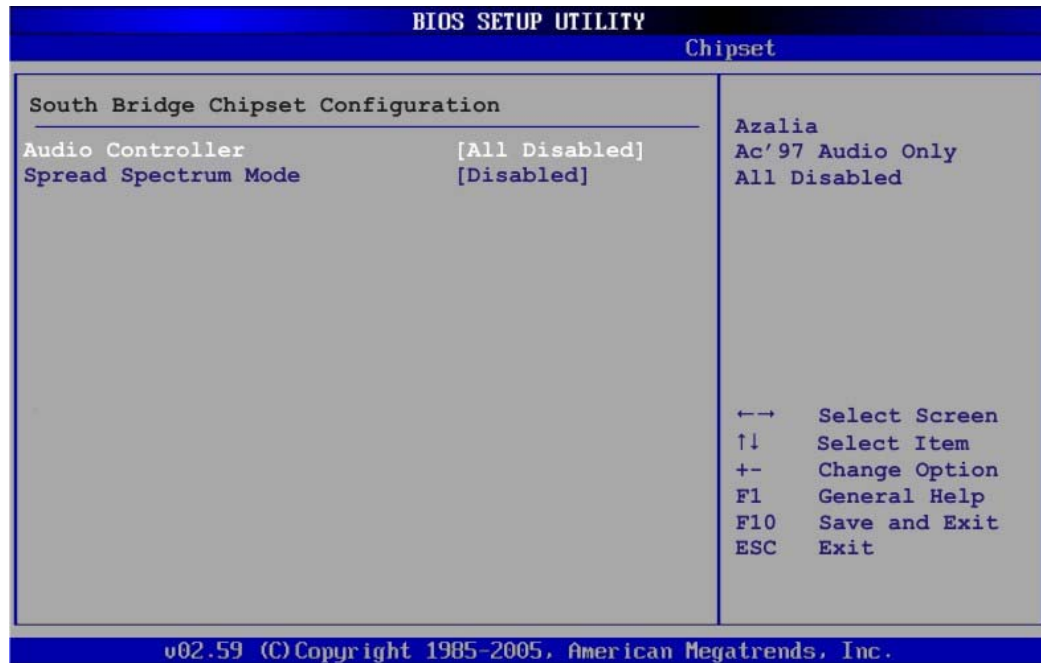
BIOS Menu 20:SouthBridge Chipset Configuration

➔ **Audio Controller [All Disabled]**

The **Audio Controller** option enables or disables the audio controller.

➔ **Azalia**   Audio controller configured as Azalia

➔ **AC'97 Audio Only**   The on-board AC'97 audio controller is enabled.

➔ **All Disabled**   DEFAULT   The on-board audio controller is disabled.

➔ **Spread Spectrum [Disabled]**

Use the **Spread Spectrum** option to reduce the EMI. Excess EMI is generated when the system clock generator pulses have extreme values. Spreading the pulse spectrum modulates changes in the extreme values from spikes to flat curves, thus reducing the EMI. This benefit may in some cases be outweighed by problems with timing-critical devices, such as a clock-sensitive SCSI device.

➔ **Disabled**   DEFAULT   EMI not reduced

➔ **Enabled**   EMI reduced

6.8 Exit

Use the **Exit** menu (**BIOS Menu 21**) to load default BIOS values, optimal failsafe values and to save configuration changes.


```
                        BIOS SETUP UTILITY
  Main    Advanced   PCIPnP    Boot    Security   Chipset    Exit

  Exit Options                                    Exit system setup
  ─────────────────────────────────              after saving the
  Save Changes and Exit                          changes.
  Discard Changes and Exit
  Discard Changes                                F10 key can be used
                                                 for this operation.
  Load Optimal Defaults
  Load Failsafe Defaults



                                                 ←→    Select Screen
                                                 ↑↓    Select Item
                                                 Enter Go to SubScreen
                                                 F1    General Help
                                                 F10   Save and Exit
                                                 ESC   Exit

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```

BIOS Menu 21:Exit

➔ **Save Changes and Exit**

Use the **Save Changes and Exit** option to save the changes made to the BIOS options and to exit the BIOS configuration setup program.

➔ **Discard Changes and Exit**

Use the **Discard Changes and Exit** option to exit the BIOS configuration setup program without saving the changes made to the system.

➔ **Discard Changes**

Use the **Discard Changes** option to discard the changes and remain in the BIOS configuration setup program.

➔ **Load Optimal Defaults**

Use the **Load Optimal Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F9 key can be used for this operation.**

➔ **Load Failsafe Defaults**

Use the **Load Failsafe Defaults** option to load failsafe default values for each of the parameters on the Setup menus. **F8 key can be used for this operation.**

Chapter

7

Software Drivers

7.1 Available Software Drivers

![NOTE icon] **NOTE:**

The content of the CD may vary throughout the life cycle of the product and is subject to change without prior notice. Visit the IEI website or contact technical support for the latest updates.

The following drivers can be installed on the system:

- Chipset
- VGA
- LAN
- Audio

Installation instructions are given below.

7.2 Starting the Driver Program

To access the driver installation programs, please do the following.

Step 1: Insert the CD-ROM that came with the system into a CD-ROM drive attached to the system.

Step 2: The screen in **Figure 7-1** appears.
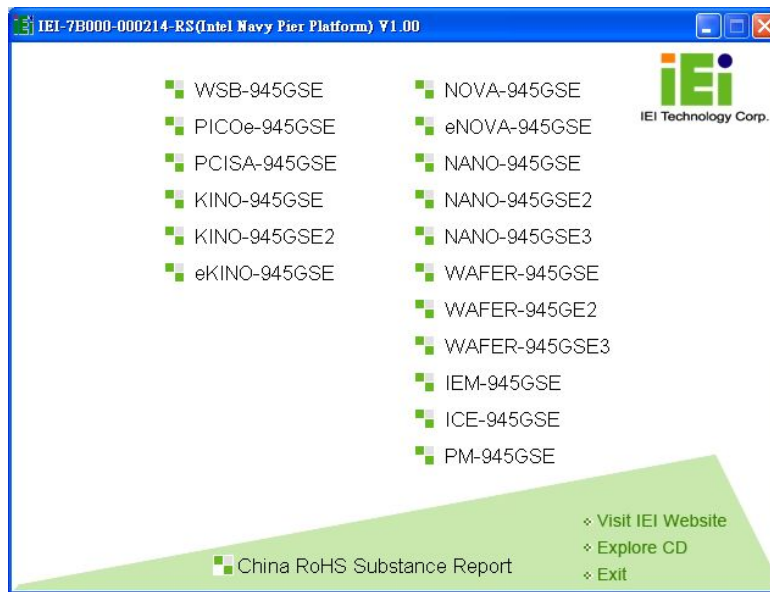
Figure 7-1: Start Up Screen

Step 3: Click **PICOe-945GSE**.

Step 4: The screen in appears.
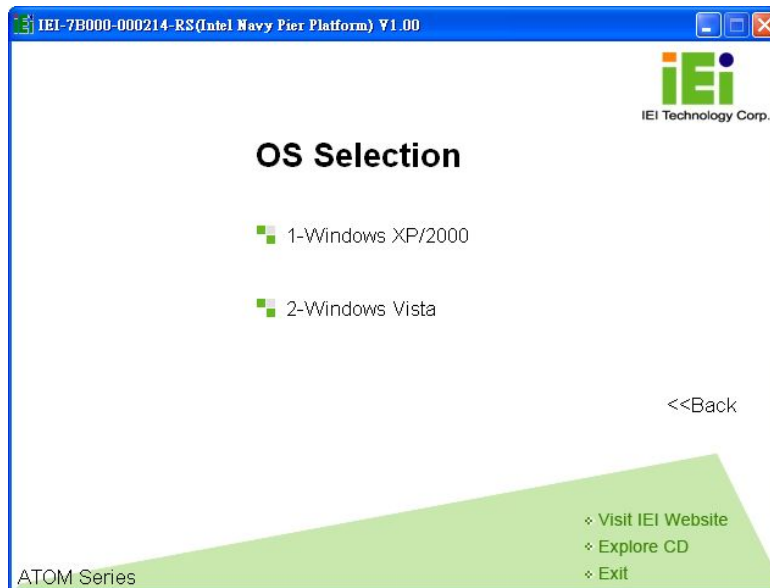
Figure 7-2: Select Operating System

Step 5: Select the operating system installed on the PICOe-945GSE system. This

manual describes the installation for a **Windows XP** operating system.

Step 6: The list of drivers in **Figure 7-3** appears.
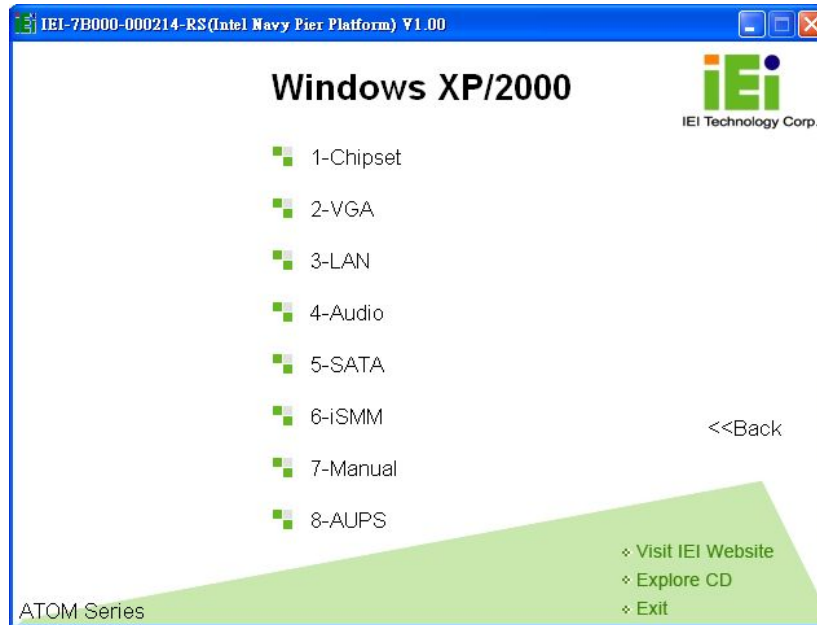
Figure 7-3: Drivers

7.3 Chipset Driver Installation

To install the chipset driver, please do the following.

Step 1: Access the driver list shown in **Figure 7-3**. (See **Section 7.2**)

Step 2: Click "**1-Chipset Driver**"

Step 3: The setup files are extracted as shown in **Figure 7-4**.

Figure 7-4: Chipset Driver Screen

Step 4: When the setup files are completely extracted the **Welcome Screen** in **Figure 7-5** appears.

Figure 7-5: Chipset Driver Welcome Screen

Step 5: Click **Next** to continue.

Step 6: The license agreement in **Figure 7-6** appears.

Step 7: Read the **License Agreement**.

Step 8: Click the **Yes** icon to continue.

Figure 7-6: Chipset Driver License Agreement

Step 9: The Read Me file in **Figure 7-7** appears.

Step 10: Click **Next** to continue.

Figure 7-7: Chipset Driver Read Me File

Step 11: **Setup Operations** are performed as shown in **Figure 7-8**.

Figure 7-8: Chipset Driver Setup Operations

Step 12: Once the **Setup Operations** are complete, click the **Next** icon to continue.

Step 13: The **Finish** screen appears.

Step 14: Select "**Yes, I want to restart the computer now**" and click the **Finish** icon.

See **Figure 7-9**.

Figure 7-9: Chipset Driver Installation Finish Screen

7.4 VGA Driver Installation

To install the VGA driver, please do the following.

Step 1: Access the driver list shown in **Figure 7-3**. (See **Section 7.2**)

Step 2: Click "**2-VGA**"

Step 3: The VGA Read Me file in **Figure 7-10** appears.

Step 4: Click **Next** to continue.
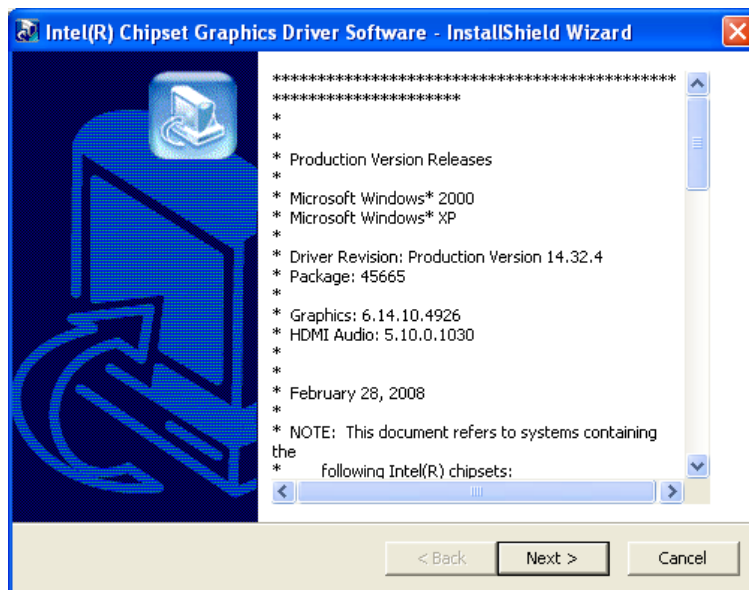
Figure 7-10: VGA Driver Read Me File

Step 5: The installation files are extracted. See **Figure 7-11**.
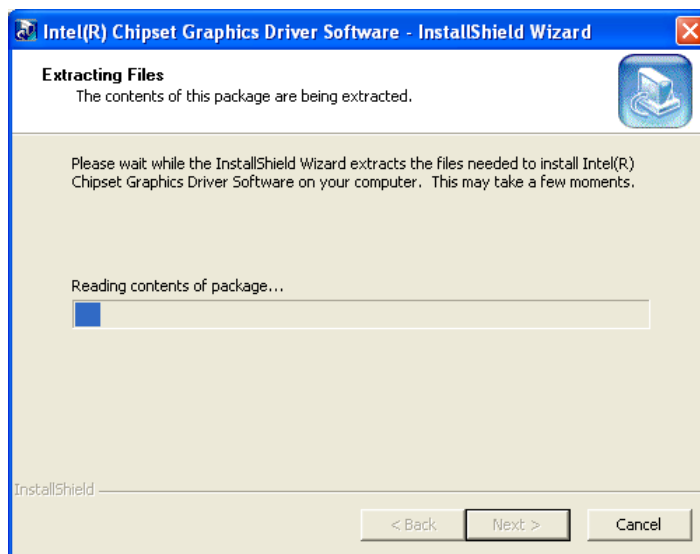
Figure 7-11: VGA Driver Setup Files Extracted

Step 6: The **Welcome Screen** in **Figure 7-12** appears.

Figure 7-12: VGA Driver Welcome Screen

Step 7: Click **Next** to continue.

Step 8: The license agreement in **Figure 7-13** appears.

Step 9: Read the **License Agreement**.

Step 10: Click the **Yes** icon to continue.
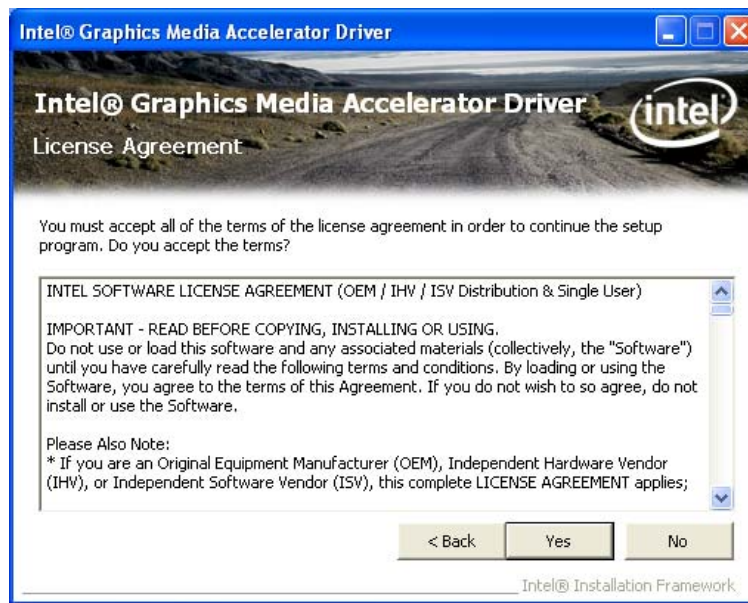
Figure 7-13: VGA Driver License Agreement

Step 11: The Read Me file in **Figure 7-14** appears.

Step 12: Click **Next** to continue.
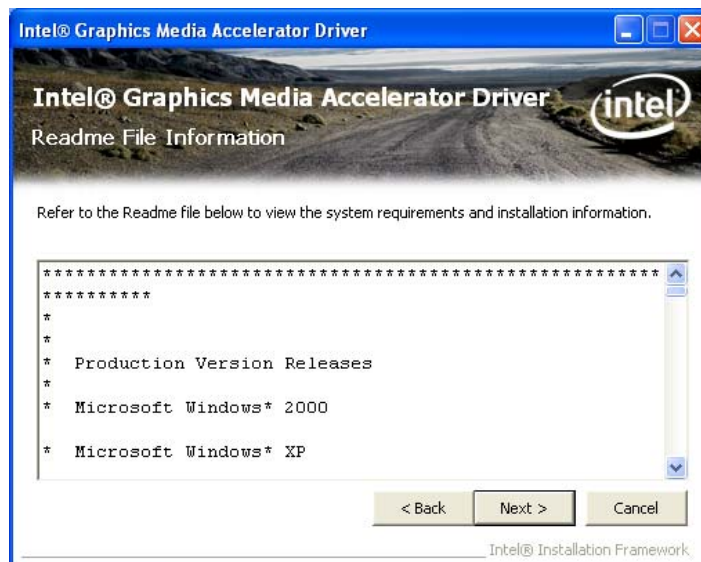
Figure 7-14: VGA Driver Read Me File

Step 13: **Setup Operations** are performed as shown in **Figure 7-15**.
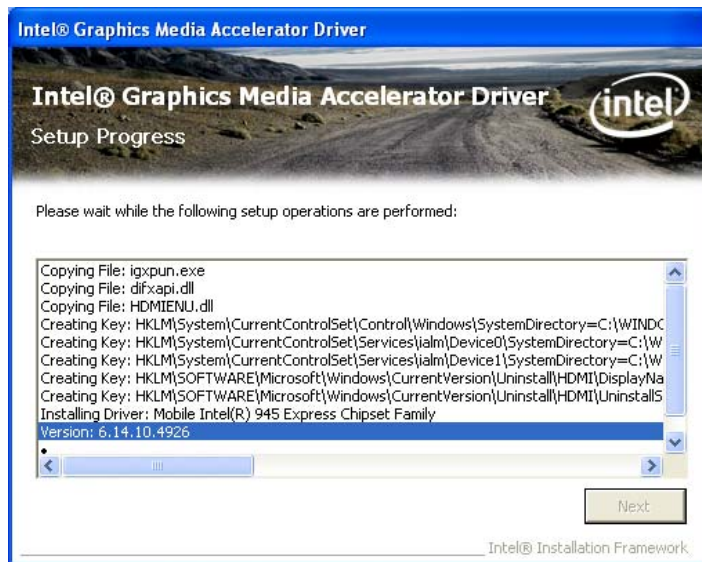
Figure 7-15: VGA Driver Setup Operations

Step 14: Once the **Setup Operations** are complete, click the **Next** icon to continue.

Step 15: The **Finish** screen appears.

Step 16: Select "**Yes, I want to restart the computer now**" and click the **Finish** icon.

See **Figure 7-16**.
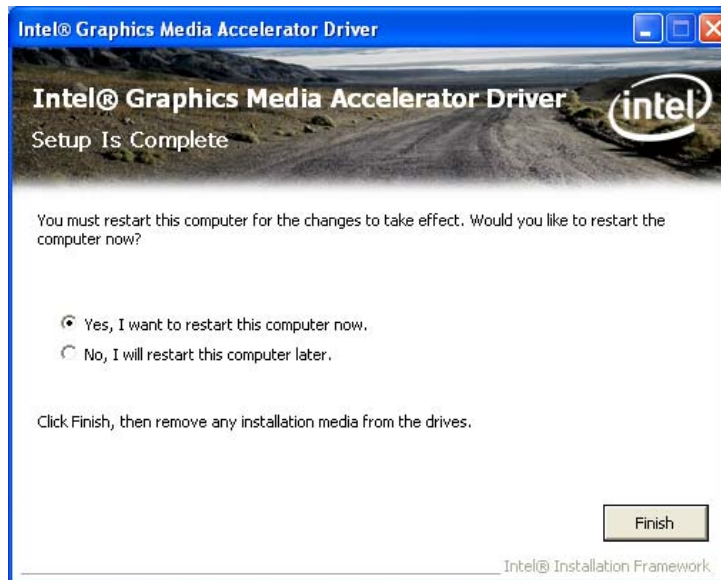
Figure 7-16: VGA Driver Installation Finish Screen

7.5 LAN Driver Installation

To install the chipset driver, please do the following.

Step 1: Access the driver list shown in **Figure 7-3**. (See **Section 7.2**)

Step 2: Click "**3-LAN**"

Step 3: The **Welcome** screen in **Figure 7-17** appears.
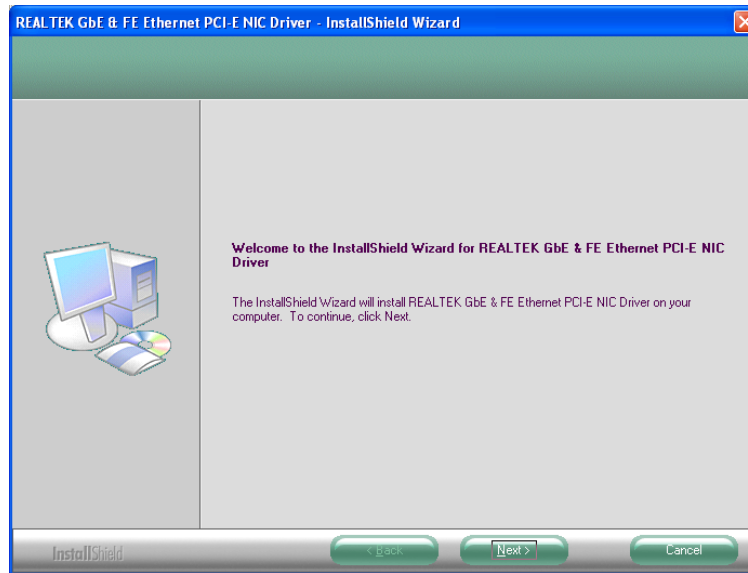
Figure 7-17: LAN Driver Welcome Screen

Step 4: Click **Next** to continue.

Step 5: The **Ready to Install** screen in **Figure 7-18** appears.

Step 6: Click **Next** to proceed with the installation.
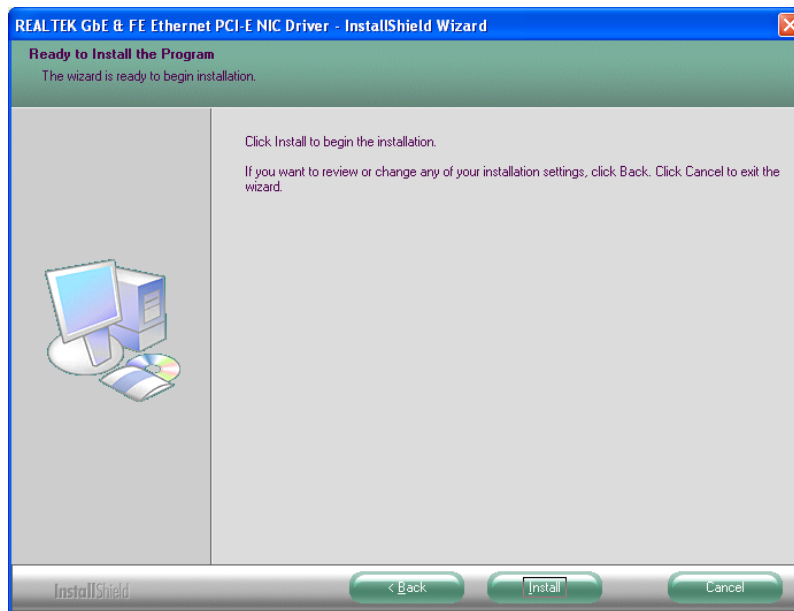
Figure 7-18: LAN Driver Welcome Screen

Step 7: The program begins to install.

Step 8: The installation progress can be monitored in the progress bar shown in **Figure 7-19**.
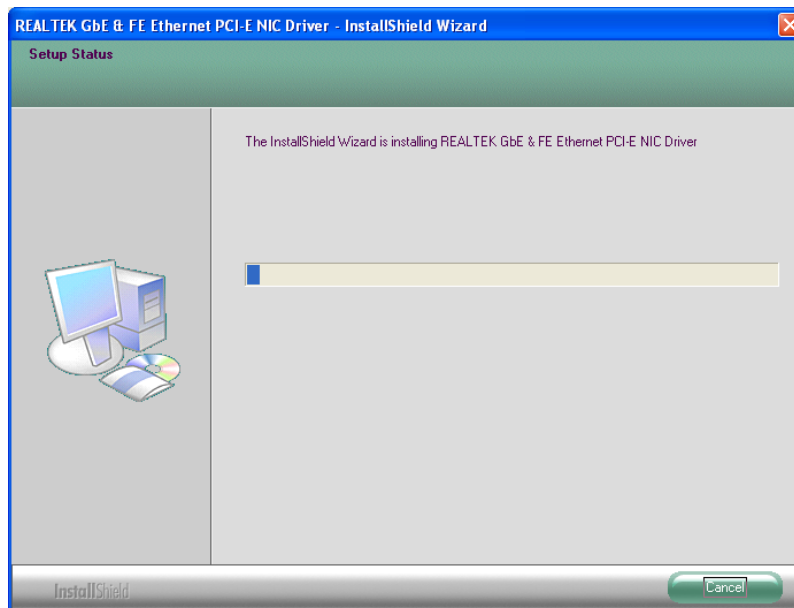
Figure 7-19: LAN Driver Installation

Step 9: When the driver installation is complete, the screen in **Figure 7-20** appears.
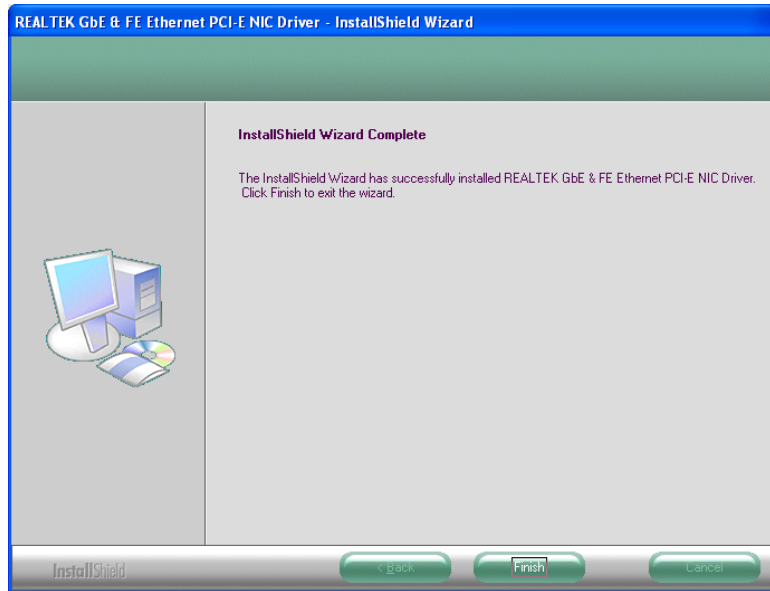
Figure 7-20: LAN Driver Installation Complete

7.6 Audio Driver Installation

To install the chipset driver, please do the following.

Step 1: Access the driver list shown in **Figure 7-3**. (See **Section 7.2**)

Step 2: Click "**4-Audio**"

Step 3: The screen in **Figure 7-21** appears.
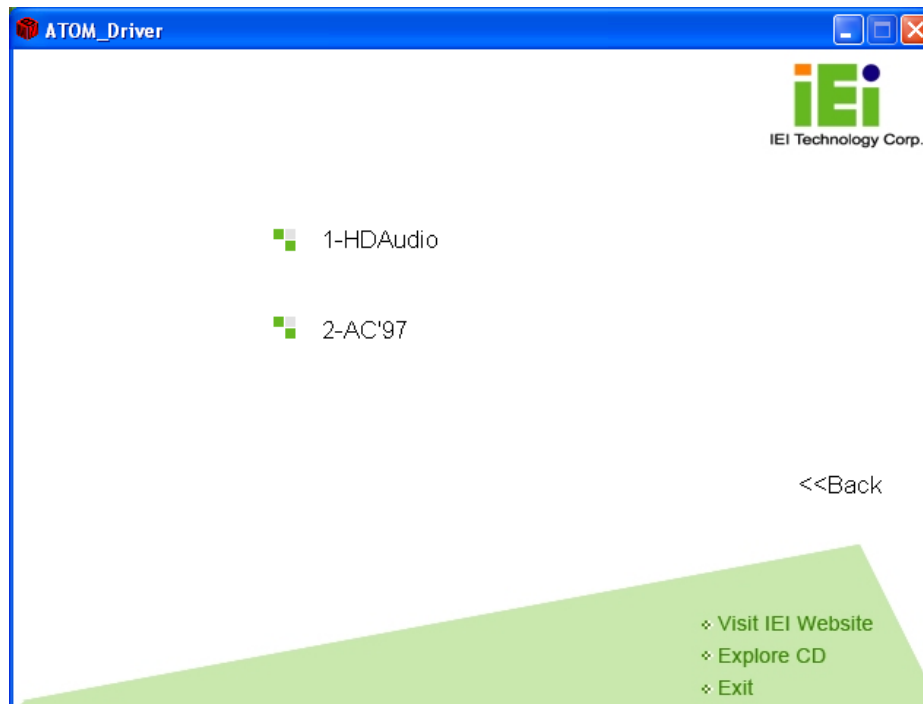
Figure 7-21: Audio Driver Options

7.6.1 HD Audio Installation

To install the HD Audio driver, please do the following:

Step 1: Select "**1-HDAudio**" in Figure 7-21.

Step 2: Installation files are extracted as shown in **Figure 7-22**.

Figure 7-22: Extract HD Audio Driver Installation Files

Step 3:   The **Welcome** screen in **Figure 7-23** appears.
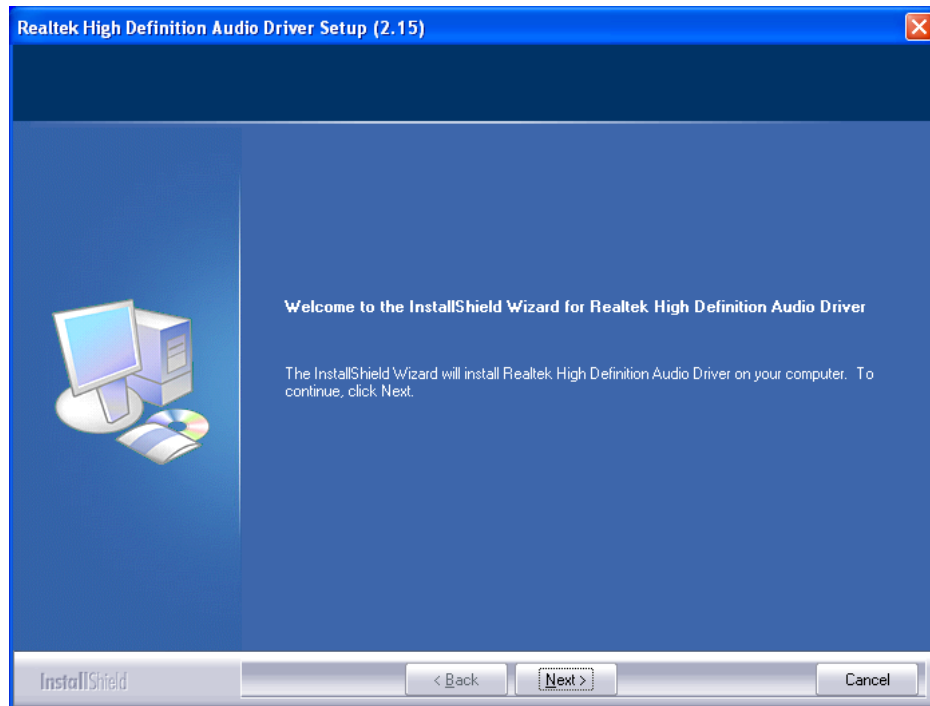
Figure 7-23: HD Audio Driver Welcome Screen

Step 4: Click **Next** to continue.

Step 5: The system updates. See **Figure 7-24**.
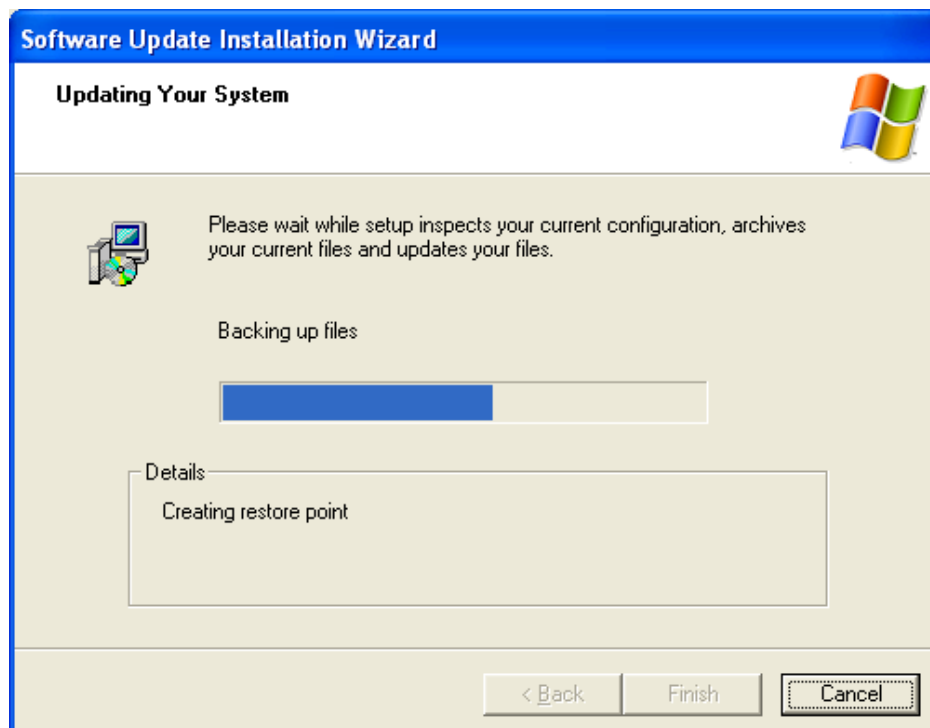
Figure 7-24: System Update

Step 6: Follow the installation instructions until the HD Audio driver installation is

complete.

7.6.2 AC'97 Driver Installation

To install the AC'97 audio driver, please do the following:

Step 1: Select "**2-AC'97**" in **Figure 7-21**

Step 2: The installation files are extracted as shown in **Figure 7-25**.
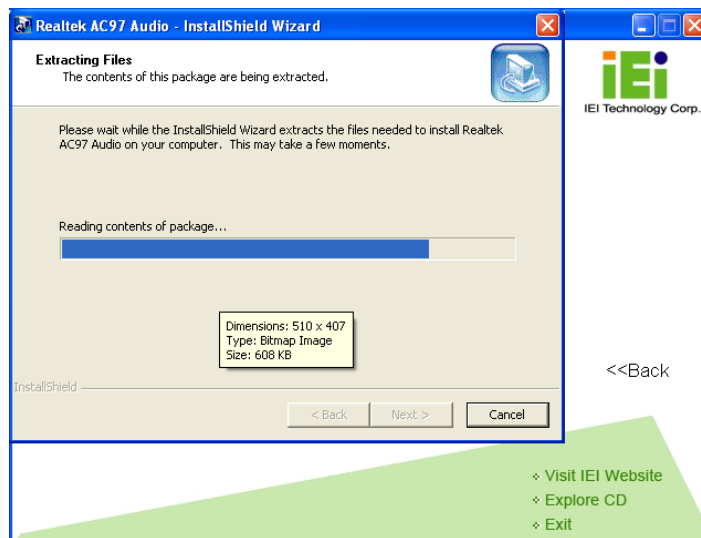
Figure 7-25: AC'97 Driver Installation File Extraction

Step 3: The AC'97 Driver Installation screen in **Figure 7-26** appears.

Step 4: Click **Next** to continue.
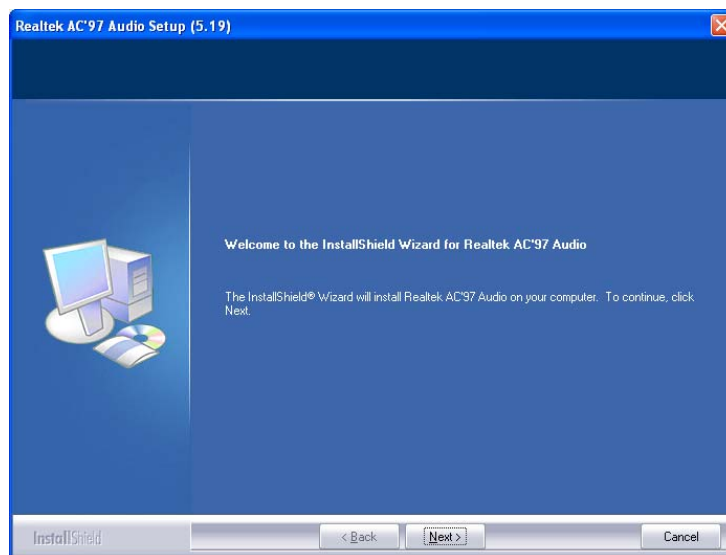
Figure 7-26: AC'97 Driver Installation Welcome Screen

Step 5: The Verification window in **Figure 7-27** may appear.

Step 6: Click "**Continue Anyway**."

Figure 7-27: AC'97 Driver Installation Verification

Step 7: The driver installation begins. See **Figure 7-28**.
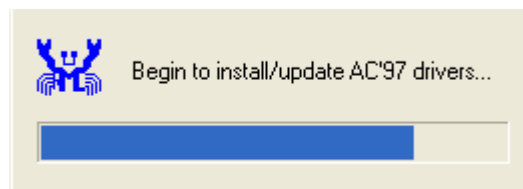
Figure 7-28: AC'97 Driver Installation

Step 8: When the driver is installed, the driver installation finish screen in **Figure 7-29** appears.

Step 9: Select "**Yes, I wish to restart my computer now**" And click **Finish**
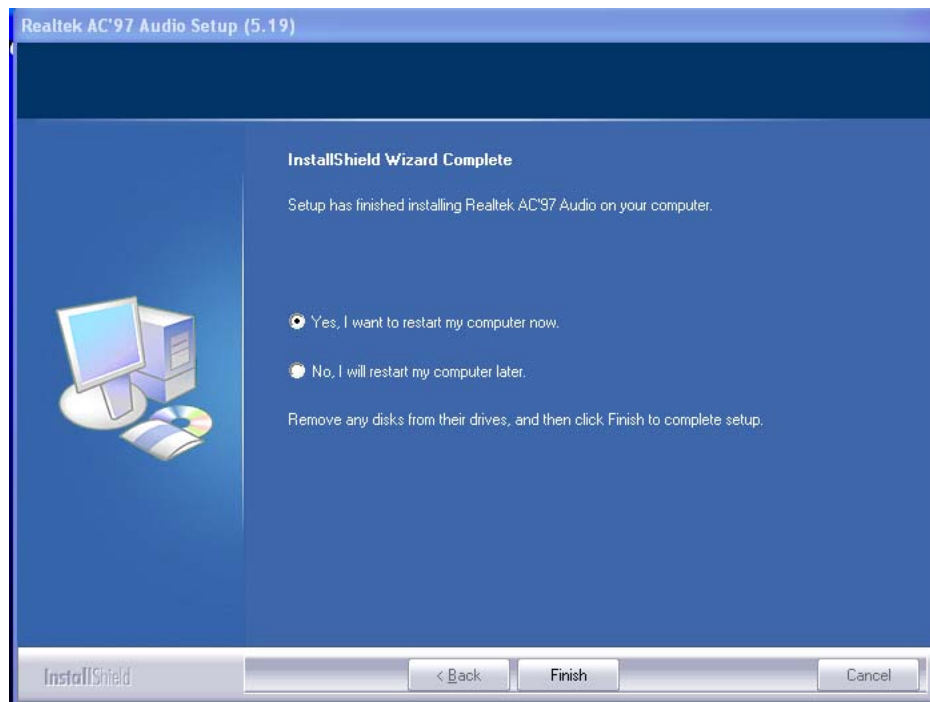
Figure 7-29: AC'97 Driver Installation Complete

Step 10: The system reboots.

Appendix

A

BIOS Menu Options

Appendix

B

Terminology

AC '97   Audio Codec 97 (AC'97) refers to a codec standard developed by

Intel® in 1997.

ACPI   Advanced Configuration and Power Interface (ACPI) is an OS-directed

configuration, power management, and thermal management interface.

AHCI   Advanced Host Controller Interface (AHCI) is a SATA Host controller

register-level interface.

ATA   The Advanced Technology Attachment (ATA) interface connects

storage devices including hard disks and CD-ROM drives to a

computer.

APM   The Advanced Power Management (APM) application program

interface (API) enables the inclusion of power management in the

BIOS.

ARMD   An ATAPI Removable Media Device (ARMD) is any ATAPI device that

supports removable media, besides CD and DVD drives.

ASKIR   Amplitude Shift Keyed Infrared (ASKIR) is a form of modulation that

represents a digital signal by varying the amplitude ("volume") of the

signal. A low amplitude signal represents a binary 0, while a high

amplitude signal represents a binary 1.

BIOS   The Basic Input/Output System (BIOS) is firmware that is first run when

the computer is turned on and can be configured by the end user

CODEC   The Compressor-Decompressor (CODEC) encodes and decodes

digital audio data on the system.

CMOS   Complimentary metal-oxide-conductor is a type of integrated circuit

used in chips like static RAM and microprocessors.

COM   COM is used to refer to serial ports. Serial ports offer serial

communication to expansion devices. The serial port on a personal

	computer is usually a male DE-9 connector.
DAC	The Digital-to-Analog Converter (DAC) converts digital signals to analog signals.
DDR	Double Data Rate refers to a data bus transferring data on both the rising and falling edges of the clock signal.
DMA	Direct Memory Access (DMA) enables some peripheral devices to bypass the system processor and communicate directly with the system memory.
DIMM	Dual Inline Memory Modules are a type of RAM that offer a 64-bit data bus and have separate electrical contacts on each side of the module.
EHCI	The Enhanced Host Controller Interface (EHCI) specification is a register-level interface description for USB 2.0 Host Controllers.
FSB	The Front Side Bus (FSB) is the bi-directional communication channel between the processor and the Northbridge chipset.
GbE	Gigabit Ethernet (GbE) is an Ethernet version that transfers data at 1.0 Gbps and complies with the IEEE 802.3-2005 standard.
GPIO	General purpose input
IrDA	Infrared Data Association (IrDA) specify infrared data transmission protocols used to enable electronic devices to wirelessly communicate with each other.
L1 Cache	The Level 1 Cache (L1 Cache) is a small memory cache built into the system processor.
L2 Cache	The Level 2 Cache (L2 Cache) is an external processor memory cache.
LVDS	Low-voltage differential signaling (LVDS) is a dual-wire, high-speed differential electrical signaling system commonly used to connect LCD displays to a computer.

MAC	The Media Access Control (MAC) protocol enables several terminals or network nodes to communicate in a LAN, or other multipoint networks.
PCIe	PCI Express (PCIe) is a communications bus that uses dual data lines for full-duplex (two-way) serial (point-to-point) communications between the SBC components and/or expansion cards and the SBC chipsets. Each line has a 2.5 Gbps data transmission rate and a 250 MBps sustained data transfer rate.
POST	The Power-on Self Test (POST) is the pre-boot actions the system performs when the system is turned-on.
QVGA	Quarter Video Graphics Array (QVGA) refers to a display with a resolution of 320 x 240 pixels.
RAID	Redundant Array of Inexpensive Disks (RAID) refers to redundantly backing up data on multiple disks to ensure that if one disk fails, the data is not lost and can be restored from the remaining disks in the array.
RAM	Random Access Memory (RAM) is a form of storage used in computer. RAM is volatile memory, so it loses its data when power is lost. RAM has very fast data transfer rates compared to other storage like hard drives.
SATA	Serial ATA (SATA) is a serial communications bus designed for data transfers between storage devices and the computer chipsets. The SATA bus has transfer speeds up to 1.5 Gbps and the SATA II bus has data transfer speeds of up to 3.0 Gbps.
S.M.A.R.T	Self Monitoring Analysis and Reporting Technology (S.M.A.R.T) refers to automatic status checking technology implemented on hard disk drives.
UART	Universal Asynchronous Receiver-transmitter (UART) is responsible for

asynchronous communications on the system and manages the

system's serial communication (COM) ports.

UHCI The Universal Host Controller Interface (UHCI) specification is a

register-level interface description for USB 1.1 Host Controllers.

USB The Universal Serial Bus (USB) is an external bus standard for

interfacing devices. USB 1.1 supports 12Mbps data transfer rates, while

USB 2.0 supports 480Mbps data transfer rates.

VGA The Video Graphics Array (VGA) is a graphics display system

developed by IBM.

Appendix

C

DIO Interface

C.1 DIO Interface Introduction

The DIO connector on the PICOe-945GSE is interfaced to GPIO ports on the ITE IT8718F Super I/O chipset. The DIO has both 4-bit digital inputs and 4-bit digital outputs. The digital inputs and digital outputs are generally control signals that control the on/off circuit of external devices or TTL devices. Data can be read or written to the selected address to enable the DIO functions.

NOTE:

For further information, please refer to the datasheet for the Winbond W83697HG Super I/O chipset.

C.2 DIO Connector Pinouts

The following table describes how the DIO connector pins are connected to the Super I/O GPIO port.

Pin	Description	Super I/O Pin	Super I/O Pin Description
1	Ground	N/A	N/A
2	VCC	N/A	N/A
3	Output 3	GP23	General Purpose I/O Port 2 Bit 3
4	Output 2	GP22	General Purpose I/O Port 2 Bit 2
5	Output 1	GP21	General Purpose I/O Port 2 Bit 1
6	Output 0	GP20	General Purpose I/O Port 2 Bit 0
7	Input 3	GP33	General Purpose I/O 33
8	Input 2	GP32	General Purpose I/O 32
9	Input 1	GP31	General Purpose I/O 31
10	Input 0	GP30	General Purpose I/O 30

C.3 Assembly Language Samples

C.3.1 Enable the DIO Input Function

The BIOS interrupt call INT 15H controls the digital I/O. An assembly program to enable digital I/O input functions is listed below.

MOV	AX, 6F08H	Sets the digital port as input
INT	15H	Initiates the INT 15H BIOS call

C.3.2 Enable the DIO Output Function

The BIOS interrupt call INT 15H controls the digital I/O. An assembly program to enable digital I/O output functions is listed below.

MOV	AX, 6F09H	Sets the digital port as output
MOV	BL, 09H	
INT	15H	Initiates the INT 15H BIOS call

Appendix

D

Watchdog Timer

NOTE:

The following discussion applies to DOS environment.　IEI support is contacted or the IEI website visited for specific drivers for more sophisticated operating systems, e.g., Windows and Linux.

The Watchdog Timer is provided to ensure that standalone systems can always recover from catastrophic conditions that cause the CPU to crash. This condition may have occurred by external EMI or a software bug. When the CPU stops working correctly, Watchdog Timer either performs a hardware reset (cold boot) or a Non-Maskable Interrupt (NMI) to bring the system back to a known state.

A BIOS function call (INT 15H) is used to control the Watchdog Timer:

INT 15H:

AH – 6FH Sub-function:	
AL – 2:	Sets the Watchdog Timer's period.
BL:	Time-out value (Its unit-second is dependent on the item "Watchdog Timer unit select" in CMOS setup).

Table D-1: AH-6FH Sub-function

Call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. While the timer value reaches zero, the system resets. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the Watchdog timer is disabled if the time-out value is set to zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.

NOTE:

When exiting a program it is necessary to disable the Watchdog Timer, otherwise the system resets.

Example program:

; **INITIAL TIMER PERIOD COUNTER**

;

W_LOOP:

        MOV   AX, 6F02H   ;setting the time-out value

        MOV   BL, 30   ;time-out value is 48 seconds

        INT   15H

 ;

; **ADD THE APPLICATION PROGRAM HERE**

;

        CMP   *EXIT_AP, 1*   *;is the application over?*

        JNE   *W_LOOP*   *;No, restart the application*

        MOV   *AX, 6F02H*   *;disable Watchdog Timer*

        MOV   *BL, 0*   *;*

        INT   *15H*

;

; **EXIT** ;

Address Mapping

E.1 I/O Address Map

```
Input/output (IO)
    [00000000 - 0000000F]  Direct memory access controller
    [00000000 - 00000CF7]  PCI bus
    [00000010 - 0000001F]  Motherboard resources
    [00000020 - 00000021]  Programmable interrupt controller
    [00000022 - 0000003F]  Motherboard resources
    [00000040 - 00000043]  System timer
    [00000044 - 0000005F]  Motherboard resources
    [00000060 - 00000060]  Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
    [00000061 - 00000061]  System speaker
    [00000063 - 00000063]  Motherboard resources
    [00000064 - 00000064]  Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
    [00000065 - 00000065]  Motherboard resources
    [00000067 - 0000006F]  Motherboard resources
    [00000070 - 00000071]  System CMOS/real time clock
    [00000072 - 0000007F]  Motherboard resources
    [00000080 - 00000080]  Motherboard resources
    [00000081 - 00000083]  Direct memory access controller
    [00000084 - 00000086]  Motherboard resources
    [00000087 - 00000087]  Direct memory access controller
    [00000088 - 00000088]  Motherboard resources
    [00000089 - 0000008B]  Direct memory access controller
    [0000008C - 0000008E]  Motherboard resources
    [0000008F - 0000008F]  Direct memory access controller
    [00000090 - 0000009F]  Motherboard resources
    [000000A0 - 000000A1]  Programmable interrupt controller
    [000000A2 - 000000BF]  Motherboard resources
    [000000C0 - 000000DF]  Direct memory access controller
    [000000E0 - 000000EF]  Motherboard resources
    [000000F0 - 000000FF]  Numeric data processor
```

[00000170 - 00000177] Secondary IDE Channel
[000001CE - 000001CF] VgaSave
[000001F0 - 000001F7] Primary IDE Channel
[00000274 - 00000277] ISAPNP Read Data Port
[00000279 - 00000279] ISAPNP Read Data Port
[000002E8 - 000002EF] VgaSave
[000002F8 - 000002FF] Communications Port (COM2)
[00000376 - 00000376] Secondary IDE Channel
[00000378 - 0000037F] Printer Port (LPT1)
[000003B0 - 000003BB] VgaSave
[000003C0 - 000003DF] VgaSave
[000003F6 - 000003F6] Primary IDE Channel
[000003F8 - 000003FF] Communications Port (COM1)
[00000400 - 0000041F] SM Bus Controller
[00000480 - 000004BF] Motherboard resources
[000004D0 - 000004D1] Motherboard resources
[00000800 - 0000087F] Motherboard resources
[00000A00 - 00000A0F] Motherboard resources
[00000A10 - 00000A1F] Motherboard resources
[00000A20 - 00000A2F] Motherboard resources
[00000A30 - 00000A3F] Motherboard resources
[00000A79 - 00000A79] ISAPNP Read Data Port
[00000D00 - 0000FFFF] PCI bus
[0000D480 - 0000D49F] Standard Universal PCI to USB Host Controller
[0000D800 - 0000D81F] Standard Universal PCI to USB Host Controller
[0000D880 - 0000D89F] Standard Universal PCI to USB Host Controller
[0000DC00 - 0000DC1F] Standard Universal PCI to USB Host Controller
[0000DC80 - 0000DC87] Video Controller (VGA Compatible)
[0000E800 - 0000E8FF] Ethernet Controller
[0000EC00 - 0000ECFF] Ethernet Controller
[0000FFA0 - 0000FFAF] Standard Dual Channel PCI IDE Controller

Table E-1: IO Address Map

E.2 IRQ Address Map

```
Interrupt request (IRQ)
    (ISA)  0    System timer
    (ISA)  1    Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
    (ISA)  3    Communications Port (COM2)
    (ISA)  4    Communications Port (COM1)
    (ISA)  8    System CMOS/real time clock
    (ISA)  9    Microsoft ACPI-Compliant System
    (ISA) 12    Microsoft PS/2 Mouse
    (ISA) 13    Numeric data processor
    (ISA) 14    Primary IDE Channel
    (PCI)  5    Ethernet Controller
    (PCI)  5    SM Bus Controller
    (PCI) 10    Video Controller (VGA Compatible)
    (PCI) 11    Ethernet Controller
    (PCI) 16    Standard Universal PCI to USB Host Controller
    (PCI) 18    Standard Universal PCI to USB Host Controller
    (PCI) 19    Standard Universal PCI to USB Host Controller
    (PCI) 23    Standard Enhanced PCI to USB Host Controller
    (PCI) 23    Standard Universal PCI to USB Host Controller
```

Table E-2: IRQ Address Map

E.3 Memory Address Map

```
Memory
    [00000000 - 0009FFFF]  System board
    [000A0000 - 000BFFFF]  PCI bus
    [000A0000 - 000BFFFF]  VgaSave
    [000C0000 - 000CFFFF]  System board
    [000D0000 - 000DFFFF]  PCI bus
    [000E0000 - 000FFFFF]  System board
    [00100000 - 3F7FFFFF]  System board
    [3F800000 - DFFFFFFF]  PCI bus
    [D0000000 - DFFFFFFF]  Video Controller (VGA Compatible)
    [E0000000 - E3FFFFFF]  Motherboard resources
    [E4000000 - FED8FFFF]  PCI bus
    [FE980000 - FE9FFFFF]  Video Controller
    [FEA3BC00 - FEA3BFFF]  Standard Enhanced PCI to USB Host Controller
    [FEA40000 - FEA7FFFF]  Video Controller (VGA Compatible)
    [FEA80000 - FEAFFFFF]  Video Controller (VGA Compatible)
    [FEBFF800 - FEBFF8FF]  Ethernet Controller
    [FEBFFC00 - FEBFFCFF]  Ethernet Controller
    [FEC00000 - FEC00FFF]  Motherboard resources
    [FED13000 - FED19FFF]  System board
    [FED1C000 - FED1FFFF]  Motherboard resources
    [FED20000 - FED3FFFF]  Motherboard resources
    [FED40000 - FED8FFFF]  Motherboard resources
    [FED90000 - FFFFFFFF]  System board
    [FEE00000 - FEE00FFF]  Motherboard resources
```

Appendix

F

Hazardous Materials Disclosure

F.1 Hazardous Material Disclosure Table for IPB Products Certified as RoHS Compliant Under 2002/95/EC Without Mercury

The details provided in this appendix are to ensure that the product is compliant with the Peoples Republic of China (China) RoHS standards. The table below acknowledges the presences of small quantities of certain materials in the product, and is applicable to China RoHS only.

A label will be placed on each product to indicate the estimated "Environmentally Friendly Use Period" (EFUP). This is an estimate of the number of years that these substances would "not leak out or undergo abrupt change." This product may contain replaceable sub-assemblies/components which have a shorter EFUP such as batteries and lamps. These components will be separately marked.

Please refer to the table on the next page.

Part Name	Toxic or Hazardous Substances and Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (CR(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
Housing	X	O	O	O	O	X
Display	X	O	O	O	O	X
Printed Circuit Board	X	O	O	O	O	X
Metal Fasteners	X	O	O	O	O	O
Cable Assembly	X	O	O	O	O	X
Fan Assembly	X	O	O	O	O	X
Power Supply Assemblies	X	O	O	O	O	X
Battery	O	O	O	O	O	O

O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in SJ/T11363-2006

X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in SJ/T11363-2006

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有"环境友好使用期限"的标签，此期限是估算这些物质"不会有泄漏或突变"的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (CR(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
壳体	X	O	O	O	O	X
显示	X	O	O	O	O	X
印刷电路板	X	O	O	O	O	X
金属螺帽	X	O	O	O	O	O
电缆组装	X	O	O	O	O	X
风扇组装	X	O	O	O	O	X
电力供应组装	X	O	O	O	O	X
电池	O	O	O	O	O	O
O: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T11363-2006 标准规定的限量要求以下。						
X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T11363-2006 标准规定的限量要求。						