IB960F

Intel ® Sandy Bridge / PCH
PICMG 1.3 SHB Express Full-Size CPU Card

USER'S MANUAL

Version 1.0

Acknowledgments

Table of Contents

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Introduction

Product Description

The IB960F PICMG 1.3 SHB Express CPU Card is based on the latest Intel® Q67 chipset. The platform supports 2nd generation Intel® Core processor family with LGA1155 packing and features an integrated dual-channel DDR3 memory controller as well as a graphics core.

The latest Intel® processors provide advanced performance in both computing and graphics quality. This meets the requirement of customers in the gaming, POS, digital signage and server market segment.

The Q67 platform is made with 32-nanometer technology that supports Intel's first processor architecture to unite the CPU and the graphics core on the transistor level. The IB960F SHB board utilizes the dramatic increase in performance provided this Intel's latest cutting-edge technology. Dimensions of the board are 338mm x 126mm.

IB960F FEATURES:

- Supports Intel® 2nd Generation Core i7/i5/i3 QC/DC desktop processors
- Two DDR3 DIMM, 1066/1333MHz, Max. 8GB memory
- Dual Intel® PCI-Express Gigabit LAN
- Integrated Graphics for CRT, DVI-I, LVDS displays
- 2x SATA 2.0, 2x SATA 3.0, 9x USB 2.0, 2x COM, Watchdog timer
- 2x SATA 2.0, 4x USB 2.0 for PICMG 1.3 backplane
- 1x PCI-E (x16), 1x PCI-E (x4), 4x PCI for PICMG 1.3 backplane

Checklist

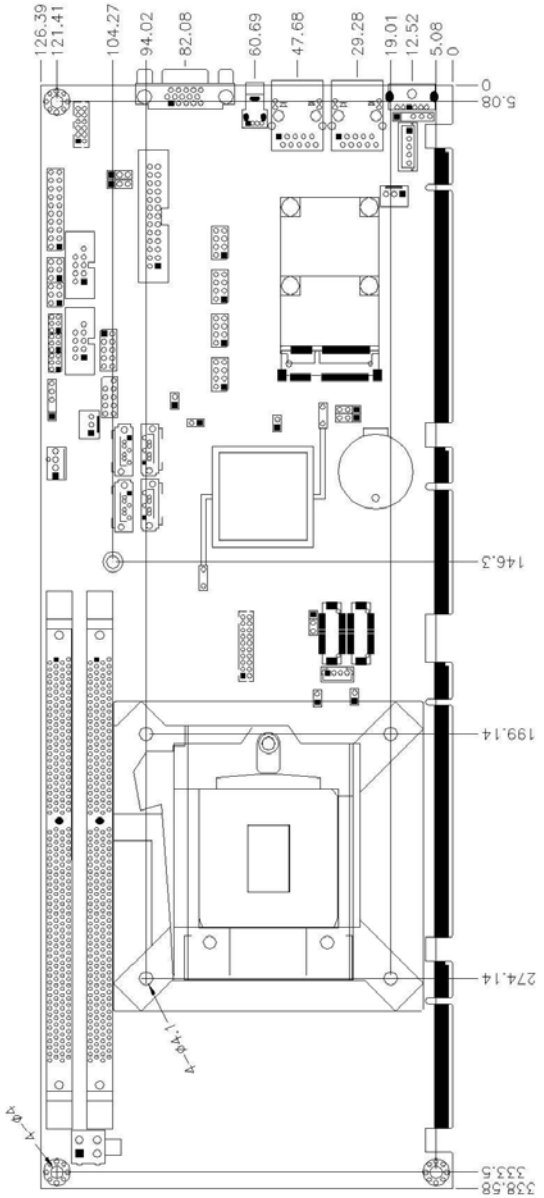
Your IB960F package should include the items listed below.

- The IB960F PICMG 1.3 SHB Express Full-Size CPU Card
- This User's Manual
- 1 CD containing chipset drivers and flash memory utility
- IB64 Cable kit (Keyboard/Mouse, Serial port, Serial ATA, USB, Parallel port)
- Audio cable (Audio-18K) option
- DVI-D cable (DVIK-3) option
- Backplane (IP380L) option

IB960F Specifications

Product Name	IB960F
Form Factor	PICMG 1.3 SHB Express full size CPU card
CPU Type	- Intel® Sandy Bridge 32nm QC/DC DT processor w/ IMC & Gfx - LGA package[37.5 mm x 37.5mm](TDP: QC= 95W/65W ; DC = 65W) **Sandy Bridge-DT is NOT socket compatible with Clarkdale/Lynnfield
CPU Speed	Up to 3.1GHz
Cache	Up to 8MB
CPU Socket	**LGA1155 (Socket H2)**
Chipset	Intel® Q67 PCH 27 x 27 mm package size
BIOS	AMI BIOS, support ACPI Function
Memory	Intel® Core™ i7/i5/i3 DT processor integrated memory controller DDR3 1066/1333 MHz (Non-ECC) DIMM x 2, Max. 8GB
VGA	- Intel® 2nd generation Core™ i7/i5/i3 mobile processor integrated Gfx • VGA • DVI-D X 1 (thru Level shifter ASM1442) • LVDS : 24-bit dual channel (Chrontel CH7308 via SDVO)
LAN	1. Intel® Q67 Gigabit MAC + PHY :Intel® 82579V GbE x1 2. Intel® 82583V PCI-e Gigabit LAN controller x1
USB	Intel® Q67 built-in USB 2.0 host controller, support **14** ports **10 ports on SHB, 4 ports to the backplane [Connector C]**
Serial ATA	Intel® Q67 PCH built-in SATA controller, supports total 6 ports 2 x SATA (3.0) 6Gbps+ 4 x SATA (2.0) 3Gbps ports **[2 x SATA 2.0 ports to the backplane Connector C]**
Audio	Intel® Q67 built-in high definition audio w/ Realtek ALC662 Codec
LPC I/O	Winbond W83627DHG-P COM1 (RS232 only), COM2 (RS232/422/485) Hardware Monitor (2 thermal inputs, 4 voltage monitor inputs & 3 Fan headers) 4 Pin PWM _Fan x 1+3 Pin DC_Fan x2
Digital IO	4 in & 4 out
KB/Mouse	Supports PS/2 Keyboard/Mouse connector [KB 1st priority]
Expansion Slots	Mini PCI-express socket x1@solder side [Full-sized]; [Support USB client]
Edge Connectors	PS/2 Connector x1 for keyboard/mouse DB15 for VGA, 2x RJ45 for LAN 1 & 2, 1x USB 2.0
Interface	1x PCIe (16x) [Connector A & B] 4x PCIe (1x) **or** 1x PCIe (4x) [Connector A] 4x PCI masters [Connector D]
Onboard Header/ Connector	2x DF13 for 24-bit LVDS 1x 4-pin box header for brightness control 1x DF11-20-pin header for DVI 2x13 pins box-header x1 for Printer 2x DF11-10-pin box-header for COM1/ COM2 4x 8-pin header for USB1-8 1x 12-pin header for Audio (Line-**Out, Line-In & Mic)** **1x 10-pin header Digital I/O** 1x 4-pin header for CPU fan (PWM smart fan) 1x 3-pin x2 header for system fan (DC-fan) 6x SATA (Black connectors x4 for SATA2; Blue connectors x2 for SATA 3) 1x 10-pin header Front panel
Watchdog Timer	Yes (256 segments, 0, 1, 2…255 sec/min)
System Voltage	ATX
Others	LAN Wakeup
Board Size	338mm x 126mm

Board Dimensions



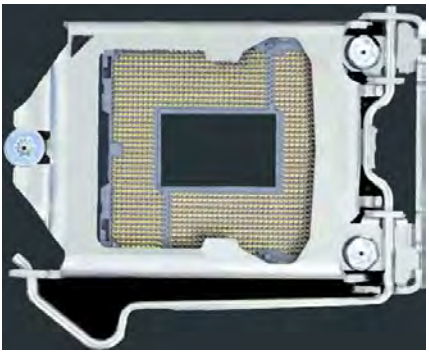
Installations

This section provides information on how to use the jumpers and connectors on the IB960F in order to set up a workable system. The topics covered are:

Installing the CPU

The IB960F board supports an LGA1155 Socket (shown below) for Intel Sandy Bridge processors.

To install the CPU, unlock first the socket by pressing the lever sideways, then lift it up to a 90-degree. Then, position the CPU above the socket such that the CPU corner aligns with the gold triangle matching the socket corner with a small triangle. Carefully insert the CPU into the socket and push down the lever to secure the CPU. Then, install the heat sink and fan.



***NOTE**: Ensure that the CPU heat sink and the CPU top surface are in total contact to avoid CPU overheating problem that would cause your system to hang or be unstable.*

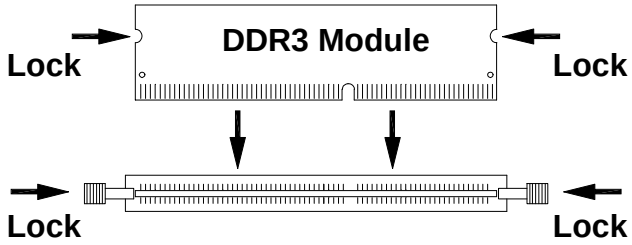
Installing the Memory

The IB960F board supports two DDR3 memory socket for a maximum total memory of 8GB in DDR3 DIMM memory type.

Installing and Removing Memory Modules

To install the DDR3 modules, locate the memory slot on the board and perform the following steps:

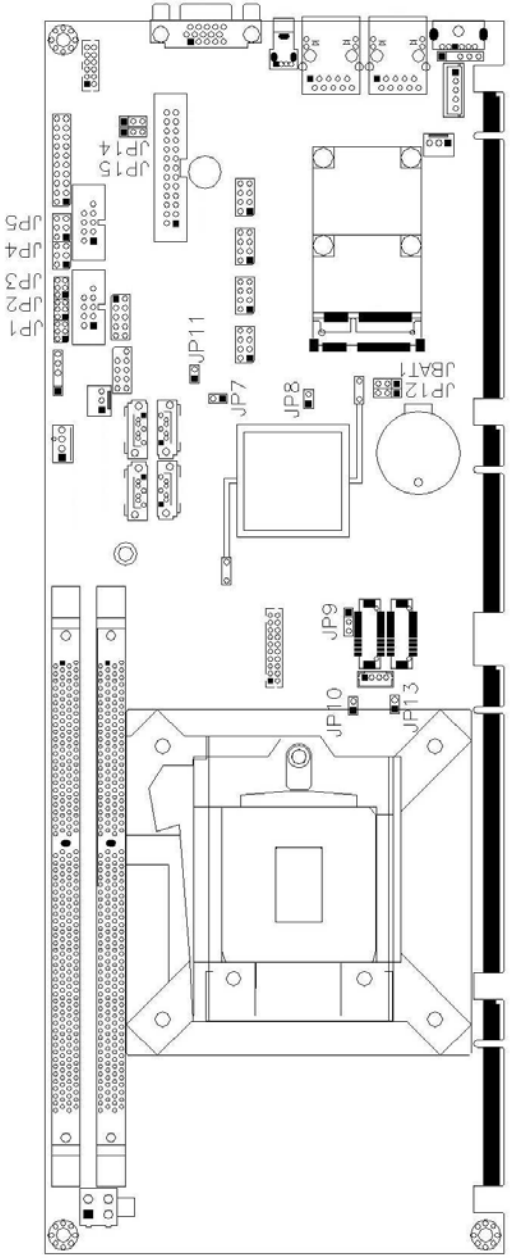
1. Hold the DDR3 module so that the key of the DDR3 module aligned with that on the memory slot.
2. Gently push the DDR3 module in an upright position until the clips of the slot close to hold the DDR3 module in place when the DDR3 module touches the bottom of the slot.
3. To remove the DDR3 module, press the clips with both hands.



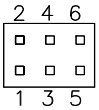
Setting the Jumpers

Jumpers are used on IB960F to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on IB960F and their respective functions.

Jumper Locations on IB960F

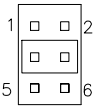


JP1, JP2, JP3: RS232/RS422/RS485 (COM2) Selection



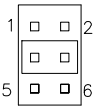
COM2 Function	RS-232	RS-422	RS-485
Jumper Setting (Pin closed)	JP1: 1-2 JP2 3-5&4-6 JP3: 3-5&4-6	JP1: 3-4 JP2: 1-3&2-4 JP3: 1-3&2-4	JP1: 5-6 JP2: 1-3&2-4 JP3: 1-3 & 2-4

JP4: COM2 RS232 RI/+5V/+12V Power Setting

JP4	Setting	Function
	Pin 1-2 Short/Closed	+12V
	Pin 3-4 Short/Closed	RI
	Pin 5-6 Short/Closed	+5V

Note: The suggested setting is RI, with maximum current lower than 1A.

JP5: COM1 RS232 RI/+5V/+12V Power Setting

JP5	Setting	Function
	Pin 1-2 Short/Closed	+12V
	Pin 3-4 Short/Closed	RI
	Pin 5-6 Short/Closed	+5V

Note: The suggested setting is RI, with maximum current lower than 1A.

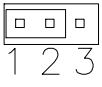
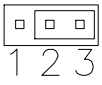
JP7: ME TLS DISABLE/ENABLE (Factory use only)

JP7	ME TLS Disable/Enable
Open	Disabled (Default)
Close	Enabled

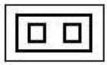
JP8: Flash Descriptor Security Override (Factory use only)

JP8	Flash Descriptor Security Override
Open	Disabled (Default)
Close	Enabled

JP9: LVDS Panel Power Select

JP9	Setting	Panel Voltage
	Pin 1-2 Short/Closed	3.3V (default)
	Pin 2-3 Short/Closed	5V

JP10: Backlight Adjust

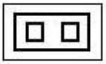
JP10	Setting	Panel Voltage
	OPEN	3.3V (default)
	CLOSE	5V

JP11: PWM voltage setting(Factory use only)

JP12: SRTC RST#(Factory use only)

JP12	Setting	Function
	Pin 1-2 Short/Closed (Default)	Normal
	Pin 2-3 Short/Closed	Clear ME

JP13: Backlight Enable

JP13	Setting	Panel Voltage
	OPEN	3.3V (default)
	CLOSE	5V

JP14: ATX or AT (Emulation) Mode Selection

JP14	Setting
	AT (Emulation)
	ATX

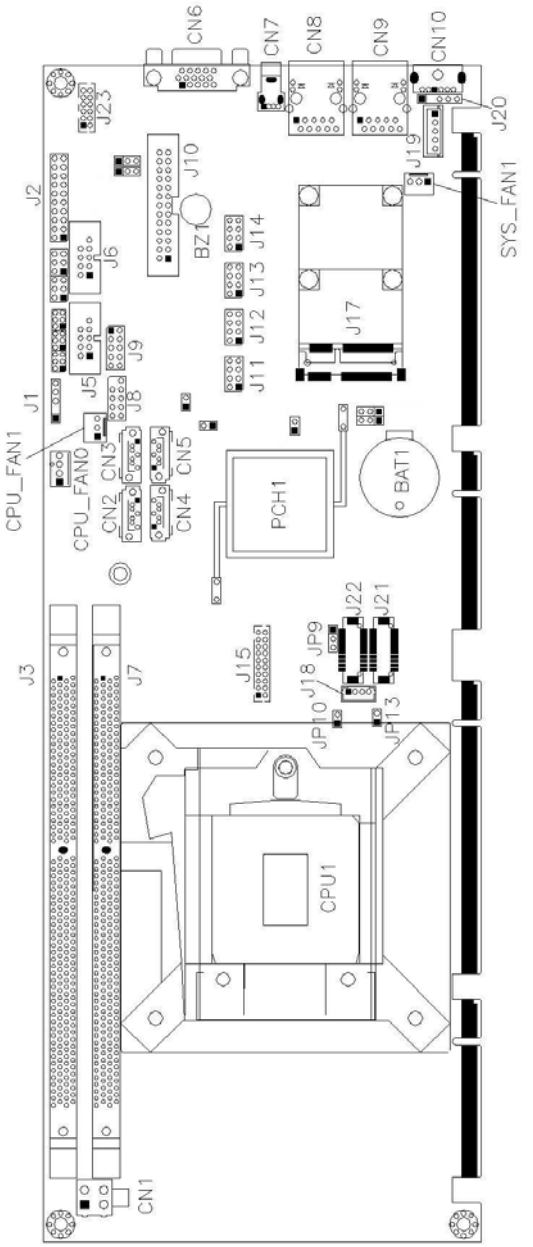
1-2: AT (Emulation), for SYS PWR_ON. Automatic power on comes after a 200ms delay.
2-3: ATX Mode, SYS PWR_ON for manual control

JBAT1: Clear CMOS Contents

JBAT1	Setting	Function
	Pin 1-2 Short/Closed	Normal
	Pin 2-3 Short/Closed	Clear CMOS

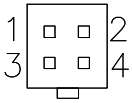
Connectors on IB960F

Connector Locations on IB960F



CN1: ATX 12V Power Connector

This connector supplies the CPU operating voltage.

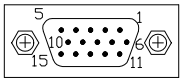


Pin #	Signal Name
1	Ground
2	Ground
3	+12V
4	+12V

CN2.CN4: SATA 3.0 Connectors(Blue)

CN3.CN5: SATA 2.0 Connectors(Black)

CN6: DB-15 VGA Connector



Signal Name	Pin #	Pin #	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
VCC	9	10	GND
N.C.	11	12	DDCDATA
HSYNC	13	14	VSYNC
DDCCLK	15		

CN7: USB2.0 Connector

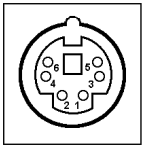
CN8: Gigabit LAN (Intel 82579V)

CN9: Gigabit LAN (Intel 82583V)

This RJ45 LAN connector features for LAN wakeup.

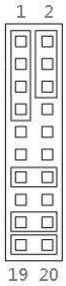
CN10: PS/2 Keyboard and Mouse Connector

CN10 uses a Y-cable with dual D-connectors.



Pin #	Signal Name
1	Keyboard Data
2	Mouse Data
3	Ground
4	Vcc
5	Keyboard Clock
6	Mouse Clock

J2: Front Panel Function

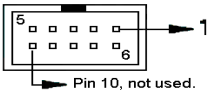


Signal Name	Pin #	Pin #	Signal Name
Speaker out	1	2	PWR LED +
No connect	3	4	No connect
GND	5	6	GND
+5V	7	8	NC
No connect	9	10	GND
No connect	11	12	GND
PWR_SW	13	14	PWR_SW
No connect	15	16	No connect
RST	17	18	GND
HDD LED -	19	20	HDD LED +

J3: DDR3 DIMM Socket Channel B

J7: DDR3 DIMM Socket Channel A

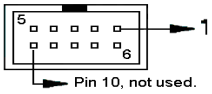
J5: COM2 Serial Port(RS232/422/485)



Please refer to JP1, JP2, JP3: RS232/422/485 (COM2) Selection

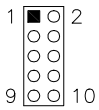
Pin #	Signal Name		
	RS-232	R2-422	RS-485
1	DCD	TX-	DATA-
2	RX	TX+	DATA+
3	TX	RX+	NC
4	DTR	RX-	NC
5	Ground	Ground	Ground
6	DSR	RTS-	NC
7	RTS	RTS+	NC
8	CTS	CTS+	NC
9	RI	CTS-	NC
10	NC	NC	NC

J6: COM1 Serial Port(RS232)



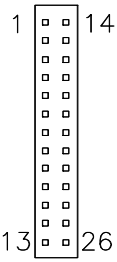
J8: SPI Flash (Factory use only)

J9: Digital I/O Port



Signal Name	Pin	Pin	Signal Name
GND	1	2	VCC
OUT3	3	4	OUT1
OUT2	5	6	OUT0
IN3	7	8	IN1
IN2	9	10	IN0

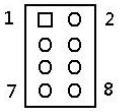
J10: Parallel Port



Signal Name	Pin #	Pin #	Signal Name
Line printer strobe	1	14	AutoFeed
PD0, parallel data 0	2	15	Error
PD1, parallel data 1	3	16	Initialize
PD2, parallel data 2	4	17	Select
PD3, parallel data 3	5	18	Ground
PD4, parallel data 4	6	19	Ground
PD5, parallel data 5	7	20	Ground
PD6, parallel data 6	8	21	Ground
PD7, parallel data 7	9	22	Ground
ACK, acknowledge	10	23	Ground
Busy	11	24	Ground
Paper empty	12	25	Ground
Select	13	26	Ground

J11: USB 2/3 Ports

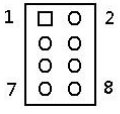
The following table shows the pin outs of the USB2.0 pin header.



Signal Name	Pin	Pin	Signal Name
Vcc	1	2	Ground
USB2-	3	4	USB3+
USB2+	5	6	USB3-
Ground	7	8	Vcc

J12: USB 6/7 Ports

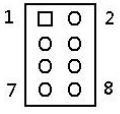
The following table shows the pin outs of the USB2.0 pin header



Signal Name	Pin	Pin	Signal Name
Vcc	1	2	Ground
USB6-	3	4	USB7+
USB6+	5	6	USB7-
Ground	7	8	Vcc

J13: USB 4/5 Ports

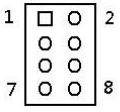
The following table shows the pin outs of the USB2.0 pin header



Signal Name	Pin	Pin	Signal Name
Vcc	1	2	Ground
USB4-	3	4	USB5+
USB4+	5	6	USB5-
Ground	7	8	Vcc

J14: USB 8/9 Ports

The following table shows the pin outs of the USB2.0 pin header

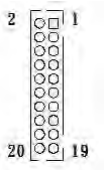


Signal Name	Pin	Pin	Signal Name
Vcc	1	2	Ground
USB8-	3	4	USB9+
USB8+	5	6	USB9-
Ground	7	8	Vcc

J15: DVI-D Port

J15 is a 20-pin header that is used to connect to the optional DVI-D cable.

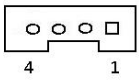
The following table shows the pin outs of the DVI-D pin header.



Signal Name	Pin #	Pin #	Signal Name
TDC1#_B	2	1	TDC1_B
Ground	4	3	Ground
TLC#_B	6	5	TLC_B
5V	8	7	Ground
N.C.	10	9	HPDET_B
TDC2#_B	12	11	TDC2_B
Ground	14	13	Ground
TDC0#_B	16	15	TDC0_B
N.C.	18	17	N.C.
SC_DDC_B	20	19	SD_DDC_B

J17: Mini PCIE Connector

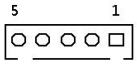
J18: LCD Backlight Control



Pin #	Signal Name
1	+12V
2	Backlight Enable
3	Backlight Adj
4	GND

J19: External PS/2 Keyboard Port

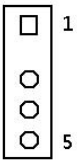
The following table shows the pin outs of the PS/2 keyboard pin header.



Pin #	J19
1	KB clock
2	KB data
3	N.C.
4	Ground
5	Vcc

J20: External PS/2 Mouse Port

The following table shows the pin outs of the PS/2 mouse pin header.

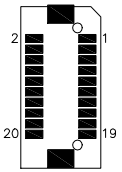


Pin #	J20
1	Mouse data
2	N.C
3	GND.
4	Mouse clock
5	Vcc

J21, J22: LVDS Connector (2nd channel, 1st channel)

The LVDS connectors, DF13 20-pin mating connectors, are composed of the 2nd channel (J21) and 1st channel (J22) to support 18-bit or 24bit

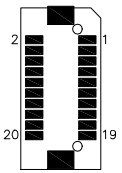
J22: first channel



Signal Name	Pin #	Pin #	Signal Name
TX0-	2	1	TX0+
Ground	4	3	Ground
TX1-	6	5	TX1+
*5V/3.3V	8	7	Ground
TX3-	10	9	TX3+
TX2-	12	11	TX2+
Ground	14	13	Ground
TXC1-	16	15	TXC1+
*5V/3.3V	18	17	BKL_EN
+12V	20	19	+12V

**JP9 can be used to set 3.3V or 5V.*

J21: Second channel

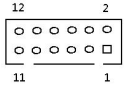


Signal Name	Pin #	Pin #	Signal Name
TX4-	2	1	TX4+
Ground	4	3	Ground
TX5-	6	5	TX5+
*5V/3.3V	8	7	Ground
TX7-	10	9	TX7+
TX6-	12	11	TX6+
Ground	14	13	Ground
TXC2-	16	15	TXC2+
*5V/3.3V	18	17	BKL_EN
+12V	20	19	+12V

**JP9 can be used to set 3.3V or 5V.*

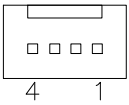
J23: External Audio Connector

J23 is a 12-pin header that is used to connect to the optional audio cable.



Signal Name	Pin #	Pin #	Signal Name
LINE OUT_L	1	2	LINE OUT_R
JD_FRONT	3	4	Ground
LINE IN_L	5	6	LINE IN R
JD LINE IN	7	8	Ground
MIC-L	9	10	MIC-R
JD MIC1	11	12	Ground

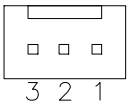
CPU_FAN0: CPU Fan0 Power Connector



Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection
4	Control

Note: CPU_FAN0 for PWM FAN mode

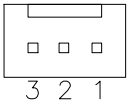
CPU_FAN1: CPU Fan1 Power Connector



Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection

Note: CPU_FAN0 for DC FAN mode

SYS_FAN1: System Fan1 Power Connector



Pin #	Signal Name
1	Ground
2	+12V
3	NC

Note: SYS_FAN1 for DC FAN mode

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BIOS Setup

This chapter describes the different settings available in the AMI BIOS that comes with the board. The topics covered in this chapter are as follows:

BIOS Introduction

The BIOS (Basic Input/Output System) installed in your computer system's ROM supports Intel processors. The BIOS provides critical low-level support for a standard device such as disk drives, serial ports and parallel ports. It also password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Pressing the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again. The following message will appear on the screen:

```
Press  <DEL>  to  Enter  Setup
```

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Warning: *It is strongly recommended that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could cause the system to become unstable and crash in some cases.*

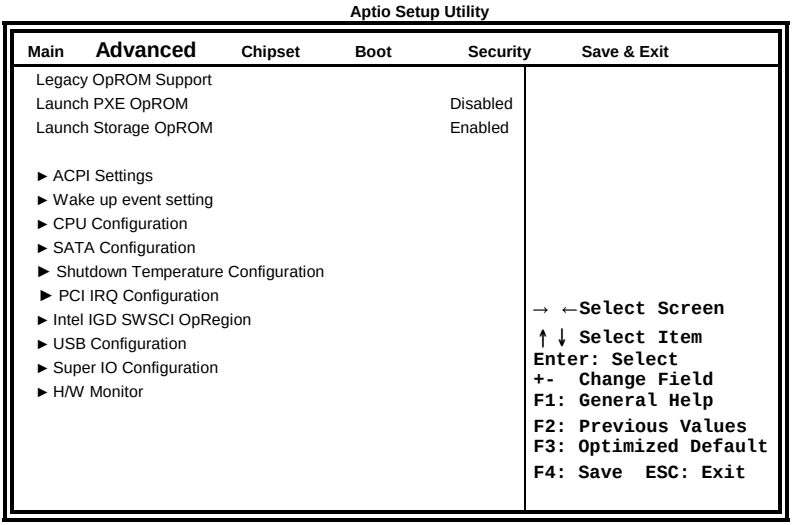
System Language
Choose the system default language.

System Date
Set the Date. Use Tab to switch between Data elements.

System Time
Set the Time. Use Tab to switch between Data elements.

Advanced Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



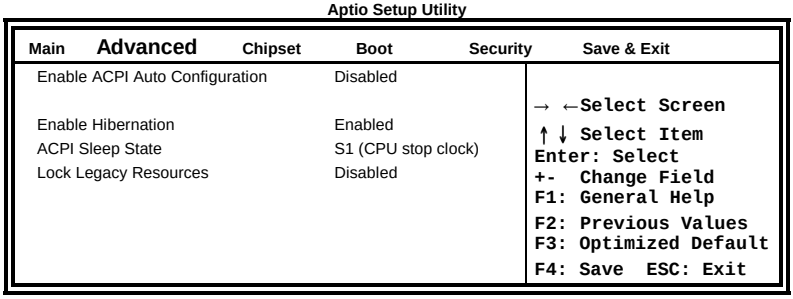
Launch PXE OpROM

Enable or Disable Boot Option for Legacy Network Devices.

Launch Storage OpROM

Enable or Disable Boot Option for Legacy Mass Storage Devices with Option ROM.

ACPI Settings



Enabled ACPI Auto Configuration

Enables or Disables BIOS ACPI Auto Configuration.

Enable Hibernation

Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

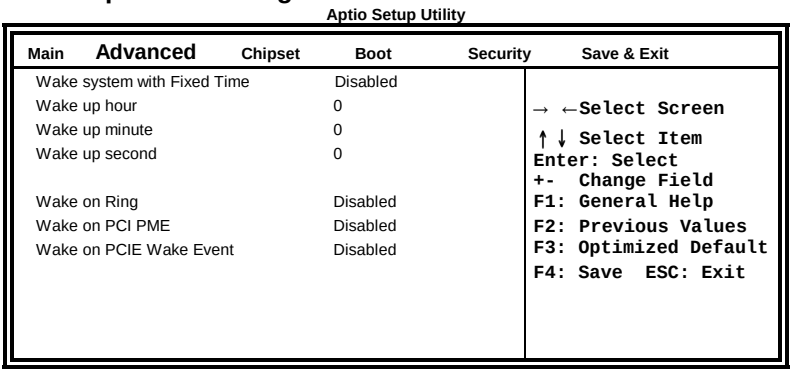
ACPI Sleep State

Select the highest ACPI sleep state the system will enter, when the SUSPEND button is pressed.

Lock Legacy Resources

Enabled or Disabled Lock of Legacy Resources.

Wake up event settings



Wake system with Fixed Time

Enables or Disables System wake on alarm event. When enabled, System will wake on the hr::min:: sec specified.

Wake on Ring

The options are Disabled and Enabled.

Wake on PCI PME

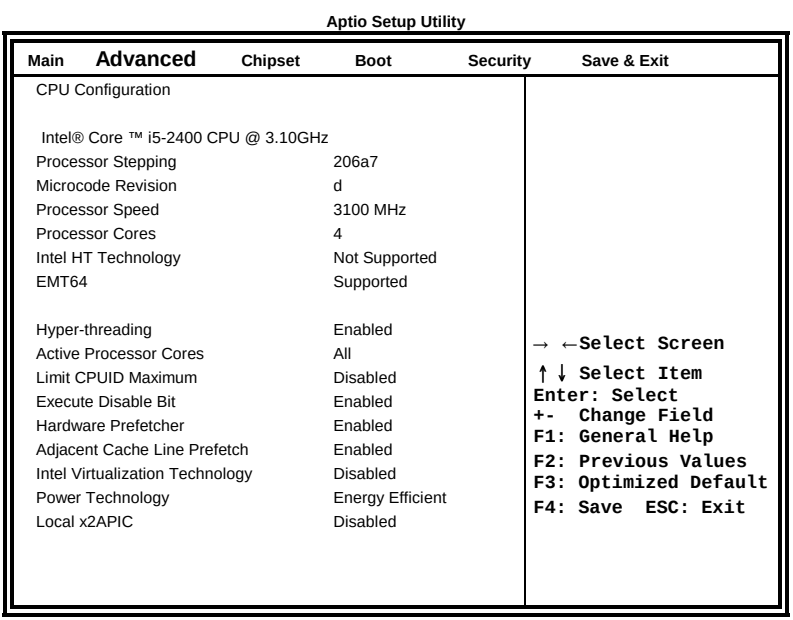
The options are Disabled and Enabled.

Wake on PCIE PME Wake Event

The options are Disabled and Enabled.

CPU Configuration

This section shows the CPU configuration parameters.



Hyper-threading

Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled, only one thread per enabled core is enabled.

Active Processor Cores

Number of cores to enable in each processor package.

Limit CPUID Maximum

Disabled for Windows XP.

Execute Disable Bit

XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, Re33dHat Enterprise 3 Update 3.)

Hardware Prefetcher

To turn on/off the MLC streamer prefetcher.

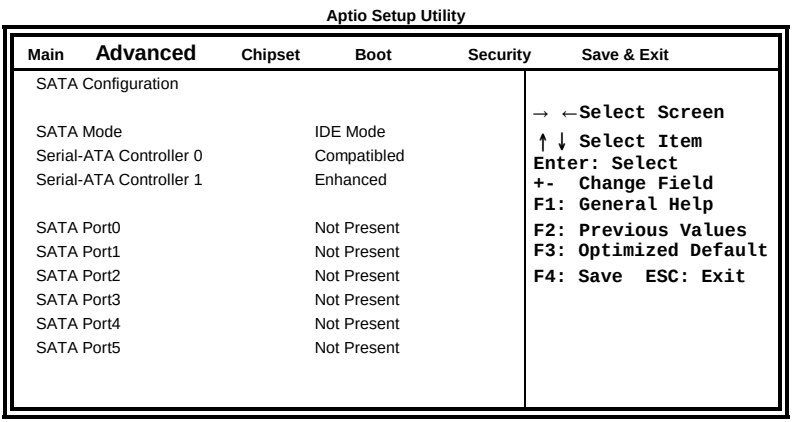
Adjacent Cache Line Prefetch
To turn on/off prefetching of adjacent cache lines.

Intel Virtualization Technology
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Power Technology
Enable the power management features.

Local x2APIC
Enable Local x2APIC. Some OSes do not support this.

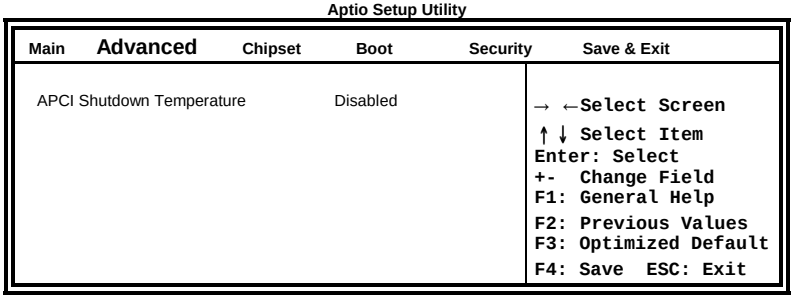
SATA Configuration
SATA Devices Configuration.



SATA Mode
(1) IDE Mode.
(2) AHCI Mode.
(3) RAID Mode.

Serial-ATA Controller
Enable / Disable Serial ATA Controller.

Shutdown Temperature Configuration



ACPI Shutdown Temperature

The default setting is Disabled.

.

PCI IRQ Configuration

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
IRQ3			PCI/ISA	→ ←Select Screen	
IRQ4			PCI/ISA	↑ ↓ Select Item	
IRQ5			PCI/ISA	Enter: Select	
IRQ6			PCI/ISA	+- Change Field	
IRQ7			PCI/ISA	F1: General Help	
IRQ10			PCI/ISA	F2: Previous Values	
IRQ11			PCI/ISA	F3: Optimized Default	
IRQ12			PCI/ISA	F4: Save ESC: Exit	

Intel IGD SWSCI OpRegion

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
Intel IGD SWSCI OpRegion Configuration					
DVMT Mode Select			DVMT Mode		
DVMT/FIXED Memory			256MB		
IGD - Boot Type			VBIOS Default		
LCD Panel Type			1024x768 LVDS		
Panel Scaling			Auto		
				→ ←Select Screen	
				↑ ↓ Select Item	
				Enter: Select	
				+- Change Field	
				F1: General Help	
				F2: Previous Values	
				F3: Optimized Default	
				F4: Save ESC: Exit	

DVMT Mode Select

Select DVMT Mode used by Internal Graphics Device.

DVMT/FIXED Memory

Select DVMT/FIXED Mode Memory size used by Internal Graphics Device. Options are 128MB, 256MB and Maximum.

IGD - Boot Type

Select the Video Device that will be activated during POST. This has no effect if external graphics present.

Note: When using the DVI port only, choose EFP option.

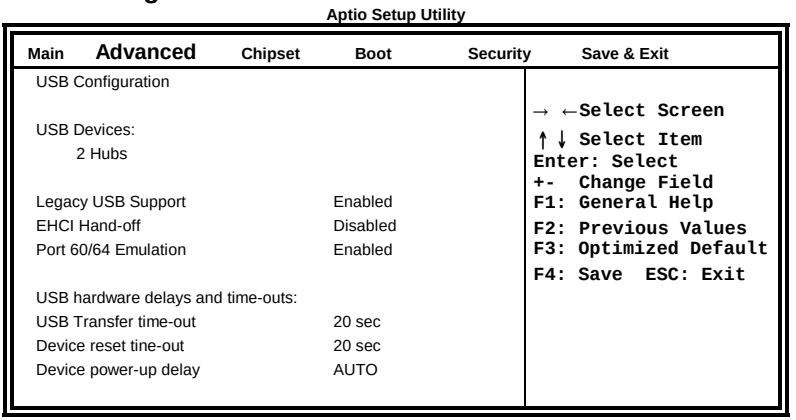
LCD Panel Type

Select LCD Panel used by Internal Graphics Device by selecting the appropriate setup item.

Panel Scaling

Select the LCD panel scaling option used by the Internal Graphics Device.

USB Configuration



Legacy USB Support

Enables Legacy USB support.
AUTO option disables legacy support if no USB devices are connected.
DISABLE option will keep USB devices available only for EFI applications.

EHCI Hand-off
Enabled/Disabled. This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

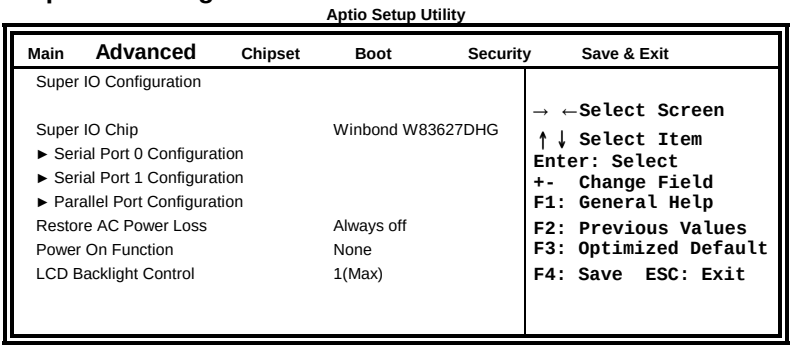
Port 64/60 Emulation
Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.

USB Transfer time-out
The time-out value for Control, Bulk, and Interrupt transfers.

Device reset tine-out
USB mass Storage device start Unit command time-out.

Device power-up delay
Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

Super IO Configuration



Serial Port Configuration

Set Parameters of Serial Ports. User can Enable/Disable the serial port and Select an optimal settings for the Super IO Device.

Restore AC Power Loss

Always on
Always off (default)

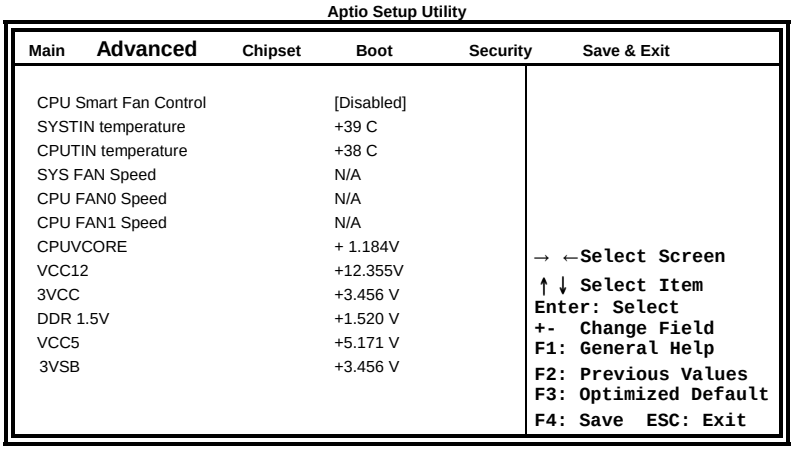
Power On function

None (default)
Mouse Left
Mouse Right
Any key

LCD Backlight Control

1(Max) (default)
2
3
4
5
6
7
8(Min)

H/W Monitor



Temperatures/Voltages

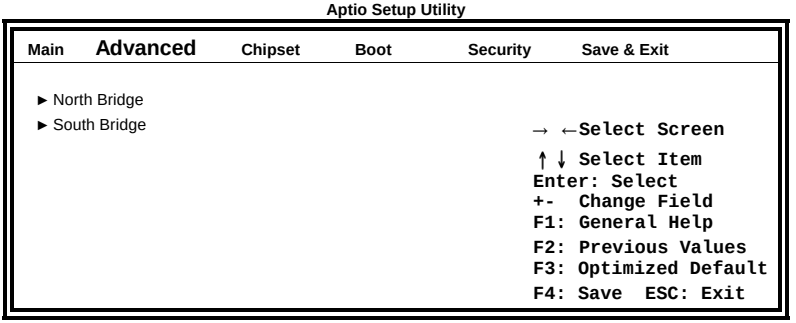
These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.

CPU Smart Fan Control

Disabled (default)
55 C
60 C
65 C
70 C

Chipset Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



North Bridge

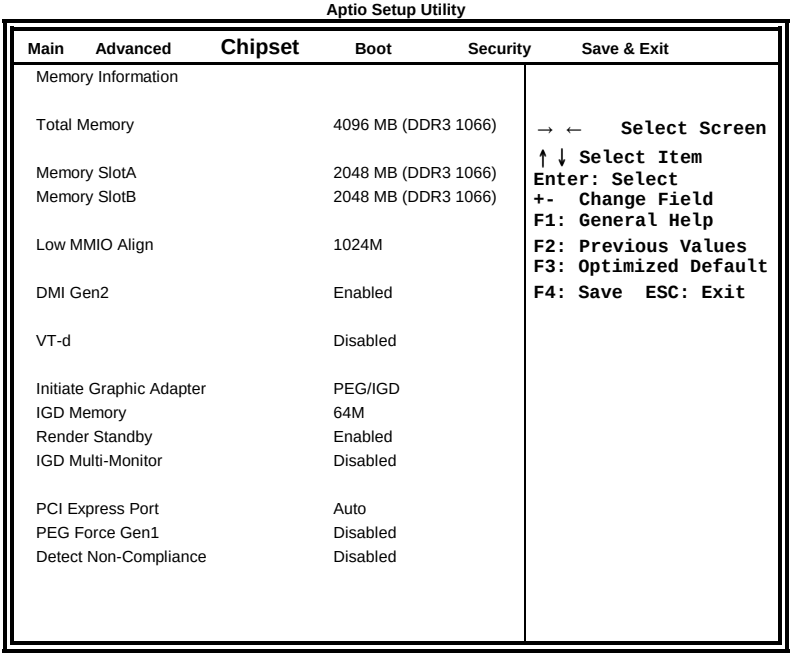
This item shows the North Bridge Parameters.

South Bridge

This item shows the South Bridge Parameters.

North Bridge

This section allows you to configure the North Bridge Chipset.



Low MMIO Align

Low MMIO resources align at 64MB/1024MB.

VT-d

VT-d Enable/Disable.

Initiate Graphic Adapter

Select which graphics controller to use as the primary boot device. Options are IGD, PCI/IGD, PCI/PEG, PEG/IGD, PEG/PCI and SG.

IGD Memory

IGD Share Memory Size. Options are Disable, 32M, 64M and 128M.

Render Standby

Enabled/Disabled Render standby by Internal Graphics Device.

IGD Multi-Monitor

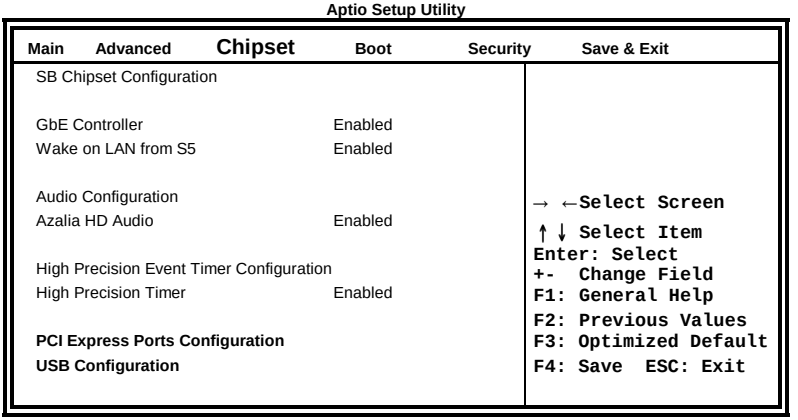
Enabled/Disabled IGD Multi-Monitor by Internal Graphics Device.

PCI Express Port
Options are Disabled, Enabled and Auto.

PEG Force Gen1
PCI Express Port Force Gen1. Options are Disabled and Enabled.

Detect Non-Compliance
Detect Non-Compliance PCI Express Device in PEG.

SB Chipset Configuration
This section allows you to configure the South Bridge Chipset.



GbE Controller
This is constantly enabled.

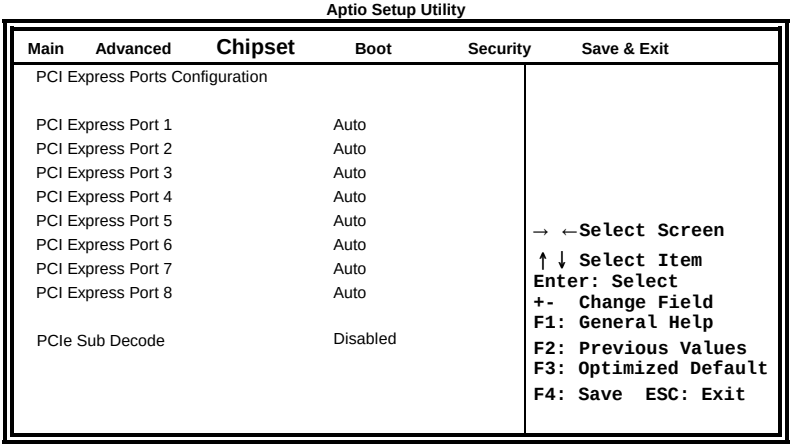
Wake on LAN from S5
Wake on LAN from S5 help.

Audio Configuration
The Audio Configuration settings Enable/Disable the Azalia HD Audio and the Azalia internal HDMI codec.

High Precision Event Timer Configuration
Enable/or Disable the High Precision Event Timer.

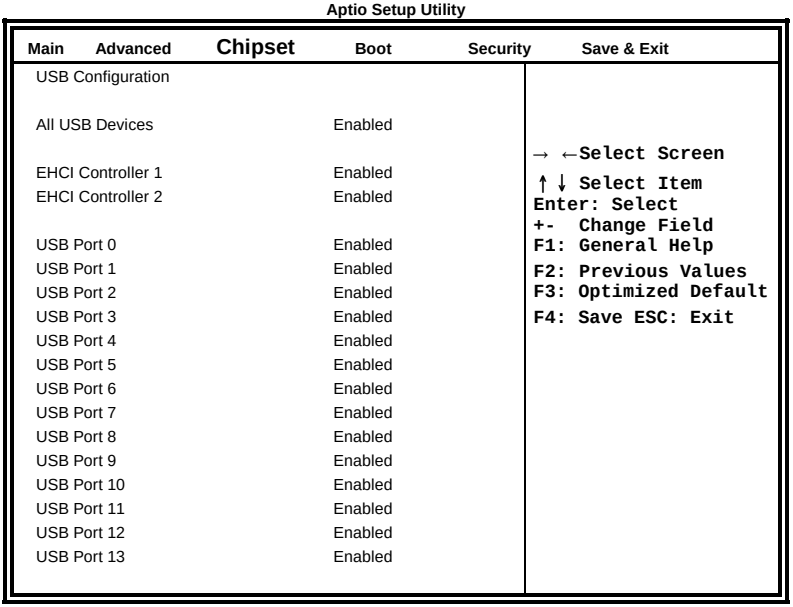
PCI Express Ports Configuration

Enable or Disable the PCI Express Ports in the Chipset.

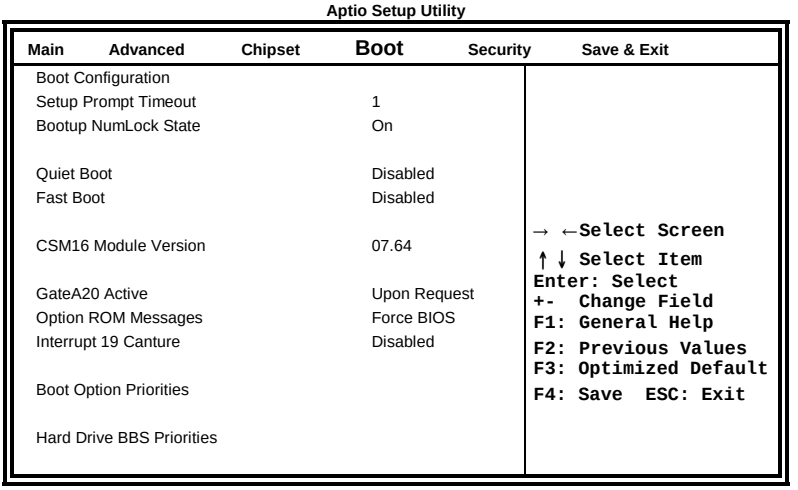


USB Configuration

Enable/Disable All USB Devices, USB 2.0 (EHCI) Support and RMH Support. The setting of AUTO on RMH Support Enable RMH support on Ibex Peak B0 Stepping.



Boot Settings



Setup Prompt Timeout
Number of seconds to wait for setup activation key.
65535(0xFFFF) means indefinite waiting.

Bootup NumLock State
Select the keyboard NumLock state.

Quiet Boot
Enables/Disables Quiet Boot option.

Fast Boot
Enables/Disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

GateA20 Active
UPON REQUEST – GA20 can be disabled using BIOS services.
ALWAYS – do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

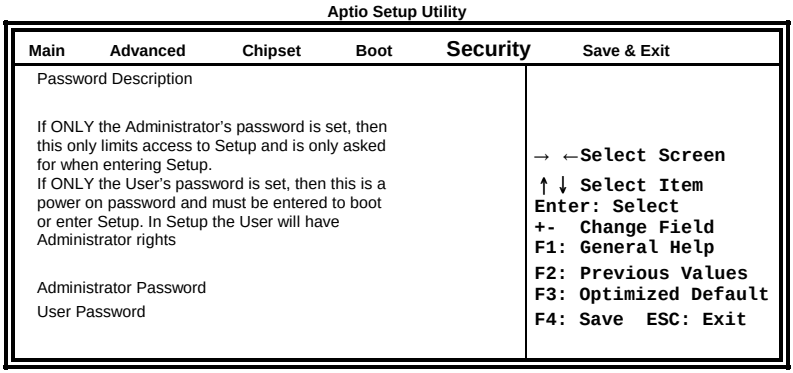
Option ROM Messages
Set display mode for Option ROM. Options are Force BIOS and Keep Current.

Interrupt 19 Capture
Enable: Allows Option ROMs to trap Int 19.

Boot Option Priorities
Sets the system boot order.

Security Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



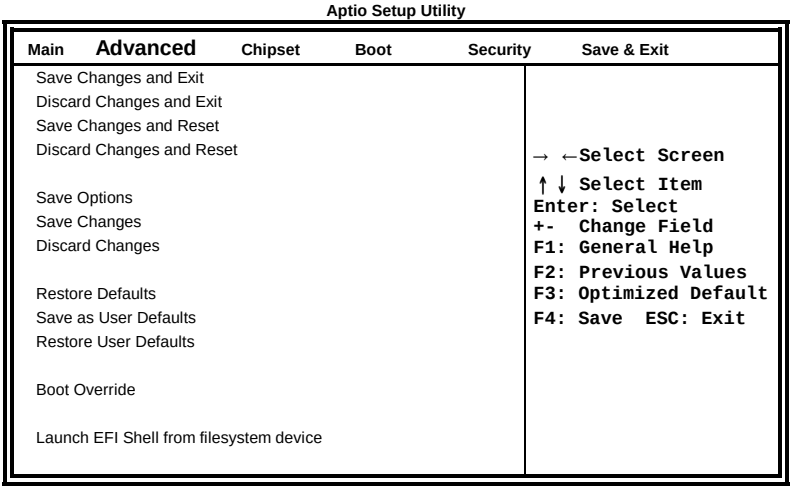
Administrator Password

Set Setup Administrator Password.

User Password

Set User Password.

Save & Exit Settings



Save Changes and Exit
Exit system setup after saving the changes.

Discard Changes and Exit
Exit system setup without saving any changes.

Save Changes and Reset
Reset the system after saving the changes.

Discard Changes and Reset
Reset system setup without saving any changes.

Save Changes
Save Changes done so far to any of the setup options.

Discard Changes
Discard Changes done so far to any of the setup options.

Restore Defaults
Restore/Load Defaults values for all the setup options.

Save as User Defaults
Save the changes done so far as User Defaults.

Restore User Defaults
Restore the User Defaults to all the setup options.

Boot Override
Pressing ENTER causes the system to enter the OS.

Launch EFI Shell from filesystem device
Attempts to Launch EFI Shell application (Shellx64.efi) from one of the available filesystem devices.

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Drivers Installation

This section describes the installation procedures for software and drivers. The software and drivers are included with the motherboard. If you find the items missing, please contact the vendor where you made the purchase. The contents of this section include the following:

IMPORTANT NOTE:
After installing your Windows operating system, you must install first the Intel Chipset Software Installation Utility before proceeding with the drivers installation.

Intel Chipset Software Installation Utility

The Intel Chipset Drivers should be installed first before the software drivers to enable Plug & Play INF support for Intel chipset components. Follow the instructions below to complete the installation.

1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) QM67/Q67 Chipset Drivers***.

2. Click ***Intel(R) Chipset Software Installation Utility.***

3. When the Welcome screen to the Intel® Chipset Device Software appears, click ***Next*** to continue.

4. Click ***Yes*** to accept the software license agreement and proceed with the installation process.

5. On the Readme File Information screen, click ***Next*** to continue the installation.

6. The Setup process is now complete. Click ***Finish*** to restart the computer and for changes to take effect.

VGA Drivers Installation

NOTE: Before installing the *Intel(R) Q67 Chipset Family Graphics Driver,* the Microsoft .NET Framework 3.5 SPI should be first installed.

1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) QM67/Q67 Chipset Drivers***.

2. Click ***Intel(R) Q67 Chipset Family Graphics Driver.***

3. When the Welcome screen appears, click ***Next*** to continue.

4. Click ***Yes*** to to agree with the license agreement and continue the installation.

5. On the Readme File Information screen, click ***Next*** to continue the installation of the Intel® Graphics Media Accelerator Driver.

6. On Setup Progress screen, click ***Next*** to continue.

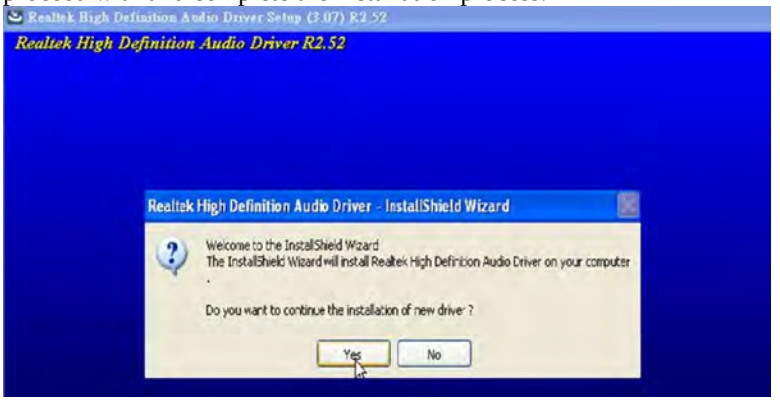
7. Setup complete. Click ***Finish*** to restart the computer and for changes to take effect.

Realtek HD Audio Driver Installation

Follow the steps below to install the Realtek HD Audio Drivers.
1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) QM67/Q67 Chipset Drivers***.

2. Click ***Realtek High Definition Audio Driver.***

3. On the Welcome to the InstallShield Wizard screen, click ***Yes*** to proceed with and complete the installation process.



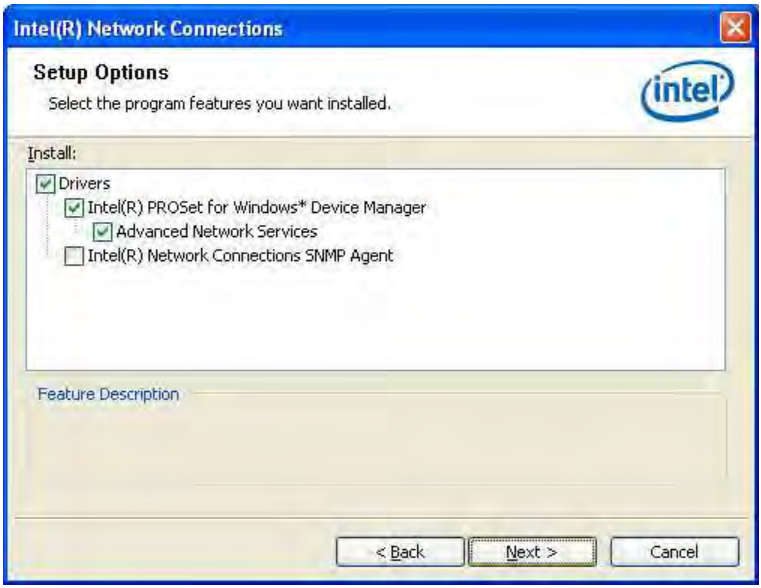
LAN Drivers Installation

1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) QM67/Q67 Chipset Drivers***.

2. Click ***Intel(R) PRO LAN Network Driver.***

3. When the Welcome screen appears, click ***Next***. On the next screen, click ***Yes*** to to agree with the license agreement.

4. Click the checkbox for **Drivers** in the Setup Options screen to select it and click **Next** to continue.

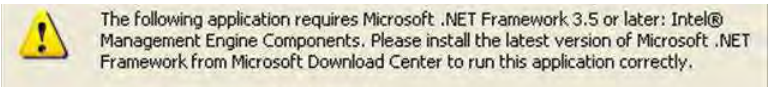


5. The wizard is ready to begin installation. Click ***Install*** to begin the installation.

6. When InstallShield Wizard is complete, click ***Finish***.

Intel® Management Engine Interface

REMARKS: The Intel iAMT 7.0 Drivers need install, but Management Engine Function not support.



Follow the steps below to install the Intel Management Engine.

1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) AMT 7.0 Drivers***.

2. When the Welcome screen to the InstallShield Wizard for Intel® Management Engine Components, click ***Next***. On the next screen, click ***Yes*** to to agree with the license agreement.

2. When the Setup Progress screen appears, click ***Next***. Then, click ***Finish*** when the setup progress has been successfully installed.

Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
2F8h - 2FFh	Serial Port #2(COM2)
2B0h- 2DFh	Graphics adapter Controller
360h - 36Fh	Network Ports
3F8h - 3FFh	Serial Port #1(COM1)

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ8	Real Time Clock
IRQ14	Primary IDE
IRQ15	Secondary IDE

C. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "W627DHG.H"
//---------------------------------------------------------------------------
int main (void);

void WDTInitial(void);
void WDTEnable(unsigned char);
void WDTDisable(void);

//---------------------------------------------------------------------------
int main (void)
{
            char SIO;

            SIO = Init_W627DHG();
            if (SIO == 0)
            {
                        printf("Can not detect Winbond 83627DHG, program
abort.\n");
                        return(1);
            }

            WDTInitial();

            WDTEnable(10);

            WDTDisable();

            return 0;
}
//---------------------------------------------------------------------------
void WDTInitial(void)
{
            unsigned char bBuf;

            bBuf = Get_W627DHG_Reg(0x2D);
            bBuf &= (~0x01);
            Set_W627DHG_Reg(0x2D, bBuf);                        //Enable WDTO
```

```
//---------------------------------------------------------------------------
void WDTEnable(unsigned char NewInterval)
{
            unsigned char bBuf;

            Set_W627DHG_LD(0x08);
            Set_W627DHG_Reg(0x30, 0x01);                        //enable timer

            bBuf = Get_W627DHG_Reg(0xF5);
            bBuf &= (~0x08);
            Set_W627DHG_Reg(0xF5, bBuf);          //count mode is second

            Set_W627DHG_Reg(0xF6, NewInterval);
            //set timer
}
//---------------------------------------------------------------------------
void WDTDisable(void)
{
            Set_W627DHG_LD(0x08);
            Set_W627DHG_Reg(0xF6, 0x00);                        //clear
watchdog timer
            Set_W627DHG_Reg(0x30, 0x00);                        //watchdog
disabled
}
//---------------------------------------------------------------------------

//---------------------------------------------------------------------------
//
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// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#ifndef __W627DHG_H
#define __W627DHG_H                                 1
//---------------------------------------------------------------------------
#define      W627DHG_INDEX_PORT                     (W627DHG_BASE)
#define      W627DHG_DATA_PORT                      (W627DHG_BASE+1)
//---------------------------------------------------------------------------
#define      W627DHG_REG_LD                                     0x07
//---------------------------------------------------------------------------
#define W627DHG_UNLOCK                              0x87
#define      W627DHG_LOCK                           0xAA
//---------------------------------------------------------------------------
unsigned int Init_W627DHG(void);
void Set_W627DHG_LD( unsigned char);
void Set_W627DHG_Reg( unsigned char, unsigned char);
unsigned char Get_W627DHG_Reg( unsigned char);
//---------------------------------------------------------------------------
#endif       //__W627DHG_H


//---------------------------------------------------------------------------
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//
//---------------------------------------------------------------------------
#include "W627DHG.H"
#include <dos.h>
//---------------------------------------------------------------------------
unsigned int W627DHG_BASE;
void Unlock_W627DHG (void);
void Lock_W627DHG (void);
//---------------------------------------------------------------------------
unsigned int Init_W627DHG(void)
{
            unsigned int result;
            unsigned char ucDid;

            W627DHG_BASE = 0x4E;
            result = W627DHG_BASE;

            ucDid = Get_W627DHG_Reg(0x20);
```

```
            if (ucDid == 0xA0)
            {           goto Init_Finish;       }
            else if (ucDid == 0xB0)                         //W83627DHG-P??
            {           goto Init_Finish;       }

            W627DHG_BASE = 0x2E;
            result = W627DHG_BASE;

            ucDid = Get_W627DHG_Reg(0x20);
            if (ucDid == 0xA0)
            {           goto Init_Finish;       }
            else if (ucDid == 0xB0)                         //W83627DHG-P??
            {           goto Init_Finish;       }

            W627DHG_BASE = 0x00;
            result = W627DHG_BASE;

Init_Finish:
            return (result);
}
//-----------------------------------------------------------------------------
void Unlock_W627DHG (void)
{
            outportb(W627DHG_INDEX_PORT, W627DHG_UNLOCK);
            outportb(W627DHG_INDEX_PORT, W627DHG_UNLOCK);
}
//-----------------------------------------------------------------------------
void Lock_W627DHG (void)
{
            outportb(W627DHG_INDEX_PORT, W627DHG_LOCK);
}
//-----------------------------------------------------------------------------
void Set_W627DHG_LD( unsigned char LD)
{
            Unlock_W627DHG();
            outportb(W627DHG_INDEX_PORT, W627DHG_REG_LD);
            outportb(W627DHG_DATA_PORT, LD);
            Lock_W627DHG();
}
//-----------------------------------------------------------------------------
void Set_W627DHG_Reg( unsigned char REG, unsigned char DATA)
{
            Unlock_W627DHG();
            outportb(W627DHG_INDEX_PORT, REG);
            outportb(W627DHG_DATA_PORT, DATA);
            Lock_W627DHG();
}
//-----------------------------------------------------------------------------
unsigned char Get_W627DHG_Reg(unsigned char REG)
{
            unsigned char Result;
            Unlock_W627DHG();
            outportb(W627DHG_INDEX_PORT, REG);
            Result = inportb(W627DHG_DATA_PORT);
            Lock_W627DHG();
            return Result;
}
//-----------------------------------------------------------------------------
```

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