HT12 286 USER'S MANUAL

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HT12 286 USER'S MANUAL

SECTION 1.0

1.1 INTRODUCTION

The HT12 286 system board is a speed and function enhanced computer mainboard that represents a significant technological advance over conventional 80286 designs. The board design includes a variety of high powered features that place the HT12 286 at the forefront of high speed 286 technology. With increased power and flexibility comes an increase in the complexity of hardware and software setup. This manual is designed to provide the basic information necessary for the end user to understand and properly use the HT12 286. It also contains the information necessary to set up more complex configurations and/or upgrade a HT12 286-based system.

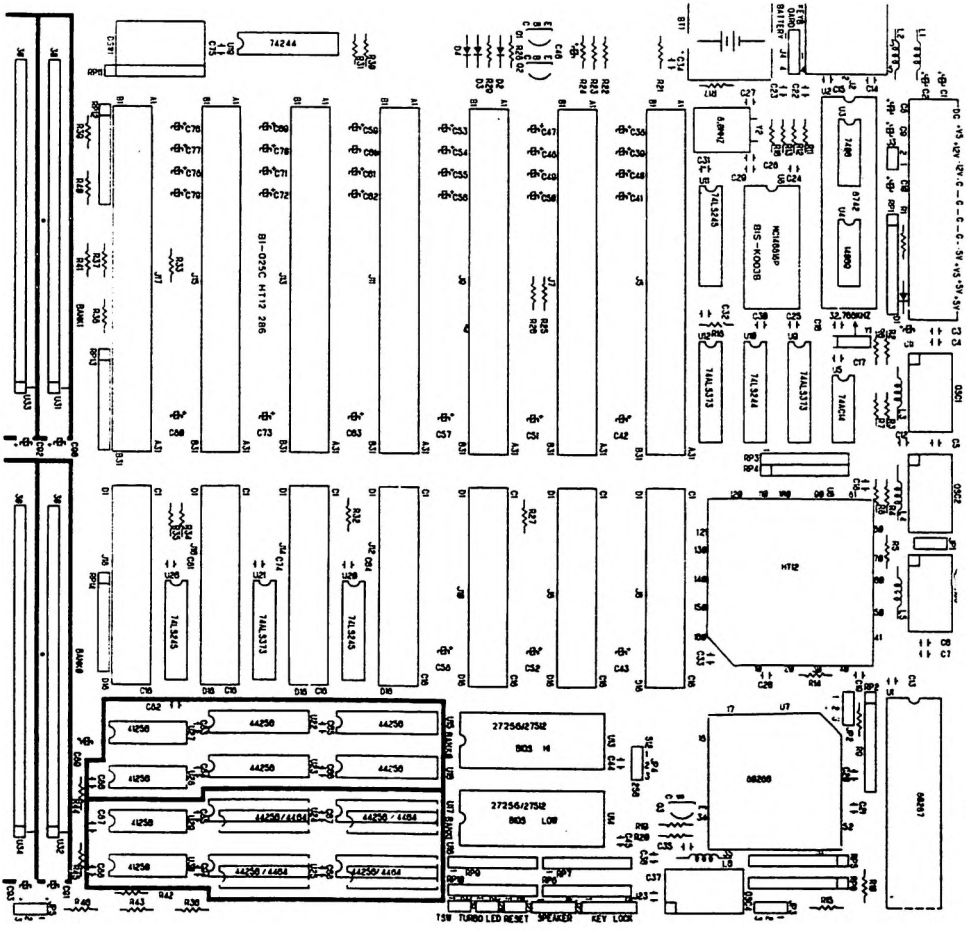
1.2 GENERAL SPECIFICATIONS

- Headland HT12 single 286 AT chip
- Surface Mounting Technology (S.M.T.) applied in chip set mountings
- Intel or AMD 80286 -- 16 MHz or 12 MHz CPU
- 0/1 wait state selectable by BIOS setup
- On board use D-TYPE RAM socket & MODULE RAM socket
- Stickers for legal Quadtel System BIOS and keyboard controller
- 5 16-bit and 2 8-bit I/O expansion slots
- Socket for 80287 math coprocessor
- CMOS RAM for system configuration
- Battery backup for CMOS RAM and Real Time Clock
- 24-bit addressing and 16-bit data path capabilities
- 16-level interrupts
- 7-channel DMA (Direct Memory Access)
- 3-programmable timers
- Hardware switchable and keyboard switchable CPU speed
- Supports 64K, 256K, 1M, x1, x4, and DRAM's up to 4 Meg.
- Power LED and reset connector
- Keylock interface provided
- 4 layer board; 22cm x 21cm (size)
- Shadow RAM for system and video BIOS
- 384K remapping in 64K blocks
- EMS with 4 registers

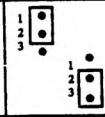
HT12 286 USER'S MANUAL

SECTION 2.0

2.1 LAYOUT OF HT12 286 MOTHERBOARD



2.2 JUMPER/CONNECTOR DESCRIPTION

J4		External Batttery Connector
J2		Key Board Connector
JP4		BIOS select 27512 27256
J20		Turbo LED
J21		Reset
J19		Turbo Switch [Ctrl][Alt][+] Lo-Speed (Keyboard Control) [Ctrl][Alt][-] Hi-Speed (Keyboard Control) Hi-Speed only
J23		Power LED/Keylock
J22		Speaker
J3		Monochrome Color
JP3		80287 CLOCK SOURCE Using the PROCLK Using the OSC4 Clock Output
JP2		80287 CLOCK MODE Indicate whether 80287 Clock input is to be divided by 3 or directly. directly divided by 3
JP1		CPU CLOCK SELECT 16 MHz 12 MHz

J2 Key Board Connector

Pin #	Assignments
1	Key Board Clock
2	Key Board Data
3	Spare
4	GND
5	+5V

J4 Battery Connector

Pin #	Assignments
1	+6V D.C. Battery Input
2	N/C
3	N/C
4	GND

J15 Power Connector

PS1	
Pin #	Assignment
1	Power Good
2	+5V
3	+12V
4	-12V
5	GND
6	GND

PS2	
Pin #	Assignment
7	GND
8	GND
9	-5V
10	+5V
11	+5V
12	+5V

J23 Keyboard Lock & power LED

Pin #	Assignments
1	LED Power
2	Spare
3	GND
4	Key Board Lock
5	GND

J22 Speaker Connector

Pin #	Assignments
1	Signal
2	N/C
3	GND
4	+5V

SECTION 3.0

3.1 FIRST TIME START-UP

The first time you start your system, you will need to follow some special procedures to specify your system configuration, initialize and format your hard disk, and install system software. This section explains these special procedures. Do not proceed until you are certain that your system has been properly installed and connected to an appropriate power source.

In this section, there are 3 procedures you will follow:

1. Turn on the system power.
2. Run the setup program to specify various system configuration parameters.
3. Initialize and format your hard disk.

3.2 TURNING ON THE POWER

Turn on the system power by first turning on the video display power switch, then turning on the power switch on the side or back of the system unit. The system will go through it's automatic power on self test (POST) and then attempt to boot (that is, to load the operating system from a disk drive).

Since your disks are not formatted, and the system doesn't yet know what type of disks your system has, you will get an error message when POST completes.

You are now ready to run the SETUP program. The following sections give the setup procedure instructions for the QUADTEL BIOS.

3.3 QUADTEL 286 SETUP

The SETUP program lets you specify your system's configuration of diskette drives, hard disk drives, video display, memory, date, time, and other setup informations. The SETUP program is build-in BIOS -- Diskette is not necessary for the SETUP.

NOTE
The following procedure is assuming the your system has the QUADTEL 286 BIOS installed. If your system has had a different BIOS installed, these procedures will not work.

To run SETUP, simultaneously press the CTRL, ALT, and S keys, the following window will be displayed:

```
Extended BIOS Setup - Copyright 1989, 1990 Quadtel Corporation

Current Date: [09/13/1990]                Video System: [Monochrome]
Current Time: [17:57:35]

[ 640  k] System Memory                   Power Up Speed: [ Fast ]
[ 1024 k] Extended Memory                 Bios Shadow:    [ System in Ram]
[ 2048 k] EMS Memory                                      [Video on Rom]
  128 k   Shadow Memory                   Wait States:    [0, All Banks]

Diskette Driver 0: [1.2 MB, 5 1/4 ]
Diskette Driver 1: [1.2 MB, 5 1/4 ]

Fixed Disk 0: Type:[ 40]  CY: 1024  HD: 9  ST: 17  LZ: 1023  WP: None
Fixed Disk 1: Type: [None]

      Move          F5 Previous Value          F9 Automatic Configuration
F1    Help          F6 Next Value              F10 Save Configuration
Esc   Exit
```

The Setup screen will allow you to modify the time, date, and setup information contain in the clock CMOS RAM. This information is used by the system BIOS for system configuration.

Use the arrow keys to select the item you want to change. When the item is selected, press F5 to select the previous (smaller) value and F6 to select the next (larger) value.

Press F9 to automatically configure the system. This will determine the amount of memory in the system and set default values for the system memory, extended memory, and video type. Auto configuration for the fixed disk is not performed and must be set manually.

Automatic configuration is especially useful if you are adding or subtracting memory. Simply add a memory board or add memory to the system board, invoke the setup utility and press F9 to set the proper memory configuration.

Press F10 to save the current configuration. The configuration, with the exception of the time and date, is not saved until F10 is pressed. Press ESC to exit from the SETUP program. If you have not saved the changes you made, you can do so at this time.

3.4 QUADTEL BIOS HARD DISK DRIVE TABLE

The Quadtel 286 BIOS supports a total of 46 drive type and one user definable drive type (Type 47). On the following page there is a table containing the standard 46 drive type provided.

The user definable drive type allows the user to create drive parameters for both fixed disk 0 of fixed disk 1. Using the built in SETUP program, you can specify the cylinders, heads, sectors, write precomp, and landing zone for a specific drive.

Default Hard Disk Drive Table

Type	Cylinders	Heads	Sectors	Write Precomp	Landing Zone
1	306	4	17	128	305
2	615	4	17	300	615
3	615	6	17	300	615
4	940	8	17	512	940
5	940	6	17	512	940
6	615	4	17	-1	615
7	462	8	17	256	511
8	733	5	17	-1	733
9	900	15	17	-1	901
10	820	3	17	-1	820
11	855	5	17	-1	855
12	855	7	17	-1	855
13	306	8	17	128	319
14	733	7	17	-1	733
15	Reserved				
16	612	4	17	0	663
17	977	5	17	300	997
18	977	7	17	-1	997
19	1024	7	17	512	1023
20	733	5	17	300	732
21	733	7	17	300	732
22	733	5	17	300	733
23	306	4	17	0	336
24	612	4	17	305	663
25	612	2	17	300	612
26	614	4	17	-1	614
27	820	6	17	-1	820
28	977	5	17	-1	977
29	1218	15	36	-1	1218
30	1224	15	17	-1	1224
31	823	10	17	512	823
32	809	6	17	128	809
33	830	7	17	-1	830
34	830	10	17	-1	830
35	1024	5	17	-1	1024
36	1024	8	17	-1	1024
37	615	8	17	128	615
38	1024	8	26	-1	1024
39	925	9	17	-1	925
40	1024	9	17	-1	1023
41	918	15	17	-1	917
42	1024	15	17	-1	1023
43	823	10	34	-1	822
44	969	5	34	-1	968
45	969	7	34	-1	968
46	969	9	34	-1	968

3.5 QUADTEL BIOS CHECKPOINT CODES (For System integrator or Dealer)

During the Power On Seft Test (POST), the BIOS signals a checkpoint by outputting a code to I/O address 80H. This code can be used to establish how far the BIOS executed throught the power on sequence and what test is currently being performed. This is done to help to troubleshoot faulty system boards. You can purchase a CHECKPOINT CARD to perform the checkpoint function.

The following is a list of the checkpoint codes which are written before their respective tests:

POST Error Codes	
02	Flag test
04	Register test
06	System hardware initialization
08	Initialize chip set registers
0A	BIOS ROM checksum
0C	DMA page register test
0E	8254 timer test
10	8254 timer initialization
12	8237 DMA controller test
14	8237 DMA initialization
16	Initialize 8259/Reset coprocessor
18	8259 interrupt controller test
1A	Memory refresh test
1C	Base 64KB address test
1E	Base 64KB memory test
20	Base 64KB test (upper 16 bits)
22	8742 Keyboard self test
24	MC146818 CMOS test
26	Start first protected mode test
28	Memory Sizing test
2A	Autosize memory chips
2C	Chip interleave enable test
2E	First protected mode test exit
30	Unexpected shutdown
32	System board memory size
34	Relocate shadow ram if configured
36	Configure EMS system
38	Configure wait states

Continuation of Post Error Codes...	
3A	Retest 64K base ram
3C	CPU speed calculation
3E	Get switches from 8042
40	Configure CPU speed
42	Initialize interrupt vectors
44	Verify video configuration
46	Initialize video system
48	Test unexpected interrupts
4A	Start second protected mode test
4C	Verify LDT instruction
4E	Verify TR instruction
50	Verify LSL instruction
52	Verify LAR instruction
54	Verify VERR instruction
56	Unexpected exception
58	Address line 20 test
5A	Keyboard ready test
5C	Determine AT or XT keyboard
5E	Start third protected mode test
60	Base memory test
62	Base memory address test
64	Shadow memory test
66	Extended memory test
68	Extended address test
6A	Determine memory size
6C	Display error messages
6E	Copy BIOS to shadow memory
70	8254 clock test
72	MC146818 real time clock test
74	Keyboard struck key test
76	Initialize hardware interrupt vectors
78	Math Coprocessor test
7A	Determine COM ports available
7C	Determine LPT ports available
7E	Initialize BIOS data area
80	Determine floppy/fixed controller
82	Floppy disk test
84	Fixed disk test
86	External ROM scan
88	System key lock test
8A	Wait for F1 key pressed
8C	Final system initialization
8E	Interrupt 19 boot loader
B0	Unexpected interrupt

All numeric entries are hexadecimal.

If error 1C, 1E, of 20 (base 64K RAM error) is detected by the BIOS, an additional word of information will be displayed to the screen and to port 80H. This word will reflect the bit or address line which failed. For example, if "1C 0002" is displayed, address line 1 (represented by bit one) has failed. If "20 1020" is displayed, then data bits 12 and 5 have failed in the upper 16 bits. Note that error 20 can only occur on 386 systems because they have a 32 rather than a 16 bit bus.

The same information will be output to port 80H. The checkpoint code will be output followed by a delay, the high order byte, another delay, and then the low order byte of the error. This will be repeated continuously.

SECTION 4.0

I/O ADDRESS MAP AND I/O CHANNEL CONNECTORS

I/O ADDRESS MAP

Hex Range	Device
000-01F	DMA Controller 1,8237A-5
020-03F	Interrupt controller 1,8259A, Master
040-05F	Timer, 8254
060-06F	8042 (keyboard)
070-07F	Real-time clock, non-maskable interrupt (NMI) mask
080-09F	DMA page register, 74LS612
0A0-0BF	Interrupt controller 2, 8259A
0C0-0DF	DMA controller 2, 8237A-5
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor
1F0-1F8	Fixed disk
200-207	Game I/O
278-27F	Parallel printer port 2
2F8-2FF	Serial port 2
300-31F	Prototype card
360-36F	Reserved
378-37F	Parallel printer port 1
380-38F	SDLC, bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome display and printer adapter
3C0-3CF	Reserved
3D0-3DF	Color/graphics monitor adapter
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1

I/O CHANNEL CONNECTORS

A SIDE, (SLOT J5,7,9,11,13,15,17)

I/O Pin	Signal Name	Input Output
A1	-I/O CH CK	Input
A2	SD7	Input/Output
A3	SD6	Input/Output
A4	SD5	Input/Output
A5	SD4	Input/Output
A6	SD3	Input/Output
A7	SD2	Input/Output
A8	SD1	Input/Output
A9	SD0	Input/Output
A10	-I/O CH RDY	Input
A11	AEN	Output
A12	SA19	Input/Output
A13	SA18	Input/Output
A14	SA17	Input/Output
A15	SA16	Input/Output
A16	SA15	Input/Output
A17	SA14	Input/Output
A18	SA13	Input/Output
A19	SA12	Input/Output
A20	SA11	Input/Output
A21	SA10	Input/Output
A22	SA9	Input/Output
A23	SA8	Input/Output
A24	SA7	Input/Output
A25	SA6	Input/Output
A26	SA5	Input/Output
A27	SA4	Input/Output
A28	SA3	Input/Output
A29	SA2	Input/Output
A30	SA1	Input/Output
A31	SA0	Input/Output

B SIDE, (SLOT J5,7,9,11,13,15,17)

I/O Pin	Signal Name	Input Output
B1	GND	Ground
B2	RESET DRV	Output
B3	+5Vdc	Power
B4	IRQ9	Input
B5	-5Vdc	Power
B6	DRQ2	Input
B7	-12Vdc	Power
B8	0WS	Input
B9	+12Vdc	Power
B10	GND	Ground
B11	-SMEMW	Output
B12	-SMEMR	Output
B13	-IOW	Input/Output
B14	-IOR	Input/Output
B15	-DACK3	Output
B16	DRQ3	Input
B17	-DACK1	Output
B18	DRQ1	Input
B19	-REFRESH	Input/Output
B20	CLK	Output
B21	IRQ7	Input
B22	IRQ6	Input
B23	IRQ5	Input
B24	IRQ4	Input
B25	IRQ3	Input
B26	-DACK2	Output
B27	T/C	Output
B28	BALE	Output
B29	+5Vdc	Power
B30	OSC	Output
B31	GND	Ground

C SIDE, (SLOT J6,8,10,12,14,16,18)

I/O Pin	Signal Name	Input Output
C1	SBHE	Input/Output
C2	LA23	Input/Output
C3	LA22	Input/Output
C4	LA21	Input/Output
C5	LA20	Input/Output
C6	LA19	Input/Output
C7	LA18	Input/Output
C8	LA17	Input/Output
C9	-MEMR	Input/Output
C10	-MEMW	Input/Output
C11	SD08	Input/Output
C12	SD09	Input/Output
C13	SD10	Input/Output
C14	SD11	Input/Output
C15	SD12	Input/Output
C16	SD13	Input/Output
C17	SD14	Input/Output
C18	SD15	Input/Output

D SIDE, (SLOT J6,8,10,12,14,16,18)

I/O Pin	Signal Name	Input Output
D1	-MEM CS16	Input
D2	-I/O CS16	Input
D3	IRQ10	Input
D4	IRQ11	Input
D5	IRQ12	Input
D6	IRQ15	Input
D7	IRQ14	Input
D8	-DACK 0	Output
D9	DRQ 0	Input
D10	-DACK 5	Output
D11	DRQ 5	Input
D12	-DACK 6	Output
D13	DRQ 6	Input
D14	-DACK 7	Output
D15	DRQ 7	Input
D16	+5Vdc	Power
D17	-MASTER	Input
D18	GND	Ground

CMOS RAM Address Map

Addresses	Description
00-0D	*Real-time clock information
0E	*Diagnostic status byte
0F	*Shutdown status byte
10	Diskette drive type byte, drives A and B
11	Reserved
12	Fixed disk type byte, drives C and D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	*Low expansion memory byte
31	*High expansion memory byte
32	*Date century byte
33	*Information flags (set during power on)
34-3F	Reserved

Real-Time Clock Information
(Addresses 00-0D)

Byte	Function	Address
0	Seconds	00
1	Second alarm	01
2	Minutes	02
3	Minute alarm	03
4	Hours	04
5	Hours alarm	05
6	Day of week	06
7	Date of month	07
8	Month	08
9	Year	09
10	Status register A	0A
11	Status register B	0B
12	Status register C	0C
13	Status register D	0D

SECTION 5.0

DMA CHANNELS, SYSTEM INTERRUPTS, AND SYSTEM TIMER
DMA CHANNELS

Channel	Function
0	Spare (8-bit transfer)
1	SDLC (8-bit transfer)
2	Floppy disk (8-bit transfer)
3	Spare (8-bit transfer)
4	Cascade for DMA controller 1
5	Spare (16-bit transfer)
6	Spare (16-bit transfer)
7	Spare (16-bit transfer)

DMA CONTROLLER REGISTERS

Hex Address	Command Codes
0C0	CH0 base and current address
0C2	CH0 base and current word count
0C4	CH1 base and current address
0C6	CH1 base and current word count
0C8	CH2 base and current address
0CA	CH2 base and current word count
0CC	CH3 base and current address
0CE	CH3 base and current word count
0D0	Read status register/Write command register
0D2	Write mode register
0D4	Read temporary register/Write command register
0D6	Write mode register
0D8	Clear byte pointer flip-flop
0DA	Read status register/Write command register
0DC	Write mode register
0DE	Write all mask register bus

PAGE REGISTER ADDRESSES

Page Register	I/O Address
DMA Channel 0	0087
DMA Channel 1	0083
DMA Channel 2	0081
DMA Channel 3	0082
DMA Channel 5	008B
DMA Channel 6	0089
DMA Channel 7	008A
Refresh	008F

INTERRUPTS

Level	Function
0	System timer output 0
1	Keyboard output buffer full
2	Interrupt from Controller 2 (levels 8-15)
3	Serial port 2
4	Serial port 1
5	Parallel port 2
6	Diskette controller
7	Parallel port
8	Real-time clock
9	Software redirected to INT 0AH
10	Reserved
11	Reserved
12	Reserved
13	80287
14	Hard Disk Controller
15	Reserved

TIMERS

Channel	Function
0	System timer
1	Refresh request generator
2	Tone generation for speaker

SECTION 6.0

EMS 4.00 DEVICE DRIVER

The Memory Management System is a device driver which manages the expanded memory space available for the HT12 286 system.

EMS DRIVER INSTALLATION

In order to use the Expanded memory, you must complete the procedure listed below.

1. Copy the HT12EMS.SYS driver from the factory supplied utility diskette onto your bootable disk drive.

   If you boot from the hard disk drive, Drive C:, insert the factory supplied diskette into Drive A:. Then, type **COPY A:\HT12EMS.SYS C:**. Then, press ENTER.

   If you do not have a hard disk drive, you may use two floppy diskette drives, Drive A: and Drive B:. Insert your DOS bootable diskette into drive A:. Insert the factory supplied diskette into Drive B:. Then, type **COPY B:\HT12EMS.SYS**, and then press ENTER.

   If you have only one floppy diskette drive, Drive A:, insert the factory supplied diskette into Drive A:. Then, type **COPY A:\HT12EMS.SYS B:**, and then press ENTER. Now, insert your DOS or bootable diskette into Drive A:. Finally, strike any key.

Add the following line to your CONFIG.SYS file on your boot drive:

DEVICE = HT12EMS.SYS

Without anything else included in this command line, the EMS driver will get loaded with the default hardware values of the I/O address that enables the EMS and the memory address used for EMS paging.

EMS DRIVER INSTALLATION (CONT.)

If you already have a CONFIG.SYS file, use a text editor (which creates pure ASCII text) to add the new line to your existing CONFIG.SYS file. Or, use the the COPY CON command described below to create a new CONFIG.SYS file. Add the other lines from the old file as needed.

Insert a new line at the top of a CONFIG.SYS file. If you experience compatibility problems with the CONFIG.SYS file's other device drivers, move the EMS line down one line and try it again. Reshuffling the lines in your CONFIG.SYS file may solve device driver conflicts.

If you do not have a CONFIG.SYS file, create one. Follow the procedure listed below.

a. If you boot drive is Drive A:, then type **COPY CON A:\CONFIG.SYS.**

b. Press ENTER.

c. Type **DEVICE = HT12EMS.SYS.**

d. Press ENTER.

e. At this time, type any other lines you wish to add to the CONFIG.SYS file. If you do not want to add any other lines, then go on to the next step.

f. Press the <F6> key or type ^Z. this generates a ^Z which signifies the end of a command sequence.

Run the Setup Utility. Refer to Running SETUP in SECTION 3. Set the following options in the Setup Utility:

[XXXXK] EMS Memory

4. When the EMS Driver is executed, a title and copyright notice will appear on the screen as follows:

Quadtel Expanded Memory Manager Version 4.00 (HT12 03.01)
Copyright 1989, 1990 Quadtel Corporation. All Rights Reserved.

Testing Memory : XXXXK

SECTION 7.0
CHIPS TECHNICAL INFORMATION

7.1 FEATURES

- Single chip 80286 PC/AT Compatible Solution
- Supports CPU speeds to 16 MHz 0 or 1 Wait State
- Up to 4 Meg on-board Memory
- EMS with 4 Registers
- Supports 1M, 256K, and 64K devices in mixed modes
- Independent Clocking Source for the AT Bus
- Shadow RAM support for system and video BIOS in 16K blocks
- 384K remapping in 64K blocks
- Hot Reset, Fast A20 Gate
- HCMOS design for high speed and low power consumption

7.2 DESCRIPTION

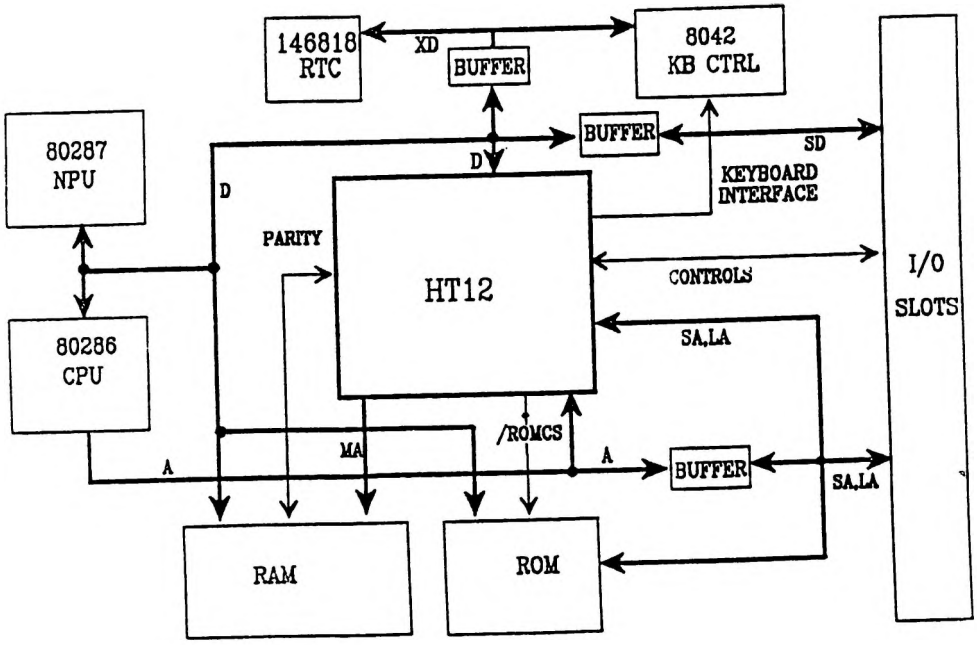
The HT12, an IBM PC/AT compatible chip, supports the 80286 CPU at clock speeds to 16MHz. This highly integrated chip solution offers high performance and reliability, with low cost, minimal power consumption, and low board-space requirements.

A full PC/AT compatible system is implemented with this chip by adding a CPU/NPU, KBD CNTRL, RTC, BIOS, Memory and a few low cost TTL devices.

This Chip supports 64K, 256K, and 1M, x1 and x4, DRAM's in configurations up to 4 Meg. A 12.5 MHz 0 wait-state system can be implemented using 80ns DRAM's while a 10MHz 0 wait-state system requires 100ns DRAM's. The memory controller also supports the shadow RAM feature and the Split Memory option. The Split Memory option allows the System RAM located between 640K and 1M to be remapped above top of memory.

The HT12 contains CPU and peripheral support functions; including DMA controllers, a memory mapper, timer/counters, interrupt controllers, and a bus controller. This chip replaces board address buffers, data transceivers, memory drivers, parity generators and their support circuits. Thsi chip is packaged in a 160 pin Flat Pack.

7.3 SYSTEM BOARD BLOCK DIAGRAM



7.4 MEMORY CONFIGURATIONS

The HT12 supports 8 different RAM configurations using combinations of 64K, 256K, and 1M x1 or x4 DRAM's. The RAM configuration is determined by three configuration pins (DACK: 2-0) on power up. The RAM configuration informations is stored in the read/write System Configuration Register (index 04K and is overidable by software). The following is a table of valid RAM combinations.

Configuration	/DACK (Read)			Bank 0	Bank 1	Total
	2	1	0	OK	OK	OK
0	0	0	0	256K	OK	512K
1	0	0	1	256K	64K	640K
2	0	1	0	256K	256K	1M
3	0	1	1	256K	1M	2.5M
4	1	0	0	1M	OK	2M
5	1	0	1	1M	1M	4M
6	1	1	0	--	--	Reserved
7	1	1	1			

BIOS Shadowing and Memory Relocation

The HT12 supports BIOS shadowing in 16K blocks in the range of C0000 to FFFFF. In the case that 1M of memory is installed, the HT12 also supports relocation of memory from address A0000 to address FFFFF that are not used in shadowing to above 1M. The table on the following page shows the various shadowing and relocation combinations. Basically, contiguous memory above A0000 that are not used in shadowing can be relocated in 64K blocks. However the combination of shadowing in only C0000-CFFFF and F0000-FFFFF can have both A0000-BFFFF and D0000-EFFFF relocated.

Shadow Range	Reloc Range	Memory Relocated
No shadowing	A0000-FFFFF	384K
C0000-	A0000-BFFFF	128K
D0000-	A0000-CFFFF	192K
E0000-	A0000-DFFFF	256K
F0000-	A0000-EFFFF	320K
C0000-CFFFF, F0000-FFFFF	A0000-BFFFF, D0000-EFFFF	256K

For shadowing operations, the BIOS should first select the required shadowing ranges in Shadow RAM Configuration Registers 1 to 2. When an address range is selected for shadowing, it becomes accessible and write only. This allows the BIOS to load ROM data into the shadow RAM. After all the shadow RAM are loaded, the BIOS enables the shadowing feature by setting the Shadow Enable bit in the Misc Feature Enable Register, Index 14H. Once shadowing is enabled, the shadow RAM becomes read only and all read cycles to the selected address ranges will be directed to the shadow RAM.

7.5 SYSTEM CONFIGURATION REGISTER (INDEX: 10H)

Bit	7	6	5	4	3	2	1	0
		WS CTRL1	WS CTRL0	0WS MEM	BUS SPEED	RAM SEL2	RAM SEL1	RAM SEL0

Bits	Access	Default	Description (As Inputs during Power On Reset)
2-0	R/W	DACK2-0	RAM Configuration RAMSEL <2:0> — Bank 0 RAM Type — Bank 1 RAM Type — Total Size 0 — OK — OK — OK 1 — 256K — OK — 512K 2 — 256K — 64K — 640K 3 — 256K — 256K — 1M 4 — 256K — 1M — 2.5M 5 — 1M — ok — 2M 6 — 1M — 1M — 4M 7
3	R/W	DACK3	AT Bus Speed 1: Low Speed on I/O 0: Full Speed
4	R/W	DACK5	0 Wait State Memory 1: 0 wait state memory 0: 1 wait state memory
6-5	R/W	DACK6-7	Wait State Controls WSCTRL (1:0) 00:1 extra Wait State for EMS + relocation cycles 01: 1 extra Wait State for EMS cycles only 10: 1 extra Wait State for Relocation cycles only 11: No extra Wait State
7	R/W	TC	Reserved

Special Note: The DACK and TC lines are used as configuration inputs during power up reset.

The DACK and TC configuration lines are sampled on the rising edge of POWERGOOD. Each DACK configuration line has an internal pull-up that the P11 sees as a logic 1 on power up. To put a logic 0 on a DACK configuration line, a 5K external pull-down resistor can be used. The TC configuration line, on the other hand, has an internal pull-down that the P11 sees as a logic 0 on power up. A 5K external pull-up resistor can be used to put a logic 1 on the TC configuration line.

7.6 EMS CONFIGURATION REGISTER (INDEX: 19H)

Bit	7	6	5	4	3	2	1	0
	EMS EN	PAGE ADDR2	PAGE ADDR1	PAGE ADDR0	PAGE3 EN	PAGE2 EN	PAGE1 EN	PAGE0 EN

Bits	Access	Default	Description
0	R/W	0	Page Enable 0 1:Enable 0:Disable If the Global EMS Enable is on (1), the enable bit associated with each EMS page enables or disables the corresponding page.
1	R/W	0	Page Enable 1 1:Enable 0:Disable
2	R/W	0	Page Enable 2 1:Enable 0:Disable
3	R/W	0	Page Enable 3 1:Enable 0:Disable
4-6	R/W	0	EMS Pages Starting Address 0(000):C000:0000 1(001):C400:0000 2(010):C800:0000 3(011):CC00:0000 4(100):D000:0000 This starting address specifies the address of EMS page 0. EMS page 1 to 3 follow consecutively in 16K increments.
7	R/W	0	Global EMS Enable 1:Enable 0:Disable If the Global EMS Enable is off (0), all EMS pages are disabled regardless of their individual enable bit.

EMS PAGE REGISTERS 0-3 (INDEX:20H-23H)

Bit	7	6	5	4	3	2	1	0
	PA 21	PA 20	PA 19	PA 18	PA 17	PA 16	PA 15	PA 14

Bits	Access	Default	Description
0-7	R/W		Translated EMS address lines