GA-386ES USER'S MANUAL

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PRINT IN TAIWAN

KEY FEATURE

HARDWARE

1. SPEED:
   (1). CPU (SYSTEM): 33 MHz 0 wait state, (25 MHz switchable).
   (2). I/O (SLOT) : 8.2MHz (33MHz) for TURBO MODE.
   6.2MHz (25MHz) for NORMAL MODE.

2. RAM:
   (1). DRAM SIZE : 1-32 MB MODUAL DRAM on board.
   (2). DRAM TYPE : 70ns or 80ns SIMM MODULE DRAM.

3. NUMERIC COPROCESSOR:
   (1). 80387 : Socket on board for 80387-33.
   (2). WEITEK : Scoket on board for WEITEK 3167/33MHz.

4. SRAM : 64KB or 128KB cache memory.

5. SHADOW RAM:
   (1). BIOS : System BLOS shadow programmable.
   (2). VIDEO : Video BIOS shadow programmable.

6. REMAP DRAM : 128KB-384KB added to EXTENTION memory.

7. 64KB LEGAL BIOS.

SOFTWARE

SETUP:

AT SETUP AND EXTENDED SETUP IN BIOS.

INTRODUCTION

The memory system of a computer plays a critical role in effecting the peak throughput. The design of the memory board is frequently the starting point in machine designs. The central problem is to:

A. Bring the input data from the outside world into memory.

B. Buffer the data there until they can be passed to a processor.

C. Compute the output data and buffer them in memory until they can be delivered outside the computer.

D. Transmit the output data from memory to the outside world.

The bandwidth between memory and the outside world limits how fast we can obtain input and deliver output. The memory system also limits how fast data can be delivered to a processor. Since instructions are also stored in memory, the architect must provide for concurrent demands on memory for data to process, instruction to execute, and input/output transfers between memory and the external world.

WHY CACHE MEMORY ?

Use of cache and virtual memory produce a very efficient hierarchical memory system. These systems are composed of a mix of memory devices that range in performance and cost. A well-designed memory system of this type tends to perform as if the entire memory were composed of the fastest devices in the structure, yet its cost tend to be dominated by slower, less expensive devices.

Conventional memory systems have been implemented with dynamic RAMs (DRAM), which provide a large amount of memory for a small amount of board space andmoney. To achive the faster computer throughput that systemusers are forever demanding, designers are developing memory subsystems that employ cache schemes. Caching promises to eliminate wasteful microprocessor wait states required by slow DRAM. It is also a low cost alternative to building a processor's complete memory system consisting of expensive static RAMs (SRAM).

WHAT'S CACHE MEMORY ?

The idea of cache memories is that some active portion of a low-speed memory is stored in duplicate, in a higher-speed cache memory. When a memory request is generated, the request is first presented to the cache memory, and if the cache cannot respond, the request is then presented to main memory.

HOW CACHE MEMORY DOES IT ?

Analysis of a large number of typical programs has shown that most of their execution time is spent in a few main routines. When execution is localized within these routines, a number of instructions are executed repeatedly. This may be in the form of a simple loop, nested loops, or a few procedures that repeatedly call each other. The actual detailed pattern of instruction sequencing is not important. The main observation is that many instructions in each of a few localized areas of the program are repeatedly executed, while the remainder of the program is accessed relatively infrequently. This phenomenon is referred to as the locality of reference.

Now, if it can be arrenged to have active segments of programs in cache memory, then the total execution time can be significantly reduced. Cache memory is inserted. between the CPU and the main memory, as shown in Figure 1.1. To make this arrangement effective, the cache memory must be considerably faster than the main memory. Their relative access times usually differ by a factor of 5 to 10. This approach is more economical than making the entire main memory as fast as the cache.

Conceptually, operation of a cache memory is very simple. The memory control circuitry is designed to take advantage of the property of locality

of reference. When a read request is received from the CPU, the contents of a block of memory words containing the specified are transferred into the cache memory. When any of the locations in this block is reference by the program, its contents are read directly from the cache. Usually, the cache memory can store a number of such blocks at any given time. The correspondence between the main memory blocks and and those in the cache memory is specified by means of a MAPPING function. When the cache memory is full and a memory word (instruction or data) is referenced that is not in the cache, a decision must be made as to which block should be removed to create space for the new block that contains the referenced word. The collection of rules for making this decision constitute the REPLACEMENT ALGORITHM.

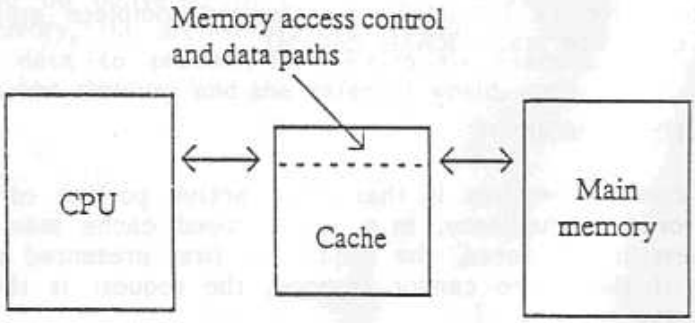


Figure 1.1.

WHAT'S PAGE/INTERLEAVED OPERATION

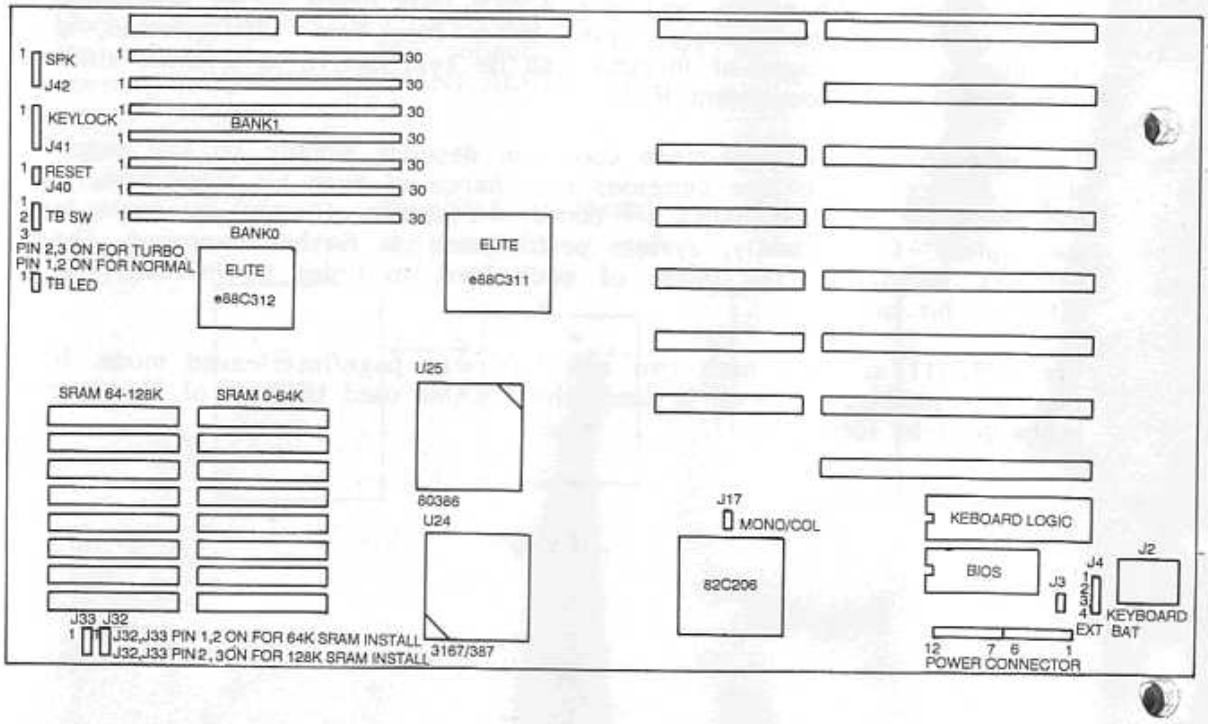
During DRAM read or write cycles, a row address and a column address is required. In most DRAMs, the row address access time is longer the column address access time. Therefore bus performance can be improved by using page-mode DRAM operation. Memory locations sharing the same row address are in the same memory page, therefore only a new column address is required. In page-mode operation, the row address strobe, RAS*, can be kept active, and only a new cas* needs to be generated, thus reducing memory cycle time. In a four bank configuration, a maximum of four pages of memory can be kept active at a time, since each bank has an independent RAS*.

The effectiveness of page-mode operation depends heavily on the page-size. A larger page size increases the chance of page hit. Therefore, if the pages for the four banks are concatenated, the effective hit space is quadrupled. Consequently, system performance is further improved. The e88C311 interleaves the pages of each bank in order to increase the effective hit space.

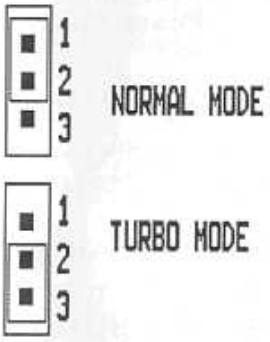
The e88C311 supports both two and four way page/interleaved mode. If four way interleaved mode is used, the DRAMs used in each of the four banks must be identical.

PART I:SETUP

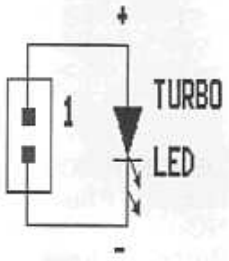
1. H/W CONFIGURATION:



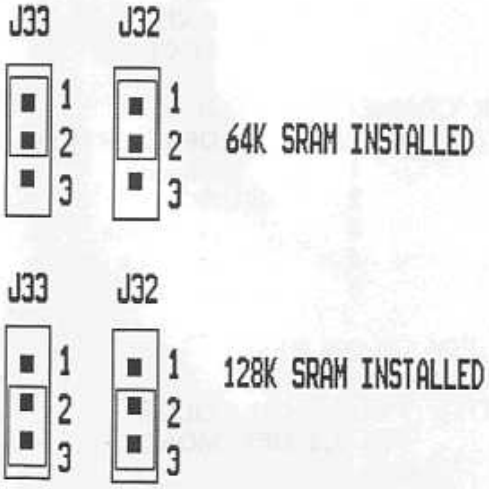
1. TB SW



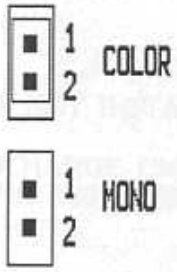
2. TB LED



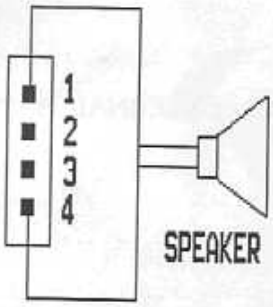
3.



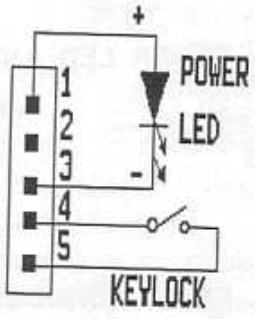
4. J17 MONO/COL



5. J42



6. J41



2. CONNECTORS PINOUT:

(1). POWER CONNECTOR:

PIN NO.	Description
1	Power Good
2	+5V
3	+12V
4	-12V
5	Ground
6	Ground
7	Ground
8	Ground
9	-5V
10	+5V
11	+5V
12	+5V

(2). KEYBOARD CONNECTOR :

PIN NO.	DESCRIPTION
1	Keylock
2	Key Data
3	RST
4	+5V
5	GND

(3). EXTERNAL BATTERY CONNECTOR (J4) :

PIN NO.	DESCRIPTION
1	Battery Plus
2	NC
3	Battery Minus
4	Battery Minus

(4). SPEAKER CONNECTOR (J42) :

PIN NO.	DESCRIPTION
1	DATA
2	NC
3	GND
4	VCC(+5V)

(5). POWER LED AND KEYLOCK CONNECTOR (J41) :

PIN NO.	DESCRIPTION
1	+Anode
2	NC
3	-Cathode
4	Keylock
5	GND

(6). RESET CONNECTOR (J40) : PIN 1,2 ON RESET

(7). CRT TYPE CONNECTOR (J17) : PIN 1,2 ON COLOR
PIN 1,2 OFF MONO

(8). TURBO LED (J34) : PIN 1 +ANODE
PIN 2 -CATHODE

(9). EXT BATT INSTALLED OR NOT (J3) :

CLOSE FOR NORMAL SETTING, EXT BATT NOT INSTALLED.

OPEN FOR EXT BATT INSTALLED OR DISCHARGE CMOS VALUE
(ALSO SAVING BATTERY POWER FOR LONG DISTANCE TRANSPOE

(10).SRAM SIZE SETTING (J32,J33) :

BOTH J32 AND J33 PIN 1,2 ON FOR 64K SRAM INSTALL.
BOTH J32 AND J33 PIN 2,3 ON FOR 128k SRAM INSTALL.

(11).TB SW CONNECTOR : PIN 1,2 ON FOR NORMAL.
PIN 2,3 ON FOR TURBO.

3. S/W CONFIGURATION

(1). COMOS SETUP is included in BIOS, please refer the following description and figure.

CMOS SETUP (C) Copyright 1985-1989, American Megatrends Inc.

Date (mn/date/year) : Mon, Jan 01 1990
Time (hour/min/sec) : 10 : 10 : 10
Floppy drive A : 1.2 MB, $5^1/_4$"
Floppy drive B : Not Installed

Hard disk C: type : 2
Hard disk D: type : Not Installed
Primary display : Monochrome
Keyboard : Installed

Scratch RAM option: 1

Base memory Size : 640 KB
Ext. memory Size : 256 KB
Numbric Processor : Installed

Cyln head Wpcom Izone sect Size
615 4 380 615 17 20MB

Sun	Mon	Tue	Wed	Thu	Fri	Sat
30	1	2	3	4	5	6
7	8	9	10	11	12	13
14	15	16	17	18	19	20
21	22	23	24	25	26	27
28	29	30	31	1	2	3
4	5	6	7	8	9	10

Month : Jan, Feb,.....Dec
Date : 01, 02, 03,.....31
Year : 1901, 1902, ...2099

ESC = Exit, ↓→↑← Select, PgUp/PgDn

ITEM A. Date (Mn/date/year): use UP, DOWN, LEFT, RIGHT ARROW KEY to move cursor and PgUp/PgDn KEY to increase/decrease DATE, MONTH, YEAR.

ITEM B. Time (hour/min/sec): use ARROW KEY to move cursor and PgUp/PgDn KEY to increase / decrease HOUR, MIN, SEC.

ITEM C. Floppy drive A: use PgUp/PgDn KEY to select Floppy drive A type, including 360KB/ 5¼", 1,2MB/ 5¼", 720KB/ 3½", 1.44MB/ 3½" and not installed.

ITEM D. Floppy drive B: the same as ITEM C.

ITEM E. Hard disk C: type: use PgUp/PgDn KEY to select Hard disk C: type, including Type 1, Type 2, Type 3 ....., Type 47 and not installed.

ITEM F. Hard disk D: type: the same as ITEM E.

ITEM G. Primary display: use PgUp/PgDn KEY to select MONITOR type, including Monochrome, Color 40x25, VGA or EGA, Color 80x25 and not installed.

ITEM H. Keyboard: use PgUp/PgDn KEY to installed or not installed Keyboard.

ITEM I. Scratch RAM option: use PgUp/PgDn KEY to select 1 or 2, 1 for using BIOS stack area at 0030:0000, 2 for reducing base memory size by 1KB when BIOS require use 256 bytes of RAM. 1 is the BIOS default value.

When setup is finished, you should press <ESC> key the reverse area, which is for comment, will appears a message like follow:

Write data into COMOS and exit?(y/n)

if you press "y" then press <ENTER> the configuration you just setup will be saved to COMOS and system will reset.

(2). XCMOS SETUP is also included in BIOS, please refer the following description.

There are three setup menus in XCMOS setup. The first is AT BUS AND LOCAL MEMORY SETUP, the second is CACHE AND PERIPHERAL IO SETUP and the last is BIOS AREA DRAM SHADOW AND REMAP.

A. AT BUS AND LOCAL MEMORY SETUP.

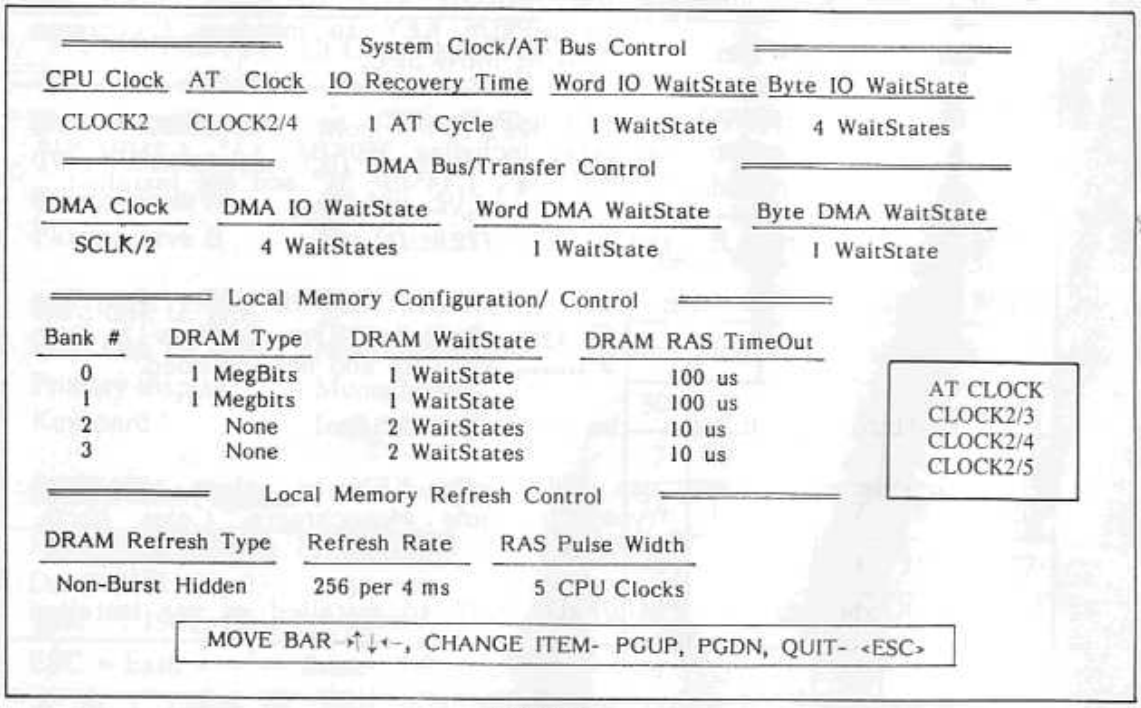


Figure A.

WARNING !!!

The improper setting-up would cause the computer system hanging up, Please be cautions with the following parameters when setting-up:

1) Cache Mode -- Direct Map.

Don't set up as 2-way mode.

2) BIOS area remapping -- Enable.

Don't set up as disable.

3) For some brands DRAM, DRAM wait state need to set 2 wait state.

4) For some AT compatible software (i.e. OS/2)

You must disabled memory size > 16MB.

B. Cache Memory and Peripheral IO Ports Setup Menu

Cache Control Setup

Cache Controller	Cache Mode	SRAM WaitStates	Page-Interleaved Mode
Enabled	Direct Map	0 WaitState	Page-Interleaved

Cache/Local Memory Control

Block #	Block Setup Mode	Block Size	Starting Address
0	Non - Cache Area	128 KBytes	00A0000H
1	Non - Cache Area	256 KBytes	00C0000H
2	Function Disabled	4 KBytes	7FFF000H
3	Function Disabled	4 KBytes	7FFF000H

Programable IO Chip Select Setup

PIO #	PIO Usage	Access Mode	4 LSBits Mask	Starting Address
0	Unused	Write/Read	Mask all	0100H
1	Unused	Write/Read	Mask all	0100H

!

On Chip Serial/Parallel Ports Control

Serial Port #1	Serial Port #2	Parallel Port #1
Disabled	Disabled	Disabled

MOVE BAR →↑↓←, CHANGE ITEM- PGUP, PGDN, QUIT- <ESC>

Figure B.

C. DRAM Between 640 KB and 1 MB Shadow and Remap Setup Menu

Shadow/Remap RAM Setup

System BIOS Shadow	Video BIOS Shadow	BIOS Area Remapping
Enabled	Disabled	Enabled
Memory size > 16 MB		Disabled
Enabled		Enabled

MOVE BAR →↑↓←, CHANGE ITEM- PGUP, PGDN, QUIT- <ESC>

Figure C.

PRESS RIGHT, LEFT, UP AND DOWN KEY TO SELECT ITEM.
PRESS PGUP AND PGDN KEY TO CHANGE ITEM VALUE.
PRESS <ESC> KEY TO QUIT.

The Figure A,B and C are the proper setting values. In order to work properply, the setting of some items must be fixed.

1. SET CPU CLOCK TO CPU CLOCK.
2. SET AT CLOCK TO CPU CLK/4.
3. SET DMA CLOCK TO SCLK/2.
4. SET DRAM RAS TIME OUT TO 10us OR 100us.
5. SET DRAM REFRESH TYPE TO AT TYPE REFRESH OR NON-BURST HIDEN OR BURST OF 2 HIDDEN OR BURST OF 4 HIDDEN.
6. SET PIO USAGE TO DISABLE (BOTH PIO#0 AND PIO#1).
7. SET SERIAL PORT#1 AND SERIAL PORT#2 TO DISABLE.
8. SET PARALLEL PORT#1 TO DISABLE.

(3). Keyboard control the following function:

INS key : Press INS key when power on until RAM count beginning, this step will use default value to boot from BIOS and don't care any setup in CMOS RAM. This function act as if discharge CMOS RAM power to clear "WRONG SETUP VALUE" that will cause boot failue from BIOS.

[CNTL] + [ALT] + [+] : ENABLE CACHE FUNCTION.

[CNTL] + [ALT] + [-] : DISABLE CACHE FUNCTION.

4. DRAM CONFIGURATION

We offer you a very flexible function to choose your DRAM TYPE and DRAM SIZE on board.

(A). USE 256K MODULE RAM ONLY.

1MB : 256KB MODULE RAM ON BANK 0.
2MB : 256KB MODULE RAM ON BANK 0 & BANK 1.

(B). USE 1M MODULE RAM ONLY.

4MB : 1M MODULE RAM ON BANK 0.
8KB : 1M MODULE RAM ON BANK 0 & BANK 1.

(C). USE 4M MODULE RAM ONLY.

16MB : 4M MODULE RAM ON BANK 0.
32MB : 4M MODULE RAM ON BANK 0 & BANK 1.

(D). USE BOTH 256K AND 1M MODULE RAM.

5MB : 1M MODULE RAM ON BANK 0 AND 256K MODULE RAM ON BANK 1.

(E). USE BOTH 256K AND 4M MODULE RAM.

17MB : 4M MODULE RAM ON BANK 0 AND 256K MODULE RAM ON BANK 1.

(F). USE BOTH 1M AND 4M MODULE RAM.

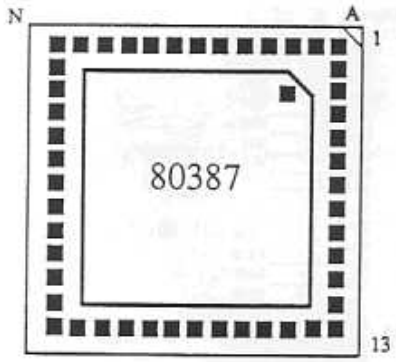
20MB : 4M MODULE RAM ON BANK 0 AND 1M MODULE RAM ON BANK 1.

(G). If the interleve mode to be use, you must have enough memory. See the following table for details.

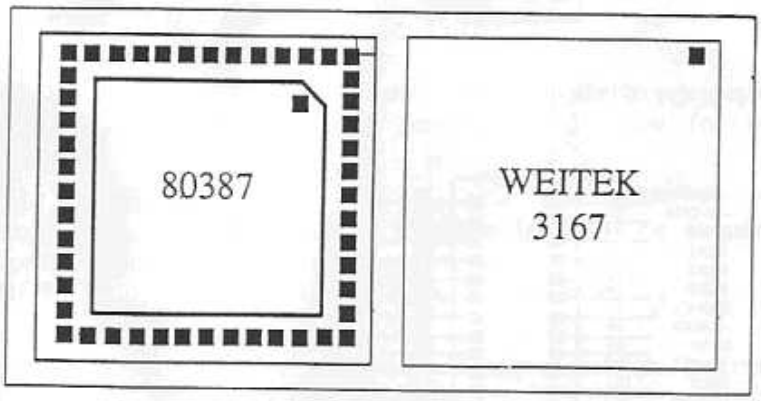
DRAM Setting		Interleaved Mode	Total Memory
Bank 0	Bank 1		
256 K	None	NO	1MB
256 K	256 K	2 - WAY	2MB
1 M	None	NO	4MB
1 M	256 K	NO	5MB
1 M	1 M	2 - WAY	8MB
4 M	None	NO	16MB
4 M	256 K	NO	17MB
4 M	1 M	NO	20MB
4 M	4 M	2 - WAY	32MB

5. COPROCESSOR CONFIGURATION

(1). 80387 : 80387-33. Please install 80387 in the central of socket.



(2). WEITEK 3167 : Use WEITEK 3167-33.



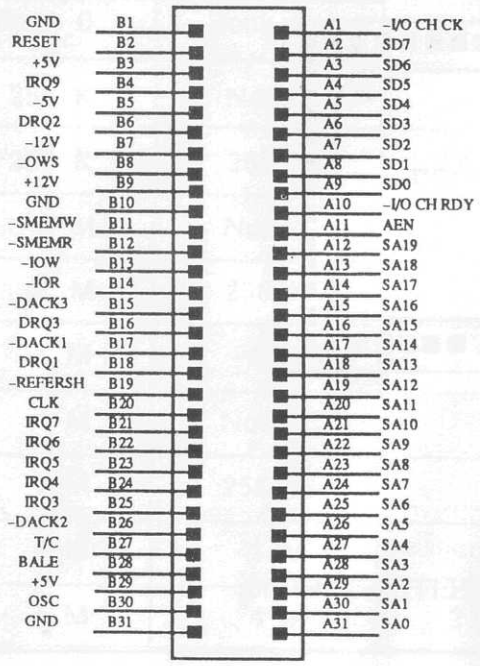
NOTE : 1. WEITEK 3167 can be used singly or with 80387.

2. If WEITEK 3167 use with 80387 simultaneously, the 80387 must install on the daughter board which WEITEK available.

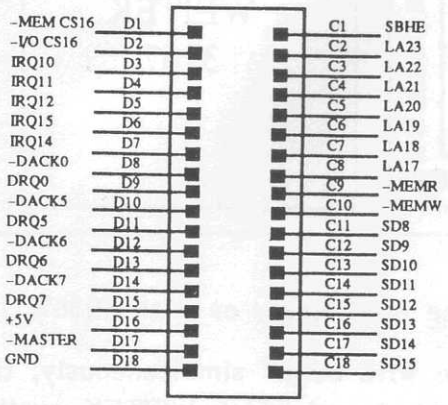
PART II:AT TECHNICAL INFORMATION

1. I/O CHANNEL MAP DESCRIPTION:

62-PIN SLOT PIN-OUT:



36-PIN SLOT PIN-OUT:



2. I/O CHANNEL SIGNAL DESCRIPTION

All signal are TTL-compatible with a maximunm loading of two low-power (LS) devices.

CLK(Output)
This is the 10MHz system clock. It is a synchronous microprocessor cycle clock with a cycle time of 100 nanoseconds. This signal should be use for synchronization.

RESET DRV(Output)
This signal goes high during power-up, low line-voltage, or hardware reset.

SA0-19(Input/Output)
The System Address Line run from bit 0 to 19. They are latched on to the falling edge of "BALE".

LA17-23(Input/Output)
The Unlatched Address Line run from bit 17 to 23.

SD0-15(Input/Output)
System data bit 0 to 15.

BALE(Output)
The Buffered-address Latch enable is used to latch SA0-19 on the falling edge. This signal is force high during DMA cycle.

I/O CH CHK(Input)
The I/O Channel Check is an active low signal which indicates that a parity error exist in I/O board.

I/O CH RDY(Input)
This signal lengths the I/O or memory read/write cycle and should be held low with valid address. It can only be held low for a maximum of 2.5 microseconds.

IRQ3-7, 9-12, 14-15(Input)
The Interrupt Request signals which indicate I/O service request attention. They are prioritized in the following sequences:
Highest IRQ9, 10, 11, 12, 14, 15, 3, 4, 5, 6, 7, Lowest.

-IOR(Input/ Output)
The I/O Read Singnal is an actuve low signal which instructs the I/O device to drive its data onto the data bus.

-IOW(Input/Output)
The I/O write is an active low signal which instructs the I/O device to read data from the data bus.

-SMEMR(Output)
The System Memory Read is low while the 1 mega byte of memory is being used.

-MEMR(Input/Output)
The Memory Read Signal is low while any memory location is being read.

-SMEMW(Output)
The System Memory Write is low while the low 1mega byte of memory is been written.

-MEMW(Input/Output)
Memory Write is low while any memory location is been written.

DRQ 0-3, 5-7(Input)
DMA Request channel 0 to 3 are for 8-bit data transfer.
DMA Request channel 4 is used internaly on the system board.
DMA Request should be held high until the corresponding DMA inactive.
Their priority is in the following sequence:
Highest DRQ 0, 1, 2, 3, 5, 6, 7, Lowest.

DACK 0-3, 5-7(Output)
The DMA Acknowledge 0 to 3, 5 to 7 are the corresponding acknowledge signals for DRQ 0 to 3, 5-7.

AEN(Output)
The DMA Address Enable is high when the DMA controller is driving the address bus. It is low when the 80386 CPU is driving the address bus.

-REFRESH(Input/Output)
This signal is to indicate the memory refresh cycle is in progress.

T/C(Output)
Terminal Count provides a puls when the terminal count for any DMA channel is reached.

SBHE(Input/Output)
The System Bus High Enable indicates high byte SD8-15 is on the data bus.

-MASTER(Input)
The Master is the signal from the I/O processor which gains control as the master and should be held low for a maximum of 15 microsecond or system memory may be lost due to the lack of refresh.

-MEM CS16(Input, Open collector)
The Memory Chip Select 16 indicates that the present data is a 1 Wait State 16-bit data memory operation.

-I/O CS16(Input, Open collector)
The I/O Chip Select indicates the present data transfer is a 1 Wait State 16-bit data I/O operation.

OSC(Output)
The Oscillator is a 14.31818 MHz signal used for the color graphic board.

OWS(Input, Open collector)
The 0 Wait State indicates to the microprocessor that the present bus cycle can be completed without inserting any additional wait cycles.

3. TIMERS

The system board has 3 programmable counter/timers in 82C206 chip.

Timer Channel 0:System timer to interrupt controller.
Timer Channel 1:Dynamic Ram refresh request.
Timer Channel 2:Speaker tone generator.

4. DMA CONTROLLERS

The system board has 2 programmable DMA controllers in 82C206 chip.

DMA Channel 0:spare
DMA Channel 1:IBM SDLC.
DMA Channel 2:Diskette adapter.
DMA Channel 3:spare
DMA Channel 4:Cascade for DMA controller 1
DMA Channel 5:spare
DMA Channel 6:spare
DMA Channel 7:spare

5. INTERRUPT CONTROLLERS

82C206 Integrated perihperal controller provide 16 levels of system interrupts. They are listed in priority as follows:

Interrupt Level	Description
NMI	Parity check error
IRQ0	System timer interrupt from timer 82C206
IRQ1	Keyboard output buffer full
IRQ2	Interrupt rerouting from IRQ8 through IRQ15
IRQ3	Serial port 2
IRQ4	Serial port 1
IRQ5	Parallel printer port 2
IRQ6	Floppy disk adapter
IRQ7	Parallel printer port 1
IRQ8	Realtime clock
IRQ9	Recounting to INT 10 from hardware IRQ2
IRQ10	Spare
IRQ11	Spare
IRQ12	Spare
IRQ13	Math Coprocessor 80287 (80387/WEITEK option)
IRQ14	Hard disk adapter
IRQ15	Spare

6. REAL TIME CLOCK AND NONVOLATILE RAM

The real time clock is included in 82C206, and its 114 bytes of RAM information are backed up by a 6V DC battery. The internal clock circuit uses 14 bytes while the rest is allocated to system configuration.

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minutes alarm
04	Hours
05	Hours alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status Register A
0B	Status Register B
0C	Status Register C
0D	Status Register D
0E	Diagnostic status byte
0F	Shutdown
10	Diskette drive type byte-drive A and B
11	Reserve
12	Fix disk type byte-drive C and D
13	Reserve
14	Equipment byte
15	Low-base memory
16	High-base memory
17	Low-extension memory
18	High-extension memory
19-2D	Reserve
2E-2F	2-byte CMOS checksum
30	Low-extension memory byte
31	High-extension memory byte
32	Date century byte
33	Information flag(set during power on)
34-3F	Reserve

7. I/O & MEMORY MAP

The I/O MAP is shown below:

I/O address	Description
000-01F	DMA controller (master)

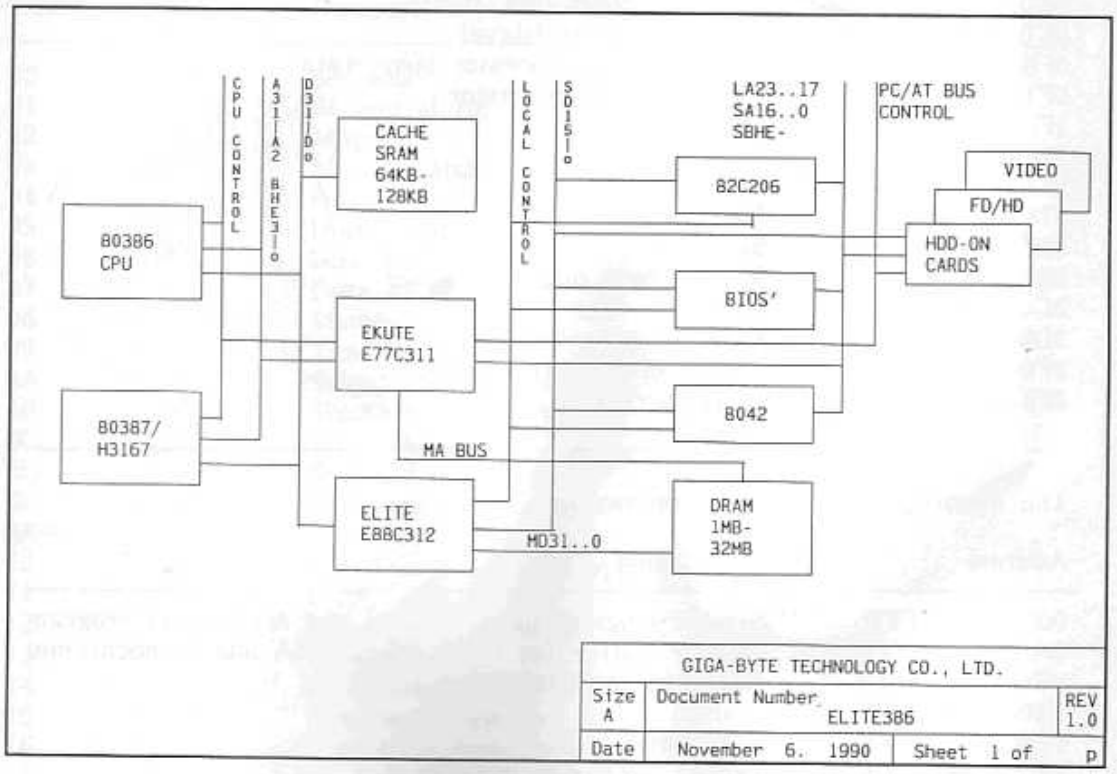
020-021	Interrupt controller (master)
022-023	Chips control registers
040-05F	Timer
060-06F	8042 (Key board controller)
070-07F	CMOS RAM & Real time clock
080-08F	DMA page registers
0A0-0A1	Interrupt controller (slave)
0C0-0DF	DMA controller (slave)
0F0	Clear Math-coprocessor busy state
0F1	Reset Math-coprocessor
1F0-1F8	Fix Disk
278-27F	Parallel port 2
2F8-2FF	Serial port 2
378-37F	Parallel port 1
380-38f	SDLC
3B0-3BF	Monochrome display adapter
3C0-3CF	EGA
3D0-3DF	CGA
3F0-3F7	Floppy disk controller
3F8-3FF	Serial port 1

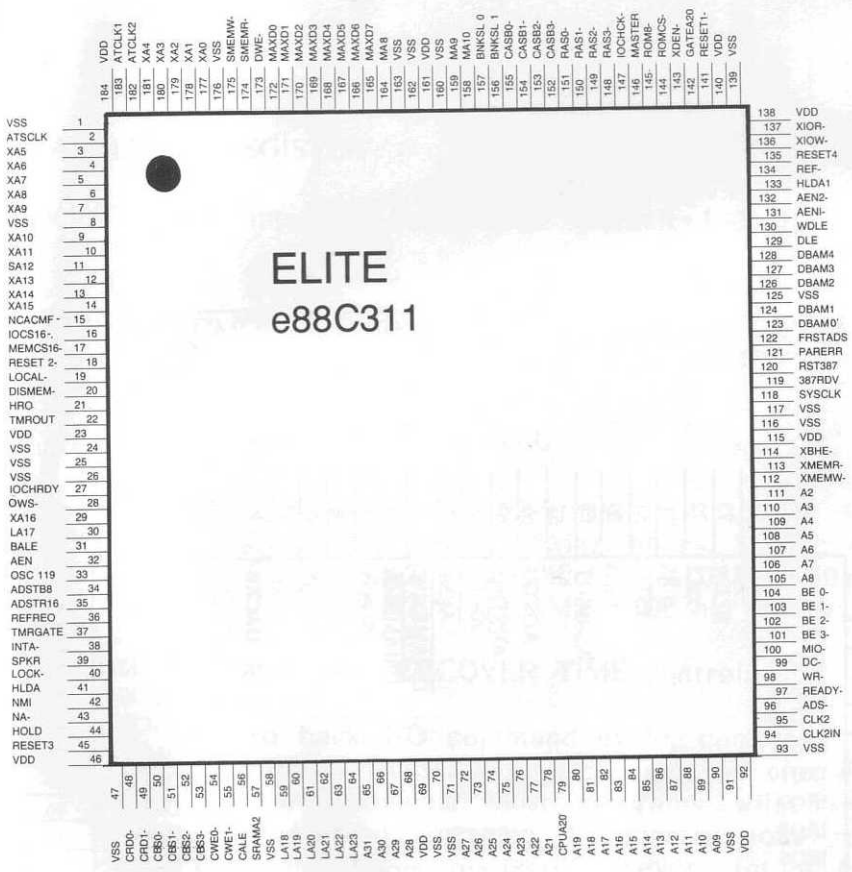
The memory MAP is shown below:

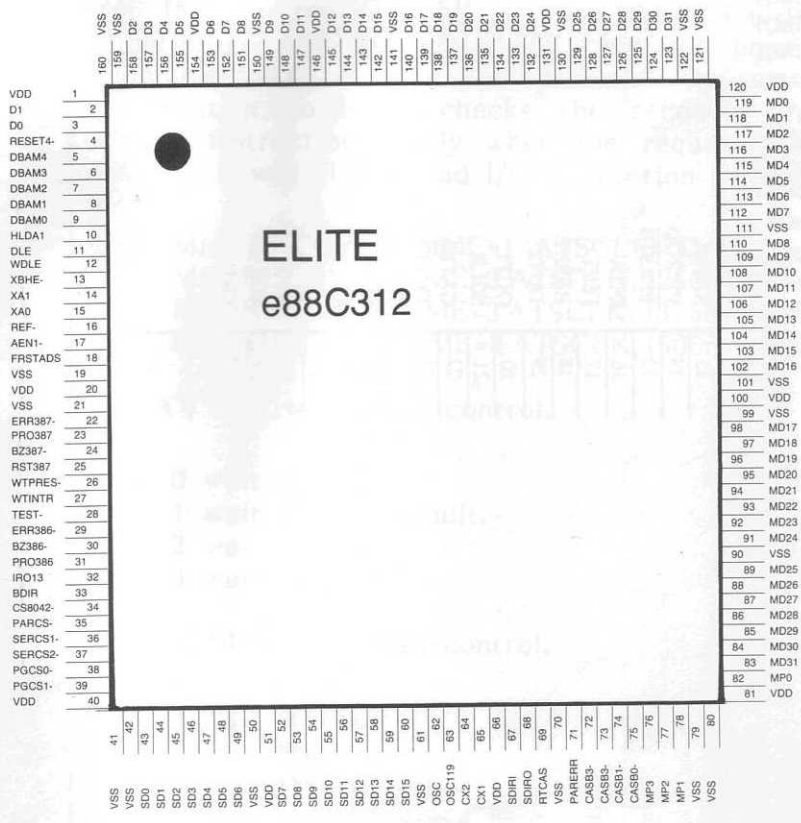
Address	Description
000000-09FFFF	System memory used by DOS and application program
0A0000-0BFFFF	Display buffer for EGA, VGA, CGA and monochrome.
0C0000-0DFFFF	Reserved for extendable I/O ROM
0E0000-0EFFFF	Unused
0F0000-0FFFFF	ROM BIOS
100000-FFFFFF	System extension memory

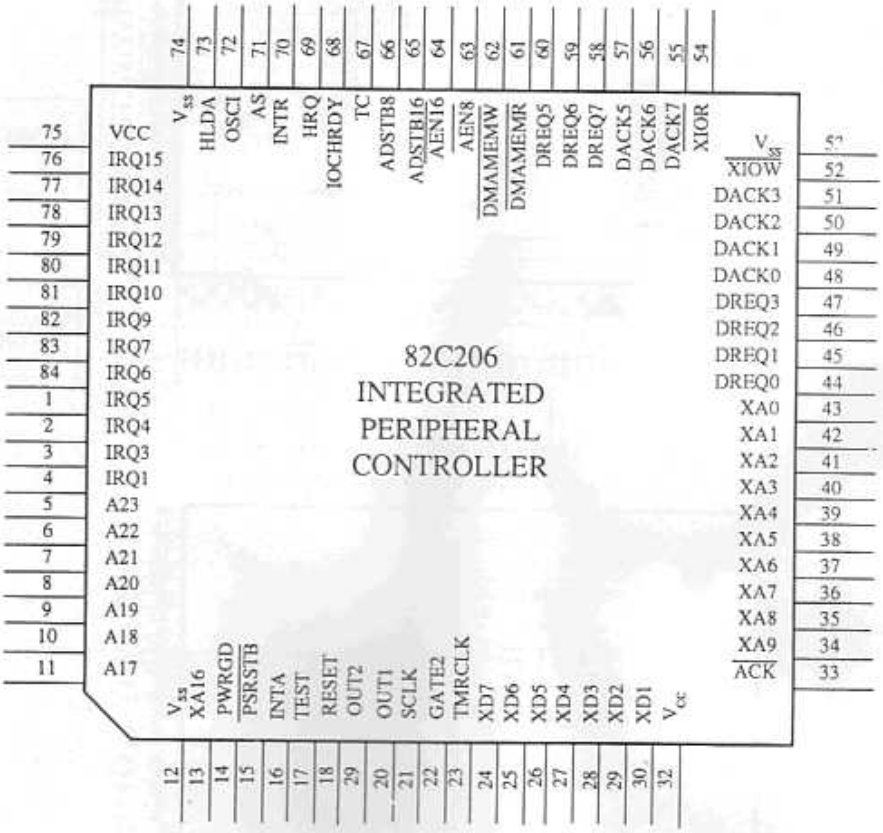
PART III:CHIPS TECHNICAL INFORMATION

1. BLOCK DIAGRAM




ELITE
e88C311


ELITE
e88C312


82C206
INTEGRATED
PERIPHERAL
CONTROLLER
75 VCC
76 IRQ15
77 IRQ14
78 IRQ13
79 IRQ12
80 IRQ11
81 IRQ10
82 IRQ9
83 IRQ7
84 IRQ6
1 IRQ5
2 IRQ4
3 IRQ3
4 IRQ1
5 A23
6 A22
7 A21
8 A20
9 A19
10 A18
11 A17
12 VSS
13 XA16
14 PWRGD
15 PSRSTB
16 INTA
17 TEST
18 RESET
29 OUT2
20 OUT1
21 SCLK
22 GATE2
23 TMRCLK
24 XD7
25 XD6
26 XD5
27 XD4
28 XD3
29 XD2
30 XD1
32 VCC
74 VSS
73 HLDA
72 OSCI
71 AS
70 INTR
69 HRQ
68 IOCHRDY
67 TC
66 ADSTB8
65 ADSTB16
64 AEN16
63 AEN8
62 DMAMEMW
61 DMAMEMR
60 DREQ5
59 DREQ6
58 DREQ7
57 DACK5
56 DACK6
55 DACK7
54 XIOR
53 VSS
52 XIOW
51 DACK3
50 DACK2
49 DACK1
48 DACK0
47 DREQ3
46 DREQ2
45 DREQ1
44 DREQ0
43 XA0
42 XA1
41 XA2
40 XA3
39 XA4
38 XA5
37 XA6
36 XA7
35 XA8
34 XA9
33 ACK

3. PROGRAMMABLE REGISTER

AT Bus Clock/Recover Time/Wait State Reg. Default=1000,0110 Index:11H

Bit 7	6	5	4	3	2	1	0
ATCKM1	ATCKM0	CMDRC1	CMDRC0	WT16B1	WT16B0	WT8B1	WT8B0

Bit(s)

7:6 AT state machine clock select.

Value
- 00: ATCLK2=ATCLK1, (62.5 ns)
- 01: ATCLK2=CLK2IN/3, (25Mhz: 60 ns, 33Mhz: 45 ns).
- 10: ATCLK2=CLK2IN/4, (25Mhz: 80 ns, 33Mhz: 60 ns), Default.
- 11: ATCLK2=CLK2IN/5, (25Mhz: 100 ns, 33Mhz: 75 ns).

5:4 I/O command cycle RECOVER TIME control.

For back to back I/O command cycle, command RECOVER TIME will be 1 ATSCLK, which may not be enough for some slow I/O devices. Most programs will have a JMP instruction inserted between I/O instructions to provide extra command recover time. However, for a high speed 386 cache machine, the extra command recover time derived from JMP instruction may be very short, causing software compatibility problem. Elite 386 chip set provides 2 programmable bits to solve this problem. By setting these 2 bits, built-in hardware checks the recover time between two I/O instructions. Only when the required recover time is satisfied, will the second I/O instruction be executed.

Value
- 00: Min. RECOVER TIME=1 ATSCLK, Default.
- 01: Min. RECOVER TIME=2 ATSCLK, (250ns when ATCLK2=62.5ns).
- 10: Min. RECOVER TIME=3 ATSCLK, (375ns when ATCLK2=62.5ns).
- 11: Min. RECOVER TIME=4 ATSCLK, (500ns when ATCLK2=62.5ns).

3:2 16-Bit AT BUS wait state control.

Value
- 00: 0 wait state.
- 01: 1 wait state, Default.
- 10: 2 wait states.
- 11: 3 wait states.

1:0 8-Bit AT BUS wait state control.

Value
- 00: 2 wait states.
- 01: 3 wait states.
- 10: 4 wait states, Default.
- 11: 5 wait states.

System Control Register Default=0110,XX01 Index:12H

Bit 7	6	5	4	3	2	1	0
SLOWCLK	FGATEA20	FRST3	SNOOP	CO387	COWTK	FLUSH	NAX

Bit(s)

7 Select CLK2 source between CLK2IN and ATCLK1.

Value
0: CLK2=CLK2IN, Default.
1: CLK2=ATCLK1.

6 FAST GATE A20. Always read/writable, even when register has been locked. When either this bit is 0 or GATEA20 (from 8042) is 0, A20 is forced to 0, when both this bit and GATEA20 are 1, A20 equals CPUA20.
Note: Bit is always read/writable, even when register has been locked.

Value
0: A20=0
1: A20=CPUA20 if GATEA20=1,Default.

5 FAST RESET 3.
A 0 to 1 transition of this bit activates RESET3 to reset CPU.

* Note - Bits 6 & 5 are writable even this register been locked.

4 Enable/Disable SNOOPING.

Value
0: Snooping is disabled, CPU will be put on hold when DMA or MASTER is using the bus (Default).
1: Snooping is enabled, CPU can keep running out of CACHE when DMA or MASTER is using the bus.

3 Intel 387 coprocessor is present. Read Only after first write.

Value
0: 387 does not exist.
1: 387 exist.

2 Weitek 3167 coprocessor is present. Read Only after first write.

Value
0: 3167 does not exist.
1: 3167 exist.
*Note-Bits 3 & 2 will be written once and become read only afterwards. These two bits should be obtained from register 4DH bits 3 & 2 before any memory access during system power up.

1 CACHE FLUSH. Write 1 to this bit clears the whole internal TAG RAM within 1024 clock cycles.

0 Next Address Request.

Value
0: Request 386 to run pipelined cycle.
1: 386 running in non-pipelined cycle (Default).

DRAM Bank 0 Configuration Register Default=0110,01XX Index:30H

Bit 7	6	5	4	3	2	1	0
B0DTY1	B0DTY0	B0DWT1	BoDWT0	B0DWT0	B0DRT0	--	--

Bit(s)

7:6 DRAM type.

Value
- 00: DRAM is not present.
- 01: 256Kx1, 256Kx4 DRAM, Default.
- 10: 1Mx1, 1Mx4 DRAM.
- 11: 4Mx1, 4Mx4 DRAM.

5:4 DRAM wait state.

Value
- 00: 0 wait state in pipelined mode when DRAM PAGE HIT.
- 01: 1 wait state in pipelined mode when DRAM PAGE HIT.
- 10: 2 wait state in pipelined mode when DRAM PAGE HIT, Default.
- 11: Reserved.

3:2 DRAM RAS TIME OUT check control.

Value
- 00: RAS TIME OUT check disabled.
- 01: RAS TIME OUT limit=10 us, Default.
- 10: RAS TIME OUT limit=100 us.
- 11: Reserved.

1:0 Reserved.

DRAM Bank 0 Start Address Register Default=XX00,0000 Index:31H

Bit 7	6	5	4	3	2	1	0
--	--	B0DA25	B0DA24	B0DA23	B0DA22	B0DA21	B0DA20

Bit(s)

7:6 Reserved.

5:0 Bank 0 DRAM start address A25 - A20

DRAM Bank 1 Configuration Register Default=00XX,XXXX Index:32H

Bit 7	6	5	4	3	2	1	0
B1DTY1	B1DTY0	B1DWT1	B1DWT0	B1DRT1	B1DRT0	--	--

Bit(s)

7:6 DRAM type.

Value
- 00: DRAM is not present (Default).
- 01: 256Kx1, 256Kx4 DRAM.
- 10: 1Mx1, 1Mx4 DRAM.
- 11: 4Mx1, 4Mx4 DRAM.

5:4 DRAM wait state.

Value
- 00: 0 wait state in pipelined mode when DRAM PAGE HIT.
- 01: 1 wait state in pipelined mode when DRAM PAGE HIT.
- 10: 2 wait state in pipelined mode when DRAM PAGE HIT.
- 11: Reserved.

3:2 DRAM RAS TIME OUT check control.

Value
- 00: RAS TIME OUT check disabled.
- 01: RAS TIME OUT limit=10 us.
- 10: RAS TIME OUT limit=100 us.
- 11: Reserved.

1:0 Reserved.

DRAM Bank 1 Start Address Register Default=XXXX,XXXX Index:33H

Bit 7	6	5	4	3	2	1	0
--	--	B1DA25	B1DA24	B1DA23	B1DA22	B1DA21	B1DA20

Bit(s)

7:6 Reserved.

5:0 Bank 1 DRAM start address A25 - A20.

DRAM Bank 2 Configuration Register Default=00XX,XXXX Index:34H

Bit 7	6	5	4	3	2	1	0
B2DTY1	B2DTY0	B2DWT1	B2DWT0	B2DRT1	B2DRT1	--	--

Bit(s)

7:6 DRAM type.

Value
- 00: DRAM is not present (Default).
- 01: 256Kx1, 256Kx4 DRAM.
- 10: 1Mx1, 1Mx4 DRAM.
- 11: 4Mx1, 4Mx4 DRAM.

5:4 DRAM wait state.

Value
- 00: 0 wait state in pipelined mode when DRAM PAGE HIT.
- 01: 1 wait state in pipelined mode when DRAM PAGE HIT.
- 10: 2 wait state in pipelined mode when DRAM PAGE HIT.
- 11: Reserved.

3:2 DRAM RAS TIME OUT check control.

Value
- 00: RAS TIME OUT check disabled.
- 01: RAS TIME OUT limit=10 us.
- 10: RAS TIME OUT limit=100 us.
- 11: Reserved.

1:0 Reserved

DRAM Bank 2 Start Address Register Default=XXXX,XXXX Index:35H

Bit 7	6	5	4	3	2	1	0
--	--	B2DA25	B2DA24	B2DA23	B2DA22	B2DA21	B2DA20

Bit(s)

7:6 Reserved.

5:0 Bank 2 DRAM start address A25 - A20.

DRAM Bank 3 Configuration Register Default=00XX,XXXX Index:36H

Bit 7	6	5	4	3	2	1	0
B3DTY1	B3DTY0	B3DWT1	B3DWT0	B3DRT1	B3DRT0	--	--

Bit(s)

7:6 DRAM type.

Value
- 00: DRAM is not present, (Default).
- 01: 256Kx1, 256x4 DRAM.
- 10: 1Mx1, 1Mx4 DRAM.
- 11: 4Mx1, 4Mx4 DRAM.

5:4 DRAM wait state.

Value
- 00: 0 wait state in pipelined mode when DRAM PAGE HIT.
- 01: 1 wait state in pipelined mode when DRAM PAGE HIT.
- 10: 2 wait state in pipelined mode when DRAM PAGE HIT.
- 11: Reserved.

3:2 DRAM RAS TIME OUT check control.

Value
- 00: RAS TIME OUT check disabled.
- 01: RAS TIME OUT limit=10 us.
- 10: RAS TIME OUT limit=100 us.
- 11: Reserved.

1:0 Reserved.

DRAM Bank 3 Start Address Register Default=XXXX,XXXX Index:37H

Bit 7	6	5	4	3	2	1	0
--	--	B3DA25	B3DA24	B3DA23	B3DA22	B3DA21	B3DA20

Bit(s)

7:6 Reserved.

5:0 Bank 3 DRAM start address A25 - A20.

Memory Control Register Default=1100,000X Index:40H

Bit 7	6	5	4	3	2	1	0
SHADMR	ENMROM	DSLOCM	DSBUSM	ITLV	ROM8	--	--

Bit(s)

7 Shadow RAM of ROM enabled at (0FE0000-0FFFFFFH).

6 ROM at (0FE0000-0FFFFFFH) is on local system.

Value
- 00: Read AT BUS (ROM), Write RAM (Local or AT BUS).
- 01: Read Local ROM, Write RAM (Local or AT BUS).
- 10: Read RAM (Local or AT BUS), write protect.
- 11: Read RAM, Write RAM (Local or AT BUS), Default.

5 Local memory access disabled.

Once set, all memory accesses, except those accessed to the LOCAL ROM (ROMCS- are generated), are directed to the AT BUS. This is used to check the presence of AT BUS memory.

Value
- 0: Local memory access enabled (Default).
- 1: Local memory access disabled.

4 All AT BUS memory accesses disabled.

Once set, all memory accesses are treated as local memory accesses, for those existing DRAM locations, RAS-, CAS-, READY- are generated. For those non-existing DRAM locations, only READY- are generated. This is used to check the presence and type of local DRAM.

Value
- 0: AT BUS Memory access enabled (Default)
- 1: AT BUS memory access disabled.

3 DRAM page interleave enabled.

Value
- 0: DRAM operating in page mode only (Default).
- 1: DRAM operating in page interleave mode, if DRAM type matches.

2 Local ROM size. read only

Value
- 0: Local ROM is 16 bit.
- 1: Local ROM is 8 bit.

1:0 Reserved.

MASTER High Page Register Default=0XXX,X000 Index:41H

Bit 7	6	5	4	3	2	1	0
MSTR32	--	--	--	--	M32A26	M32A25	M32A24

Bit(s)

7 Enable MASTER's access to local memory up to 64 MB.

Value

0: MASTER can only access 16M local memory, Default.

1: Enable MASTER to access local memory up to 64 MB.

6:3 Reserved.

2:0 MASTER access address extension A26 - A24.

When register 41 bit 7 is set to 1, during MASTER access, these 3 bits will be used as address bit 26 - 24, combined with LA(23:17), XA(16:1) and XBHE-, to enable MASTER to access local memory above 16M.

System ROM/Shadow RAM Control Register C. Default=0000,0000 Index:42H

Bit 7	6	5	4	3	2	1	0
SHADC3	ENROMC3	SHADC2	ENROMC2	SHADC1	ENROMC1	SHADC0	ENROMC0

Bit(s)

7 Enable shadow RAM of ROM AT (0CC000-0CFFFFH).

6 ROM at (0CC000-0CFFFFH) is on local system.

5 Enable shadow RAM of ROM at (0C8000-0CBFFFH).

4 ROM at (0C8000-0CBFFFH) is on local system.

3 Enable shadow RAM of ROM at (0C4000-0C7FFFH).

2 ROM at (0C4000-0C7FFFH) is on local system.

1 Enable shadow RAM of ROM at (0C0000-0C3FFFH).

0 ROM at (0C0000-0C3FFFH) is on local system.

System ROM/Shadow RAM Control Register D. Default=0000,0000 Index:43H

Bit 7	6	5	4	3	2	1	0
SHADD3	ENROMD3	SHADD2	ENROMD2	SHADD1	ENROMD1	SHADD0	ENROMD0

Bit(s)

7 Enable shadow RAM of ROM at (0DC000-0DFFFFH).
6 ROM at (0DC000-0DFFFFH) is on local system.

5 Enable shadow RAM of ROM at (0D8000-0DBFFFH).
4 ROM at (0D8000-0DBFFFH) is on local system.

3 Enable shadow RAM of ROM at (0D4000-0D7FFFH).
2 ROM at (0D4000-0DFFFH) is on local system.

1 Enable shadow RAM of ROM at (0D0000-0D3FFFH).
0 ROM at (0D0000-0D3FFFH) is on local system.

SHAD ENROM

Value

00: Read AT BUS (ROM), Write RAM (Local or AT BUS).
01: Read Local ROM, Write RAM (Local or AT BUS).
10: Read RAM (Local or AT BUS), write protect.
11: Read RAM, Write RAM (Local or AT BUS).

*Procedure to turn on SHADOW RAM:

1. Set corresponding SHAD=0,ENROM=1 for LOCAL ROM, SHAD=0, ENROM=0 for AT BUS ROM.
2. Repeat "Read then write to the same address" for the entire ROM block.
3. After finishing ROM copy, Set corresponding SHAD=1, ENROM=0.

System ROM/Shadow RAM control Register E. Default=0000,0000 Index:44H

Bit 7	6	5	4	3	2	1	0
SHADE3	ENROME3	SHADE2	ENROME2	SHADE1	ENROME1	SHADE0	ENROME0

Bit(s)

7 Shadow RAM of ROM enabled at (0EC000-0EFFFFH).
6 ROM at (0EC000-0EFFFFH) is on local system.

5 Shadow RAM of ROM enabled at (0E8000-0EBFFFH).
4 ROM at (0E8000-0EBFFFH) is on local system.

3 Shadow RAM of ROM enabled at (0E4000-0E7FFFH).
2 ROM at (0E4000-0E7FFFH) is on local system.

1 Shadow RAM of ROM enabled at (0E0000-0E3FFFH).
0 ROM at (0E0000-0E3FFFH) is on local system.

System ROM/Shadow RAM Control Register F. Default=0101,0101 Index:45H

Bit 7	6	5	4	3	2	1	0
SHADF3	ENROMF3	SHADF2	ENROMF2	SHADF1	ENROMF1	SHADF0	ENROMF0

Bit(s)

7 Shadow RAM of ROM enabled at (0FC000-0FFFFFH).
6 ROM at (0FC000-0FFFFFH) is on local system.

5 Shadow RAM of ROM enabled at (0F8000-0FBFFFH).
4 ROM at (0F8000-0FBFFFH) is on local system.

3 Shadow RAM of ROM enabled at (0F4000-0F7FFFH).
2 ROM at (0F4000-0F7FFFH) is on local system.

1 Shadow RAM of ROM enabled at (0F0000-0F3FFFH).
0 ROM at (0F0000-0F3FFFH) is on local system.

SHAD ENROM
Value

00: Read AT BUS (ROM), Write RAM (Local or AT BUS).
01: Read Local ROM, Write RAM (Local or AT BUS).
10: Read RAM (LOCAL or AT BUS), write protect.
11: Read RAM, Write RAM (Local or AT BUS).

*Procedure to turn on SHADOW RAM:

1. Set corresponding SHAD=0, ENROM=1 for LOCAL ROM, SHAD=0, ENROM=0 for AT BUS ROM.
2. Repeat "Read then write to the same address" for the entire ROM block.
3. After finishing ROM copy, set corresponding SHAD=1, ENROM=0.

Remapping Control Register Default=XXXX,0000 Index:46H

Bit 7	6	5	4	3	2	1	0
--	--	--	--	REMAPC	REMAPD	REMAPE	REMAPF

Bit(s)

7:4 Reserved.
Value

3:0 0000: Remap memory at 0A0000-0BFFFFH to above the Remap Base Address specified by register 47H.
0100: Remap memory at 0A0000-0BFFFFH and 0D0000-0DFFFFh to above the Remap Base address specified by register 47H
0110: Remap memory at 0A0000-0BFFFFH and 0D0000-0EFFFFh to above the Remap Base Address specified by register 47H.
1110: Remap memory at 0A0000-0EFFFFH to above the Remap Base Address specified by register 47H.
1111: Remap memory at 0A0000-0FFFFFH to above the Remap Base Address specified by register 47H.
else: Reserved.

Remap Base Address Register Default=X000,0001 Index:47H

Bit 7	6	5	4	3	2	1	0
--	RMPA26	RMPA25	RMPA24	RMPA23	RMPA22	RMPA21	RMPA20

Bit(s)

7 Reserved.

6:0 Remapping Base Address A26 - A20.

Refresh Control Register Default=0X11,0000 Index:48H

Bit 7	6	5	4	3	2	1	0
HIDREF	--	REFPU1	REFPU0	BURST1	BURST0	SLWREF1	SLWREF0

Bit(s)

7 Enable Hidden Refresh.

Value

0: Hidden Refresh disabled. AT type refresh will be generated, Default.

1: Hidden Refresh enabled. CPU will not be put on hold when REFRESH is running.

6 Reserved.

5:4 RAS pulse width during refresh.

Value

00: 5 CLK2.
01: 6 CLK2.
10: 7 CLK2.
11: 8 CLK2, Default.

3:2 BURST refresh control.

Should be used only when HIDDEN REFRESH is enabled, and only LOCAL DRAM will run BURST refresh once enabled, AT BUS refresh is always in single refresh mode.

Value

00: disable burst refresh, Default.
01: burst of 2.
10: burst of 4.
11: burst of 8.

1:0 Slow Rate Refresh control.

Normally refresh is running at a rate of 256/4ms, but some low power DRAMs can run refresh at a slower rate. These 2 bits are used to control refresh rate of the LOCAL DRAM, if a low power DRAM is used. However AT BUS refresh is always running at a rate of 256/4ms.

Value

00: normal refresh rate, 256/4ms, Default.
01: 128/4ms.
10: 64/4ms.
11: 32/4ms.

Parity Error Diagnostic Register 1 Default=00XX,XXXX Index:49H

Bit 7	6	5	4	3	2	1	0
ENPCHK	PARERR	--	--	--	PERRA26	PERRA25	PERRA24

Bit(s)

7 Enable Parity Check.
Note: Bit is always read/writable, even when register has been locked.

value
0: Parity check disable (Default).
1: Parity check enabled

6 Parity Error.

This bit is set to 1 when a parity error occurs. The address bit 26 - 2 is latched and can be read from CREG_4A-CREG_4D for debugging. After reading the error address, this bit should be written as 0 to reopen the latches.
Note: Bit is always read/writable, even when register has been locked.

Value
0: Open Parity Error Address Latches, Default.
1: Parity Error has occurred.

Note - Bit 6 is writable even this register been locked.

5:3 Reserved.

2:0 Parity Error Address bit 26 - 24.

Parity Error Diagnostic Register 2 Default=XXXX,XXXX Index:4AH

Bit 7	6	5	4	3	2	1	0
PERRA23	PERRA22	PERRA21	PERRA20	PERRA19	PERRA18	PERA17	PERRA16

Bit(s)

7:0 Parity Error Address bit 23 - 16.

Parity Error Diagnostic Register 3 Default=XXXX,XXXX Index:4BH

Bit 7	6	5	4	3	2	1	0
PERRA15	PERRA14	PERRA13	PERRA12	PERRA11	PERRA10	PERA9	PERRA8

Bit(s)

7:0 Parity Error Address bit 15 - 8.

Parity Error Diagnostic Register 4 Default=XXXX,XXXX Index:4CH

Bit 7	6	5	4	3	2	1	0
PERRA7	PERRA6	PERRA5	PERRA4	PERRA3	PERRA2	--	--

Bit(s)

7:2 Parity Error Address bit 7 -2

1:0 Reserved.

Parity Error Diagnostic Register 5 Default=XXXX,XXXX Index:4DH

Bit 7	6	5	4	3	2	1	0
--	--	--	--	PERRB3	PERRB2	PERRB1	PERRB8

Bit(s)

7:4 Reserved

3 Parity Error is caused by BYTE 3.
Value
0: No Parity Error.
1: BYTE 3 has Parity Error.

2 Parity Error is caused by BYTE 2.
Value
0: No Parity Error.
1: BYTE 2 has Parity Error.

1 Parity Error is caused by BYTE 1.
value
0: No Parity Error.
1: BYTE 1 has Parity Error.

0 Parity Error is caused by BYTE 0.
Value
0: No Parity Error.
1: BYTE 0 has Parity Error.

*Note - Bits 3 & 2 also indicate the presence of the INTEL 80387 and Weitek 3167 coprocessor installation status respectively but only before CPU accesses any memory during power up. These 2 bits correspond to bits 3 & 2 of register 12H.
Value
0: coprocessor not installed.
1: coprocessor installed.

**Configuration register 4D is the only register that resides in the e88C312.

Non-Cache/Disable DRAM Block 0 Register 1 Default=00XX,XXXX Index:50H

Bit 7	6	5	4	3	2	1	0
DSDRAM0	NCDRAM0	--	--	NC0SZ3	NC0SZ2	NC0SZ1	NC0SZ0

Bit(s)

7:6 Non-Cache/Disable DRAM Block 0 control.

Value

00: Function disabled, Default.

01: Non-Cache the DRAM block specified by 50 - 52H.

10: The DRAM block specified by 50 - 52H is disabled. All memory access is directed to AT BUS, and will not be cached.

11: Reserved.

5:4 Reserved.

3:0 Non-Cache/Disable DRAM Block 0 Size.

Value

0000: 4KB
0001: 8KB.
0010: 16KB.
0011: 32KB.
0100: 64KB.
0101: 128KB.
0110: 256KB.
0111: 512KB.
1000: 1MB.
1001: 2MB.
1010: 4MB.

Non-Cache/Disable DRAM Block 0 Register 2 Default=XXXX,XXXX Index:51H

Bit 7	6	5	4	3	2	1	0
--	NC0A26	NC025	NC0A24	NC0A23	NC0A22	NC0A21	NC0A20

Bit(s)

7 Reserved.

6:0 Non-Cache/Disable DRAM Block 0 base address bit 26 - 20.

Non-Cache/Disable

Non-Cache/Disable DRAM Block 0 Register 3 Default=XXXX,XXXX Index:52H

Bit 7	6	5	4	3	2	1	0
NC0A19	NC0A18	NC0A17	NC0A16	NC0A15	NC0A14	NC0A13	NC0A12

Bit(s)

7:0 Non-Cache/Disable DRAM Block 0 base address bit 19 - 12.

Non-Cache/Disable DRAM Block 1 Register 1 Default=00XX,XXXX Index:53H

Bit 7	6	5	4	3	2	1	0
DSDRAM1	NCDRAM1	--	--	NC1SZ3	NC1SZ2	NC1SZ1	NC1SZ0

Bit(s)

7:6 Non-Cache/Disable FRAM Block 1 control.

Value

00: Function disabled.

01: Non-Cache the DRAM block specified by 53 - 55H.

10: The DRAM block specified by 53 - 55H is disabled. All memory access is directed to the AT BUS, and will not be cached.

11: Reserved.

5:4 Reserved.

3:0 Non-Cache/Disable DRAM Block 1 Size.

Value

0000: 4KB.
0010: 16KB.
0011: 32KB.
0100: 64KB.
0101: 128KB.
0110: 256KB.
0111: 512KB.
1000: 1KB.
1001: 2MB.
1010: 4MB.

Non-Cache/Disable DRAM Block 1 Register 2 Default=XXXX,XXXX Index:54H

Bit 7	6	5	4	3	2	1	0
--	NC1A26	NC1A25	NC1A24	NC1A23	NC1A22	NC1A21	NC1A20

Bit(s)

7 Reserved.

6:0 Non-Cache/Disable DRAM Block 1 base address bit 26 - 20.

Non-Cache/Disable DRAM Block 1 Register 3 Default=XXXX,XXXX Index:55H

Bit 7	6	5	4	3	2	1	0
NC1A19	NC1A18	NC1A17	NC1A16	NC1A15	NC1A14	NC1A13	NC1A12

Bit(s)

7:0 Non-Cache/Disable DRAM Block 1 base address bit 19 - 12.

Non-Cache/Disable DRAM Block 2 Register 1 Default=00XX,XXXX Index:56H

Bit 7	6	5	4	3	2	1	0
DSDRAM2	NCDRAM2	--	--	NC2SZ2	NC2SZ1	NC2SZ1	NC2SZ0

Bit(s)

7:6 Non-Cache/Disable DRAM Block 2 control.

Value

00: Function disabled.

01: Non-Cache the DRAM block specified by 56 - 58H.

10: The DRAM block specified by 56 - 58H is disabled. All memory access is directed to the AT BUS, and will not be cached.

11: Reserved.

5:4 Reserved.

3:0 Non-Cache/Disable DRAM Block 2 Size.

Value

0000: 4KB.
0010: 16KB.
0011: 32KB.
0100: 64KB.
0101: 128KB.
0110: 256KB.
0111: 512KB.
1000: 1MB.
1001: 2MB.
1010: 4MB.

Non-Cache/Disable DRAM Block 2 Register 2 Default=XXXX,XXXX Index:57H

Bit 7	6	5	4	3	2	1	0
--	NCDRA26	NC2A25	NC2A24	NC2A23	NC2A22	NC2A21	NC2A20

Bit(s)

7 Reserved.

6:0 Non-Cache/Disable DRAM Block 2 base address bit 26 - 20.

Non-Cache/Disable DRAM Block 2 Register 3 Default=XXXX,XXXX Index:58H

Bit 7	6	5	4	3	2	1	0
NC2A19	NC2A18	NC2A17	NC2A16	NC2A15	NC2A14	NC2A13	NC2A12

Bit(s)

7:0 Non-Cache/Disable DRAM Block 2 base address bit 19 - 12.

Non-Cache/Disable DRAM Block 3 Register 1 Default=00XX,XXXX Index:59H

Bit 7	6	5	4	3	2	1	0
DSDRAM3	NCDRAM3	--	--	NC3SZ3	NC3SZ2	NC2SZ1	NC3SZ0

Bit(s)

7:6 Non-Cache/Disable DRAM Block 3 control.

Value

00: Function disabled.

01: Non-Cache the DRAM block specified by 59 - 5BH.

10: The DRAM block specified by 59 - 5BH is disabled. All memory access is directed to the AT BUS, and will not be cached.

11: Reserved.

5:4 Reserved.

3:0 Non-Cache/Disable DRAM Block 3 Size.

Value

0000: 4KB.
0001: 8KB.
0010: 16KB.
0011: 32KB.
0100: 64KB.
0101: 128KB.
0110: 256KB.
0111: 512KB.
1000: 1MB.
1001: 2MB.
1010: 4MB.

Non-Cache/Disable DRAM Block 3 Register 2 Default=XXXX,XXXX Index:5AH

Bit 7	6	5	4	3	2	1	0
--	NC3A26	NC3A25	NC3A24	NC3A23	NC3A22	NC2321	NC3A20

Bit(s)

7 Reserved.

6:0 Non-Cache/Disable DRAM Block 3 base address bit 26 - 20.

Non-Cache/Disable DRAM Block 3 Register 3 Default=XXXX,XXXX Index:5BH

Bit 7	6	5	4	3	2	1	0
NC3A19	NC3A18	NC3A17	NC3A16	NC3A15	NC3A14	NC3A13	NC3A12

Bit(s)

7:0 Non-Cache/Disable DRAM Block 3 base address bit 19 - 12.

Cache Control Register Default=0000,0010 Index:60H

Bit 7	6	5	4	3	2	1	0
ENCAH	FREEZE	SRMSZ1	SRMSZ0	DIRMAP	SRMCSM	SRMWT	EDASRAM

Bit(s)

7 Enable CACHE.

Value
- 0: CACHE disabled (Default).
- 1: CACHE enabled.

6 CACHE FREEXE. Once set, a read miss will not cause updating of the CACHE, a write hit will modify the CACHE data to maintain coherence. In other words, the content of SRAM is 'FREEZED' if read missed.

Value
- 0: Normal CACHE, Default.
- 1: CACHE FREEZE.

5:4 CACHE Size selection.

Value
- 00: 32KB, Default.
- 01: 64KB.
- 10: 128KB.
- 11: Reserved.

3 2-Way/Direct Mapped selection.

Value
- 0: 2-Way set associative CACHE, Default.
- 1: Direct Mapped CACHE.

2 SRAM Output Enable/Chip Select mode selection.

Value
- 0: SRAM is in Output Enable Mode, CRD# will not be generated when CWE# is active, Default.
- 1: SRAM is in Chip Select Mode, CRD# will be generated when CWE# is active.

1 SRAM Wait state selection.

Value
- 0: 0 wait state.
- 1: 1 wait state, Default.

0 Enables Direct Access to SRAM. Once enabled, SRAM can be directly accessed starting at location 040000H up to cache size.

Value
- 0: SRAM direct access is disabled (Default).
- 1: SRAM direct access is enabled.

	CRD0#,CWE0#	CRD1#,CWE1#
32K (2-Way,Direct):	040000-043FFFH	044000-047FFFH
64K (2-Way,Direct):	040000-047FFFH	048000-04FFFFH
128K (2-Way,Direct):	040000-04FFFFH	050000-05FFFFH

TAG RAM Control Register 1 Default=0XXX,XXXX Index:61H

Bit 7	6	5	4	3	2	1	0
ENDRTAG	DRTAGM2	DRTAGM1	DRTAGM0	--	--	--	DRTAGA8

Bit(s)

7 Enables TAG RAM Access.

Value

0: Direct access to TAG RAM disabled (Default).

1: Direct access to TAG RAM enabled. Once enabled, TAG RAM be accessed through I/O port.

6:4 Direct TAG RAM access mode control.

Value

000: Set 0 TAG low byte and LRU bit, D(7:2)=TAGA0(19:14), D(0)=LRU

001: Set 0 TAG high byte, D(6:0)=TAGA0(26:20).

010: Set 0 VALID field byte, D(7:0)=VLD0(7:0).

011: Set 0 VALID field high byte, D(7:0)=VLD0(15:8).

100: Set 1 TAG low byte and LRU bit, D(7:2)=TAGA1(19:14).

101: Set 1 TAG high byte, D(6:0)=TAGA1(26:20).

110: Set 1 VALID field low byte, D(7:0)=VLD1(7:0).

111: Set 1 VALID field high byte, D(7:0)=VLD1(15:8).

Note: For Direct Mapped CACHE, Set 0 refers to the lower half of TAG RAM (block 0-511. Set 1 refers to the upper half of the TAG RAM (block 512-1023).

3:1 Reserved.

Value

0 TAG RAM address bit 8.

TAG RAM Control register 2 Default=XXXX,XXXX Index:62H

Bit 7	6	5	4	3	2	1	0
DRTAGA7	DRTAGA6	DRTAGA5	DRTAGA4	DRTAGA3	DRTAGA2	DRTAGA1	DRTAGA0

Bit(s)

7:0 TAG RAM address bit 7 - 0.

TAG RAM Control Register 3 Default=XXXX,XXXX Index:63H

Bit 7	6	5	4	3	2	1	0
PORT USED TO ACCESS TAG RAM DIRECTLY							

Bit(s)

7:0 Data bit 7 - 0 when access TAG RAM.

TAG RAM Error Diagnostic Register 1 Default=00XX,XXXX Index:64H

Bit 7	6	5	4	3	2	1	0
ENCANM1	CAERR	--	--	--	--	--	TAGERA8

Bit(s)

7 Enables Cache Error NMI. Once enabled, NMI will be activated if CACHE ERROR occurs.
Note: Bit is always read/writable, even when register has been locked.

Value
0: Disables Cache Error NMI (Default).
1: Enables Cache Error NMI.

6 Cache Error.
Note: Bit always read/writable, even when register has been locked.

In a 2-Way set CACHE configuration, if both sets are determined to be a hit during a memory access, this bit will be set, indicating a CACHE ERROR has occurred, and adress bit 7 - 0 of the TAG ERROR location will be latched at configuration register 64 - 65H. After reading the error address, this bit should be written 0 to reopen the latches.

Value
0: Open Cache Error Address Latches, Default.
1: Cache Error has occurred.

*Note - Bit 6 is writable even if this register has been locked.

5:1 Reserved.

Value
0 Adress bit 8 of TAG ERROR location.

TAG RAM Error Diagnostic Register 2 Default=XXXX,XXXX Index:65H

Bit 7	6	5	4	3	2	1	0
TAGERA7	TAGERA6	TAGERA5	TAGERA4	TAGERA3	TAGERA2	TAGERA1	TAGERA0

Bit(s)

7:0 Address bit 7:0 of TAG ERROR location.

EMS Control Register Default=01XX,XXXX Index:70H

Bit 7	6	5	4	3	2	1	0
ENEMS	EMSWT	--	--	--	--	--	--

Bit(s)

7 EMS is disabled, Default.

Value
0: EMS is disabled, Default.
1: EMS is enabled.

6 Add 1 more wait state to DRAM when EMS is enabled.

Value
0: No extra wait added to DRAM when EMS is enabled.
1: 1 extra wait state added to DRAM when EMS is enabled.

5:0 Reserved.

EXTENSION COMOS RAM: (included in 82C206)

Use 70H as addressing port and use 71H as data port. BIOS use 40H-7FH (64 bytes) to keep special function setup data, and after power on BIOS will retrive these data to setup programmable REG. If these data lost, you can re-set thses data by setup program in the diskette.

PART IV: GUIDE TO USE BIOS

GA-386ES use LEGAL AMI BIOS and this BIOS provides the following feature in a ROM:

Standard Features

Built-in CMOS setup utility to set system configuration for Hard Disk types, Floppy Disk driver (5¼" or 3½"), time, date and disply adaptor.

Bypassing memory test

BIOS will test memory on the main board when power up, at this time, you can press <ESC> to bypass memory test.

Enter Setup Utility

When system configuration is changed, you should setup your system to build new configuration. At this time you can press <DEL> after the following message is shown on the screen:

Press <DEL> key is you want to run SETUP Utility.

after few second a menu appears on the screen, then you can use <Up-arrow> and <Down-arrow> key to select (1). Boot the system.
(2). Setup system and use <ENTER> to enter the option.

How to Use Setup Utility

Once you enter setup utility, there is a reverse cursor on the date selection and a reverse area at the bottom of the screen (this area is just for a simple comment), at this time you can press <PgUp> and <PgDn> to change the date or press <Up-arrow> or <Dn-arrow> to skip to next term.

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