

Friend-386SX Mainboard

User's Guide

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# How to Use This Manual

This manual contains information to help you get the best from your Friend-386SX system board. You should understand some of the concepts of computer architecture before using this publication. Here's what you'll find in this manual:

- Chapter 1, "System Board Features," presents an overview of the Friend-386SX system board.
- Chapter 2, "Configuring the System Board," shows you the procedures for setting up your system board for operation.
- Chapter 3, "System Board Hardware," describes the components of the Friend-386SX system board.
- Chapter 4, "The EMS 4.0 Device Driver," helps you to install the resident driver program for an optional expanded memory subsystem.

The appendixes contain reference tables for the Power-On Self Test, AMI ROM BIOS, and Phoenix ROM BIOS. You'll also find a glossary of computer terms at the end of the manual.

## Chapter 1

# System Board Features

The Friend-386SX system board provides the performance benefits of a 32-bit programming architecture with the cost savings associated with 16-bit hardware systems. The Friend-386SX is fully compatible with the IBM PC/AT, but offers greater efficiency and higher performance than PC/AT system boards.

The Friend-386SX incorporates the 32-bit Intel 80386SX microprocessor with a 16-bit external data bus. The Friend-386SX uses advanced technologies and the Chips & Technologies NEAT CHIPSet to provide high-speed performance for the most advanced multi-user, multitasking computer applications available today. The system board offers the following advanced features:

- Fully IBM PC/AT-compatible
- Intel 80386SX microprocessor runs both 16- and 32-bit software
- Microprocessor support:
  - Seven-channel direct memory access (DMA) controllers
  - 16-level interrupt system
  - system clock
  - three programmable timers

- ROM subsystem
- RAM subsystem
- 32-bit channel
- Audio subsystem with speaker
- Keyboard controller and connector
- Socket for optional 80387SX math coprocessor
- Landmark Speed Index (Version 0.99) of 26.1 MHz at 20 MHz, zero wait state
- \* 3.2 MIPS (Power Meter Test, V1.02)
- Licensed AMI BIOS (Phoenix BIOS optional)
- Six 16-bit and Two 8-bit input/output (I/O) expansion slots
- Shadow RAM for ROM BIOS and video ROM to improve system performance
- LIM-EMS 4.0 support
- Page-interleaved memory controller provides higher performance than conventional DRAM access schemes
- Low power consumption: +5V, 3.5AMP
- \* Dimensions (length x width): 21.8 x 32.8 cm (8.6 x 12.9 inches)

## Chapter 2

# Configuring the System Board

### Setting the Jumpers

Jumpers on the system board are preset. If you reconfigure your computer system, you may need to change the settings of one or more of the following jumpers. Refer to Figure 1 for the positions of the jumpers on the system board.

NOTE: A jumper is CLOSED (sometimes referred to as 'shorted') with the plastic jumper block inserted over both pins of the jumper. A jumper is OPEN with the plastic jumper block inserted over one or no pin(s) of the jumper.

#### **JP1: Speaker**

1. Speaker out
2. GND
3. N.C.
4. +5V

#### **JP2: Power LED and Keylock**

1. Power LED
2. N.C.
3. GND
4. Keylock
5. GND

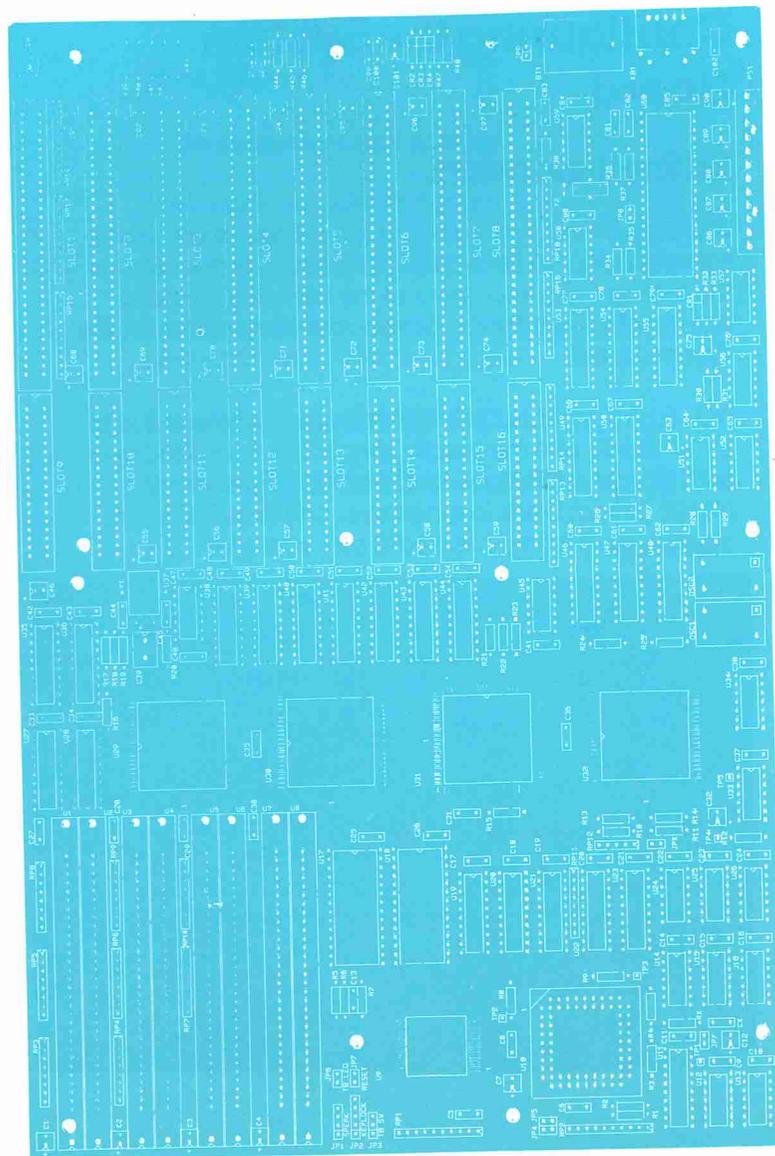


Figure 1. System Board Outline.

#### 4 Configuring the System Board

#### JP3: Clock Speed

Set the default speed of the CPU clock with this jumper:

- X - Pins 1 and 2 closed: 16 Mhz
- Pins 2 and 3 closed: 8 Mhz

The clock speed can be changed from the keyboard or with the turbo button on the system unit.

#### JP4: Coprocessor Speed Select

- Pins 1 and 2 closed: Asynchronous
- X ⊖ Pins 1 and 2 open: Synchronous

#### JP5: CPU Next Address Operation

- ⊖ Pins 1 and 2 closed: next address operation (default) 16 Mhz Pipeline
- Pins 1 and 2 open: Non-next address operation Non-Pipeline

#### JP6: Turbo LED

For connecting a Turbo LED indicator.

#### JP7: Hardware Reset

Shorting the JP7 pins will reset the system.

#### JPY: 80387/SX Install select

- W/80387-SX, "open".
- X W/O 80387-SX, "close".

### JP8: Display Type

- Pins 1 and 2 closed: color monitor is connected.
- Pins 1 and 2 open: monochrome monitor is connected.

### JP9: Battery Selection

- Pins 1 and 2 closed: on-board battery
- Pins 2 and 3 closed: discharge the CMOS Real Time Clock.

### PS1: Power Supply Connector

1. Power good
2. + 5V
3. +12V
4. - 12V
5. GND
6. GND
7. GND
8. GND
9. - 5V
10. + 5V
11. + 5V
12. + 5V

### Changing the CPU Speed

When you boot your computer, the Friend-386S will operate at the clock speed that you have chosen with the CMOS Setup software (see the next section of this chapter for information on CMOS Setup software).

Change the clock speed by pressing the turbo switch on your computer. You can also press the CTRL, ALT, and "-" or CTRL, ALT, and "+" keys simultaneously.

### CMOS Software Setup

CMOS (Complementary Metal Oxide Semiconductor) RAM is used to store configuration information such as:

- the date and time
- the storage capacity of the system board
- what type of display adapter is installed
- the number and type of disk drives installed

The CMOS memory is maintained by a battery that is installed on the system board. By using the battery, all memory in CMOS can be retained when the system power switch is turned off. You may change the CMOS configuration by running the ROM BIOS Setup utility.

### Using the AMI BIOS Setup Utility

To enter the setup utility, turn on or reset the computer system. The ROM BIOS performs system diagnostics and displays the size of the memory being tested. You can bypass the memory test by pressing the <ESC> key. This option is useful if system memory is large.

This prompt appears on the screen next:

Press <DEL> Key to run SETUP or DIAGS

Press the DEL key to enter the Setup or Diagnostics

After you press the DEL key, the following message appears on the screen:

```
EXIT FOR BOOT
RUN CMOS SETUP
RUN DIAGNOSTICS
```

1. Select RUN CMOS SETUP
2. use function key <→> or <←> to select the item
3. Use function key <PgUp> or <PgDn> to modify the data
4. After all data is setup complete press <ESC> to write data into CMOS and exit

```
CMOS SETUP (C) Copyright 1985-1989, American Megatrends Inc..
Data (mn/date/year): Sat, Jul 08 1989   Base memory size : 640 KB
Time (hour/min/sec): 08 : 14 : 25       Ext. memory size : 0 KB
Floppy drive A: : 1.2 MB, 5"           Numeric processor : Not Installed
Floppy drive B: : Not Installed

Cyl  Head  WPcom  LZone  Sec   Size
615   4      300    615   17    20 MB

Hard disk C: type : 2
Hard disk D: type : Not Installed
Primary display  : Monochrome
Keyboard         : Installed

Sun*Mon*Tue*Wed*Thu*Fri*Sat
15* 16* 17* 18* 19* 20* 21*
2*  3*  4*  5*  6*  7*  8*
9* 10* 11* 12* 13* 14* 15*
16* 17* 18* 19* 20* 21* 22*
23* 24* 25* 26* 27* 28* 29*

Scratch RAM option : 1

Write data into CMOS and exit (Y/N)? Y

ESC = Exit.      = Select.  PaUp/PaDn = Modify  0* 1*  2*  3*  4*  5*
```

5. After reboot run set386sx setup utility to set the parameters of the chipsets.

Enter the correct time in the format shown on the screen. To keep the current time, press the <ENTER> key. From this point, the setup takes one of two different paths, depending upon the status of the CMOS RAM.

## CMOS Initialized

If the CMOS RAM has already been initialized, you will see the following information on the screen:

```
Fixed disk drive C type : X (If Installed else Not Installed)
Fixed disk drive D type : X (If Installed else Not Installed)
Diskette drive A is    : High Capacity (If 360KB then Double
                        Sided, If not present not installed)
Diskette drive B is    : Double sided (Other options as above)
Base Memory Size is    : XXX KB
Expansion memory size is : XXXX KB
```

Are these options correct (Y/N)?

If the information displayed above is correct, press <Y> and then the <ENTER> key to boot the system with the new information.

## CMOS Uninitialized

If the CMOS RAM has not been initialized, you must first enter the disk drive type definition for fixed drive C. The following message appears on screen:

.....WARNING.....

Entering the wrong disk drive TYPE causing improper operation of the disk. If disk not installed press <RETURN> For disk TYPE details press <ESC>

Enter disk drive C type (1 - 47)?

To see a list of disk type details, press the ESC key. This information is also provided in Appendix B. When you have finished viewing the disk type details, press ESC again to return to the above screen.

Enter the appropriate number for your drive type and then press the ENTER key. Note that pressing the ENTER key without first entering a number indicates the absence of the drive C. You will then be asked to enter the type of the disk drive D. The procedure for entering the drive D disk type details is the same as that described above for drive C. If you do not have a disk drive D on your system, press the ENTER key without entering a number.

At this point you have entered all the information the BIOS requires for starting the system.

NOTE: BIOS detects a few details by itself, e.g., the diskette drive type for a 360KB drive.

### NEAT Setup

The NEAT Setup utility is provided on disk. When you enter the NEAT Setup utility, a series of menus (see Figure 2) lets you set the parameters of the 82C206, 82C211, and 82C212. The NEAT Setup utility also lets you enable or disable the shadow RAM and EMS functions.

**CAUTION: Changing NEAT parameters is not recommended for users who have not had previous experience. If in doubt, you should refer the job to a qualified maintenance person.**

NOTE: To use the shadow RAM function, you need at least 1MB RAM on-board.

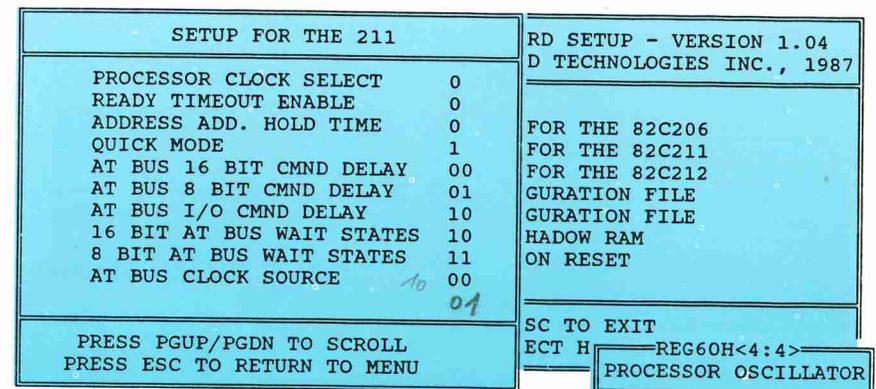
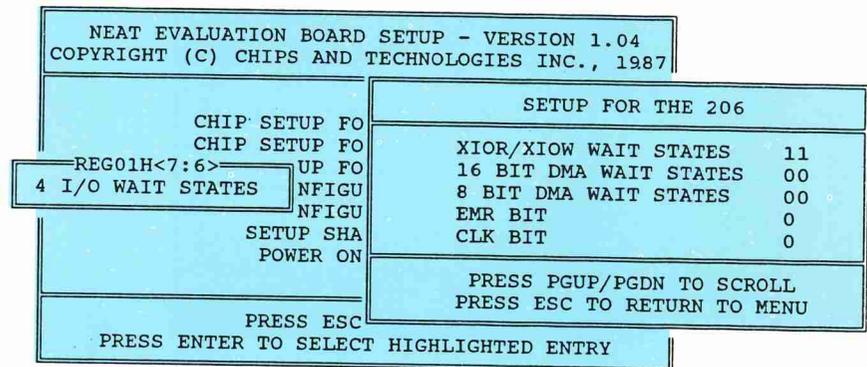
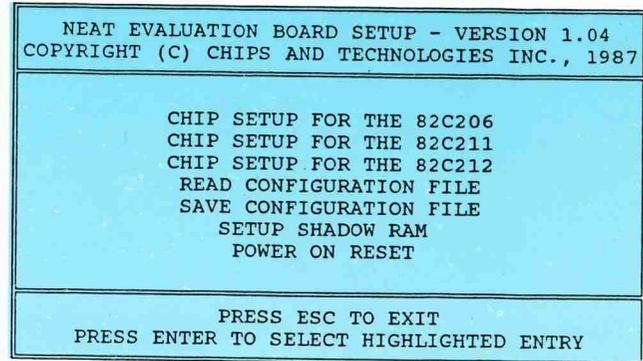


Figure 2. NEAT Setup Screens

oEAS EAS

SETUP FOR THE 212			
RAM/ROM CONFIGURATION	0000	EMS ENABLE	0
RAM/ROM CONTROL	1110	EMS WAIT STATES	00
512K - 640K ADDRESS MAP	0	RW-ROM WAIT STATES	11
MAP RAM AT 0A0000-0BFFFFH	00000000	EMS BASE ADDRESS (HEX)	2
MAP RAM AT 0C0000-0DFFFFH	00000000	EMS PAGE REG. I/O-BASE (HEX)	0
MAP RAM AT 0E0000-0FFFFFH	00000000	EMS PAGE 0 - POSITION	00
BANK 0/1 DRAM TYPE	10	EMS PAGE 1 - POSITION	00
BANK 0/1 NUMBER OF BANKS	0	EMS PAGE 2 - POSITION	00
BANK 2/3 DRAM TYPE	00	EMS PAGE 3 - POSITION	00
BANK 2/3 NUMBER OF BANKS	0	EMS SIZE (HEX)	0
DRAM ACCESS WAIT STATES	1	DTO - RAS T/O ENABLE	0
INTERLEAVED PAGE MODE	1	PGA20 - GATE A20 CONTROL	0
RELOCATE DRAM AT 640K-1MB	0	EXTERNAL EMS MAPPER ENABLE	0

PRESS PGUP/PGDN TO SCROLL  
PRESS ESC TO RETURN TO MENU

REG65H<7:7>  
RAM AT 768K R/W

NEAT EVALUATION BOARD SETUP - VERSION 1.04  
COPYRIGHT (C) CHIPS AND TECHNOLOGIES INC., 1987

CHIP SETUP FOR THE 82C206  
CHIP SETUP FOR THE 82C211

CONFIGURATION FILE NAME: AS201 (default valus)

SETUP SHADOW RAM  
POWER ON RESET

PRESS ESC TO EXIT  
PRESS ENTER TO SELECT HIGHLIGHTED ENTRY

NEAT EVALUATION BOARD SETUP - VERSION 1.04  
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CHIP SETUP FOR THE 82C206  
CHIP SETUP FOR THE 82C211

DISABLE SHADOW RAM

UP FOR  
NFIGU  
NFIGU  
SETUP SHA  
POWER ON

SETUP SHADOW RAM FOR 212  
SHADOW FOR ROM BIOS 0  
SHADOW FOR VIDEO RAM 0

PRESS PGUP/PGDN TO SCROLL  
PRESS ESC TO RETURN TO MENU

PRESS ESC  
PRESS ENTER TO SELECT HIGHLIGHTED ENTRY

Figure 2. NEAT Setup Screens

## Chapter 3

# System Board Hardware

The Friend-386SX system board is a multi-layer printed circuit board (PCB) that fits in any system unit designed for PC/XT or baby AT boards. The Friend-386SX system board offers a cost-effective alternative for upgrading your current system to the 32-bit level.

The Friend-386SX system board employs Very Large Scale Integrated (VLSI) modules such as the Intel 80386SX central processing unit (CPU) and the Chips & Technologies NEAT CHIPSet. The Friend-386SX includes a socket for an optional 80387SX math coprocessor. It employs dry-film and solder-mask materials, and features an 8MHz AT-compatible I/O channel bus and the AMI ROM BIOS (Phoenix BIOS optional).

The Friend-386SX receives direct current from the power supply via two six-pin connectors. Other connectors on the system board are for the keyboard, speaker, and battery.

### The 80386SX Microprocessor

The heart of the Friend-386SX system board is the 80386SX microprocessor. The 80386SX is the integrated circuit responsible for performing arithmetic and logical operations and controlling the flow of information throughout the computer system.

cal operations and controlling the flow of information throughout the computer system.

**Table 1. 80286, 80386SX, and 80386 comparison.**

	80286	80386SX	80386
Internal Architecture (bits)	16	32	32
Data Bus Size (bits)	16	16	32
Address Bus Size (bits)	24	24	32
Physical Address Space	16 MB	16 MB	4 GB
Virtual Address Space	1 GB	64 TB	64 TB
Paging	NO	YES	YES
Protection	YES	YES	YES
Virtual 86 Mode	NO	YES	YES
Arithmetic Coprocessor	80287	80387SX	80387

The 80386SX is a high-performance 32-bit microprocessor that is 100% object code compatible with the Intel 80286, 8088 and 8086 microprocessors. With virtual 8086 mode addressing, the microprocessor can concurrently execute multiple programs written for the

8088 or 8086 using an operating system such as UNIX or Microsoft OS/2.

The 80386SX microprocessor subsystem includes the following features:

- Full 32-bit Internal Architecture
- Runs 386 Software in a cost effective 16-bit hardware environment
- High performance 16-bit data bus
- Integrated Memory Management Unit
- Virtual 8086 mode allows execution of 8086 software in a protected and paged system
- High speed numerics support with the optional 80387SX coprocessor
- Large uniform address space

**80386SX Base Architecture**

The 386SX microprocessor consists of a central processing unit, a memory management unit and a bus interface.

The CPU consists of the execution unit and the instruction unit. The execution unit contains the eight 32-bit general purpose registers that are used for both address calculation and data operations and a 64-bit barrel shifter used to speed shift, rotate, multiply, and divide operations. The instruction unit decodes the

instruction opcodes and stores them in the decoded instruction queue for immediate use by the execution unit.

The memory management unit (MMU) consists of a segmentation unit and a paging unit. Segmentation allows the managing of the logical address space by providing an extra addressing component, one that allows easy code and data relocatability, and efficient sharing. The paging mechanism operates beneath and is transparent to the segmentation process, to allow management of the physical address space.

The segmentation unit provides four levels of protection for isolating and protecting applications and the operating system from each other. The hardware enforced protection allows the design of systems with a high degree of integrity.

The 386SX microprocessor has two modes of operation: Real Address Mode (Real Mode), and Protected Virtual Address Mode (Protected Mode). In Real Mode the 386SX microprocessor operates as a very fast 8086, but with the 32-bit extensions if desired. Real Mode is required primarily to set up the processor for Protected Mode operation.

Within Protected Mode, software can perform a task switch to enter into tasks designated as Virtual 8086 Mode tasks. Each such task behaves with 8086 semantics, thus allowing 8086 software (an application program or an entire operating system) to execute. The Virtual 8086 tasks can be isolated and protected from one another and the host 386SX microprocessor oper-

ating system by use of paging.

### **The 80387SX Math Coprocessor**

The Friend-386SX system board has a socket for an optional 80387SX math coprocessor.

The 80387SX math coprocessor is an integrated circuit that enables the system to perform high-speed arithmetic, logarithmic, and trigonometric operations. The coprocessor works in parallel with the microprocessor. The parallel operation decreases operating time by allowing the coprocessor to do mathematical calculations while the microprocessor continues to do other functions.

The 80387SX is compatible at the object code level with the 80387 math coprocessor. It contains the same 16/24-bit bus structure as the 80386SX microprocessor. The 80387SX implements the IEEE-754 floating-point standard and delivers three to five times the performance of the 80287.

The coprocessor works with seven numeric data types, which are divided into the following three classes:

- Binary integers (3 types)
- Decimal integers (1 type)
- Real numbers (3 types)

If a program does a lot of calculations, it may run much faster with an 80387SX. However, in order to take advantage of an 80387SX, your application programs must be designed to use the 80387SX's features. If

you want to use an 80387SX to speed up a program, check with the maker of the program to see whether it can take advantage of an 80387SX.

### Installing a Math Coprocessor

To install an optional math coprocessor on the system board, proceed as follows.

**CAUTION: This installation is not recommended for users who have not had previous experience in the assembly of AT class computer systems. If in doubt, you should refer the job to a qualified maintenance person.**

1. Make sure that you observe precautions against static electricity; a math coprocessor is sensitive to such damage.
2. Turn off your system.
3. Align the 80387SX so that the beveled corner of the chip corresponds to the corner of the socket U10 labeled "1".
4. Align the individual pins with the socket holes.

straighten the pins, grasp the 80387SX, lay all the pins on one side flat against a hard surface (e.g., the top of the power supply) and gently bend them inwards.

**CAUTION: Math coprocessor pins are fragile and easily bent or broken.**

5. Carefully but firmly press the chip into the socket.
6. To indicate the presence of the coprocessor, remove the plastic jumper block from pins 1 and 2 of JPY.

### Expansion Slots

The I/O channel is accessed via eight expansion slots on the 80386SX system board. These slots are actually 62- and 36-pin connectors.

Two slots (marked slots 1 and 7) are 8-bit slots that are compatible with those on the IBM PC and PC/XT. These 62-pin address up to 1 MB, and allow 8-bit data transfers.

Six slots (marked slots 2/10, 3/11, 4/12, 5/13, 6/14, and 8/15) are 62-pin and 34-pin slots that are compatible with those on the IBM PC/AT. The slots have 16 MB address ability, enabling 16-bit data transfers.

### RAM

The RAM (random-access memory) is used to store the programs currently being executed and the data required or generated by their execution. On the system

board, RAM is located in eight rows of SIMMs (single in-line modules).

Combine different SIMMs on the system board to obtain the desired amount of RAM (from 512 KB to 8 MB). Each row of SIMM sockets can hold a 256 Kbit or 1 Mbit module. Use DRAM with an access time of 100 nanoseconds, to run the CPU at 16MHz; use 80-nanosecond DRAM to run the CPU at 20MHz. The following table shows possible memory combinations for the system board.

### System Board Memory Sizes

	DRAM Type				Total Memory
	Bank 0	Bank 1	Bank 2	Bank 3	
1.	256kB	0	0	0	512KB
2.	256kB	256kB	0	0	1MB
3.	256kB	256kB	256kB	256kB	2MB
4.	1mB	0	0	0	2MB
5.	1mB	1mB	0	0	4MB
6.	1mB	1mB	1mB	1mB	8MB

To install a SIMM, align pin 1 on the SIMM to the edge of the SIMM socket marked on the board with a stenciled triangle.

## ROM and ROM BIOS

The system board has two Read-Only Memory (ROM) modules (16 x 2) that contain the system BIOS (Basic Input/Output System). Either 27128 or 27256 ROM chips can be inserted into the sockets, but only the same type of chip can be inserted in the sockets at the same time.

The CPU accesses ROM through a local I/O bus 16 bits at a time. The system board functions correctly with ROM devices that have 250 nanosecond or shorter access times.

The BIOS is made up of code and programs that provide the device-level control for the major I/O devices in the system. The BIOS contains a set of routines that check out the system when you turn it on (called POST, for Power-On Self Test).

The BIOS is compatible with the IBM PC/AT BIOS as long as programs access the BIOS using software interrupts and do not specify absolute memory locations. Programs that refer to absolute locations in the IBM PC/AT BIOS will not function correctly while running on the Friend-386SX system board. The ROM BIOS does not contain code for the BASIC interpreter.

## The NEAT CHIPSet

The Chips & Tech CS8221 NEAT CHIPSet is an enhanced, high performance 4-chip VLSI implementation of the control logic used on the IBM PC/AT. The NEAT CHIPSet consists of the 82C211 CPU/Bus controller, the 82C212 Page Interleave and EMS Memory control-

ler, the 82C215 Data/Address buffer and the 82C206 Integrated Peripherals Controller (IPC).

The NEAT CHIPSet supports the local CPU bus, a 16-bit system memory bus, and the AT buses. The 82C211 provides synchronization and control signals for all buses. The 82C211 also provides an independent AT bus clock and allows for dynamic selection between the processor clock and the user-selectable AT bus clock. Command delays and wait states are software configurable, providing flexibility for slow or fast peripheral boards.

- Separate CPU and AT bus clocks
- Page/Interleaved Memory Controller
- Integrated Lotus-Intel-Microsoft Expanded Memory Specification (LIM EMS) Memory Controller. Supports EMS 4.0.
- Software configurable command delays, wait states, and memory organisation
- Optimized for OS/2 operation
- Shadow RAM for BIOS to improve system performance

#### **The 82C212 Page/Interleave and EMS Memory Controller**

The 82C212 Page/Interleave and EMS Memory Controller provides an interleaved memory subsystem design with page mode operation. It supports up to 8 MB of on-board DRAM with combinations of 256 Kbit and 1 Mbit DRAMs. Through the Page/Interleaved memory

scheme, the processor can operate at 20MHz with zero wait state memory accesses, using 100 nanosecond DRAMs.

Shadow RAM loads system BIOS or video BIOS from slower ROM directly into fast RAM on boot-up of the computer. The shadow RAM feature allows faster execution of code stored in ROM. The firmware routines of the BIOS are copied into a special memory area; then, through the memory-mapping abilities of the 80386SX, the copy of the BIOS is assigned to the same addresses the BIOS originally used. The original code is switched out of reach.

In an MS-DOS environment, memory above 1 MB can be treated as LIM EMS memory.

#### **82C206 Integrated Peripherals Controller (IPC)**

The 82C206 is an LSI implementation of the standard peripherals required to implement an IBM PC/AT system board. It is fully compatible to Intel's 8237 DMA controller, 8259 Interrupt controller, 8254 Timer/Counter, and Motorola's 146818 Real Time Clock. It offers 7 DMA channels, 13 interrupt request channels, 2 timer/counter channels, and a real-time clock. The 82C206 provides all of the standard peripherals required for a system board implementation except the keyboard interface controller.

The equivalent of two DMA controllers is provided in the 82C206. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information between a peripheral device and memory directly. This allows high-speed information transfer with little CPU intervention.

The two DMA controllers are internally connected in such a way as to provide the user with four DMA channels (DMA1) for transfers to 8-bit peripherals and three channels for 16-bit transfers (DMA2). DMA2 channel 0 provides the cascade interconnection between the two devices, thereby maintaining IBM PC/AT compatibility. Included as part of the DMA subsystem is the Page Register (DMAPAGE) device, which is used to supplement the DMA and drive the upper address lines when required.

The DMA controllers are cascaded together to service seven DMA channels. Each of the seven channels is assigned a unique I/O address:

Channel	I/O Address	Function
0	0087	spare
1	0083	SDLC
2	0081	diskette adapter
3	0082	spare
4	cascading	cascade for DMA controller 1
5	0088	spare
6	0089	spare
7	008A	spare

The equivalents of two 8259 Programmable Interrupt Controllers are included in the 82C206, providing sixteen interrupt channels. An interrupt (int) is a signal, generated by either hardware or software, that alerts the CPU that some function needs to be carried out. The interrupt channels accept requests from peripherals, resolve priority on pending interrupts and interrupts in service, issue an interrupt request to the CPU, and provide a vector that is used as an index by the CPU to determine which interrupt service routine executes.

The interrupt channels are partitioned into two cascading controllers (INTC1 and INTC2) with 8 inputs each. Of these 16 channels, three are connected internally to various devices, allowing 13 user-definable channels of interrupt. The three internally connected channels are as follows:

Channel 0 – Counter/Timer

Channel 2 – Cascade to Slave Interrupt Controller (INTC2)

Channel 8 – Real Time Clock Interrupt

The remaining 13 channels may be defined and used as necessary to meet specific system requirements.

A Counter/Timer subsystem, containing three independent counters, is provided in the 82C206. All three counters are driven from a clock input pin that is independent from the other clock inputs to the device. Counter 0 is connected to interrupt 0 of INTC1. It is intended to be used as a multi-level interrupt to the system for such tasks as time keeping and task switching. Counter 1 may be programmed to generate pulses or square waves for use by external devices. Counter 2 is a full-function Counter/Timer with a gate input for controlling the internal counter. This channel can be used as an interval counter, a timer, or as a gated rate/pulse generator.

The 82C206 includes a Real Time Clock (RTC) for maintaining the time and date in addition to storing computer system configuration information. This subsystem also contains 114 bytes of RAM in addition to the Clock/Calendar registers. The Clock/Calendar information

and RAM are kept active by connecting the device to an external battery when system power is turned off. The use of CMOS technology means that the RTC consumes very little power and can be maintained for long periods of time with an inexpensive battery.

### System Memory

**Table 2. System Memory Map**

address	capacity	function
000000 – 09FFFF	640KB	base memory
0A0000 – 0BFFFF	128KB	video RAM; graphics, display buffer
0C0000 – 0DFFFF	128KB	reserved for ROM on I/O adapters
0E0000 – 0FFFFFF	128KB	BIOS ROM on system board
100000 – FDDEEE	15MB	extended memory board
FE0000 – FFFFFFF	128KB	duplicated code assignment at address 0E0000

### I/O Port Addresses

**Table 3. I/O Port Address Map**

Devices on system board:

Address	Device
000 – 01F	1st DMA chip
020 – 03F	1st interrupt controller chip
040 – 05F	timer
060 – 06F	keyboard controller (8042)
070 – 07F	real time clock (82C206)
080 – 08F	DMA page registers
0A0 – 0BF	2nd interrupt controller chip
0C0 – 0DF	2nd DMA chip
0F0	clear math coprocessor busy
0F1	reset math coprocessor
0F8	math coprocessor

Devices on I/O slots:

address	device
1F0 – 1F8	hard disk
200 – 207	game I/O
278 – 27F	parallel printer port 2 (LPT3)

2F8 – 2FF	serial port 2 (COM2)
300 – 31F	prototype card
360 – 36F	reserved
378 – 37F	parallel printer port 1 (LPT2)
380 – 38F	SDLC2
3A0 – 3AF	SDLC1
3B0 – 3BF	monochrome video and parallel printer (LPT1)
3C0 – 3CF	reserved
3D0 – 3DF	CGA video card
3F0 – 3F7	floppy disk controller
3F8 – 3FF	serial port 1 (COM1)

## Chapter 4

### The EMS 4.0 Device Driver

The EMS (Expanded Memory Specification) Version 4.0 device driver is a standard MS-DOS device driver that gets loaded at boot time by the CONFIG.SYS file. Because EMS 4.0 is a device driver, it should look like this in the CONFIG.SYS file:

```
DEVICE=EMM.SYS
```

Without anything else included in this command line, the EMS driver will get loaded with the default hardware values of the I/O address that enables the EMS and the memory address used for EMS paging. These default values are dependent on the NEAT implementation of EMS.

To change these default values, as well as add a few extra features, the EMS device driver command line can look like this:

```
DEVICE=EMM.SYS -Ix -My -Pzz -D
```

where

I	= I/O address to enable EMS pages
x	= 0 == 208h
	= 1 == 218h
	= 5 == 258h
	= 6 == 268h
	= A == 2A8h
	= B == 2B8h
	= E == 2E8h

M	= page frame address (address of 64KB window)
y	= 1 == C000h = 2 == C400h = 3 == C800h = 4 == CC00h = 5 == D000h
P	= maximum number of open processes (defaults to 64)
zz	= number of processes (1 -128)
D	= enable EMS diagnostics

The command line parameters can be in either upper or lower case.

When the EMS driver is first executed, a title and copyright notice will appear on the screen as follows:

```
EMS Expanded Memory Device Driver  Ver. 4.0
Copyright (c) Chips and Technologies Inc., 1987
```

If the EMS driver detects that a previous EMS driver has been loaded, it will put this message on the screen:

```
An Expanded Memory Manager has already
been installed.
```

The EMS driver will then not get loaded into the system.

When the EMS driver gets loaded by MS-DOS, an internal check is done on the EMS configuration in hard-

ware. If the driver detects any conflicts that would cause EMS not to function properly, the message:

```
The EMS setup has been incorrectly
specified. No EMS is available.
```

will appear on the screen after the EMS copyright notice and EMS will be disabled. If the EMS hardware is configured properly and the I/O address is overridden by the command line parameter, the screen will show this message:

```
The EMS I/O address has been changed.
```

If the diagnostics option is selected, this message will appear on the screen:

```
Testing EMS Expanded Memory Page Num-
ber: NNN
```

The NNN represents the page number currently under test. If the diagnostics fail, the EMS will be disabled and the following message appears on the screen:

```
Expanded Memory FAILED diagnostics
test.
```

If the diagnostics pass, or if diagnostics were not specified on the command line, the EMS driver has been loaded correctly and EMS is enabled. The final message to appear on the screen is:

```
There are XXX pages, or YYYY Kbytes of
EMS Expanded Memory on the system.
```

The system can now be used to support Lotus/Intel/Microsoft EMS 4.0 in the same manner as standard EMS cards.

## Appendix A:

# The Power-On Self Test

The Power-On Self Test (POST) runs each time the system is turned on. The POST checks memory, the CPU, the display monitor, the keyboard, the disk drives, and other installed options.

**Table 4. POST Boot Messages.**

Message	Possible Cause	Solution
Diskette configuration error	The specified configuration is not supported	Change the configuration
Diskette drive reset failed	The diskette adapter has failed	Check the diskette adapter
Diskette drive 1 seek failure	The B: drive failed or is missing	Check the B: drive
Diskette drive 0 seek failure	The A: drive failed or is missing	Check the A: drive
Diskette drive reset failed	The diskette adapter has failed.	Check the diskette adapter.
Diskette read failure-strike F1 to retry boot	The diskette is either not formatted or is defective.	Replace the diskette with a bootable diskette and retry boot.
Display adapter failed; using alternate	<ul style="list-style-type: none"><li>• The color/monochrome switch is set wrong</li><li>• The primary video adapter failed.</li></ul>	<ul style="list-style-type: none"><li>• Change the switch to the correct setting.</li><li>• Check the primary video adapter.</li></ul>
Errors found disk X: Failed initialization	POST reports hard disk configuration information is incorrect.	Rerun SETUP and enter correct hard disk information.

Errors found Incorrect configuration information memory size miscompare	POST reports the size of base or expansion memory does not agree with configuration information.	Rerun SETUP and enter correct memory size.
Gate A20 failure	Protected mode cannot be enabled.	Check the system board.
Hard disk configuration error	The specified configuration is not supported.	Correct the fixed disk configuration.
Hard disk controller failure.	The controller card has failed.	Replace the controller card.
Hard disk failure	Bad disk	Retry boot. If that doesn't work, replace the hard disk.
Hard disk read failure – strike F1 to retry boot	The hard disk is defective.	Retry boot. If that doesn't work, replace the hard disk.
Invalid configuration information – please run SETUP program	<ul style="list-style-type: none"> <li>• Memory size is incorrect.</li> <li>• Display adapter is configured incorrectly.</li> <li>• Wrong number of diskette drives.</li> </ul>	Run the SETUP utility.
Keyboard clock line failure	Either the keyboard or the keyboard cable connection is defective	Make sure the keyboard cable and keyboard are connected properly.
Keyboard data line failure		
Keyboard controller failure	The keyboard controller firmware has failed	Check the keyboard controller.
Keyboard is locked – please unlock	The keyboard lock located at the front of the computer is activated.	Unlock the keyboard.

Keyboard stuck key failure	A key is jammed.	Try pressing the key again.
Memory address line failure at <i>hex-value</i> , read <i>hex-value</i> , expecting <i>hex-value</i>	Circuitry associated with the memory chips has failed.	Check the circuitry.
Memory data line failure at <i>hex-value</i> , read <i>hex-value</i> , expecting <i>hex-value</i>	One of the memory chips or associated circuitry has failed	Replace the memory chips.
Memory high address line failure at <i>hex-value</i> , read <i>hex-value</i> , expecting <i>hex-value</i>	Circuitry associated with the memory chips has failed.	Check the circuitry.
Memory double word logic failure at <i>hex-value</i> , read <i>hex-value</i> , expecting <i>hex-value</i>	Memory chip circuitry has failed.	Replace the memory chip.
Memory odd/even logic failure at <i>hex-value</i> , read <i>hex-value</i> , expecting <i>hex-value</i>	Circuitry associated with the memory chips has failed	Check the circuitry.
Memory parity failure at <i>hex-value</i> , read <i>hex-value</i> , expecting <i>hex-value</i>	One of the parity memory chips has failed.	Replace the memory chips.
Memory write/read failure at <i>hex-value</i> , read <i>hex-value</i> , expecting <i>hex-value</i>	One of the memory chips has failed.	Replace the memory chips.
No boot device available – strike F1 to retry boot	Either diskette drive A: the hard disk, or the diskette itself is defective	Retry boot. If that doesn't work, replace the floppy diskette or the hard disk.

No boot sector on hard disk – strike F1 to retry boot	The C: drive is not formatted or is not bootable	Format the C: drive. Make it bootable.
Not a boot diskette – strike F1 to retry boot	The diskette in drive A: is not formatted as a bootable diskette	Replace the diskette with a bootable diskette and retry boot.
No timer tick interrupt	The timer chip has failed	Check the timer chip on the system board.
Hex-value optional ROM bad checksum = hex-value	The peripheral card contains a defective ROM.	Replace the peripheral card.
Shutdown failure	The keyboard controller its associated logic has failed.	Check the keyboard controller.
Time-of-day clock stopped	The CMOS time-of-day clock chip has failed.	Run the SETUP utility.
Time-of-day not set – please run SETUP program	Clock not set.	Run the SETUP utility.
Timer chip counter 2 failed	Chip failed.	Check the timer chip system board.
Timer or interrupt controller bad	Either the timer chip or the interrupt controller is defective.	Check the timer chip or the interrupt controller on the system board.
Unexpected interrupt in protected mode	The non-maskable interrupt (NMI) port can't be disabled.	Check the system board, particularly the logic associated with the non-maskable interrupt.

**Table 5. POST Information Messages.**

Message	Meaning
Hex-value Base Memory	The amount of base memory that tested successfully.
Hex-value Expanded Memory	The amount of expanded memory that tested successfully.
Hex-value Extended Memory	The amount of extended memory that tested successfully.
Hex-value Extra Memory	The amount of extra memory that tested successfully.
Hex-value Standard Memory	The amount of standard memory that tested successfully.
Decreasing available memory	This message immediately follows any memory error message, and informs you that the memory chips are failing.
Memory tests terminated by keystroke	This message indicates that you have pressed the Spacebar while the memory tests were running. This stops the memory tests.
Strike the F1 key to continue	This message indicates that an error was found during POST. Pressing the F1 key allows the system to attempt to boot.

**Table 6. Run-Time Messages.**

Run-time messages are displayed if an error occurs after the boot procedure is complete.

Message	Possible Cause	Solution
I/O card parity interrupt at <i>address</i> . Type (S)hut off NMI, (R)eboot, other keys to continue.	The peripheral card has failed.	Type (S)hut off NMI.  Note: This will only temporarily allow you to continue. You must replace the peripheral card.
Memory parity interrupt at <i>address</i> . Type (s)hut off NMI, (R)eboot, other keys to continue	A memory chip(s) has failed.	Type (S)hut off NMI.  Note: This will only temporarily allow you to continue. You must replace the memory chip(s).
Unexpected HW interrupt <i>interrupt</i> at <i>address</i> . Type (R)eboot, other keys to continue	This could be any hardware-related problem.  Note; Not displayed if the extended interrupt handler is not enabled.	Check the hardware.
Unexpected SW interrupt <i>interrupt</i> at <i>address</i> . Type (R)eboot, other keys to continue	There is an error(s) in the software program.  Note: Not displayed if the extended interrupt handler is not enabled.	Try turning the machine off and then on again. If that doesn't work, check the program.
Unexpected type 02 interrupt at <i>address</i> . Type (S)hut off NMI, (R)eboot, other keys to continue	There is an error(s) in the software program.  Note: Not displayed if the extended interrupt handler is not enabled.	Try turning the machine off and then on again. If that doesn't work, check the program.

**Appendix B:**

**AMI ROM BIOS**

**Table 7. AMI ROM BIOS Fixed Drive Type**

Type	Cylinders	Heads	Write-Precomp	Landing Zone	Capacity (MB)
1	306	4	128	305	10
2	615	4	300	615	21
3	615	6	300	615	31
4	940	8	512	940	64
5	940	6	512	940	48
6	615	4	FFFF	615	21
7	462	8	256	511	31
8	733	5	FFFF	733	31
9	900	15	FFFF	901	115
10	820	3	FFFF	820	21
11	855	5	FFFF	855	36
12	855	7	FFFF	855	51
13	306	8	128	319	21
14	733	7	FFFF	733	44
15	000	0	000	000	00
16	612	4	0000	663	21
17	977	5	300	977	42
18	977	7	FFFF	977	58
19	1024	7	512	1023	61
20	733	5	300	732	31
21	733	7	300	732	42
22	733	5	300	733	31
23	306	4	0000	336	10
24	925	7	0000	925	56
25	925	9	FFFF	925	72
26	754	7	754	754	46
27	754	11	FFFF	754	72
28	699	7	256	699	42
29	823	10	FFFF	823	71
30	918	7	918	918	55
31	1024	11	FFFF	1024	98
32	1024	15	FFFF	1024	133
33	1024	5	1024	1024	44
34	612	2	128	612	10

35	1024	9	FFFF	1024	80
36	1024	8	512	1024	71
37	615	8	128	615	42
38	987	3	987	987	25
39	987	7	987	987	60
40	820	6	820	820	42
41	977	5	977	977	42
42	981	5	981	981	42
43	830	7	512	830	50
44	830	10	FFFF	830	72
45	917	15	FFFF	918	115
46	000	00	000	000	00

**Table 8. AMI ROM BIOS Error Message Reference**

**Errors Displayed on Screen:**

Error Condition	Error Type
Gate A20 Error	Fatal
Interrupt Controller #1 Failure	Fatal
Keyboard Error	Nonfatal
Keyboard/Interface error	Nonfatal
CMOS battery state low	Nonfatal
CMOS system options not set	Nonfatal
CMOS checksum failure	Nonfatal
CMOS memory size mismatch	Nonfatal
CMOS system time and date not set	Nonfatal
CMOS display configuration mismatch	Nonfatal
Display switch setting not proper	Nonfatal
Keyboard is locked -- unlock it	Nonfatal
Floppy disk controller failure	Nonfatal
Hard disk unit 0 error	Nonfatal
Hard disk unit 1 error	Nonfatal
Hard disk unit 1 is not defined in CMOS	Nonfatal

**Error Generation Beeps:**

Error Condition	Error Type	Beep Count
DRAM refresh failure	Fatal	1
Parity circuit failure	Fatal	2
Base 64 KB RAM failure	Fatal	3
System timer failure	Fatal	4
Processor failure	Fatal	5
Keyboard controller --		
Gate A20 Error	Fatal	6
Virtual mode exception error	Fatal	7
Display memory		
R/W test failure	Nonfatal	8
ROM BIOS checksum failure	Fatal	9

**Table 9. AMI BIOS List of Checkpoints**

Check Point	Meaning
01	NMI disabled and 286/386 register test about to start
02	286 register test over
03	ROM checksum over
04	8259 initialization OK
05	CMOS pending interrupt disabled
06	Video disabled and system timer counting OK
07	CH-2 of 8253 OK
08	CH-2 delta count test OK
09	CH-1 delta count test OK
0A	CH-0 delta count test OK
0B	Parity status cleared
0C	Refresh and system timer OK
0D	Refresh link toggling OK
0E	Refresh period ON/OFF 50% OK

10 Confirmed refresh ON and start 64KB memory test  
 11 Address line test OK  
 12 64 KB base memory test OK  
 13 Interrupt vectors initialized  
 14 8242 keyboard controller test OK  
 15 CMOS read/write test OK  
 16 CMOS checksum/battery OK  
 17 Monochrome mode set OK  
 18 Color mode set OK  
 19 About to look optional video ROM  
 1A Optional video ROM control OK  
 1B Display memory read/write test OK  
 1C Display memory read/write test for alternate display OK  
 1D Video retrace check OK  
 1E Global equipment byte set for video OK  
 1F Mode set callfor mono/color OK  
 20 Video test OK  
 21 Video display OK  
 22 Power on message display OK  
 30 Virtual mode memory test about to begin  
 31 Virtual mode memory test started  
 32 Processor in virtual mode  
 33 Memory address line test in progress  
 34 Memory address line test in progress  
 35 Memory below 1 MB calculated  
 36 Memory size computation OK  
 37 Memory test in progress  
 38 Memory initialization below 1 MB over  
 39 Memory initialization over 1 MB over  
 3A Display memory size  
 3B About to start below 1 MB memory test  
 3C Memory test below 1 MB OK  
 3D Memory test above 1 MB OK  
 3E About to go to real mode (Shutdown)  
 3F Shutdown successful and entered in real mode  
 40 About to disable Gate A20 address line  
 41 Gate A20 line disabled successfully  
 42 About to start DMA controller test  
 4E Address line test OK  
 4F Processor in real mode after shutdown  
 50 DMA page register test OK  
 51 DMA unit 1 base register test about to started  
 52 DMA unit 1 channel OK, about to begin CH-2

53 DMA channel 2 base register test OK  
 54 About to test F/F latch for unit 1  
 55 F/F latch test for both units OK  
 56 DMA units 1 and 2 programs OK  
 57 8259 initialization over  
 58 8259 mask register check OK  
 59 Master 8259 mask register OK  
 5A About to check timer and keyboard interrupt level  
 5B Timer interrupt OK  
 5C About to test keyboard interrupt  
 5D Error... Timer/keyboard interrupt not in proper level  
 5E 8259 interrupt controller error  
 5F 8259 interrupt controller test OK  
 70 Start of keyboard test  
 71 Keyboard battery test OK  
 72 Keyboard test OK  
 73 Keyboard global data setup OK  
 74 Floppy setup about to begin  
 75 Floppy setup OK  
 76 Hard disk setup about to start  
 77 Hard disk setup OK  
 79 About to initialize timer data area  
 7A Verify CMOS battery power  
 7B CMOS battery verification done  
 7D About to analyze diagnostics memory test results  
 7E CMOS memory size update OK  
 7F About to check optional ROM at C000:0  
 80 Keyboard sensed to enable setup  
 81 Optional ROM control OK  
 82 Printer global data initialization OK  
 83 RS-232 global data initialization OK  
 84 80287 check/test OK  
 85 About to display soft error messages  
 86 About to give control to system ROM at E000:0  
 87 System ROM E000:0 check over  
 00 Control given to INT 19, boot loader

## Appendix C:

# Phoenix ROM BIOS

**Table 10. Phoenix ROM BIOS Fixed Drive Type**

The system BIOS supports two fixed drives. Each drive can be one of the types listed in the following table:

Drive Type	Cylinders	Heads	Write Precomp	Landing Zone	Sectors	Capacity (MB)
1	306	4	128	305	17	10
2	615	4	300	615	17	20
3	615	6	300	615	17	30
4	940	8	512	940	17	62
5	940	6	512	940	17	46
6	615	4	-1	615	17	20
7	462	8	256	511	17	30
8	733	5	-1	733	17	30
9	900	15	-1	901	17	112
10	820	3	-1	820	17	20
11	855	5	-1	855	17	35
12	855	7	-1	855	17	49
13	306	8	128	319	17	20
14	733	7	-1	733	17	56
16	612	4	0	663	17	20
17	977	5	300	977	17	42
18	977	7	-1	977	17	56
19	1024	7	512	1023	17	59
20	733	5	300	732	17	30
21	733	7	300	732	17	42
22	733	5	300	733	17	30
23	306	4	0	336	17	10
25	615	4	0	615	17	20
26	1024	4	-1	1023	17	34
27	1024	5	-1	1023	17	42
28	1024	8	-1	1023	17	68

29	512	8	256	512	17	34
30	615	2	615	615	17	10
31	989	5	0	989	17	41
32	1020	15	-1	1024	17	127
35	1024	9	1024	1024	17	76
36	1024	5	512	1024	17	42
37	830	10	-1	830	17	68
38	823	10	256	824	17	68
39	615	4	128	664	17	20
40	615	8	128	664	17	40
41	917	15	-1	918	17	114
42	1023	15	-1	1024	17	127
43	823	10	512	823	17	68
44	820	6	-1	820	17	40
45	1024	8	-1	1024	17	68
46	925	9	-1	925	17	69
47	699	7	256	700	17	40

**Table 11. Phoenix ROM BIOS Error Message Reference**

**Beep Codes**

**Description of Test or Failure**

--	80286 register test in progress
1-1-3	CMOS write/read test in progress or failure
1-1-4	BIOS ROM checksum in progress or failure
1-2-1	Programmable interval timer test in progress or failure
1-2-2	DMA initialization in progress or failure
1-2-3	DMA page register write/read test in progress or failure
1-3-1	RAM refresh verification in progress or failure
--	1st 64 KB RAM test in progress
1-3-3	1st 64 KB RAM chip or data line failure -- multi-bit
1-3-4	1st 64 KB RAM odd/even logic failure
1-4-1	1st 64 KB RAM address line failure
1-4-2	1st 64 KB RAM parity test in progress or failure
2-1-1	1st 64 KB RAM chip or data line failure -- bit 0
2-1-2	1st 64 KB RAM chip or data line failure -- bit 1
2-1-3	1st 64 KB RAM chip or data line failure -- bit 2
2-1-4	1st 64 KB RAM chip or data line failure -- bit 3
2-2-1	1st 64 KB RAM chip or data line failure -- bit 4
2-2-2	1st 64 KB RAM chip or data line failure -- bit 5
2-2-3	1st 64 KB RAM chip or data line failure -- bit 6

2-2-4	1st 64 KB RAM chip or data line failure -- bit 7
2-3-1	1st 64 KB RAM chip or data line failure -- bit 8
2-3-2	1st 64 KB RAM chip or data line failure -- bit 9
2-3-3	1st 64 KB RAM chip or data line failure -- bit A
2-3-4	1st 64 KB RAM chip or data line failure -- bit B
2-4-1	1st 64 KB RAM chip or data line failure -- bit C
2-4-2	1st 64 KB RAM chip or data line failure -- bit D
2-4-3	1st 64 KB RAM chip or data line failure -- bit E
2-4-4	1st 64 KB RAM chip or data line failure -- bit F

3-1-1	Slave DMA register test in progress or failure
3-1-2	Master DMA register test in progress or failure
3-1-3	Master interrupt mask register test in progress or failure
3-1-4	Slave interrupt mask register test in progress or failure
--	Interrupt vector loading in progress
3-2-4	Keyboard controller test in progress or failure
--	CMOS power-failure and checksum checks in progress
--	CMOS configure information validation in progress
3-3-4	Screen memory test in progress or failure
3-4-1	Screen initialization in progress or failure
3-4-2	Screen retrace tests in progress or failure
--	Search for video ROM in progress
--	Screen believed operable: screen believed running w/ video ROM
--	monochrome screen believed operable
--	40-column color screen believed operable
--	80-column color screen believed operable
4-2-1	Timer tick interrupt test in progress or failure
4-2-2	Shutdown test in progress or failure
4-2-3	Gate A20 failure
4-2-4	Unexpected interrupt in protected mode
4-3-1	RAM test in progress or failure above address 0FFFFh
4-3-3	Interval timer channel 2 test in progress or failure
4-3-4	Time-of-day clock test in progress or failure
4-4-1	Serial port test in progress or failure
4-4-2	Parallel port test in progress or failure
4-4-3	Math coprocessor test in progress or failure

## Appendix D:

### Glossary

**adapter card** -- a printed circuit card that gives your computer some added capability, such as more memory or control of a new device. A card plugs into an expansion slot on the system board.

**benchmark** -- a program used to test and evaluate the performance characteristics of different systems.

**BIOS** -- Basic Input/Output System. Programs that are permanently stored in the system board's ROM chips providing functions such as the Power-On Self Test. See also ROM.

**card** -- See "adapter card."

**central processing unit** -- An integrated circuit chip that performs the actual computing functions of the computer. Other chips in a computer perform support functions like storing data and controlling peripherals.

**chip** -- See "integrated circuit."

**CMOS RAM** -- Complementary metal oxide semiconductor. A logic circuit family that uses very little power. It works with a wide variety of power supply voltages.

**configuration** -- The way in which a computer and peripheral equipment (such as printers and display monitors) are interconnected and programmed to operate as a system.

**coprocessor** -- A microprocessor device connected to a central microprocessor that performs specialized computations (such as floating-point arithmetic) much more efficiently than the CPU alone.

**CPU** -- See "central processing unit."

**device** -- A computer hardware accessory that is used for input or output, such as a disk drive, printer, or keyboard.

**direct memory addressing** -- A method for transferring data directly to and from main memory, bypassing the CPU.

**disk-cache** -- A software utility that reduces floppy and hard disk access, thus speeding operation. A disk-cache stores data in memory that is repeatedly read from or written to disk.

**DMA** -- See "direct memory addressing."

**EMS** -- a functional definition of a bank-switched memory-expansion subsystem made up of hardware expansion modules and a user-installable resident driver program specific for those modules.

**ESDI** -- Enhanced Storage Device Interface.

**expanded memory specification (EMS)** -- A bank-switched memory expansion subsystem made up of hardware expansion modules and a resident driver program.

**expansion slot** -- A connector on the system board for holding an adapter card.

**hertz (hz)** -- A unit of frequency equal to one cycle per second.

**I/O** -- An abbreviation for "input/output," the two basic operations that a computer performs on its peripherals.

**interface** -- A device that alters or converts actual electrical signals between distinct devices, programs, or systems.

**integrated circuit** -- An electronic device that combines thousands of transistors on a small sliver, or chip, of silicon. Such devices are the building blocks of computers.

**interleaving** -- A technique for improving the performance of computer memories. Successive memory locations are assigned to different banks, cycling through the available banks.

**jumper** -- On a printed circuit board, a patch cable or wire used to establish a circuit.

**memory** -- Another name for computer storage. See also "RAM" and "ROM."

**microprocessor** -- See "central processing unit."

**MIPS** -- Million instructions per second.

**multitasking** -- The concurrent execution of two or more tasks, typically applications, by a computer; may also be the concurrent execution of a single program that is used by many tasks.

**open circuit** – A discontinuous circuit; that is, one that is broken at one or more points and, consequently, cannot conduct current.

**page** -- A set of consecutive bytes. Pages begin on 4KB boundaries. Pages divide programs into multiple uniform-sized pages that have no direct relationship to the logical structure of a program.

**parameter** -- A variable that is given value for a specific program. A definable characteristic of an item, device, or system.

**parity bit** -- An additional noninformation bit appended to a group of bits to make the number of ones in the group of bits either an odd or even number; a basic and elementary mechanism for error checking.

**peripheral** -- A device that a computer uses to transfer information back and forth between itself and the user. Some examples of peripherals are the display monitor, disk drives, and printer.

**Power-On Self Test (POST)** -- Check-out procedures that the computer runs automatically when it is turned on. These procedures verify that all the computer's hardware is functioning properly. If the test detects problems, the computer displays error codes before (or instead of) starting the operating system. The error codes can help a service person determine what is wrong with your computer.

**RAM** -- An acronym for "random-access memory." The type of computer memory that can be used to store information while a program is running. All data stored in RAM is lost when the computer is turned off or power is

lost. RAM is stored in a number of small integrated circuits that are plugged into the system board.

**ROM** -- An acronym for "read-only memory." The type of computer memory that is used to permanently store the information vital to computer operation, including some parts of the operating system. ROM is permanent and the contents will not be lost when the computer is turned off.

**SCSI** -- Small Computer System Interface.

**setup** – The arrangement of connections between an assembly of individual computing units, and the adjustments needed for the computer to operate.

**shadow RAM** -- a method of copying BIOS routines in slower ROM chips to much faster RAM, increasing system performance speed.

**virtual memory** -- a technique for running programs that are larger than the available physical memory. Pieces of the program are stored on disk and are moved into memory only as necessary. This movement is automatically performed by the operating system and is invisible to the program.

**wait state** -- A delay in the computer's information processing cycle caused by a difference in speed between a faster processor and slower memory, which holds data. A zero wait state means the processor does not have to "wait" for memory, and can access data as fast as it is needed.

**write precompensation** – The varying of the timing of the head current from the outer tracks to the inner tracks of the disk to keep a constant 'write' signal.