

RADIO FREQUENCY INTERFERENCE STATEMENT

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference with radio and television reception.

If this equipment does cause interference to radio or TV reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- * Reorient the receiving antenna.*
- * Relocate the computer away from the receiver.*
- * Move the computer away from the receiver.*
- * Plug the computer into a different outlet so that computer and receiver are on different branch circuits.*
- * Ensure that card slot covers are in place when no card is installed.*
- * Ensure that card mounting screws, attachment connector screws, and ground wires are tightly secured.*
- * If peripherals are used with this system, it is suggested to use shielded, grounded cables, with in-line filters if necessary.*

If necessary, the user should consult the dealer service representative for additional suggestions.

The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications to this equipment. It is the responsibility of the user to correct such interference.

NOTE

1. *When you see an error message appear on the screen after turning the power on, leave the system switched on for one or two hours to recharge the battery. You can then enter the system configuration.*
2. *Leave your system switched on for 10 to 15 hours to completely recharge the battery.*
3. *If you had left the system switched off for more than one month, follow step 2, above.*

VERSION : 1.1

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SECTION 1 GENERAL FEATURES

The Fox-M286 system board is high performance system board that represents a significant technological advance over the original 80286 designs. It offers an increased power and flexibility architecture by supporting 80286 processor speeds up to 16 MHz^(). This manual is designed to provide the basic information necessary for the end user to understand the Fox-M286 system board.*

The Fox-M286 system board is designed for the most advanced computer-based applications for today and in the future. The Fox-M286 system provides a highly integrated approach to implement a very flexible system based on the PC/AT and the 80286 CPU. Key features of the board are summarized below:

1.1 PROCESSOR AND SYSTEM

- * *16 bit 80286 CPU*
- * *Optional 80287 numeric coprocessor*
- * *6/12 MHz system speed hardware/software switchable*
- * *I/O wait state hardware selectable*
- * *On board battery backup for CMOS configuration table and real-time clock*
- * *On board power good test circuit*

(*) Note :

Fox-M286 is available in two models :
- Fox M286-16
- Fox M286-12

Specifications are the same for the two models except that

FOX M286-16 operates much faster, up to 16MHz at turbo mode and 8MHz at normal mode.

1.2 MEMORY SUBSYSTEM ⁽¹⁾

*** Memory Capacity:**

*1MB using 256K X 4 DRAM chips
4MB using 1M SIMM DRAM chips*

*** Memory Configuration:**

*256KB/0KB
512KB/0KB
640KB/0KB
640KB/384KB
640KB/1408KB
640KB/3456KB*

*** Parity bit can either be enabled or disabled**

*** ROM Capacity:**

256K EPROM BIOS space for custom BIOS applications

*NOTE (1) : FOX-M286 system board is available in two models :-
Options for without installation of SIMM Memory that only support
44256K DIPs on board memory configuration.*

1.3 I/O SUBSYSTEM

*** 6 expansion slots**

- 4 with AT card-edge socket
- 2 with XT card-edge socket

*** Additional Features**

**** Hardware control support**

- Keylock
- Reset
- Turbo LED
- Power LED
- Speaker
- Wait State
- External Battery
- Turbo Switch

**** System support function:**

- 7-Channel Direct Memory Access
- 16-level interrupt
- Three programmable timers
- System clock

SECTION 2 INTRODUCTION

The design of cost effective IBM PC/AT compatible microcomputer requires taking advantage of every possible advanced technology. Cost effectiveness usually can be achieved in utilizing the least expensive parts available and the lowest counts of the required parts. The Fox-M286 is designed with top performance and flexibility in mind. It is a fully PC/AT compatible system board implemented with the high integration G2 AT chip set which supports the 80286 CPU at clock speeds up to 16 MHz and zero wait state performance.

One main advantage of this design includes the dual clock system. This innovation makes it possible for your computer to operate at either of two clock speeds: 8 MHz or 16 MHz. In the 16 MHz zero wait-state mode, your computer will operate much faster than a conventional 80286-based computer.

The board also features zero wait-state DRAM accesses in a design which supports Four MByte of DRAMs on the system board. This allows higher system performance relative to older PC-AT designs. And by selection of switch setting, you can configure the RAM for the one-wait/zero-wait option. This flexibility in configuration allows you to select an ideal cost/performance combination.

It also provides on-board powergood source. The on-board powergood generator provides a 'powergood' signal to indicate proper operation of the power supply. It allows you to use XT grade power supply which does not provide the circuitry to generate the power good signal.

The Fox-M286 system is hardware and software compatible with associated PC-AT products. This means that virtually all the hardware and software that is available for the PC/AT can also be run on a system you build around the Fox-M286 system board.

The Fox-M286 is fully software compatible with the IBM PC-AT design. The Fox-M286 is designed such that software is completely portable between the PC-AT to the Fox-M286. Note that "real-time" types of software programs could be the exception, as the higher operating speed of the Fox-M286 could cause execution or human interface problems.

The Fox-M286 supports MS-DOS Version 2.0 and above, Xenix and all PC/AT application programs. Users can run applications designed for the PC/AT on the Fox-M286 without any modification. Multi-tasking and multi-user capabilities are fully functional on the Fox-M286 system board.

In addition, the Fox-M286 provides standard expansion bus connectors so that add-on cards developed for the PC-AT will interface correctly.

The Fox-M286 features high performance, low power consumption, low board space requirements, reliability and low cost.

SECTION 3 SYSTEM BOARD SWITCH SETTING

The switches on the system board are shown in the figure below and on the following pages. These settings are used to specify the system board memory size and zero or one wait state operation.

Warning: Before you change any switch settings, make a note of how the switches are presently set.

<i>SWITCH</i>	<i>FUNCTION</i>
<i>1</i>	<i>Zero/One Wait State Function</i>
<i>2</i>	<i>256KB / 1M SIMM</i>
<i>3,4</i>	<i>RAM Size Selection</i>

3.1 SYSTEM BOARD SWITCH BLOCK LOCATION

The following figure shows where the switch block is on the system board.

Note: *The switch settings below are for example only.*

Change the switch settings by using the tip of a pen to gently pushing the switches into the correct position.

3.2 RAM CONFIGURATION AND INSTALLATION

The Fox-M286 supports 44256K DIPs or 1MB SIMM on-board memory configuration. Switch 1 selects zero-wait state or one-wait state operation. Switch 2 selects 256KB DIP or 1MB SIMM. Switch 3 & 4 are set to reflect the total amount of memory in your system. The Fox-M286 system board provides four 20-pins DIP sockets (for 44256 DRAMs) and four 38-pins dual sockets (for either 44256 or 4464 DRAMs) for 1 MB or 640 KB memory configuration. And also provides four SIMM socket for 2MB or 4MB memory configuration.

Memory can be installed/split as follows:

	256KB/0KB	(512KB installed)
44256K DIPs:	512KB/0KB	(512KB installed)
	640KB/0KB	(640KB installed)
	640KB/384KB	(1MB installed)
1M SIMM:	640KB/1408KB	(2MB installed)
	640KB/3456KB	(4MB installed)

Utilizing 44256K/1MB SIMM

System Memory Switch Setting RAM Location/Type

256KB	U27,U28,U33,U34-
44256	U21,U22(parity)-
41256	
512KB	U27,U28,U33,U34-
44256	U21,U22(parity)-
41256	
640KB	U27,U28,U33,U34-
44256	U21,U22(parity)-
41256	U25,U26,U31,U32-
4464	U19,U20(parity)-4164
640KB/384KB	U27,U28,U33,U34-
44256	U25,U26,U31,U32-
44256	U19,U20,U21,U22-
41256	(parity)
640KB/1408KB	SM1,SM2-411000

(W parity)

**640KB/3456KB
411000 (W parity)**

SM1,SM2,SM3,SM4-

U19, U20, U21 and U22 are the parity bits used for data checking. In normal situations, those bits are not needed. Hence, the user can left those sockets blank and thus allowing you to minimize the system cost.

(For more detail, please refer to the section on parity)

3.3 ONE-WAIT/ZERO-WAIT STATE SWITCH SETTING

What is Zero Wait State?

In a high performance PC/AT system based on the 80286 microprocessor running at its maximum bus transfer speed, only two system clock cycles would be required for any given byte (8-bit) or word (16-bit) transfer. The problem is that most subsystems cannot keep up with this pace, especially at system speeds exceeding 8 MHz. This implies the need for wait states during some accesses. Which means that the 80286 microprocessor has to wait in a do nothing loop until memory can respond to its needs for data. For this reason, the processor has to insert wait states. This is when the wait state comes in.

But the secret to high performance is to eliminate the wait states during the most frequent operations. The system board DRAM accesses are the most important target for no wait state performance. By far the most common memory or I/O cycle performed by the 80286 in an AT is a memory access to the DRAM on the system motherboard. These are important because most PC/AT applications spend over 90% of their time executing these types of cycles. Streamlining these cycles is the best way to achieve high performance in a PC/AT compatible system.

To achieve a true zero-wait state in the Fox-M286 system board, it has been designed such that memory subsystem is fast enough to respond to the CPU data, and thus memory bus cycle can be completed in just 2 cycles, eliminating the needs for wait states. This is what we refer to as zero wait state cycle.

Switch 1 is used to select the zero-wait state or one-wait state operation. Refer to the following figure for location of Switch 1 and the proper setting:

Zero-wait State

One-wait State

SECTION 4 SYSTEM BOARD JUMPER SELECTION

The mainboard jumpers allow the user to select the desired system configuration. The tables below shows the function and the default settings of these jumpers. Details of these jumpers will be discussed in the following sections.

<i>Jumper</i>	<i>Function</i>
<i>JP1</i>	<i>Parity enable/disable</i>
<i>JP2</i>	<i>BIOS ROM chip selection</i>
<i>JP3</i>	<i>Display adapter selection</i>
<i>JP4</i>	<i>DRAM speed selector</i>

<i>Default</i>	<i>Settings</i>
<i>JP1</i>	<i>Pin 2,3 short (parity check enable)</i>
<i>JP2</i>	<i>Pin 2,3 short (256K ROM BIOS)</i>
<i>JP3</i>	<i>Open (Monochrome)</i>
<i>JP4</i>	<i>Pin 2,3 short</i>

4.1 PARITY ENABLE/DISABLE

What is Parity?

Parity is a method for detecting errors in data communications. The parity bit is added at the end of a data word. The value of this bit is a function of the rest of the data word. There are several ways that the parity bit can be calculated.

"Even parity" means that the parity bit is set so that the sum of all the bits in the data word (including the parity bit) is even.

"Odd parity" is similar; the parity bit is set so that the sum of all the data bits in a word, including the parity bit, is an odd number.

"No parity" means that no parity bit is added to the end of a data word.

For the Fox-M286 System board, Memory Data Parity Check can either be enabled or disabled by altering the setting of jumper JP1.

When installing DIP type RAM chips; U19, U20, U21 and U22 are the DRAM chips for the parity bit. If data parity check is not desired, the sockets for U19, U20, U21 and U22 can be left blank; thus enabling the user to minimize the number of RAM chips installed for the system.

For 1MB memory configuration, 41256 RAM chips are used for parity bits.

For 640KB memory configuration, 41256 RAM chips are used for BANK 0 parity bits (U21 and U22); 4164 RAM chips are used for BANK 1 parity bits (U19 and U20).

Refer to the figure below for the location of jumper JP1, parity bits and the appropriate setting:

<i>JP1 Setting</i>	<i>Parity Check</i>
<i>1-2</i>	<i>Disable</i>
<i>2-3</i>	<i>Enable</i>

* For 1MB SIMM memory, the parity check setting to enable

4.2 ROM CONFIGURATION AND INSTALLATION

The Fox-M286 contains sockets for two BIOS EPROMs that can either be 27128 or 27256. Setting of jumper JP2 determines the ROM size and the type of ROM being used in the system board. Installation of the chips is explained in the table below. No matter what BIOS is used, the low-byte chip should be inserted in socket U5 and the high-byte chip should be inserted in socket U6.

<i>JP2</i>	<i>Type of</i>	<i>ROM chip</i>	<i>installation</i>
<i>Setting</i>	<i>BIOS</i>	<i>U5</i>	<i>U6</i>
<i>1-2</i>	<i>64KB size</i>	<i>27256</i>	<i>27256</i>
<i>2-3</i>	<i>32KB size</i>	<i>27128</i>	<i>27128</i>

4.3 DISPLAY ADAPTER SETTINGS

The Fox-M286 system can work with various display units if provided with a suitable display adapter. Jumper JP3 is used to signal the system what type of display adapter is installed. If you want to use two monitors (a color monitor and a high-resolution monochrome monitor, for example), set the adapter type to the monitor you want to use when the system boots. Refer to the figure below for the location of jumper JP3 and the appropriate setting:

<i>JP3 Settings</i>	<i>Adapter Type</i>
<i>ON</i>	<i>Color Graphics Adapter or Enhanced Graphics Adapter</i>
<i>OFF</i>	<i>Monochrome Adapter</i>

4.4 DRAM SPEED SELECTOR

The jumper JP4 allows the user to be able to use DRAM from different sources available in the market. This option is included in order to render superior tolerance to the wide range of DRAM's specifications. This will ensure the highest degree of compatibility performance with those various DRAMs' timing requirements.

The default setting for JP4 is pin 2,3 shorted. This setting should satisfy most DRAMs' timing requirements. In case system memory is not behaving reliably, try to alter JP4 setting to pin 1,2 to solve such problem.

Refer to the figure below for the default setting.

SECTION 5 SYSTEM BOARD CONNECTOR

This section describes with details of the hardware feature in the system board. You may find the information in this section useful. Under typical conditions, these connectors will have to connect to the indicator and switches of the system unit.

<i>Connector</i>	<i>Function</i>
<i>P1</i>	<i>Speaker Connector</i>
<i>P2</i>	<i>Hardware Reset Connector</i>
<i>P3</i>	<i>Turbo LED Connector</i>
<i>P4</i>	<i>Power LED and Ext-Lock Connector</i>
<i>P5</i>	<i>Turbo Switch Connector</i>
<i>P6,P7</i>	<i>Power Supply Connector</i>
<i>P8</i>	<i>External Battery Connector</i>
<i>KB1</i>	<i>Keyboard Connector</i>

Pin assignments are as follows:

5.1 P1 - Speaker Connector

The speaker connector is a 4-pin , keyed ,Berg strip. The pin assignment follow.

Pin	Assignments
1	Data out
2	+5 Vdc
3	Ground
4	+5 Vdc

5.2 P2 - Hardware Reset Connector

A reset will restart the computer from the **RAM** test stage. If you encounter any problem while using unfamiliar software, you can always restart from the beginning by pressing the restart button.

Pin	Assignments
1	Selection Pin
2	Ground

5.3 P3 - Turbo LED Connector

The turbo LED indicates operation in turbo mode (12MHZ). This is a 2-pin keyed, Berg strip (0.1") male pin connector.

<i>Pin</i>	<i>Assignments</i>
1	+5 Vdc
2	LED signal

5.4 P4 - Power LED and Ext-lock Connector

The power LED indicates whether the power is on. The keylock is used to enable or disable the keyboard. By disabling the keyboard, the user ensures that anyone who does not have a key will be unable to use the computer. Unlocking the keylock enables the keyboard.

The power LED and keylock connector is a 5-pin Berg strip. Its pin assignment are as follow:

<i>Pin</i>	<i>Assignments</i>
1	LED Power
2	Key
3	Ground
4	Keyboard inhibit
5	Ground

5.5 P5 - Turbo Switch Connector

The operating speed of the system board can be selected by the turbo switch setting. A speed switchover circuit ensures a smooth switchover between operating speeds, even during system operation. Also software selection via keyboard is allowed if appropriate BIOS is used.

Hardware Select Mode:

The turbo switch changes operation mode between 8MHz and 16MHz. This setting determines the speed at which the processor runs after booting. If you have a hardware switch on your case panel, connect it to jumper P5. You can push the hardware switch to enter either Normal mode or Software select mode. The pin assignment are as follows:

<i>Pin</i>	<i>Assignments</i>
<i>1</i>	<i>Select Pin</i>
<i>2</i>	<i>Ground</i>

Software Select Mode:

In addition to setting the processor clock speed by front-panel switch (Turbo switch), you can also change processor speed 'on-the-fly' via keyboard command. The Fox-M286 has speed switching circuitry allowing it to change speed during operation, even while you are running a program.

The system is default to run in high speed, but the operating mode can also be changed. You can toggle the operating speed between turbo mode and normal mode by pressing the following keystrokes simultaneously:

[Ctrl], [Alt], [+]
or [Ctrl], [Alt], [-]

The turbo LED light will light up to show whether your computer is now running in turbo mode or normal mode. When the Turbo LED is turned on, the system is in Turbo mode (16MHz). IF the Turbo is off, the system is in Normal mode (8MHz).

5.6 P6,P7 - Power Supply Connector

	<i>Pin</i>	<i>Assignments</i>
<i>P6:</i>	<i>1</i>	<i>Ground</i>
	<i>2</i>	<i>Ground</i>
	<i>3</i>	<i>-5 Vdc</i>
	<i>4</i>	<i>+5 Vdc</i>
	<i>5</i>	<i>+5 Vdc</i>
	<i>6</i>	<i>+5 Vdc</i>

	<i>Pin</i>	<i>Assignments</i>
<i>P7:</i>	<i>1</i>	<i>Power good</i>
	<i>2</i>	<i>+5 Vdc</i>
	<i>3</i>	<i>+12 Vdc</i>
	<i>4</i>	<i>-12 Vdc</i>
	<i>5</i>	<i>Ground</i>
	<i>6</i>	<i>Ground</i>

5.7 P8 - External Battery Connector

*This is for connecting four size "AA" batteries instead of the on-board battery to the **CMOS RAM**. This feature provides the same function as the on-board batteries.*

<i>Pin</i>	<i>Assignments</i>
1	6 Vdc
2	N/C
3	Ground
4	Ground

5.8 KB1 (DIN Connector) - Keyboard Connector

The keyboard connector is a five-pin DIN 90-degree printed circuit board (PCB) mounting. The pin assignments are as follows:

<i>Pin</i>	<i>Assignments</i>
1	Keyboard Clock
2	Keyboard Data
3	Spare
4	Ground
5	+5 Vdc

5.9 80287 Numeric Processor Installation

If you use certain application or programming languages, you may want to install a math co-processor to enhance the performance of your system. Be ware however, that your application program must be specifically designed to take advantage of the math co-processor to benefit from its presence in the system.

The 80287 Numeric Processor operates in conjunction with the 80286 CPU and will enhance the system's math capabilities. To install the 80287, simply insert the LSI chip into the empty socket (U7) below the power connector.

Important

Each pin on this LSI has a unique function. The 80287 should therefore be inserted into the socket in the correct direction. If it is inserted incorrectly, the LSI or the computer may be damaged. Install the LSI correctly by referring to the illustration. Care should be taken not

to bend and damage any of the pins. When inserting the LSI into the socket, apply force evenly over the LSI body.

SECTION 6 SYSTEM OPERATION

6.1 SYSTEM BIOS

All microcomputer systems use a Basic Input Output System (BIOS). This is software that has been permanently recorded in a ROM (Read Only Memory) chip and functions as the basic point of communication between the system board and the rest of the computer.

The BIOS provides an operational interface to the system and relieves the programmer from worrying about the characteristics of hardware devices. Thus, hardware modifications and enhancements become transparent to user's programs, access to BIOS is through the program interrupts of the 80286 microprocessor. Each BIOS entry point is available through its own interrupt.

6.2 POWER UP

Upon your turning on the power of your FOX-M286 system, the system will go through a self-test routine which checks all of its internal devices. Complete testings will be carried out on the CPU, base 640K RAM, extended RAM, ROM, system board, CMOS memory, video controllers, parallel and serial subsystems, floppy and fixed disk subsystems and the keyboard.

When the self-test is completed, the system will search for the DOS (disk operating system) system file in drive A. If no system diskette is put in drive A, it will check the fixed disk (if installed).

6.3 FIRST TIME STARTUP

If it is the first time that the computer is started up, you will need to configure the system by telling the SETUP program what hardware configuration your system contains.

6.4 CONFIGURING YOUR SYSTEM

The AMI BIOS, in addition to the BIOS program itself, contains a setup program that is called up everytime the system boots up. This is called the SETUP. The SETUP program lets you specify your system's configuration of diskette drives, hard disk drives, video display, memory, and date and time. The AMI BIOS provides a one-screen interactive equipment and machine configuration setup. The SETUP can be run after the system has been turned on and the memory test is finished or has been escaped. The SETUP program is built-in, you do not need a diskette to use it.

If your FOX-M286 is already installed in a working system, you will not need to use the SETUP program unless the configuration already recorded in the on-board CMOS RAM is lost or a change is made in your system hardware configuration. If the information is lost due to loss of battery power, you will need to reenter the configuration. If the configuration is altered, the changes must be recorded.

6.4.1 Memory Test Bypass

After the system is powered on or after a reset, the BIOS performs diagnostics of the system and displays the size of the memory being tested.

*Note that you can bypass the memory test by pressing the **<ESC>** key. This option would be useful when the memory on the system is quite large. You may hit the **<ESC>** key when the message following message appears on the screen:*

Press <ESC> Key to bypass MEMORY test

6.4.2 Running Setup

*Follow the instructions as they come up on the screen to complete the procedure. The initial prompt on the screen tells you to press the **** key if you want to use the setup program. It is displayed briefly just after the RAM test is run when you first turn on the system. If it disappears before you have a chance to respond turn the system off and on again or reset the system and the message will reappear. The initial screen prompt will be similar to:*

Press key if you want to run SETUP or DIAGS.

*Hit **** key to get into the Setup Mode. (Note that **** key will get you into the setup mode, only when the above message is displayed on the screen.)*

Upon your pressing of the **** key, the following message will appear on the screen :

EXIT FOR BOOT
RUN CMOS SETUP
RUN DIAGNOSTICS

Use **<Up>** and **<Down>** keys to highlight the selected item. Highlight **RUN CMOS SETUP** for the *SETUP* program and press the **<Return>** key to enter this option.

In a moment, the following SETUP menu will appear :

Once you have entered the *SETUP* menu, enter the date, time, the primary display type, the floppy drive installed and the hard disk drive type (if installed). See

Appendix 1 for a printed list of hard disk drive types.

The *SETUP* program will automatically determines your computer's memory configuration and displays it on the *SETUP* menu.

Use the **<Up>**, **<Down>**, **<Left>**, **<Right>**, and **<Return>** keys to move between options. The field shown in reverse video is the current field, which is the one the user may changes. Then use **<Pg Up>** and **<Pg Dn>** keys to select the correct values.

After you have entered the correct values to all of the *SETUP* options, you may now exit the *SETUP* program. To do so, press **<ESC>** key to exit. The following message will then appear :

Write data into CMOS and exit (Y/N)?

Press **Y** to update the data and exit the *SETUP* program.

The computer now performs a cold boot (equivalent to turning the power off and back on again), performs the memory test, and then tries to boot from the disk drive. If your hard disk has not yet been initialized, be sure that you have a bootable DOS diskette in the A drive.

6.5 RUNNING AMI BIOS DIAGNOSTICS

Following the above procedures until the following display is shown on the screen :

EXIT FOR BOOT
RUN CMOS SETUP
RUN DIAGNOSTICS

*Use the <Up> & <Down> to move the highlight bar to select "**RUN DIAGNOSTICS**" and then press <Enter>. The following screen will then appear :*

The AMI Utilities include services for the hard disk, floppy, keyboard, video and miscellaneous. It provides an easy to operate screen-menu allowing inexperienced users to operate the program. Simply press **<Left>** or **<Right>** and **<Up>** or **<Down>** keys to move the highlight bar the option desired.

SECTION 7 TECHNICAL INFORMATION

This section provides the technical materials about the FOX-M286 system board. The information in this section is for reference, and is intended for advanced readers who needs to understand the basic design and operation of the FOX-M286 system.

7.1 GC101/GC102 AT CHIP SET

The GC101 Peripheral Controller is the heart of the three chip system and forms most of the control circuits and "glue" logic of the AT architecture in a single CMOS VLSI chip.

The GC101 performs CPU and peripheral support functions including the following:

- * All Peripheral Devices and Refresh Counters*
- * All mega functions*
 - 82284 Clock Generator*
 - 82288 Bus Controller*
 - 8254 Timer*
 - 8259 Interrupt Controller (2)*
 - 8237 DMA Controller*

The GC102 may be configured as either an Address Buffer or Data Buffer by strapping one pin high or low. This chip replaces address buffer, data transceivers, memory drivers, parity generators and supporting circuitry.

GC102 Data Buffer provides:

- * Buffers and latches data for the CPU expansion bus and memory*
- * Parity bit generation and checking*
- * Slew rate controlled outputs*

GC102 Address Buffer provides:

- * Address buffering for expansion bus, local I/O bus and DRAM address bus.*
- * 10 bit DRAM address bus*

7.2 FOX-M286 SYSTEM BLOCK DIAGRAM

7.3 MICROPROCESSOR

The 80286 is a high-performance microprocessor with a 16-bit external data path, up to 16 megabytes of directly addressable physical memory and up to one gigabyte of virtual memory space. The operating speed of the 80286 chip is 8 MHz in Normal mode and 16 MHz in Turbo mode.

The 80286 operates in two modes: protected virtual address and real address.

Virtual address mode

The virtual address mode provides a 1-gigabyte virtual address space mapped onto a 16 megabyte physical address space. Virtual address space is larger than physical address space, and the use of a virtual address that does not map to a physical address location will cause a restartable interrupt.

This mode uses 32-bit pointers that consist of a 16-bit selector and offset components. The selector specifies an index into a memory-resident table, and the 24 bit base address of the desired segment is obtained from the memory table. A 16-bit offset is added to the segment base address to form the physical address. The microprocessor automatically references the tables whenever a segment register is loaded with a selector. Instructions that load a segment register will refer to the memory-based tables without additional program support. The memory-based tables contain 8-byte values called descriptors.

Real address mode

In this mode, physical memory is a contiguous array of up to 1 megabyte. The selector portion of the pointer is interpreted as the upper 16 bits of a 20-bit address, and the remaining 4 bits are set to zero. This mode of operation is compatible with the 8088 and 8086.

Segments in this mode are 64KB in size and may be read, written or executed. An interrupt may occur if data operands or instructions attempt to wrap around the end of a segment. In this mode, the information contained in the segment does not use the full 64KB, and the unused end of the segment may be overlay by another segment to reduce physical memory requirements.

7.4 SYSTEM MEMORY MAP

<i>Address</i>	<i>Range</i>	<i>Function</i>
<i>000000-7FFFFFFF</i>	<i>000K-512K</i>	<i>System Board Memory (512K)</i>
<i>080000-09FFFF</i>	<i>512K-640K</i>	<i>System Board Memory (128K)</i>
<i>0A0000-0BFFFF</i>	<i>640K-768K</i>	<i>Display Buffer (128K)</i>
<i>0C0000-0DFFFF</i>	<i>768K-896K</i>	<i>Adaptor ROM (128K)</i>
<i>0E0000-0EFFFF</i>	<i>896K-960K</i>	<i>System ROM (64K)</i>
<i>0F0000-0FFFFFFF</i>	<i>960K-1024K</i>	<i>System BIOS ROM (64K)</i>
<i>100000-7FFFFFFF</i>	<i>1024K-8192K</i>	<i>System Memory</i>

7.5 I/O ADDRESS MAP

I/O Address Map on System Board

I/O address hex 000 to 0FF are reserved for the system board I/O.

<i>ADDRESS (HEX)</i>	<i>DEVICE</i>
<i>000-01F</i>	<i>DMA Controller 1, 8237</i>
<i>020-03F</i>	<i>Interrupt Controller 1, 8259, Master</i>
<i>040-05F</i>	<i>Timer, 8254</i>
<i>060-06F</i>	<i>Keyboard Controller</i>
<i>070-07F</i>	<i>Real Time Clock, NMI (non-maskable interrupt) mask</i>
<i>080-09F</i>	<i>DMA Page Register, 74LS612</i>
<i>0A0-0BF</i>	<i>Interrupt Controller 2, 8259</i>
<i>0C0-0DF</i>	<i>DMA Controller 2, 8237</i>
<i>0F0</i>	<i>Clear Math Coprocessor 80287 Busy</i>
<i>0F1</i>	<i>Reset Math Coprocessor 80287</i>
<i>0F8-0FF</i>	<i>Math Coprocessor 80287</i>

I/O Address Map on the I/O slots

I/O address hex 100 to 3FF are available on the I/O channel.

<i>ADDRESS (HEX)</i>	<i>DEVICE</i>
<i>1F0-1F8</i>	<i>Fixed Disk</i>
<i>200-207</i>	<i>Game I/O</i>
<i>278-27F</i>	<i>Parallel Printer Port 2</i>
<i>2F8-2FF</i>	<i>Serial Port 2</i>
<i>300-31F</i>	<i>Prototype Card</i>
<i>360-36F</i>	<i>Reserved</i>
<i>378-37F</i>	<i>Parallel Printer Port 1</i>
<i>380-38F</i>	<i>SDLC, bisynchronous 2</i>
<i>3A0-3AF</i>	<i>Bisynchronous 1</i>
<i>3B0-3BF</i>	<i>Monochrome Display and Printer Adapter</i>
<i>3C0-3CF</i>	<i>Reserved</i>
<i>3D0-3DF</i>	<i>Color Graphics Monitor Adapter</i>
<i>3F0-3F7</i>	<i>Diskette Controller</i>
<i>3F8-3FF</i>	<i>Serial Port 1</i>

7.6 SYSTEM TIMERS

The system has three programmable timer/counters controlled by the timer/counter from the GC101 chip set and are defined as channels 0 through 2 :

<i>Channel 0</i>	<i>System Timer</i>
<i>Gate 0</i>	<i>Tied on</i>
<i>Clk in 0</i>	<i>1.190 MHz OSC</i>
<i>Clk out 0</i>	<i>8259 IRQ 0</i>

<i>Channel 1</i>	<i>Refresh Request Generator</i>
<i>Gate 1</i>	<i>Tied on</i>
<i>Clk in 1</i>	<i>1.190 MHz OSC</i>
<i>Clk out 1</i>	<i>Request Refresh Cycle</i>

Note: Channel 1 is programmed to generate a 15-micro-second period signal.

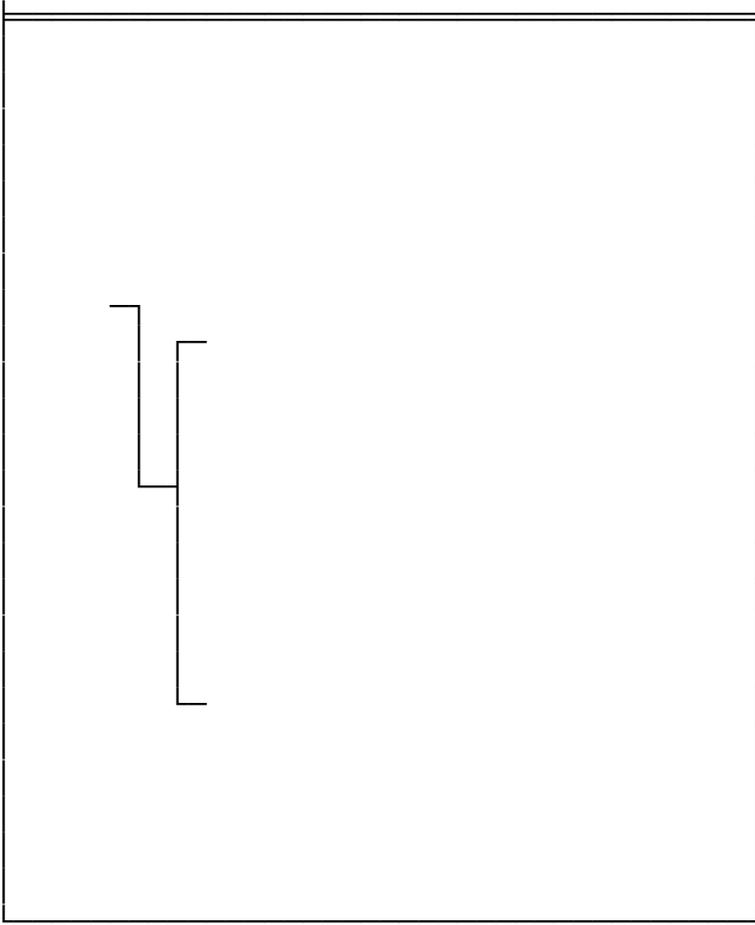
<i>Channel 2</i>	<i>Tone Generation of Speaker</i>
<i>Gate 2</i>	<i>Controlled by bit 0 of port hex 61 PPI bit</i>
<i>Clk in 2</i>	<i>1.190 MHz OSC</i>
<i>Clk out 2</i>	<i>Used to drive the speaker</i>

The 8254 Timer/Counter is treated by system programs as an arrangement of four programmable external I/O ports. Three are treated as counters, the fourth is a control register for mode programming.

7.7 SYSTEM INTERRUPTS

Sixteen levels of system interrupts are provided by the 80286 NMI and two 8259 Interrupt Controller within the GC101 chip set. The following shows the interrupt-level assignments in decreasing priority.

Level		Function
Microprocessor NMI		Parity or I/O Channel Check
Interrupt Controllers		
CTLR 1	CTLR 2	
IRQ0		Timer Output 0
IRQ1		Keyboard (Output Buffer Full)
IRQ2		Interrupt from CTLR 2
	IRQ8	Realtime Clock Interrupt
	IRQ9	Software Redirected to INT 0AH (IRQ2)
	IRQ10	Reserved
	IRQ11	Reserved
	IRQ12	Reserved
	IRQ13	Coprocessor
	IRQ14	Fixed Disk Controller
	IRQ15	Reserved
IRQ3		Serial Port 2
IRQ4		Serial Port 1
IRQ5		Parallel Port 2
IRQ6		Diskette Controller
IRQ7		Parallel Port 1



7.8 DIRECT MEMORY ACCESS (DMA)

The system supports seven DMA channels. Two DMA Controller are included in the GC101, with four channels for each chip. The DMA channels are assigned as follows:

<i>Channel</i>	<i>Function</i>
0	<i>Spare (8 bit transfer)</i>
1	<i>SDLC (8 bit transfer)</i>
2	<i>Floppy Disk (8 bit transfer)</i>
3	<i>Spare (8 bit transfer)</i>
4	<i>Cascade for DMA Controller 1</i>
5	<i>Spare (16 bit transfer)</i>
6	<i>Spare (16 bit transfer)</i>
7	<i>Spare (16 bit transfer)</i>

The following shows the addresses for the page register.

<i>Page Register</i>	<i>I/O Address (HEX)</i>
<i>DMA Channel 0</i>	<i>0087</i>
<i>DMA Channel 1</i>	<i>0083</i>
<i>DMA Channel 2</i>	<i>0081</i>
<i>DMA Channel 3</i>	<i>0082</i>
<i>DMA Channel 5</i>	<i>008B</i>
<i>DMA Channel 6</i>	<i>0089</i>
<i>DMA Channel 7</i>	<i>008A</i>
<i>Refresh</i>	<i>008F</i>

7.9 REAL TIME CLOCK AND CMOS RAM

The CMOS RAM Chip (146818) contains the real-time clock and 64 bytes of CMOS RAM, it keeps configuration information when power is off. Upon you turn the system power on, CMOS will load the recorded configuration into the system so that the system can function in the right track with the equipped components. However, if you haven't configured the CMOS, or the battery which supports the power to the CMOS is weaken, you need to redefine the necessary parameters whenever the system is booting up.

The program of the CMOS setting will be loaded into the system automatically from the sub-system named BIOS. The following table shows the CMOS RAM addresses.

CMOS RAM Address Map

<i>Addresses</i>	<i>Description</i>
<i>00-0D</i>	<i>* Real-time clock information</i>
<i>0E</i>	<i>* Diagnostic status byte</i>
<i>0F</i>	<i>* Shutdown status byte</i>
<i>10</i>	<i>Diskette drive type byte - drives A and B</i>
<i>11</i>	<i>Reserved</i>
<i>12</i>	<i>Fixed disk type byte - drives C and D</i>
<i>13</i>	<i>Reserved</i>
<i>14</i>	<i>Equipment byte</i>
<i>15</i>	<i>Low base memory byte</i>
<i>16</i>	<i>High base memory byte</i>
<i>17</i>	<i>Low expansion memory byte</i>
<i>18</i>	<i>High expansion memory byte</i>
<i>19-2D</i>	<i>Reserved</i>
<i>2E-2F</i>	<i>2-byte CMOS checksum</i>
<i>30</i>	<i>* Low expansion memory byte</i>
<i>31</i>	<i>* High expansion memory byte</i>
<i>32</i>	<i>* Date century byte</i>
<i>33</i>	<i>* Information flags (set during power on)</i>
<i>34-3F</i>	<i>Reserved</i>

** These bytes are not included in the checksum calculation and are not part of the configuration record.*

Real-time Clock Information

The following table describes real-time clock bytes and specifies their addresses.

Byte	Function	Address
0	Seconds	00
1	Second alarm	01
2	Minutes	02
3	Minute alarm	03
4	Hours	04
5	Hour alarm	05
6	Day of week	06
7	Date of month	07
8	Month	08
9	Year	09
10	Status Register A	0A
11	Status Register B	0B
12	Status Register C	0C
13	Status Register D	0D

Note: The setup program initializes registers A, B, C, and D when the time and date are set. Also Interrupt 1A is the BIOS's interface to read/set the time and date. It initializes the status bytes the same as the setup program.

7.10 MATH COPROCESSOR

The 80287 Math Coprocessor enables the FOX-M286 system to perform high-speed arithmetic, logarithmic functions, and trigonometric operations with extreme accuracy.

The coprocessor works in parallel with the microprocessor. The parallel operation decreases operating time by allowing the coprocessor to do mathematical calculations while the microprocessor continues to do other functions.

The Mathematics Coprocessor, 80287 is treated as an I/O device through I/O port address hex 0F8, 0FA and 0FC. The microprocessor sends OP codes and operands through these I/O ports. The microprocessor also receives and stores results through the same I/O ports. The "BUSY" signal generated by the coprocessor signifies to the microprocessor to wait until the coprocessor has finished executing.

The following describes the mathematics coprocessor control ports:

0F0 The latched Mathematics Coprocessor busy signal can be cleared with an 8-bit Out command, to port F0. The coprocessor will latch "BUSY", if it asserts its error signal. Data output should be zero.

0F1 The Mathematics Coprocessor will reset to real address mode which is in the 8087 compatible if an 8-bit Out command is sent to port F1. Again, the data output should be zero.

7.11 SYSTEM EXPANSION BUS

The FOX-M286 provides drive for up to six XT-compatible cards (four of which can be AT-compatible with the second connector)

The I/O channel supports:

- * I/O address space from hex 100 to hex 3FF*
- * Selection of data access (either 8 or 16 bit)*
- * 24 bit memory addresses (16MB)*
- * Interrupts*
- * DMA channels*
- * Refresh of system memory from channel microprocessors*

There are six 62-pin (JA1-JA6) and four 36-pin (JB1-JB4) edge connector sockets for I/O channel adapter cards. In two positions, the 36-pin connector is not present. These positions can support only 62-pin I/O bus adapters.

The following figure shows the pin numbering for I/O channel connectors JA1 to JA6.

*I/O Channel Pin Numbering
(62 Pin)*

The following figure shows the pin numbering for I/O channel connectors JB1-JB4.

*I/O Channel Pin Numbering
(36 Pin)*

The following table summarizes pin assignments for the I/O channel connectors.

I/O Channel (A-Side, JA1-JA6)

<i>I/O Pin</i>	<i>Signal Name</i>	<i>I/O</i>
A1	-I/O CH CK	I
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	-I/O CH RDY	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O

A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

I/O Channel (B-Side, JA1-JA6)

I/O Pin	Signal Name	I/O
B1	GND	Ground
B2	RESET DRV	I
B3	+5 Vdc	Power
B4	IRQ9	I
B5	-5 Vdc	Power
B6	DRQ2	I
B7	-12 Vdc	Power
B8	OWS	I
B9	+12 Vdc	Power
B10	GND	Ground
B11	-SMEMW	O
B12	-SMEMR	O
B13	-IOW	I/O
B14	-IOR	I/O
B15	-DACK3	I
B16	DRQ3	O
B17	-DACK1	I
B18	DRQ1	O
B19	-Refresh	I/O
B20	CLK	O

<i>B21</i>	<i>IRQ7</i>	<i>I</i>
<i>B22</i>	<i>IRQ6</i>	<i>I</i>
<i>B23</i>	<i>IRQ5</i>	<i>I</i>
<i>B24</i>	<i>IRQ4</i>	<i>I</i>
<i>B25</i>	<i>IRQ3</i>	<i>I</i>
<i>B26</i>	<i>-DACK2</i>	<i>O</i>
<i>B27</i>	<i>T/C</i>	<i>O</i>
<i>B28</i>	<i>BALE</i>	<i>O</i>
<i>B29</i>	<i>+5 Vdc</i>	<i>Power</i>
<i>B30</i>	<i>OSC</i>	<i>O</i>
<i>B31</i>	<i>GND</i>	<i>GROUND</i>

I/O Channel (C-Side JB1-JB4)

<i>I/O Pin</i>	<i>Signal Name</i>	<i>I/O</i>
<i>C1</i>	<i>SBHE</i>	<i>I/O</i>
<i>C2</i>	<i>LA23</i>	<i>I/O</i>
<i>C3</i>	<i>LA22</i>	<i>I/O</i>
<i>C4</i>	<i>LA21</i>	<i>I/O</i>
<i>C5</i>	<i>LA20</i>	<i>I/O</i>
<i>C6</i>	<i>LA19</i>	<i>I/O</i>
<i>C7</i>	<i>LA18</i>	<i>I/O</i>
<i>C8</i>	<i>LA17</i>	<i>I/O</i>
<i>C9</i>	<i>-MEMR</i>	<i>I/O</i>
<i>C10</i>	<i>-MEMW</i>	<i>I/O</i>
<i>C11</i>	<i>SD8</i>	<i>I/O</i>
<i>C12</i>	<i>SD9</i>	<i>I/O</i>
<i>C13</i>	<i>SD10</i>	<i>I/O</i>
<i>C14</i>	<i>SD11</i>	<i>I/O</i>
<i>C15</i>	<i>SD12</i>	<i>I/O</i>
<i>C16</i>	<i>SD13</i>	<i>I/O</i>
<i>C17</i>	<i>SD14</i>	<i>I/O</i>
<i>C18</i>	<i>SD15</i>	<i>I/O</i>

I/O Channel (D-Side JB1-JB4)

<i>I/O Pin</i>	<i>Signal Name</i>	<i>I/O</i>
<i>D1</i>	<i>-MEM CS16</i>	<i>I</i>
<i>D2</i>	<i>-I/O CS16</i>	<i>I</i>
<i>D3</i>	<i>IRQ10</i>	<i>I</i>
<i>D4</i>	<i>IRQ11</i>	<i>I</i>
<i>D5</i>	<i>IRQ12</i>	<i>I</i>
<i>D6</i>	<i>IRQ15</i>	<i>I</i>
<i>D7</i>	<i>IRQ14</i>	<i>I</i>
<i>D8</i>	<i>-DACK0</i>	<i>O</i>
<i>D9</i>	<i>DRQ0</i>	<i>I</i>
<i>D10</i>	<i>-DACK5</i>	<i>O</i>
<i>D11</i>	<i>DRQ5</i>	<i>I</i>
<i>D12</i>	<i>-DACK6</i>	<i>O</i>
<i>D13</i>	<i>DRQ6</i>	<i>I</i>
<i>D14</i>	<i>-DACK7</i>	<i>O</i>
<i>D15</i>	<i>DRQ7</i>	<i>I</i>
<i>D16</i>	<i>+5 Vdc</i>	<i>Power</i>
<i>D17</i>	<i>-MASTER</i>	<i>I</i>
<i>D18</i>	<i>GND</i>	<i>Ground</i>

APPENDIX

FOX-M286 SYSTEM BOARD LAYOUT

Hard Disk Drives supported by AMI BIOS

Type	Cylinders	Head	Write Precomp	Landing Zone	Capacity
1	306	4	128	305	10MB
2	615	4	300	615	21MB
3	615	6	300	615	31MB
4	940	8	512	940	64MB
5	940	6	512	940	48MB
6	615	4	None	615	21MB
7	462	8	256	511	31MB
8	733	5	None	733	31MB
9	900	15	None	901	115MB
10	820	3	None	802	21MB
11	855	5	None	855	36MB
12	855	7	None	855	51MB
13	306	8	128	319	21MB
14	733	7	None	733	44MB
15	<i>Reserved</i>				
16	612	4	All	663	21MB
17	997	5	300	997	42MB
18	997	7	None	997	58MB
19	1024	7	512	1023	61MB
20	733	5	300	977	31MB
21	733	7	300	732	42MB
22	733	5	300	733	31MB
23	306	4	All	336	10MB
24	925	7	All	925	56MB
25	925	9	None	925	72MB
26	754	7	754	754	46MB
27	754	11	None	754	72MB
28	699	7	256	699	46MB
29	923	10	None	823	71MB
30	918	7	918	918	55MB
31	1024	111	None	1024	98MB

A-

32	1024	15	None	1024	133MB
33	1024	5	1024	1024	44MB
34	624	2	128	612	10MB
35	1024	9	None	1024	80MB
36	1024	8	512	1024	71MB
37	615	8	128	615	42MB
38	987	3	987	987	25MB
39	987	7	987	987	60MB
40	820	6	820	820	42MB
41	977	5	977	977	42MB
42	981	5	981	981	42MB
43	830	7	512	830	50MB
44	830	10	None	830	72MB
45	917	15	None	918	115MB
46	1224	15	None	1223	152MB
47	USER TYPE				

A-

SUMMARY OF SYSTEM BOARD SETTINGS

<i>Switch 1</i>	<i>Function</i>
<i>ON</i>	<i>Zero wait state</i>
<i>OFF</i>	<i>One wait state</i>

<i>Switch 2</i>	<i>Function</i>
<i>ON</i>	<i>256KB DIPs</i>
<i>OFF</i>	<i>1M SIMM</i>

<i>Switch</i>	<i>Setting</i>		
<i>3</i>	<i>4</i>		<i>Memory configuration</i>
<i>Using 4</i>	<i>4256K/ 1M</i>	<i>SIMM:</i>	
<i>SW 2</i>	<i>SW 3</i>	<i>SW 4</i>	
<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>256KB / 0KB</i>
<i>ON</i>	<i>OFF</i>	<i>ON</i>	<i>512KB / 0KB</i>
<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>640KB / 0KB</i>
<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>640KB / 384KB</i>
<i>OFF</i>	<i>ON</i>	<i>OFF</i>	<i>640KB / 1408KB</i>
<i>OFF</i>	<i>OFF</i>	<i>OFF</i>	<i>640KB / 3456KB</i>

<i>Jumper</i>	<i>Pin</i>	<i>Function</i>
<i>JP1</i>	<i>1,2</i>	<i>Parity bit disable</i>
	<i>2,3</i>	<i>Parity bit enable</i>
<i>JP2</i>	<i>1,2</i>	<i>256K ROM BIOS</i>
	<i>2,3</i>	<i>128K ROM BIOS</i>
<i>JP3</i>	<i>short</i>	<i>CGA / EGA / VGA</i>
	<i>open</i>	<i>Monochrome</i>
<i>JP4</i>	<i>2,3 (default)</i>	<i>DRAM speed selector</i>

<i>Connector</i>	<i>Function</i>
<i>P1</i>	<i>Speaker Connector</i>
<i>P2</i>	<i>Hardware Reset Connector</i>
<i>P3</i>	<i>Turbo LED Connector</i>
<i>P4</i>	<i>Power LED & Ext-Lock Connector</i>
<i>P5</i>	<i>Turbo Switch Connector</i>
<i>P6, P7</i>	<i>Power Supply Connector</i>
<i>P8</i>	<i>External Battery Connector</i>
<i>KB1</i>	<i>Keyboard Connector</i>