80286-16/20/25

Mother Board User's Manual

DATE : SEPTEMBER, 1990

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PREFACE

1.1 INTRODUCTION

The **80286-16/20/25** motherboard is compatible with the **PC/AT**. This means that virtually all software that is available for the PC/AT can be used on the systems built around the **80286-16/20/25** mother board. The purpose of this manual is to offer you some information on how to configure your powerful **80286-16/20/25** mothe board. In addition, this manual will provide you with the standard specifications that you may need in order to set up a complete system. Please read through each chapter carefully, to ensure full utilization of the high performance benefit of this **80286-16/20/25**

***** NOTE :**

If you find the **80286-16/20/25** shows different performance when using different **DOS** version, or different **LANDMARK** or there are other resident programs in memory such as **EMS DRIVER, VIRTUAL DISK DRIVER** etc.. That is because different RAM configuration would make different **HIT-RATE** (HIT is accessing to same ROW ADDRESS) on **PAGE/INTERLEAVE MODE**. If HIT-RATE is high, then it will show high performance.

The solution is to append a command **buffers = XX** into **config.sys** to adjust the RAM assignment. Try the XX from **1 to 20.**

1.2 FEATURES

The general specification of **80286-16/20/25** are as follow :

- Harris 80C286-16/ 20/ 25 Microprocessor
- Optional 80287 Co-processor (speed selectable)
- 16/20/25MHZ , zero/one wait states
- Memory Options 512KB, 1MB, 2MB, 4MB (Module RAM)
- Supports Lotus-Intel-Microsoft EMS
- Hardware and Software speed switchable
- Keyboard attachment and security
- Speaker attachment
- 6 Expansion Slots -- 5 for 16 bits, 1 for 8 bits
- 7 channel direct memory access
- 16 level interrupts
- Clock Calendar with battery backup
- Chargeable battery on board
- Connector for external battery

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1.3 FIGURE 1-1

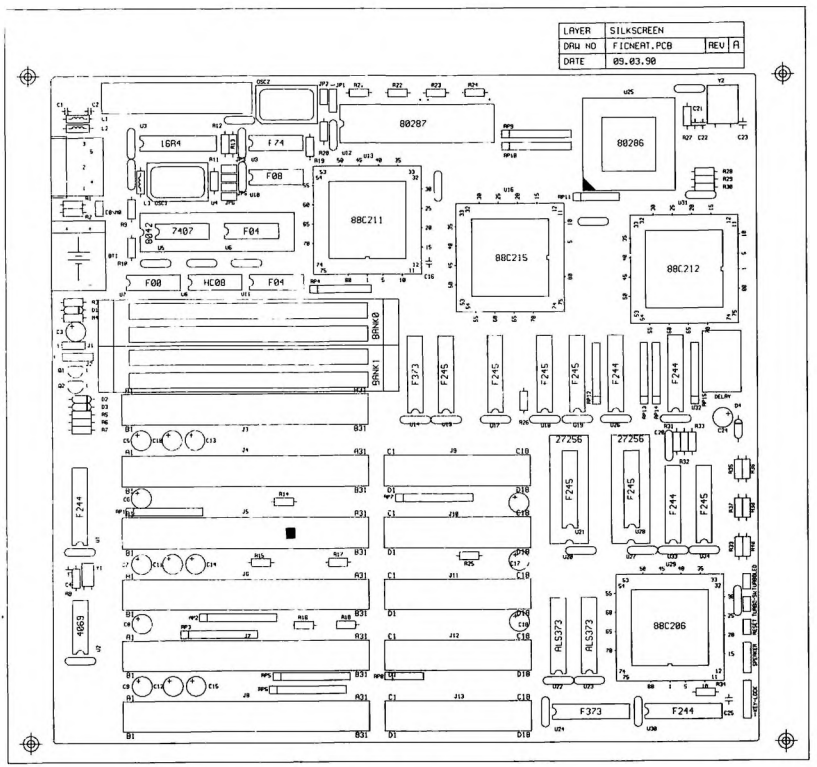
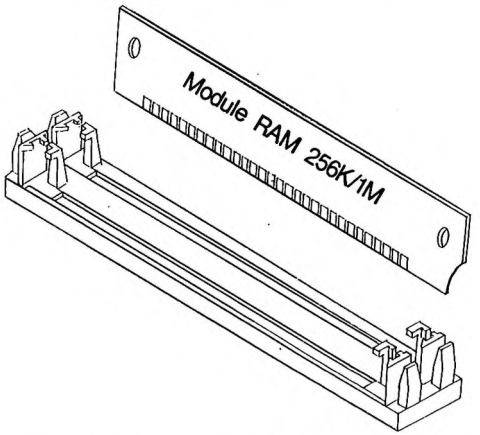


FIGURE 1-1

HARDWARE SPECIFICATION

2.1 MODULE RAM INSTALLATION

The **80286-16/20/25** can be upgraded to **4MB** on board so you can find 4 30-pins Module RAM sockets on board.
The figure below shows ways of Module RAM insertion.



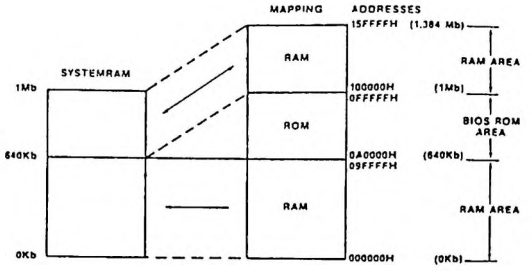
Following are the possible configurations for onboard memory:

Module RAM TYPE Bank0	Bank1	TOTAL MEMORY	Wait States
256K	0	512KB	1
1M	0	2MB	1
256K	256K	1MB	0
1M	1M	4MB	0

- **Memory Mapping:**

Through the memory mapping logic, for up to 1 Mbyte of system RAM, it is possible to map RAM that overlaps the EPROM area (640 Kbyte - 1 Mbyte) to above the 1 Mbyte area. Hence, for 1 Mbyte of on board RAM, the software can address it from 0 to 640 Kbytes and from 1 Mbyte to 1.384 Mbytes. The EPROM can be addressed from the 640 Kbyte area to the 1 Mbyte area.

For normal mode of operation, one bank of DRAM may be used. However, for the page/interleaved mode of operation, RAM bank pairs must be used.

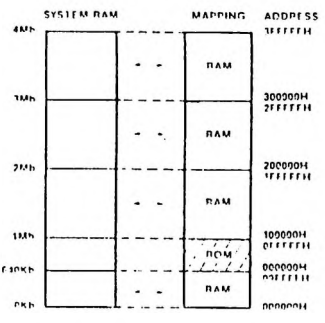


System RAM/ROM Mapping for 1MB System RAM

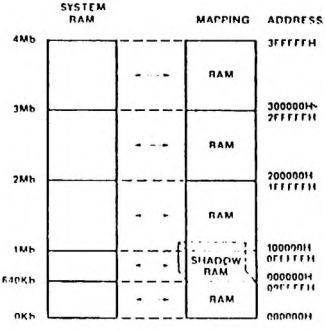
- **Shadow RAM feature:**

For efficient execution of BIOS, it is preferable to execute BIOS code through RAM rather than through slower EPROMs. The **SHADOW RAM** feature allows the BIOS code to be executed from system RAM resident at the same physical address as the BIOS EPROM. This feature significantly improves the performance in BIOS-call intensive application. Performance improvements as high as **300 to 400%** have been observed in **BENCHMARK** tests on the shadow RAM. The shadow RAM feature is invoked by enabling the corresponding bits in the ROM enable register and the RAM mapping register.

If more than 1 Mbyte of system RAM exists, you can enable a shadow RAM feature to overlap or shadow the EPROM area. For accesses beyond the 1 Mbyte address range, the processor is switched from real to protected mode from BIOS.



RAM ROM Mapping Without Shadow RAM (More Than 1MB of RAM)



RAM Mapping with Shadow RAM (More Than 1MB of RAM)

2.2 OPTIONAL PROCESSOR SPEED

For some applications that require slower operation (such as installing copy-protected software), this motherboard offers a "**slow-down**" mode which emulates **10MHZ** operation.

The power-on default speed is **20MHZ**. You can use the following two ways to change the processor speed :

- **Select by keyboard:**

  BIOS from "**PHOENIX SOFTWARE ASOCIATES LTD.**"

  Pressing : CTRL + ALT +"--" : Toggle HIGH speed or LOW speed

- **Select by turbo switch : TURBO — SW**

Normally TURBO-SW is connected to the speed selecting switch and LED on the front panel. Pressing the switch on the front panel will cause the speed toggle between Turbo mode and Emulated slow -down mode.

***** NOTE :**
"**TOGGLE**" means the speed will be changed from your current speed mode to another.
The pin layout of TURBO-SW

2.3 HARDWARE RESET :

Hard ware reset jumper used for connecting a push button. A close-open action on this jumper (or push and release of push-button) will cause a system reset through out the board.

JUMPER SETTING

3.1 MATH COPROCESSOR CLOCK SELECT : JP2

The **80286-16/20/25** include socket (U12) for installi an **80287**.

JP2 is used for frequency divide control. When close JP2 coprocessor works at **one-third** the frequency of the system clock. Open JP2 , coprocessor works at the same frequency as the system microprocessor clock.

Jumper	Description
ON	* Internal divide by 3
OFF	No divide (DEFAULT)

JP 1 is used for selecting clock source. Pins 1 & 2 shorted for choosing processor clock (40 MHZ for 20 MHZ system). Pins 2 & 3 shorted for choosing external oscillator that is installed in socket osc 2 . There is one **oscillator in osc** 2 on the board.

Jumper	Description
[1 2] 3	Processor clock
1 [2 3]	* External OSC. (DEFAULT)

The following table describes the relationship between the external oscillator clock speed (i.e. **JP1 is shorted in 2 & 3**) and the 80287 operating speed:

80287 SPEED	OSC 2 CLOCK	
6MHZ	24MHZ	
8MHZ	32MHZ	(DEFAULT)
10MHZ	40MHZ	

3.2 MONITOR TYPE OPTION : CO \ MO

When a **COLOR** monitor is used, **Co \ Mo** should be closed. If the system has a **MONOCHROME** or **EGA** monitor, please open in **Co \ Mo.**

CO/MO	Description
ON	Color Monitor
OFF	Mono Monitor

3.3 BATTERY SELECTER : J1

Normally we place a jumper cap over **J1** for battery charging enable. If you want to connect an external battery you will take the jumper cap off **J1** for battery charging disable.

J1	Description
[1 2] 3	**External** battery
1 [2 3]	**Internal** battery **(DEFAULT)**

3.4 BATTERY CONNECTOR : J2

You will notice that a **Ni-Cd battery** has been built in the main board, but there is also a mechanical switch (J2) which can be connected to an external battery.

Pin	Assignments
1	Battery (+6V)
2	NC
3	Ground
4	Ground

3.5 KEYLOCK & LED :

The keylock is used to enable or disable the key-board. Whenever the keyboard is disable, any operation on the keyboard will be void on your system.

KEYLOCK & LED can be connected with a keylock switch that is generally installed on the front panel.
Pin assignments of **KEYLOCK & LED** are shown as below

Pin	Assignments
1	POWER FOR LED
2	NC
3	Ground
4	Keylock Switch
5	Ground

» Please refer to the orientation shown in **FIGURE 1-1**

3.6 SPEAKER CONNECTOR :

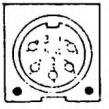
The following is the pin assignments of speaker , the speaker connector.

Pin	Assignments
1	Speaker signal
2	NC
3	Ground
4	+5 V

» Please refer to the orientation shown in **FIGURE 1-1**

3.7 KEYBOARD :

The keyboard connector is a 5-pin Din connector. The following is the pin assignments :

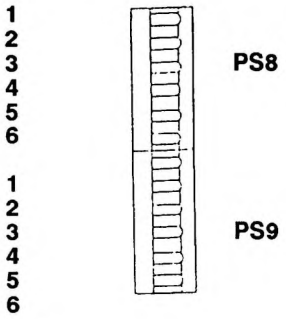


KEYBOARD PLUG

Pin	Assignments
1	KEYCLK
2	KEYDAT
3	SPARE
4	GROUND
5	+5V

» Pin-position please refer to orientation shown in **FIGURE 1-1**

3.8 POWER CONNECTOR : PS8& PS9



Pin	Assignments	Connector
1	Power good	
2	+5 V	
3	+12 V	
4	-12 V	PS8
5	Ground	
6	Ground	
1	Ground	
2	Ground	
3	-5 V	
4	+5 V	PS9
5	+5 V	
6	+5 V	

3.9 TURBO LED & SWITCH CONNECTOR :

It is recommended to slow down the speed of the system while running certain software packages. You may use the speed select switch on the front panel to change the speed. " **Light on**"corresponds to the normal speed mode, while " **Light off** " corresponds to the emulated slow-down speed mode. The speed connector for the **LED** is located at Turbo - LED.

The pin assignments are shown as below :

TURBO-SW	**Description**
ON	**Low speed**
OFF	**high speed**

HARDWARE COMPATIBILITY

4.1 THE NEAT CHIPSet

80286-16/20/25 incorporate the **CS822 NEAT CHIPSet** which consists of the **82C211 CPU/Bus controller**, the **82C212 Page/Interleave** and **EMS Memory controller**, the **82C215 Data/Address buffer** and the **82C206 integrated Peripherals Controller (IPC).**

The **82C211** provides synchronization and control signals for all buses. The 82C211 also provides an independent AT bus clock. Command delays and wait states are software configurable, providing flexibility for slow or fast peripheral boards.

The **82C212** Page/Interleave and EMS Memory controller provides an Interleaved memory sub-system design with page mode operation. It supports up to 4 MB of on-board DRAM with combinations of 256Kbit and 1Mbit DRAMs. The Shadow RAM feature allows faster execution of code stored in EPROM, by down loading code from EPROM to RAM. The RAM then sahdows the EPROM for further code execution. In a DOS environment, memory above 1Mb can be treated as LIM EMS memory.

The **82C215** Date/Address buffer provides the buffering and latching between the local CPU address bus and the Peripheral address bus. It also provides buffering between the local CPU data bus and the memory date bus. The parity bit generation and error detection logic resides in the 82C215.

The **82C206** Integrated Peripheral Controller Incorporates two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 Timer Counter, one 146818 Real Time Clock, 74LS612 Memory Mapper, in addition to serval other TTL/SSI interface logic chips to provide a single-chip integration of all the peripherals attached to the peripheral bus (X_Bus) in the IBM™ PC/AT™

4.2 SYSTEM TIMERS

The system has three programmable timer/counters controlled by **82C206** and defined as Channels 0 through 2 as follows:

CHANNEL 0	SYSTEM TIMER
GATE 0	Tied on
CLK IN 0	1.190 MHZ
CLK OUT 0	IRQ 0
CHANNEL 1	**REFRESH REQUEST GENERATOR**
GATE 1	Tied on
CLK IN 1	1.190 MHZ
CLK OUT 1	Request Refresh Cycle
CHANNEL 2	**TONE GENERATION FOR SPEAKER**
GATE 2	Controlled by bit 0 of port hex 61 PPI bit
CLK IN 2	1.190 MHZ
CLK OUT 2	Used to drive the speaker

***** NOTE :**

Channel 1 is programmed as a rate generator to produce a **15-microsecond** period signal.

4.3 SYSTEM INTERRUPTS

The **82C206** provides 16 levels of system interrupts. The following shows the interrupt-level assignments in decreasing priority.

LEVEL		FUNCTION
MicroProcessor NMI		Parity or I/O Channel Check
Interrupt CTLR 1	Controllers CTLR 2	
IRQ 0		Timer Output 0
IRQ 1		Keyboard (Output Buffer Full)
IRQ 2		Interrupt from CTLR 2
	IRQ 8	Real time Clock Interrupt
	IRQ 9	Software Redirected to INT 0AH (IRQ 2)
	IRQ 10	Reserved
	IRQ 11	Reserved
	IRQ 12	Reserved
	IRQ 13	Coprocessor
	IRQ 14	Fixed Disk Controller
	IRQ 15	Reserved
IRQ 3		Serial Port 2
IRQ 4		Serial Port 1
IRQ 5		Parallel Port 2
IRQ 6		Diskette Controller
IRQ 7		Parallel Port 1

***** NOTE :**

Any or all interrupts may be masked (including the microprocessor's NMI).

4.4 DIRECT MEMORY ACCESS (DMA)

The system supports seven DMA channels, provided by **82C206.** The DMA channels are assigned as follows:

DMA CHANNELS

CTLR 1		CTLR 2	
Ch 0	**- Spare**	**Ch 4**	**- Cascade for Ctlr 1**
Ch 1	**- SDLC**	**Ch 5**	**- Spare**
Ch 2	**- Diskette**	**Ch 6**	**- Spare**
Ch 3	**- Spare**	**Ch 7**	**- Spare**

DMA controller 1 contains channels 0 through 3. These channels support 8-bit data transfers between 8-bit I/O adapters and 8-bit or 16-bit system memory. Each channel can transfer date throughout the 16-megabyte system-address space in 64Kb blocks.

DMA controller 2 contains channels 4 through 7. Channel 4 is used to cascade channels 0 through 3 to the microprocessor. Channels 5, 6 and 7 support 16-bit data transfers between 16-bit I/O adapters and 16-bit system memory. These DMA channels can transefer data throughout the 16-mefgabyte system-address space in 128Kb blocks. channels 5, 6, and 7 cannot transfer data on odd byte boundaries.

4.5 I/O CHANNEL SLOTS

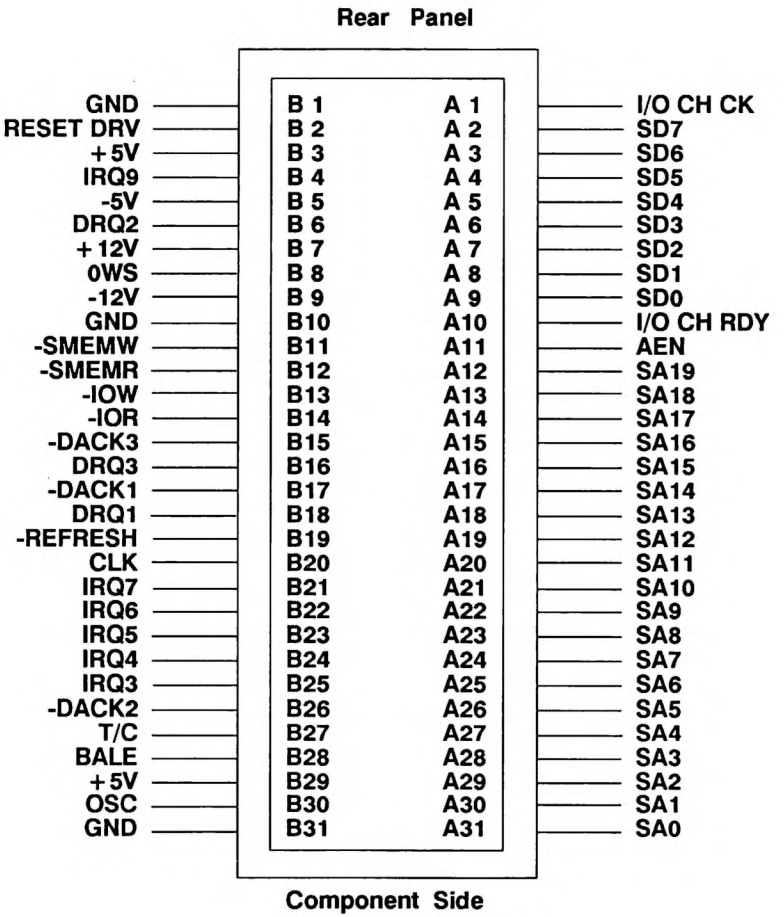
80286-16/20/25 provides AT compatible buses an high speed memory buses. The board contains the following bus types:

1. **ONE 8-bit slots** for use by PC compatible ADD-ON cards.
2. **FIVE 16-bit slots** for use by PC/AT compatible ADD-ON cards.

SLOTS #	DATA WIDTH	ADDRESS WIDTH
J3 ,	8	20
J4 , J9	16/8	24
J5 , J10	16/8	24
J6 , J11	16/8	24
J7 , J12	16/8	24
J8 , J13	16/8	24

The following figure shows the location and the order of the I/O channel connectors.

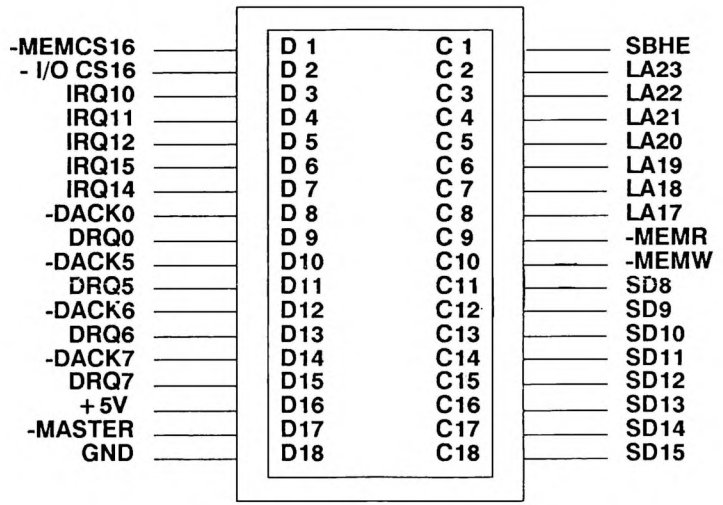
- **8-BIT (Sixty-two pin) channels**



I/O Channel J3 to J8

- 16-BIT (thirty-six pin) channels

Rear Panel



Component Side

I/O Channel J3, J9 ,J10,J11,J12,J13

PHOENIX BIOS ON 80286-16/20/25

A.1 SYSTEM SET-UP

The system has **CMOS RAM** with battery backup, so, after power off and power on again, the system configuration informations which are stored in CMOS RAM, will recall automatically.

The system set-up program is included in **ROM BIOS** written by **Phoenix Technologies Ltd.** In the set-up program you can use keyboard to set/change your system configuration such items as the time, date, disk drive, memory size, display card.

⌘ SET-UP PROCEDURE

Turn the computer on, the BIOS performs diagnostics of the system and displays as below :

Phoenix 80286 ROM BIOS PLUS Version 3.10. 21
Copyright (C) 1985-1989 Phoenix Technologies Ltd.
All Rights Reserved

PCT COMPUTER

then display the size of the memory being tested (at this time you can bypass the memory test by pressing **<SPACE BAR>**). If you have wrong configuration of your system, error messages will be displayed on the screen :

Invalid configuration information - please run SETUP program
Strike the F1 key to continue, F2 to run the setup utility

You can press **<F1>** key to ignore it or pressing **<F2>** key to enter ROM set-up program.

*** **NOTE :**

If you reboot the system before enter the operation system successfully, the **BIOS** will load a set of default value when **POST** (Power On Self Test) regardless of the **CMOS** values, and display as below while the memory size is greater than **512K:**

= =

Last Boot Failed, using default values
512K Base Memory, 00000K Extended

Invalid configuration information - please run SETUP program
Strike the F1 key to continue, F2 to run the setup utility

= =

Then you can **reset again**, the system will reload the CMOS values.

Once you have entered the set-up program, you will see the following screen :

```
Phoenix Technologies Ltd.
System Configuration Setup V4.02


Time:   15:09:55
Date :  Fri  Jan 01,  1988


Diskette A:          5.25 Inch, 1.2 MB
Diskette B:          5.25 Inch, 1.2 MB  Cyl Hd  Pre  Lz  Sec Size
Hard Disk 1:         Type 17            977 5   300  977 17  40
Hard Disk 2:         Not  Installed
Base Memory:         640  KB
Extended Memory:     384 KB
Display:             VGA/EGA
Keyboard:            Installed
CPU Speed:           HIGH

Coprocessor:         Installed


Up and Down Arrow to select entries
Left and Right Arrow to change entries
PgUp for CS8221 chip set options
F1 for help.  F10 to Exit.  Esc to reboot.
```

Follow the screen prompts, press **<Up>**, **<Down>**, **<Left>**, **<Right>** key to select/change entries. Press **<F1>** key, online help is displayed for the current menu item where the cursor is located.

» Time & Date

This enables your computer to know the correct time of day and date whenever you turn on your system.

» Diskette

This setting is used to identify the type of diskette drives you have.

» Hard disk

This setting is used to identify what type of hard disks you have, and display the parameters for the currently selected hard disks on the main menu screen. The **PHOENIX** set-up utility provide **forty nine** types, you can hit **< F1 >** key to see the list of drives.

***** NOTE :**

For special model that is excluded in the built-in device table, user can press **< Up >** key to set-up the parameters of hard disk in **Type 48** and **Type 49.**

Following table are the hard disk drive parameters of **PHOENIX BIOS PLUS Version 3.10 . 21**

DRV TYPE	CYL	HD	WRITE PRECOMP	LANDING ZONE	SETCORS	MEGA BYTE
1	306	4	128	305	17	10
2	615	4	300	615	17	20
3	615	6	300	615	17	30
4	940	8	512	940	17	62
5	940	6	512	940	17	46
6	615	4	-1	615	17	20
7	462	8	256	511	17	30
8	733	5	-1	733	17	30
9	900	15	-1	901	17	112
10	820	3	-1	820	17	20
11	855	5	-1	855	17	35
12	855	7	-1	855	17	49
13	306	8	128	319	17	20
14	733	7	-1	733	17	42
16	612	4	0	663	17	20
17	977	5	300	977	17	40
18	977	7	-1	977	17	56
19	1024	7	512	1023	17	59
20	733	5	300	732	17	30
21	733	7	300	732	17	42
22	733	5	300	733	17	30
23	306	4	0	336	17	10
25	615	4	0	615	17	20
26	1024	4	-1	1023	17	34
27	1024	5	-1	1023	17	42
28	1024	8	-1	1023	17	68
29	512	8	256	512	17	34
30	615	2	615	615	17	1

DRV TYPE	CYL	HD	WRITE PRECOMP	LANDING ZONE	SECTORS	MEGA BYTE
31	989	5	0	989	17	41
32	1020	15	-1	1024	17	127
35	1024	9	1024	1024	17	76
36	1024	5	512	1024	17	42
37	830	10	-1	830	17	68
38	823	10	256	824	17	68
39	615	4	128	664	17	20
40	615	8	128	664	17	40
41	917	15	-1	918	17	114
42	1023	15	-1	1024	17	127
43	823	10	512	823	17	68
44	820	6	-1	820	17	40
45	1024	8	-1	1024	17	68
46	925	9	-1	925	17	69
47	699	7	256	700	17	40
48	0	0	0	0	0	0
49	0	0	0	0	0	0

» Base Memory

This setting is used by the power on self tests in your computer to identify the amount of base memory available

Selecting "**Backfill**" will cause the computer to use all memory up to the beginning of video memory.

***** NOTE :**

Video Memory Backfill allows the use of all memory up to the beginning of the video memory area, for DOS and the user to access this additional memory area. The actual amount of memory available to the BIOS is dependent on the actual video adapter being used.

To use Video Memory Backfill option, base RAM size must be greater than **640K** and **640K-1024K** relocation must be disabled.

The following table specifies the amount of memory available with different adapters:

ADAPTER	MEMORY ENABLED
EGA	640K
MONOCHROME	704K
CGA	736K

» Extended Memory

This setting is used by the power on self tests in your computer to identify the amount of extended memory available.

» Display

This setting is used to identify the type of display that is attached to your computer

» Keyboard

This setting is used to identify whether or not there is a keyboard installed.

» CPU Speed

This setting is used to set the default CPU speed at boot time.

» Coprocessor

Whether coprocessor installed or not will be detected automatically during POST.

The **PHOENIX BIOS** have two pages in set-up program, change to next page by pressing **<PgUp>** key.

***** NOTE :**

If you are convienced that all the information you have entered into the set-up utility main menu is right, press **<ESC>** key ending set-up procedures.

¤ Set-up 2nd page are described on next sections
- APPENDIX A.2 , A.3.

A.2 SHADOW RAM

The meaning of **SHADOW RAM** is load the **BIOS ROM** into **RAM**, since the speed of RAM is faster than ROM (typically RAM access time is about 60 ns to 120 ns, ROM access time is about 200 ns), therefore, copying the BIOS ROM into RAM speeds up execution of the BIOS code, will imporve the overall performance of your computer.

¤ The **PHOENIX** set-up utility provide **Shadow RAM** option for **BIOS, Video ROM** and **Option ROM** in 2nd page :

Shadow BIOS ROM:	Disabled
Shadow Video ROM:	Disabled
Shadow 16K at C4000:	Disabled
Shadow 16K at C8000:	Disabled
Shadow 16K at CC000:	Enabled
Shadow 16K at D0000:	Disabled
Shadow 16K at D4000:	Disabled
Shadow 16K at D8000:	Enabled
Shadow 16K at DC000:	Disabled
Shadow 16K at E0000:	Disabled
Shadow 16K at E4000:	Disabled
Shadow 16K at E8000:	Disabled
Shadow 16K at EC000:	Disabled

You can press **<Up>**, **<Down>**, **<Left>**, **<Right>** key to disable or enable shadow RAM.

The standard BIOS allows load the system BIOS and/or the Video BIOS into shadow RAM for operation at 0/1 wait states, other ROMs in the C4000 to EC000 region can also be copied to shadow RAM.

Shadow RAM operation is allowed only if both the base memory size is greater than **640K** and **640K - 1024K** relocation is not enabled.

⌑ **Memory Wait States :**

This setting allow user to specify **0 or 1 DRAM Wait States**.

During the Power On Self-Test and Initialization procedure. the BIOS will set the DRAM Wait States to the value stored in CMOS by the set-up utility.

⌑ **640-1024K Relocation :**

This setting allows **384K** of memory from 640K - 1024K to be relocated to above 1MB and used as extended memory.

Use of this feature requires exactly **1MB** of system board memory.

If enable 640K - 1024K relocation, the BIOS will not perform **Video Memory Backfill** nor the **Shadow** option for ROM BIOS, Video ROM, and Option ROMs.

A.3 EMS DRIVER INSTALLATION

EMS (Expanded Memory Specification) memory is a special type of memory that allows specially written software packages to access program data far larger than 640KB limit imposed by DOS.

The **EMS driver program - EMM.SYS** (Version 4.1.1 can set your system memory to utilize the Lotus, Intel, Microsoft (LIM) Expanded Memory Specification to enable software recognition of this expanded memory.

The procedure of set-up BIOS utility program and install EMS driver in config.sys file on your system are as follow.

¤ BIOS SET-UP

If you want install EMS on your system, you must modify the presented parameter in the BIOS :

- Press <**F2**> key if the BIOS has the CMOS set-up option, or press <**Ctrl**>-<**Alt**>-<**S**> on DOS prompt to run the set-up utility.
- Press <**PgUp**>, then the 2nd page of the set-up utility appears.
- Press <**Down**> to "EMS Base Memory Address:" in the right of screen and press <**Left**> or <**Right**> to change entries if necessary.

EMS Base Memory Address:	Segment C000:
EMS Base I/O Address:	208/209h
EMS Page 0 Reg. Extension	1M to 2M
EMS Page 1 Reg. Extension	1M to 2M
EMS Page 2 Reg. Extension	1M to 2M
EMS Page 3 Reg. Extention	1M to 2M
EMS Memory Size:	0.5M
EMS Wait States:	0 Wait Stats
EMS Memory:	Disabled

» EMS Base Memory Address

This setting is used to set the base memory address for EMS Memory. There are **C000, C400, C800, CC00, D000, D400, D800, DC00, E000** available.

***** NOTE :**

Make sure not to conflict with any add-on card that is installed on your system.

» EMS Base I/O Address

This setting is set up the mapping information of EMS I/O port address The EMS driver provide seven I/O ports: **208/209h 218/219h, 258/259h, 268/269h, 2A8/2A9h, 2B8/2B9h, 2E8/2E9h**, you can select one of these ports for EMS memory use.

***** NOTE :**

Make sure not to conflict with any add-on card that is installd on your system.

» EMS Page x Reg. Extension

This setting is set up the page register address extension of page 0 - page 3 and mapping to **1M to 2M, 2M to 4M, 4M to 6M, 6M to 8M.**

» EMS Memory Size

This setting is set the EMS memory size, there are **0.5M to 7M** memory supported.

» EMS Wait States

This setting is set the EMS memory for **0 wait states or 1 wait states.**

» EMS Memory

This setting is set the **EMS memory** to **enabled or disabled** before booting.

Press <**ESC**> to reboot the system, The EMS has been successfuly loaded.

⌘ EMS DRIVER SET-UP

Boot PC system by using DOS, then Copy the **EMM.SYS** file to the root directory.

Type:

COPY CON CONFIG.SYS <Enter>
device=emm.sys -D <Enter>
^z (or press <**F6**> key) <Enter>

The screen will display as follows :

1 File(s) copied

» Please refer to the EMM.DOC in the utility diskette.

***** NOTE :**

If you already have a **CONFIG.SYS** file on your disk, simply edit it using **EDLIN.COM** in DOS or other **ASCII** text editor, adding the " **device=emm.sys -D** " line to CONFIG.SYS file.

Re-boot your system. The screen will display the following as confirmation that the EMM.SYS has been installed :

CHIPS Expanded Manager ,Version 4.1.1
(C) Copyright Chips & Technologies, Inc.1988, All Right Reserved

PCT

There are xx pages, or xxxx Kbytes of EMS Expanded Memory on the system

APPENDIX B

AMI BIOS ON 80286-16/20/25

B.1 Setup System Configuration

A setup program has been built into the system BIOS so the configurations stored in the CMOS RAM can be changed. This program should be executed only after:

1) User has changed system configuration,
2) User has changed system backup battery, or
3) System has detected a configuration error and has asked the user to run the setup program.

After power-on RAM testing, the message: "PRESS < DEL > if you want to run SETUP/EXTD" is displayed on the screen. Press "DEL" to runsetup or do nothing to bypass. if "Del" key pressed, the following messages will be displayed:

EXIT FOR BOOT
RUN CMOS SETUP
RUN XCMOS SETUP

Figure B-1: Setup Menu Screen

Use and keys to select and press "Enter" to run the selected Program.
The setup program is completely menu driven. Use arrow keys to select entry; " PgDn " / " PgDn " keys to change seiected entry; and " ESC " key to exit. Help messages are displayed in a window on the screen.

```
    CMOS SETUP (C) Cdpyright 1985-1989, American Megatrends Inc.
Date (mn/date/year): Mon, May 01 1989   Base memory size : 640 KB
Time (hour/min/sec): 10 : 06 : 29       Ext. memory size : 3072 KB
Floppy drive a :    : 1.2  MB, 5 1/4"   Numeric Processor: Installed
Floppy drive b :    : 1.2  MB, 5 1/4"

                                        Cyln Head WPcom LZone Sec Size
Hard Disk c: type   : 47 = USER TYPE    1024  9   1024  1024  26  117MB
Hard Disk d: type   : Not Installed
Primary display     : VGA or EGA
Keyboard            : Not Installed


 Scrtatch.RAMoption :  1
                                          Sun Mon Tue Wed Thu Fri Sat
                                           30   1   2   3   4   5   6
 Month : Jan, Feb ..... Dec                7   8   9  10  11  12  13
 Date  : 01   02   03,... 31               14  15  16  17  18  19  20
 Year  : 1901, 1902,..... 2099             21  22  23  24  25  26  27
                                           28  29  30  31   1   2   3
 ESC = Exit,  Select, PgUp/PgDn = Modify    4   5   6   7   8   9  10
```

Figure B-2: CMOS Setup Screen

RUN CMOS SETUP

If this option is chosen then the screen as in Figure B-2 is displayed.

System BIOS automatically detects memory size and the presence of numeric processor, no changes is necessary. After the changes are made, press "ESC" key to exit. User is prompted "Write data into CMOS and exit (Y/N)?" Press "Y" to save the changes and reboot. Press "N" to go back to the setup program.

No changes will be in effect until the system is rebooted

EXTENDED CHOS SETUP PROGRAM Ver - 1.50 ,(C)1988, American Megatrends Ine.

NEAT CHIPSET SETUP PROGRAM
MAIN MENU

EASY NEAT CHIPSET REGISTER SETUP
ADVANCED NEAT CHIPSET REGISTER SETUP
ENABLE/DISABLE VIDED AND MAIN BIOS SHADOW
WRITE CMOS REGISTERS AND EXIT
DO NOT WRITE CMOS REGISTERS AND EXIT

Figure B-3 XCMOS Setup Menu Screen

RUN XCMOS SETUP

Extended CMOS SETUP program ("XCMOS") allows user to select special functions such as memory wait state or shadow

```
EEXTENDED CMOS SETUP PROGRAM Ver - 1.50 ,(C)1988, American Megatrends

                    Memory Configuration
 Bank       Enable/Disable       DRAM Type        Waitstste
 ----       --------------       ---------        ----------
  0         ENABLED              1 MEG            0 WAIT STATE
  1         ENABLED              1 MEG            0 WAIT STATE
  2         DISABLED                              0 WAIT STATE
  3         DISABLED                              0 WAIT STATE
                  Clock Source Sslscted
  Processor Clock     Bus Clock      DMA Clock
  ---------------     ---------      ---------     F0000 SHADOW ENABLE
  CLK2IN              CLK2IN/2       SCLK/2        F0000 SHADOW DISABLE

                                                   MOVE BAR-<PgUp/PgDn>
                                                   CHANGE WINDOW.....
            Shadow RAM/Interleave                  EXIT - <ESC>

   BIOS Shadow          Video Shadow          Memory
   F000H,64K       C000H,16K  C4000H,16K     Interleave
   -----------     ---------  ----------     ----------
   ENABLED         ENABLED    ENABLED        ENABLED
```

Figure B-4: Easy NEAT Chipset Register Setup Screen

RAM by changing the register value. When selectted, you will see a XCMOS setup program menu screen as in Figure B-3

A warning message as in Figure B-4 is displayed befor entering these setup programs.

User are not encouraged to run XCMOS setup program. Your system should have been fine tuned before shipping. Improper setup may cause the system to fail. Consult your dealer before making any changes.

EASY NEAT CHIPSET REGISTER SETUP

This setup program provides fillowing selection:

1) Memory wait state based on system RAM speed, select 1 or 0 wait state.
2) Shadow RAM and memory interleave enable or disable BIOS/video shadow and memory interleave function.

EXTENDED CMOS SETUP PROGRAM Ver - 1.50, (C)1988, American megatrends

WARNING--IMPROPER USE OF SETUP MAY CAUSE THE SYSTEM TO
FAIL NORMAL OPERATIONS !
IF THE SYSTEM FAILS, PRESS AND HOLD THE <INS> KEY
AND TURN THE MACHINE OFF AND THEN ON !

RELEASE THE <INS> KEY AFTER MEMORY TEST SARTS !

H I T <ESC> T O S T O P N O W !
H I T <ENTER> T O C O N T I N U E !

Figure B-5: XCMOS Setup Warning Message Screen

A screen as in Figure B-5 is displayed if this option is chosen

ADVANCED NEAT CHIPSET REGISTER SETUP

This setup program provides selections of:

1) Memory type selects DRAM type such as 256Kb or 1Mb.
2) Memory Bank Enable/disable active memory bank.
3) EMS Memory Enable/disable EMS memory, set EMS memory size

A screen as in Figure B-6 is displayed if this option is chosen.

```
EXTXENDED CMOS SETUP PROGRAM Ver - 1.50, (C)1988, American Megaterends

              BITS   7 - 8
 82C211     60H - 00   0 0 R 0 R 0      Go to Prev/Next Register -
            61H - 0 1   00   01   01      Go to Prev/Next Entry   -
            62H - RR    01   10   00       Scroll Bit Value - PgUp/PgDn
                                           Return to MAIN MENU  - <ESC>
 82C212B    64H - 0      01    RRRRR
            65H - 0 0 0 0 1 1 1 0      PROCCLK Register RA0
            66H - 1 0 0       RRRRR
            67H - 0 0 0 0 0 0 0 0      82C211 Revision number
            68H - 0 0 0 0 0 0 0 0
            69H - 0 0 0 0 0 0 0 0
            6AH - 10   1      RRRRR
            6BH - 1 0 0 1   01   10
            6CH - 10      1   0 RRRR
            6DH - 0100          0000
            6EH - 00    00   00   00
            6FH - 000   0 R   1 1 R

 82C286     01H - 11   00   00   0 0
```

Figure B-6: Advanced Chip Registers Setup Screen

Help messages in the lower righthand window describes the function of each register selected.

```
 ENABLE/DISBALE VIDEO AND BIOS SHADOW
-------------------------------------------------------------

  Use this setup program to enable/disable video and BIOS
```

```
EXTENDED CMOS SETUP PROGRAM Ver - 1.50, (C)1988, American Megatrends

     SETUP SHADOW RAM FOR 212              Go to Prev/Next Register -
                                            Go to Prev/Next Entry   -
 MAIN BIOS SHADOW AT F0000H.64K ->1        Scroll Bit value - PgUp/PgDn
 VIDEO BIOS SHADOW AT C0000H.16K ->1
 VIDEO BIOS SHADOW AT C4000H.16K ->1
                                        MAIN BIOS SHADOW AT F0000H.64K

                                             1 = SHADOW ENABLE
                                             0 = SHADOW DISABLE
```

Figure B-7: Shadow RAM Setup Screen

shadow function. A screen as Figure B-7 is displayed if this option is chosen:

WRITE CMOS REGISTERS AND EXIT

Select this option and press "Enter" key after xcmos setup is done to activate the changes. System will change registers value and reboot.

DO NOT WRITE XMOS REGISTERS AND EXIT

When this option is selected, system will ignore changes you've made and reboot.

SYSTEM HANG SAVER

If the system fails due to improper setup, press and hold the < INS > key, and turn the machine off and then on. Release the < INS > key after memory test starts. This will reset all NEAT registers to the system defaults.

SYSTEM DEFAULT FOR NEAT CHIPSET

When the system is powered on, memory size along with the memory banks enable. DRAM type is determined automati-cally by the hardware. Other NEAT configuration registers will contain the default values.
Major NEAT configuration default parameters are summarized as the following:

* Wait state:
  - RAM access cycle = 1 wait state
  - EMS memory access cycle = 2 wait states
  - ROM access cycle = 3 wait states
  - (XIOR/XIOW) read/write cycle = 4 wait states
  - 16-bit DMA cycle = 1 wait state
  - 8-bit DMA cycle = 1 wait state
  - 16-bit AT bus cycle = 1 wait state
  - 8-bit AT bus cycle = 4 wait states

* Command delay:
  - AT bus 1/0 cycle = 1 command delay
  - AT bus 16-bit memory cycle = 0command delay
  - AT bus 8-bit memory cycle = 1 command delay

* 88C211 Mode
  - Quick mode is disabled (default is normal mode)

* Clock Source
  - Processor clock (PROCCLK) = CLK2IN (CLK2IN = the clock speed which the turbo switch selects)
  - AT bus clock (BCLK) = CLK2IN/2
  - DMA clock (DMACLK) = SCLK/2 (SCLK = PROCCLK/2)

* Memory interleave
  - Memory interleave is enabled.
  - If 2 banks are used, 2-way interleaved.
  - If 4 banks are used, 4-way interleaved.

* Shadow RAM function
  - Shadow RAM is Disabled.
  - Shadow RAM write protection = READ/WRITE.
  - Only [F0000H - FFFFFH] of ROM is enabled.

* EMS function
  - EMS function = Disbled
  - EMS memory size = 0
  - EMS base addresses = D0000H, D4000H, D8000H, DC000H
  - EMS page register 1/0 base addresses = 208H/209H
  - EMS page 0 - 3 addresses extension range 1M - 2M
  - External EMS mapper status = disabled

SYSTEM OPTIMIZATION

The following changes can increase your 80286 NEAT system performance no matter what hardware configuration/ adaptor is used, provided that you use the 80ns DRAM:

- The Turbo switch is default to the higher clock speed.

  Maintain PROCCLK = CLK2IN.

- Memory interleave function is default enabled.

- Change RAM access wait state to 0.

- Shandow Main BIOS, VIDEO BIOS or others in RAM.

The system can be tuned up even better by decreasing the various other wait-states command-delays, and increasing the Bus/DMA clock speed. However, these changes are usually dependent on the adapptor's capability.

EMS SETUP

If the user wants to use the EMS function, you must select the " ADVANCED NEAT CHIPSET REGISTER SETUP " select (1) enable EMS function = Bit 4 of RB7, and (2) determine the EMS memory size = Bit (7 - 5) of RB11. Other related EMS items may be changed or maintain default values the system reboots and is under DOS control, you should install your EMS driver foollowing its documentation. NOW, you are ready to run any software using the EMS function !

NOT - TO - DO

All bits of RB1, RB3, RB4, and RB5 in 82C212B for shadow RAM function CAN NOT be set within setup progrsams by the user directly. You can only use " ENABLE/DISABLE VIDEO AND MAIN BIOS SHANDOW " while in "EASY NEAT CHIPSET REGISTER SETUP " After you write the CMOS RAM and exit, the system will reboot and load the data from the ROM area to the shadow RAM before it actually sets the corresponding bits. These bits should never be set by the users directly.Or,you may hang the system or lose your video screen.