The following jumper settings are silkscreened on the board:

CPU Select: (5V only board!)
486SX: JP18 Open, JP19 Open, JP20 2-3
486DX: JP18 1-2, JP19 CLOSE, JP20 1-2
UMC U5S sort of works with the 486SX setting, but it doesn't seem well utilized by the board (scores are suspiciously low with the U5S).
Cyrix 486DX does not seem to work on this board for some reason, comes up -- on the POST probe regardless of BIOS.

AV9107C-03 Clock Generator Speeds:
16MHz: JP11 CLOSE, JP12 CLOSE, JP13 CLOSE, JP14 CLOSE
20MHz: JP11 Open, JP12 CLOSE, JP13 CLOSE, JP14 Open
25MHz: JP11 Open, JP12 CLOSE, JP13 Open, JP14 CLOSE
33MHz: JP11 Open, JP12 Open, JP13 CLOSE, JP14 CLOSE
50MHz (see JP50 too): JP11 Open, JP12 Open, JP13 CLOSE, JP14 Open

JP50 Timing Jumper: CLOSE for 50MHz, Open for all other speeds

Cache Settings:
64KB: JP15 Open, JP16 Open, JP6 Open, JP5 Open, JP8 2-3, JP7 Open, U39 8Kx8, U40 N/A, populate SRAM bank 0 and 1 with 8x 8Kx8 SRAMs
128KB: JP15 Open, JP16 CLOSE, JP6 Open, JP5 CLOSE, JP8 1-2, JP7 CLOSE, U39 8Kx8, U40 N/A, populate SRAM bank 0 with 4x 32Kx8 SRAMs
256KB: JP15 CLOSE, JP16 CLOSE, JP6 CLOSE, JP5 CLOSE, JP8 2-3, JP7 CLOSE, U39 8Kx8, U40 8Kx8, populate SRAM banks 0 and 1 with 8x 32Kx8 SRAMs. You can alternatively use a 32Kx8 in U39 and leave U40 open.

U24 is for the Dirty bit TAG SRAM. It requires a 64Kx1, 12/15ns SRAM (such as a Cypress CY7C187-15PC) to be populated here for proper write back cache operation. Without it, the board's already sluggish off-cache access latency is DOUBLED according to Cachechk V3! You will likely need to solder a 22-pin socket to the open pads (noting the key notch silkscreen), and add a 0.22uF ceramic bypass capacitor to C186.

JP17: Open for PQFP 486SX, CLOSED for PGA 486DX/SX/etc.

JP1 CMOS Erase Jumper: 1-2 for Discharge/Erase, 2-3 for Normal Operation