# intel®

# Intel® Desktop Board
# DH57DD
## Technical Product Specification

# Revision History

| Revision | Revision History | Date |
|---|---|---|
| -001 | First release of the Intel® Desktop Board DH57DD Technical Product Specification | March 2010 |

This product specification applies to only the standard Intel® Desktop Board DH57DD with BIOS identifier JGIBX10J.86A.

Changes to this specification will be published in the Intel Desktop Board DH57DD Specification Update before being incorporated into a revision of this document.

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# Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the Intel® Desktop Board DH57DD.

## Intended Audience

The TPS is intended to provide detailed, technical information about the Intel Desktop Board DH57DD and its components to the vendors, system integrators, and other engineers and technicians who need this level of information.  It is specifically *not* intended for general audiences.

## What This Document Contains

| Chapter | Description |
|---------|-------------|
| 1 | A description of the hardware used on the Intel Desktop Board DH57DD |
| 2 | A map of the resources of the Intel Desktop Board |
| 3 | The features supported by the BIOS Setup program |
| 4 | A description of the BIOS error messages, beep codes, and POST codes |
| 5 | Regulatory compliance and battery disposal information |

## Typographical Conventions

This section contains information about the conventions used in this specification.  Not all of these symbols and abbreviations appear in all specifications of this type.

### Notes, Cautions, and Warnings

**NOTE**

*Notes call attention to important information.*

⚠ **CAUTION**

*Cautions are included to help you avoid damaging hardware or losing data.*

## Other Common Notation

| | |
|---|---|
| # | Used after a signal name to identify an active-low signal (such as USBP0#) |
| GB | Gigabyte (1,073,741,824 bytes) |
| GB/s | Gigabytes per second |
| Gb/s | Gigabits per second |
| KB | Kilobyte (1024 bytes) |
| Kbit | Kilobit (1024 bits) |
| kbits/s | 1000 bits per second |
| MB | Megabyte (1,048,576 bytes) |
| MB/s | Megabytes per second |
| Mbit | Megabit (1,048,576 bits) |
| Mbits/s | Megabits per second |
| xxh | An address or data value ending with a lowercase h indicates a hexadecimal value. |
| x.x V | Volts.  Voltages are DC unless otherwise specified. |
| * | This symbol is used to indicate third-party brands and names that are the property of their respective owners. |

# Contents

# 3 Overview of BIOS Features

# 4 Error Messages and Beep Codes

# 5 Regulatory Compliance and Battery Disposal Information

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# 1 Product Description

## 1.1 Overview

### 1.1.1 Feature Summary

Table 1 summarizes the major features of the board.

**Table 1. Feature Summary**

| Form Factor | microATX (9.6 inches by 9.6 inches [243.84 millimeters by 243.84 millimeters]) |
|---|---|
| Processor | • Intel® Core™ i7, Intel® Core™ i5, Intel® Core™ i3, Intel® Pentium® processors, and Intel® Xeon® processor 3400 series in an LGA1156 socket:<br>— Integrated graphics processing (processors with Intel® High Definition Graphics (Intel® HD Graphics))<br>— External graphics interface controller<br>— Integrated memory controller |
| Chipset | Intel® H57 Express Chipset consisting of the Intel® H57 Platform Controller Hub (PCH) |
| Memory | • Four 240-pin DDR3 SDRAM Dual Inline Memory Module (DIMM) sockets<br>• Dual Channel DDR3 1333 MHz and DDR3 1066 MHz support<br>• Support for 1 Gb and 2 Gb memory technology<br>• Support for up to 16 GB of system memory with four DIMMs using 2 Gb memory technology<br>• Support for non-ECC memory |
| Graphics | • Integrated graphics support for processors with Intel HD Graphics:<br>— High Definition Multimedia Interface* (HDMI*)<br>— DVI-I<br>• Discrete graphics support for PCI Express 2.0 x16 add-in graphics card |
| Audio | • 10-channel (7.1+2) Intel® High Definition Audio via the Realtek* ALC889 audio codec<br>• 8-channel (7.1) Intel High Definition Audio via the HDMI interface |
| Peripheral Interfaces | • Fourteen USB 2.0 ports:<br>— Six ports are implemented with stacked back panel connectors<br>— Eight front panel ports are implemented with four dual-port internal headers<br>• Five internal Serial ATA (SATA) 3.0 Gb/s ports<br>• One external SATA (eSATA) back panel connector<br>• One serial port header<br>• Two front panel IEEE 1394a ports |
| Legacy I/O Control | Nuvoton W83677i Super I/O controller for serial port support |
| BIOS | • Intel® BIOS resident in the SPI Flash device<br>• Support for Advanced Configuration and Power Interface (ACPI), Plug and Play, and SMBIOS |

continued

**Table 1. Feature Summary** (continued)

| | |
|---|---|
| **Instantly Available PC Technology** | • Support for PCI* Local Bus Specification Revision 2.3<br>• Support for PCI Express*<br>• Suspend to RAM support<br>• Wake on PCI, PCI Express, LAN, front panel, serial, USB ports, and Consumer IR |
| **LAN Support** | Gigabit (10/100/1000 Mbits/s) LAN subsystem using the Intel® 82578DC Gigabit Ethernet Controller |
| **Expansion Capabilities** | • One PCI Express 2.0 x16 add-in card connector<br>• Two PCI Express 1.0 x1 bus add-in card connectors<br>• One Conventional PCI bus add-in card connector |
| **Hardware Monitor Subsystem** | • Intel® Quiet System Technology (Intel® QST) implemented through Intel® Management Engine (Intel® ME) in the Intel H57 PCH<br>• Voltage sense to detect out of range power supply voltages<br>• Thermal sense to detect out of range thermal values<br>• Two fan headers using PWM control<br>• 4-pin header for the processor fan<br>• 4-wire and 3-wire (linear) fan speed control support for the front and rear chassis fans<br>• Support for Platform Environmental Control Interface (PECI) |

## 1.1.2      Board Layout

Figure 1 shows the location of the major components on Intel Desktop Board DH57DD.



OM22196
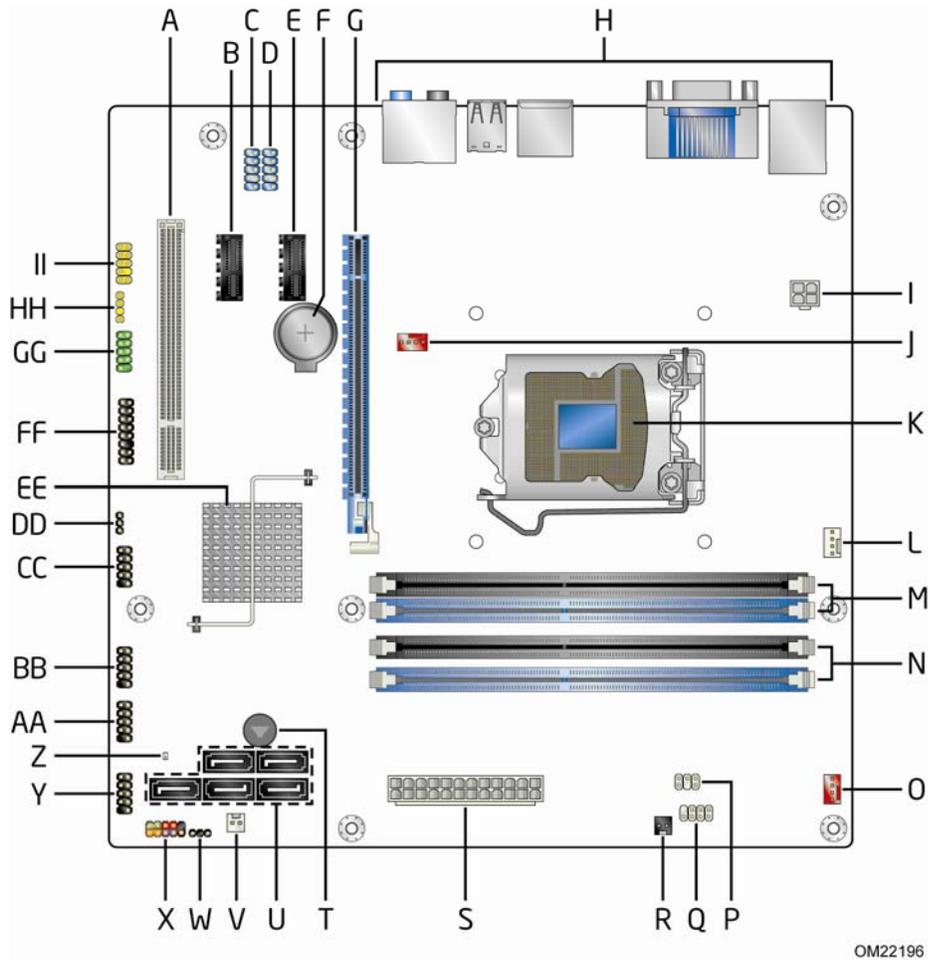
**Figure 1.  Major Board Components**

Table 2 lists the components identified in Figure 1.

**Table 2.  Components Shown in Figure 1**

| Item/callout from Figure 1 | Description |
| --- | --- |
| A | Conventional PCI bus add-in card connector |
| B | PCI Express x1 add-in card connector |
| C | Front panel IEEE 1394a header |
| D | Front panel IEEE 1394a header |
| E | PCI Express x1 add-in card connector |
| F | Battery |
| G | PCI Express x16 add-in card connector |
| H | Back panel connectors |
| I | Processor core power connector (2 x 2) |
| J | Rear chassis fan header |
| K | LGA1156 processor socket |
| L | Processor fan header |
| M | Channel A DIMM 0 socket |
| N | Channel B DIMM 0 socket |
| O | Front chassis fan header |
| P | Consumer IR receiver (input) header |
| Q | Consumer IR emitter (output) header |
| R | Chassis intrusion header |
| S | Main power connector (2 x 12) |
| T | Piezoelectric speaker |
| U | SATA connectors |
| V | Intel Remote Assist PC header |
| W | Alternate front panel power LED header |
| X | Front panel header |
| Y | Front panel USB header |
| Z | Standby power LED |
| AA | Front panel USB header |
| BB | Front panel USB header |
| CC | Front panel USB header |
| DD | BIOS setup configuration jumper block |
| EE | Intel H57 Express Chipset |
| FF | Intel High Definition Audio Link header |
| GG | Serial port header |
| HH | S/PDIF header |
| II | Front panel audio header |

# 1.1.3 Block Diagram

Figure 2 is a block diagram of the major functional areas of the board.
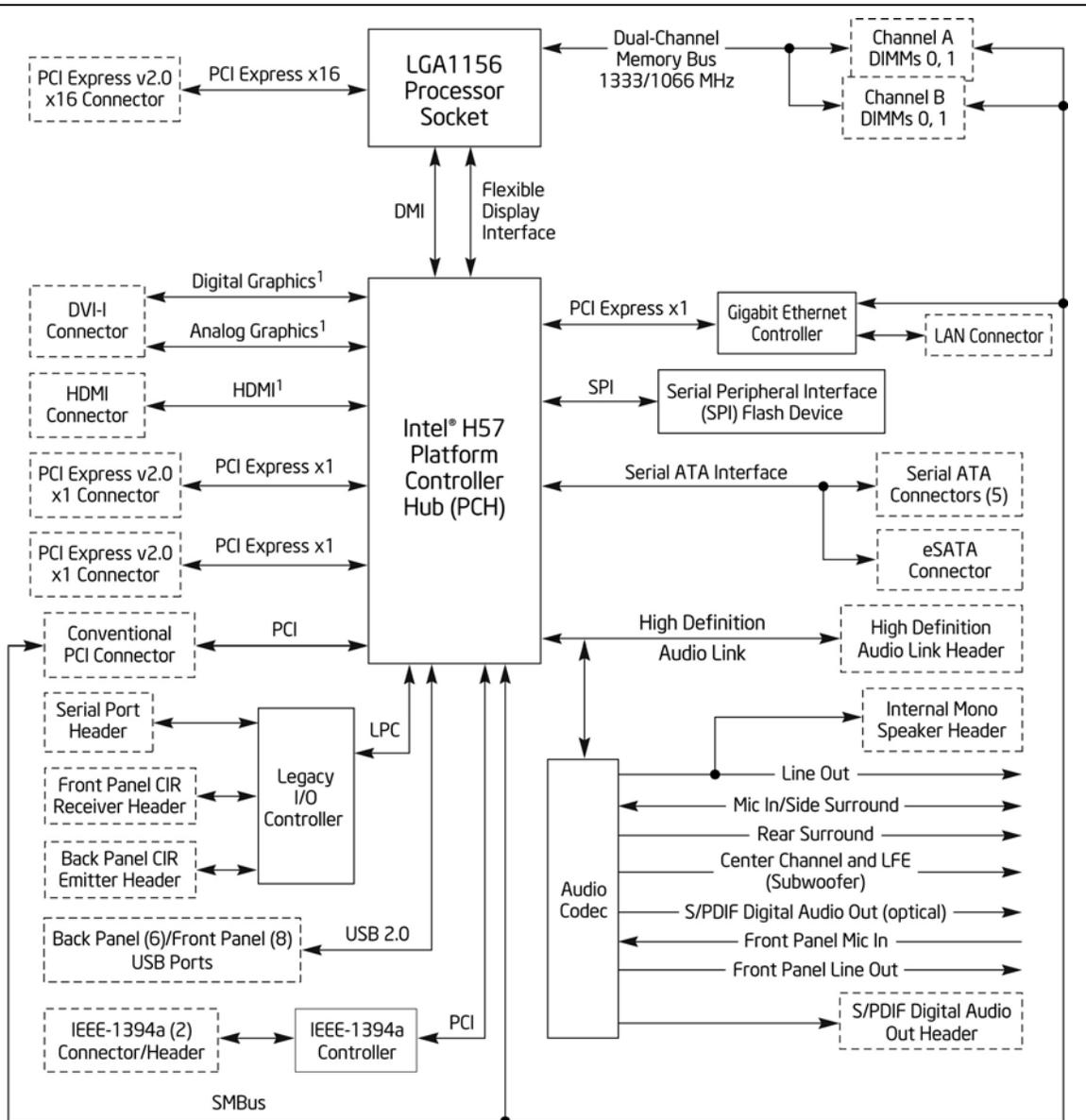


**Figure 2. Block Diagram**

## 1.2    Legacy Considerations

This board differs from other Intel Desktop Board products, with specific changes including (but not limited to) the following:

- No floppy drive connector
- No parallel port connector
- No PS/2 connector
- No PATA interface

## 1.3    Online Support

| To find information about... | Visit this World Wide Web site: |
| --- | --- |
| Intel Desktop Board DH57DD | http://www.intel.com/products/motherboard/DH57DD/index.htm |
| Desktop Board Support | http://www.intel.com/support/motherboards/desktop |
| Available configurations for the Intel Desktop Board DH57DD | http://www.intel.com/products/motherboard/DH57DD/index.htm |
| Supported processors | http://processormatch.intel.com |
| Chipset information | http://www.intel.com/products/desktop/chipsets/index.htm |
| BIOS and driver updates | http://downloadcenter.intel.com |
| Tested memory | http://www.intel.com/support/motherboards/desktop/sb/CS-025414.htm |
| Integration information | http://www.intel.com/support/go/buildit |

## 1.4    Processor

The board is designed to support the Intel Core i7, Intel Core i5, Intel Core i3, Intel Pentium processors, and Intel Xeon processor 3400 series processors in an LGA1156 socket.

Other processors may be supported in the future. This board is designed to support processors with a maximum TDP of 87 W.  See the Intel web site listed below for the most up-to-date list of supported processors.

| For information about... | Refer to: |
| --- | --- |
| Supported processors | http://processormatch.intel.com |

⚠ **CAUTION**

*Use only the processors listed on the web site above.  Use of unsupported processors can damage the board, the processor, and the power supply.*

**NOTE**

*This board has specific requirements for providing power to the processor.  Refer to Section 2.5.1 on page 54 for information on power supply requirements for this board.*

## 1.5    Intel® H57 Express Chipset

The Intel H57 Express Chipset consisting of the Intel H57 Platform Controller Hub (PCH) provides interfaces to the processor and the USB, SATA, LPC, audio, network, display, Conventional PCI, and PCI Express x1 interfaces.  The PCH is a centralized controller for the board's I/O paths.

| For information about | Refer to |
| --- | --- |
| The Intel H57 Express Chipset | http://www.intel.com/products/desktop/chipsets/index.htm |
| Resources used by the chipset | Chapter 2 |

## 1.6    System Memory

The board has four DIMM sockets and supports the following memory features:

- Four independent memory channels with interleaved mode support
- Support for non-ECC, unbuffered, single-sided or double-sided DIMMs with x8 organization and single-sided DIMMs with x16 organization
- 16 GB maximum total system memory (with 2 Gb memory technology).  Refer to Section 2.1.1 on page 37 for information on the total amount of addressable memory.
- Minimum total system memory:  512MB using 1 Gb x16 module
- Serial Presence Detect
- DDR3 1333 MHz and DDR3 1066 MHz SDRAM DIMMs

### NOTE

*To be fully compliant with all applicable DDR SDRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure.  This allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance.  If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted or the DIMMs may not function under the determined frequency.*

Table 3 lists the supported DIMM configurations.

**Table 3.  Supported Memory Configurations**

| DIMM Capacity | Configuration (Note) | SDRAM Density | SDRAM Organization Front-side/Back-side | Number of SDRAM Devices |
| --- | --- | --- | --- | --- |
| 512 MB | SS | 1 Gbit | 1 Gb x16/empty | 4 |
| 1024 MB | SS | 1 Gbit | 1 Gb x8/empty | 8 |
| 2048 MB | DS | 1 Gbit | 1 Gb x8/1 Gb x8 | 16 |
| 2048 MB | SS | 2 Gbit | 2 Gb x8/empty | 8 |
| 4096 MB | DS | 2 Gbit | 2 Gb x8/2 Gb x8 | 16 |

Note:   "DS" refers to double-sided memory modules (containing two rows of SDRAM) and "SS" refers to single-sided memory modules (containing one row of SDRAM).

| For information about... | Refer to: |
| --- | --- |
| Tested Memory | http://www.intel.com/support/motherboards/desktop/sb/CS-025414.htm |

## 1.6.1    Memory Configurations

The Intel Core i7, Intel Core i5, Intel Core i3, Intel Pentium processors, and Intel Xeon processor 3400 series processors support the following types of memory organization:

- **Dual channel (Interleaved) mode**.  This mode offers the highest throughput for real world applications.  Dual channel mode is enabled when the installed memory capacities of both DIMM channels are equal.  Technology and device width can vary from one channel to the other but the installed memory capacity for each channel must be equal.  If different speed DIMMs are used between channels, the slowest memory timing will be used.

- **Single channel (Asymmetric) mode**.  This mode is equivalent to single channel bandwidth operation for real world applications.  This mode is used when only a single DIMM is installed or the memory capacities are unequal.  Technology and device width can vary from one channel to the other.  If different speed DIMMs are used between channels, the slowest memory timing will be used.

| For information about... | Refer to: |
| --- | --- |
| Memory Configuration Examples | http://www.intel.com/support/motherboards/desktop/sb/cs-011965.htm |

Figure 3 illustrates the memory channel and DIMM configuration.



Channel A, DIMM 1
Channel A, DIMM 0
Channel B, DIMM 1
Channel B, DIMM 0

OM22205

**Figure 3.  Memory Channel and DIMM Configuration**

### 1.7.1.3    Digital Visual Interface (DVI-I)

The DVI-I port supports both digital and analog DVI displays.  The maximum supported resolution is 1900 x 1200 (WUXGA).  The DVI port is compliant with the DVI 1.0 specification.  DVI analog output can also be converted to VGA using a DVI-VGA converter.

Depending on the type of add-in card installed in the PCI Express x16 connector, the DVI port will behave as described in Table 5.

**Table 5.  DVI Port Status Conditions**

| PCI Express x16 Connector Status | DVI Digital (DVI-D) Port Status | DVI Analog (DVI-A) Port Status(Note) |
|---|---|---|
| No add-in card installed | Enabled | Enabled |
| Non-video PCI Express x1 add-in card installed | Enabled | Enabled |
| PCI Express x16 add-in card installed | Disabled | Disabled |

Note: DVI analog output can also be converted to VGA with a DVI-VGA converter.

### 1.7.1.3.1    Analog Display (VGA)

The VGA port supports analog displays.  The maximum supported resolution is 2048 x 1536 (QXGA).

The VGA port is enabled for POST whenever a monitor is attached, regardless of the HDMI and DVI-I connector status.

## 1.7.2    PCI Express x16 Graphics

The Intel Core i7, Intel Core i5, Intel Core i3, Intel Pentium processors, and Intel Xeon processor 3400 series processors in an LGA1156 socket support discrete add in graphics cards via the PCI Express 2.0 x16 graphics connector:

- Supports PCI Express GEN2 frequency of 2.5 GHz resulting in 5.0 Gb/s each direction (500 MB/s) per lane.  Maximum theoretical bandwidth on interface is 8 GB/s in each direction, simultaneously, when operating in x16 mode.
- Supports PCI Express GEN1 frequency of 1.25 GHz resulting in 2.5 Gb/s each direction (250 MB/s) per lane.  Maximum theoretical bandwidth on interface is 4 GB/s in each direction, simultaneously, when operating in x16 mode.

## 1.8    USB

The board supports up to fourteen USB 2.0 ports through two EHCI host controllers on the PCH that allow the use of EHCI-compatible drivers.

The port arrangement is as follows:

- Six ports are implemented with stacked back panel connectors
- Eight front panel ports are implemented with four dual-port internal headers

| For information about | Refer to |
|---|---|
| The location of the USB connectors on the back panel | Figure 9, page 40 |
| The location of the front panel USB headers | Figure 10, page 41 |

# 1.9    SATA Interfaces

The board provides five internal SATA connectors (black) and one external SATA connector through the PCH, which support one device per connector.

The PCH provides independent SATA ports with a theoretical maximum transfer rate of 3 Gb/s per port.  A point-to-point interface is used for host to device connections, unlike Parallel ATA (PATA) IDE which supports a master/slave configuration and two devices per channel.

The underlying SATA functionality is transparent to the operating system.  The SATA controller can operate in both legacy and native modes.  In legacy mode, standard IDE I/O and IRQ resources are assigned (IRQ 14 and 15).  In Native mode, standard Conventional PCI bus resource steering is used.  Native mode is the preferred mode for configurations using the Windows* XP, Windows Vista*, and Windows 7* operating systems.

For more information, see: http://www.serialata.org/.

| For information about | Refer to |
|---|---|
| The location of the SATA connectors | Figure 10, page 41 |

# 1.10   Legacy I/O Controller

The Legacy I/O Controller provides the following features:

- One serial port
- Serial IRQ interface compatible with serialized IRQ support for Conventional PCI bus systems
- Intelligent power management, including a programmable wake-up event interface
- One back panel CIR emitter header
- One front panel CIR receiver header

The BIOS Setup program provides configuration options for the Legacy I/O controller.

## 1.10.1    Serial Port

The serial port is implemented as a 10-pin header on the board.  The serial port supports data transfers at speeds up to 115.2 kbits/sec with BIOS support.

| For information about | Refer to |
|---|---|
| The location of the serial port header | Figure 10, page 41 |

# 1.11 Audio Subsystem

The board supports Intel High Definition Audio through the Realtek ALC889 audio codec as well as through the HDMI interface.

The ALC889-based audio subsystem supports the following features:

- Advanced jack sense for the back panel audio jacks that enables the audio codec to recognize the device that is connected to an audio port.
- Stereo input and output via back panel jacks
- Headphone and Mic in functions for front panel audio jacks
- 108 dB Signal-to-Noise ratio (SNR) playback (DAC) quality and 104 dB SNR recording (ADC) quality
- Content Protection for Full Rate loss-less DVD Audio and Blu-ray Disc* audio content playback (with selected versions of media player software)

The audio subsystem supports the following audio interfaces:

- 7.1 analog back panel audio connectors
- Optical S/PDIF-out audio connector
- S/PDIF header (support for optical or coaxial S/PDIF output)
- Front panel audio header with support for Intel HD Audio and AC '97 audio
- Intel High Definition Audio link header

## NOTE

*Systems built with an AC '97 audio front panel will not be able to obtain the Microsoft Windows Vista logo.*

Table 6 lists the supported functions of the front panel and back panel audio jacks.

**Table 6. Audio Jack Retasking Support**

| Audio Jack | Micro-phone | Head-phones | Front Speakers | Line In | Side Surround | Rear Surround | Center/ Sub |
|---|---|---|---|---|---|---|---|
| FP Green | | Default | | | | | |
| FP Pink | Default | | | | | | |
| Rear Blue | | | | Default | | | |
| Rear Green | | Ctrl panel | Default | | | | |
| Rear Pink | | | | | Default | | |
| Rear Black | | | | | | Default | |
| Rear Orange | | | | | | | Default |

## 1.11.1 Audio Subsystem Software

Audio software and drivers are available from Intel's World Wide Web site.

| For information about | Refer to |
|---|---|
| Obtaining audio software and drivers | Section 1.3, page 14 |

# 1.11.2    Audio Connectors and Headers

The board contains audio connectors and headers on both the back panel and the component side of the board.  The component-side audio headers include the following:

- Front panel audio (a 2 x 5-pin header that provides headphone and mic in signals for front panel audio connectors) (yellow)
- S/PDIF audio header (1 x 4-pin header) (yellow)
- HD Audio Link header

| For information about | Refer to |
| --- | --- |
| The locations of the front panel audio header and S/PDIF header | Figure 10, page 41 |
| The signal names of the front panel audio header | Table 15 and Table 16, page 43 |
| The signal names of the S/PDIF header | Table 14, page 43 |
| The signal names of the HD Audio Link header | Table 17, page 44 |
| The back panel audio connectors | Section 2.2.1, page 40 |

## 1.11.2.1    Back Panel Audio Connectivity

The available configurable back panel audio connectors are shown in Figure 4.
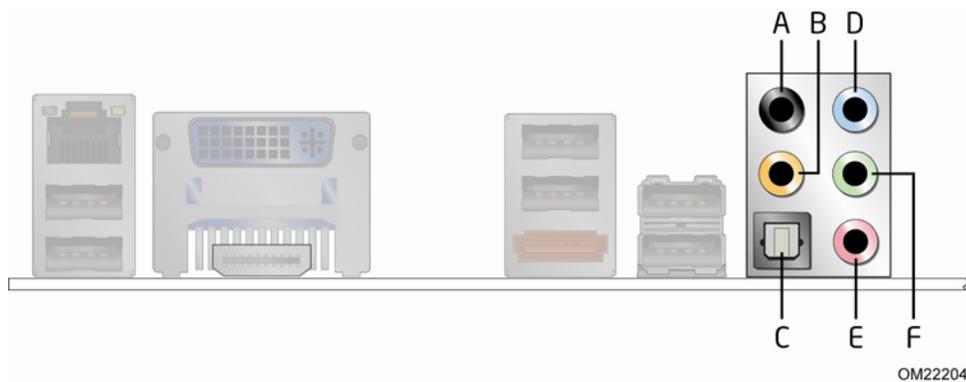


| Item | Description |
| --- | --- |
| A | Rear surround |
| B | Center channel and LFE (subwoofer) |
| C | S/PDIF out (optical) |
| D | Line in |
| E | Mic in/side surround |
| F | Line out/front speakers |

**Figure 4.  Back Panel Audio Connectors**

The back panel audio connectors are configurable through the audio device drivers.

| For information about | Refer to |
|---|---|
| The back panel audio connectors | Section 2.2.1, page 40 |

The front panel headphone output is supported through a separate audio channel pair allowing multi-streaming audio configurations such as simultaneous surround playback and stereo audio conferencing (through back panel speakers and front panel headset, respectively).

## 1.12   LAN Subsystem

The LAN subsystem consists of the following:
- Intel 82578DC Gigabit Ethernet Controller (10/100/1000 Mbits/s)
- RJ-45 LAN connector with integrated status LEDs

The Intel 82578DC Gigabit Ethernet Controller supports the following features:
- 10/100/1000 BASE-T IEEE 802.3 compliant
- PCI Express link
- Compliant to IEEE 802.3x flow control support
- 802.1p and 802.1q
- TCP, IP, and UDP checksum offload (for IPv4 and IPv6)
- Transmit TCP segmentation
- Full device driver compatibility
- PCI Express power management support

LAN software and drivers are available from Intel's World Wide Web site.

| For information about | Refer to |
|---|---|
| Obtaining LAN software and drivers | http://downloadcenter.intel.com |

## 1.12.1 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector (shown in Figure 5).



| Item | Description |
|------|-------------|
| A | Link/Activity LED (green) |
| B | Link Speed LED (green/yellow) |

**Figure 5. LAN Connector LED Locations**

Table 7 describes the LED states when the board is powered up and the LAN subsystem is operating.

**Table 7. LAN Connector LED States**

| LED | LED Color | LED State | Condition |
|-----|-----------|-----------|-----------|
| Link/Activity | Green | Off | LAN link is not established. |
| | | On | LAN link is established. |
| | | Blinking | LAN activity is occurring. |
| Link Speed | Green/Yellow | Off | 10 Mbits/s data rate is selected or negotiated. |
| | | Green | 100 Mbits/s data rate is selected or negotiated. |
| | | Yellow | 1000 Mbits/s data rate is selected or negotiated. |

## 1.13   Real-Time Clock Subsystem

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory.  When the computer is not plugged into a wall socket, the battery has an estimated life of three years.  When the computer is plugged in, the standby current from the power supply extends the life of the battery.

The clock is accurate to $\pm$ 13 minutes/year at 25 ºC with power applied via the power supply 5V STBY rail.

**NOTE**

*If the battery and AC power fail date and time values will be reset and the user will be notified during the POST.*

When the voltage drops below a certain level, the BIOS Setup program settings stored in CMOS RAM (for example, the date and time) might not be accurate.  Replace the battery with an equivalent one.  Figure 1 on page 11 shows the location of the battery.

## 1.14   Hardware Management Subsystem

The hardware management features enable the board to be compatible with the Wired for Management (WfM) specification.  The board has several hardware management features, including the following:

- Hardware monitoring and fan control
- Fan Monitoring
- Chassis intrusion detection
- Thermal monitoring

### 1.14.1   Hardware Monitoring and Fan Control

The features of the hardware monitoring and fan control include:

- Intel Quiet System Technology, delivering acoustically-optimized thermal management
- Thermal sensors in the processor and PCH, as well as near the CPU voltage regulators and system memory
- Monitoring of five system voltages (+5 V, +12 V, +3.3 V, Memory V-SM and +V$_{CCP}$) to detect levels above or below acceptable values
- Thermally monitored closed-loop fan control for all fans that can adjust fan speed as needed

## 1.14.2    Fan Monitoring

Fan monitoring can be observed through the BIOS setup user interface, Intel® Desktop Utilities, or third-party software.

| For information about | Refer to |
|---|---|
| The functions of the fan headers | Section 1.15.2.2, page 32 |

## 1.14.3    Chassis Intrusion Detection

The board supports a chassis security feature that detects if the chassis cover is removed.  The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion header.  When the chassis cover is removed, the mechanical switch is in the closed position.

| For information about | Refer to |
|---|---|
| The location of the chassis intrusion header | Figure 10, page 41 |

## 1.14.4    Thermal Monitoring

Figure 6 shows the locations of the thermal sensors and fan headers.
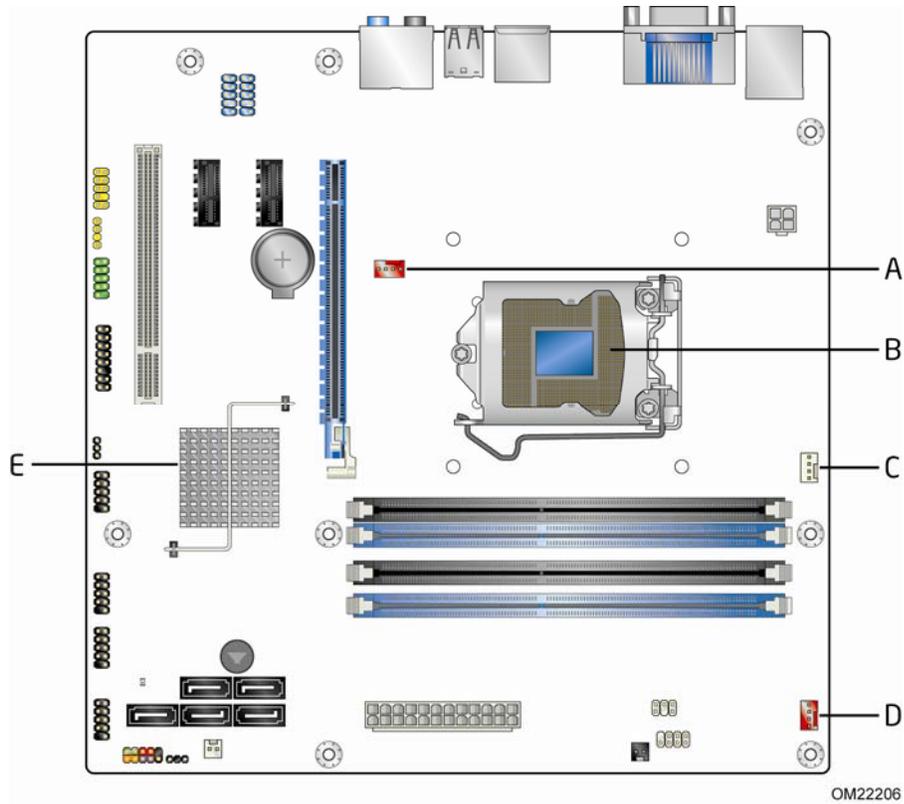


| Item | Description |
|------|-------------|
| A | Rear chassis fan header |
| B | Thermal diode, located on processor die |
| C | Processor fan header |
| D | Front chassis fan header |
| E | Thermal diode, located on the Intel H57 PCH |

**Figure 6.  Thermal Sensors and Fan Headers**

# 1.15  Power Management

Power management is implemented at several levels, including:

- Software support through Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  — Power connector
  — Fan headers
  — LAN wake capabilities
  — Instantly Available PC technology
  — Wake from USB
  — PCI Express WAKE# signal support
  — Wake from serial port
  — Wake from Consumer IR

## 1.15.1  ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer.  The use of ACPI with this board requires an operating system that provides full ACPI support.  ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 15-watt system operation in the power-on/standby sleeping state
- A Soft-off feature that enables the operating system to power-off the computer
- Support for multiple wake-up events (see Table 10 on page 30)
- Support for a front panel power and sleep mode switch

Table 8 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

**Table 8.  Effects of Pressing the Power Switch**

| If the system is in this state… | …and the power switch is pressed for | …the system enters this state |
|---|---|---|
| Off (ACPI G2/G5 – Soft off) | Less than four seconds | Power-on (ACPI G0 – working state) |
| On (ACPI G0 – working state) | Less than four seconds | Soft-off/Standby (note) (ACPI G1 – sleeping state) |
| On (ACPI G0 – working state) | More than six seconds | Fail safe power-off (ACPI G2/G5 – Soft off) |
| Sleep (ACPI G1 – sleeping state) | Less than four seconds | Wake-up (ACPI G0 – working state) |
| Sleep (ACPI G1 – sleeping state) | More than six seconds | Power-off (ACPI G2/G5 – Soft off) |

Note:  System can only enter Standby state if power switch action is properly configured by the operating system.

### 1.15.1.1   System States and Power States

Under ACPI, the operating system directs all system and device power state transitions.  The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications.  Devices that are not being used can be turned off.  The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 9 lists the power states supported by the board along with the associated system power targets.  See the ACPI specification for a complete description of the various system and power states.

**Table 9.  Power States and Targeted System Power**

| Global States | Sleeping States | Processor States | Device States | Targeted System Power (Note 1) |
|---|---|---|---|---|
| G0 – working state | S0 – working | C0 – working | D0 – working state. | Full power > 30 W |
| G1 – sleeping state | S1 – Processor stopped | C1 – stop grant | D1, D2, D3 – device specification specific. | 5 W < power < 52.5 W |
| G1 – sleeping state | S3 – Suspend to RAM.  Context saved to RAM. | No power | D3 – no power except for wake-up logic. | Power < 5 W  (Note 2) |
| G1 – sleeping state | S4 – Suspend to disk.  Context saved to disk. | No power | D3 – no power except for wake-up logic. | Power < 5 W  (Note 2) |
| G2/S5 | S5 – Soft off. Context not saved. Cold boot is required. | No power | D3 – no power except for wake-up logic. | Power < 5 W  (Note 2) |
| G3 – mechanical off  AC power is disconnected from the computer. | No power to the system. | No power | D3 – no power for wake-up logic, except when provided by battery or external source. | No power to the system. Service can be performed safely. |

Notes:

1.   Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.

2.   Dependent on the standby power consumption of wake-up devices used in the system.

## 1.15.1.2    Wake-up Devices and Events

Table 10 lists the devices or specific events that can wake the computer from specific states.

**Table 10.  Wake-up Devices and Events**

| These devices/events can wake up the computer… | …from this state |
| --- | --- |
| Power switch | S1, S3, S4, S5 |
| RTC alarm | S1, S3, S4, S5 |
| LAN | S1, S3, S4, S5 |
| USB | S1, S3 |
| WAKE# signal | S1, S3, S4, S5 |
| Serial | S1, S3 |
| Consumer IR | S3 |

Notes:
- S4 implies operating system support only.
- USB ports are turned off during S4/S5 states.

**NOTE**

*The use of these wake-up events from an ACPI state requires an operating system that provides full ACPI support.  In addition, software, drivers, and peripherals must fully support ACPI wake events.*

## 1.15.2    Hardware Support

⚠ **CAUTION**

*Ensure that the power supply provides adequate +5 V standby current if LAN wake capabilities and Instantly Available PC technology features are used.  Failure to do so can damage the power supply.  The total amount of standby current required depends on the wake devices supported and manufacturing options.*

The board provides several power management hardware features, including:

- Power connector
- Fan headers
- LAN wake capabilities
- Instantly Available PC technology
- Wake from USB
- WAKE# signal wake-up support
- Wake from serial port
- +5 V Standby Power Indicator LED
- Wake from Consumer IR

LAN wake capabilities and Instantly Available PC technology require power from the +5 V standby line.

📝 **NOTE**

*The use of Wake from USB from an ACPI state requires an operating system that provides full ACPI support.*

### 1.15.2.1    Power Connector

ATX12V-compliant power supplies can turn off the system power through system control.  When an ACPI-enabled system receives the correct command, the power supply removes all non-standby voltages.

When resuming from an AC power failure, the computer returns to the power state it was in before power was interrupted (on or off).  The computer's response can be set using the Last Power State feature in the BIOS Setup program's Boot menu.

| For information about | Refer to |
|---|---|
| The location of the main power connector | Figure 10, page 41 |
| The signal names of the main power connector | Table 27, page 47 |

## 1.15.2.2 Fan Headers

The function/operation of the fan headers is as follows:

- The fans are on when the board is in the S0 or S1 state
- The fans are off when the board is in the S3, S4, or S5 state
- Each fan header is wired to a fan tachometer input of the hardware monitoring and fan control ASIC
- All fan headers support closed-loop fan control that can adjust the fan speed or switch the fan on or off as needed
- All fan headers have a +12 V DC connection
- 4-pin fan headers are controlled by Pulse Width Modulation
- The chassis fan headers also support linear fan control on a 3-wire fan

| For information about | Refer to |
|---|---|
| The location of the fan headers | Figure 10, page 41 |
| The location of the fan headers and sensors for thermal monitoring | Figure 6, page 27 |

## 1.15.2.3 LAN Wake Capabilities

⚠ **CAUTION**

*For LAN wake capabilities, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing LAN wake capabilities can damage the power supply.*

LAN wake capabilities enable remote wake-up of the computer through a network. The LAN subsystem monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet* frame, the LAN subsystem asserts a wake-up signal that powers up the computer.

## 1.15.2.4    Instantly Available PC Technology

⚠ **CAUTION**

*For Instantly Available PC technology, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current.  Failure to provide adequate standby current when implementing Instantly Available PC technology can damage the power supply.*

Instantly Available PC technology enables the board to enter the ACPI S3 (Suspend-to-RAM) sleep-state.  While in the S3 sleep-state, the computer will appear to be off (the power supply is off and the front panel power LED will behave as configured by the BIOS "S3 State Indicator" option).  When signaled by a wake-up device or event, the system quickly returns to its last known wake state.  Table 10 on page 30 lists the devices and events that can wake the computer from the S3 state.

The board supports the *PCI Bus Power Management Interface Specification*.  Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

The use of Instantly Available PC technology requires operating system support and PCI 2.3 compliant add-in cards, PCI Express add-in cards, and drivers.

## 1.15.2.5    Wake from USB

USB bus activity wakes the computer from ACPI S1 or S3 states.

📝 **NOTE**

*Wake from USB requires the use of a USB peripheral that supports Wake from USB and is supported by the operating system.*

## 1.15.2.6    WAKE# Signal Wake-up Support

When the WAKE# signal on a PCI Express add-in card is asserted, the computer wakes from an ACPI S1, S3, S4, or S5 state.

## 1.15.2.7    Wake from Serial Port

Serial port activity wakes the computer from an ACPI S1 or S3 state.

## 1.15.2.8    Wake from Consumer IR

CIR activity wakes the computer from an ACPI S3 state.

## 1.15.2.9    +5 V Standby Power Indicator LED

The +5 V standby power indicator LED shows that power is still present even when the computer appears to be off.  Figure 7 shows the location of the standby power indicator LED on the board.



OM22201
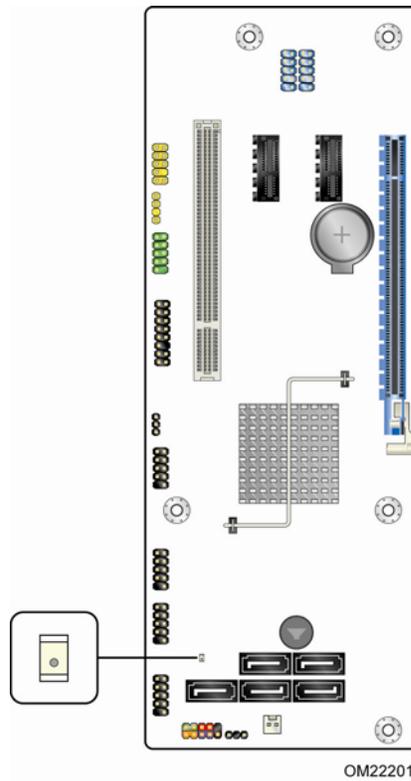
**Figure 7.  Location of the Standby Power LED**

## ⚠ CAUTION

*If AC power has been switched off and the standby power indicators are still lit, disconnect the power cord before installing or removing any devices connected to the board.  Failure to do so could damage the board and any attached devices.*

## 1.15.3    ENERGY STAR* 5.0, E-Standby, and ErP Compliance

The US Department of Energy and the US Environmental Protection Agency have continually revised the ENERGY STAR requirements.  Intel has worked directly with these two governmental agencies in the definition of new requirements.

Intel Desktop Board DH57DD meets the following program requirements in an adequate system configuration, including appropriate selection of an efficient power supply:

- Energy Star v5.0, category B
- EPEAT*
- Korea e-Standby
- European Union Energy-related Products Directive 2009 (ErP)

| For information about | Refer to |
|---|---|
| ENERGY STAR requirements and recommended configurations | http://www.intel.com/go/energystar |
| Electronic Product Environmental Assessment Tool (EPEAT) | http://www.epeat.net/ |
| Korea e-Standby Program | http://www.kemco.or.kr/new_eng/pg02/pg02100300.asp |
| European Union Energy-related Products Directive 2009 (ErP) | http://ec.europa.eu/enterprise/policies/sustainable-business/sustainable-product-policy/ecodesign/index_en.htm |

# 2    Technical Reference

## 2.1    Memory Resources

### 2.1.1    Addressable Memory

The board utilizes 16 GB of addressable system memory.  Typically the address space that is allocated for Conventional PCI  bus add-in cards, PCI Express configuration space, BIOS (SPI Flash device), and chipset overhead resides above the top of DRAM (total system memory).  On a system that has 16 GB of system memory installed, it is not possible to use all of the installed memory due to system address space being allocated for other system critical functions.  These functions include the following:

- BIOS/SPI Flash device (64 Mbit)
- Local APIC (19 MB)
- Direct Media Interface (40 MB)
- PCI Express configuration space (256 MB)
- PCH base address registers and PCI Express ports (up to 256 MB)
- Memory-mapped I/O that is dynamically allocated for Conventional PCI bus and PCI Express add-in cards (256 MB)

The board provides the capability to reclaim the physical memory overlapped by the memory mapped I/O logical address space.  The board remaps physical memory from the top of usable DRAM boundary to the 4 GB boundary to an equivalent sized logical address range located just above the 4 GB boundary.  Figure 8 shows a schematic of the system memory map.  All installed system memory can be used when there is no overlap of system addresses.
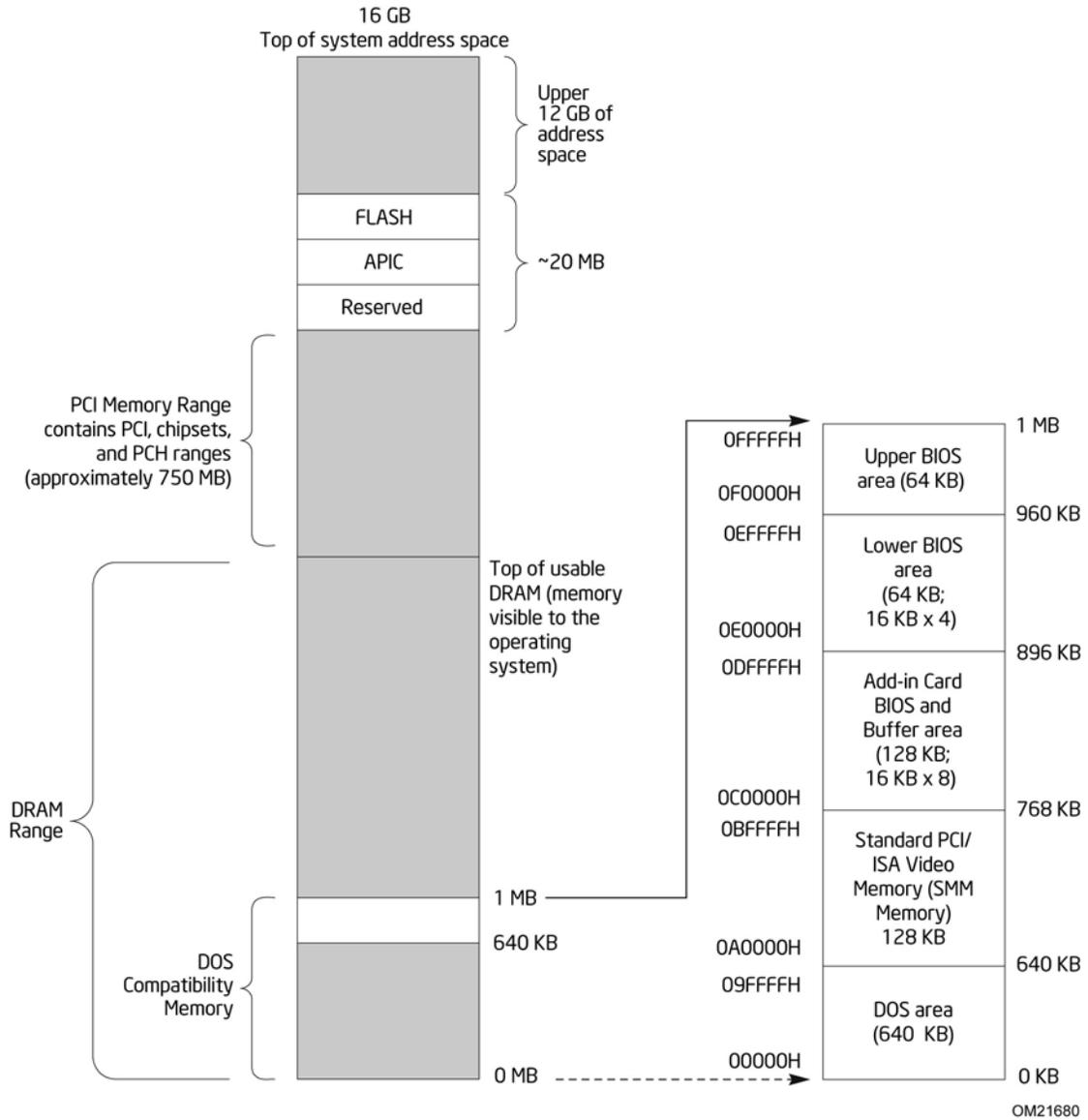
**Figure 8.  Detailed System Memory Address Map**

## 2.1.2    Memory Map

Table 11 lists the system memory map.

**Table 11.  System Memory Map**

| Address Range (decimal) | Address Range (hex) | Size | Description |
|---|---|---|---|
| 1024 K - 16777216 K | 100000 - 3FFFFFFFF | 16382 MB | Extended memory |
| 960 K - 1024 K | F0000 - FFFFF | 64 KB | Runtime BIOS |
| 896 K - 960 K | E0000 - EFFFF | 64 KB | Reserved |
| 800 K - 896 K | C8000 - DFFFF | 96 KB | Potential available high DOS memory (open to the Conventional PCI bus).  Dependent on video adapter used. |
| 640 K - 800 K | A0000 - C7FFF | 160 KB | Video memory and BIOS |
| 639 K - 640 K | 9FC00 - 9FFFF | 1 KB | Extended BIOS data (movable by memory manager software) |
| 512 K - 639 K | 80000 - 9FBFF | 127 KB | Extended conventional memory |
| 0 K - 512 K | 00000 - 7FFFF | 512 KB | Conventional memory |

# 2.2    Connectors and Headers

⚠ **CAUTION**

*Only the following connectors and headers have overcurrent protection:  back panel and front panel USB, and IEEE 1394a.*

*The other internal connectors and headers are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals.  Do not use these connectors or headers to power devices external to the computer's chassis.  A fault in the load presented by the external devices could cause damage to the computer, the power cable, and the external devices themselves.*

*Furthermore, improper connection of USB header single wire connectors may eventually overload the overcurrent protection and cause damage to the board.*

This section describes the board's connectors.  The connectors can be divided into these groups:

- Back panel I/O connectors
- Component-side I/O connectors and headers (see page 41)

## 2.2.1 Back Panel Connectors

Figure 9 shows the location of the back panel connectors for the board.
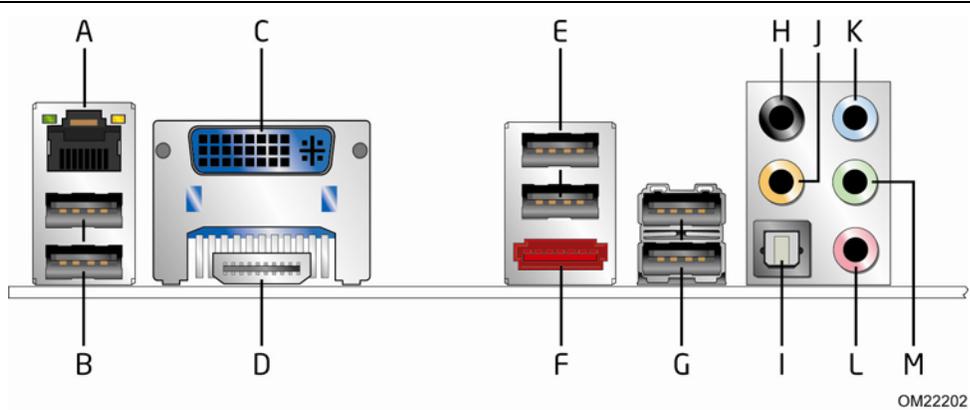


| Item | Description |
| --- | --- |
| A | LAN |
| B | USB ports |
| C | DVI-I connector |
| D | HDMI connector |
| E | USB ports |
| F | eSATA connector |
| G | USB ports |
| H | Rear surround |
| I | S/PDIF out (optical) |
| J | Center channel and LFE (subwoofer) |
| K | Line in |
| L | Mic in/side surround |
| M | Line out/front speakers |

**Figure 9.  Back Panel Connectors**

**NOTE**

*The back panel audio line out connector is designed to power headphones or amplified speakers only.  Poor audio quality occurs if passive (non-amplified) speakers are connected to this output.*

## 2.2.2 Component-side Connectors and Headers

Figure 10 shows the locations of the component-side connectors and headers.
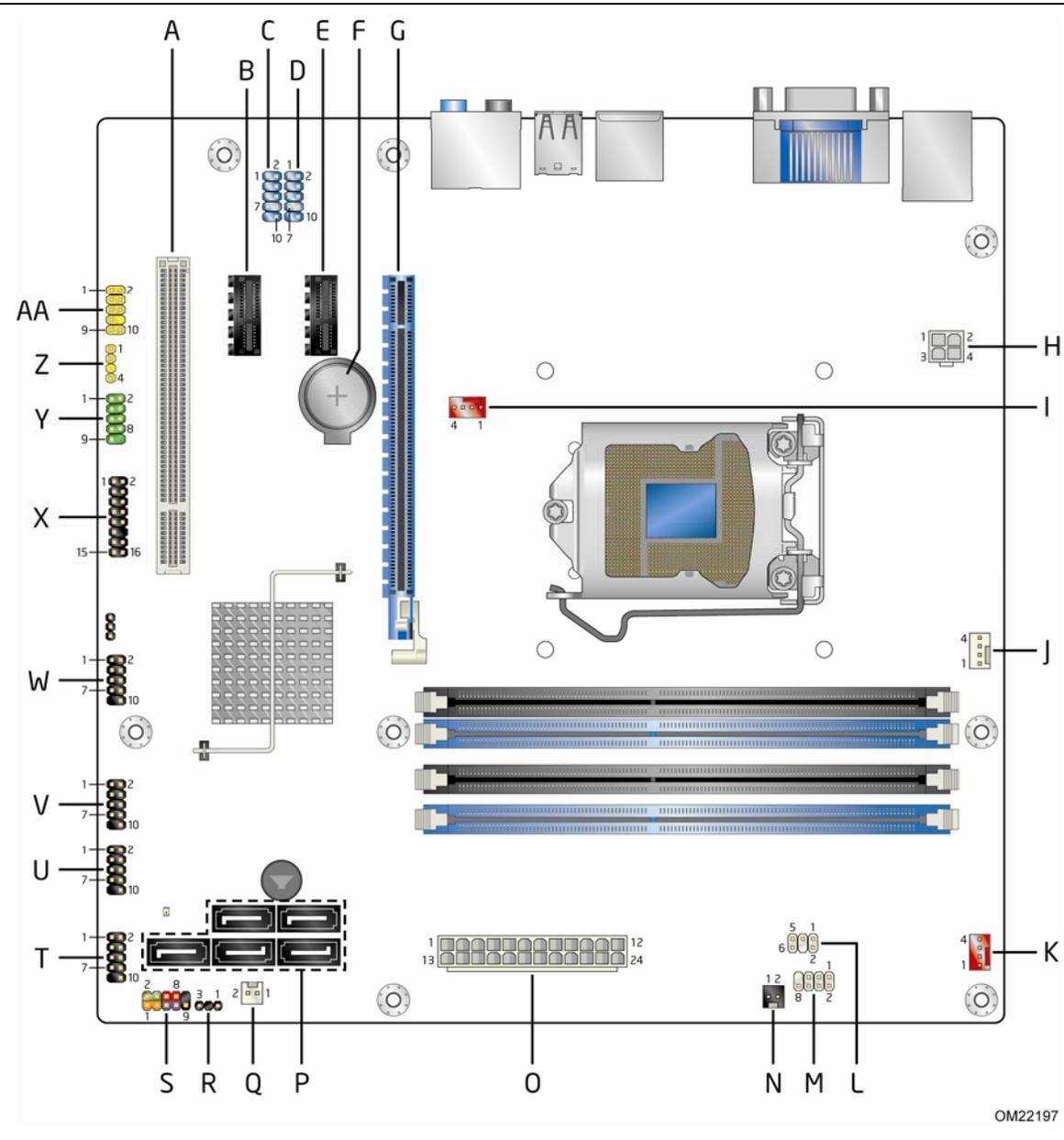


**Figure 10.  Component-side Connectors and Headers**

Table 12 lists the component-side connectors and headers identified in Figure 10.

**Table 12.  Component-side Connectors and Headers Shown in Figure 10**

| Item/callout from Figure 10 | Description |
| --- | --- |
| A | Conventional PCI bus add-in card connector |
| B | PCI Express x1 add-in card connector |
| C | Front panel IEEE 1394a header |
| D | Front panel IEEE 1394a header |
| E | PCI Express x1 add-in card connector |
| F | Battery |
| G | PCI Express x16 add-in card connector |
| H | Processor core power connector (2 x 2) |
| I | Rear chassis fan header |
| J | Processor fan header |
| K | Front chassis fan header |
| L | Consumer IR receiver (input) header |
| M | Consumer IR emitter (output) header |
| N | Chassis intrusion header |
| O | Main power connector (2 x 12) |
| P | SATA connectors |
| Q | Intel Remote Assist PC header |
| R | Alternate front panel power LED header |
| S | Front panel header |
| T | Front panel USB header |
| U | Front panel USB header |
| V | Front panel USB header |
| W | Front panel USB header |
| X | Intel High Definition Audio Link header |
| Y | Serial port header |
| Z | S/PDIF header |
| AA | Front panel audio header |

## 2.2.2.1    Signal Tables for the Connectors and Headers

**Table 13.  Serial Port Header**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | DCD (Data Carrier Detect) | 2 | RXD# (Receive Data) |
| 3 | TXD# (Transmit Data) | 4 | DTR (Data Terminal Ready) |
| 5 | Ground | 6 | DSR (Data Set Ready) |
| 7 | RTS (Request To Send) | 8 | CTS (Clear To Send) |
| 9 | RI (Ring Indicator) | 10 | Key (no pin) |

**Table 14.  S/PDIF Header**

| Pin | Signal Name |
|---|---|
| 1 | Ground |
| 2 | S/PDIF out |
| 3 | Key (no pin) |
| 3 | +5V_DC |

**Table 15.  Front Panel Audio Header for Intel HD Audio**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | [Port 1] Left channel | 2 | Ground |
| 3 | [Port 1] Right channel | 4 | PRESENCE# (HD Audio/AC '97 detect) |
| 5 | [Port 2] Right channel | 6 | [Port 1] SENSE_RETURN |
| 7 | SENSE_SEND (Jack detection) | 8 | Key (no pin) |
| 9 | [Port 2] Left channel | 10 | [Port 2] SENSE_RETURN |

**Table 16.  Front Panel Audio Header for Passive AC '97 Audio**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | MIC | 2 | AUD_GND |
| 3 | MIC_BIAS | 4 | PRESENCE# (HD Audio/AC '97 detect) |
| 5 | FP_OUT_R | 6 | AUD_GND |
| 7 | NC (no connect) | 8 | KEY (no pin) |
| 9 | FP_OUT_L | 10 | AUD_GND |

**Table 17. Intel HD Audio Link Header**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | BCLK | 2 | Ground |
| 3 | RST# | 4 | DVDD IO |
| 5 | SYNC | 6 | Ground |
| 7 | SDO | 8 | 3.3 V DVDD CORE |
| 9 | SDI0 | 10 | +12 V |
| 11 | SDI1 | 12 | Key (no pin) |
| 13 | Not connected | 14 | 3.3 V DUAL |
| 15 | Not connected | 16 | Ground |

**Table 18. Front Panel USB Headers**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | +5 VDC | 2 | +5 VDC |
| 3 | D- | 4 | D- |
| 5 | D+ | 6 | D+ |
| 7 | Ground | 8 | Ground |
| 9 | KEY (no pin) | 10 | No Connect |

**Table 19. SATA Connectors**

| Pin | Signal Name |
|---|---|
| 1 | Ground |
| 2 | TXP |
| 3 | TXN |
| 4 | Ground |
| 5 | RXN |
| 6 | RXP |
| 7 | Ground |

**Table 20. Chassis Intrusion Header**

| Pin | Signal Name |
|---|---|
| 1 | Intruder# |
| 2 | Ground |

**Table 21.  Processor (4-Pin) Fan Header**

| Pin | Signal Name |
|-----|-------------|
| 1 | Ground |
| 2 | +12 V |
| 3 | FAN_TACH |
| 4 | FAN_CONTROL |

**Table 22.  Front and Rear Chassis Fan Headers**

| Pin | 4-Wire Support | Pin | 3-Wire Support |
|-----|----------------|-----|----------------|
| 1 | Ground | 3 | Ground |
| 2 | Fan power | 2 | Fan power |
| 3 | Fan tach | 1 | Fan tach |
| 4 | Fan control | N/A | N/A |

**Table 23.  Intel Remote PC Assist Technology Header**

| Pin | Signal Name |
|-----|-------------|
| 1 | RPAT# |
| 2 | Ground |

**Table 24.  Back Panel CIR Emitter (Output) Header**

| Pin | Signal Name |
|-----|-------------|
| 1 | Emitter out 1 |
| 2 | Emitter out 2 |
| 3 | Ground |
| 4 | Key (no pin) |
| 5 | Jack detect 1 |
| 6 | Jack detect 2 |

**Table 25.  Front Panel CIR Receiver (Input) Header**

| Pin | Signal Name |
|-----|-------------|
| 1 | Ground |
| 2 | LED |
| 3 | NC |
| 4 | Learn in |
| 5 | 5 V standby |
| 6 | VCC |
| 7 | Key (no pin) |
| 8 | CIR input |

## 2.2.2.2    Add-in Card Connectors

The board has one PCI Express 2.0 x16 connector.  This connector supports simultaneous transfer speeds of up to 8 GB/s of peak bandwidth.

## 2.2.2.3    Power Supply Connectors

The board has the following power supply connectors:

- **Main power** – a 2 x 12 connector.  This connector is compatible with 2 x 10 connectors previously used on Intel Desktop boards.  The board supports the use of ATX12V power supplies with either 2 x 10 or 2 x 12 main power cables.  When using a power supply with a 2 x 10 main power cable, pins 11, 12, 23, and 24 must remain unconnected.
- **Processor core power** – a 2 x 2 connector.  This connector provides power directly to the processor voltage regulator and must always be used.  Failure to do so will prevent the board from booting.

## ⚠ CAUTION

*If a high power (75 W or greater) add-in card is installed in the PCI Express x16 connector, that card must also be connected directly to the power supply.  Failure to do so may cause damage to the board and the add-in card.*

**Table 26.  Processor Core Power Connector**

| Pin | Signal Name | Pin | Signal Name |
| --- | --- | --- | --- |
| 1 | Ground | 2 | Ground |
| 3 | +12 V | 4 | +12 V |

**Table 27.  Main Power Connector**

| Pin | Signal Name | Pin | Signal Name |
|-----|-------------|-----|-------------|
| 1 | +3.3 V | 13 | +3.3 V |
| 2 | +3.3 V | 14 | −12 V |
| 3 | Ground | 15 | Ground |
| 4 | +5 V | 16 | PS-ON# (power supply remote on/off) |
| 5 | Ground | 17 | Ground |
| 6 | +5 V | 18 | Ground |
| 7 | Ground | 19 | Ground |
| 8 | PWRGD (Power Good) | 20 | −5 V (obsolete) |
| 9 | +5 V (Standby) | 21 | +5 V |
| 10 | +12 V | 22 | +5 V |
| 11 | +12 V (Note) | 23 | +5 V (Note) |
| 12 | +3.3 V 2 x 12 connector detect (Note) | 24 | Ground (Note) |

Note:  When using a 2 x 10 power supply cable, this pin will be unconnected.

| For information about | Refer to |
|-----------------------|----------|
| Power supply considerations | Section 2.5.1 on page 54 |

## 2.2.2.4    Front Panel Header

This section describes the functions of the front panel header.  Table 28 lists the signal names of the front panel header.  Figure 11 is a connection diagram for the front panel header.

**Table 28.  Front Panel Header**

| Pin | Signal | In/Out | Description | Pin | Signal | In/Out | Description |
|---|---|---|---|---|---|---|---|
| Hard Drive Activity LED | | | | Power LED | | | |
| 1 | HD_PWR | Out | Hard disk LED pull-up to +5 V | 2 | FP_LED+ | Out | Front panel green LED |
| 3 | HDA# | Out | Hard disk active LED | 4 | FP_LED− | Out | Front panel yellow LED |
| Reset Switch | | | | On/Off Switch | | | |
| 5 | Ground | | Ground | 6 | PWR# | In | Power switch |
| 7 | FP_RESET# | In | Reset switch | 8 | Ground | | Ground |
| Power | | | | Not Connected | | | |
| 9 | +5 V | | Power | 10 | N/C | | Not connected |
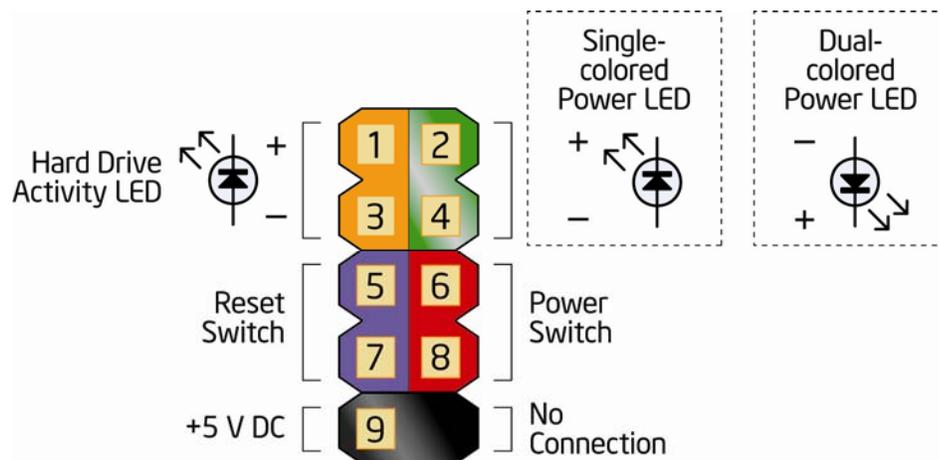


**Figure 11.  Connection Diagram for Front Panel Header**

### 2.2.2.4.1    Hard Drive Activity LED Header

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to an internal storage device.  Proper LED function requires a SATA hard drive or optical drive connected to an onboard SATA connector.

**2.2.2.4.2        Reset Switch Header**

Pins 5 and 7 can be connected to a momentary single pole, single throw (SPST) type switch that is normally open.  When the switch is closed, the board resets and runs the POST.

**2.2.2.4.3        Power LED Header**

Pins 2 and 4 can be connected to a one- or two-color LED.  Table 29 shows the default states for this LED.  More options are available through BIOS setup.

**Table 29.  States for a One-Color Power LED**

| LED State | Description |
|-----------|-------------|
| Off | Power off/sleeping |
| Steady Lit | Running |
| Blink | Standby |

**2.2.2.4.4        Power Switch Header**

Pins 6 and 8 can be connected to a front panel momentary-contact power switch.  The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off.  (The time requirement is due to internal debounce circuitry on the board.)  At least two seconds must pass before the power supply will recognize another on/off signal.

## 2.2.2.5     Alternate Front Panel Power LED Header

Pins 1 and 3 of this header duplicate the signals on pins 2 and 4 of the front panel header.

**Table 30.  Alternate Front Panel Power LED Header**

| Pin | Signal Name | In/Out | Description |
|-----|-------------|--------|-------------|
| 1 | FP_LED+ | Out | FP_LED+ |
| 2 | Not connected | | |
| 3 | FP_LED− | Out | FP_LED− |

## 2.2.2.6 Front Panel USB Headers

Figure 12 is a connection diagram for the front panel USB headers.

📝 **NOTE**
- *The +5 V DC power on the USB headers is fused.*
- *Use only a front panel USB connector that conforms to the USB 2.0 specification for high-speed USB devices.*
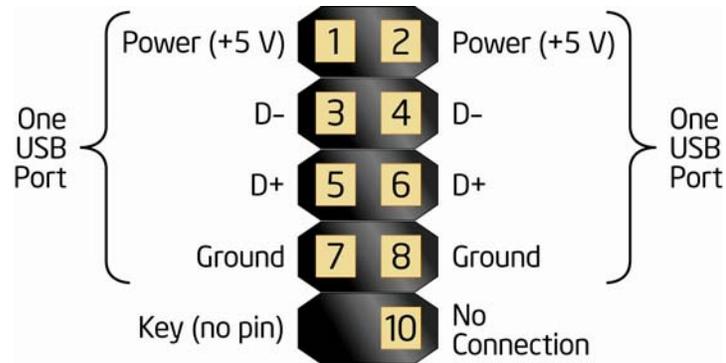


**Figure 12. Connection Diagram for Front Panel USB Headers**

## 2.2.2.7 Front Panel IEEE 1394a Header

Figure 13 is a connection diagram for the IEEE 1394a header.

📝 **NOTE**
- *The +12 V DC power on the IEEE 1394a header is fused.*
- *The IEEE 1394a header provides one IEEE 1394a port.*
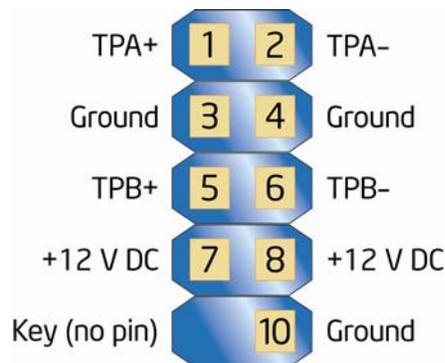


**Figure 13. Connection Diagram for IEEE 1394a Header**

## 2.3    Jumper Block

⚠ **CAUTION**

*Do not move the jumper with the power on.  Always turn off the power and unplug the power cord from the computer before changing a jumper setting.  Otherwise, the board could be damaged.*

Figure 14 shows the location of the jumper block.  The 3-pin jumper block determines the BIOS Setup program's mode.  Table 31 describes the jumper settings for the three modes:  normal, configure, and recovery.
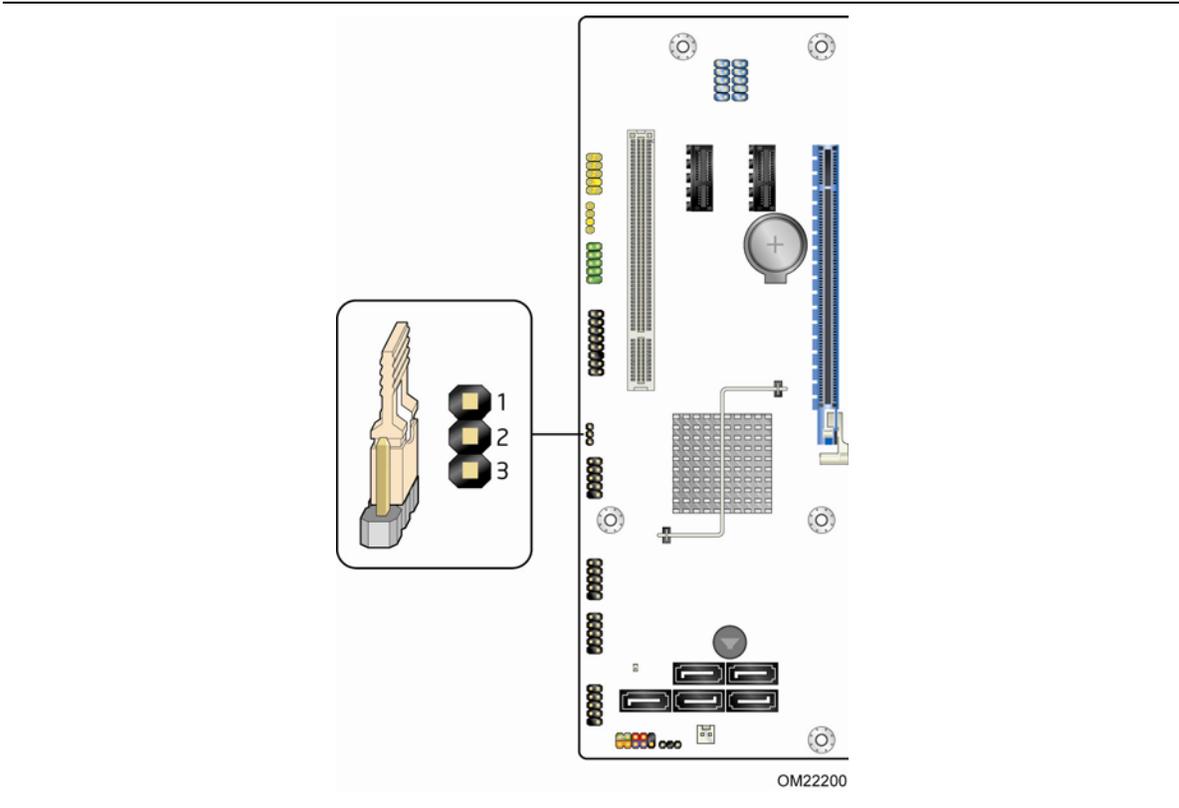


**Figure 14.  Location of the Jumper Block**

**Table 31.  BIOS Setup Configuration Jumper Settings**

| Function/Mode | Jumper Setting | | Configuration |
|---|---|---|---|
| Normal | 1-2 | | The BIOS uses current configuration information and passwords for booting. |
| Configure | 2-3 | | After the POST runs, Setup runs automatically.  The maintenance menu is displayed.<br><br>Note that this Configure mode is the only way to clear the BIOS/CMOS settings.  Press F9 (restore defaults) while in Configure mode to restore the BIOS/CMOS settings to their default values. |
| Recovery | None | | The BIOS attempts to recover the BIOS configuration.  A recovery CD or USB flash drive is required. |
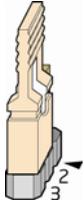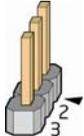
# 2.4 Mechanical Considerations

## 2.4.1 Form Factor

The board is designed to fit into a microATX form-factor chassis. Figure 15 illustrates the mechanical form factor for the board. Dimensions are given in inches [millimeters]. The outer dimensions are 9.6 inches by 9.6 inches [243.84 millimeters by 243.84 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the ATX specification.
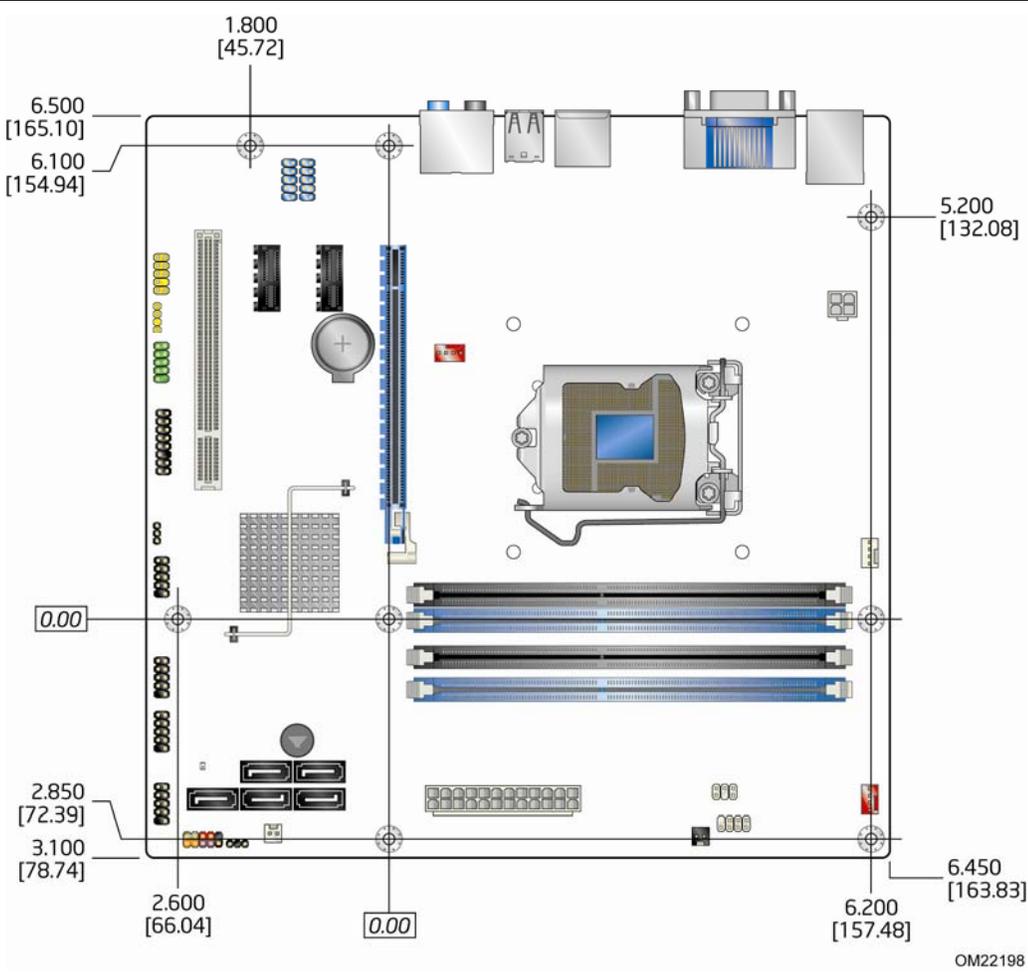


**Figure 15. Board Dimensions**

# 2.5 Electrical Considerations

## 2.5.1 Power Supply Considerations

⚠️ **CAUTION**

*The +5 V standby line from the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.*

Additional power required will depend on configurations chosen by the integrator.

The power supply must comply with the indicated parameters of the ATX form factor specification.

- The potential relation between 3.3 VDC and +5 VDC power rails
- The current capability of the +5 VSB line
- All timing parameters
- All voltage tolerances

For example, for a system consisting of a supported 87 W TDP processor (see Section 1.4 on page 14 for information on supported processors), up to 16 GB DDR3 memory, integrated graphics, one hard disk drive, one optical drive, and all board peripherals enabled, the minimum recommended power supply is about 260 W with current ratings as listed in Table 32

**Table 32. Recommended Power Supply Current Values**

| Output Voltage | 3.3 V | 5 V | 12 V1 | 12 V2 | -12 V | 5 VSB |
|---|---|---|---|---|---|---|
| **Current** | 12 A | 18 A | 14 A | 16 A | 0.3 A | 2 A |

📝 **NOTE**

*+12 V1 denotes the 12 V rail at the 2 x 12 power connector.*

*+12 V2 denotes the 12 V rail at the 2 x 2 power connector.*

| For information about | Refer to |
|---|---|
| Selecting an appropriate power supply | http://www.intel.com/support/motherboards/desktop/sb/CS-026472.htm |

## 2.5.2 Fan Header Current Capability

⚠ **CAUTION**

*The processor fan must be connected to the processor fan header, not to a chassis fan header. Connecting the processor fan to a chassis fan header may result in onboard component damage that will halt fan operation.*

Table 33 lists the current capability of the fan headers.

**Table 33. Fan Header Current Capability**

| Fan Header | Maximum Available Current |
|---|---|
| Processor fan | 2.0 A |
| Front chassis fan | 1.5 A |
| Rear chassis fan | 1.5 A |

## 2.5.3 Add-in Board Considerations

The board is designed to provide 2 A (average) of current for each add-in board from the +5 V rail. The total +5 V current draw for add-in boards for a fully loaded board (all expansion slots filled) must not exceed the system's power supply +5 V maximum current.

# 2.6     Thermal Considerations

⚠ **CAUTION**

*Use of a processor heat sink that provides omni-directional airflow to maintain required airflow across the processor voltage regulator area is highly recommended.*

⚠ **CAUTION**

*Failure to ensure appropriate airflow may result in reduced performance of both the processor and/or voltage regulator or, in some instances, damage to the board.  For a list of chassis that have been tested with Intel desktop boards please refer to the following website:*

*http://www3.intel.com/cd/channel/reseller/asmo-na/eng/tech_reference/53211.htm*

*All responsibility for determining the adequacy of any thermal or system design remains solely with the reader.  Intel makes no warranties or representations that merely following the instructions presented in this document will result in a system with adequate thermal performance.*

⚠ **CAUTION**

*The ambient temperature must not exceed the board's maximum operating temperature.  Failure to do so could cause components to exceed their maximum case temperature and malfunction.  For information about the maximum operating temperature, see the environmental specifications in Section 2.8.*

⚠ **CAUTION**

*Ensure that proper airflow is maintained in the processor voltage regulator circuit. Failure to do so may result in damage to the voltage regulator circuit.*

Figure 16 shows the locations of the localized high temperature zones.



OM22199
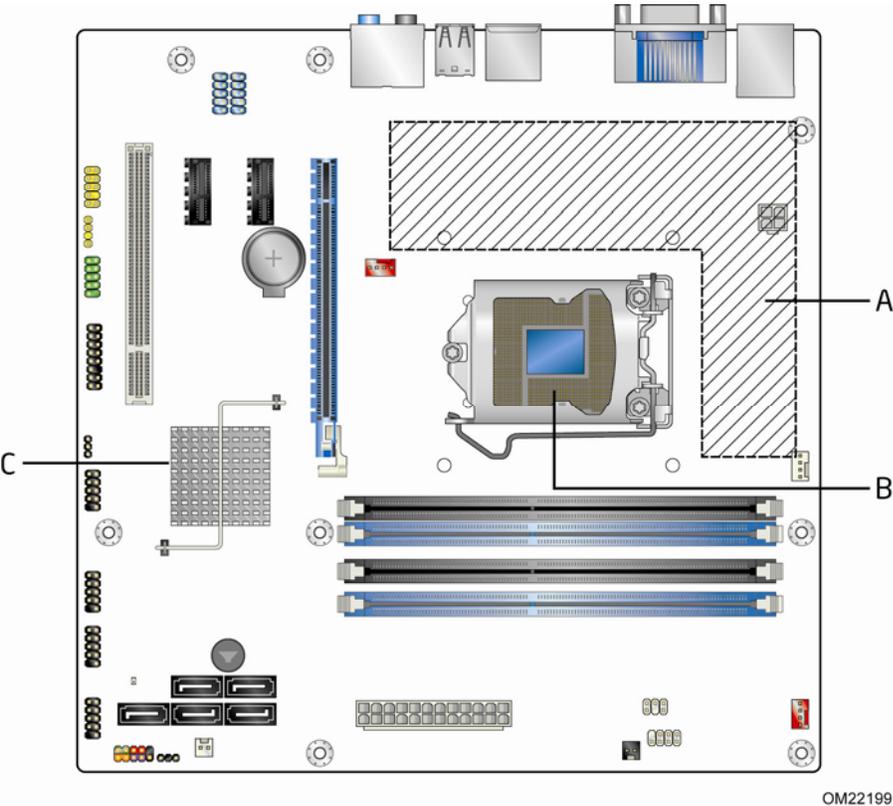
| Item | Description |
|------|-------------|
| A | Processor voltage regulator area |
| B | LGA1156 processor socket |
| C | Intel H57 Express Chipset |

**Figure 16.  Localized High Temperature Zones**

Table 34 provides maximum case temperatures for the components that are sensitive to thermal changes. The operating temperature, current load, or operating frequency could affect case temperatures. Maximum case temperatures are important when considering proper airflow to cool the board.

**Table 34. Thermal Considerations for Components**

| Component | Maximum Case Temperature |
|---|---|
| Processor | For processor case temperature, see processor datasheets and processor specification updates |
| Intel H57 Express Chipset | 111 ºC |

To ensure functionality and reliability, the component is specified for proper operation when Case Temperature is maintained at or below the maximum temperature listed in Table 34. This is a requirement for sustained power dissipation equal to Thermal Design Power (TDP is specified as the maximum sustainable power to be dissipated by the components). When the component is dissipating less than TDP, the case temperature should be below the Maximum Case Temperature. The surface temperature at the geometric center of the component corresponds to Case Temperature.

It is important to note that the temperature measurement in the system BIOS is a value reported by embedded thermal sensors in the components and does not directly correspond to the Maximum Case Temperature. The upper operating limit when monitoring this thermal sensor is Tcontrol, as shown in Table 35.

**Table 35. Tcontrol Values for Components**

| Component | Tcontrol |
|---|---|
| Processor | For processor case temperature, see processor datasheets and processor specification updates |
| Intel H57 Express Chipset | 107 ºC |

| For information about | Refer to |
|---|---|
| Processor datasheets and specification updates | Section 1.3, page 14 |

# 2.7    Reliability

The Mean Time Between Failures (MTBF) prediction is calculated using component and subassembly random failure rates.  The calculation is based on the Telcordia SR-332, Method I Case 1 50% electrical stress, 40 ⁰C ambient.  The MTBF prediction is used to estimate repair rates and spare parts requirements.

The MTBF data is calculated from predicted data at 50 ⁰C.  The MTBF for the board is 165,378 hours.

# 2.8    Environmental

Table 36 lists the environmental specifications for the board.

**Table 36.  Environmental Specifications**

| Parameter | Specification | | |
|---|---|---|---|
| **Temperature** | | | |
| Non-Operating | -40 °C to +60 °C | | |
| Operating | 0 °C to +40 °C | | |
| **Shock** | | | |
| Unpackaged | 50 g trapezoidal waveform | | |
| | Velocity change of 170 inches/second² | | |
| Packaged | Half sine 2 millisecond | | |
| | Product Weight (pounds) | Free Fall (inches) | Velocity Change (inches/sec²) |
| | <20 | 36 | 167 |
| | 21-40 | 30 | 152 |
| | 41-80 | 24 | 136 |
| | 81-100 | 18 | 118 |
| **Vibration** | | | |
| Unpackaged | 5 Hz to 20 Hz:  0.01 g² Hz sloping up to 0.02 g² Hz | | |
| | 20 Hz to 500 Hz:  0.02 g² Hz (flat) | | |
| Packaged | 5 Hz to 40 Hz:  0.015 g² Hz (flat) | | |
| | 40 Hz to 500 Hz:  0.015 g² Hz sloping down to 0.00015 g² Hz | | |

# 3 Overview of BIOS Features

## 3.1 Introduction

The board uses an Intel BIOS that is stored in a 64 Mbit (8,192 KB) Serial Peripheral Interface Flash Memory (SPI Flash) device which can be updated using a set of utilities. The SPI Flash contains the BIOS Setup program, POST, LAN EEPROM information, Plug and Play support, and other firmware.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOSs are identified as JGIBX10J.86A.

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

| Maintenance | Main | Advanced | Performance | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|---|

**NOTE**

*The maintenance menu is displayed only when the board is in Maintenance mode. Section 2.3 on page 51 shows how to put the board in Maintenance mode.*

Table 37 lists the BIOS Setup program menu features.

**Table 37.  BIOS Setup Program Menu Bar**

| Maintenance | Main | Advanced | Performance | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|---|
| Clears passwords and displays processor information | Displays processor and memory configuration | Configures advanced features available through the chipset | Configures Memory and Processor overrides | Sets passwords and security features | Configures power management features | Selects boot options | Saves or discards changes to Setup program options |

Table 38 lists the function keys available for menu screens.

**Table 38.  BIOS Setup Program Function Keys**

| BIOS Setup Program Function Key | Description |
|---|---|
| <←> or <→> | Selects a different menu screen (Moves the cursor left or right) |
| <↑> or <↓> | Selects an item (Moves the cursor up or down) |
| <Tab> | Selects sub-items within a field (i.e., date/time) |
| <Enter> | Executes command or selects the submenu |
| <F9> | Load the default configuration values for the current menu |
| <F10> | Save the current values and exits the BIOS Setup program |
| <Esc> | Exits the menu |

## 3.2    System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components.  Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components.  The MIF database defines the data and provides the method for accessing this information.  The BIOS enables applications such as third-party management software to use SMBIOS.  The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems require an additional interface for obtaining the SMBIOS information.  The BIOS supports an SMBIOS table interface for such operating systems.  Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.  Additional board information can be found in the BIOS under the Additional Information header under the Main BIOS page.

## 3.3    Legacy USB Support

Legacy USB support enables USB devices to be used even when the operating system's USB drivers are not yet available.  Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB.  By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads.  While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system.  (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

## 3.4     BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel World Wide Web site:

- Intel® Express BIOS Update utility, which enables automated updating while in the Windows environment.  Using this utility, the BIOS can be updated from a file on a hard disk, a USB drive (a flash drive or a USB drive), or an optical drive.
- Intel® Flash Memory Update Utility, which requires booting from DOS.  Using this utility, the BIOS can be updated from a file on a hard disk, a USB drive (a flash drive or a USB drive), or an optical drive.
- Intel® F7 switch allows a user to select where the BIOS .bio file is located and perform the update from that location/device.  Similar to performing a BIOS Recovery without removing the BIOS configuration jumper.

Both utilities verify that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.

### NOTE

*Review the instructions distributed with the upgrade utility before attempting a BIOS update.*

| For information about | Refer to |
| --- | --- |
| BIOS update utilities | http://www.intel.com/support/motherboards/desktop/sb/CS-022312.htm. |

## 3.4.1     Language Support

The BIOS Setup program and help messages are supported in US English.  Check the Intel web site for support.

## 3.4.2    Custom Splash Screen

During POST, an Intel® splash screen is displayed by default.  This splash screen can be augmented with a custom splash screen.  The Intel Integrator's Toolkit that is available from Intel can be used to create a custom splash screen.

| For information about | Refer to |
|---|---|
| Intel® Integrator Toolkit | http://developer.intel.com/design/motherbd/software/itk/ |
| Additional Intel® software tools | http://developer.intel.com/products/motherboard/DH57DD/tools.htm<br>and<br>http://developer.intel.com/design/motherbd/software.htm |

# 3.5    BIOS Recovery

It is unlikely that anything will interrupt a BIOS update; however, if an interruption occurs, the BIOS could be damaged.  Table 39 lists the drives and media types that can and cannot be used for BIOS recovery.  The BIOS recovery media does not need to be made bootable however, it must contain the motherboard .bio file at the root level.

**Table 39.  Acceptable Drives/Media Types for BIOS Recovery**

| Media Type | Can be used for BIOS recovery? |
|---|---|
| Optical drive connected to the SATA interface | Yes |
| USB removable drive (a USB Flash Drive, for example) | Yes |
| USB diskette drive (with a 1.44 MB diskette) | No |
| USB hard disk drive | No |
| Legacy diskette drive (with a 1.44 MB diskette) connected to the legacy diskette drive interface | No |

| For information about | Refer to |
|---|---|
| BIOS recovery | http://www.intel.com/support/motherboards/desktop/sb/cs-023360.htm |

# 3.6    Boot Options

In the BIOS Setup program, the user can choose to boot from a hard drive, optical drive, removable drive, or the network.  The default setting is for the optical drive to be the first boot device, the hard drive second, removable drive third, and the network fourth.

## 3.6.1    Optical Drive Boot

Booting from the optical drive is supported in compliance to the El Torito bootable CD-ROM format specification.  Under the Boot menu in the BIOS Setup program, the optical drive is listed as a boot device.  Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the optical drive, the system will attempt to boot from the next defined drive.

## 3.6.2    Network Boot

The network can be selected as a boot device.  This selection allows booting from the onboard LAN or a network add-in card with a remote boot ROM installed.

Pressing the <F12> key during POST automatically forces booting from the LAN.  To use this key during POST, the User Access Level in the BIOS Setup program's Security menu must be set to Full.

## 3.6.3    Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

## 3.6.4    Changing the Default Boot Device During POST

Pressing the <F10> key during POST causes a boot device menu to be displayed.  This menu displays the list of available boot devices.  Table 40 lists the boot device menu options.

**Table 40.  Boot Device Menu Options**

| Boot Device Menu Function Keys | Description |
| --- | --- |
| <↑> or <↓> | Selects a default boot device |
| <Enter> | Exits the menu, and boots from the selected device |
| <Esc> | Exits the menu and boots according to the boot priority defined through BIOS setup |

## 3.7    BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer.  A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program.  This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program.  This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup.  Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer.  The password prompt will be displayed before the computer is booted.  If only the supervisor password is set, the computer boots without asking for a password.  If both passwords are set, the user can enter either password to boot the computer.
- For enhanced security, use different passwords for the supervisor and user passwords.
- Valid password characters are A-Z, a-z, and 0-9.  Passwords may be up to 16 characters in length.

Table 41 shows the effects of setting the supervisor password and user password.  This table is for reference only and is not displayed on the screen.

**Table 41.  Supervisor and User Password Functions**

| Password Set | Supervisor Mode | User Mode | Setup Options | Password to Enter Setup | Password During Boot |
|---|---|---|---|---|---|
| Neither | Can change all options (Note) | Can change all options (Note) | None | None | None |
| Supervisor only | Can change all options | Can change a limited number of options | Supervisor Password | Supervisor | None |
| User only | N/A | Can change all options | Enter Password Clear User Password | User | User |
| Supervisor and user set | Can change all options | Can change a limited number of options | Supervisor Password Enter Password | Supervisor or user | Supervisor or user |

Note:    If no password is set, any user can change all Setup options.

# 4 Error Messages and Beep Codes

## 4.1 Speaker

The board-mounted piezo speaker provides audible error code (beep code) information during POST.

| For information about | Refer to |
|---|---|
| The location of the onboard speaker | Figure 1, page 11 |

## 4.2 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS causes the board's piezo speaker to beep an error message describing the problem (see Table 42).

**Table 42. BIOS Beep Codes**

| Type | Pattern | Frequency/Comments |
|---|---|---|
| F2 Setup/F10 Boot Menu Prompt | One 0.5 second beep when BIOS is ready to accept keyboard input | 932 Hz |
| BIOS update in progress | None | |
| Video error (no add-in graphics card installed) | On-off (1.0 second each) two times, then 2.5-second pause (off), entire pattern repeats (beeps and pause) once and the BIOS will continue to boot. | 932 Hz<br>For processors requiring an add-in graphics card |
| Memory error | On-off (1.0 second each) three times, then 2.5-second pause (off), entire pattern repeats (beeps and pause) until the system is powered off. | 932 Hz |
| Thermal trip warning | Alternate high and low beeps (1.0 second each) for eight beeps, followed by system shut down. | High beep 2000 Hz<br>Low beep 1500 Hz |

# 4.3 Front-panel Power LED Blink Codes

Whenever a recoverable error occurs during POST, the BIOS causes the board's front panel power LED to blink an error message describing the problem (see Table 43).

**Table 43. Front-panel Power LED Blink Codes**

| Type | Pattern | Note |
|------|---------|------|
| F2 Setup/F10 Boot Menu Prompt | None | |
| BIOS update in progress | Off when the update begins, then on for 0.5 seconds, then off for 0.5 seconds. The pattern repeats until the BIOS update is complete. | |
| Video error (no add-in graphics card installed) | On-off (0.5 second each) two times, then 3.0-second pause (off), entire pattern repeats (blink and pause) until the system is powered off. | For processors requiring an add-in graphics card |
| Memory error | On-off (0.5 second each) three times, then 3.0-second pause (off), entire pattern repeats (blinks and pause) until the system is powered off. | |
| Thermal trip warning | Each beep will be accompanied by the following blink pattern: .25 seconds On, .25 seconds Off, .25 seconds On, .25 seconds Off. This will result in a total of 32 blinks. | |

# 4.4 BIOS Error Messages

Table 44 lists the error messages and provides a brief description of each.

**Table 44. BIOS Error Messages**

| Error Message | Explanation |
|---------------|-------------|
| CMOS Battery Low | The battery may be losing power. Replace the battery soon. |
| CMOS Checksum Bad | The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values. |
| Memory Size Decreased | Memory size has decreased since the last boot. If no memory was removed, then memory may be bad. |
| No Boot Device Available | System did not find a device to boot. |

## 4.5 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h.  If the POST fails, execution stops and the last POST code generated is left at port 80h.  This code is useful for determining the point where an error occurred.

The following tables provide information about the POST codes generated by the BIOS:

- Table 45 lists the Port 80h POST code ranges
- Table 46 lists the Port 80h POST codes themselves
- Table 47 lists the Port 80h POST sequence

## NOTE

*In the tables listed above, all POST codes and range values are listed in hexadecimal.*

**Table 45.  Port 80h POST Code Ranges**

| Range | Category/Subsystem |
|---|---|
| 00 – 0F | Debug codes:  Can be used by any PEIM/driver for debug. |
| 10 – 1F | Host Processors:  1F is an unrecoverable CPU error. |
| 20 – 2F | Memory/Chipset:  2F is no memory detected or no useful memory detected. |
| 30 – 3F | Recovery:  3F indicated recovery failure. |
| 40 – 4F | Reserved for future use. |
| 50 – 5F | I/O Busses:  PCI, USB, ATA, etc.  5F is an unrecoverable error.  Start with PCI. |
| 60 – 6F | Reserved for future use (for new busses). |
| 70 – 7F | Output Devices:  All output consoles.  7F is an unrecoverable error. |
| 80 – 8F | Reserved for future use (new output console codes). |
| 90 – 9F | Input devices:  Keyboard/Mouse.  9F is an unrecoverable error. |
| A0 – AF | Reserved for future use (new input console codes). |
| B0 – BF | Boot Devices:  Includes fixed media and removable media.  BF is an unrecoverable error. |
| C0 – CF | Reserved for future use. |
| D0 – DF | Boot device selection. |
| E0 – FF | E0 – EE:  Miscellaneous codes. See Table 46.<br>EF:  boot/S3 resume failure.<br>F0 – FF:  FF processor exception. |

**Table 46.  Port 80h POST Codes**

| POST Code | Description of POST Operation |
|---|---|
| | **Host Processor** |
| 10 | Power-on initialization of the host processor (Boot Strap Processor) |
| 11 | Host processor cache initialization (including APs) |
| 12 | Starting Application processor initialization |
| 13 | SMM initialization |
| | **Chipset** |
| 21 | Initializing a chipset component |
| | **Memory** |
| 22 | Reading SPD from memory DIMMs |
| 23 | Detecting presence of memory DIMMs |
| 24 | Programming timing parameters in the memory controller and the DIMMs |
| 25 | Configuring memory |
| 26 | Optimizing memory settings |
| 27 | Initializing memory, such as ECC init |
| 29 | Memory testing completed |
| | **PCI Bus** |
| 50 | Enumerating PCI busses |
| 51 | Allocating resources to PCI bus |
| 52 | Hot Plug PCI controller initialization |
| 53 – 57 | Reserved for PCI Bus |
| | **USB** |
| 58 | Resetting USB bus |
| 59 | Reserved for USB |
| | **ATA/ATAPI/SATA** |
| 5A | Resetting PATA/SATA bus and all devices |
| 5B | Reserved for ATA |
| | **SMBus** |
| 5C | Resetting SMBus |
| 5D | Reserved for SMBus |
| | **Local Console** |
| 70 | Resetting the VGA controller |
| 71 | Disabling the VGA controller |
| 72 | Enabling the VGA controller |
| | **Remote Console** |
| 78 | Resetting the console controller |
| 79 | Disabling the console controller |
| 7A | Enabling the console controller |

**Table 46.  Port 80h POST Codes** (continued)

| POST Code | Description of POST Operation |
|---|---|
| | **Keyboard (USB)** |
| 90 | Resetting keyboard |
| 91 | Disabling keyboard |
| 92 | Detecting presence of keyboard |
| 93 | Enabling the keyboard |
| 94 | Clearing keyboard input buffer |
| 95 | Instructing keyboard controller to run Self Test (PS/2 only) |
| | **Mouse (USB)** |
| 98 | Resetting mouse |
| 99 | Disabling mouse |
| 9A | Detecting presence of mouse |
| 9B | Enabling mouse |
| | **Fixed Media** |
| B0 | Resetting fixed media |
| B1 | Disabling fixed media |
| B2 | Detecting presence of a fixed media (hard drive detection etc.) |
| B3 | Enabling/configuring a fixed media |
| | **Removable Media** |
| B8 | Resetting removable media |
| B9 | Disabling removable media |
| BA | Detecting presence of a removable media (CD-ROM detection, etc.) |
| BC | Enabling/configuring a removable media |
| | **BDS** |
| D$y$ | Trying boot selection y (y=0 to 15) |
| | **PEI Core** |
| E0 | Started dispatching PEIMs (emitted on first report of EFI_SW_PC_INIT_BEGIN EFI_SW_PEI_PC_HANDOFF_TO_NEXT) |
| E2 | Permanent memory found |
| E1, E3 | Reserved for PEI/PEIMs |
| | **DXE Core** |
| E4 | Entered DXE phase |
| E5 | Started dispatching drivers |
| E6 | Started connecting drivers |

continued

**Table 46.  Port 80h POST Codes** (continued)

| POST Code | Description of POST Operation |
|---|---|
| | **DXE Drivers** |
| E7 | Waiting for user input |
| E8 | Checking password |
| E9 | Entering BIOS setup |
| EB | Calling Legacy Option ROMs |
| | **Runtime Phase/EFI OS Boot** |
| F4 | Entering Sleep state |
| F5 | Exiting Sleep state |
| F8 | EFI boot service ExitBootServices ( ) has been called |
| F9 | EFI runtime service SetVirtualAddressMap ( ) has been called |
| FA | EFI runtime service ResetSystem ( ) has been called |
| | **PEIMs/Recovery** |
| 30 | Crisis Recovery has initiated per user request |
| 31 | Crisis Recovery has initiated by software (corrupt flash) |
| 34 | Loading recovery capsule |
| 35 | Handing off control to the recovery capsule |
| 3F | Unable to recover |

**Table 47.  Typical Port 80h POST Sequence**

| POST Code | Description |
| --- | --- |
| 21 | Initializing a chipset component |
| 22 | Reading SPD from memory DIMMs |
| 23 | Detecting presence of memory DIMMs |
| 25 | Configuring memory |
| 28 | Testing memory |
| 34 | Loading recovery capsule |
| E4 | Entered DXE phase |
| 12 | Starting application processor initialization |
| 13 | SMM initialization |
| 50 | Enumerating PCI busses |
| 51 | Allocating resourced to PCI bus |
| 92 | Detecting the presence of the keyboard |
| 90 | Resetting keyboard |
| 94 | Clearing keyboard input buffer |
| 95 | Keyboard Self Test |
| EB | Calling Video BIOS |
| 58 | Resetting USB bus |
| 5A | Resetting PATA/SATA bus and all devices |
| 92 | Detecting the presence of the keyboard |
| 90 | Resetting keyboard |
| 94 | Clearing keyboard input buffer |
| 5A | Resetting PATA/SATA bus and all devices |
| 28 | Testing memory |
| 90 | Resetting keyboard |
| 94 | Clearing keyboard input buffer |
| E7 | Waiting for user input |
| 01 | INT 19 |
| 00 | Ready to boot |

# 5 Regulatory Compliance and Battery Disposal Information

## 5.1 Regulatory Compliance

This section contains the following regulatory compliance information for Intel Desktop Board DH57DD:

- Safety standards
- European Union Declaration of Conformity statement
- Product Ecology statements
- Electromagnetic Compatibility (EMC) standards
- Product certification markings

### 5.1.1 Safety Standards

Intel Desktop Board DH57DD complies with the safety standards stated in Table 48 when correctly installed in a compatible host system.

**Table 48. Safety Standards**

| Standard | Title |
|---|---|
| CSA/UL 60950-1, First Edition | Information Technology Equipment – Safety - Part 1: General Requirements (USA and Canada) |
| EN 60950-1:2006, Second Edition | Information Technology Equipment – Safety - Part 1: General Requirements  (European Union) |
| IEC 60950-1:2005, Second Edition | Information Technology Equipment – Safety - Part 1: General Requirements (International) |

## 5.1.2   European Union Declaration of Conformity Statement

We, Intel Corporation, declare under our sole responsibility that the product Intel®
Desktop Board DH57DD is in conformity with all applicable essential requirements
necessary for CE marking, following the provisions of the European Council Directive
2004/108/EC (EMC Directive) and 2006/95/EC (Low Voltage Directive).

The product is properly CE marked demonstrating this conformity and is for
distribution within all member states of the EU with no restrictions.

$$\epsilon$$

This product follows the provisions of the European Directives 2004/108/EC and
2006/95/EC.

**Čeština**  Tento výrobek odpovídá požadavkům evropských směrnic 2004/108/EC a
2006/95/EC.

**Dansk**  Dette produkt er i overensstemmelse med det europæiske direktiv
2004/108/EC & 2006/95/EC.

**Dutch**  Dit product is in navolging van de bepalingen van Europees Directief
2004/108/EC & 2006/95/EC.

**Eesti**  Antud toode vastab Euroopa direktiivides 2004/108/EC ja 2006/95/EC
kehtestatud nõuetele.

**Suomi**  Tämä tuote noudattaa EU-direktiivin 2004/108/EC & 2006/95/EC määräyksiä.

**Français**  Ce produit est conforme aux exigences de la Directive Européenne
2004/108/EC & 2006/95/EC.

**Deutsch**  Dieses Produkt entspricht den Bestimmungen der Europäischen Richtlinie
2004/108/EC & 2006/95/EC.

**Ελληνικά**  Το παρόν προϊόν ακολουθεί τις διατάξεις των Ευρωπαϊκών Οδηγιών
2004/108/EC και 2006/95/EC.

**Magyar**  E termék megfelel a 2004/108/EC és 2006/95/EC Európai Irányelv
előírásainak.

**Icelandic**  Þessi vara stenst reglugerð Evrópska Efnahags Bandalagsins númer
2004/108/EC & 2006/95/EC.

**Italiano**  Questo prodotto è conforme alla Direttiva Europea 2004/108/EC &
2006/95/EC.

**Latviešu**  Šis produkts atbilst Eiropas Direktīvu 2004/108/EC un 2006/95/EC
noteikumiem.

**Lietuvių**  Šis produktas atitinka Europos direktyvų 2004/108/EC ir 2006/95/EC
nuostatas.

**Malti**  Dan il-prodott hu konformi mal-provvedimenti tad-Direttivi Ewropej
2004/108/EC u 2006/95/EC.

**Norsk**  Dette produktet er i henhold til bestemmelsene i det europeiske direktivet
2004/108/EC & 2006/95/EC.

**Polski**  Niniejszy produkt jest zgodny z postanowieniami Dyrektyw Unii Europejskiej
2004/108/EC i 73/23/EWG.

**Portuguese**  Este produto cumpre com as normas da Diretiva Européia 2004/108/EC
& 2006/95/EC.

***Español*** Este producto cumple con las normas del Directivo Europeo 2004/108/EC & 2006/95/EC.

***Slovensky*** Tento produkt je v súlade s ustanoveniami európskych direktív 2004/108/EC a 2006/95/EC.

***Slovenščina*** Izdelek je skladen z določbami evropskih direktiv 2004/108/EC in 2006/95/EC.

***Svenska*** Denna produkt har tillverkats i enlighet med EG-direktiv 2004/108/EC & 2006/95/EC.

***Türkçe*** Bu ürün, Avrupa Birliği'nin 2004/108/EC ve 2006/95/EC yönergelerine uyar.

# 5.1.3 Product Ecology Statements

The following information is provided to address worldwide product ecology concerns and regulations.

## 5.1.3.1 Disposal Considerations

This product contains the following materials that may be regulated upon disposal: lead solder on the printed wiring board assembly.

## 5.1.3.2 Recycling Considerations

As part of its commitment to environmental responsibility, Intel has implemented the Intel Product Recycling Program to allow retail consumers of Intel's branded products to return used products to selected locations for proper recycling.

Please consult the http://www.intel.com/intel/other/ehs/product_ecology for the details of this program, including the scope of covered products, available locations, shipping instructions, terms and conditions, etc.

### 中文

作为其对环境责任之承诺的部分，英特尔已实施 Intel Product Recycling Program
（英特尔产品回收计划），以允许英特尔品牌产品的零售消费者将使用过的产品退还至指定地点作恰当的重复使用处理。

请参考http://www.intel.com/intel/other/ehs/product_ecology
了解此计划的详情，包括涉及产品之范围、回收地点、运送指导、条款和条件等。

### *Deutsch*

Als Teil von Intels Engagement für den Umweltschutz hat das Unternehmen das Intel Produkt-Recyclingprogramm implementiert, das Einzelhandelskunden von Intel Markenprodukten ermöglicht, gebrauchte Produkte an ausgewählte Standorte für ordnungsgemäßes Recycling zurückzugeben.

Details zu diesem Programm, einschließlich der darin eingeschlossenen Produkte, verfügbaren Standorte, Versandanweisungen, Bedingungen usw., finden Sie auf der http://www.intel.com/intel/other/ehs/product_ecology

### *Español*

Como parte de su compromiso de responsabilidad medioambiental, Intel ha implantado el programa de reciclaje de productos Intel, que permite que los consumidores al detalle de los productos Intel devuelvan los productos usados en los lugares seleccionados para su correspondiente reciclado.

Consulte la http://www.intel.com/intel/other/ehs/product_ecology para ver los detalles del programa, que incluye los productos que abarca, los lugares disponibles, instrucciones de envío, términos y condiciones, etc.

### *Français*

Dans le cadre de son engagement pour la protection de l'environnement, Intel a mis en œuvre le programme Intel Product Recycling Program (Programme de recyclage des produits Intel) pour permettre aux consommateurs de produits Intel de recycler les produits usés en les retournant à des adresses spécifiées.

Visitez la page Web http://www.intel.com/intel/other/ehs/product_ecology pour en savoir plus sur ce programme, à savoir les produits concernés, les adresses disponibles, les instructions d'expédition, les conditions générales, etc.

### 日本語

インテルでは、環境保護活動の一環として、使い終えたインテル
ブランド製品を指定の場所へ返送していただき、リサイクルを適切に行えるよう、インテル製品リサイクル
プログラムを発足させました。

対象製品、返送先、返送方法、ご利用規約など、このプログラムの詳細情報は、http://www.intel.com/intel/other/ehs/product_ecology（英語）をご覧ください。

### *Malay*

Sebagai sebahagian daripada komitmennya terhadap tanggungjawab persekitaran, Intel telah melaksanakan Program Kitar Semula Produk untuk membenarkan pengguna-pengguna runcit produk jenama Intel memulangkan produk terguna ke lokasi-lokasi terpilih untuk dikitarkan semula dengan betul.

Sila rujuk http://www.intel.com/intel/other/ehs/product_ecology untuk mendapatkan butir-butir program ini, termasuklah skop produk yang dirangkumi, lokasi-lokasi tersedia, arahan penghantaran, terma & syarat, dsb.

### *Portuguese*

Como parte deste compromisso com o respeito ao ambiente, a Intel implementou o Programa de Reciclagem de Produtos para que os consumidores finais possam enviar produtos Intel usados para locais selecionados, onde esses produtos são reciclados de maneira adequada.

Consulte o site http://www.intel.com/intel/other/ehs/product_ecology (em Inglês) para obter os detalhes sobre este programa, inclusive o escopo dos produtos cobertos, os locais disponíveis, as instruções de envio, os termos e condições, etc.

***Russian***

В качестве части своих обязательств к окружающей среде, в Intel создана программа утилизации продукции Intel (Product Recycling Program) для предоставления конечным пользователям марок продукции Intel возможности возврата используемой продукции в специализированные пункты для должной утилизации.

Пожалуйста, обратитесь на веб-сайт [http://www.intel.com/intel/other/ehs/product_ecology](http://www.intel.com/intel/other/ehs/product_ecology) за информацией об этой программе, принимаемых продуктах, местах приема, инструкциях об отправке, положениях и условиях и т.д.

***Türkçe***

Intel, çevre sorumluluğuna bağımlılığının bir parçası olarak, perakende tüketicilerin Intel markalı kullanılmış ürünlerini belirlenmiş merkezlere iade edip uygun şekilde geri dönüştürmesini amaçlayan Intel Ürünleri Geri Dönüşüm Programı'nı uygulamaya koymuştur.

Bu programın ürün kapsamı, ürün iade merkezleri, nakliye talimatları, kayıtlar ve şartlar v.s dahil bütün ayrıntılarını ögrenmek için lütfen [http://www.intel.com/intel/other/ehs/product_ecology](http://www.intel.com/intel/other/ehs/product_ecology)

Web sayfasına gidin.
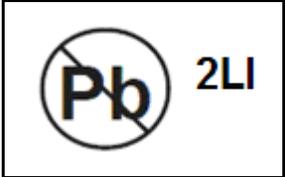
## 5.1.3.3   Lead Free Desktop Board

This Intel Desktop Board is a European Union Restriction of Hazardous Substances (EU RoHS Directive 2002/95/EC) compliant product.  EU RoHS restricts the use of six materials.  One of the six restricted materials is lead.

This Intel Desktop Board is lead free although certain discrete components used on the board contain a small amount of lead which is necessary for component performance and/or reliability.  This Intel Desktop Board is referred to as "Lead-free second level interconnect."  The board substrate and the solder connections from the board to the components (second-level connections) are all lead free.

China bans the same substances and has the same limits as EU RoHS; however it requires different product marking and controlled substance information.  The required mark shows the Environmental Friendly Usage Period (EFUP).  The EFUP is defined as the number of years for which controlled listed substances will not leak or chemically deteriorate while in the product.

Table 49 shows the various forms of the "Lead-Free $2^{nd}$ Level Interconnect" mark as it appears on the board and accompanying collateral.

**Table 49.  Lead-Free Board Markings**

| Description | Mark |
|---|---|
| Lead-Free 2nd Level Interconnect: This symbol is used to identify electrical and electronic assemblies and components in which the lead (Pb) concentration level in the desktop board substrate and the solder connections from the board to the components (second-level interconnect) is not greater than 0.1% by weight (1000 ppm). | <br><br>or<br><br><br><br>or<br><br> |

## 5.1.4      EMC Regulations

Intel Desktop Board DH57DD complies with the EMC regulations stated in Table 50 when correctly installed in a compatible host system.

**Table 50.  EMC Regulations**

| Regulation | Title |
|---|---|
| FCC 47 CFR Part 15, Subpart B | Title 47 of the Code of Federal Regulations, Part15, Subpart B, Radio Frequency Devices.  (USA) |
| ICES-003 Issue 4 | Interference-Causing Equipment Standard, Digital Apparatus.  (Canada) |
| EN55022:2006 | Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment.  (European Union) |
| EN55024:1998 | Information Technology Equipment – Immunity Characteristics Limits and methods of measurement.  (European Union) |
| EN55022:2006 | Australian Communications Authority, Standard for Electromagnetic Compatibility.  (Australia and New Zealand) |
| CISPR 22:2005 +A1:2005 +A2:2006 | Limits and methods of measurement of Radio Disturbance Characteristics of Information Technology Equipment.  (International) |
| CISPR 24:1997 +A1:2001 +A2:2002 | Information Technology Equipment – Immunity Characteristics – Limits and Methods of Measurement.  (International) |
| VCCI V-3/2007.04, V-4/2007.04 | Voluntary Control for Interference by Information Technology Equipment.  (Japan) |
| KN-22, KN-24 | Korean Communications Commission – Framework Act on Telecommunications and Radio Waves Act (South Korea) |
| CNS 13438:2006 | Bureau of Standards, Metrology and Inspection (Taiwan) |

Japanese Kanji statement translation:  this is a Class B product based on the standard of the Voluntary Control Council for Interference from Information Technology Equipment (VCCI).  If this is used near a radio or television receiver in a domestic environment, it may cause radio interference.  Install and use the equipment according to the instruction manual.

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＢ情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。
　取扱説明書に従って正しい取り扱いをして下さい。

Korean Class B statement translation:  this is household equipment that is certified to comply with EMC requirements.  You may use this equipment in residential environments and other non-residential environments.

이 기기는 가정용으로 전자파적합등록을 한 기기로서
주거지역에서는 물론 모든 지역에서 사용할 수 있습니다.

# 5.1.5      Product Certification Markings (Board Level)

Intel Desktop Board DH57DD has the product certification markings shown in Table 51:

**Table 51.  Product Certification Markings**

| Description | Mark |
|---|---|
| UL joint US/Canada Recognized Component mark.  Includes adjacent UL file number for Intel desktop boards:  E210882. | |
| FCC Declaration of Conformity logo mark for Class B equipment.  Includes Intel name and DH57DD model designation. | |
| CE mark.  Declaring compliance to European Union (EU) EMC directive and Low Voltage directive. | |
| Australian Communications Authority (ACA) and New Zealand Radio Spectrum Management (NZ RSM) C-tick mark.  Includes adjacent Intel supplier code number, N-232. | |
| Japan VCCI (Voluntary Control Council for Interference) mark. | |
| S. Korea KCC (Korean Communications Commission) mark.  Includes adjacent KCC certification number:  CPU-DH57DD (B) | |
| Taiwan BSMI (Bureau of Standards, Metrology and Inspections) mark.  Includes adjacent Intel company number, D33025. | |
| Printed wiring board manufacturer's recognition mark.  Consists of a unique UL recognized manufacturer's logo, along with a flammability rating (solder side). | V-0 |
| China RoHS/Environmentally Friendly Use Period Logo:  This is an example of the symbol used on Intel Desktop Boards and associated collateral.  The color of the mark may vary depending upon the application.  The Environmental Friendly Usage Period (EFUP) for Intel Desktop Boards has been determined to be 10 years. | |

## 5.2 Battery Disposal Information

⚠️ **CAUTION**

*Risk of explosion if the battery is replaced with an incorrect type.  Batteries should be recycled where possible.  Disposal of used batteries must be in accordance with local environmental regulations.*

⚠️ PRECAUTION

*Risque d'explosion si la pile usagée est remplacée par une pile de type incorrect.  Les piles usagées doivent être recyclées dans la mesure du possible.  La mise au rebut des piles usagées doit respecter les réglementations locales en vigueur en matière de protection de l'environnement.*

⚠️ FORHOLDSREGEL

*Eksplosionsfare, hvis batteriet erstattes med et batteri af en forkert type.  Batterier bør om muligt genbruges.  Bortskaffelse af brugte batterier bør foregå i overensstemmelse med gældende miljølovgivning.*

⚠️ OBS!

*Det kan oppstå eksplosjonsfare hvis batteriet skiftes ut med feil type.  Brukte batterier bør kastes i henhold til gjeldende miljølovgivning.*

⚠️ VIKTIGT!

*Risk för explosion om batteriet ersätts med felaktig batterityp.  Batterier ska kasseras enligt de lokala miljövårdsbestämmelserna.*

⚠️ VARO

*Räjähdysvaara, jos pariston tyyppi on väärä.  Paristot on kierrätettävä, jos se on mahdollista. Käytetyt paristot on hävitettävä paikallisten ympäristömääräysten mukaisesti.*

⚠️ VORSICHT

*Bei falschem Einsetzen einer neuen Batterie besteht Explosionsgefahr.  Die Batterie darf nur durch denselben oder einen entsprechenden, vom Hersteller empfohlenen Batterietyp ersetzt werden.  Entsorgen Sie verbrauchte Batterien den Anweisungen des Herstellers entsprechend.*

⚠️ AVVERTIMENTO

*Esiste il pericolo di un esplosione se la pila non viene sostituita in modo corretto. Utilizzare solo pile uguali o di tipo equivalente a quelle consigliate dal produttore.  Per disfarsi delle pile usate, seguire le istruzioni del produttore.*

⚠ PRECAUCIÓN

*Existe peligro de explosión si la pila no se cambia de forma adecuada. Utilice solamente pilas iguales o del mismo tipo que las recomendadas por el fabricante del equipo. Para deshacerse de las pilas usadas, siga igualmente las instrucciones del fabricante.*

⚠ WAARSCHUWING

*Er bestaat ontploffingsgevaar als de batterij wordt vervangen door een onjuist type batterij. Batterijen moeten zoveel mogelijk worden gerecycled. Houd u bij het weggooien van gebruikte batterijen aan de plaatselijke milieuwetgeving.*

⚠ ATENÇÃO

*Haverá risco de explosão se a bateria for substituída por um tipo de bateria incorreto. As baterias devem ser recicladas nos locais apropriados. A eliminação de baterias usadas deve ser feita de acordo com as regulamentações ambientais da região.*

⚠ AŚCIAROŽZNAŚĆ

*Існуе рызыка выбуху, калі заменены акумулятар неправільнага тыпу. Акумулятары павінны, па магчымасці, перепрацоўвацца. Пазбаўляцца ад старых акумулятараў патрэбна згодна з мясцовым заканадаўствам па экалогіі.*

⚠ UPOZORNÌNÍ

*V případě výměny baterie za nesprávný druh může dojít k výbuchu. Je-li to možné, baterie by měly být recyklovány. Baterie je třeba zlikvidovat v souladu s místními předpisy o životním prostředí.*

⚠ Προσοχή

*Υπάρχει κίνδυνος για έκρηξη σε περίπτωση που η μπαταρία αντικατασταθεί από μία λανθασμένου τύπου. Οι μπαταρίες θα πρέπει να ανακυκλώνονται όταν κάτι τέτοιο είναι δυνατό. Η απόρριψη των χρησιμοποιημένων μπαταριών πρέπει να γίνεται σύμφωνα με τους κατά τόπο περιβαλλοντικούς κανονισμούς.*

⚠ VIGYAZAT

*Ha a telepet nem a megfelelő típusú telepre cseréli, az felrobbanhat. A telepeket lehetőség szerint újra kell hasznosítani. A használt telepeket a helyi környezetvédelmi előírásoknak megfelelően kell kiselejtezni.*

⚠ 注意

異なる種類の電池を使用すると、爆発の危険があります。リサイクル
が可能な地域であれば、電池をリサイクルしてください。使用後の電
池を破棄する際には、地域の環境規制に従ってください。

⚠️ AWAS

*Risiko letupan wujud jika bateri digantikan dengan jenis yang tidak betul. Bateri sepatutnya dikitar semula jika boleh. Pelupusan bateri terpakai mestilah mematuhi peraturan alam sekitar tempatan.*

⚠️ OSTRZEŻENIE

*Istnieje niebezpieczeństwo wybuchu w przypadku zastosowania niewłaściwego typu baterii. Zużyte baterie należy w miarę możliwości utylizować zgodnie z odpowiednimi przepisami ochrony środowiska.*

⚠️ PRECAUŢIE

*Risc de explozie, dacă bateria este înlocuită cu un tip de baterie necorespunzător. Bateriile trebuie reciclate, dacă este posibil. Depozitarea bateriilor uzate trebuie să respecte reglementările locale privind protecţia mediului.*

⚠️ ВНИМАНИЕ

*При использовании батареи несоответствующего типа существует риск ее взрыва. Батареи должны быть утилизированы по возможности. Утилизация батарей должна проводится по правилам, соответствующим местным требованиям.*

⚠️ UPOZORNENIE

*Ak batériu vymeníte za nesprávny typ, hrozí nebezpečenstvo jej výbuchu. Batérie by sa mali podľa možnosti vždy recyklovať. Likvidácia použitých batérií sa musí vykonávať v súlade s miestnymi predpismi na ochranu životného prostredia.*

⚠️ POZOR

*Zamenjava baterije z baterijo drugačnega tipa lahko povzroči eksplozijo. Če je mogoče, baterije reciklirajte. Rabljene baterije zavrzite v skladu z lokalnimi okoljevarstvenimi predpisi.*

⚠️ คำเตือน

*ระวังการระเบิดที่เกิดจากเปลี่ยนแบตเตอรี่ผิดประเภท หากเป็นไปได้ ควรนำแบตเตอรี่ไปรีไซเคิล การทิ้งแบตเตอรี่ใช้แล้วต้องเป็นไปตามกฎข้อบังคับด้านสิ่งแวดล้อมของท้องถิ่น.*

⚠️ UYARI

*Yanlış türde pil takıldığında patlama riski vardır. Piller mümkün olduğunda geri dönüştürülmelidir. Kullanılmış piller, yerel çevre yasalarına uygun olarak atılmalıdır.*

⚠️ ОСТОРОГА

*Використовуйте батареї правильного типу, інакше існуватиме ризик вибуху. Якщо можливо, використані батареї слід утилізувати. Утилізація використаних батарей має бути виконана згідно місцевих норм, що регулюють охорону довкілля.*

⚠️ UPOZORNĚNÍ

*V případě výměny baterie za nesprávný druh může dojít k výbuchu. Je-li to možné, baterie by měly být recyklovány. Baterie je třeba zlikvidovat v souladu s místními předpisy o životním prostředí.*

⚠️ **ETTEVAATUST**

*Kui patarei asendatakse uue ebasobivat tüüpi patareiga, võib tekkida plahvatusoht. Tühjad patareid tuleb võimaluse korral viia vastavasse kogumispunkti. Tühjade patareide äraviskamisel tuleb järgida kohalikke keskkonnakaitse alaseid reegleid.*

⚠️ FIGYELMEZTETÉS

*Ha az elemet nem a megfelelő típusúra cseréli, felrobbanhat. Az elemeket lehetőség szerint újra kell hasznositani. A használt elemeket a helyi környezetvédelmi előírásoknak megfelelően kell kiselejtezni.*

⚠️ UZMANĪBU

*Pastāv eksplozijas risks, ja baterijas tiek nomainītas ar nepareiza veida baterijām. Ja iespējams, baterijas vajadzētu nodot attiecīgos pieņemšanas punktos. Bateriju izmešanai atkritumos jānotiek saskaņā ar vietējiem vides aizsardzības noteikumiem.*

⚠️ DĖMESIO

*Naudojant netinkamo tipo baterijas įrenginys gali sprogti. Kai tik įmanoma, baterijas reikia naudoti pakartotinai. Panaudotas baterijas išmesti būtina pagal vietinius aplinkos apsaugos nuostatus.*

⚠️ ATTENZJONI

*Riskju ta' splużjoni jekk il-batterija tinbidel b'tip ta' batterija mhux korrett. Il-batteriji għandhom jiġu riċiklati fejn hu possibbli. Ir-rimi ta' batteriji użati għandu jsir skond ir-regolamenti ambjentali lokali.*

⚠️ OSTRZEŻENIE

*Ryzyko wybuchu w przypadku wymiany na baterie niewłaściwego typu. W miarę możliwości baterie należy poddać recyklingowi. Zużytych baterii należy pozbywać się zgodnie z lokalnie obowiązującymi przepisami w zakresie ochrony środowiska.*