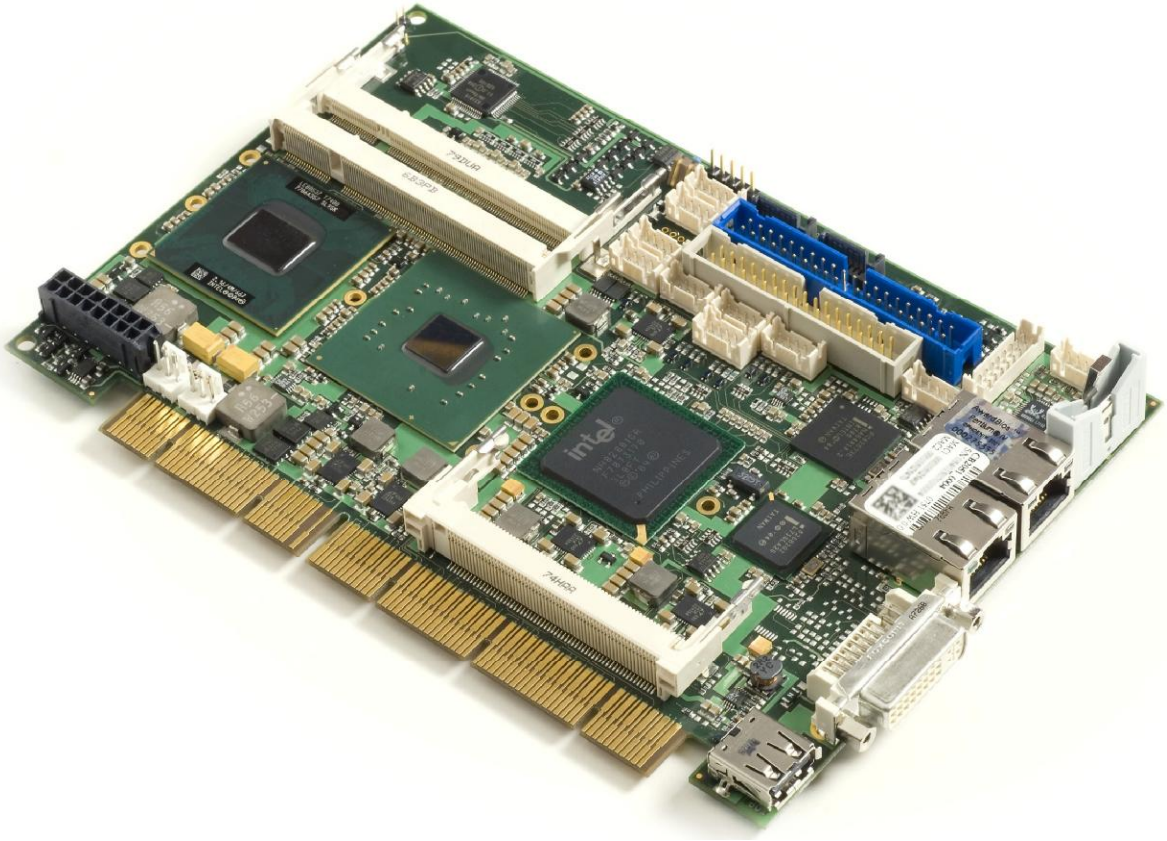
BECKHOFF

CB2051

Manual

rev 1.1



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0 Document History

Version	Changes
0.1	first pre-release
0.2	dimensional drawings added
1.0	updated contact details, minor changes
1.1	minor changes

NOTE

All company names, brand names, and product names referred to in this manual are registered or unregistered trademarks of their respective holders and are, as such, protected by national and international law.

1 Introduction

1.1 Notes on the Documentation

This description is only intended for the use of trained specialists in control and automation engineering who are familiar with the applicable national standards. It is essential that the following notes and explanations are followed when installing and commissioning these components.

1.1.1 Liability Conditions

The responsible staff must ensure that the application or use of the products described satisfy all the requirements for safety, including all the relevant laws, regulations, guidelines and standards.
The documentation has been prepared with care. The products described are, however, constantly under development. For that reason the documentation is not in every case checked for consistency with performance data, standards or other characteristics. None of the statements of this manual represents a guarantee (Garantie) in the meaning of § 443 BGB of the German Civil Code or a statement about the contractually expected fitness for a particular purpose in the meaning of § 434 par. 1 sentence 1 BGB. In the event that it contains technical or editorial errors, we retain the right to make alterations at any time and without warning. No claims for the modification of products that have already been supplied may be made on the basis of the data, diagrams and descriptions in this documentation.

1.1.2 Copyright

© This documentation is copyrighted. Any reproduction or third party use of this publication, whether in whole or in part, without the written permission of Beckhoff Automation GmbH, is forbidden.

1.2 Safety Instructions

Please consider the following safety instructions and descriptions. Product specific safety instructions are to be found on the following pages or in the areas mounting, wiring, commissioning etc.

1.2.1 Disclaimer

All the components are supplied in particular hardware and software configurations appropriate for the application. Modifications to hardware or software configurations other than those described in the documentation are not permitted, and nullify the liability of Beckhoff Automation GmbH.

1.2.2 Description of Safety Symbols

The following safety symbols are used in this documentation. They are intended to alert the reader to the associated safety instructions.

ACUTE RISK OF INJURY!

If you do not adhere to the safety advise next to this symbol, there is immediate danger to life and health of individuals!

RISK OF INJURY!

If you do not adhere to the safety advise next to this symbol, there is danger to life and health of individuals!

HAZARD TO INDIVIDUALS, ENVIRONMENT, DEVICES, OR DATA!

If you do not adhere to the safety advise next to this symbol, there is obvious hazard to individuals, to environment, to materials, or to data.

NOTE OR POINTER

This symbol indicates information that contributes to better understanding.

1.3 Essential Safety Measures

1.3.1 Operator's Obligation to Exercise Diligence

The operator must ensure that

- the product is only used for its intended purpose
- the product is only operated in sound condition and in working order
- the instruction manual is in good condition and complete, and always available for reference at the location where the products are used
- the product is only used by suitably qualified and authorised personnel
- the personnel is instructed regularly about relevant occupational safety and environmental protection aspects
- the operating personnel is familiar with the operating manual and in particular the safety notes contained herein

1.3.2 National Regulations Depending on the Machine Type

Depending on the type of machine and plant in which the product is used, national regulations governing the controllers of such machines will apply, and must be observed by the operator. These regulations cover, amongst other things, the intervals between inspections of the controller. The operator must initiate such inspections in good time.

1.3.3 Operator Requirements

- Read the operating instructions

All users of the product must have read the operating instructions for the system they work with.

- System know-how

All users must be familiar with all accessible functions of the product.

1.4 Functional Range

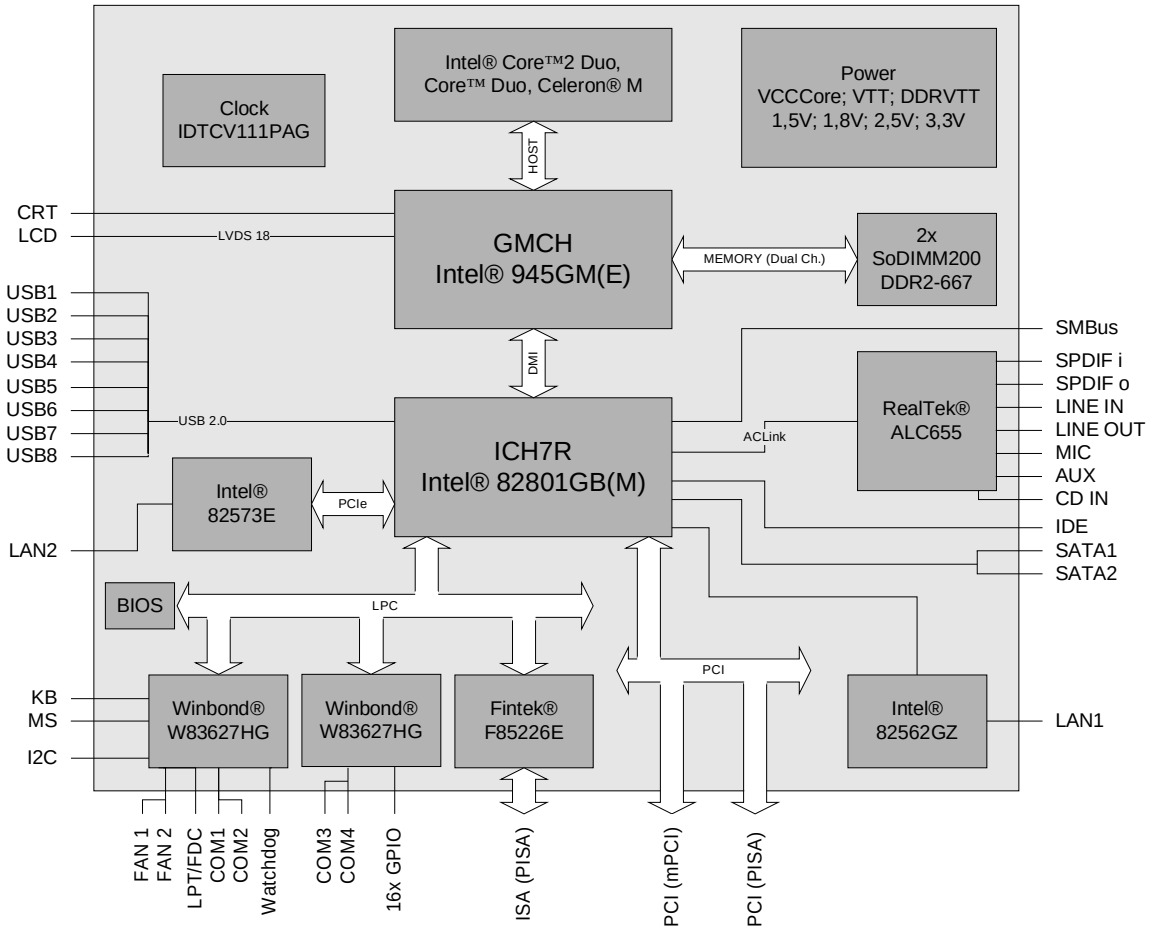
NOTE

The descriptions contained in the present documentation represent a detailed and extensive product description. As far as the described motherboard was acquired as an integral component of an Industrial PC from Beckhoff Automation GmbH, this product description shall be applied only in limited scope. Only the contractually agreed specifications of the corresponding Industrial PC from Beckhoff Automation GmbH shall be relevant. Due to several models of Industrial PCs, variations in the component placement of the motherboards are possible. Support and service benefits for the built-in motherboard will be rendered by Beckhoff Automation GmbH exclusively as specified in the product description (inclusive operation system) of the particular Industrial PC.

2 Overview

2.1 Features

The CB2051 is a computer motherboard for industrial applications. It complies with the PISA-Slot form factor and ships with either Intel® Celeron® M, Intel® Core™ Duo or Intel® Core™2 Duo CPUs. Two SO-DIMM200 slots allow a maximum of 2 GByte DDR2-667 RAM. The CB2051 offers a high degree of flexibility in terms of connecting external devices to the board. In addition to the ISA and PCI busses being available through the PISA connector there is also a MiniPCI connector. Furthermore we have two SATA channels and one IDE channel, four serial ports, two LAN connectors, several analog and digital sound in- and outputs, eight USB ports, CRT and LCD connectors.



- Processor Intel® Celeron® M, Intel® Core™ Duo or Intel® Core™2 Duo
- Chipset Intel® 945GM and Intel® ICH7
- Two SO-DIMM200 slots for up to 2 GByte DDR2-667
- Four serial ports COM1 to COM4
- LAN Ethernet 10/100 (Base-T)
- LAN Ethernet 10/100/1000 (Base-T)
- Two SATA channels
- IDE interface
- PS2 keyboard/mouse interface
- LPT interface

- Eight USB 2.0 interfaces
- AWARD BIOS 6.10
- CRT interface
- TFT interface via LVDS 18 Bit
- AC97 compatible sound including SPDIF in and output
- RTC with external CMOS battery
- MiniPCI slot
- PCI bus via PISA slot connector
- ISA bus via PISA slot connector
- 16x GPIO
- Format: mm x mm

2.2 Specifications and Documents

In making this manual and for further reading of technical documentation the following documents, specifications and web-pages were used and are recommended.

§ PISA Specification
Version 1.8
us.kontron.com

§ PCI Specification
Version 2.3 resp. 3.0
www.pcisig.com

§ Mini-PCI Specification
Version 1.0
www.pcisig.com

§ ACPI Specification
Version 3.0
www.acpi.info

§ ATA/ATAPI Specification
Version 7 Rev. 1
www.t13.org

§ USB Specifications
www.usb.org

§ SM-Bus Specification
Version 2.0
www.smbus.org

§ Intel Chipset Description
Mobile Intel 945 Express Chipset Family Datasheet
www.intel.com

§ Intel Chip Description
ICH7 Datasheet
www.intel.com

§ Intel Chip Descriptions
Celeron M, Core Duo/Solo, Core2 Duo
www.intel.com

§ Winbond Chip Description
W83627HG Datasheet
www.winbond-usa.com oder www.winbond.com.tw

§ Intel Chip Description
82562EZ/GZ Datasheet
www.intel.com

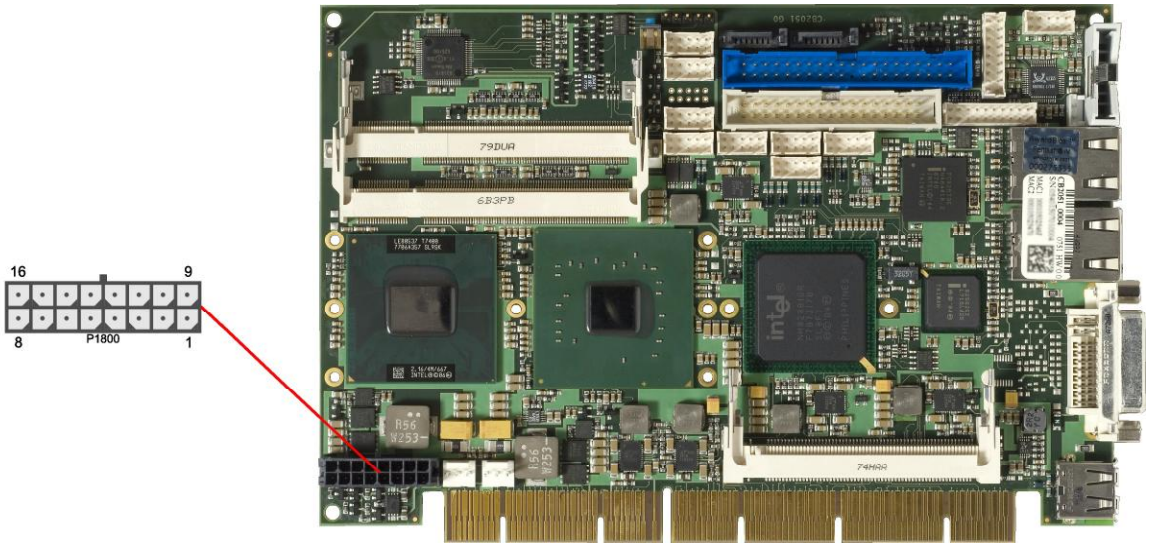
§ Intel Chip Description
82573L(E) Datasheet
www.intel.com

§ IDT Chip Description
IDTCV111i Datasheet
www.idt.com

3 Connectors

3.1 Power Supply

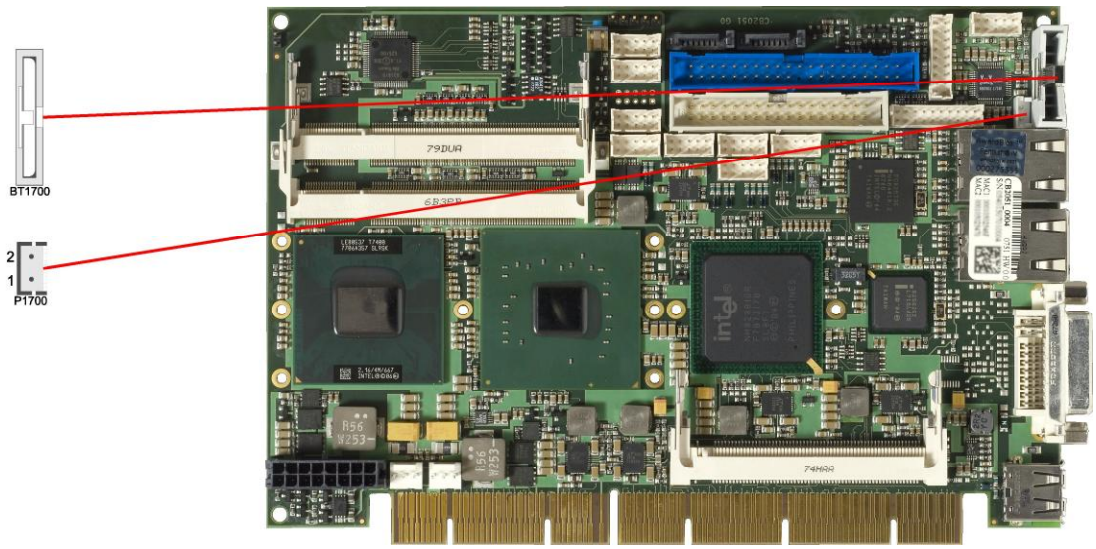
The power supply of the hardware module is effected via a 2x8-pin connector (Molex PS 43045-16xx, mating connector: Molex PS 43025-16xx). The pins for 12 volt have the sole purpose of supplying one or both fans with the necessary current. Thus, when no fan is installed, these pins have no function. COM3 RXD and TXD can also be used for connecting a second power supply unit, e. g. for UPS. As an ordering option SMBus signals SCL/SDA can be provided (replacing COM3 TXD/RXD).



Description	Name	Pin		Name	Description
COM3 transmit data	TXD	1	9	RXD	COM3 receive data
PSU on	PS-ON	2	10	RESET#	PSU reset
powerbutton PSU	PWRBTN#	3	11	SVCC	standby-supply 5V
12 volt supply	12V	4	12	12V	12 volt supply
ground	GND	5	13	GND	ground
ground	GND	6	14	GND	ground
5 volt supply	VCC	7	15	VCC	5 volt supply
5 volt supply	VCC	8	16	VCC	5 volt supply

3.2 CMOS battery

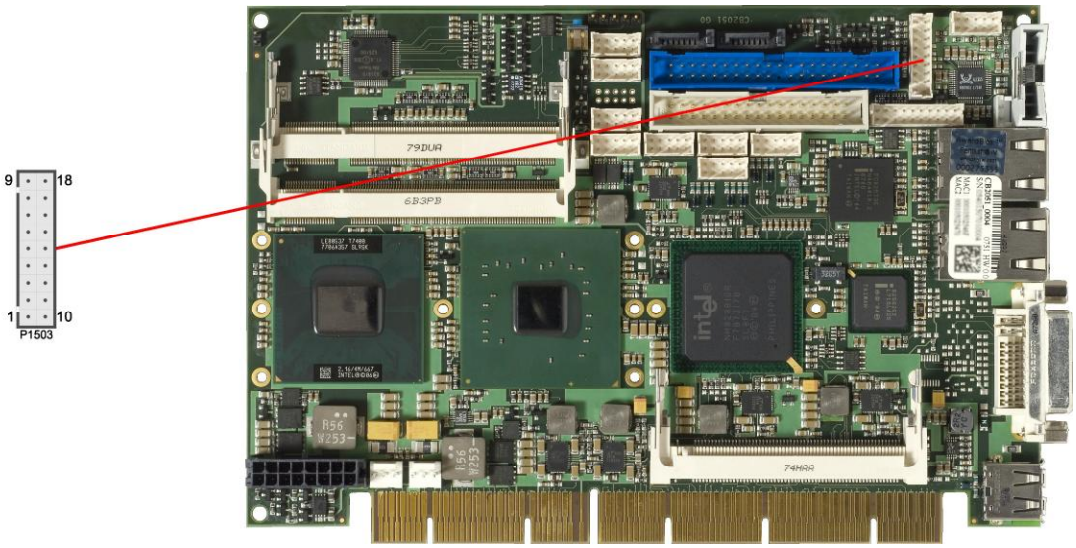
The board ships with a CR2032 battery holder (Renata VBH2032-1) and 3V battery. Alternatively, an external battery can be connected via a 2pin connector (JST B2B-EH-A, mating connector: EHR-2).



Pin	Name	Description
1	BATT	battery 3.3 volt
2	GND	ground

3.3 System

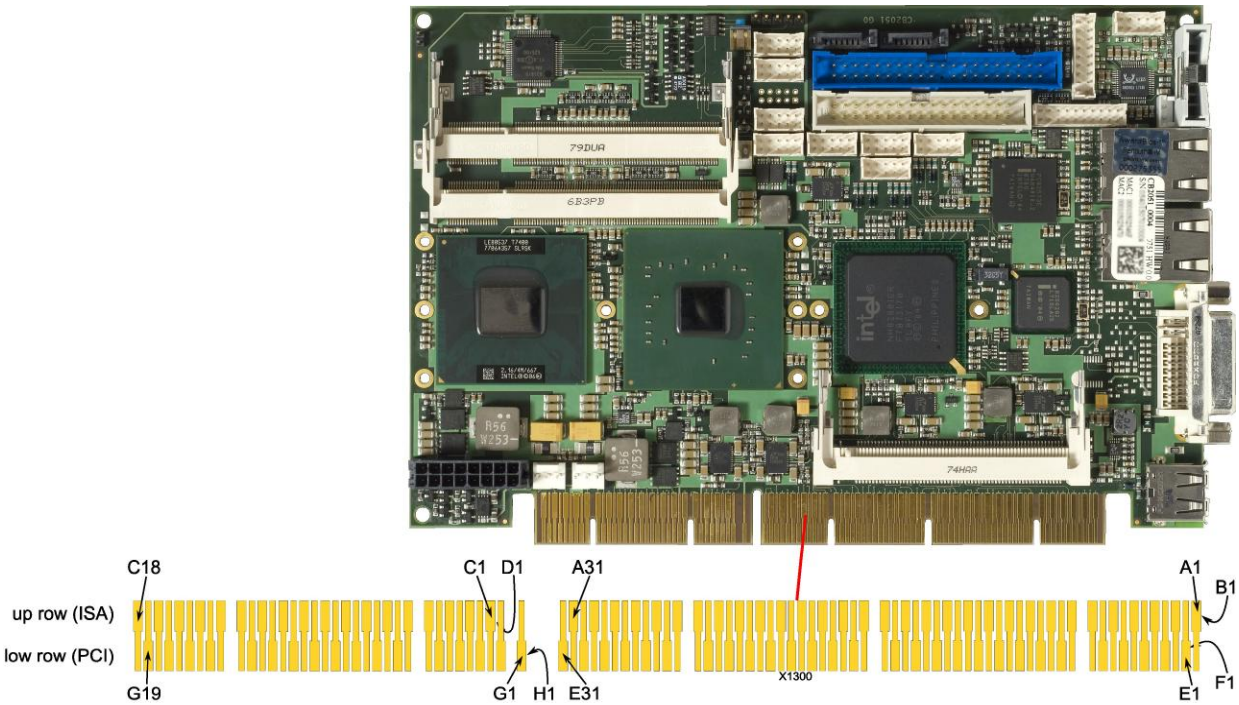
Some typical signals for system control are provided through a 2x9 pin connector (JST B18B-PHDSS, mating connector: PHDR-18VS). This connector combines signals for power button, reset, keyboard, speaker, and several LEDs such as harddisk LED, touch screen LED, suspend LED, and three additional LEDs which are driven by GPIOs. Of these three GPIO-LEDs, LED1 and LED2 are already provided with a series resistor. As can be seen from the pinout table below, corresponding signals are often placed vis-à-vis or at least near to each other.



Description	Name	Pin		Name	Description
ground	GND	1	10	PWRBTN#	on/suspend button
ground	GND	2	11	RESET#	reset to ground
LED touch screen	TOUCHLED	3	12	3.3V	3.3 volt supply
LED suspend / ACPI	S-LED	4	13	S3.3V	standby supply 3.3 volt
LED harddisk	HDLED	5	14	3.3V	3.3 volt supply
LED GPIO device	LED1	6	15	3.3V	3.3 volt supply
LED GPIO device	LED2	7	16	LED3	LED GPIO device
speaker to 5 volt	SPEAKER	8	17	KDAT	keyboard data
standby supply 5 volt	(S)VCC	9	18	KCLK	keyboard clock

3.4 PISA Slot

The CB2051 module requires a backplane board in which it is inserted using the PISA slot. This slot combines PCI and ISA signals in one single connector which is useful in situations where limited space is an issue. The CB2051 currently supports only PCI.



NOTE

Please note the unusual pin numbering scheme of the PISA slot. There is an "up row" (for ISA signals) and a "low row" (for PCI signals). The former is divided into segments A through D while the latter is divided into segments E through H (cf. the illustration above).

Pinout "up row":

Description	Name	Pin		Name	Description
IO channel check	IOCHK#	A1	B1	GND	ground
system data 7	SD7	A2	B2	RSTDRV	reset drive
system data 6	SD6	A3	B3	VCC	5 volt supply
system data 5	SD5	A4	B4	IRQ9	interrupt request 9
system data 4	SD4	A5	B5	-5V	-5 volt
system data 3	SD3	A6	B6	DRQ2	DMA request 2
system data 2	SD2	A7	B7	-12V	-12 volt supply
system data 1	SD1	A8	B8	WS0#	wait state 0
system data 0	SD0	A9	B9	12V	12 volt supply
IO channel ready	IOCHRDY	A10	B10	GND	ground
address enable	AEN	A11	B11	SMEMW#	memory write below 1MB
system address 19	SA19	A12	B12	SMEMR#	memory read below 1MB
system address 18	SA18	A13	B13	IOW#	IO write
system address 17	SA17	A14	B14	IOR#	IO read
system address 16	SA16	A15	B15	DACK3#	DMA acknowledge 3
system address 15	SA15	A16	B16	DRQ3	DMA request 3
system address 14	SA14	A17	B17	DACK1#	DMA acknowledge 1

Description	Name	Pin		Name	Description
system address 13	SA13	A18	B18	DRQ1	DMA request 1
system address 12	SA12	A19	B19	REFRESH#	refresh
system address 11	SA11	A20	B20	SYSCLK	system clock
system address 10	SA10	A21	B21	IRQ7	interrupt request 7
system address 9	SA9	A22	B22	IRQ6	interrupt request 6
system address 8	SA8	A23	B23	IRQ5	interrupt request 5
system address 7	SA7	A24	B24	IRQ4	interrupt request 4
system address 6	SA6	A25	B25	IRQ3	interrupt request 3
system address 5	SA5	A26	B26	DACK2#	DMA acknowledge 2
system address 4	SA4	A27	B27	T/C	terminal count
system address 3	SA3	A28	B28	BALE	address latch enable
system address 2	SA2	A29	B29	VCC	5 volt supply
system address 1	SA1	A30	B30	OSC14	14.31818 MHz
system address 0	SA0	A31	B31	GND	ground
byte high enable	SBHE#	C1	D1	MEMCS16#	memory chip select
latched address 23	LA23	C2	D2	IOCS16#	IO chip select
latched address 22	LA22	C3	D3	IRQ10	interrupt request 10
latched address 21	LA21	C4	D4	IRQ11	interrupt request 11
latched address 20	LA20	C5	D5	IRQ12	interrupt request 12
latched address 19	LA19	C6	D6	IRQ13	interrupt request 13
latched address 18	LA18	C7	D7	IRQ14	interrupt request 14
latched address 17	LA17	C8	D8	DACK0#	DMA acknowledge 0
memory read	MEMR#	C9	D9	DRQ0	DMA request 0
memory write	MEMW#	C10	D10	DACK5#	DMA acknowledge 5
system data 8	SD8	C11	D11	DRQ5	DMA request 5
system data 9	SD9	C12	D12	DACK6#	DMA acknowledge 6
system data 10	SD10	C13	D13	DRQ6	DMA request 6
system data 11	SD11	C14	D14	DACK7#	DMA acknowledge 7
system data 12	SD12	C15	D15	DRQ7	DMA request 7
system data 13	SD13	C16	D16	VCC	5 volt supply
system data 14	SD14	C17	D17	MASTER#	bus master
system data 15	SD15	C18	D18	GND	ground

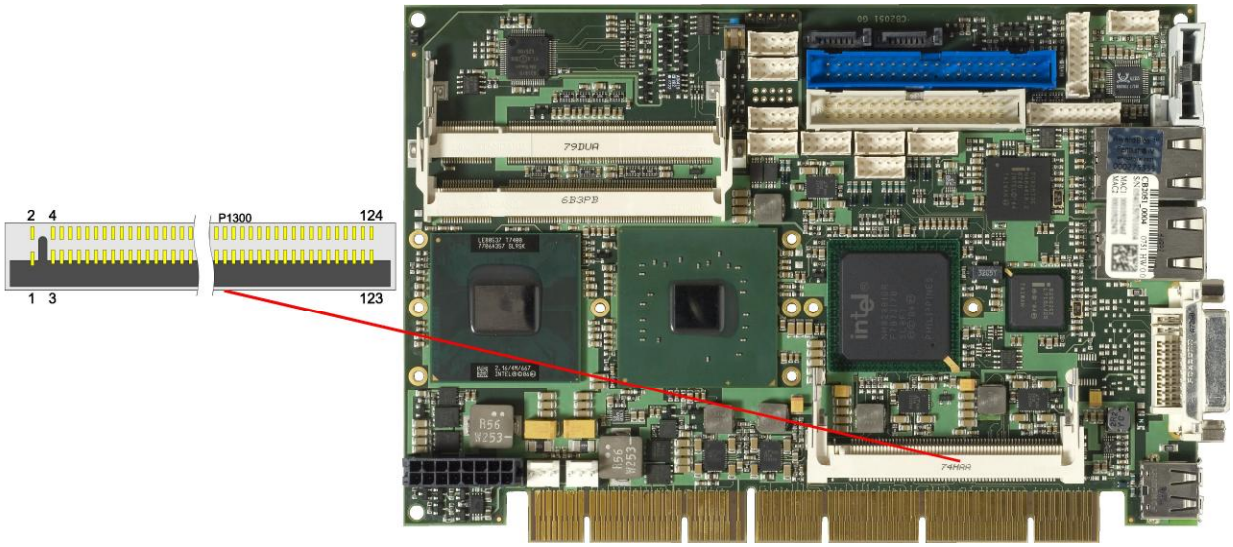
Pinout "low row":

Description	Name	Pin		Name	Description
I2C clock	I2CLK	E1	F1	I2DAT	I2C data
ground	GND	E2	F2	GND	ground
interrupt B	INTB#	E3	F3	INTA#	interrupt A
interrupt D	INTD#	E4	F4	INTC#	interrupt C
5 volt supply	VCC	E5	F5	VCC	5 volt supply
coded	N/C	E6	F6	N/C	coded
5 volt supply	VCC	E7	F7	VIO	IO supply
PCI reset 2	PRST2#	E8	F8	PCLK2	PCI clock
grant 0	GNT0#	E9	F9	GND	ground
request 0	REQ0#	E10	F10	GNT1#	grant 1
ground	GND	E11	F11	GND	ground
PCI clock 1	PCLK1	E12	F12	REQ1#	request 1
ground	GND	E13	F13	AD31	address/data 31
address/data 30	AD30	E14	F14	AD29	address/data 29
request 2	REQ2#	E15	F15	PCLK3	PCI clock 3
coded	N/C	E16	F16	N/C	coded
grant 2	GNT2#	E17	F17	PCLK4	PCI clock 4
address/data 28	AD28	E18	F18	AD27	address/data 27
address/data 26	AD26	E19	F19	AD25	address/data 25

Description	Name	Pin		Name	Description
address/data 24	AD24	E20	F20	CBE3#	bus cmd/byte enable 3
address/data 22	AD22	E21	F21	AD23	address/data 23
address/data 20	AD20	E22	F22	AD21	address/data 21
address/data 18	AD18	E23	F23	AD19	address/data 19
reset	RESET#	E24	F24	REQ3#	request 3
coded	N/C	E25	F25	N/C	coded
ground	GND	E26	F26	GNT3#	grant 3
address/data 16	AD16	E27	F27	AD17	address/data 17
cycle frame	FRAME#	E28	F28	IRDY#	initiator ready
bus cmd/byte enable 2	CBE2#	E29	F29	DEVSEL#	device select
target ready	TRDY#	E30	F30	PLOCK#	lock bus
stop req by target	STOP#	E31	F31	PERR#	parity error
ground	GND	G1	H1	SERR#	system error
reserved	N/C	G2	H2	AD15	address/data 15
bus cmd/byte enable 1	CBE1#	G3	H3	AD14	address/data 14
parity	PAR	G4	H4	AD12	address/data 12
ground	GND	G5	H5	GND	ground
coded	N/C	G6	H6	N/C	coded
ground	GND	G7	H7	GND	ground
address/data 13	AD13	G8	H8	AD10	address/data 10
address/data 11	AD11	G9	H9	AD8	address/data 8
address/data 9	AD9	G10	H10	AD7	address/data 7
bus cmd/byte enable 0	CBE0#	G11	H11	AD5	address/data 5
address/data 6	AD6	G12	H12	AD3	address/data 3
address/data 4	AD4	G13	H13	AD1	address/data 1
address/data 2	AD2	G14	H14	AD0	address/data 0
coded	N/C	G15	H15	N/C	coded
5 volt supply	VCC	G16	H16	VIO	IO supply
5 volt supply	VCC	G17	H17	VCC	5 volt supply
ground	GND	G18	H18	GND	ground
ground	GND	G19	H19	GND	ground

3.5 Mini-PCI

The CB2051 allows you to add expansion cards complying to the Mini-PCI standard (type III). One such card can be inserted into the Mini-PCI slot available on the board.

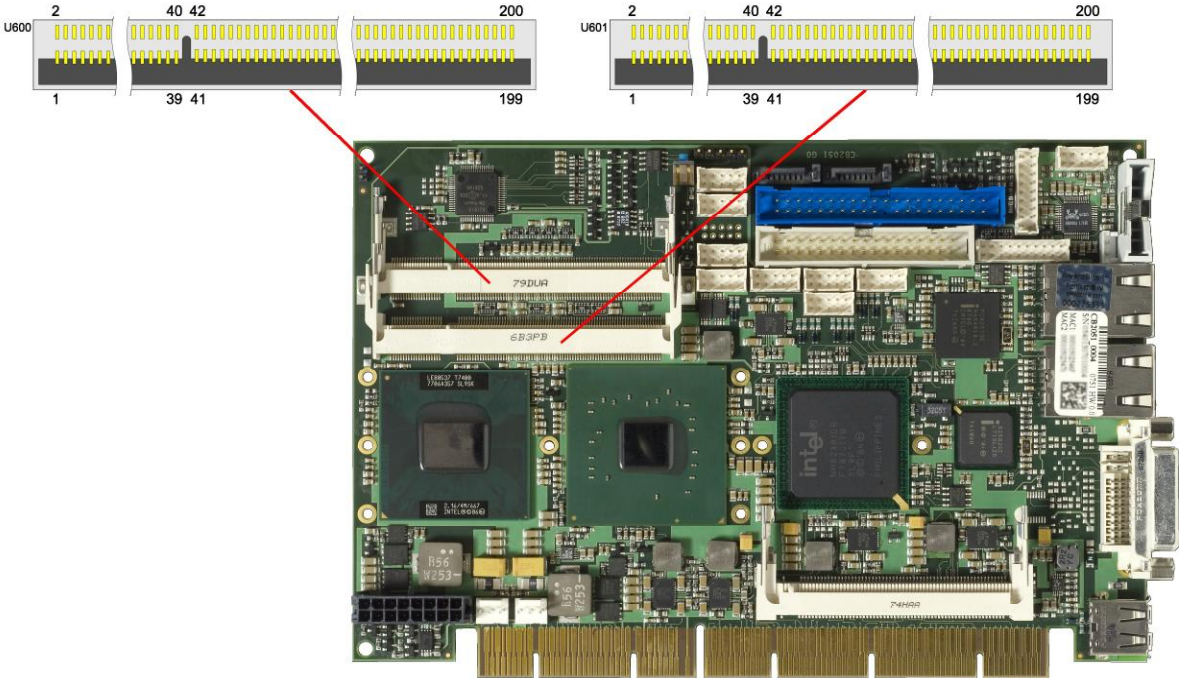


Description	Name	Pin		Name	Description
reserved	N/C	1	2	N/C	reserved
reserved	N/C	3	4	N/C	reserved
reserved	N/C	5	6	N/C	reserved
reserved	N/C	7	8	N/C	reserved
reserved	N/C	9	10	N/C	reserved
reserved	N/C	11	12	N/C	reserved
reserved	N/C	13	14	N/C	reserved
reserved	N/C	15	16	N/C	reserved
interrupt B	INTB#	17	18	VCC	5 volt supply
3.3 volt supply	3.3V	19	20	INTA#	interrupt A
reserved	N/C	21	22	N/C	reserved
ground	GND	23	24	S3.3V	3.3 volt supply
PCI clock	PCLK	25	26	PRST#	reset
ground	GND	27	28	3.3V	3.3 volt supply
PCI request	REQ#	29	30	GNT#	PCI grant
3.3 volt supply	3.3V	31	32	GND	ground
address/data 31	AD31	33	34	PME#	power management event
address/data 29	AD29	35	36	N/C	reserved
ground	GND	37	38	AD30	address/data 30
address/data 27	AD27	39	40	3.3V	3.3 volt supply
address/data 25	AD25	41	42	AD28	address/data 28
reserved	N/C	43	44	AD26	address/data 26
bus cmd/byte enables 3	CBE3#	45	46	AD24	address/data 24
address/data 23	AD23	47	48	IDSEL	init device select
ground	GND	49	50	GND	ground
address/data 21	AD21	51	52	AD22	address/data 22
address/data 19	AD19	53	54	AD20	address/data 20
ground	GND	55	56	PAR	parity
address/data 17	AD17	57	58	AD18	address/data 18

Description	Name	Pin		Name	Description
bus cmd/byte enables 2	CBE2#	59	60	AD16	address/data 16
initiator ready	IRDY#	61	62	GND	ground
3.3 volt supply	3.3V	63	64	FRAME#	cycle frame
clock running	CLKRUN#	65	66	TRDY#	target ready
system error	SERR#	67	68	STOP#	stop request by target
ground	GND	69	70	3.3V	3.3 volt supply
parity error	PERR#	71	72	DEVSEL#	device select
bus cmd/byte enables 1	CBE1#	73	74	GND	ground
address/data 14	AD14	75	76	AD15	address/data 15
ground	GND	77	78	AD13	address/data 13
address/data 12	AD12	79	80	AD11	address/data 11
address/data 10	AD10	81	82	GND	ground
ground	GND	83	84	AD9	address/data 9
address/data 8	AD8	85	86	CBE0#	bus cmd/byte enables 0
address/data 7	AD7	87	88	3.3V	3.3 volt supply
3.3 volt supply	3.3V	89	90	AD6	address/data 6
address/data 5	AD5	91	92	AD4	address/data 4
reserved	N/C	93	94	AD2	address/data 2
address/data 3	AD3	95	96	AD0	address/data 0
5 volt supply	VCC	97	98	N/C	reserved
address/data 1	AD1	99	100	N/C	reserved
ground	GND	101	102	GND	ground
reserved	N/C	103	104	GND	ground
reserved	N/C	105	106	N/C	reserved
reserved	N/C	107	108	N/C	reserved
reserved	N/C	109	110	N/C	reserved
reserved	N/C	111	112	N/C	reserved
reserved	N/C	113	114	GND	ground
reserved	N/C	115	116	N/C	reserved
reserved	N/C	117	118	N/C	reserved
reserved	N/C	119	120	N/C	reserved
reserved	N/C	121	122	N/C	reserved
5 volt supply	VCC	123	124	S3.3V	3.3 volt supply

3.6 Memory

Conventional SO-DIMM200 memory modules, as familiar from notebook computers, are used to equip the board with memory. For mechanical reasons it is possible that particular memory modules cannot be employed. Please ask your distributor for recommended memory modules.
With currently available SO-DIMM200 modules a memory extension up to 2 GByte is possible (DDR2-667).
All timing parameters for different memory modules are automatically set by BIOS.



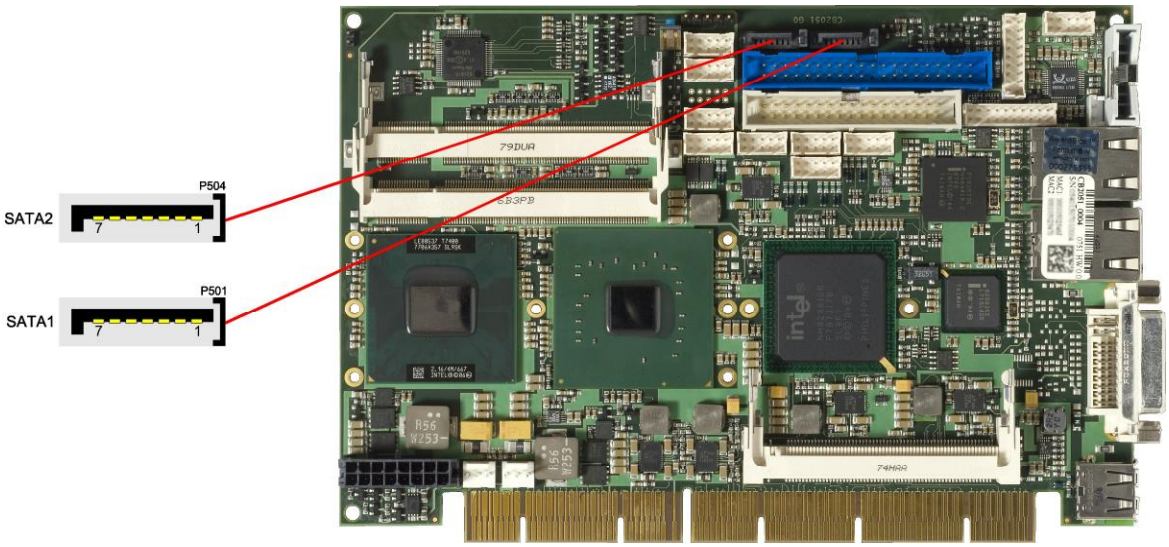
Description	Name	Pin		Name	Description
memory reference current	REF	1	2	GND	ground
ground	GND	3	4	DQ4	data 4
data 0	DQ0	5	6	DQ5	data 5
data 1	DQ1	7	8	GND	ground
ground	GND	9	10	DQM0	data mask 0
data strobe 0 -	DQS0#	11	12	GND	ground
data strobe 0 +	DQS0	13	14	DQ6	data 6
ground	GND	15	16	DQ7	data 7
data 2	DQ2	17	18	GND	ground
data 3	DQ3	19	20	DQ12	data 12
ground	GND	21	22	DQ13	data 13
data 8	DQ8	23	24	GND	ground
data 9	DQ9	25	26	DQM1	data mask 1
ground	GND	27	28	GND	ground
data strobe 1 -	DQS1#	29	30	CK0	clock 0 +
data strobe 1 +	DQS1	31	32	CK0#	clock 0 -
ground	GND	33	34	GND	ground
data 10	DQ10	35	36	DQ14	data 14
data 11	DQ11	37	38	DQ15	data 15
ground	GND	39	40	GND	ground

Description	Name	Pin		Name	Description
ground	GND	41	42	GND	ground
data 16	DQ16	43	44	DQ20	data 20
data 17	DQ17	45	46	DQ21	data 21
ground	GND	47	48	GND	ground
data strobe 2 -	DQS2#	49	50	N/C	reserved
data strobe 2 +	DQS2	51	52	DQM2	data mask 2
ground	GND	53	54	GND	ground
data 18	DQ18	55	56	DQ22	data 22
data 19	DQ19	57	58	DQ23	data 23
ground	GND	59	60	GND	ground
data 24	DQ24	61	62	DQ28	data 28
data 25	DQ25	63	64	DQ29	data 29
ground	GND	65	66	GND	ground
data mask 3	DQM3	67	68	DQS3#	data strobe 3 -
reserved	N/C	69	70	DQS3	data strobe 3 +
ground	GND	71	72	GND	ground
data 26	DQ26	73	74	DQ30	data 30
data 27	DQ27	75	76	DQ31	data 31
ground	GND	77	78	GND	ground
clock enables 0	CKE0	79	80	CKE1	clock enables 1
1.8 volt supply	1.8V	81	82	1.8V	1.8 volt supply
reserved	N/C	83	84	N/C	reserved
SDRAM bank 2	BA2	85	86	N/C	reserved
1.8 volt supply	1.8V	87	88	1.8V	1.8 volt supply
address 12	A12	89	90	A11	address 11
address 9	A9	91	92	A7	address 7
address 8	A8	93	94	A6	address 6
1.8 volt supply	1.8V	95	96	1.8V	1.8 volt supply
address 5	A5	97	98	A4	address 4
address 3	A3	99	100	A12	address 2
address 1	A1	101	102	A0	address 0
1.8 volt supply	1.8V	103	104	1.8V	1.8 volt supply
address 10	A10	105	106	BA1	SDRAM bank 1
SDRAM bank 0	BA0	107	108	RAS#	row address strobe
write enable	WE#	109	110	S0#	chip select 0
1.8 volt supply	1.8V	111	112	1.8V	1.8 volt supply
column address strobe	CAS#	113	114	ODT0	on die termination 0
chip select 1	S1#	115	116	A13	address 13
1.8 volt supply	1.8V	117	118	1.8V	1.8 volt supply
on die termination 1	ODT1	119	120	N/C	reserved
ground	GND	121	122	GND	ground
data 32	DQ32	123	124	DQ36	data 36
data 33	DQ33	125	126	DQ37	data 37
ground	GND	127	128	GND	ground
data strobe 4 -	DQS4#	129	130	DQM4	data mask 4
data strobe 4 +	DQS4	131	132	GND	ground
ground	GND	133	134	DQ38	data 38
data 34	DQ34	135	136	DQ39	data 39
data 35	DQ35	137	138	GND	ground
ground	GND	139	140	DQ44	data 44
data 40	DQ40	141	142	DQ45	data 45
data 41	DQ41	143	144	GND	ground
ground	GND	145	146	DQS5#	data strobe 5 -
data mask 5	DQM5	147	148	DQS5	data strobe 5 +
ground	GND	149	150	GND	ground

Description	Name	Pin		Name	Description
data 42	DQ42	151	152	DQ46	data 46
data 43	DQ43	153	154	DQ47	data 47
ground	GND	155	156	GND	ground
data 48	DQ48	157	158	DQ52	data 52
data 49	DQ49	159	160	DQ53	data 53
ground	GND	161	162	GND	ground
test	TEST	163	164	CK1	clock 1 +
ground	GND	165	166	CK1#	clock 1 -
data strobe 6 -	DQS6#	167	168	GND	ground
data strobe 6	DQS6	169	170	DQM6	data mask 6
ground	GND	171	172	GND	ground
data 50	DQ50	173	174	DQ54	data 54
data 51	DQ51	175	176	DQ55	data 55
ground	GND	177	178	GND	ground
data 56	DQ56	179	180	DQ60	data 60
data 57	DQ57	181	182	DQ61	data 61
ground	GND	183	184	GND	ground
data mask 7	DQM7	185	186	DQS7#	data strobe 7 -
ground	GND	187	188	DQS7	data strobe 7 +
data 58	DQ58	189	190	GND	ground
data 59	DQ59	191	192	DQ62	data 62
ground	GND	193	194	DQ63	data 63
SMBus data	SDA	195	196	GND	ground
SMBus clock	SCL	197	198	SA0	SPD address
3.3 volt supply	3.3V	199	200	SA1	SPD address

3.7 SATA Interfaces

The CB2051 provides two SATA interfaces allowing transfer rates of up to 3 GBit per second. These interfaces are made available via two 7 pin connectors.
The required settings are made in the BIOS setup.

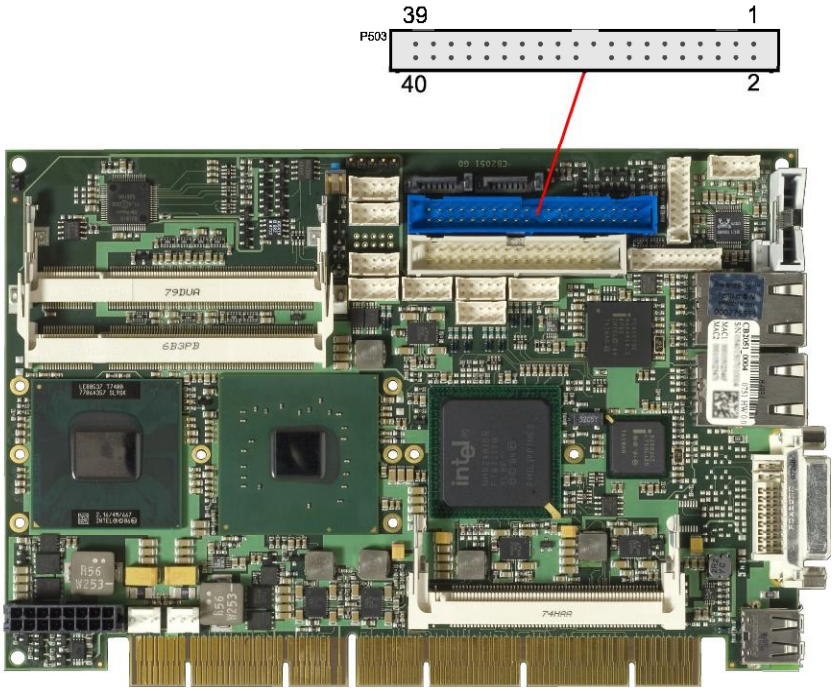


Pinbelegung SATA:

Pin	Name	Beschreibung
1	GND	Masse
2	SATATX	SATA Senden +
3	SATATX#	SATA Senden -
4	GND	Masse
5	SATARX	SATA Empfangen +
6	SATARX#	SATA Empfangen -
7	GND	Masse

3.8 IDE interface

To connect IDE devices you can plug a ribbon cable into the standard 40pin connector.

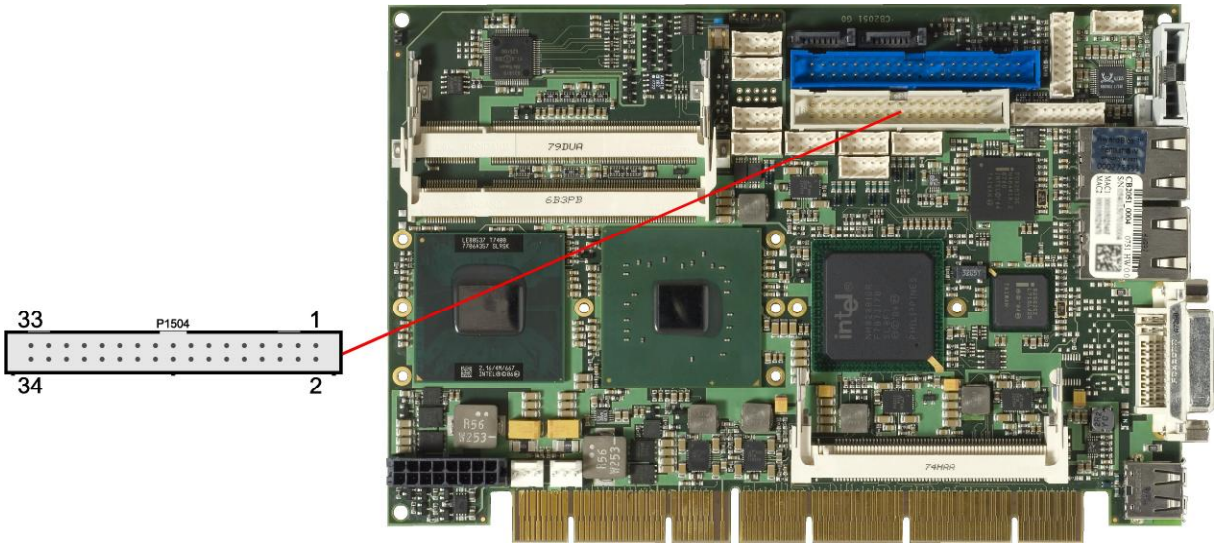


Pinout IDE interface:

Description	Name	Pin		Name	Description
reset	PRST#	1	2	GND	ground
data bit 7	PDD7	3	4	PDD8	data bit 8
data bit 6	PDD6	5	6	PDD9	data bit 9
data bit 5	PDD5	7	8	PDD10	data bit 10
data bit 4	PDD4	9	10	PDD11	data bit 11
data bit 3	PDD3	11	12	PDD12	data bit 12
data bit 2	PDD2	13	14	PDD13	data bit 13
data bit 1	PDD1	15	16	PDD14	data bit 14
data bit 0	PDD0	17	18	PDD15	data bit 15
ground	GND	19	20	N/C	coded
DMA request signal	PDDREQ	21	22	GND	ground
write signal	PDIOW#	23	24	GND	ground
read signal	PDIOR#	25	26	GND	ground
ready signal	PDRDY	27	28	N/C	reserved
DMA acknowledge signal	PDDACK#	29	30	GND	ground
interrupt signal	PDIRQ	31	32	N/C	reserved
address bit 1	PDA1	33	34	PDMA66EN	enable UDMA66
address bit 0	PDA0	35	36	PDA2	address bit 2
chip select signal 0	PDSC0#	37	38	PDCS1#	chip select signal 1
LED	PHDLED	39	40	GND	ground

3.9 Floppy interface

A floppy drive can be attached using a standard 2x17-pin connector (FCI 75869-306LF) for ribbon cables.

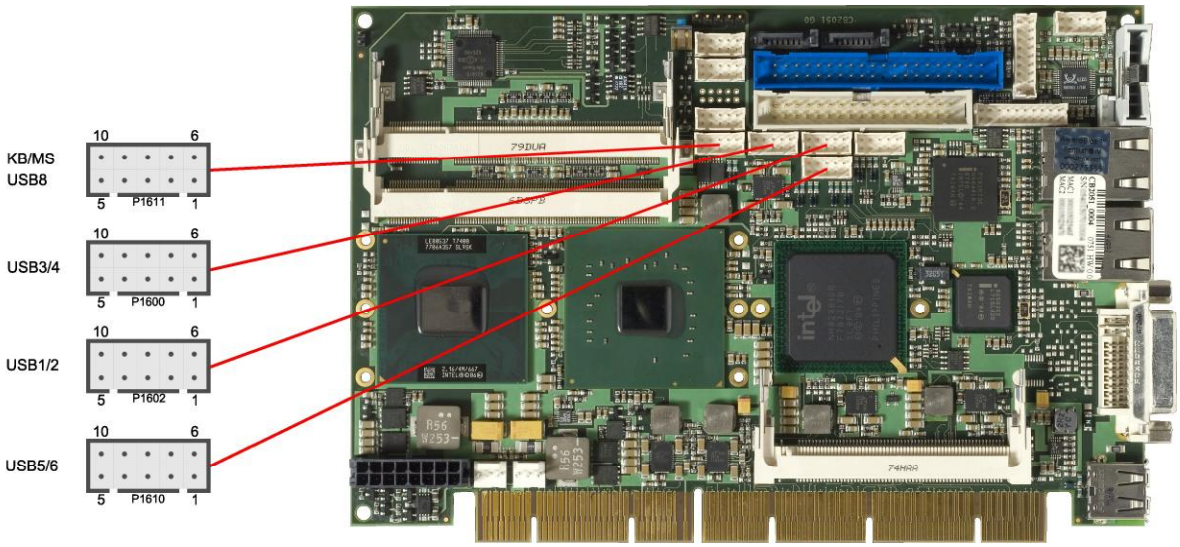


Pinout FDD 2x17 pin connector:

Description	Name	Pin		Name	Description
ground	GND	1	2	DRVDEN0	drive density sel 0
ground	GND	3	4	N/C	reserved
ground	GND	5	6	DRVDEN1	drive density sel 1
ground	GND	7	8	IDX#	index
ground	GND	9	10	MT0#	motor enable 0
ground	GND	11	12	DR1#	drive sel 1
ground	GND	13	14	DR0#	drive sel 0
ground	GND	15	16	MT1#	motor enable 1
ground	GND	17	18	DIR#	direction
ground	GND	19	20	STP#	step
ground	GND	21	22	WD#	write data
ground	GND	23	24	WE#	write enable
ground	GND	25	26	TR0#	track 0
ground	GND	27	28	WPRT#	write protect
reserved	N/C	29	30	RDATA#	read data
ground	GND	31	32	HDSL#	head select
reserved	N/C	33	34	DC#	disk change

3.10 USB, Keyboard/Mouse

The CB2051 offers eight USB channels one of which (USB7) is available as a standard USB connector. The other seven (USB1-6 and USB8) are provided via four 2x5pin connectors. In the case of USB8 the 2x5pin connector also integrates signals for keyboard and mouse.



Pinout 2x5 pin connector USB 1/2

Description	Name	Pin		Name	Description
5 volt for USB1	VCC	1	6	VCC	5 volt for USB2
minus channel USB1	USB1#	2	7	USB2#	minus channel USB2
plus channel USB1	USB1	3	8	USB2	plus channel USB2
ground	GND	4	9	GND	ground
reserved	N/C	5	10	N/C	reserved

Pinout 2x5 pin connector USB 3/4

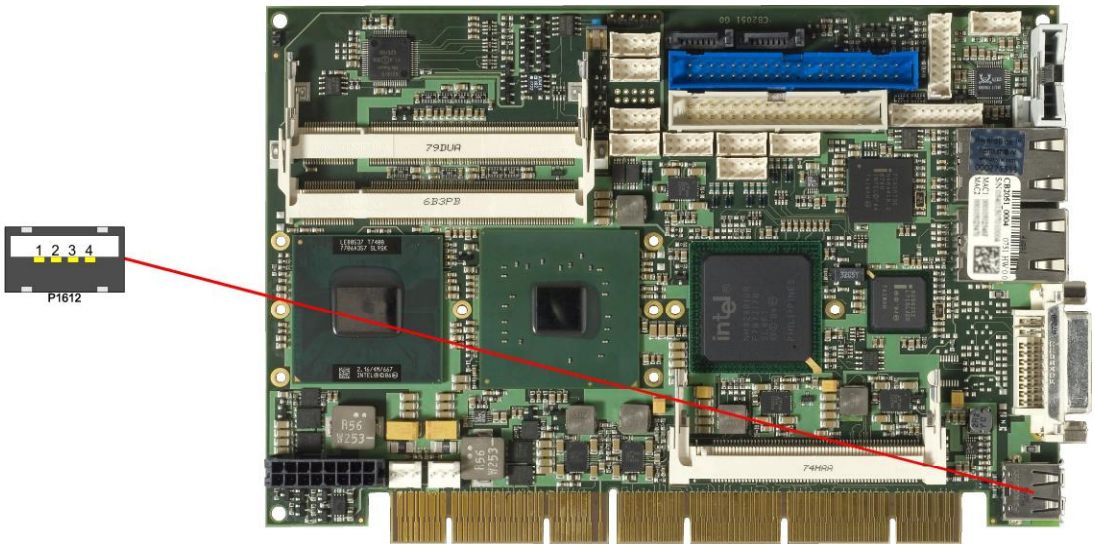
Description	Name	Pin		Name	Description
5 volt for USB3	VCC	1	6	VCC	5 volt for USB4
minus channel USB3	USB3#	2	7	USB4#	minus channel USB4
plus channel USB3	USB3	3	8	USB4	plus channel USB4
ground	GND	4	9	GND	ground
reserved	N/C	5	10	N/C	reserved

Pinout 2x5 pin connector USB 5/6

Description	Name	Pin		Name	Description
5 volt for USB5	VCC	1	6	VCC	5 volt for USB6
minus channel USB5	USB5#	2	7	USB6#	minus channel USB6
plus channel USB5	USB5	3	8	USB6	plus channel USB6
ground	GND	4	9	GND	ground
reserved	N/C	5	10	N/C	reserved

Pinout 2x5 pin connector USB 8/Keyboard-Mouse

Description	Name	Pin		Name	Description
5 volt for USB8	VCC	1	6	VCC	5 volt supply
minus channel USB8	USB8#	2	7	KCLK	keyboard clock
plus channel USB8	USB8	3	8	KDAT	keyboard data
ground	GND	4	9	MCLK	mouse clock
reserved	N/C	5	10	MDAT	mouse data

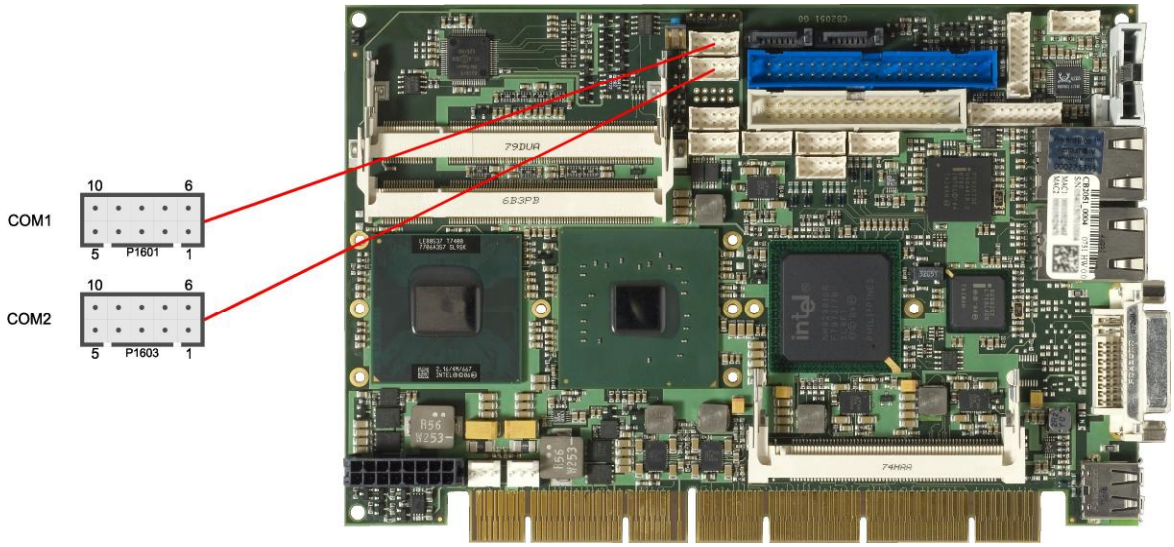


Pinout USB connector for channel X:

Pin	Name	Description
1	VCC	5 volt for USBX
2	USBX#	minus channel USBX
3	USBX	plus channel USBX
4	GND	ground

3.11 Serial Interfaces COM1 & COM2

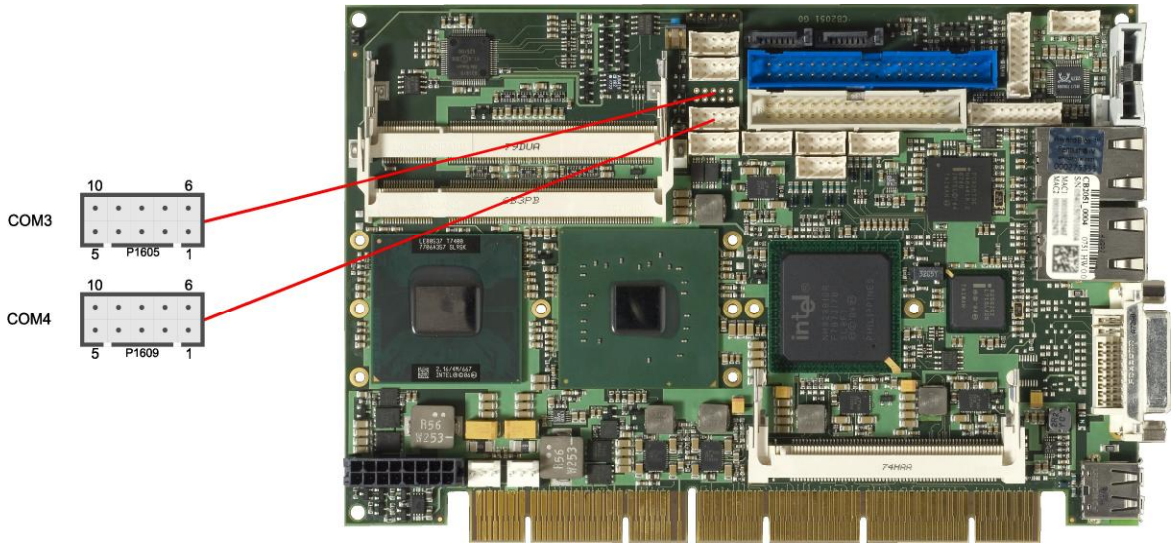
The serial interfaces COM1 and COM2 are made available via two 2x5 pin connectors (JST B10B-PHDSSLFSN, mating connector: PHDR-10VS). According to the product order, TTL level signals or RS232 standard signals are provided.
The port address and the interrupt are set via the BIOS setup.



Description	Name	Pin		Name	Description
data carrier detect	DCD	1	6	DSR	data set ready
receive data	RXD	2	7	RTS	request to send
transmit data	TXD	3	8	CTS	clear to send
data terminal ready	DTR	4	9	RI	ring indicator
ground	GND	5	10	VCC	5 volt supply

3.12 Serial Interfaces COM3 & COM4

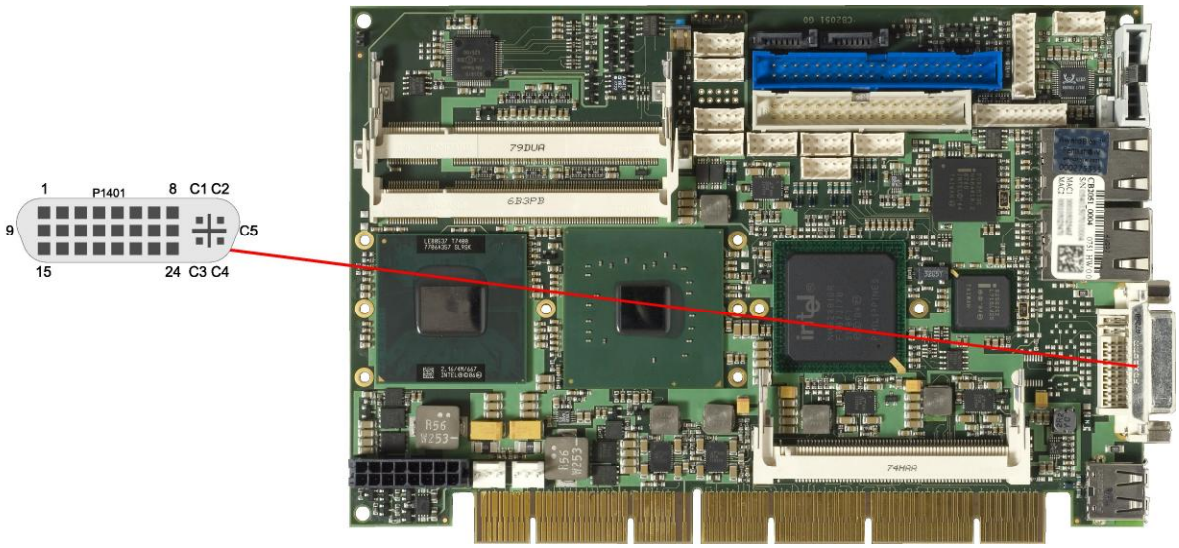
The serial interfaces COM1 and COM2 are made available via two 2x5 pin connectors (JST B10B-PHDSSLFSN, mating connector: PHDR-10VS). According to the product order, TTL level signals or RS232 standard signals are provided.
The port address and the interrupt are set via the BIOS setup.



Description	Name	Pin		Name	Description
data carrier detect	DCD	1	6	DSR	data set ready
receive data	RXD	2	7	RTS	request to send
transmit data	TXD	3	8	CTS	clear to send
data terminal ready	DTR	4	9	RI	ring indicator
ground	GND	5	10	VCC	5 volt supply

3.13 VGA/DVI

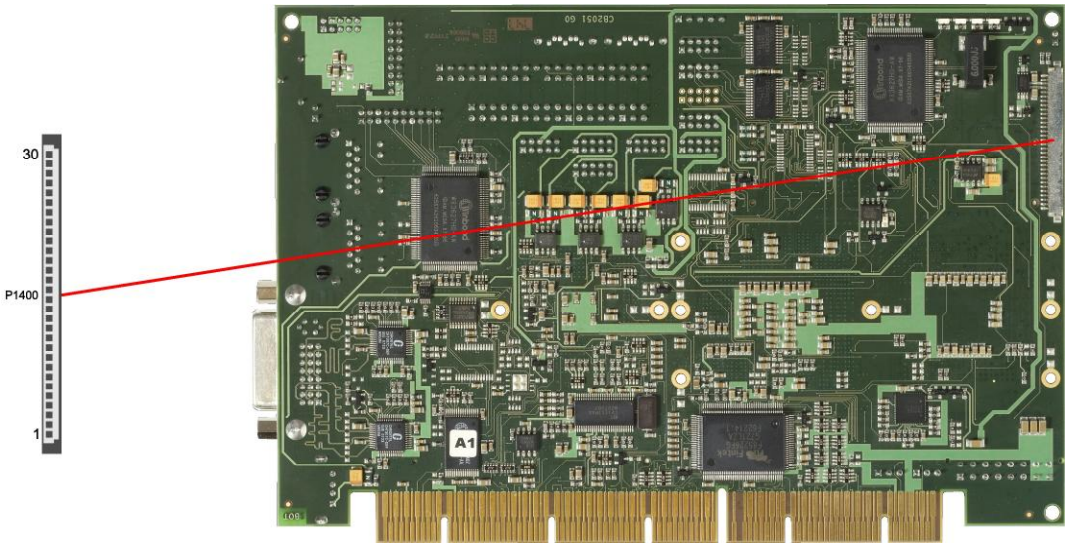
The module is equipped with a standard DVI-I-connector, which can be used to connect either a DVI capable display or a standard VGA CRT – using a DVI-DSUB adapter, if necessary.



Pin	Name	Description
1	TMDSDAT2#	DVI data 2
2	TMDSDAT2	DVI data 2
3	GND	ground
4	N/C	reserved
5	N/C	reserved
6	DDC CLK	DDC clock (DVI/VGA)
7	DDC DAT	DDC data (DVI/VGA)
8	VSYNC	VGA vertical sync
9	TMDSDAT1#	DVI data 1
10	TMDSDAT1	DVI data 1
11	GND	ground
12	N/C	reserved
13	N/C	reserved
14	VCC	5 volt supply
15	GND	ground
16	HP_DETECT	hot plug detect
17	TMDSDAT0#	DVI data 0
18	TMDSDAT0	DVI data 0
19	GND	ground
20	N/C	reserved
21	N/C	reserved
22	GND	ground
23	TMDS CLK	DVI clock
24	TMDS CLK#	DVI clock
C1	RED	VGA red
C2	GREEN	VGA green
C3	BLUE	VGA blue
C4	HSYNC	VGA horizontal sync
C5	GND	ground

3.14 LVDS

The board also offers the possibility to use displays with LVDS interface. These can be connected via a 30 pin flat-cable plug (JAE FI-X30S-HF-NPB, mating connector: FI-X30C(2)-NPB). Only shielded and twisted cables may be used. The display type is to be chosen over the BIOS setup. The connector has two additional shield pins S1 and S2 which are omitted in the pinout table below.



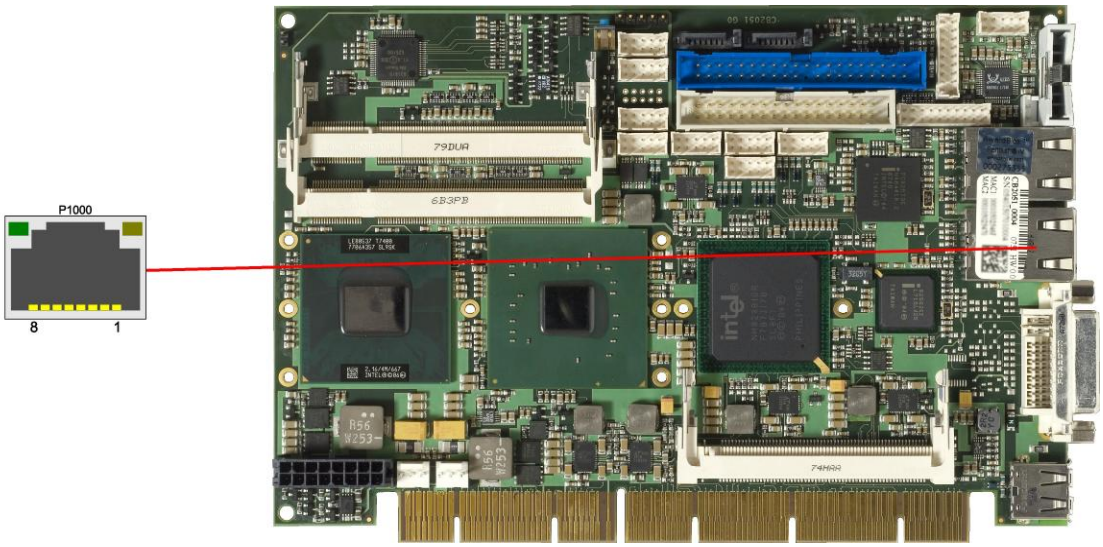
Pinout LVDS connector:

Pin	Name	Description
1	TXO00#	LVDS even data 0 -
2	TXO00	LVDS even data 0 +
3	TXO01#	LVDS even data 1 -
4	TXO01	LVDS even data 1 +
5	TXO02#	LVDS even data 2 -
6	TXO02	LVDS even data 2 +
7	GND	ground
8	TXO0C#	LVDS even clock -
9	TXO0C	LVDS even clock +
10	TXO03#	LVDS even data 3 -
11	TXO03	LVDS even data 3 +
12	TXO10#	LVDS odd data 0 -
13	TXO10	LVDS odd data 0 +
14	GND	ground
15	TXO11#	LVDS odd data 1 -
16	TXO11	LVDS odd data 1 +
17	GND	ground
18	TXO12#	LVDS odd data 2 -
19	TXO12	LVDS odd data 2 +
20	TXO1C#	LVDS odd clock -
21	TXO1C	LVDS odd clock +
22	TXO13#	LVDS odd data 3 -
23	TXO13	LVDS odd data 3 +
24	GND	ground
25	3.3V	3.3 volt supply
26	DDC_CLK	EDID clock for LCD
27	DDC_DAT	EDID data for LCD

Pin	Name	Description
28	FP_3.3V	switched 3.3 volt for display
29	FP_BL	switched 5 volt for backlight
30	VCC	5 volt supply

3.15 LAN1

The module has two LAN interfaces. LAN1 supports 10BaseT and 100BaseT compatible net components with automatic bandwidth selection. It also offers auto-cross and auto-negotiate functionality. The controller chip is the Intel® 82562. PXE and RPL functions are also supported.

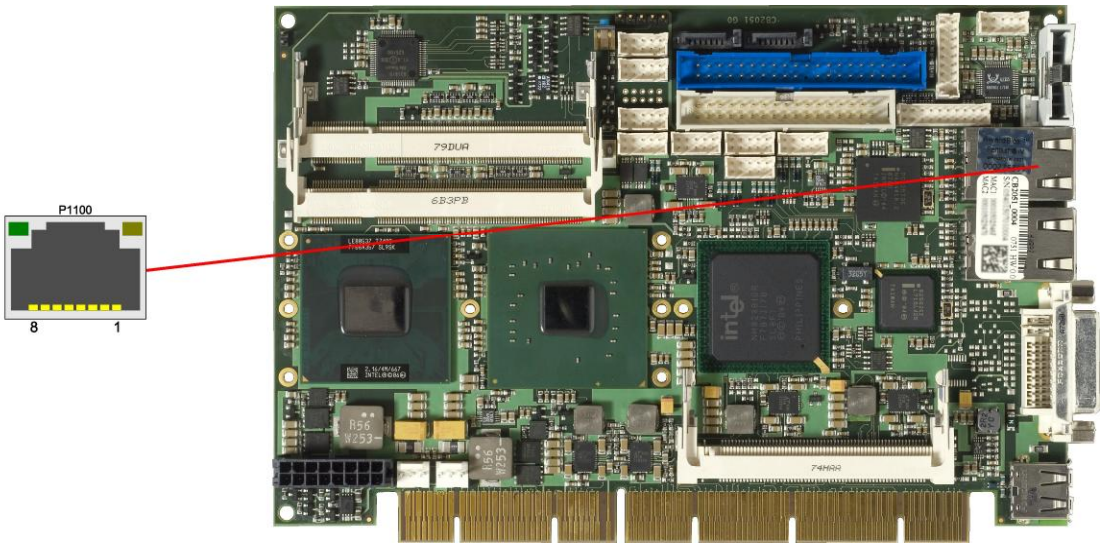


Pinout LAN 10/100:

Pin	Name	Description
1	LAN1-0	LAN1 transmit plus
2	LAN1-0#	LAN1 transmit minus
3	LAN1-1	LAN1 receive plus
4	N/C	reserved
5	N/C	reserved
6	LAN1-1#	LAN1 receive minus
7	N/C	reserved
8	N/C	reserved

3.16 LAN2

LAN2 supports 10BaseT, 100BaseT and 1000BaseT compatible net components with automatic bandwidth selection. It does not offer auto-cross and auto-negotiate functionality. The controller chip is the Intel® 82573L(E). PXE and RPL functions are not supported.

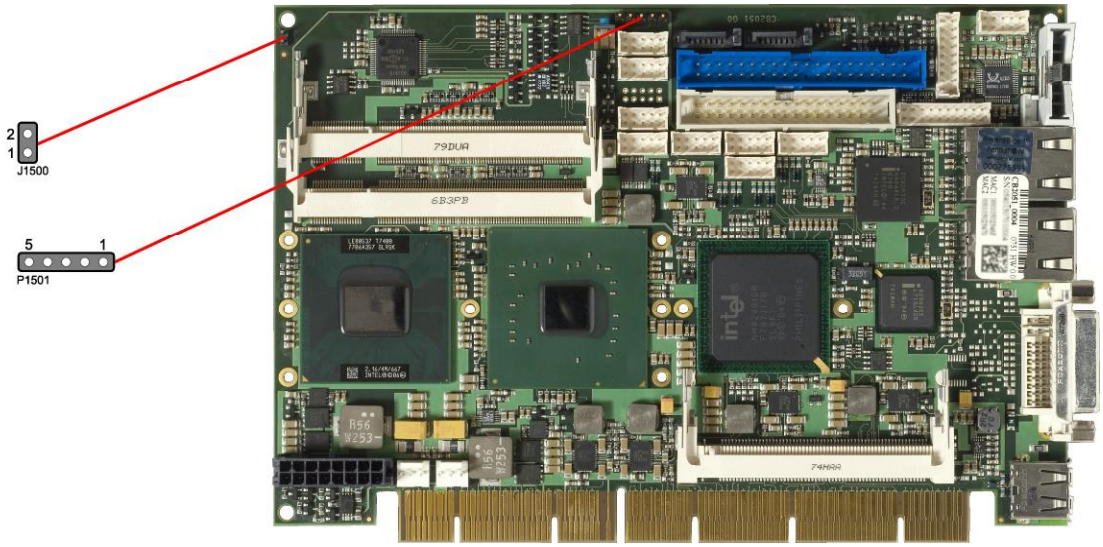


Pinout LAN 10/100/1000:

Pin	Name	Description
1	LAN2-0	LAN2 channel 0 plus
2	LAN2-0#	LAN2 channel 0 minus
3	LAN2-1	LAN2 channel 1 plus
4	LAN2-1#	LAN2 channel 1 minus
5	LAN2-2	LAN2 channel 2 plus
6	LAN2-2#	LAN2 channel 2 minus
7	LAN2-3	LAN2 channel 3 plus
8	LAN2-3#	LAN2 channel 3 minus

3.17 Touch Screen

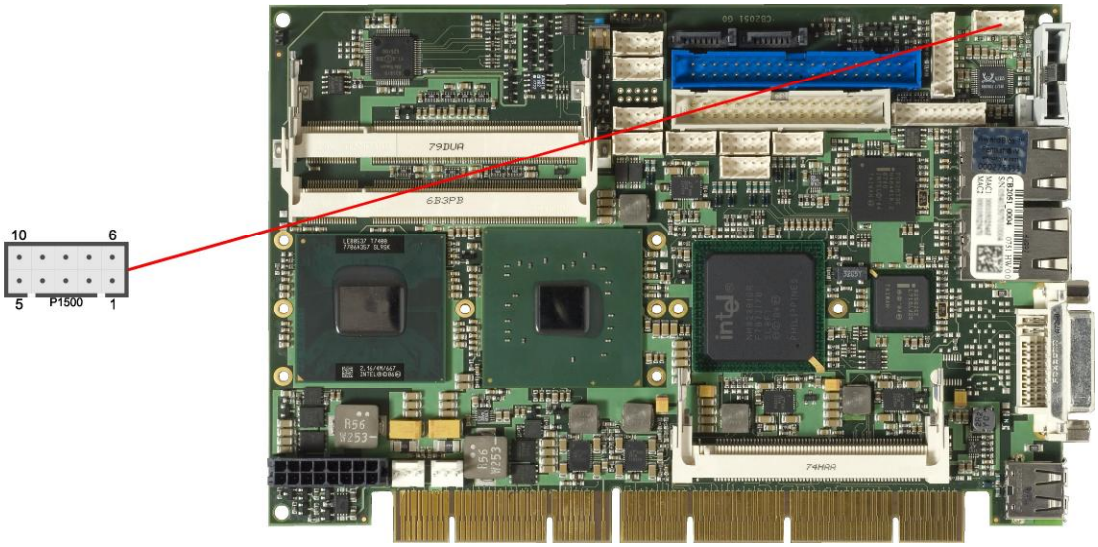
A key feature of the CB2051 is the possibility to connect a touch screen. Both 4-wire and 5-wire resistive touch screens are supported. For receiving the relevant signals a 5 pin standard IDC socket connector with a spacing of 2.54 mm is provided. If the connected touch screen is 4-wire then pin 1 will not be used. Next to this connector is a jumper which, if shorted at boot time, triggers the NVRST-signal in the controller, thereby resetting all parameters of NVRAM to default values.
Conversion to the respective connector of the touch screen must be provided externally. Please consult the manufacturer's documentation to figure out the relevant technical details.
Note: In the pinout table below H, X, S, Y, and L are the signal names in the case of 5-wire, XL, XR, YT, and YB are the names in the case of 4-wire.



Pin	Name	Description
1	H-DRV	H driver control
2	X/XL-DRV	X/XL driver control
3	S/XR-DRV	S/XR driver control
4	Y/YT-DRV	Y/YT driver control
5	L/YB-DRV	L/YB driver control

3.18 Audio

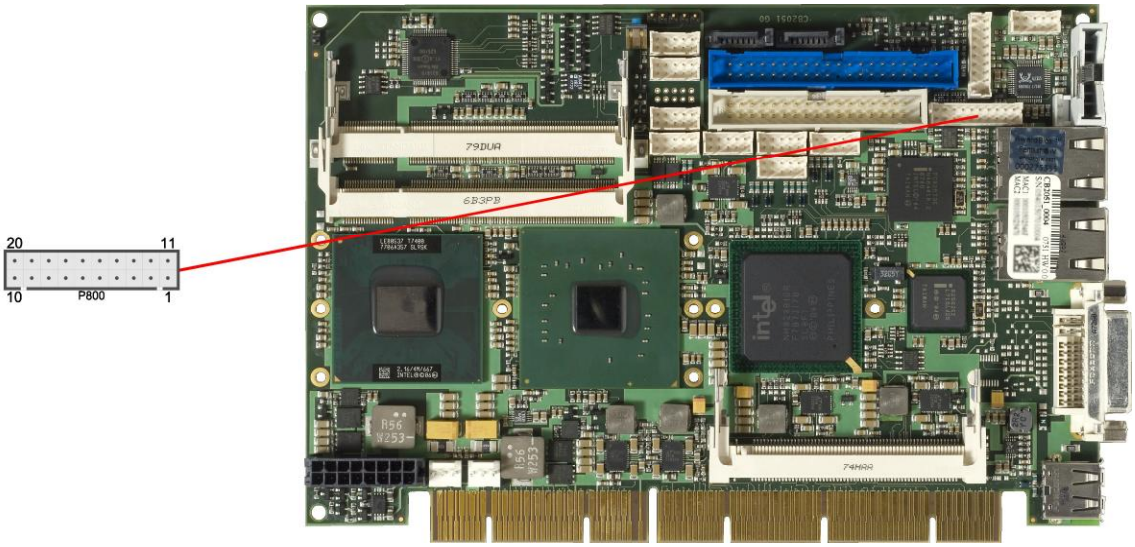
Audio input and output functions can be accessed via a 2x5 pin connector (JST B10B-PHDSSLFSN, mating connector: PHDR-10VS). There are two ways to use this connector. Default functionality is the familiar audio in, audio out, and microphone. OS dependent device drivers can switch these signals to support an 5.1 output; thus in this mode no audio input signals are available.
Signals "SPDIFI" and "SPDIFO" provide digital input and output. If a transformation to a coaxial or optical connector is necessary this must be performed externally.



Description	Name	Pin		Name	Description
digital output SPDIF	SPDIFO	1	6	3.3V	3.3 volt supply
digital input SPDIF	SPDIFI	2	7	S_AGND	analog ground sound
sound output right / front output right	LOUT_R / FRONT_R	3	8	LOUT_L / FRONT_L	sound output left / front output left
AUX input right / rear output right	AUXA_R / REAR_R	4	9	AUXA_L / REAR_L	AUX input left / rear output left
microphone input 1 / center output	MIC1 / CENTER	5	10	MIC2 / LFE	microphone input 2 / LFE output

3.19 GPIO

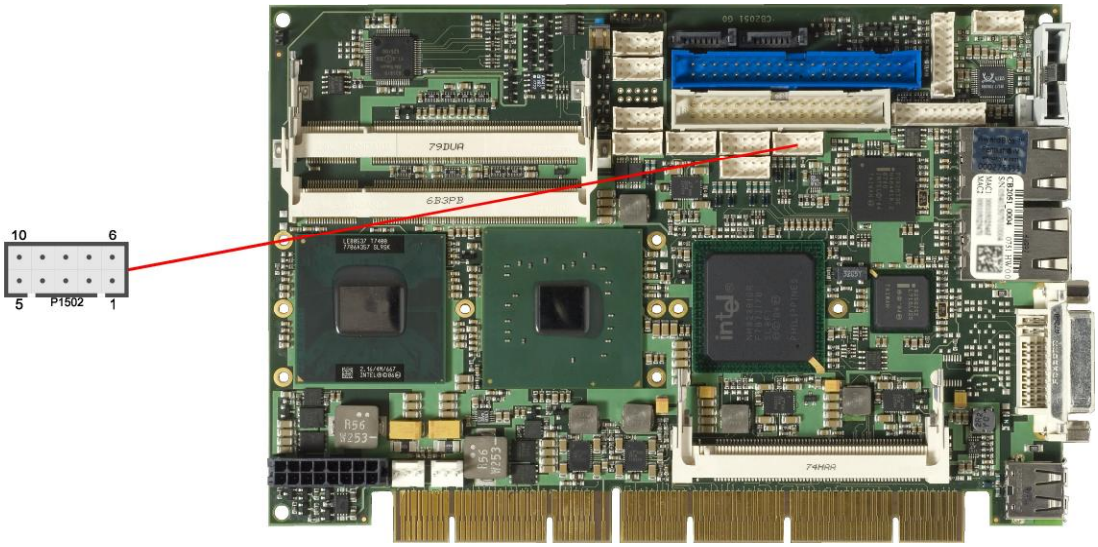
The General Purpose Input/Output interface is made available through a 2x10 pin connector (JST B20B-PHDSSLFSN, mating connector: PHDR-20VS). To make use of this interface the SIO2 unit (Winbond W83627) must be programmed accordingly. Please refer to your distributor for information on available software support.



Description	Name	Pin		Name	Description
5 volt supply	VCC	1	11	VCC	5 volt supply
GP input/output 10	GPIO10	2	12	GPIO20	GP input/output 20
GP input/output 11	GPIO11	3	13	GPIO21	GP input/output 21
GP input/output 12	GPIO12	4	14	GPIO22	GP input/output 22
GP input/output 13	GPIO13	5	15	GPIO23	GP input/output 23
GP input/output 14	GPIO14	6	16	GPIO24	GP input/output 24
GP input/output 15	GPIO15	7	17	GPIO25	GP input/output 25
GP input/output 16	GPIO16	8	18	GPIO26	GP input/output 26
GP input/output 17	GPIO17	9	19	GPIO27	GP input/output 27
ground	GND	10	20	GND	ground

3.20 SMB/I2C

The CB2051 can communicate with external devices via the SMBus protocol or the I2C protocol. The signals for these protocols are available through a 2x5 pin connector (JST B10B-PHDSSLFSN, mating connector: PHDR-10VS). The SMBus signals are processed by the ICH chip (Intel 82801), the I2C signals are processed by the SIO1 unit (Winbond W83627).

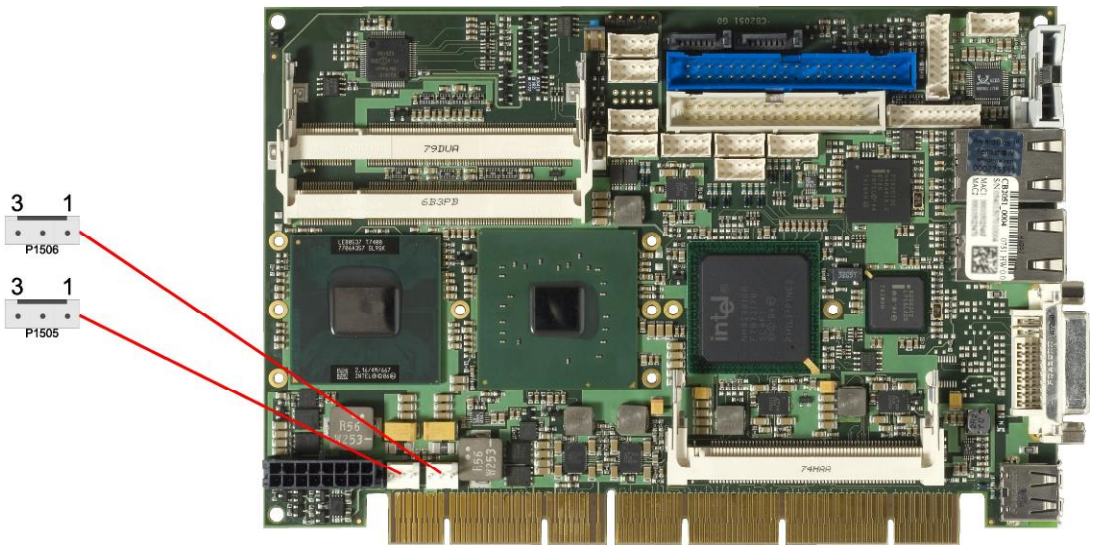


Pinout SMBus/I2C connector:

Description	Name	Pin		Name	Description
3.3 volt supply	3.3V	1	6	GND	ground
SMBus clock	SMBCLK	2	7	SMBDAT	SMBus data
SMBus alarm	SMBALRT#	3	8	SVCC	standby supply 5V
I2C bus clock	I2CLK	4	9	I2DAT	I2C bus data
5 volt supply	VCC	5	10	GND	ground

3.21 Fan Connectors

Two 3 pin connectors are available for controlling and monitoring external fans (12 volt). For the monitoring the fans must provide a corresponding speed signal.



Pinout fan connector:

Pin	Name	Description
1	GND	ground
2	12V	12 volt supply regulated
3	TACHO	fan monitoring signal

4 BIOS Settings

4.1 Remarks for Setup Use

In a setup page, standard values for its setup entries can be loaded. Fail-safe defaults are loaded with F6 and optimized defaults are loaded with F7. These standard values are independent of the fact that a board has successfully booted with a setup setting before.
This is different if these defaults are called from the Top Menu. Once a setup setting was saved, which subsequently leads to a successful boot process, those values are loaded as default for all setup items afterwards.
See also the chapters “Load Fail-Safe Defaults" (5.10) and “Load Optimized Defaults” (5.11).

NOTE

BIOS features and setup options are subject to change without further notice. The settings displayed in the screenshots on the following pages are meant to be examples only. Neither do they represent the recommended settings nor the default settings. What the appropriate settings are depends entirely on the particular application scenario in which the board is used.

4.2 Top Level Menu

```
                    Phoenix – AwardBIOS CMOS Setup Utility
 ► Standard CMOS Features          ► Frequency/Voltage Control
 ► Advanced BIOS Features            Load Fail-Safe Defaults
 ► Advanced Chipset Features         Load Optimized Defaults
 ► Integrated Peripherals            Set Password
 ► Power Management Setup            Save & Exit Setup
 ► PnP/PCI Configurations            Exit Without Saving
 ► PC Health Status
Esc : Quit                          ↑ ↓ → ←  : Select Item
F10 : Save & Exit Setup
                  "brief description of selected item"
```

The sign „►“ in front of an item means that there is a sub menu.
The „x“ sign in front of an item means, that the item is disabled but can be enabled by changing or selecting some other item (usually somewhere above the disabled item on the same screen).
Use the arrow buttons to navigate from one item to another. For selecting an item press Enter which will open either a sub menu or a dialog screen.

4.3 Standard CMOS Features

```
                    Phoenix – AwardBIOS CMOS Setup Utility
                              Standard CMOS Features
  Date (mm:dd:yy)                Wed, Mar 12 2008          Item Help
  Time (hh:mm:ss)                19 : 13 : 35

► IDE Channel 0 Master           [ None]
► IDE Channel 0 Slave            [ None]
► IDE Channel 1 Master           [ None]
► IDE Channel 1 Slave            [ None]
► SATA 0                         [ None]
► SATA 1                         [ None]
► SATA 2                         [ None]
► SATA 3                         [ None]

  Drive A                        [None]
  Halt On                        [No Errors]

  Base Memory                         640K
  Extended Memory                 1038336K
  Total Memory                    1039360K

  ↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
  F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **Date (mm:dd:yy)**
  Options: mm: month
  dd: day
  yy: year

- **Time (hh:mm:ss)**
  Options: hh: hours
  mm: minutes
  ss: seconds

- **IDE Channel 0 Master**
  Sub menu: see "IDE Channel 0 Master/Slave" (p. 44)

- **IDE Channel 0 Slave**
  Sub menu: see "IDE Channel 0 Master/Slave" (p. 44)

- **IDE Channel 1 Master**
  Sub menu: see "IDE Channel 0 Master/Slave" (p. 44)

- **IDE Channel 1 Slave**
  Sub menu: see "IDE Channel 0 Master/Slave" (p. 44)

- **SATA 0**
  Sub menu: see "SATA channels" (p. 45)

- **SATA 1**
  Sub menu: see "SATA channels" (p. 45)

- **SATA 2**
  Sub menu: see "SATA channels" (p. 45)

- **SATA 3**
  Sub menu: see "SATA channels" (p. 45)

- **Drive A**
  Options: None / 360K, 5.25 in. / 1.2M, 5.25 in. / 720K, 3.5 in. / 1.44M, 3.5 in. / 2.88M, 3.5 in.

- **Halt On**
  Options: All Errors / No Errors / All, But Keyboard / All, But Diskette / All, But Disk/Key

- **Base Memory**
  Options: none

- **Extended Memory**
  Options: none

- **Total Memory**
  Options: none

4.3.1 IDE Channel 0 Master/Slave

```
                    Phoenix – AwardBIOS CMOS Setup Utility
                              IDE Channel 0 Master
   IDE HDD Auto-Detection        [Press Enter]                 Item Help

   IDE Channel 0 Master          [Auto]
   Access Mode                   [Auto]

   Capacity                           0 MB

   Cylinder                           0
   Head                               0
   Precomp                            0
   Landing Zone                       0
   Sector                             0

 ↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **IDE HDD Auto-Detection**
  Options: none

- **IDE Channel 0 Master**
  Options: None / Auto / Manual

- **Access Mode**
  Options: CHS / LBA / Large / Auto

- **Capacity**
  Options: none

- **Cylinder**
  Options: none

- **Head**
  Options: none

- **Precomp**
  Options: none

- **Landing Zone**
  Options: none

- **Sector**
  Options: none

4.3.2 SATA channels

```
                    Phoenix – AwardBIOS CMOS Setup Utility
                                   SATA 0
IDE Auto-Detection            [Press Enter]          Item Help

Extended IDE Drive            [Auto]
Access Mode                   [Auto]

Capacity                           0 MB

Cylinder                           0
Head                               0
Precomp                            0
Landing Zone                       0
Sector                             0

↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **IDE Auto-Detection**
  Options: none

- **Extended IDE Drive**
  Options: None / Auto

- **Access Mode**
  Options: Large / Auto

- **Capacity**
  Options: none

- **Cylinder**
  Options: none

- **Head**
  Options: none

- **Precomp**
  Options: none

- **Landing Zone**
  Options: none

- **Sector**
  Options: none

4.4 Advanced BIOS Features

```
                    Phoenix – AwardBIOS CMOS Setup Utility
                            Advanced BIOS Features
  ► CPU Feature                    [Press Enter]      Item Help
  ► Hard Disk Boot Priority        [Press Enter]
    Virus Warning                  [Disabled]
    CPU L1 & L2 Cache              [Enabled]
    CPU L3 Cache                   [Enabled]
    Quick Power On Self Test       [Enabled]
    First Boot Device              [Hard Disk]
    Second Boot Device             [Hard Disk]
    Third Boot Device              [Disabled]
    Boot Other Device              [Enabled]
    Boot Up Floppy Seek            [Disabled]
    Boot Up NumLock Status         [On]
    Gate A20 Option                [Fast]
    Typematic Rate Setting         [Disabled]
  x Typematic Rate (Chars/Sec)      6
  x Typematic Delay (Msec)          250
    Security Option                [Setup]
    APIC Mode                      [Enabled]
    MPS Version Control For OS     [1.4]
    OS Select For DRAM > 64MB      [Non OS2]
    HDD S.M.A.R.T. Capability      [Enabled]
    Full Screen LOGO Show          [Disabled]
  ↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
  F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **CPU Feature**
  Sub menu: see "CPU Feature" (p. 48)

- **Hard Disk Boot Priority**
  Sub menu: see "Hard Disk Boot Priority" (p. 49)

- **Virus Warning**
  Options: Enabled / Disabled

- **CPU L1 & L2 Cache**
  Options: Enabled / Disabled

- **CPU L3 Cache**
  Options: Enabled / Disabled

- **Quick Power On Self Test**
  Options: Enabled / Disabled

- **First Boot Device**
  Options: Floppy / LS120 / Hard Disk / CDROM / ZIP100 / USB-FDD / USB-ZIP / USB-CDROM / LAN / Disabled

- **Second Boot Device**
  Options: Floppy / LS120 / Hard Disk / CDROM / ZIP100 / USB-FDD / USB-ZIP / USB-CDROM / LAN / Disabled

- **Third Boot Device**
  Options: Floppy / LS120 / Hard Disk / CDROM / ZIP100 / USB-FDD / USB-ZIP / USB-CDROM / LAN / Disabled

- **Boot Other Device**
  Options: Enabled / Disabled

- **Boot Up Floppy Seek**
  Options: Enabled / Disabled

- **Boot Up NumLock Status**
  Options: Off / On

- **Gate A20 Option**
  Options: Normal / Fast

- **Typematic Rate Setting**
  Options: Enabled / Disabled

- **Typematic Rate (Chars/Sec)**
  Options: 6 / 8 / 10 / 12 / 15 / 20 / 24 / 30

- **Typematic Delay (Msec)**
  Options: 250 / 500 / 750 / 1000

- **Security Option**
  Options: Setup / System

- **APIC Mode**
  Options: Enabled / Disabled

- **MPS Version Control For OS**
  Options: 1.1 / 1.4

- **OS Select For DRAM > 64MB**
  Options: Non-OS2 / OS2

- **HDD S.M.A.R.T. Capability**
  Options: Enabled / Disabled

- **Full Screen LOGO Show**
  Options: Enabled / Disabled

4.4.1 CPU Feature

```
                    Phoenix – AwardBIOS CMOS Setup Utility
                                CPU Feature
   Delay Prior to Thermal         TM disable          Item Help
   C1E Function                  [Auto]
   Execute Disable Bit           [Enabled]
   Virtualization Technology     [Enabled]

↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **Delay Prior to Thermal**
  Options: none

- **C1E Function**
  Options: Auto / Disabled

- **Execute Disable Bit**
  Options: Enabled / Disabled

- **Virtualization Technology**
  Options: Enabled / Disabled

4.4.2 Hard Disk Boot Priority

```
Phoenix – AwardBIOS CMOS Setup Utility
Hard Disk Boot Priority
1. Bootable Add-in Cards                    Item Help

↑↓→←:Move PU/PD/+/-:Change Priority F10:Save ESC:Exit
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

ü **[list of available devices]**

Options: this dialog allows you to set the order in which the available bootable devices shall be accessed for an attempt to boot.

ü **Attention!**

in this sub menu the buttons <Page Up>, <Page Down>, <+> and <-> have a different function than in the rest of the setup: They serve to move the items of the list up or down.

4.5 Advanced Chipset Features

```
                    Phoenix – AwardBIOS CMOS Setup Utility
                          Advanced Chipset Features
  DRAM Timing Selectable        [By SPD]                  Item Help
x CAS Latency Time               Auto
x DRAM RAS# to CAS# Delay        Auto
x DRAM RAS# Precharge            Auto
x Precharge delay (tRAS)         Auto
x System Memory Frequency        Auto
  SLP_S4# Assertion Widtch      [4 to 5 Sec.]
  System BIOS Cacheable         [Enabled]
  Video BIOS Cacheable          [Disabled]
  Memory Hole At 15M-16M        [Disabled]
► PCI Express Root Port Func    [Press Enter]

  ** VGA Setting **
  PEG/Onchip VGA Control        [Auto]
  On-Chip Frame Buffer Size     [ 8MB]
  DVMT Mode                     [DVMT]
  DVMT/FIXED Memory Size        [ 128MB]
  Boot Display                  [Auto]
  Panel Scaling                 [Auto]
  Panel Number                  [ 640x480]
  ↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
  F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **DRAM Timing Selectable**
  Options: By SPD / Manual

- **CAS Latency Time**
  Options: 5 / 4 / 3 / 6 / Auto

- **DRAM RAS# to CAS# Delay**
  Options: 2 / 3 / 4 / 5 / 6 / Auto

- **DRAM RAS# Precharge**
  Options: 2 / 3 / 4 / 5 / 6 / Auto

- **Precharge delay (tRAS)**
  Options: Auto / 4 / 5 / 6 / 7 / 8 / 10 / 11 / 12 / 13 / 14 / 15

- **System Memory Frequency**
  Options: Auto / 533MHz / 667MHz

- **SLP_S4# Assertion Width**
  Options: 4 to 5 Sec. / 3 to 4 Sec. / 2 to 3 Sec. / 1 to 2 Sec.

- **System BIOS Cacheable**
  Options: Enabled / Disabled

- **Video BIOS Cacheable**
  Options: Enabled / Disabled

- **Memory Hole At 15M-16M**
  Options: Enabled / Disabled

- **PCI Express Root Port Func**
  Sub menu: see "PCI Express Root Port Function" (p. 52)

- **PEG/Onchip VGA Control**
  Options: Onchip VGA / PEG Port / Auto

- **On-Chip Frame Buffer Size**
  Options: 1MB / 8MB

- **DVMT Mode**
  Options: FIXED / DVMT / BOTH

- **DVMT/FIXED Memory Size**
  Options: 64MB / 128MB / 224MB

- **Boot Display**
  Options: VBIOS Default / LFP / EFP / EFP2

- **Panel Scaling**
  Options: Auto / On / Off

- **Panel Number**
  Options: 640x480 / 800x600 / 1024x768 / 1280x1024 / 1400x1050 / 1600x1200 / 1280x768 / 1680x1050 / 1920x1200 / 1280x800 / 1440x900

4.5.1 PCI Express Root Port Function

```
                Phoenix – AwardBIOS CMOS Setup Utility
                      PCI Express Root Port Func
  PCI Express Port 1            [Auto]                    Item Help
  PCI Express Port 2            [Auto]
  PCI Express Port 3            [Auto]
  PCI Express Port 4            [Auto]
  PCI-E Compliancy Mode         [v1.0a]

  ↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
  F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **PCI Express Port 1**
  Options: Auto / Enabled / Disabled

- **PCI Express Port 2**
  Options: Auto / Enabled / Disabled

- **PCI Express Port 3**
  Options: Auto / Enabled / Disabled

- **PCI Express Port 4**
  Options: Auto / Enabled / Disabled

- **PCI-E Compliancy Mode**
  Options: v1.0a / v1.0

4.6 Integrated Peripherals

```
                Phoenix – AwardBIOS CMOS Setup Utility
                        Integrated Peripherals
 ► OnChip IDE Device              [Press Enter]      Item Help
 ► Onboard Device                 [Press Enter]
 ► SuperIO Device                 [Press Enter]

↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **OnChip IDE Device**
  Sub menu: see "OnChip IDE Devices" (p. 54)

- **Onboard Device**
  Sub menu: see "Onboard Devices" (p. 55)

- **SuperIO Device**
  Sub menu: see "SuperIO Devices" (p. 56)

4.6.1 OnChip IDE Devices

```
                Phoenix – AwardBIOS CMOS Setup Utility
                           OnChip IDE Device
   IDE HDD Block Mode            [Enabled]                Item Help
   IDE DMA transfer access       [Enabled]
   On-Chip Primary   PCI IDE     [Enabled]
   IDE Primary Master PIO        [Auto]
   IDE Primary Slave  PIO        [Auto]
   IDE Primary Master UDMA       [Auto]
   IDE Primary Slave  UDMA       [Auto]

*** On-Chip Serial ATA Setting   ***
   SATA Mode                     [IDE]
   On-Chip Serial ATA            [Disabled]
   SATA PORT Speed Settings      [Disabled]
   PATA IDE Mode                 [Secondary]
   SATA Port                     P0,P2 is Primary

  ↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
  F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **IDE HDD Block Mode**
  Options: Enabled / Disabled

- **IDE DMA transfer access**
  Options: Enabled / Disabled

- **On-Chip Primary PCI IDE**
  Options: Enabled / Disabled

- **IDE Primary Master PIO**
  Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

- **IDE Primary Slave PIO**
  Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

- **IDE Primary Master UDMA**
  Options: Disabled / Auto

- **IDE Primary Slave UDMA**
  Options: Disabled / Auto

- **SATA Mode**
  Options: IDE / RAID / AHCI

- **On-Chip Serial ATA**
  Options: Disabled / Auto / Combined Mode / Enhanced Mode / SATA Only

- **SATA PORT Speed Settings**
  Options: Disabled / Force GEN I / Force GEN II

- **PATA IDE Mode**
  Options: none

- **SATA Port**
  Options: none

4.6.2 Onboard Devices

```
                    Phoenix – AwardBIOS CMOS Setup Utility
                                Onboard Device
   USB Controller                [Enabled]          Item Help
   USB 2.0 Controller            [Enabled]
   USB Keyboard Support          [Disabled]
   Azalia/AC97 Audio             [Auto]
   Touch                         [Enabled]

↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **USB Controller**
  Options: Enabled / Disabled

- **USB 2.0 Controller**
  Options: Enabled / Disabled

- **USB Keyboard Support**
  Options: Enabled / Disabled

- **Azalia/AC97 Audio Select**
  Options: Auto / AC97 Audio only / All Disabled

- **Touch**
  Options: Enabled / Disabled

4.6.3 SuperIO Devices

```
                    Phoenix – AwardBIOS CMOS Setup Utility
                                SuperIO Device
  Onboard FDC Controller        [Enabled]                  Item Help
  Onboard Serial Port 1         [3F8/IRQ4]
  Onboard Serial Port 2         [2F8/IRQ3]
  UART Mode Select              [Normal]
x RxD , TxD Active              Hi,Lo
x IR Transmission Delay         Enabled
x UR2 Duplex Mode               Half
x Use IR Pins                   RxD2,TxD2
  Onboard Parallel Port         [378/IRQ7]
  Parallel Port Mode            [Normal]
x EPP Mode Select                EPP1.9
x ECP Mode Use DMA               3
  Onboard Serial Port 3         [3E8/IRQ11]
  Onboard Serial Port 4         [2E8/IRQ10]

  ↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
  F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **Onboard FDC Controller**
  Options: Enabled / Disabled

- **Onboard Serial Port 1**
  Options: Disabled / 3F8/IRQ4 / 2F8/IRQ3 / 3E8/IRQ4 / 2E8/IRQ3 / Auto

- **Onboard Serial Port 2**
  Options: Disabled / 3F8/IRQ4 / 2F8/IRQ3 / 3E8/IRQ4 / 2E8/IRQ3 / Auto

- **UART Mode Select**
  Options: IrDA / ASKIR / Normal

- **RxD , TxD Active**
  Options: Hi,Hi / Hi,Lo / Lo,Hi / Lo,Lo

- **IR Transmission Delay**
  Options: Enabled / Disabled

- **UR2 Duplex Mode**
  Options: Full / Half

- **Use IR Pins**
  Options: RxD2,TxD2 / IR-Rx2Tx2

- **Onboard Parallel Port**
  Options: Disabled / 378/IRQ7 / 278/IRQ5 / 3BC/IRQ7

- **Parallel Port Mode**
  Options: SPP / EPP / ECP / ECP+EPP / Normal

- **EPP Mode Select**
  Options: EPP1.9 / EPP1.7

- **ECP Mode Use DMA**
  Options: 1 / 3

- **Onboard Serial Port 3**
  Options: Disabled / 3F8/IRQ11 / 2F8/IRQ11 / 3E8/IRQ11 / 2E8/IRQ11

- **Onboard Serial Port 4**
  Options: Disabled / 3F8/IRQ10 / 2F8/IRQ10 / 3E8/IRQ10 / 2E8/IRQ10

4.7 Power Management Setup

```
                Phoenix – AwardBIOS CMOS Setup Utility
                        Power Management Setup
  ACPI Function                  [Enabled]                  Item Help
  ACPI Suspend Type              [S1(POS)]
  Run VGABIOS if S3 Resume        Yes
  Power Management               [User Define]
  Video Off Method               [DPMS]
  Video Off in Suspend           [Yes]
  Suspend Type                   [Stop Grant]
  Modem Use IRQ                  [3]
  Suspend Mode                   [Disabled]
  HDD Power Down                 [Disabled]
  Soft-Off by PWR-BTTN           [Instant-Off]
  PWRON After PWR-Fail           [On]
  Wake-Up by PCI card            [Disabled]
  Power On by Ring               [Disabled]
x USB KB Wake-Up From S3          Disabled
  Resume by Alarm                [Disabled]
x  Date(of Month) Alarm            0
x  Time(hh:mm:ss)                  0 : 0 : 0

 ↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **ACPI function**
  Options: Enabled / Disabled

- **ACPI Suspend Type**
  Options: S1(POS) / S3(STR) / S1&S3

- **Run VGABIOS if S3 Resume**
  Options: Auto / Yes / No

- **Power Management**
  Options: User Define / Min Saving / Max Saving

- **Video Off Method**
  Options: Blank Screen / V/H SYNC+Blank / DPMS

- **Video Off In Suspend**
  Options: No / Yes

- **Suspend Type**
  Options: Stop Grant / PwrOn Suspend

- **MODEM Use IRQ**
  Options: NA / 3 / 4 / 5 / 7 / 9 / 10 / 11

- **Suspend Mode**
  Options: Disabled / 1 Min / 2 Min / 4 Min / 8 Min / 12Min / 20 Min / 30 Min / 40 Min / 1 Hour

- **HDD Power Down**
  Options: Disabled / 1 Min ... 15 Min

- **Soft-Off by PWR-BTTN**
  Options: Instant-Off / Delay 4 Sec

- **PWRON After PWR-Fail**
  Options: Former Sts / On / Off

- **Wake Up by PCI Card**
  Options: Enabled / Disabled

- **Power-On by Ring**
  Options: Enabled / Disabled

- **USB KB Wake Up From S3**
  Options: Enabled / Disabled

- **Resume by Alarm**
  Options: Enabled / Disabled

- **Date(of Month) Alarm**
  Options: 1 / ... / 31

- **Time (hh:mm:ss) Alarm**
  Options: insert [hh], [mm] and [ss]

- **Primary IDE 0**
  Options: Enabled / Disabled

- **Primary IDE 1**
  Options: Enabled / Disabled

- **Secondary IDE 0**
  Options: Enabled / Disabled

- **Secondary IDE 1**
  Options: Enabled / Disabled

- **FDD,COM,LPT Port**
  Options: Enabled / Disabled

- **PCI PIRQ[A-D]#**
  Options: Enabled / Disabled

- **HPET Support**
  Options: Enabled / Disabled

- **HPET Mode**
  Options: 32-bit mode / 64-bit mode

4.8 PnP/PCI Configuration

```
                Phoenix – AwardBIOS CMOS Setup Utility
                        PNP/PCI Configurations
  Init Display First            [PCI Slot]          Item Help
  Reset Configuration Data      [Disabled]

  Resources Controlled By       [Manual]
► IRQ Resources                 [Press Enter]

  PCI/VGA Palette Snoop         [Disabled]

  ** PCI Express relative       items **
  Maximum Payload Size          [128]

  ↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
  F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **Init Display First**
  Options: PCI Slot / Onboard

- **Reset Configuration Data**
  Options: Enabled / Disabled

- **Resources Controlled By**
  Options: Auto(ESCD) / Manual

- **IRQ Resources**
  Sub menu: see "IRQ Resources" (p. 61)

- **PCI/VGA Palette Snoop**
  Options: Enabled / Disabled

- **Maximum Payload Size**
  Options: 128 / 256 / 512 / 1024 / 2048 / 4096
  (Note: The Intel® 945GM and SCH US15W chipsets only support an MPL of 128B)

4.8.1 IRQ Resources

```
                    Phoenix – AwardBIOS CMOS Setup Utility
                                IRQ Resources
   IRQ-3  assigned to            [PCI Device]          Item Help
   IRQ-4  assigned to            [PCI Device]
   IRQ-5  assigned to            [PCI Device]
   IRQ-7  assigned to            [PCI Device]
   IRQ-9  assigned to            [PCI Device]
   IRQ-10 assigned to            [PCI Device]
   IRQ-11 assigned to            [PCI Device]
   IRQ-12 assigned to            [PCI Device]
   IRQ-14 assigned to            [PCI Device]
   IRQ-15 assigned to            [PCI Device]

  ↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **IRQ-3 assigned to**
  Options: PCI Device / Reserved

- **IRQ-4 assigned to**
  Options: PCI Device / Reserved

- **IRQ-5 assigned to**
  Options: PCI Device / Reserved

- **IRQ-7 assigned to**
  Options: PCI Device / Reserved

- **IRQ-9 assigned to**
  Options: PCI Device / Reserved

- **IRQ-10 assigned to**
  Options: PCI Device / Reserved

- **IRQ-11 assigned to**
  Options: PCI Device / Reserved

- **IRQ-12 assigned to**
  Options: PCI Device / Reserved

- **IRQ-14 assigned to**
  Options: PCI Device / Reserved

- **IRQ-15 assigned to**
  Options: PCI Device / Reserved

4.9 PC Health Status

```
                    Phoenix – AwardBIOS CMOS Setup Utility
                              PC Health Status
   On Die Digital Temp.          41°C/105°F                Item Help
   Temp. Board                   38°C
   Temp. DDR                     43°C
   CPU Core                      1.20V
   GMCH Core                     1.05V
   CPU VTT                       1.02V
   Memory 1.8 V                  1.84V
   +3.3 V                        3.29V
   +5.0 V                        4.99V
   +1.5 V                        1.50V
   -5 V   / -12 V               -4.92V  -11.64V
   12 V   / DDR VTT             12.31V    0.91V
   S3.3 V / S1.2 V               3.31V    1.20V
   VBatt                         3.28V
   Fan1 / 2 Speed               4166 RPM     0 RPM

   Board Revision                1

   ↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
  F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **On Die Digital Temp.**
  Options: none

- **Temp. Board**
  Options: none

- **Temp. DDR**
  Options: none

- **CPU Core**
  Options: none

- **GMCH Core**
  Options: none

- **CPU VTT**
  Options: none

- **Memory 1.8 V**
  Options: none

- **+3.3 V**
  Options: none

- **+5.0 V**
  Options: none

- **+1.5 V**
  Options: none

- **-5 V / -12 V**
  Options: none

- **12 V / DDR VTT**
  Options: none

- **S3.3 V / S1.2 V**
  Options: none

- **VBatt**
  Options: none

- **Fan1 / 2 Speed**
  Options: none

- **Board Revision**
  Options: none

4.10 Frequency/Voltage Control

```
                    Phoenix – AwardBIOS CMOS Setup Utility
                          Frequency / Voltage Control
   Auto Detect PCI Clk            [Enabled]                 Item Help
   Spread Spectrum                [-0.25%]

   ↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
   F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **Auto Detect PCI Clk**
  Options: Enabled / Disabled

- **Spread Spectrum**
  Options: Disabled / -0.25% / -0.5% / -0.75% / -1% / +-0.125% / +-0.25% / +-0.375% / +-0.5%

4.11 Load Fail-Safe Defaults

If this option is chosen, the last working setup is loaded from flash. Working means that the setup setting has already led to a successful boot process.
At the first setting of the BIOS setup, safe values are loaded which lets the board boot. This status is reached again, if the board is reprogrammed with the corresponding flash-program and the required parameters.

4.12 Load Optimized Defaults

This option applies like described under “Remarks for Setup Use” (5.1).
At first start of the BIOS, optimized values are loaded from the setup, which are supposed to make the board boot. This status is achieved again, if the board is reprogrammed using the flash program with the required parameters.

4.13 Set Password

Here you can enter a password to protect the BIOS settings against unauthorized changes. Use this option with care! Forgotten or lost passwords are a frequent problem.

4.14 Save & Exit Setup

Settings are saved and the board is restarted.

4.15 Exit Without Saving

This option leaves the setup without saving any changes.

5 BIOS update

If a BIOS update becomes necessary, the program “AWDFLASH.EXE” of the company Phoenix is used for this. It is important, that the program is started from a DOS environment without a virtual memory manager such as for example “EMM386.EXE”. In case such a memory manager is loaded, the program will stop with an error message.
The system must not be interrupted during the flash process, otherwise the update is stopped and the BIOS is destroyed afterwards.
The program should be started as follows:

```
awdflash [biosfilename] /sn /cc /cd /cp
```

/sn	Do not save the current BIOS
/cc	Clear the CMOS
/cd	Clear the DMI information
/cp	Clear the PnP information

The erasure of CMOS, DMI and PnP is strongly recommended. This ensures, that the new BIOS works correctly and that all chipset registers, which were saved in the setup, are reinitialized through the BIOS.
A complete description of all valid parameters is shown with the parameter “/?”.
In order to make the updating process run automatically, the parameter “/py” must be added. This parameter bypasses all security checks during programming.

CAUTION

Updating the BIOS in an improper way can render the board unusable. Therefore, you should only update the BIOS if you really need the changes/corrections which come with the new BIOS version.

CAUTION

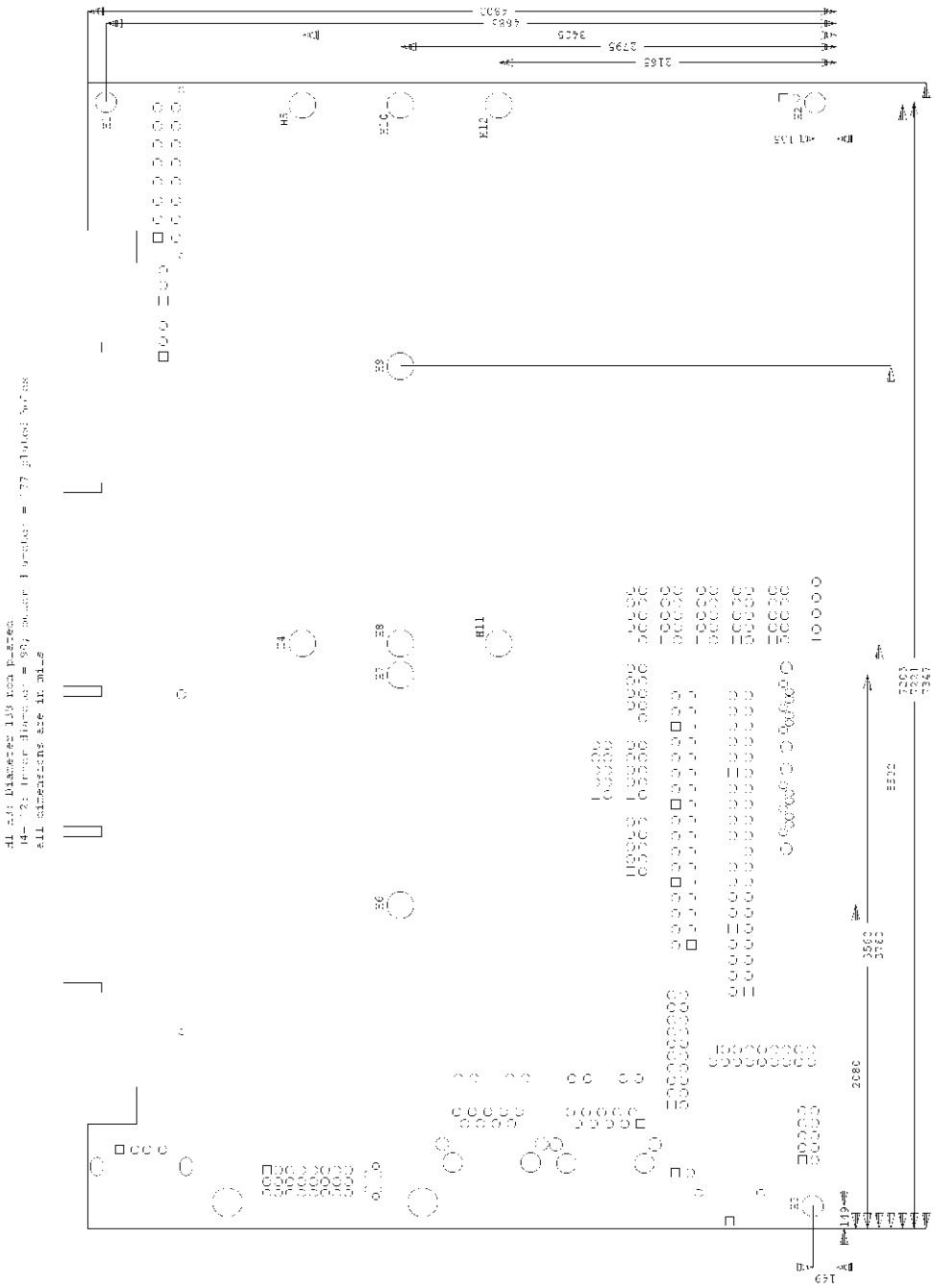
Before you proceed to update the BIOS you need to make absolutely sure that you have the right BIOS file which was issued for the exact board and exact board revision that you wish to update. If you try to update the BIOS using the wrong file the board will not start up again.

6 Mechanical Drawing

6.1 PCB: Mounting Holes

NOTE

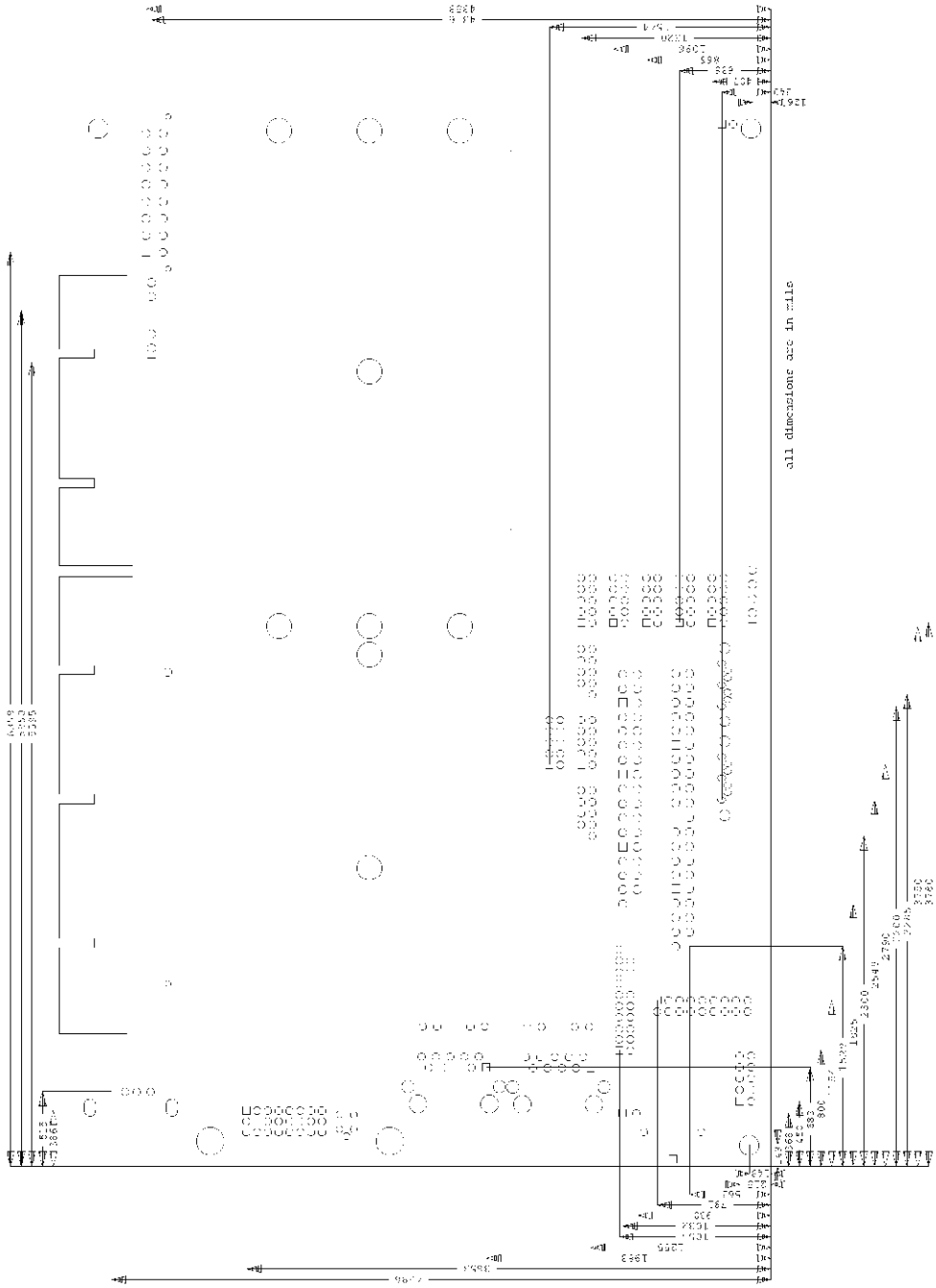
All dimensions are in mil (1 mil = 0.0254 mm)



6.2 PCB: Pin1 Dimensions

NOTE

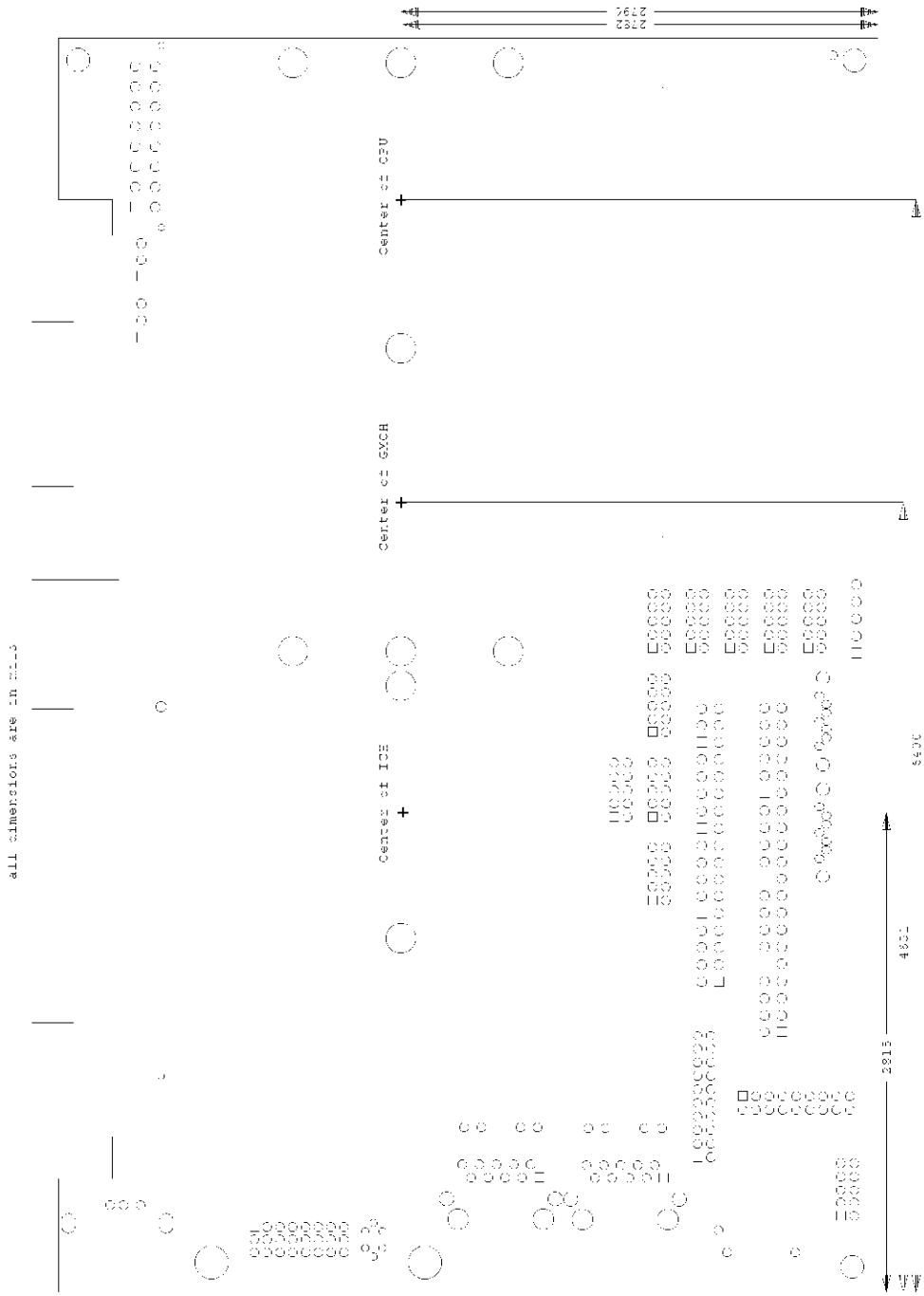
All dimensions are in mil (1 mil = 0.0254 mm)



6.3 PCB: Die Center

NOTE

All dimensions are in mil (1 mil = 0.0254 mm)



7 Technical Data

7.1 Electrical Data

Power Supply:

Board:	+5V, -5V, +12V, -12V (+/-5%)
RTC:	>= 3 Volt

Electric Power Consumption:

Board:	tbd
RTC:	<= 10µA

7.2 Environmental Conditions

Temperature Range:

Operating:	0°C to +60°C (extended temperature on request)
Storage:	-25°C up to +85°C
Shipping:	-25°C up to +85°C, for packaged boards

Temperature Changes:

Operating:	0.5°C per minute, 7.5°C per 30 minutes
Storage:	1.0°C per minute
Shipping:	1.0°C per minute, for packaged boards

Relative Humidity:

Operating:	5% up to 85% (non condensing)
Storage:	5% up to 95% (non condensing)
Shipping:	5% up to 100% (non condensing), for packaged boards

Shock:

Operating:	150m/s^2, 6ms
Storage:	400m/s^2, 6ms
Shipping:	400m/s^2, 6ms, for packaged boards

Vibration:

Operating:	10 up to 58Hz, 0.075mm amplitude
	58 up to 500Hz, 10m/s^2
Storage:	5 up to 9Hz, 3.5mm amplitude
	9 up to 500Hz, 10m/s^2
Shipping:	5 up to 9Hz, 3.5mm amplitude
	9 up to 500Hz, 10m/s^2, for packaged boards

CAUTION

Shock and vibration figures pertain to the motherboard alone and do not include additional components such as heat sinks, memory modules, cables etc.

7.3 Thermal Specifications

The board is specified to operate in an environmental temperature range from 0°C to +60°C (extended temperature on request). Maximum die temperature is 100°C. To keep the processor under this threshold an appropriate cooling solution needs to be applied. This solution has to take typical and maximum power consumption into account. The maximum power consumption may be twice as high and should be used as a basis for the cooling concept. Additional controllers may also affect the cooling concept. The power consumption of such components may be comparable to the consumption of the processor.
The board design includes thermal solution mounting points that will provide the best possible thermal interface between die and solution. Since we take thermal solutions seriously we have several advanced, aggressive cooling solutions in our product portfolio. Please contact your sales representative to order or discuss your thermal solution needs.

CAUTION

The end customer has the responsibility to ensure that the die temperature of the processor does not exceed 100°C. Permanent overheating may destroy the board!
In case the temperature exceeds 100°C the environmental temperature must be reduced. Under certain circumstances sufficient air circulation must be provided.

8 Support and Service

Beckhoff and their partners around the world offer comprehensive support and service, making available fast and competent assistance with all questions related to Beckhoff products and system solutions.

8.1 Beckhoff's Branch Offices and Representatives

Please contact your Beckhoff branch office or representative for local support and service on Beckhoff products.
The addresses of Beckhoff's branch offices and representatives around the world can be found on her internet pages: http://www.beckhoff.com
You will also find further documentation for Beckhoff components there.

8.2 Beckhoff Headquarters

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8.2.1 Beckhoff Support

Support offers you comprehensive technical assistance, helping you not only with the application of individual Beckhoff products, but also with other, wide-ranging services:

- support
- design, programming and commissioning of complex automation systems
- and extensive training programs for Beckhoff system components

hotline: +49(0)5246/963-157
fax: +49(0)5246/963-9157
e-mail: support@beckhoff.com

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- on-site service
- repair service
- spare parts service
- hotline service

hotline: +49(0)5246/963-460
fax: +49(0)5246/963-479
e-mail: service@beckhoff.com

I Annex: Post-Codes

Code	Description
01h	The Xgroup-program code is written in the random access memory from address 1000:0 onwards.
03h	Initialise Variable/Routine "Superio_Early_Init".
05h	1. Cancel display 2. Cancel CMOS error flag
07h	1. Cancel 8042 (keyboard controller) Interface Register 2. Initialising and self testing of 8042 (keyboard controller)
08h	1. Test of special keyboard controllers (Winbond 977 super I/O Chip-series). 2. Enabling of the keyboard-interface register
0Ah	1. Disabling of the PS/2 mouse interface (optional). 2. Auto-detection of the connectors for Keyboard and mouse, optional: swap of PS/2 mouse ports and PS/2 interfaces.
0Eh	Test of the F000h-memory segment (Read/Write ability). In case of an error a signal will come out of the loud speakers.
10h	Auto-detection of the flash-rom-type and loading of the suitable Read/Write program into the run time memory segment F000 (it is required for ESCD-data & the DMI-pool-support).
12h	Interface-test of the CMOS RAM-logic (walking 1's"-algorithm). Setting of the power status of the real-time-clock (RTC), afterwards test of register overflow.
14h	Initialising of the chip-set with default values. They can be modified through a software (MODBIN) by the OEM-customer.
16h	Initialise Variable/Routine "Early_Init_Onboard_Generator".
18h	CPU auto-detection (manufacturer, SMI type (Cyrix or Intel), CPU-class (586 or 686).
1Bh	Initialising if the interrupt pointer table. If nothing else is pretended, the hardware interrupts will point on "SPURIOUS_INT_HDLR and the software interrupts will point on SPURIOUS_soft_HDLR.
1Dh	Initialise Variable/Routine EARLY_PM_INIT.
1Fh	Load the keyboard table (Notebooks)
21h	Initialising of the hardware power management (HPM) (Notebooks)
23h	1. Test the validity of the RTC-values (Example: "5Ah" is an invalid value for an RTC-minute). 2. Load the CMOS-values into the BIOS Stack. Default-values are loaded if CMOS-checksum errors occur. 3. Preparing of the BIOS 'resource map' for the PCI & plug and play configuration. If ESCD is valid, take into consideration the ESCD's legacy information. 4. Initialise the onboard clock generator. Clock circuit at non-used PCI- and DIMM slots. 5. First initialising of PCI-devices: assign PCI-bus numbers - alot memory- & I/O resources - search for functional VGA-controllers and VGA-BIOS and copy the latter into memory segment C000:0 (Video ROM Shadow).
27h	Initialise cache memory for INT 09
29h	1. Program the CPU (internal MTRR at P6 and PII) for the first memory address range (0-640K). 2. Initialising of the APIC at CPUs of the Pentium-class. 3. Program the chip-set according to the settings of the CMOS-set-up (Example: Onboard IDE-controller). 4. Measuring of the CPU clock speed. 5. Initialise the video BIOS.
2Dh	1. Initialise the "Multi-Language"-function of the BIOS 2. Soft copy, e.g. Award-Logo, CPU-type and CPU clock speed…
33h	Keyboard-reset (except super I/O chips of the Winbond 977 series)
3Ch	Test the 8254 (timer device)
3Eh	Test the interrupt Mask bits of IRQ-channel 1 of the interrupt controller 8259.
40h	Test the interrupt Mask bits of IRQ-channel 2 of the interrupt controller 8259
43h	Testing the function of the interrupt controller (8259).
47h	Initialise EISA slot (if existent).

Code	Description
49h	1. Determination of the entire memory size by revising the last 32-Bit double word of each 64k memory segment. 2. Program “write allocation” at AMD K5-CPUs.
4Eh	1. Program MTRR at M1 CPUs 2. Initialise level 2-cache at CPUs of the class P6 and set the “cacheable range” of the random access memory. 3. Initialise APIC at CPUs of the class P6. 4. Only for multiprocessor systems (MP platform): Setting of the “cacheable range” on the respective smallest value (for the case of non-identical values).
50h	Initialise USB interface
52h	Testing of the entire random access memory and deleting of the extended memory (put on “0”)
55h	Only for multi processor systems (MP platform): Indicate the number of CPUs.
57h	1. Indicate the plug and play logo 2. First ISA plug and play initialising – CSN-assignment for each identified ISA plug and play device.
59h	Initialise TrendMicro anti virus program code.
5Bh	(Optional:) Indication of the possibility to start AWDFLASH.EXE (Flash ROM programming) from the hard disk.
5Dh	1. Initialise Variable/Routine Init_Onboard_Super_IO. 2. Initialise Variable/Routine Init_Onbaord_AUDIO.
60h	Release for starting the CMOS set-up (this means that before this step of POST, users are not able to access the BIOS set-up).
65h	Initialising of the PS/2 mouse.
67h	Information concerning the size of random access memory for function call (INT 15h with AX-Reg. = E820h).
69h	Enable level 2 cache
6Bh	Programming of the chip set register according to the BIOS set-up and auto-detection table.
6Dh	1. Assignment of resources for all ISA plug and play devices. 2. Assignment of the port address for onboard COM-ports (only if an automatic junction has been defined in the setup).
6Fh	1. Initialising of the floppy controller 2. Programming of all relevant registers and variables (floppy and floppy controller).
73h	Optional feature: Call of AWDFLASH.EXE if: - the AWDFLASH program was found on a disk in the floppy drive. - the shortcut ALT+F2 was pressed.
75h	Detection and installation of the IDE drives: HDD, LS120, ZIP, CDROM…
77h	Detection of parallel and serial ports.
7Ah	Co-processor is detected and enabled.
7Fh	1. Switch over to the text mode, the logo output is supported. - Indication of possibly emerged errors. Waiting for keyboard entry. - No errors emerged, respective F1 key was pressed (continue): Deleting of the EPA- or own logo.
82h	1. Call the pointer to the “chip set power management”. 2. Load the text font of the EPA-logo (not if a complete picture is displayed) 3. If a password is set, it is asked here.
83h	Saving of the data in the stack, back to CMOS.
84h	Initialising of ISA plug and play boot drives (also Boot-ROMs)
85h	1. Final initialising of the USB-host. 2. At network PCs (Boot-ROM): Construction of a SYSID structure table 3. Backspace the scope presentation into the text mode 4. Initialise the ACPI table (top of memory). 5. Initialise and link ROMs on ISA cards 6. Assignment of PCI-IRQs 7. Initialising of the advanced power management (APM) 8. Set back the IRQ-register.

Code	Description
93h	Reading in of the hard disk boot sector for the inspection through the internal anti virus program (trend anti virus code)
94h	1. Enabling of level 2 cache 2. Setting of the clock speed during the boot process 3. Final initialising of the chip set. 4. Final initialising of the power management. 5. Erase the onscreen and display the overview table (rectangular box). 6. Program “write allocation” at K6 CPUs (AMD) 7. Program “write combining” at P6 CPUs (INTEL)
95h	1. Program the changeover of summer-and winter-time 2. Update settings of keyboard-LED and keyboard repeat rates
96h	1. Multi processor system: generate MP-table 2. Generate and update ESCD-table 3. Correct century settings in the CMOS (20xx or 19xx) 4. Synchronise the DOS-system timer with CMOS-time 5. Generate an MSIRQ-Routing table..
C0h	Chip set initialising: - Cut off shadow RAM - Cut off L2 cache (apron 7 or older) - Initialise chip set register
C1h	Memory detection: Auto detection of DRAM size, type and error correction (ECC or none) Auto detection of L2 cache size (apron 7 or older)
C3h	Unpacking of the packed BIOS program codes into the random access memory.
C5h	Copying of the BIOS program code into the shadow RAM (segments E000 & F000) via chipset hook.
CFh	Testing of the CMOS read/write functionality
FFh	Boot trial over boot-loader-routine (software-interrupt INT 19h)

II Annex: Resources

A IO Range

The used resources depend on setup settings.
The given values are ranges, witch are fixed by AT compatibility. Other IO ranges are used, which are dynamically adjusted by Plug & Play BIOS while booting.

Address	Function
0-FF	Reserved IO area of the board
170-17F	IDE2
1F0-1F7	IDE1
278-27F	LPT2
2E8-2EF	COM4
2F8-2FF	COM2
370-377	FDC2
378-37F	LPT1
3BC-3BF	LPT3
3E8-3EF	COM3
3F0-3F7	FDC1
3F8-3FF	COM1

B Memory Range

The used resources depend on setup settings.
If the USB boot function or legacy support is enabled, the BIOS uses 16KByte RAM in the range from A0000-FFFFF. If the entire range is clogged through option ROMs, these functions do not work any more.

Address	Function
A0000-BFFFF	VGA-RAM
C0000-CFFFF	VGA-Bios
E0000-EFFFF	System-BIOS while booting
F0000-FFFFF	System-BIOS

C Interrupt

The used resources depend on setup settings.
The listed interrupts and their use are given through AT compatibility.
If interrupts must exclusively be available on the ISA side, they have to be reserved through the BIOS setup. The exclusivity is not given and not possible on the PCI side.

Address	Function
IRQ0	Timer
IRQ1	PS/2 Keyboard
IRQ2 (9)	(COM3)
IRQ3	COM1
IRQ4	COM2
IRQ5	(COM4)
IRQ6	FDC
IRQ7	LPT1
IRQ8	RTC
IRQ9	
IRQ10	
IRQ11	

Address	Function
IRQ12	PS/2 Mouse
IRQ13	FPU
IRQ14	IDE Primary
IRQ15	(IDE Secondary)

D PCI Devices

All listed PCI devices exist on the board. Some PCI devices or functions of devices may be disabled in the BIOS setup. Once a device is disabled other devices may get PCI bus numbers different from the ones listed in the table.

AD	INTA	REQ	PCI	Dev.	Fkt.	Controller / Slot
16	-	-	0	0	0	Host Bridge (GMCH) ID27AC
18	A	-	0	2	0	VGA Graphics (GMCH) ID27AE
12	(A)	-	0	28	0	PCI Express Port 1 (ICH)
12	(B)	-	0	28	1	PCI Express Port 2 (ICH)
12	(C)	-	0	28	2	PCI Express Port 3 (ICH)
12	(D)	-	0	28	3	PCI Express Port 4 (ICH)
12	(A)	-	0	28	4	PCI Express Port 5 (ICH)
12	(B)	-	0	28	5	PCI Express Port 6 (ICH)
13	(A)	-	0	29	0	USB UHCI Controller #1 (ICH) ID27C8
13	(B)	-	0	29	1	USB UHCI Controller #2 (ICH) ID27C9
13	(C)	-	0	29	2	USB UHCI Controller #3 (ICH) ID27CA
13	(D)	-	0	29	3	USB UHCI Controller #4 (ICH) ID27CB
13	(A)	-	0	29	7	USB 2.0 EHCI Controller (ICH) ID27CC
14	-	-	0	30	0	PCI-to-PCI Bridge (ICH) ID244E
14	(A)	-	0	30	2	AC ’97 Audio Controller (ICH) ID27DE
14	(B)	-	0	30	3	AC ’97 Modem Controller (ICH)
15	-	-	0	31	0	LPC Controller (ICH) ID27B8
15	(A)	-	0	31	1	IDE Controller (ICH) ID27DF
15	(B)	-	0	31	2	SATA Controller (ICH)
15	(B)	-	0	31	3	SMBus Controller (ICH) ID27DA
19	A	0?	m	3		External Slot 1 (PISA backplane)
20	D?	1?	m	4		External Slot 2 (PISA backplane)
21	C?	2?	m	5		External Slot 3 (PISA backplane)
22	B?	3?	m	6		External Slot 4 (PISA backplane)
23	?	4	m	7		External Slot mPCI
24	(E)	-	n	8	0	LAN Intel 82562GZ (ICH) ID27DC

E SMB Devices

Address	Function
10-11	Standard slave address
60-61	Reserviert by BIOS
88-89	BIOS defined slave address
A0-A1	DIMM 1
A2-A3	DIMM 2
A4-AF	Reserved by BIOS
D2-D3	IDTCV111PAG
D4-D5	ICS9P952