BM2C/2D SCAT
USER'S MANUAL

63-52036-020

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User's Guide

BM-2C/2D SCAT **USER'S MANUAL**

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BM2C/2D SCAT USER'S MANUAL

Interference

If this equipment does cause interface to radio or TV reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of following measures:

* Re-orient the position of the receiving antenna.
* Relocate the equipment with reset to the receiver.
* Move the equipment away from the receiver.
* Plug the equipment into a different outlet so that the equipment and receive are on different branch circuit.
* Make sure that all add-on cards mounting screws, connector screws and ground are no cards installed.
* Verify that the covers for the card slot are securely in position, if there are no cards installed.
* If peripheral that are not offered by the manufacturer are used with this equipment, it is suggested that you use shielded ground cables with in-line filters.

Safety Warning

The manufacturer recommends which that product be used with a ground plug to ensure user safety, it should be used in conjunction with properly grounded power receptable to avoid possible electric shock.

Before operating this device, please verify the correct voltage setting for your system. The manufacturer of this equipment is not responsible for any demage incurred in the operation of this system if the correct operational voltage detting is not selected prior to operation.

CHAPTER 1

GENERATION INFORMATION

1-1 Introduction

The SCAT system board is a highly integrated system board computer based on INTEL 80286 CPU, Headland SCAT HT12 and other VLSI technology.

The board uses the PC-BUS interface standard with wide product support while is decouples the 80286 from PC-BUS to take advantage of it's higher performance.

The SCAT system can boost performace in application originally designed for PC compatible computer. With this compatiblity, performance can be improved without requiring major hardware or software change.

1-2 Specification

* 80286 12 MHz zero wait or 16 MHz one wait state system design.
* 80287 math coprocessor socket support.
* Leagal BIOS for 16-bit EPROM from AMI, Award, Phoenix, Quadtel.
* Supports LIM EMS-4.0 32 register.
* Hot CPU reset and fast A20 gate.
* Supports base memory on-board (SIMM) up to 4MB.
* Independent AT Bus clock and processor clock for add-on card compatibility.
* Internal real time clock and processor clock for add-on card compatibility.
* External real time clock controller with battery back-up.
* Shadow RAM supported for system and video BIOS.
* Selected memory wait state.
* Five 16-bit slot and two 8-bit slot design.
* Turbo and normal speed selection.

* On-board rechargeable back-up battery and/or battery for external battery pack.
* Half size two layer main board design.

1-3 Key Features

The SCAT is a VLSI device that incorporate most of the motherboard logic required to build a low cost, highly-integrated IBM PC AT compatible computer. The following list are most important features:

* 80286 single chip AT support CPU speeds to 16MHz 0 or 1 wait state.
* A 146818 real time clock with 114 bytes of CMOS RAM.
* Two 8237 compatible DMA controllers.
* Two 8259 compatible interrupt controllers.
* An 8254 compatible programmable interval timer.
* An 8255 compatible programmable peripheral interface.
* An 82288 compatible Bus controller.
* An 82284 compatible clock generation and ready interface.
* A DRAM controller that supports up to 4MB of DRAM.
* A memory controller that provides shadow RAM and either 16-bit ROM.
* A DRAM refresh controller.
* Independent clocking source for the AT Bus.
* 32 EMS page register. (LIM EMS 4.0 compatible)
* Interface logic for an 80287 numeric coprocessor.
* Interface logic for an 8042 keyboard controller.
* Hot reset, fast A20 gate.
* HCMOS design for high speed and low power consumption.

HT11/12 PERFORMANCE

	HT11/12 16MHz True "0" Wait State	NEAT "0" ws/Page/Int
Landmark	20.5MHz	20.5MHz
QA Plus	4138 Drystones 8607 Video Speed	3034 Drystones 7889 Video Speed
MIPS by C&T	2.2 MIPS	1.9 MIPS
Power Meter	3.17 MIPS	2.56 MIPS

Both with: 286 CPU/387-10 NPU/1024i 16-Bit Video Card

1-4 Power Requirement

Voltage: A. +5V, +/− 5%
B. +12V, +/− 5%
C. −12V, +/− 5%
D. −5V, +/− 5%

System power consumption

150 watt to 200 watt depended on system configuration.

1-5 Mechanical Specification

Size: Length: 228mm
Width: 218mm

Mounting Holes: Fit any PC/XT, AT or compatible case.

1-6 Operation Environment

Operation Temperature: 0 — 45 degree C or 32 — 113 degree F.

Storage Temperature: −20 — 50 degree C or −4 — 122 degree F.

Humidity: Over 85%
ESD: Over 12KV

CHAPTER 2

KNOWING YOUR SCAT MAIN BOARD SYSTEM

2-1 SCAT System Jumper Define

The SCAT system has the following jumpers and connectors:

JP1 : Reset switch connector.
JP2 : Turbo LED.
JP3 : Turbo/normal speed connector.
JP5 : Speaker connector.
JP6 : Keylock connector.
JP7 : Coprocessor clock selection.
JP9 : ROM selection.
JP10: Display type selection.
JP11: External battery connector.
PS1/PS2: Power connector.
J13: Keyboard connector.

Jumper setting and connector define

JP1: Reset switch connector
On: System reset
Off: Normal operation

JP2: Turbo LED

Pin#	Assignment
1.	LED anode (+)
2.	LED cathode (−)

JP3: Turbo/normal selection
On: Turbo speed
Off: Normal speed

JP5: Speaker connector

Pin#	Assignment
1.	Speak out
2.	N.C.
3.	Ground
4.	+5V

JP6: Keylock connector

Pin#	Assignment
1.	LED power
2.	N.C.
3.	Ground
4.	Keylock
5.	Ground

JP7: Coprocessor clock selection
1-2 on: Sync mode
2-3 on: Unsync mode

JP9: ROM Selection
1-2 on: 128K
2-3 on: 256K

JP10: Display type selection
1-2 on: Mono
2-3 on: Color

JP11: External battery connector

Pin#	Assignment
1.	+6V battery input
2.	N.C.
3.	N.C.
4.	Ground

PS1/PS2: Power connector

Pin# (PS1)	Assignment
1.	Power good
2.	+5V
3.	+12V
4.	−12V
5.	Ground
6.	Ground
1.	Ground
2.	Ground
3.	−5V
4.	+5V
5.	+5V
6.	+5V

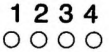
J13: Keyboard connector

Pin#	Assignment
1.	Keyboard clock
2.	Keyboard data
3.	N.C.
4.	Ground
5.	+5V

JP7: NPX CLK optional

: 1-2 on (Sync mode)
: 2-3 on (Unsync mode)

JP5: Speaker conn.



J10: Display selection

1-2: Mono
2-3: Color

JP6: Keylock

1 5

○ ○ ○ ○ ○

JP11: External battery

1 5

○ ○ ○ ○ ○

JP3: Turbo SW

○ ○

JP2: Turbo LED

○ ○

J13: Keyboard connector

JP1: Reset switch

○ ○

PS1/PS2: Power connector

2-2 Setup BIOS (AMI, Quadtel, Phoenix, Award)

Please Refer the Following Description and Figure

CMOS SETUP (C) Copyright 1985-1989, American megatrends Inc.

Date (mn/date/year): Mon, Jan 01 1990
Time (hour/min/sec): 10 : 10 : 10
Floppy drive A : 1.2 MB, 5¼"
Floppy drive B : Not Installed

Hard disk C: type : 2
Hard disk D: type : Not Installed
Primary display : Monochrome
Keyboard : Installed

Scratch RAM option: 1

Month : Jan, Feb, ... Dec
Date : 01, 02, 03, ... 31
Year : 1901, 1902, .. 2099

ESC = Exit, ↓ → ↑ ← Select, PgUp/PgDn

Base memory Size : 640 KB
Ext. memory Size : 0 KB
Numeric Processor : Installed

Cyln	head	Wpcom	Izone	sect	Size
65	4	380	615	17	20MB

Sun	Mon	Tue	Wed	Thu	Fri	Sat
30	1	2	3	4	5	6
7	8	9	10	11	12	13
14	15	16	17	18	19	20
21	22	23	24	25	26	27
28	29	30	31	1	2	3
4	5	6	7	8	9	10

ITEM A. Date (Mn/date/year): use UP, DOWN, LEFT, RIGHT ARROW KEY to move cursor and PgUp/PgDn KEY to increase/decrease DATE, MONTH, YEAR.

ITEM B. Time (hour/min/sec): use ARROW KEY to move cursor and PgUp/PgDn KEY to increase/decrease HOUR, MIN, SEC.

ITEM C. Floppy drive A: use PgUp/PgDn KEY to select Floppy drive A type, included 360KB/5¼", 1.2MB/5¼", 720KB/3½", 1.44MB/3½" and not installed.

ITEM D. Floppy drive B: the same as ITEM C.

ITEM E. Hard disk C: type: use PgUp/PgDn KEY to select Hard disk C: type, included Type 1, Type 2, Type 3 ....., Type 47 and and not installed.

ITEM F. Hard disk D:type: the same as ITEM E.

ITEM G. Primary display: use PgUp/PgDn KEY to select MONITOR type, included Monochrome, Color 40 x 25, VGA or EGA, Color 80 x 25 and not installed.

ITEM H. Keyboard: use PgUp/PgDn KEY to installed or not installed Keyboard.

ITEM I. Scratch RAM option: use PgUp/PgDn KEY to select 1 or 2, 1 for using BIOS stack area at 0030:0000, 2 for reducing base memory size by 1KB when BIOS require use 256 bytes of RAM. 1 is the BIOS default value.

When setup is finished, you should press <ESC> key the reverse area, which is for comment, will appears a message like follow:

Write data into CMOS and exit? (y/n)

if you press "y" then press <ENTER> the configuration you just setup will be saved to CMOS and system will reset.

Keyboard control the following function:

INS key: Press INS key when power on until RAM count beginning, this step will use default value to boot from BIOS and don't care any setup in CMOS RAM. This function act as if discharge CMOS RAM power to clear "WRONG SETUP VALUE" that will cause boot failure from BIOS.

CTRL, ALT, –: Press these three keys simultaneously will switch CPU Speed to low speed.

CTRL, ALT, +: Press these three keys simultaneously will switch CPU Speed to High speed.

2-3 DRAM Configuration

Access DRAM by PAGE MODE. Both DIP RAM and SIMM MODULE RAM can be used.

We offer you a very flexible function to choose your DRAM TYPE and DRAM SIZE on board:

(A) USE 256K SIMM MODULE RAM.

512K: 256K SIMM MODULE RAM ON BANK 0.
1024K: 256K SIMM MODULE RAM ON BANK 0 & BANK 1.

(B) USE 1M SIMM MODULE RAM.

2048K: 1M SIMM MODULE RAM ON BANK 0.
4096K: 1M SIMM MODULE RAM ON BANK 0 & BANK 1.

2-4 On Board EMS User Guide

If you want to use on board EMS function, you must have enough memory size on board. See the following table for details.

DRAM Setting		Total Memory	Base Memory Occupy	BIOS, VGA/EGA Shadow Enable or Not	Allowable Maximun EMS Size	EXT Memory
Bank 0	Bank 1					
256 K	None	512KB	512KB	Disable	None	None
256 K	256 K	1024KB	640KB	Enable	None	None
256 K	256 K	1024KB	640KB	Disable	None	384KB
1 M	None	2048KB	640KB	don't care	None	1024KB
1 M	1 M	4096KB	640KB	don't care	3072KB	None
1 M	1 M	4096KB	640KB	don't care	2816KB	256KB
1 M	1 M	4096KB	640KB	don't care	2560KB	512KB
1 M	1 M	4096KB	640KB	don't care	2048KB	1024KB

Besides the correct setting of the allowable maximun EMS size and enable EMS function on our setup program named HT12.EMS you must install our EMS drive named HT12.EMS to CONFIG.SYS.

The HT12.EMS is compatible with LIM Ver 4.0.

HT12 PARAMETER SPECIFICATION

There are 5 parameters can be specified to make the EMS work properly.

Following is the format of parameter specification:

DEVICE = HT12.EMS [FRAME = aaaa] [EXCLUDE = xxxx-cccc] [INCLUDE = xxxx-cccc] [HANDLES = hhh] [IOADDR = aaa]
Where [ ] is the optional term.

Following are there purposes:

FRAME = aaaa

Specifies the page frame address (the address of the 64K segment through which expanded memory is mapped.) "aaaa" must be either D000 or E000. Specifying FRAME will override the automatic choice of page frame by the driver.

EXCLUDE = xxxx [-cccc]

Specifies an area of memory which should not be under the control of the HT12.EMS driver. "xxxx" and "cccc" specify the address or range of addresses of memory to be excluded and should be in multiples of 16K (i.e. end in 00). EXCLUDED may be used several times on the driver command line to exclude multiple blocks of memory, though at least 64K of memory should remain above 640K (A000). The driver will find all RAM/ROM in the range D000-EFFF, and will adjust for them.

INCLUDE = xxxx [-cccc]

Specifies memory to be included under the control of the HT12.EMS driver. Parameters are similar to EXCLUDE above.

HANDLES = hhh

Specifies the number of handles and names available. "hhh" must be in the range of 16 to 255, with the default being 64.

IOADDR = aaa

Overrides the default base I/O address at which the "SCAT" Chip should be configured. aaa must be either 208 or 218.

2-5 Coprocessor Configuration

The 80286 system board have an empty 40 pins Dip socket (U6) allow you to install a 80287 math coprocessor.

CHAPTER 3

SCAT SYSTEM SOFTWARE CONFIGURATION

3-1 Setup Reference

This chapter provides the information for you to set up the system BIOS and other system configuration.

3-1-1 AMI BIOS Setup

Following BIOS setup are included in AMI BIOS:

AMI BIOS setup table referance

When RAM counting over then press key = "DEL" to into

Exit for boot
Run CMOS setup
Run diagnostic

First step you want selection "Run CMOS setup"
Then into following table:

CMOS SETUP (C) Copyright 1985-1990, American Megatrends Inc.

Date (mn/date/year) : Thu, Jan 04 1990
Time (hour/min/sec) : 13 : 24 : 57
Floppy drive A : Not installed
Floppy drive B : Not installed

Hard disk C: type : 17
Hard disk D: type : Not installed
Primary display : Monochrome
Keyboard : Installed
BIOS shadow option: Disable
Scratch RAM option : 1
EMS size option : 0KB
0 wait state option : Enable
Memory relocation : Enable

Option: –
Enabled : RAM access 0 wait state
Disabled RAM access 1 wait state

ESC = Exit, ← → = Select, PgUp/PgDn = Modify

Base memory size : 512KB
Ext. memory aize : 0KB
Numeric Processor : Not installed

Cyln	head	wpcom	lzone	sect	size
977	5	300	977	17	41MB

Sun	Mon	Tue	Wed	Thu	Fri	Sat
31	1	2	3	4	5	6
7	8	9	10	11	12	13
14	15	16	17	18	19	20
21	22	23	24	25	26	27
28	29	30	31	1	2	3
4	5	6	7	8	9	10

You can move cursor to setup date, time, floppy, harddisk,display, keyboard, BIOS shadow, EMS, wait state, memory.

Second step when your setup is right then write to CMOS and boot your system.

3-1-2 Award Software CMOS Setup

Award Software CMOS Setup

Date (mm/dd/yy) 1/4/90 Time (hh:mm:ss) 14:48:37

Diskette 1 None
Diskette 2 None

		Cyls.	Heads	Sector	Precomp	Landzone
Disk 1	40MB	977	5	17	300	977
Disk 2	****MB	306	4	17	128	306

Video Mono

Base Memory 512
Extended Memory 0 Memory Read/Write 1 Wait State
EMS Memory 0

Error Halt Halt on All Errors
Shadow RAM Disable
Speed Select No Change

↑ ← → ↓ Moves Between Items, Selects Values
F10 Records Changes, F1 Exits, F2 for Color Toggle

Finally You Can Press Key "F5" and "F10" Write to CMOS

3-1-3 Quadtel HT12 BIOS Setup

Extended BIOS Software Copyright 1989, Quadtel Corp.
Setup Park Fixed Disks Format Fixed Disk
↑ ↓ Move Enter Select Esc Exit

```
Extended BIOS Setup — Copyright 1989, 1990 Quadtel Corporation

Current Date: [11/15/1990]                Video System      [EGA/VGA]
Current Time: [09:36:45]

 640K System Memory                       Power Up Speed:   [Fast]
[384K] Extended Memory                    BIOS Shadow:      [System in ROM]
[  0K] EMS Memory                                           [Video in ROM]
   0K Shadow Memory                       Wait States:      [0, All Banks]

Diskette Drive 0: [1.2 MB, 5 1/4]
Diskette Drive 1: [1.44 MB, 3 1/2]

Fixed Disk 0: Type: [   36]  CY: 1024  HD: 8  ST: 17  LZ: 1024  WP: None
Fixed Disk 1: Type: [None]

↑ ↓  Move          F5  Previous Value        F9   Automatic Configuration
F1   Help          F6  Next Value            F10  Save Configuration
Esc  Exit
```

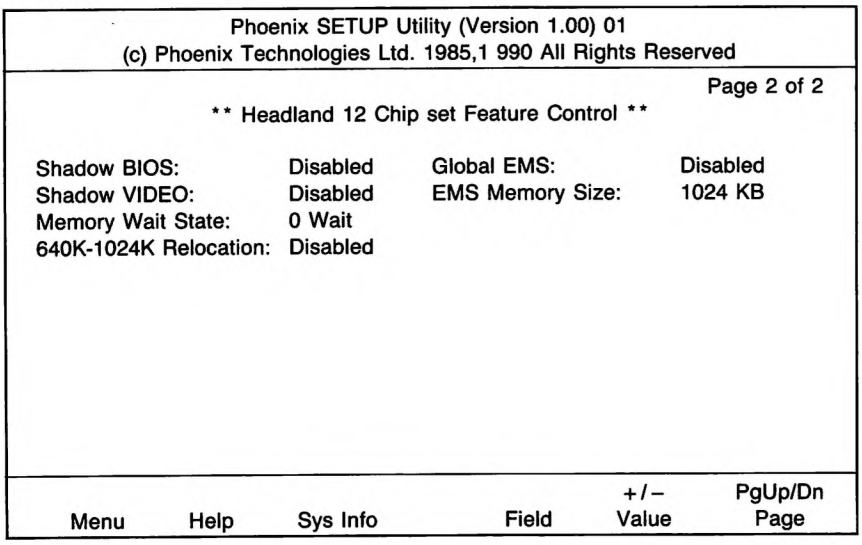
3-1-4 Phoenix HT12 BIOS Setup

Press CTRL + ALT + S to Run Setup

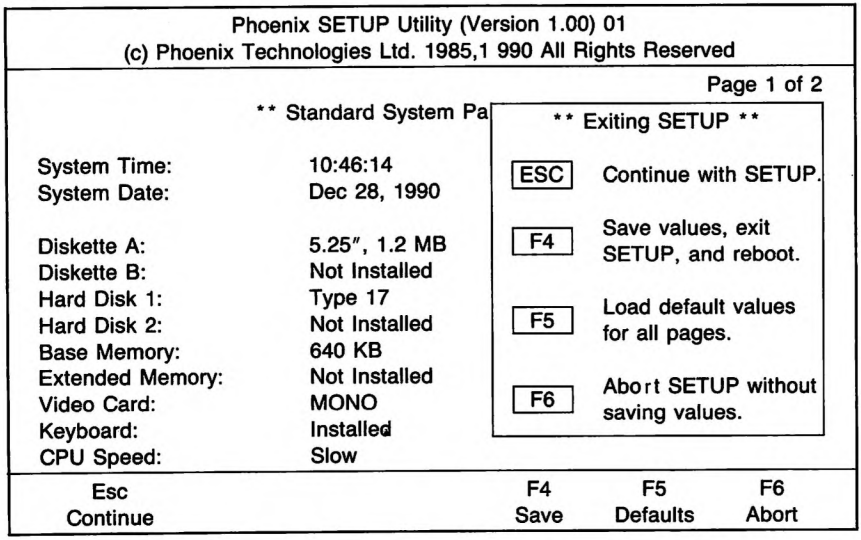
Step-1

```
                Phoenix SETUP Utility (Version 1.00) 01
        (c) Phoenix Technologies Ltd. 1985, 1990 All Rights Reserved

                                                              Page 1 of 2
                      ** Standard System Parameters **

System Time:          10:04:06        NumLock on at boot: YES
System Date:          Dec 28, 1990

Diskette A:           5.25", 1.2 MB
Diskette B:           Not Installed     Cyl  Hd  Pre  LZ   Sec  Size
Hard disk 1:          Type 17           977  5   300  977  17   40
Hard Disk 2:          Not Installed
Base Memory:          640 KB
Extended Memory:      Not Installed
Video Card:           MONO
Keyboard:             Installed
CPU Speed:            Fast

                                                    +/-      PgUp/Dn
  Menu      Help      Sys Info          Field       Value      Page
```

Step-2


Phoenix SETUP Utility (Version 1.00) 01
(c) Phoenix Technologies Ltd. 1985,1 990 All Rights Reserved
Page 2 of 2
** Headland 12 Chip set Feature Control **
Shadow BIOS: Disabled
Shadow VIDEO: Disabled
Memory Wait State: 0 Wait
640K-1024K Relocation: Disabled
Global EMS: Disabled
EMS Memory Size: 1024 KB
Menu
Help
Sys Info
Field
+/-
Value
PgUp/Dn
Page

Step-3


Phoenix SETUP Utility (Version 1.00) 01
(c) Phoenix Technologies Ltd. 1985,1 990 All Rights Reserved
Page 1 of 2
** Standard System Pa
System Time: 10:46:14
System Date: Dec 28, 1990
Diskette A: 5.25", 1.2 MB
Diskette B: Not Installed
Hard Disk 1: Type 17
Hard Disk 2: Not Installed
Base Memory: 640 KB
Extended Memory: Not Installed
Video Card: MONO
Keyboard: Installed
CPU Speed: Slow
** Exiting SETUP **
ESC Continue with SETUP.
F4 Save values, exit SETUP, and reboot.
F5 Load default values for all pages.
F6 Abort SETUP without saving values.
Esc
Continue
F4
Save
F5
Defaults
F6
Abort

3-2 SCAT Register Configuration

Command Delay, Wait States Based on Cycle Type					
Command Delay	Local ROM Read		Local RAM Read		Write
	No		No		No
	At Bus Memory 8 Bit	16 Bit	AT Bus I/O 8 Bit	16 Bit	At Bus Interrupt Acknowledge
Command Delay	Yes	No	Yes	Yes	Yes
Wait States	4	1	4	1	4

I/O Address Map		
Hex Range	**Device Address**	**Part Number**
000 - 0FF	Reserved for System board I/O	
000 - 01F	DMA Controller #1	8237A-5
020 - 03F	Interrupt Controller #1	8259A
040 - 05F	Timer	8254-2
060,062 - 06F	Keyboard Controller	8042
061	Port B Register, PPI	8255
070 - 07F	Real Time Clock, NMI (Non-interruptable Mask) bit	
080 - 08F	DMA Page Register	74LS612
090 - 091	Reserved	
092	Hot Reset and A20Gate	
093 - 09F	Reserved	
0A0 - 0BF	Interrupt Controller #2	8259A
0C0 - 0DF	DMA Controller #2	8237A-5
0F0	Clear Math Coprocessor Busy	
0F1	Reset Math Coprocessor	
0F2 - 0F7	Reserved	
0F8 - 0FF	Math Coprocessor	80287 only
1ED, 1EF	Configuration Registers	

PORT B (8255) PPI Register, Address 61h	
Data Written	
Bit 3 = 1	Disable NMI for IOCHCK(*)
Bit 2 = 1	Disable NMI for Memory Parity error
Bit 1	Speaker data
Bit 0 = 1	Enable Timer (8254) for speaker
Data read back	
Bit 7 = 1	Memory Parity error
Bit 6 = 1	IOCHCK error(*)
Bit 5	Timer 2 (8254), output
Bit 4	REFRESH detect
Bit 3 = 1	NMI disabled, for IOCHCK(*)
Bit 2 = 1	NMI disabled for Memory Parity error(*)
Bit 1	Speaker data
Bit 0 = 1	Timer 2 (8254) for speaker enabled
	NOTE(*) Cleared on RESET

Hot Reset and A20Gate (Port 92H)

The HT12 supports the Hot Reset and A20Gate functions as defined in the PS/2 Technical Reference. Both functions can be used in conjunction with the keyboard controller functions.

Independent Bus Clock

HT12 supports two independent clock sources. It normally runs off the high speed clock (CLKX2), but switches to the asynchronous clock (CLKASN) for off-board memory accesses or I/O accesses such that AT bus timing requirements are satisfied. The AT bus clock (SYSCLK) is maintained constant at 1/4 the asynchronous clock (CLKASN).

Address and Data Bus

The HT12 uses a modified address and data bus design. The address bus is made up of the upper 15 address signals from the CPU and the lower 9 address signals from the SA bus. The remaining portion of the SA bus and the LA bus are generated externally using TTL latches and

buffers. The direct use of CPU high order addresses allows the chip to perform fast DRAM accesses. All peripherals normally connected to XA should be connected to A and SA.

The data bus consists of the 16-bit CPU D bus and the lower 8 bits of the SD bus. The upper 8 bits of the SD bus and the XD bus are generated externally using TTL buffers. The MD bus is eliminated in the design. On-board DRAMs and BIOS EPROMs are both tied to the CPU local D bus.

To generate MA for the row addresses in time for RAS, the row addresses must come directly from the CPU address bus especially when running at 16MHz. The HT12 must include address lines A(23:9) in its address bus and use the remaining pins to generate SA(0:7). Since only a portion of the SA bus is generated by the HT12, five TTL latches/buffers are used to generate the remaining SA and LA signals. Furthermore, although the column address timing is not as critical as the row address timing, to provide proper column MA, the SA signals must be latched with an Early ALE signal.

Memory Controller

The memory controller consists of five major sub-blacks:

ECONTROL

The ECONTROL block is used to generate the early control signals EALE,/EMEMR and /EMEMW. The /EMEMR and /EMEMW signals are synchronized to the processor clock for master cycles. Since A1 is not directly accessible, EALE is generated for CPU shutdown/half cycle as well, so that A1 can be accessed via SA1.

Memory Configurations

The HT12 supports 8 different RAM configurations using combinations of 64K, 256K and 1M × 1 or × 4 DRAMs. The RAM configuration is determined by three configuration pins (DACK:2-0) on power up. The RAM

configuration information is stored in the read/write System Configuration Register (index 04H and is overridable by software. The following is a table of valid RAM combinations.

Configuration	/DACK (Read)			Bank 0	Bank 1	Total
	2	1	0			
0	0	0	0	0K	0K	0K
1	0	0	1	256K	0K	512K
2	0	1	0	256K	64K	640K
3	0	1	1	256K	256K	1M
4	1	0	0	256K	1M	2.5M
5	1	0	1	1M	0K	2M
6	1	1	0	1M	1M	4M
7	1	1	1	—	—	Reserved

BIOS Shadowing and Memory Relocation

The HT12 supports BIOS shadowing in 16K blocks in the range of C0000 to FFFFF. In the case that 1M of memory is installed, the HT12 also supports relocation of memory from address A0000 to address FFFFF that are not used in shadowing to above 1M. The following table shows the various shadowing and relocation combinations. Basically, contiguous memory above A0000 that are not used in shadowing can be relocated in 64K blocks. However, the combination of shadowing in only C0000-CFFFF and F0000-FFFFF can have both A0000-BFFFF and D0000-EFFFF relocated.

Shadow Range	Reloc Range	Memory Relocated
No shadowing	A0000-FFFFF	384K
C0000-	A0000-BFFFF	128K
D0000-	A0000-CFFFF	192K
E0000-	A0000-DFFFF	256K
F0000-	A0000-EFFFF	320K
C0000-CFFFF, F0000-FFFFF	A0000-BFFFF, D0000-EFFFF	256K

For shadowing operations, the BIOS should first select the required shadowing ranges in Shadow RAM Configuration Registers 1 to 2. When an address range is selected for shadowing, it becomes accessible and write only. This allows the BIOS to load ROM data into the shadow RAM. After all the shadow RAM are loaded, the BIOS enables the shadowing feature by setting the Shadow Enable bit in the Misc Feature Enable Register, Index 14H. Once shadowing is enabled, the shadow RAM becomes read only and all read cycles to the selected address ranges will be directed to the shadow RAM.

PARGEN

Due to the tight RAM access time, RAM data are not valid until the very end of a RAM read. To ensure sufficient time for parity generation, parity generation logic is required to allow separate read and write path for the parity generation. Moreover, on a RAM read, the data are latched to provide more time for the parity to be generated.

ADDRTRAN

To support mixed 64K/256K/1M DRAMs, BIOS shadowing, EMS and memory relocation, an address translating and decoding block ADDRTRAN is required. Given the RAM configuration, the ADDRTRAN block performs address translations to relocate unused memory in segments A000-F000 to the top of memory and provides output signals to indicate shadow RAM accesses and relocated memory accesses.

RAMCONTROL

The RAMCONTROL logic is a state machine that generates the necessary RAS, CAS and WE signals. It provides 10MHz to 16MHz accesses in either 0 or 1 wait state.

MAGEN

The MAGEN block generates the row and column addresses for the DRAM. It supports mixed 64K, 256K and 1M DRAM types.

Nine read/write registers are available in the P11. They consist of eight configuration registers and a Hot reset and Gate A20 control register.

The configuration registers are accessed through the two I/O ports at locations 1ED and 1EF. Port 1ED serves as an index register in determining which configuration register is accessed at port 1EF. To access a configuration register, the corresponding index must first be written into the index register at location 1ED. The index register and all configuration registers are read/write register. The status registers are Read only.

The Hot reset and Gate A20 control register is a partial emulation of the PS/2 Port 92H. It supports the Hot Reset and the Gate A20 functionalities as defined in the PS/2 Technical Reference.

INDEXED CONFIGURATION REGISTERS

	Index Port: 1ED Data Port: 1EF
Index	**Resister**
10H	System configuration Register
11H	Reserved
12H	Shadow RAM configuration Register 1
13H	Shadow RAM configuration Register 2
14H	Misc Feature Enable Register
15H	Misc Status Register
16H	Extended Information Register
17H	Revision Information Register
18H	Top of Memory Register
19H	EMS Configuration Register
20H	EMS Page Register 0
21H	EMS Page Register 1
22H	EMS Page REgister 2
23H	EMS Page Register 3

I/O MAPPED REGISTERS

Address	**Register**
92H	Hot Reset and A20 Gate Control Register

NOTE: When modifying a configuration register **always** read the configuration register first. Change only the bits that must be changed, then write the data back to the register. This will insure compatibility with future design features.

SYSTEM CONFIGURATION REGISTER (INDEX: 10H)

Bit	7	6	5	4	3	2	1	0
		WS CTRL1	WS CTRL0	0 WS MEM	BUS SPEED	RAM SEL2	RAM SEL1	RAM SEL0

Bits	Accress	Default	Description (As Input during Power On Reset)
2-0	R/W	DACK2-0	RAM Configuration RAMSEL <2:0≥ — Bank 0 RAM Type — Bank 1 RAM Type — Total Size 0 — 0K — 0K — 0K 1 — 256K — 0K — 512K 2 — 256K — 64K — 640K 3 — 256K — 256K — 1M 4 — 256K — 1M — 2.5M 5 — 1M — 0K — 2M 6 — 1M — 1M — 4M 7 — — — — —
3	R/W	DACK3	AT Bus Speed 1: Low Speed on I/O 0: Full Speed
4	R/W	DACK5	0 Wait State Memory 1: 0 wait state memory 0: 1 wait state memory
6-5	R/W	DACK6-7	Wait State (Control* WSCTRL (1:0) 0 0: 1 extra Wait State for EMS + relocation cycles 0 1: 1 extra Wait State for EMS cycles only 1 0: 1 extra Wait State for Relocation Cycles only 1 1: No extra Wait State
7	R/W	TC	Reserved

Special Note: the DACK and TC lines are used as configuration inputs during power up reset.

*Wait state control can be used to add an extra wait state for the above cycle types. When a memory cycle of the selected type occurs, the cycle will not be started until one wait state later. For example, if WSCTRL <1:0> is set to 0, EMS cycles that require memory relocation would have an extra wait state inserted; that is, a normally 0 wait state cycle would become 1 wait state and a normally 1 wait state cycle would become 2 wait state. This allows additional RAM address setup time for high speed operations.

SHADOW RAM CONFIGURATION REGISTER 1 (INDEX: 12H)

Bit	7	6	5	4	3	2	1	0
	DC000 DFFFF	D8000 DBFFF	D4000 D7FFF	D0000 D3FFF	CC000 CFFFF	C8000 CBFFF	C4000 C7FFF	C0000 C3FFF

Bits	Access	Default	Description
0	R/W	0	Enable Shadowing C0000-C3FFF 1: Enable 0: Disable
1	R/W	0	Enable Shadowing C4444-C7FFF 1: Enable 0: Disable
2	R/W	0	Enable Shadowing C8000-CBFFF 1: Enable 0: Disable
3	R/W	0	Enable Shadowing CC000-CFFFF 1: Enable 0: Disable
4	R/W	0	Enable Shadowing D0000-D3FFF 1: Enable 0: Disable
5	R/W	0	Enable Shadowing D4000-D7FFF 1: Enable 0: Disable
6	R/W	0	Enable Shadowing D8000-DBFFF 1: Enable 0: Disable
7	R/W	0	Enable Shadowing DC000-DFFFF 1: Enable 0: Disable

SHADOW RAM CONFIGURATION REGISTER 2 (INDEX: 13H)

Bit	7	6	5	4	3	2	1	0
	FC000 FFFFF	F8000 FBFFF	F4000 F7FFF	F0000 F3FFF	EC000 EFFFF	E8000 EBFFF	E4000 E7FFF	E0000 E3FFF

Bits	Access	Default	Description
0	R/W	0	Enable Shadowing E0000-E3FFF 1: Enable 0: Disable
1	R/W	0	Enable Shadowing E4000-E7FFF 1: Enable 0: Disable
2	R/W	0	Enable Shadowing E8000-EBFFF 1: Enable 0: Disable
3	R/W	0	Enable Shadowing EC000-EFFFF 1: Enable 0: Disable
4	R/W	0	Enable Shadowing F0000-F3FFF 1: Enable 0: Disable
5	R/W	0	Enable Shadowing F4000-F7FFF 1: Enable 0: Disable
6	R/W	0	Enable Shadowing F8000-FBFFF 1: Enable 0: Disable
7	R/W	0	Enable Shadowing FC000-FFFFF 1: Enable 0: Disable

MISC FEATURE ENABLE REGISTER (INDEX: 14H)

Bit	7	6	5	4	3	2	1	0
			MEM PAR DIS	ENABLE 64K BIOS	256K-640K	RELOC ENABLE	SHADOW ENABLE	QUIET BUS

Bits	Access	Default	Description
0	R/W	1	Quiet Bus Enable 1: Enable 0: Disable
1	R/W	0	Enable Shadowing Function 1: Enable 0: Disable
2	R/W	0	Enable Relocation Functiion 1: Enable 0: Disable
3	R/W	1	Enable Memory 40000H-9FFFFH 1: Enable 0: Disable
4	R/W	0	Enable 64K BIOS This option selects the size of the system BIOS. When enabled, the system BIOS occupies only the 64K addressing space F000:0000-F000:FFFF. When disabled, the system BIOS occupies the normal AT compatible 128K addressing space E000:0000-F000:FFFF. 1: Enable 0: Disable
5	R/W	0	Memory Parity Disable This optiona allows memory parity to be disabled regardless of the port 61H bit 2 setting. 0: Don't disable parity 1: Disable Parity
6-7	R/W		Reserved Must be set to 0 by BIOS on power up.

MISC STATUS REGISTER (INDEX: 15H)

Bit	7	6	5	4	3	2	1	0
							NMI	8042
	0	0	0	0	0	0	EN	A20GATE

Bits	Access	Default	Description
0	R		8042 A20Gate 1: A20 Enabled 0: A20 Forced Low
1	R		NMI Enable Status 1: NMI Enabled 0: NMI Disabled (inverse of data written at Port 70)
2-7	R	0	Reserved

EXTENDED INFO REGISTER (INDEX: 16H)

Bit 7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Bits	Access	Default	Description
0-7	R	0	Reserved

REVISION INFO REGISTER (INDEX: 17H)

Bit 7	6	5	4	3	2	1	0
CHIP ID	CHIP ID	CHIP ID	CHIP ID	REV	REV	REV	REV

Bits	Access	Default	Description
3-0	R		Revision Number 0 = Rev. A
7-4	R	1	HT12 Identification Number

TOP OF EXTENDED MEMORY REGISTER (INDEX: 18H)

Bit 7	6	5	4	3	2	1	0
		TA 21	TA 20	TA 19	TA 18	TA 17	TA 16

Bits	Access	Default	Description
0-5	R/W	03FH	Top of Extended Memory This register specifies the top of extended memory with a granularity of 64K. Extended memory address must be less than or equal to the Top of Memory setting. The memory above the Top of Extended Memory and below the total available memory can be used for EMS. This register defaults to 03FH (No EMS memory). On power up, the BIOS should set this register to reflect the actual top of extended memory.
6-7			Reserved

EMS Configuration Register (Index: 19H)

Bit 7	6	5	4	3	2	1	0
EMS EN	PAGE ADDR2	PAGE ADDR1	PAGE ADDR0	PAGE3 EN	PAGE2 EN	PAGE1 EN	PAGE0 EN

Bits	Access	Fefault	Description
0	R/W	0	Page Enable 0 1: Enalbe 0: Disable If the Global EMS Enable is on (1), the enable bit associated with each EMS page enables or disables the corresponding page.
1	R/W	0	Page Enable 1 1: Enable 0: Disable
2	R/W	0	Page Enable 2 1: Enalbe 0: Disable
3	R/W	0	Page Enable 3 1: Enable 0: Disable
4-6	R/W	0	EMS Page Starting Address: 0 (000): C000:0000 1 (001): C400:0000 2 (010): C800:0000 3 (011): CC00:0000 4 (100): D000:0000 This starting address specifies the address of EMS page 0.EMS page 1 to 3 follow consecutively in 16K increments.
7	R/W	0	Global EMS Enable 1: Enable 0: Disable If the Global EMS Enable is off (0), all EMS pages are disabled regardless of their individual enable bit.

EMS PAGE REGISTERS 0-3 (INDEX: 20H-23H)

Bit 7	6	5	4	3	2	1	0
PA 21	PA 20	PA 19	PA 18	PA 17	PA 16	PA 15	PA 14

Bits	Access	Default	Description
0-7	R/W		Translated EMS address lines

PORT 92H (HOT RESET AND GATE A20)

Bit 7	6	5	4	3	2	1	0
						GATE	HOT
0	0	0	0	0	0	A20	RESET

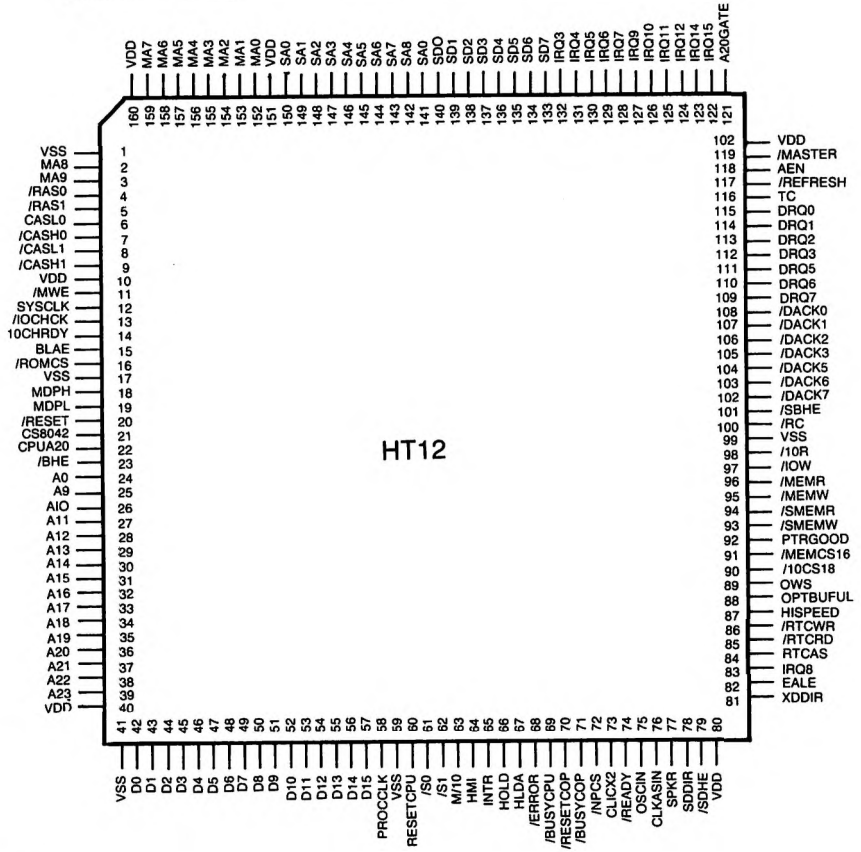
Bits	Access	Default	Description
0	R/W	0	Hot Reset This function provides an alternate means to reset the CPU. When this bit is set high, it triggers an alternate reset pulse to the reset logic. The reset occurs after a minimum of 6.72us and the entire reset operation takes 13.4us. When the reset bit is set to 1, it remains set until cleared by the BIOS. 1: Reset 0: Clear reset
1	R/W	0	Gate A20 1: A20 active 0: A20 inactive
2-7	R	0	Reserved

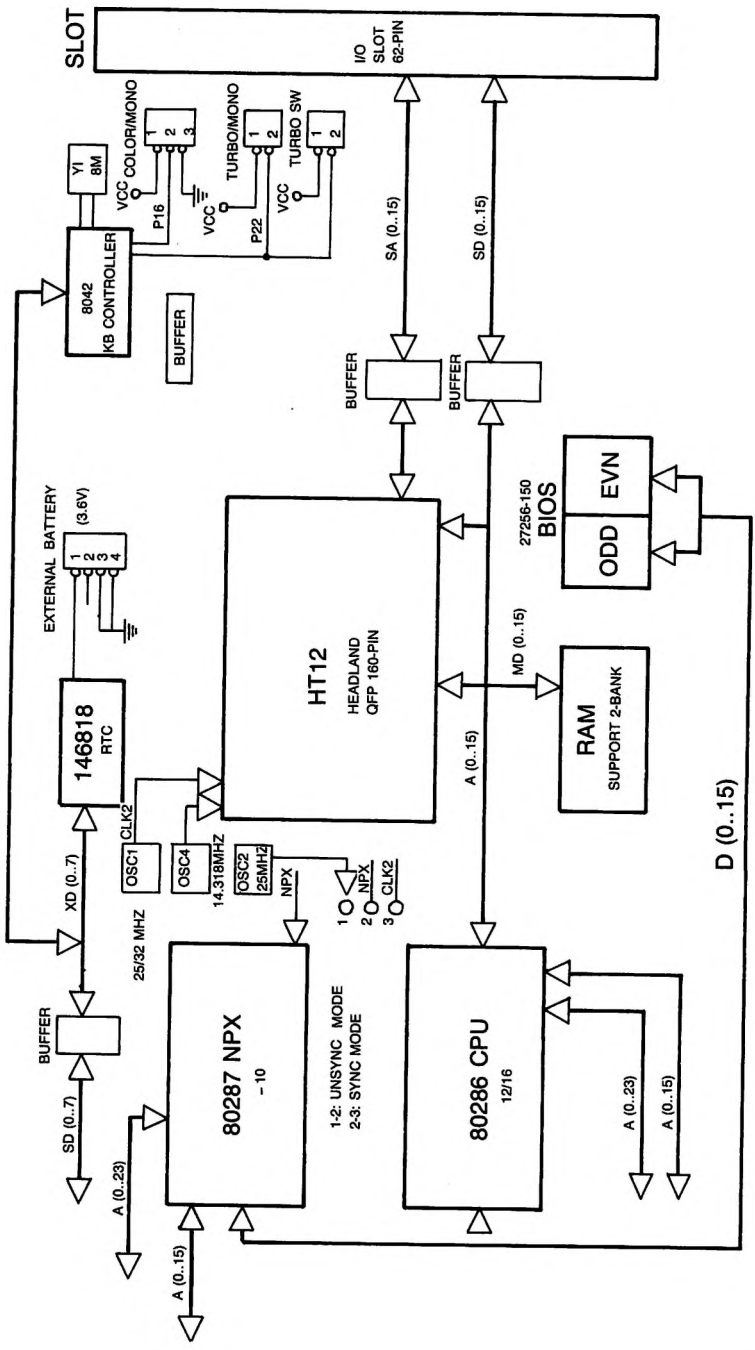
CHARTER 4

SCAT SYSTEM HARDWARE CONFIGURATION

SUPPORT TO SCAT HARDWARE SIGNAL DEFINIATION AND SIGNAL HOW TO ACTION FOR SCAT SYSTEM ALL ARCHITECTURE.

4-1. SCAT PIN DIAGRAM & ASSIGNMENT FOLLOWING IN FIGURE 4-1.




SLOT
I/O SLOT 62-PIN
SA (0..15)
SD (0..15)
Y1 8M
VCC COLOR/MONO
P16
VCC TURBO/MONO
P22
VCC TURBO SW
8042 KB CONTROLLER
BUFFER
BUFFER
BUFFER
EXTERNAL BATTERY (3.6V)
146818 RTC
CLK2
OSC1
OSC4
14.318MHZ
OSC2 25MHZ
NPX
1 NPX
2 CLK2
3
HT12 HEADLAND QFP 160-PIN
MD (0..15)
A (0..15)
27256-150 BIOS
ODD EVN
RAM SUPPORT 2-BANK
D (0..15)
XD (0..7)
25/32 MHZ
BUFFER
SD (0..7)
A (0..23)
A (0..15)
80287 NPX -10
1-2: UNSYNC MODE
2-3: SYNC MODE
80286 CPU 12/16
A (0..23)
A (0..15)

4-2 I/O Channel Signal Description

All signal are TTL-compatible with a maximum loading of two low-power (LS) devices.

CLK (Output)
This is the 8MHz system clock. It is a synchronous microprocessor cycle clock. This signal should be used for synchronization.

RESET DRV (Output)
This signal goes high during power-up, low line-voltage, or hardware reset.

SA0-19 (Input/Output)
The System Address Line run from bit 0 to 19. They are latched on to the falling edge of "BALE".

LA17-23 (Input/Output)
The Unlatched Address Line run from bit 17 to 23.

SD0-15 (Input/Output)
System data bit 0 to 15.

BALE (Output)
The Buffered-address Latch enable is used to latch SA0-19 on the falling edge. This signal is force high during DMA cycle.

I/O CH CHK (Input)
The I/O Channel Check is an active low signal which indicates that a parity error exist in I/O board.

I/O CH RDY (Input)
This signal lengths the I/O or memory read/write cycle and should be held low with valid address. It can only be held low for a maximum of 2.5 microseconds.

IRQ3-7, 9-12, 14-15 (Input)
The Interrupt Request signals which indicate I/O service request attention. They are prioritized in the following sequences:
Highest IRQ 9, 10, 11, 12, 14, 15, 3, 4, 5, 6, 7 Lowest.

-IOR (Input/Output)
The I/O Read Signal is an active low signal which instructs the I/O device to drive its data onto the data bus.

-IOW (Input/Output)
The I/O write is an active low signal which instructs the I/O device to read data from the data bus.

-SMEMR (Output)
The System Memory Read is low while the low 1 mega byte of memory is being used.

-MEMR (Input/Output)
The Memory Read Signal is low while any memory location is being read.

-SMEMW (Output)
The System Memory Write is low while the low 1 mega byte of memory is been written.

-MEMW (Input/Output)
Memory Write is low while any memory location is been written.

DRQ 0-3, 5-7 (Input)
DMA Request channel 0 to 3 are for 8-bit data transfer.
DMA Request channel 4 is used internaly on the system board.
DMA Request should be held high until the corresponding DMA inactive. Their priority is in the following sequence:
Highest DRQ 0, 1, 2, 3, 5, 6, 7 Lowest.

DACK 0-3, 5-7 (Output)
The DMA Acknowledge 0 to 3,5 to 7 are the corresponding acknowledge signals for DRQ 0 to 3, 5-7.

AEN (Output)
The DMA Address Enable is high when the DMA controller is driving the address bus. It is low when the 80286 CPU is driving the address bus.

-REFRESH (Input/Output)
This signal is to indicate the memory refresh cycle is in progress.

T/C (Output)
Terminal Count provides a puls when the terminal count for any DMA channel is reached.

SBHE (Input/Output)
The System Bus High Enable indicates high byte SD8-15 is on the data bus.

-MASTER (Input)
The Master is the signal from the I/O processor which gains control as the master and should be held low for a maximum of 15 microsecond or system memory may be lost due to the lack of refresh.

-MEM CS16 (Input, Open collector)
The Memory Chip Select 16 indicates that the present data is a 1 Wait State 16-bit data memory operation.

-I/O CS16 (Input, Open collector)
The I/O Chip Select indicates the present data transfer is a 1 Wait State 16-bit data I/O operation.

OSC (Output)
The Oscillator is a 14.31818 MHz signal used for the color graphic board.

0WS (Input, Open collector)
The 0 Wait State indicates to the microprocessor that the present bus cycle can be completed without inserting any additional wait cycles.

4-3 Timers

The system board has 3 programmable counter/timers in 82C235 chip.

Timer Channel 0: System timer to interrupt controller.
Timer Channel 1: Dynamic RAM refresh request.
Timer Channel 2: Speaker tone generator.

4-4 DMA Controllers

The system board has 2 programmable DMA controllers in 82C235 chip.

DMA Channel 0: spare
DMA Channel 1: IBM SDLC.
DMA Channel 2: Diskette adapter.
DMA Channel 3: spare
DMA Channel 4: Cascade for DMA controller 1
DMA Channel 5: spare
DMA Channel 6: spare
DMA Channel 7: spare

4-5 Interrupt Controllers

82C235 Integrated peripheral controller provide 16 levels of system interrupts. They are listed in priority as follows:

Interrupt Level	Description
NMI	Parity check error
IRQ0	System timer interrupt from timer
IRQ1	Keyboard output buffer full
IRQ2	Interrupt rerouting from IRQ8 through IRQ15
IRQ3	Serial port 2
IRQ4	Serial port 1
IRQ5	Parallel printer port 2
IRQ6	Floppy disk adapter
IRQ7	Parallel printer port 1
IRQ8	Realtime clock
IRQ9	Recounting to INT 10 from hardware IRQ2
IRQ10	Spare
IRQ11	Spare
IRQ12	Spare
IRQ13	Math Coprocessor 80287
IRQ14	Hard disk adapter
IRQ15	Spare

4-6 Real Time Clock and Nonvolatile RAM

The real time clock is included in 82C235, and its 114 bytes of RAM information are backed up by a 3.6V DC battery. The internal clock circuit uses 14 bytes while the rest is allocated to system configuration.

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minutes alarm
04	Hours
05	Hours alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status Register A
0B	Status Register B
0C	Status Register C
0D	Status Register D
0E	Diagnostic status byte
0F	Shutdown
10	Diskette drive type byte-drive A and B
11	Reserve
12	Fix disk type byte-drive C and D
13	Reserve
14	Equipment byte
15	Low-base memory
16	High-base memory
17	Low-extension memory
18	High-extension memory
19-2D	Reserve
2E-2F	2-byte CMOS checksum
30	Low-extension memory byte
31	High-extension memory byte
32	Date century byte
33	Information flag (set during power on)
34-3F	Reserve

CHAPTER 5

TROUBLESHOOTING

This chapter provides explanations and possible troubleshooting procedures for hardware and software errors that may occur during setup and operation of the BM-2C/2D motherboard. Product support and service information are provided in the event that further technicall assistance or product service is required.

5.1 Hardware and CMOS Errors

Troubleshooting Hardware Problems

If you are unable to obtain a display on the screen or beeps from the speaker after motherboard installation, follow the listed troubleshooting procedures:

1. Check to ensure that the power supply is properly connected and supplying current to the motherboard.
2. Make sure that the main board is not shorted electrically to the case in any way.
3. Check to ensure that the BIOS ROM is seated properly in its socket.
4. Make sure that the CPU and memory are seated securely and no pins are bent.
5. Make sure that add-on cards are firmly seated and are not shorting out any pins in the expansion slot.
6. Press <INS> key when power on until memory test begins. This step will reset CMOS parameters to default values.

If, after following these steps, you are still not able to obtain a display or beep, contact your dealer for assistance.

CMOS Error Messages

The AMI BIOS performs various diagnostic tests at the time the system is powered up. This procedure is refered to as POST (Power On Self Test) and tests the various hardware components in your system. Warning beeps and messages during the POST tests at power on indicate errors encountered by the built-in diagnostics. If an error is encountered before the display device is initialized, no message will be displayed. If the error encountered is non-fatal, the POST will continue after the error is reported. All fatal errors will halt the system. This section lists the most often encountered error messages and the recommended action.

POST Beep Count and Error Condition

If there is no display on the screen but you bear beeps sounding from the speaker, count the number of beeps and refer to the following list for the error condition.

Beeps	Error Condition
1	DRAM refresh is not working.
2	Parity Circuit is not working.
3	First 64K memory test failure.
4	System timer is not counting properly.
5	Processor register/flag test failure.
6	Keyboard controller gate-A20 failure.
7	Virtual mode exception error.
8	Display memory R/W test failure. (Non-Fatal).
9	ROM-BIOS checksum error.

Consult the following table for the recommended action if you receive error beeps from the system speaker.

Beeps	Recommended Action
3	Check to ensure that all memory have been properly installed and that no pins are bent. You may have defective memory chips.
8	Check to ensure that your display adapter is securely inserted into the slot. Display adapter may be defective.
All Others	Your motherboard may be defective. Contact your dealer for assistance.

Fatal Error Messages

If you encounter the following fatal error messages during system boot-up, your motherboard may be defective:

GATE-A20 Error
INTERRUPT CONTROLLER #1 FAILURE

These errors will halt all system operations. Contact your dealer for assistance.

Non-Fatal Error Messages

Keyboard Error: Check to ensure that the keyboard has been connected and that the cable connector is tightly inserted into the keyboard connector socket. Be sure that the AT/XT switch on your keyboard is set to the AT position.

Keyboard/Interface Error: Same as above.

CMOS Battery State Low: Indicates a low charge in the on-board battery. Leave system powered on so that the battery may have a chance to recharge. If the problem persists, have your dealer inspect the battery to determine whether a replacement is needed.

CMOS System Option Not Set: System configuration detected does not match what is specified in the CMOS setup. Perform the BIOS CMOS setup to ensure that parameters are set properly.

CMOS Checksum Failure: Perform CMOS setup to ensure parameters are properly set.

CMOS Memory Size Mismatch: Memory size has been changed and does not match what is specified in the CMOS setup. Perform the BIOS CMOS setup.

CMOS System Time and Date Not Set: The system has lost back-up power and the time and date information needs to be re-entered. Perform CMOS setup.

CMOS Display Configuration Mismatch: The installed display adapter has not been properly specified in the CMOS setup. Enter CMOS setup and make the necessary correction.

Display Switch Setting Not Proper: The display type jumper switch has been set incorrectly. Verify that the jumper selection matches the display adapter installed.

Keyboard is Locked-Unlock It: The keylock switch on your computer case has been activated. The keyboard is locked out until you unlock it.

Floppy Disk Controller Failure: Check to ensure that the disk controller card has been installed properly and that it is tightly seated in the slot. Your disk controller card may be defective.

HDD Controller Failure: Same as above.

C: Drive Error/Failure: Check to ensure that the drive type has been properly specified in the CMOS setup and that the drive has been low-level formatted. Make sure the hard drive is spinning and all cables have been securely connected. Your hard drive may be defective.

D: Drive Error/Failure: Same as above.

5.2 Product Support Information

You should be able to rely on the user's manual to answer questions about installing and configuring the BM-2C/2D motherboard. If you do encounter a technical problem that you can not resolve, contact a technical support specialist at an authorized dealer for assistance.

We ask you to follow these steps before you call or write:

- Read the section of the manual that describes the procedure you are trying to perform.
- If the problem relates to your software, check to insure that the software is properly configured.
- Please include the following information in your letter, or have it in front of you when you phone:

  Motherboard Model & Serial Number
  DOS Version
  Hardware & Peripherals Used
  Contents of *AUTOEXEC.BAT* File
  Contents of *CONFIG.SYS* File
  Any RAM Resident Programs Used

If, after following these steps, you are still not able to solve the problem, contact your dealer for technical support. If writing, be sure to include your daytime phone number and the best time to reach you.

APPENDIX A