RadiSys®

Base-G

Long-Life Pentium Based NLX Baseboard

User's Guide

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1.0 Baseboard Description

1.1 Functional Overview

The Base-G is a Pentium-based, NLX compliant PC-compatible baseboard. The Base-G baseboard requires a NLX compliant chassis with integrated riser card and power supply. The NLX riser card provides bus termination, power connection, floppy drive connection, hard drive connections, and PCI/ISA expansion.

Base-G NLX baseboard features include the following:

Intel Processor
- 233MHz Pentium with MMX technology

Main Memory
- Three 168-pin DIMM sockets
- Supporting up to 512Mbytes DRAM
- Supports 50-60ns EDO or 60-70ns FPM (non-parity, parity or ECC)

Intel 82430HX PCI Chip-set
- 82439HX provides the following: DRAM control, cache support and PCI to local bus bridge
- 82371SB (PIIX3) provides the following: PCI to ISA bridge, two EIDE controllers and interrupt controller

Integrated SMC FD37C669 Super I/O
- Integrates the following: two asynchronous RS-232C FIFO serial ports, one IEEE-1284-1984 and Centronics compatible, ECP, EPP parallel port, 8042 compatible keyboard controller, 765A compatible floppy controller

Standard NLX Riser Connector Expansion Slot Support
- Up to two PCI slots
- Maximum of four ISA slots

Ethernet
- Digital 21143 10/100BaseTX with RJ45 with RJ45 connector

Video Graphics
- Option: RadiSys SBCPMCM64A PMC SVGA video module with ATI 3D Rage II+ controller

I/O Connectors
- Two serial port 9-pin male D-sub
- One parallel port 25-pin female D-sub
- Two IPS-2 6-pin mini DIN for keyboard/mouse
- One ethernet female RJ45
- One SVGA 15-pin female D-sub
- Standard NLX I/O shield

Other Features

- Phoenix BIOS
- Plug and Play Compatible
- Support for Advanced Power Management (APM)
- Benchmarq BQ3285 Real Time Clock

1.2 Base-G Features

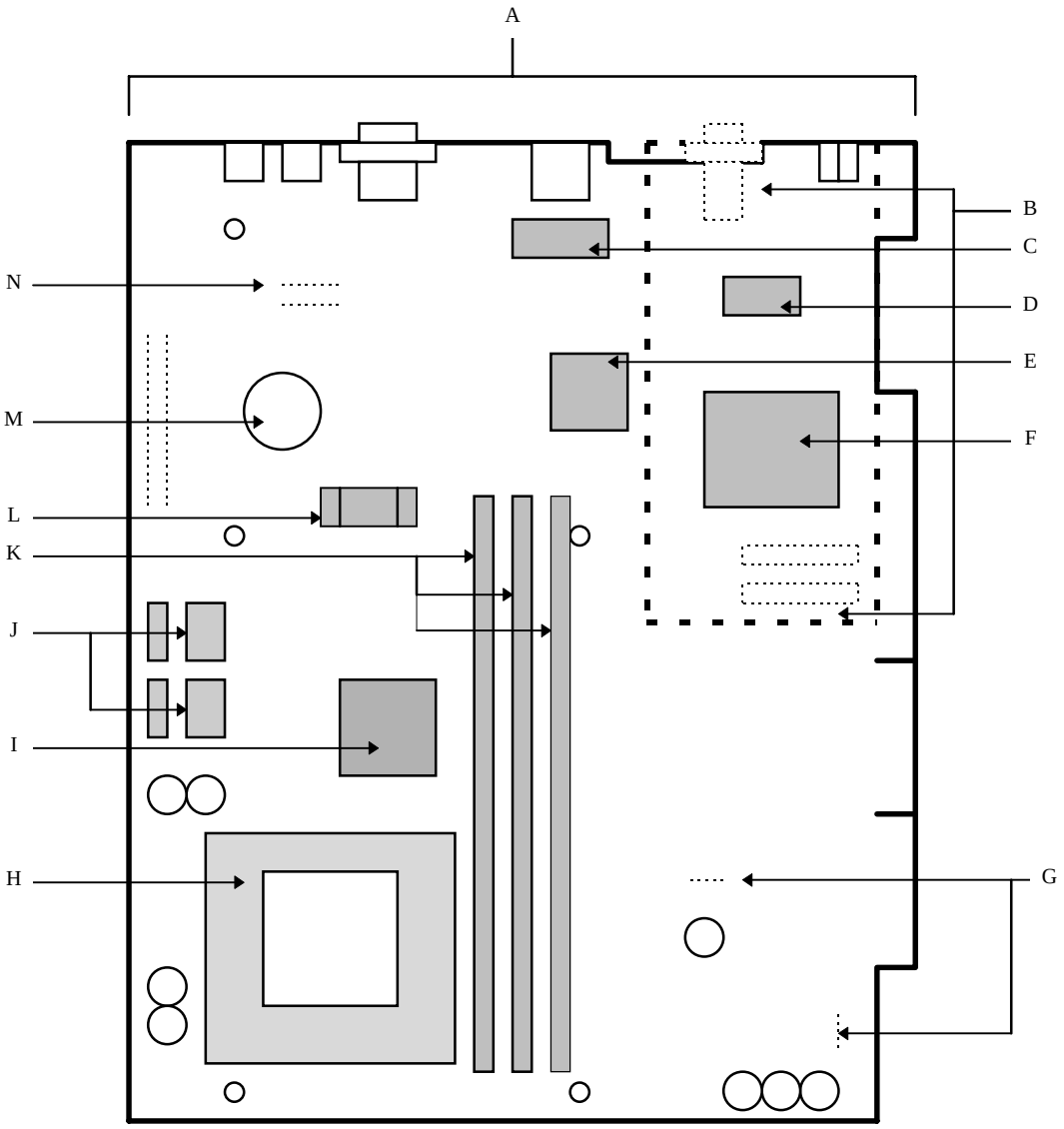
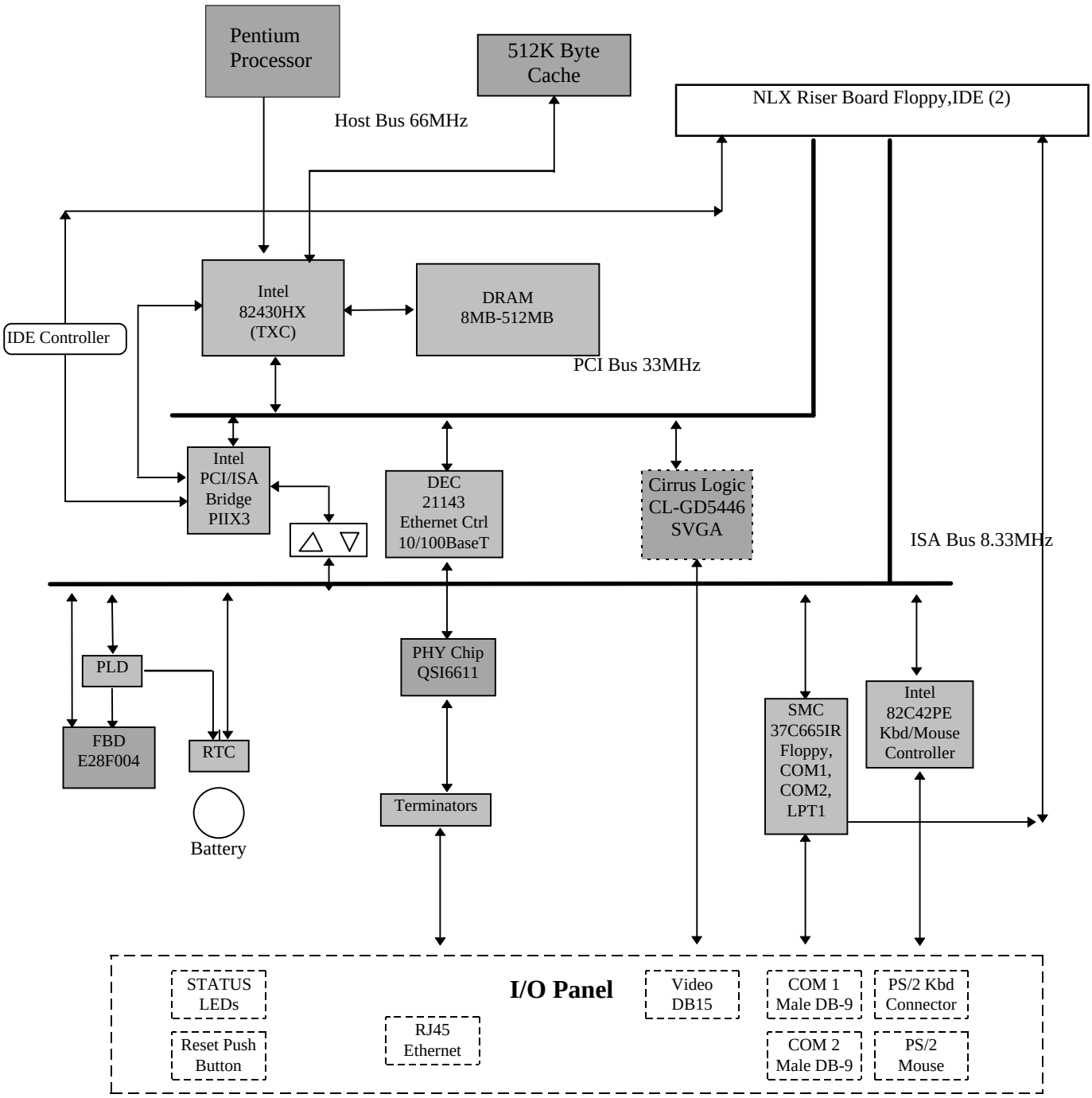


Figure 1. Baseboard Features

A. I/O connectors
B. Optional PMC SVGA video module
C. QSI 6611 PHY (Physical Interface)
D. SMC 37C66R integrated Super I/O
E. Digital 21143 10/100Base-TX ethernet controller
F. Intel 82371SB (PIIX3)
G. MMX reset jumpers
H. Pentium MMX processor socket
I. Intel 82439HX
J. 512K flash SRAM
K. DIMM sockets
L. BIOS flash
M. Battery
N. BIOS force recovery jumper

1.3 Base-G Block Diagram.



1.4 Memory

1.4.1 DRAM Memory

The Base-G baseboard has three Dual Inline Memory Module (DIMM) gold plated sockets. The DRAM DIMMs must be gold plated. DIMM memory can be installed in only one socket if required. The 82430HX chip-set supports up to 512Mbytes of DRAM memory.

EDO (50ns-60ns) and FPM (60ns-70ns) DRAM is supported. Different DIMM memory sizes can be installed to any DIMM socket. EDO and FPM DIMM memory can both be installed in different sockets on the same board. The Base-G supports both 64-bit non-parity and 72-bit ECC DRAM DIMMs. Non-parity and ECC memory and cannot be mixed. If ECC memory is to be used, all sockets must contain ECC DIMMs. The minimum memory size is 8 Mbytes, the maximum memory is size is 512Mbytes. The BIOS automatically detects the memory type, size and speed.

Base-G memory supports the following:

- 168-pin 3.3V DIMMs with gold plated contacts
- 50ns - 60ns 3.3V unbuffered EDO memory
- 60ns-70ns FPM memory
- Caching of the first 64 Mbytes of main memory
- 64-bit data path
- Single or double-sided DIMMs

DIMM Size
8 Mbyte
16 Mbyte
32 Mbyte
64 Mbyte
128 Mbyte
256 Mbyte

Please see Appendix C for DIMM module insertion and DIMM module removal instructions.

Memory Performance.

Processor Cycle Type (pipelined)	Clock Count (ADS# to BRDY#)	Comments
Burst read page hit	7-2-2-2	EDO
Read row miss	9(12)-2-2-2 (see note)	EDO
Read page miss	12-2-2-2	EDO
Back-to-back burst reads page hit	7-2-2-2-3-2-2-2	EDO

Note: Numbers in parentheses indicate additional lead-off cycles needed when the page isn't open.

1.4.2 Second-level Cache

The Base-G includes 512KB of L2 write-back cache, consisting of two 64 Kbit x 32 Pipeline PBSRAM devices and two 32Kbit x 8 external Tag SRAM soldered to the baseboard.

	Sync Pipelined Burst
CACHE size:	512K
Data SRAMs:	64Kx32 (3V)
Data SRAM Speed:	8.5ns
Tag bits:	11
Tag SRAMs:	16Kx8 (5V)
Tag SRAM speed:	15ns
Burst Reads:	3-1-1-1
Burst Writes:	3-1-1-1
Pipelined Burst Reads:	3-1-1-1-1-1-1-1

1.5 PCI Chip-set

The Base-G board uses the Intel 82430HX chip-set, consisting of the 82439HX System Controller (TXC), and the 82371SB PCI ISA IDE Xcelerator (PIIX3)..

1.5.1 82430HX

The 82430HX (TXC) System Controller provides the DRAM controller, cache controller, PCI bus interface, and host bus interface. TXC features include the following:

- Host-to-PCI microprocessor interface control
- Integrated L2 cache controller
- Integrated DRAM controller
- Fully synchronous , minimum latency PCI bus interface

1.5.1 82371SB (PIIX3)

The PIIX3 generates ISA bus signals, provides a fast IDE interface, 82C54 timer, two 82C59 interrupt controllers, two 8237 DMA controllers, and system power management. PIIX3 features implemented on the Base-G include the following:

- PCI-to-ISA bridge
- Integrated dual-channel enhanced IDE interface
- Interrupt controller based on the 82C59
- 16-bit counters/timers based on the 82C54
- Enhanced DMA controller
- Power management logic

1.6 Super I/O Chip SMC FDC37C665IR

The SMC FDC37C665IR Super I/O chip resides on the ISA bus. Each feature this device provides accessed at standard PC locations. FDC37C665IR Super I/O features implemented on the Base-G include the following:

- Standard PC floppy disk port
- Two standard PC serial ports (COM1 and COM2)
- Standard PC parallel port..

1.7 Serial Ports

The SMC FDC37C665IR Super I/O chip implements a set of standard PC serial (COM) ports. The COM ports are compatible with standard 16C450/16C550 architectures. COM1 is at I/O addresses 3F8-3FF, and uses IRQ4. COM2 is at I/O addresses 2F8-2FF, and uses IRQ3.

The COM1 and COM2 signals are buffered to EIA/TIA-232-E levels, and are connected to a standard male DB9 connector at the front panel. ESD protection devices provide a high-voltage shunt from the serial port external signals to chassis ground. Ferrite beads are used on the signals as they cross the boundary from chassis ground reference to board signal ground reference, providing an EMI block.

1.8 Parallel Port

The SMC FDC37C665IR Super I/O chip implements an IEEE-1284-C bi-directional parallel port. The port can be configured to run in standard mode, enhanced mode (EPP), or Microsoft high speed mode (ECP). MS-DOS and Windows will recognize this port as LPT1 (I/O address = 378-37B, IRQ7). The parallel port is interrupt is IRQ7 only.

The parallel port signals are series terminated or pulled up by resistors, as directed for an IEEE-1284-II driver by the IEEE-1284-1994 specification.

The parallel port signals are not buffered and are routed to the NLX I/O shield backplane connector.

1.9 Floppy

The SMC FDC37C665IR Super I/O chip implements a standard PC floppy disk port. This port resides on the ISA bus, and is accessed at the standard PC I/O addresses of 3F0h-3F7h. The floppy interrupt is IRQ6 only. The following floppy drive capacities/sizes are supported:

- 360KB, 5.25”
- 1.2BB, 5.25”
- 720KB, 3.5”
- 1.2BB, 3.5”
- 1.44BB, 3.5”
- 2.88BB, 3.5”

The floppy interface signals are routed to the NLX riser card following NLX guidelines. The standard 34 pin floppy header resides on the NLX riser card.

1.10 IDE

There are two independent bus mastering PCI IDE interfaces, with each interface supporting 1 master and 1 slave peripheral. The PIIX3 controls the bus master Enhanced IDE interface, with support for Modes 1,2,3,4 as well as Bus Master (DMA) Modes 0,1 and 2. The legacy IDE register at I/O address 3F7 is not supported. The IDE circuitry contains an 8 x 32 bit buffer for Bus Master IDE PCI burst transfers and can transfer data at rates up to 22Mbytes/second.

The BIOS does not automatically detect the presence of an IDE/EIDE hard drive at power-up. Set-up must be used to enable and detect an IDE/EIDE hard drive.

Only PCI Masters have access to the IDE port. ISA Bus masters cannot access the IDE I/O port addresses. The IDE data transfer command strobes, DMA request/grant signals, and IORDY signal interface directly to the chip-set. The IDE data lines also interface directly to the chip-set and are buffered to provide part of the ISA address bus as well as the XD bus chip select signals. The IDE address and chip select signals are multiplexed onto the LA[23-17] lines.

1.11 Keyboard and Mouse

An Intel S82C42PE with Phoenix MultiKey/42G firmware is used to implement a PC compatible keyboard and mouse controller. The device resides on the ISA bus, and is accessed at the standard PC I/O addresses of 60h and 64h. IRQ1 is used for the keyboard and IRQ12 is used for the mouse.

The BIOS allows booting without a keyboard.

The keyboard and mouse interface signals are routed to I/O Shield connectors. The pinout for these connectors are shown in the Mechanical Details section of this document. This specific signals routed are as follows:

1.12 On-board Ethernet

The PCI based Ethernet controller is the Digital 21143-TF. Both 10BASE-T and 100BASE-TX are supported.. The 10/100BASE-TX connection is a RJ45 connector via NLX I/O Shield. The PCI interrupt is INTB with REQ0 and GNT0 used, configured via standard PCI configuration space registers.

A QSI 6611 PHY (Physical Interface) chip is used with the Digital 21143 for 100BASE-TX network support. The QSI 6611 utilizes a symbol based interface between the two chips.

1.13 Optional SVGA Graphics

This Base-G video option is the RadiSys SB PMCM64A graphics card, containing the ATI 3D Rage II+ SVGA video controller. A standard 15-pin SVGA connector is provided via the NLX I/O Shield. The graphics card is on a standard PMC card using a standard PMC connection 15mm PMC to the PCI bus. This provides simple, modular, on-board video.

If a PCI SVGA board is installed in a PCI slot on the NLX riser, the local SVGA graphics controller is automatically disabled by the BIOS. If an ISA based video controller is installed in a ISA slot on the NLX riser, the PCI and/or PMC based controllers will be disabled. Only the ISA video controller is enabled.

1.14 Baseboard Connectors

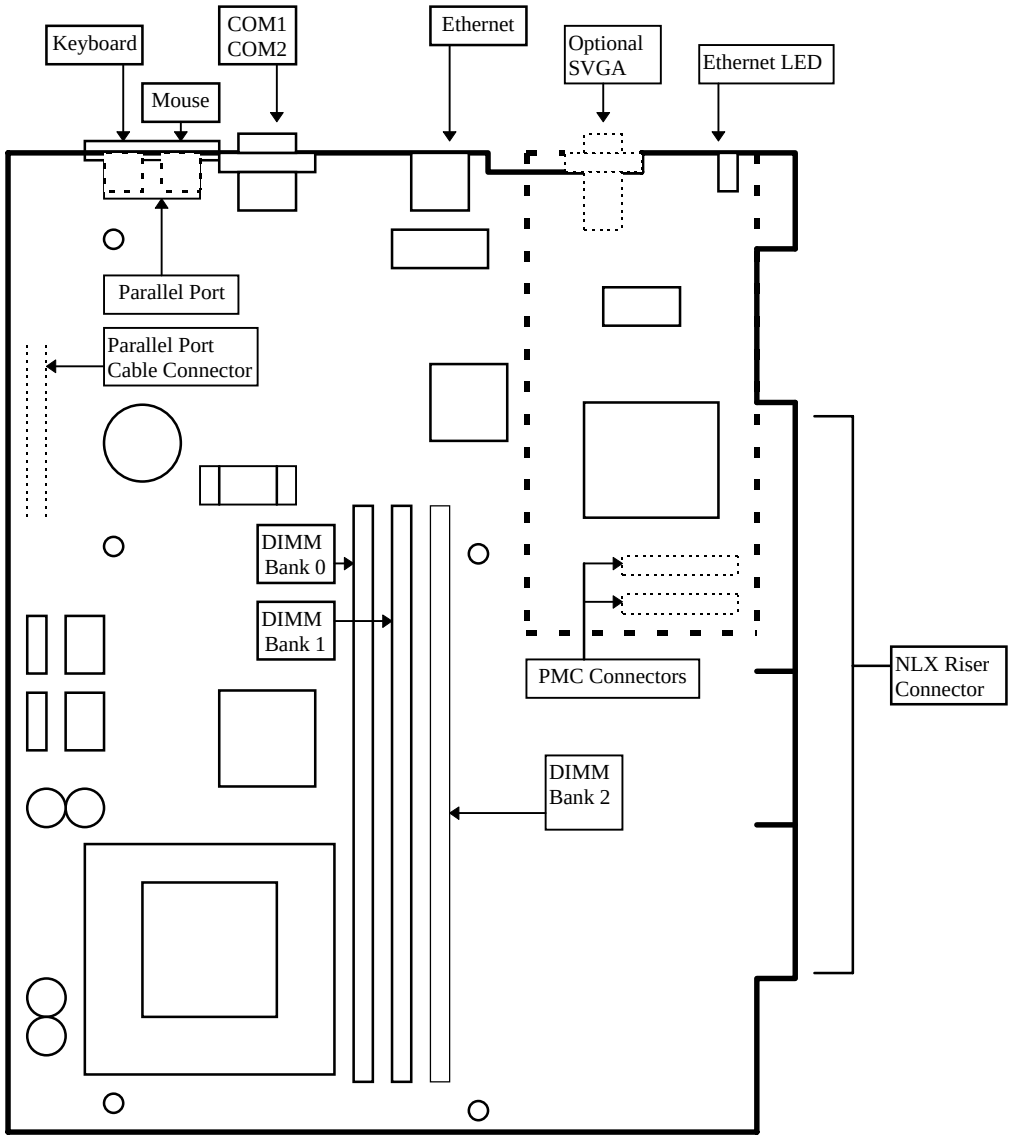


Figure 2. Baseboard Connectors

1.14.1 NLX Card Edge Connector

The Base-G NLX baseboard connects to the NLX riser via a 340 pin, 1mm pitch, card edge connector. The Base-G NLX compliant card edge connector provides the following:

- PCI expansion bus signals
- ISA expansion bus signals
- EIDE signals
- Floppy signals
- Misc. front panel signals
- Power

The NLX specification requires the riser to provide the following:

- PCI expansion slots
- ISA expansion slots
- IDE connectors/headers
- One floppy connector/header
- Front panel signals
- Power supply connector

1.14.1.1 Riser Interconnect Pin-out

The following is the pin-out for the riser card edge connector. The A side is the secondary (bottom) of the baseboard. The B side is the primary (top) of the baseboard. Pin 1 is towards the baseboard I/O connectors.

Table 1. PCI Segment, Riser Interconnect Pin-out

Pin #	Signal Name	Type	I/O	Termination	Pin #	Signal Name	Type	I/O	Termination
Al	-12V	PWR	NA	NA	B 1	PCSPKR-RT	AUDIO	O	NA
A2	REQ4#	PCI	I	RIS	B2	+12V	PWR	NA	NA
A3	+12V	PWR	NA	NA	B3	PCSPKR-LFT	AUDIO	O	NA
A4	GNT4#	PCI	O	RIS	B4	+12V	PWR	NA	NA
A5	3.3VDC	PWR	NA	NA	B5	PCICLKO	PCI	O	BB
A6	PCIINT3#	PCI	I	RIS	B6	GND	PWR	NA	NA
A7	3.3VDC	PWR	NA	NA	B7	PCICLKI	PCI	O	BB
A8	PCIINTO#	PCI	I	RIS	B8	SER-IRQ	MISC	I/O	BB
A9	PCIINTI#	PCI	I	RIS	B9	PCIINT2#	PCI	I	RIS
A1O	PCICLK2	PCI	O	BB	B1O	3.3VDC	PWR	NA	NA
A11	3.3VDC	PWR	NA	NA	B11	PCICLK3	PCI	O	BB
A12	PCI-RST#	PCI	O	BB	B12	GND	PWR	NA	NA
A13	GNTO#	PCI	O	RIS	B13	GNT3#	PCI	O	RIS
A14	PCICLK4	PCI	O	BB	B14	3.3VDC	PWR	NA	NA
A15	GND	PWR	NA	NA	B15	GNT2#	PCI	O	RIS
A16	GNTI#	PCI	O	RIS	B16	AD[31]	PCI	I/O	RIS
A17	3.3VDC	PWR	NA	NA	B17	REQO#	PCI	I	RIS
A18	REQ2#	PCI	I	RIS	B18	GND	PWR	NA	NA
A19	REQ3#	PCI	I	RIS	B19	AD[29]	PCI	I/O	RIS
A20	AD[30]	PCI	I/O	RIS	B20	AD[28]	PCI	I/O	RIS
A21	GND	PWR	NA	NA	B21	AD[26]	PCI	I/O	RIS
A22	AD[25]	PCI	I/O	RIS	B22	3.3VDC	PWR	NA	NA
A23	REQI#	PCI	I	RIS	B23	AD[24]	PCI	I/O	RIS

Table 1. PCI Segment, Riser Interconnect Pin-out (cont.)

Pin #	Signal Name	Type	I/O	Termination	Pin #	Signal Name	Type	I/O	Termination
A24	AD[27]	PCI	I/O	RIS	B24	C/BE[3]#	PCI	I/O	RIS
A25	3.3VDC	PWR	NA	NA	B25	AD[22]	PCI	I/O	RIS
A26	AD[23]	PCI	I/O	RIS	B26	GND	PWR	NA	NA
A27	AD[20]	PCI	I/O	RIS	B27	AD[21]	PCI	I/O	RIS
A30	AD[17]	PCI	I/O	RIS	B30	3.3VDC	PWR	NA	NA
A31	IRDY#	PCI	I/O	RIS	B31	C/BE[2]#	PCI	I/O	RIS
A32	DEVSEL#	PCI	I/O	RIS	B32	FRAME#	PCI	uo	RIS
A33	3.3VDC	PWR	NA	NA	B33	TRDY#	PCI	I/O	RIS
A34	STOP#	PCI	I/O	RIS	B34	GND	PWR	NA	NA
A35	PERR#	PCI	I/O	RIS	B35	SDONE	PCI	I/O	RIS
A36	SERR#	PCI	I/O	RIS	B36	LOCK#	PCI	I/O	RIS
A37	GND	PWR	NA	NA	B37	SBO#	PCI	I/O	RIS
A38	C/BE[l]#	PCI	I/O	RIS	B38	3.3VDC	PWR	NA	NA
A39	AD[13]	PCII	I/O	RIS	B39	AD[15]	PCI	I/O	RIS
A40	AD[10]	PCI	I/O	RIS	B40	PAR	PCI	I/O	RIS
A41	GND	PWR	NA	NA	B41	AD[14]	PCI	I/O	RIS
A42	C/BE[0]#	PCI	I/O	RIS	B42	GND	PWR	NA	NA
A43	AD[00]	PCI	I/O	RIS	B43	AD[11]	PCI	I/O	RIS
A44	AD[06]	PCI	I/O	RIS	B44	AD[12]	PCT	I/O	RIS
A45	3.3VDC	PWR	NA	NA	B45	AD[09]	PCI	I/O	RIS
A46	AD[05]	PCI	I/O	RIS	B46	3.3VDC	PWR	NA	NA
A47	AD[01]	PCI	I/O	RIS	B47	AD[08]	PCI	I/O	RIS
A48	AD[03]	PCI	I/O	RIS	B48	AD[07]	PCI	I/O	RIS
A49	GND	PWR	NA	NA	B49	AD[04]	PCI	I/O	RIS
A50	AD[02]	PCI	I/O	RIS	B50	GND	PWR	NA	NA
A51	5VDC	PWR	NA	NA	B51	PCI_PM#	PCI	I/O	BB

Table 2. ISA Segment, Riser Interconnect Pin-out

Pin #	Signal Name	Type	I/O	Termination	Pin #	Signal Name	Type	I/O	Termination
A52	RSTDRV	ISA	O	BB	B52	5VDC	PWR	NA	NA
A53	IOCHK#	ISA	I	BB	B53	IRQ9	ISA	O	BB
A54	SD[6]	SA	I/O	BB	B54	DRQ2	ISA	I	BB
A55	SD[7]	ISA	I/O	BB	B55	SD[3]	ISA	I/O	BB
A56	SD[4]	ISA	I/O	BB	B56	0WS#	ISA	I	BB
A57	5VDC	PWR	NA	NA	B57	SD[I]	ISA	I/O	BB
A58	SD[2]	ISA	I/O	BB	B58	AEN	ISA	O	BB
A59	SD[5]	ISA	IO	BB	B59	IOCHRDY	ISA	I	BB
A60	SD[0]	ISA	I/O	BB	B60	SA[18]	ISA	I/O	BB
A61	SMEMW#	ISA	O	BB	B61	SMEMR#	ISA	O	BB
A62	SA[19]	ISA	I/O	BB	B62	SA[16]	ISA	I/O	BB
A63	low#	ISA	I/O	BB	B63	IOR#	ISA	I/O	BB
A64	SA[17]	ISA	I/O	BB	B64	DRQ3	ISA	I	BB
A65	GND	PWR	NA	NA	B65	SA[15]	ISA	I/O	BB
A66	DACK#3	ISA	O	BB	B66	GND	PWR	NA	NA
A67	SA[14]	ISA	I/O	BB	B67	SA[13]	ISA	I/O	BB
A68	DACKI#	ISA	O	BB	B68	5VDC	PWR	NA	NA
A69	DRQI	ISA	I	BB	B69	REFRESH#	ISA	I/O	BB
A70	SA[12]	ISA	I/O	BB	B70	SA[11]	ISA	I/O	BB
A71	SYSCLK	ISA	O	BB	B71	SA[10]	ISA	I/O	BB
A72	SA[9]	ISA	I/O	BB	B72	IRQ7	ISA	I	BB
A73	5VDC	PWR	NA	NA	B73	IRQ6	ISA	I	BB
A74	IRQ5	ISA	I	BB	B74	SA[8]	ISA	I/O	BB
A75	SA[7]	ISA	I/O	BB	B75	SA[6]	ISA	I/O	BB
A76	IRQ3	ISA	I	BB	B76	DACK2#	ISA	O	BB
A77	IRQ4	ISA	I	BB	B77	SA[4]	ISA	I/O	BB
A78	SA[5]	ISA	I/O	BB	B78	GND	PWR	NA	NA
A79	TC	ISA	O	BB	B79	SA[3]	ISA	I/O	BB
A80	BALE	ISA	O	BB	B80	SA[2]	ISA	I/O	BB

Table 2. ISA Segment, Riser Interconnect Pin-out (cont.)

Pin #	Signal Name	Type	I/O	Termination	Pin #	Signal Name	Type	I/O	Termination
A81	GND	PWR	NA	NA	B81	SA[l]	ISA	I/O	BB
A82	OSC	ISA	O	BB	B82	SA[0]	ISA	I/O	BB
A83	IOCS16#	ISA	I	BB	B83	SBHE#	ISA	I/O	BB
A84	MEMCS16#	ISA	I	BB	B84	LA[23]	ISA	I/O	BB
A85	IRQ11	ISA	I	BB	B85	LA[22]	ISA	I/O	BB
A86	IRQ10	ISA	I	BB	B86	LA[21]	ISA	I/O	BB
A87	IRQ15	ISA	I	BB	B87	LA[20]	ISA	I/O	BB
A88	IRQ12	ISA	I	BB	B88	LA[19]	ISA	I/O	BB
A89	GND	PWR	NA	NA	B89	LA[18]	ISA	I/O	BB
A90	IRQ14	ISA	I	BB	B90	LA[17]	ISA	I/O	BB
A91	DRQ0	ISA	I	BB	B91	DACKO#	ISA	O	BB
A92	MEMR#	ISA	I/O	BB	B92	DACK5#	ISA	O	BB
A93	MEMW#	ISA	I/O	BB	B93	SD[8]	ISA	I/O	BB
A94	SD[9]	ISA	I/O	BB	B94	DACK6#	ISA	O	BB
A95	DRQ5	ISA	I	BB	B95	SD[10]	ISA	I/O	BB
A96	DRQ6	ISA	I	BB	B96	5VDC	PWR	NA	NA
A97	5VDC	PWR	NA	NA	B97	SD[11]	ISA	I/O	BB
A98	SD[12]	ISA	I/O	BB	B98	DRQ7	ISA	I	BB
A99	DACK7#	ISA	O	BB	B99	SD[13]	ISA	I/O	BB
A100	SD[14]	ISA	I/O	BB	B100	SD[15]	ISA	I/O	BB
A101	MASTER#	ISA	I	BB	B101	GND	PWR	NA	NA

Table 3. IDE, Floppy, and Front Panel Section, Riser Interconnect Pin-out

Pin #	Signal Name	Type	I/O	Termination	Pin #	Signal Name	Type	I/O	Termination
A102	IDEA-DD8	DE	I/O	BB	B102	GND	PWR	NA	NA
A103	IDEA-RESET#	IDE	O	BB	B103	IDEA_DD7	IDE	I/O	BB
A104	IDEA-DD9	IDE	I/O	BB	B104	IDEA-DD6	IDE	I/O	BB
A105	5VDC	PWR	NA	NA	B105	IDEA-DD5	IDE	I/O	BB
A106	IDEA DD4	IDE	I/O	BB	B106	IDEA-DD 11	IDE	I/O	BB
A107	IDEA-DD10	IDE	I/O	BB	B107	IDEA-DD12	IDE	I/O	BB
A108	IDEA-DD3	IDE	I/O	BB	B108	GND	PWR	NA	NA
A109	IDEA-DD13	IDE	I/O	BB	B109	IDEA-DD14	IDE	I/O	BB
A110	IDEA-DD1	IDE	I/O	BB	B110	IDEA DD2	IDE	I/O	BB
A111	GND	PWR	NA	NA	B111	IDEA DD0	IDE	I/O	BB
A112	IDEA-DIOW#	IDE	O	BB	B112	IDEA-DD15	IDE	I/O	BB
A113	IDEA-DMARQ	IDE	I	BB	B113	IDEA-DIOR#	IDE	I/O	BB
A114	IDEA-IORDY	IDE	I	BB	B114	IDEA-CSEL	IDE	I/O	BB
Al 15	IDEA-DMACK#	IDE	O	BB	B115	IDEA INTRQ	IDE	I/O	BB
A116	RESERVED	RES	NA	NA	B116	5VDC	PWR	NA	NA
Al 17	IDEA-DA2	IDE	O	BB	B117	IDEA-DA1	IDE	I/O	BB
A118	IDEA-CS0#	IDE	O	BB	B118	IDEA DA0	IDE	I/O	BB
A119	5VDC	PWR	NA	NA	B119	IDEA-CS1#	IDE	I/O	BB
A120	IDEA DASP#	IDE	RIS	B120	IDEB-DD8		IDE	I/O	BB
A121	IDEB-RESET#	IDE	O	BB	B121	IDEB-DD7	IDE	I/O	BB
A122	IDEB-DD9	IDE	I/O	BB	B122	GND	PWR	NA	NA
A123	IDEB-DD6	IDE	I/O	BB	B123	IDEB-DDIO	IDE	I/O	BB
A124	IDEB DD5	IDE	I/O	BB	B124	5VDC	PWR	NA	NA
A125	IDEB DD11	IDE	I/O	BB	B125	IDEB-DD4	IDE	I/O	BB
A126	IDEB DD12	IDE	I/O	BB	B126	IDEB-DD3	IDE	I/O	BB
A127	GND	PWR	NA	NA	B127	IDEB-DD13	IDE	I/O	BB
A128	IDEB-DD2	IDE	I/O	BB	B128	IDEB-DD14	IDE	I/O	BB
A129	IDEB-DD15	IDE	I/O	BB	B129	IDEB-DDI	IDE	I/O	BB
A130	IDEB DIOW#	IDE	I/O	BB	B]30	IDEB-DDO	IDE	I/O	BB
A131	IDEB-DMARQ	IDE	I	BB	B131	IDEB-DIOR#	IDE	I/O	BB
A132	IDEB-IORDY	IDE	I	BB	B132	IDEB-CSEL	IDE	O	BB
A133	GND	PWR	NA	NA	B133	IDEB-INTRQ	IDE	I	BB
A134	IDEB-DMACK#	IDE	O	BB	B134	IDEB-DAI	IDE	O	BB
A135	RESERVED	RES	NA	NA	B135	IDEB-DA2	IDE	O	BB

Table 3. IDE, Floppy, and Front Panel Section, Riser Interconnect Pin-out (cont.)

Pin #	Signal Name	Type	I/O	Termination	Pin #	Signal Name	Type	I/O	Termination
A136	IDEB DA0	IDE	O	BB	B]36	IDEB CSI#	IDE	O	BB
A137	IDEB CS0#	IDE	O	BB	B137	IDEB-DASP#	IDE	I	RIS
A138	DRV2#	FLOPPY	GND	NA	B138	GND	PWR	NA	NA
A139	5VDC	PWR	A	NA	B139	DRAT'E0	FLOPPY	O	NA
A140	RESERVED	RES	NA	NA	B140	FDS1#	FLOPPY	O	NA
A141	DENSEL	FLOPPY	0	NA	B 141	FDSO#	FLOPPY	O	NA
A142	FDMEO#	FLOPPY	O	NA	B 142	DIR#	FLOPPY	O	NA
A143	INDX#	FLOPPY	I	RIS	B 143	MSENI	FLOPPY	I	NA
A144	FDMEI#	FLOPPY	O	NA	B 144	GND	PWR	NA	NA
A145	GND	PWR	NA	NA	B 145	WRDATA#	FLOPPY	O	NA
A146	WE#	FLOPPY	O	NA	B 146	TRKO#	FLOPPY	I	RIS
A147	STEP#	FLOPPY	O	NA	B 147	MSENO	FLOPPY	I	NA
A148	WP#	FLOPPY	I	RIS	B 148	RDDATA#	FLOPPY	I	RIS
A149	HDSEL#	FLOPPY	O	NA	B149	DSKCHG#	FLOPPY	I	RIS
A150	SDA	MISC	I/O	BB	B150	GND	PWR	NA	NA
A151	SCL	MISC	O	BB	B 151	IRSL0	MISC	I/O	NA
A152	FAN-TACHI	MISC	I	NA	B152	IRSL1	MISC	I/O	NA
A153	FAN-TACH2	MISC	I	NA	B153	IRSL2	MISC	I/O	NA
A154	FAN-TACH3	MISC	I	NA	B154	IRTX	MISC	I/O	NA
A155	FAN-CTL	MISC	I	NA	B155	IRRX	MISC	I/O	NA
A156	5VDC	PWR	NA	NA	B156	FP-SLEEP-	MISC	I	BB
A157	USB 1/3-N	MISC	I/O	RIS	B157	FP-RST#	MISC	I	BB
A158	USBI/3-P	MISC	I/O	RIS	B158	GND	PWR	NA	NA
A159	USBI/3-OC#	MISC	I	RIS	B159	PWRLED#	MISC	O	RIS
A160	USB2/4-N	MISC	I/O	RIS	B160	PWOK	PWR	I	NA
A161	USB2/4 P	MISC	I/O	RIS	B 161	SOFT-ON/OFF#	PWR	I	BB
A162	USB2/4-OC#	MISC	I	RIS	B162	PS-ON#	PWR	O	NA
A163	GND	PWR	NA	NA	B163	LAN-WAKE	MISC	I	BB
A164	VBAT	MISC	O	RIS	B164	LAN-ACTVY-LED#	MISC	O	NA
A165	TAMP-DET#	MISC	I	BB	B165	MDM WAKE#	MIS	I	BB
A166	MSG WAIT LED#	MISC	O	RIS	B166	1394-PWR	PWR	I	NA
A167	1394-GND	PWR	O	NA	B167	RESERVED	RES	NA	NA
A168	RESERVED	RES	NA	NA	B168	RESERVED	RES	NA	NA
A169	5VSB	PWR	I	NA	B169	RESERVED	RES	NA	NA
A170	3.3VSENSE	PWR	O	NA	B170	-5V	PWR	NA	NA

I/O Column Definitions Relative to Motherboard

O = Output from motherboard to riser

I = Input from riser to motherboard

Termination Column Definitions:

BB = Termination/Pullup/Pulldown/debounce is on the Baseboard

RIS = Termination/Pullup/Pulldown is on Riser card

NA = Not on Baseboard or Riser

1.14.1.2 ISA Bus Implementation

The 82371SB (PIIX3), PCI to ISA bus bridge, provides a fully ISA compatible master and slave interface capable of driving five ISA slots without external data buffers. External buffers are used on the ISA signals SA[19:8] and SBHE# to permit them to be used with the IDE interface. The ISA interface also provides byte swapping logic, I/O recovery support, wait state generation and SYSCLK. SYSCLK is a 8.33MHz clock.

The keyboard controller, real-time-clock, and BIOS flash are on a buffered version of the ISA bus called the XD bus. The XD bus prevents these devices from loading the ISA bus.

The SMC FDC37C665IR Super I/O device also resides on the ISA bus with each feature accessed via standard PC compatible locations. Provided is a standard floppy port, both standard COM1/COM2 ports, and a standard parallel port. The SMC FDC37C665IR Super I/O IDE interface is not used.

1.14.1.3 PCI Bus Implementation

The Base-G PCI bus is a 5 volt, 33MHz bus. The Base-G supports up to two PCI slots on a NLX Riser without a PCI-to-PCI bridge. Two REQ/GNT pairs for two PCI slots are routed to the NLX connector. The other three possible REQ/GNT pairs are not driven.

A requirement of the PCI bus is the length of the PCI clock lines have no more than 2nS of skew. The Base-G board assumes the maximum clock length on the riser card is 4 inches, with the clock lengths extended to match these lengths to all on board peripherals. . Only the clocks for the first two PCI slots are implemented.

All pull-up resistors required for the PCI control signals must be implemented on the Riser Board. Only the reverse terminated lines for clocks have series resistors located on the baseboard.

1.14.2 Keyboard/Mouse Connectors

Pin	Signal
1	DATA
2	UNUSED
3	GND
4	+5V
5	CLOCK
6	UNUSED

1.14.3 Serial (COM1/COM2) Port Connectors

Pin	Signal
1	DATA CARRIER DETECT (IN) (CD)
2	RECEIVE DATA (IN) (RXD)
3	TRANSMIT DATA (OUT) (TXD)
4	DATA TERMINAL READY (OUT) (DTR)
5	SIGNAL GROUND
6	DATA SET READY (IN) (DSR)
7	REQUEST TO SEND (OUT) (RTS)
8	CLEAR TO SEND (IN) (CTS)
9	RING INDICATOR (IN) (RI)

1.14.4 Parallel Port Connector

Pin	Signal	Pin	Signal
1	~STROBE	14	~AF AUTO FEED
2	D0	15	~ERR
3	D1	16	~INIT
4	D2	17	~SELIN
5	D3	18	SIGNAL GND
6	D4	19	SIGNAL GND
7	D5	20	SIGNAL GND
8	D6	21	SIGNAL GND
9	D7	22	SIGNAL GND
10	~ACK	23	SIGNAL GND
11	BUSY	24	PNF
12	PE (PAPER END)	25	SIGNAL GND
13	SELECT		

1.14.5 Optional SVGA Video Connector

Pin	Signal Name	Pin	Signal Name
1	RED	9	N/C
2	GREEN	10	GND
3	BLUE	11	N/C
4	N/C[1]	12	MID1 (DDC)
5	GND	13	H SYNC
6	ANALOG GND	14	V SYNC
7	ANALOG GND	15	MID3 (DDC)
8	ANALOG GND		

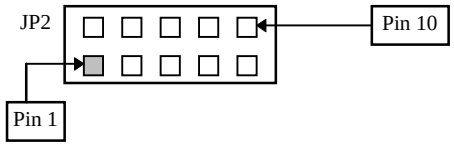
1.14.6 Ethernet RJ45 Connectors

Pin	Description
1	TRANSMIT +
2	TRANSMIT -
3	RECEIVE +
4	NC
5	NC
6	RECEIVE -
7	NC
8	NC

1.15 Jumper Settings

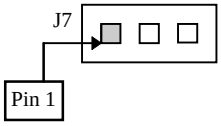
As shipped from the factory , the few jumpers on the Base-G simply provide the correct clock frequency and core voltage levels to Pentium microprocessor. Jumper block JP2 allows a user force the BIOS into a recovery mode or re-flash the BIOS.

1.15.1 Jumper Block JP2



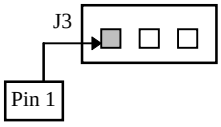
Pin	Description
2-4	CPU Reset
7-8	FORCE RECOVERY
3-10	BOOT BLOCK UPDATE

1.15.2 Jumper Block J7, RESET



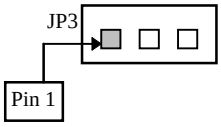
Pin	Description
1-2	VRT reset voltage level
2-3	MMX Reset voltage level

1.15.3 Jumper Block J3, PROC VOLTAGE



Pin	Description
1-2	MMX 2.8V core voltage
2-3	VRT 3.1V core voltage

1.15.4 Jumper Block JP3, Power Soft On/Off Feature



Pin	Description
1-2	Power Soft On Enabled
2-3	Power Soft On Disabled

2.0 Baseboard Resources

2.1 Memory Map

Range	CPU address	Region	Cached
0 to 640K	00000000-0009FFFF	DRAM (640KB)	YES
640K to 768K	000A0000-000BFFFF	SVGA MEMORY	NO
768K to 800K	000C0000-000CBFFF	SHADOWED SVGA BIOS	YES
800K to 912K	000CC000-000DFFFF	EMBEDDED BIOS EXTENSION. IF NO EXTENSION, ISA (ALIASED)	YES NO
912K to 1M	000E0000-000FFFFF	SHADOWED SYSTEM BIOS	YES
1M to 16M	00100000-0FFFFFF	DRAM UP TO 16BB. IF NO DRAM FORWARDED TO ISA	YES NO
16M to (4.0G-512K)	08000000-FFF7FFFF	DRAM (UP TO 512M) IF NO DRAM, PCI BUS PRODUCES A "MASTER ABORT"	YES
Top 512K	FFF80000-FFFFFFFF	FLASH BOOT DEVICE	NO

2.2 I/O Map

The following registers are accessible in the I/O space. Note that only the A9-A0 address bits are decoded for the I/O registers that are addressed between 0x200-0x3FF, resulting in the standard AT bus I/O address aliasing.

Port Address	Functional group	R/W	Usage	Access from
0000	DMA Controller 1	R/W	DMA 1 Channel 0 address	PCI
0001		R/W	DMA 1 Channel 0 count	PCI
0002		R/W	DMA 1 Channel 1 address	PCI
0003		R/W	DMA 1 Channel 1 count	PCI
0004		R/W	DMA 1 Channel 2 address	PCI
0005		R/W	DMA 1 Channel 2 count	PCI
0006		R/W	DMA 1 Channel 3 address	PCI
0007		R/W	DMA 1 Channel 3 count	PCI
0008		R W	DMA 1 Command DMA 1 Status	PCI PCI
0009		W	DMA 1 Write Request	PCI
000A		W	DMA 1 Single Mask Bit	PCI
000B		W	DMA 1 Write Mode	PCI
000C		W	DMA 1 Clear byte pointer	PCI
000D		W	DMA 1 Master clear	PCI
000E		W	DMA 1 Clear Mask	PCI
000F		R/W	DMA 1 Read/write all mask register bits	PCI
0020	Interrupt Controller 1	R/W	INT 1 Control	PCI
0021		R/W	INT 1 Mask	PCI

Port Address	Functional group	R/W	Usage	Access from
0040	Timer/Counter	R/W	Counter 0 Count	PCI
0041		R/W	Counter 1 Count	PCI
0042		R/W	Counter 2 Count	PCI
0043		W	Command Mode	PCI
0060	Keyboard Controller	R/W R	Data I/O register Reset XBus IRQ12/M and IRQ1	PCI/ISA PCI/ISA
0061	NMI Status and Control	R W	NMI Status NMI Control	PCI PCI
0	Keyboard Con064troller	R W	Status Register Command Register	PCI/ISA PCI/ISA
0070	Real-time clock, NMI	W	RTC Index Register = bits 6-0 NMI Enable = bit 7	PCI/ISA
0071		R/W	RTC Data Register	PCI/ISA
			0	seconds
			1	seconds alarm
			2	minutes
			3	minutes alarm
			4	hours
			5	hours alarm
			6	day of week
			7	date of month
			8	month
			9	year
			A	status A
			B	status B
			C	status C
			D	status D
			E ... 3F	NVRAM
0080	DMA	R/W	DMA Page (reserved)	PCI
0081		R/W	DMA Channel 2 page register	PCI
0082		R/W	DMA Channel 3 page register	PCI
0083		R/W	DMA Channel 1 page register	PCI
0084		R/W	DMA Page (reserved)	PCI
0085		R/W	DMA Page (reserved)	PCI
0086		R/W	DMA Page (reserved)	PCI
0087		R/W	DMA Channel 0 page register	PCI
0089		R/W	DMA Channel 6 page register	PCI
008A		R/W	DMA Channel 7 page register	PCI
008B		R/W	DMA Channel 5 page register	PCI
008C		R/W	DMA Page (reserved)	PCI
008D		R/W	DMA Page (reserved)	PCI
008E		R/W	DMA Page (reserved)	PCI
008F		R/W	DMA Low Page Register Refresh	PCI
0094	SVGA Controller	R/W	POS102 Access Control	PCI
00A0	Interrupt Controller 2	R/W	INT 2 Control	PCI
00A1		R/W	INT 2 Mask	PCI
00B2	Power Management	R/W	Control	PCI
00B3		R/W	Status	PCI

Port Address	Functional group	R/W	Usage	Access from
00C0	DMA Controller 2	R/W	DMA 2 Channel 4 address	PCI
00C2		R/W	DMA 2 Channel 4 count	PCI
00C4		R/W	DMA 2 Channel 5 address	PCI
00C6		R/W	DMA 2 Channel 5 count	PCI
00C8		R/W	DMA 2 Channel 6 address	PCI
00CA		R/W	DMA 2 Channel 6 count	PCI
00CC		R/W	DMA 2 Channel 7 address	PCI
00CE		R/W	DMA 2 Channel 7 count	PCI
00D0		R W	DMA 2 Status DMA 2 Command	PCI
00D2		W	DMA 2 Write Request	PCI
00D4		W	DMA 2 Write Single Mask Bit	PCI
00D6		W	DMA 2 Write Mode	PCI
00D8		W	DMA 2 Clear Byte Pointer	PCI
00DA		W	DMA 2 Master Clear	PCI
00DC		W	DMA 2 Clear Mask	PCI
00DE		R/W	DMA 2 Read/Write all register mask bits	PCI
00F0	Coprocessor	W	Coprocessor Error	PCI
0102	SVGA Controller	R/W	POS102 Register	PCI
02F8	COM2 Serial Port	R W	Receiver buffer Transmitter buffer	PCI/ISA
		R/W	Baud rate divisor latch (LSB)	PCI/ISA
02F9		R/W	Interrupt enable register	PCI/ISA
		R/W	Baud rate divisor latch (MSB)	PCI/ISA
02FA		R W	Interrupt ID register FIFO Control register	PCI/ISA
02FB		R/W	Line control register	PCI/ISA
02FC		R/W	Modem control register	PCI/ISA
02FD		R	Line status register	PCI/ISA
02FE		R/W	Modem status register	PCI/ISA
0378	LPT1 Parallel Port	R/W	Data register	PCI/ISA
0379		R	Status register	PCI/ISA
037A		R/W	Control register	PCI/ISA
0398	SuperI/O	R/W	Index Register	PCI/ISA
0399	Configuration	R/W	Data Register	PCI/ISA
03B4	SVGA Controller	R/W	CRT Controller index (mono)	PCI
03B5		R/W	CRT Controller data (mono)	PCI
03BA		R W	Input Status Register 1 (mono) Feature control output (mono)	PCI
03C0		W	Attribute controller Index/Data	PCI
03C1		R	Attribute controller Index/Data	PCI
03C2		R W	Input Status Register 0 Miscellaneous output	PCI
03C3		R/W	Motherboard Sleep	PCI
03C4		R/W	Sequencer Index	PCI
03C5		R/W	Sequencer Data	PCI
03C6		R/W R/W	Video DAC pixel mask Hidden DAC register	PCI PCI

Port Address	Functional group	R/W	Usage	Access from
03C7		R W	DAC State Pixel address read mode	PCI
03C8		R/W	Pixel mask write mode	PCI
03C9		R/W	Pixel data	PCI
03CA		R	Feature control readback	PCI
03CC		R	Miscellaneous output readback	PCI
03CE		R/W	Graphics controller index	PCI
03CF		R/W	Graphics controller data	PCI
03D4		R/W	CRT controller index (color)	PCI
03D5		R/W	CRT controller data (color)	PCI
03DA		R W	Input Status Register 1 (color) Feature Control (color)	PCI
03F0	Floppy Disk Controller	R	Status Register A	PCI/ISA
03F1		R	Status Register B	PCI/ISA
03F2		R/W	Digital Output Register	PCI/ISA
03F3		R/W	Tape Driver Register	PCI/ISA
03F4		R W	Main Status Register Data Rate Select Register	PCI/ISA
03F5		R/W	Data Register	PCI/ISA
03F6			Reserved	
03F7		R W	Digital Input Register Configuration Control Register	PCI/ISA
03F8	COM1 Serial Port	R W	Receiver buffer Transmitter buffer	PCI/ISA
		R/W	Baud rate divisor latch (LSB)	PCI/ISA
03F9		R/W	Interrupt enable register	PCI/ISA
		R/W	Baud rate divisor latch (MSB)	PCI/ISA
03FA		R W	Interrupt ID register FIFO Control register	PCI/ISA
03FB		R/W	Line control register	PCI/ISA
03FC		R/W	Modem control register	PCI/ISA
03FD		R	Line status register	PCI/ISA
03FE		R/W	Modem status register	PCI/ISA
0550	Register	R/W	Auxiliary GP Output Control	ISA
0552	Register	R/W	HW revision serial PROM control	ISA
0CF8 - 0CFB (Dword only)	PCI Configuration	R/W	Configuration Address Register	PCI
0CFC - 0CFF		R/W	Configuration Data Register	PCI
46E8	SVGA Controller	R/W	Adapter sleep	PCI
8150-815F	Watchdog Timer	R/W	Setting Watchdog timer	ISA

2.3 Interrupt Assignment

Interrupt	Usage
IRQ0	Timer
IRQ1	Keyboard controller
IRQ2	Cascade interrupt input
IRQ3	COM2, COM1 or unassigned
IRQ4	COM1, COM2 or unassigned
IRQ5	Unassigned
IRQ6	Floppy Disk or unassigned
IRQ7	LPT1 or unassigned
IRQ8	Real time clock
IRQ9	Unassigned or watchdog timer
IRQ10	Unassigned
IRQ11	Unassigned
IRQ12	Mouse
IRQ13	Numeric Coprocessor
IRQ14	Primary EIDE
IRQ15	Secondary EIDE or unassigned
NMI	ISA bus IOCCHK/Memory Parity
SMI	Power Management/ECC

2.4 PCI Device Assignments

Peripheral	IDSEL#	Device #	Function #	Arbitration Signals REQ#/GNT#
HOST-PCI BRIDGE (82439HX)	AD11	0	0	NA
ETHERNET 1 (DEC 21134)	AD12	1	0	0
ETHERNET 2 OPTION (DEC 21134)	AD13	2	0	1
PMC VIDEO (CIRRUS LOGIC GD5446)	AD14	3	0	1
PIIX3 PCI/ISA BUS BRIDGE (82371SB) PCI/ISA BRIDGE IDE INTERFACE USB	AD18	7	 0 1 2	NA

2.5 PCI Interrupt Routing & Assignment

The PCI specification allows PCI devices to share PCI bus interrupts. The sharing of PCI interrupts can result in a small amount of latency that typically does not affect device operation. Maximum performance can be achieved by dedicating a PCI interrupt to a specific IRQ.

PCI interrupts are categorized in the following groups:

INTA: Add-in cards requiring only one interrupt. For cards that require more than one interrupt, INTA is assigned to the first interrupt.

INTB: Generally (though not an absolute requirement) used as the second interrupt on add-in cards.

INTC & INTD: Generally used as the third and fourth interrupt respectfully on add-in cards.

The PIIX3 has four programmable Interrupt Request (PIRQ) PCI interrupt input signals. Any PCI interrupt source, either an on-board device or an add-in card, connects to on of these PIRQ signals. Some PCI interrupt sources are mechanically tied together, sharing the same PCI interrupt.

PIIX3 PIRQ Signal	Signal Assignment
PIRQA	PMC VIDEO , OPTIONAL ETHERNET 2
PIRQB	ETHERNET 1
PIRQC	
PIRQD	OPTIONAL USB

Note: The Base-G optional PMCM64A video with the ATI 3D Rage II+ does not require the use of a PCI interrupt and does not conflict with the second ethernet option

3.0 BIOS Set-up Screens

The System BIOS setup screens and options are the standard Phoenix NuBIOS 4.05 (with Plug and Play and PCI support) screens with RadiSys extensions. A legend at the bottom of each screen provides information for the user to manipulate setup options. Depressing the "F2" just after POST has completed provides access to the BIOS set-up screens

The System BIOS contains a setup engine to display and alter the system configuration. This information is maintained in nonvolatile CMOS RAM and is used by the System BIOS to initialize the hardware.

The up and down cursor (arrow) keys to move from field to field while the right and left arrows move from menu to menu, as noted in the menu bar at the top of the screen. If the arrow keys are used to leave a menu and then return, the active field is always at the beginning of the menu. Fields with a triangle to the left are sub-menu headings; pressing Enter when the cursor rests on one of these headings reaches that sub-menu. For most fields, positioning the cursor at the field and from the numeric keypad, pressing the + and - keys rotates through the available choices. Once the entry has been changed to appear as desired, using the up and down arrow moves to the next field.

3.1 Main Setup Menu

The Main Setup Menu is shown below:

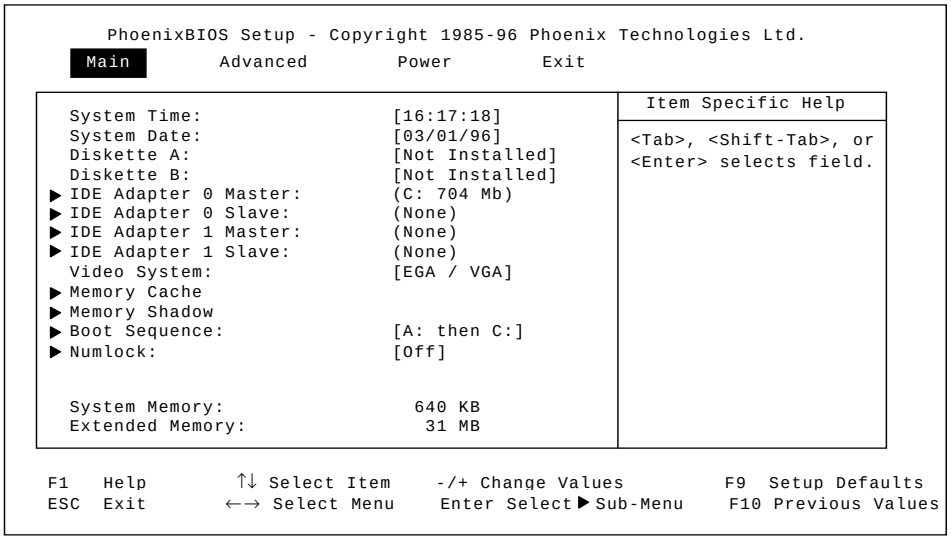


Figure 3. Main BIOS Setup Menu

The fields in each menu and sub-menu are explained below. Additional help information is available in the help area on the Setup screen.

System Time:/System Date:

These values are changed by moving to each field and typing in the desired entry. The TAB key moves from hours to minutes to seconds, or from months to days to years.

Diskette A:/Diskette B:

This field identifies the type of floppy disk drive installed as the A:/B: drive. Possible settings are "Not Installed", "360 KB, 5¼"", "720 KB, 3½"", "1.2 MB, 5¼"", "1.44 MB, 3½"", and "2.88 MB, 3½"". The BIOS defaults to "Not Installed" for drive A: and B:.

IDE Adapter 0 Master/Slave: Sub-menus

These fields are headings for menus that allow entering complete disk drive information. Once the information is entered for the drive, the entry in the Main Menu shows the drive selected..

Video System:

This field is used to select the video type. The selections are: “EGA/VGA”, “CGA 80x25”, and “Monochrome”. The default is “EGA/VGA”.

Memory Cache Sub-menu

Used have the BIOS executed The term “Memory Cache” refers to the technique of caching BIOS images.

Memory Shadow Sub-menu

The term “Memory Shadow” refers to the technique of copying information from an extension ROM into DRAM and accessing it in this alternate memory location.

Boot Sequence Sub-menu

The Boot Sequence Sub-menu allows changing the boot delay, boot sequence, or disable several displays during the boot process, such as the SETUP prompt, POST errors, floppy drive check, and summary screen. Once the boot sequence has been set, it displays in this entry in the Main menu.

Keyboard Features (Numlock) Sub-menu

This menu enables or disables various keyboard features, including enabling the Numlock key, enabling the key click, and setting the keyboard auto-repeat rate and delay. The Numlock setting displays for this entry in the Main Menu.

System Memory

This field cannot be edited and displays the amount of conventional memory (below 1MB).

Extended Memory

This field cannot be edited and displays the amount of extended memory (above 1MB).

3.2 IDE Adapter Sub-menu

There are a total of four IDE adapter sub-menus for the primary and secondary hard disk controllers and the master and slave drives. The detailed characteristics of the drive connected to the adapter is available in the IDE Adapter 0 and Adapter 1 sub-menus, which display the following screen:

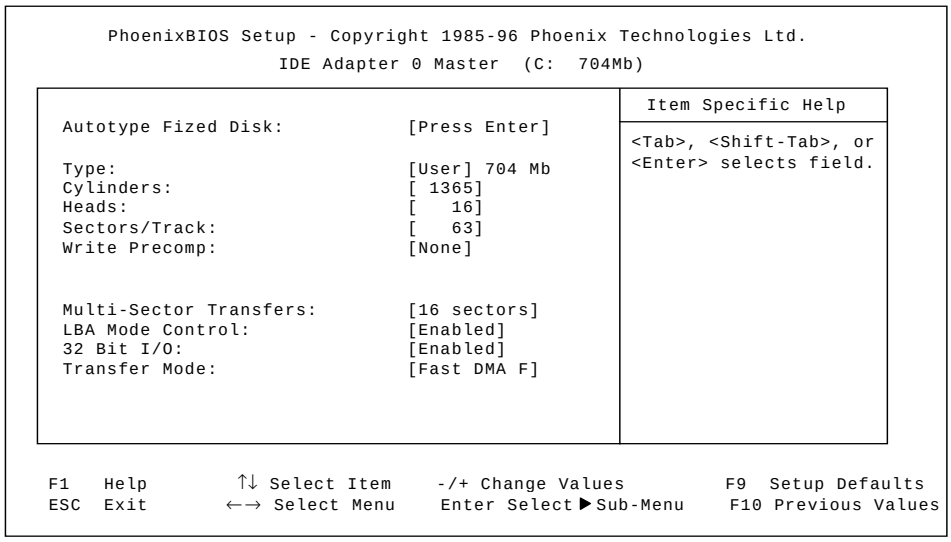


Figure 4. Fixed Disk Sub-Menu

Autotype Fixed Disk

This option is used to set up new disks and allows Setup to determine the proper settings of the disk based on information from the disk, detected for drives that comply with ANSI specifications. The ENTER key invokes this function.

Existing (formatted) disks must be set up using the same parameters that were used originally when the disk was formatted. The specific cylinder, head, sector information as listed on the label attached to the drive at the factory must be manually entered on this screen using a "User" type described below.

Type

"None" is selected if there is no IDE hard disk drive for this adapter. If the "Autotype" feature cannot be employed, the "User" type must be selected with the correct drive values for cylinders, heads, sectors/track, and write precompensation entered. Selecting "Auto" for this option causes the System BIOS to automatically autotype the hard disk every time POST is executed. The default is "None".

Multi-Sector Transfers

This option allows the user to configure the System BIOS to read ahead by the specified number of sectors whenever a disk access is performed. This has the effect of reading more data at once to reduce the absolute number of discrete disk reads performed by the operating system, which may increase system performance. The possible selections are "Disabled", "2 sectors", "4 sectors", "8 sectors", or "16 sectors" . The default is "Disabled".

LBA Mode Control

When enabled, this option allows the System BIOS to reference hard disk data as logical blocks instead of using the traditional Cylinders/Heads/Sectors (CHS) method. This option can only be used if both the hard disk being configured and the operating system supports Logical Block Addressing (LBA). If disabled, CHS mode is used. Autotyping may change this value if the hard disk reports it supports LBA. The default is “Disabled”.

32-bit I/O

This option allows the System BIOS to access the hard disk controller with 32-bit I/O accesses, increasing system performance. This selection is not affected by autotyping. If the PCI IDE controller in the T2 chip-set is being used, then this option should be set to “Enabled” to maximize system performance. The default is “Enabled”.

Transfer Mode

This option selects the mode that the System BIOS uses to access the hard disk. The selections are:

Standard (default)
Fast PIO 1
Fast PIO 2
Fast PIO 3
Fast PIO 4
Fast DMA A
Fast DMA B
Fast DMA F

Older hard disks only support “Standard”. Newer hard disks adhering to “Fast ATA” or “Enhanced IDE” specifications may support the fast programmed I/O or DMA modes. Autotyping may change this value depending on the transfer modes that the hard disk reports it supports. The fast DMA modes take full advantage of the onboard bus mastering hard disk controller and should yield the highest performance when used in conjunction with operating systems that support it. The default is “Standard”.

3.3 Boot Sequence Sub-menu

The Boot Sequence Sub-menu allows changing the boot sequence options. The following is displayed:

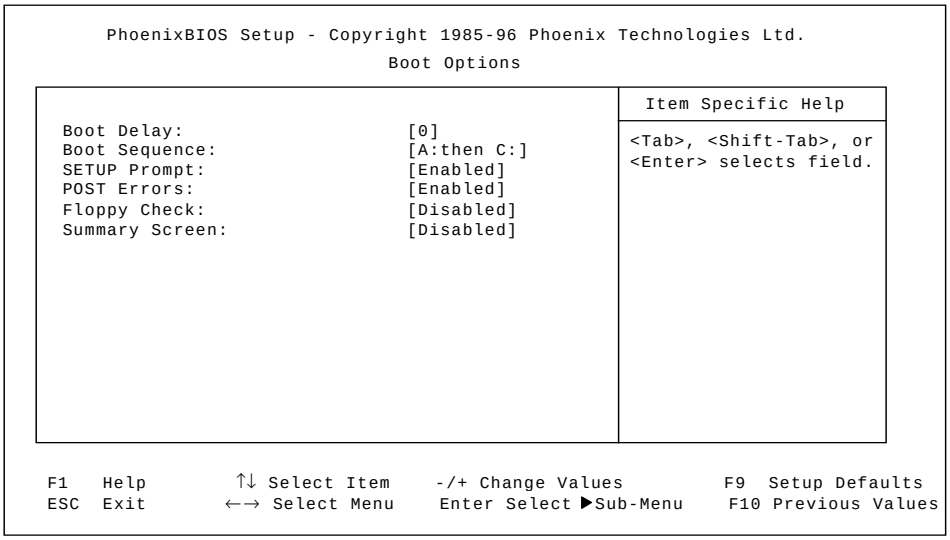


Figure 5. Boot Options Menu

Boot Delay:

This option sets the system to delay booting for a time period in seconds. This allows for long start up times on boot devices that spin up slowly and ranges from 0 through 255 seconds. The default is “0” seconds.

Boot Sequence:

This option defines how the system treats floppy drive A: when booting. Booting can occur from a floppy in the A: drive or directly from the fixed disk drive. The options are as follows:

1. A: then C: Used to boot from the floppy drive, or if no floppy disk is present in the A: drive, boot from the C: drive.
2. C: then A: Used to boot from the C: drive, or if none is present, boot from the A: drive.
3. C: only: Used to boot from the C: drive without searching for an A: drive.

The default is “A: then C:”

Setup Prompt:

This option enables or disables the message “Press F2 to enter Setup.” Even if the message is disabled, the F2 key can still be pressed to enter the Setup Menu. The default is “Enabled”.

POST Errors:

This option is used to stop the boot process if the POST encounters errors. Otherwise, the system continues to attempt to boot despite any startup error messages displayed. The default is “Enabled”.

Floppy Check:

This option enables or disables the floppy drive search during the boot. It is possible to boot from the A: drive with the floppy check disabled. The default is “Disabled”.

Summary Screen:

This option enables or disables a summary of the system configuration, displayed before the operating system starts to load. The default is “Disabled”.

3.4 Keyboard Features Menu

Use this sub-menu to enable or disable various keyboard features.

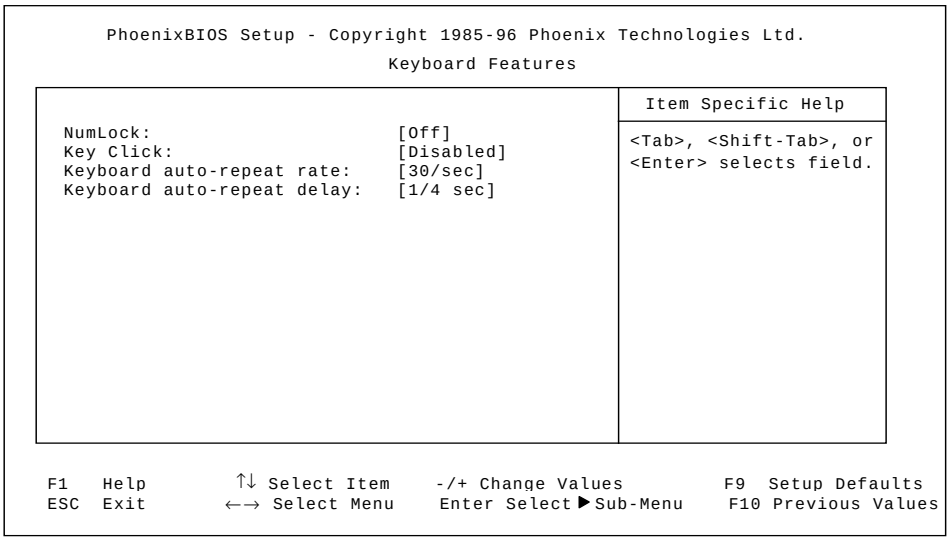


Figure 6. Keyboard Menu

Numlock

This option enables or disables the Numlock feature of the keyboard on booting. This enables the use of the keypad numbers. The default is “Off”, which automatically disengages the Numlock key at boot time.

Key Click:

This option enables or disables the key click feature on the keyboard. If enabled, the system produces an audible click each time a key is pressed. The default is “Disabled”.

Keyboard auto-repeat rate:

This option sets the auto-repeat rate if holding a key down on the keyboard. The rates can be set to one of: “2/sec”, “6/sec”, “10/sec”, “13.3/sec”, “18.5/sec”, “21.8/sec”, 26.7/sec”, and “30/sec”. The default rate is “30/sec”.

Keyboard auto-repeat delay:

This sets the delay between when a key is pressed and when the auto-repeat feature begins. Options are “1/4 sec”, “1/2 sec”, “3/4 sec”, and “1 sec” . The default delay is “1/4 sec”.

3.5 Advanced Menu

The Advanced Menu contains settings for integrated peripherals, memory shadow, cache, and large disk access mode.

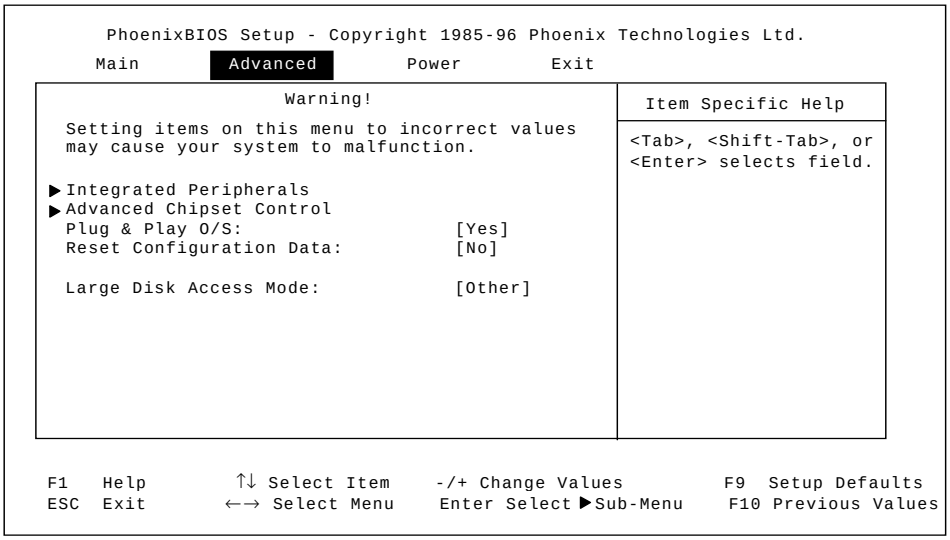


Figure 7. Advanced Menu

Integrated Peripherals Sub-menu

This option selects the Integrated Peripherals sub-menu to configure the onboard I/O ports, IDE controller, and Ethernet controller.

Advanced Chip-set Control Sub-menu

This option selects the Advanced Chip-set Control sub-menu to configure the PCI chip-set.

Plug & Play OS

If enabled, this option informs the System BIOS that the booted operating system supports Plug and Play. This forces the Plug and Play portion of the System BIOS to only configure motherboard devices and those peripherals necessary for booting (display, hard disk, etc). The default is “Yes”.

Reset Configuration Data

If enabled, this option clears the Extended System Configuration Data (ESCD) block residing in the BIOS flash. This is necessary the first time a board/system is powered or if the ESCD becomes corrupted. The default is “No”. This option is automatically reset to “No” after the ESCD is cleared.

Large Disk Access Mode:

If a hard disk larger than 528MB is used, this selection should be set to “DOS” if running MS-DOS, or set to “Other” if using a different operating system. When set to “DOS”, this selection causes the System BIOS to perform cylinder/head translation if the drive is configured in Setup to have more than 1024 cylinders. This allows MS-DOS systems to use hard disks up to 8GB (1024C x 255H x 63S) in size without special drivers. The default is “Other”.

3.6 Integrated Peripherals Sub-menu

The options in this sub-menu configure the onboard serial ports, parallel port and disk controllers.

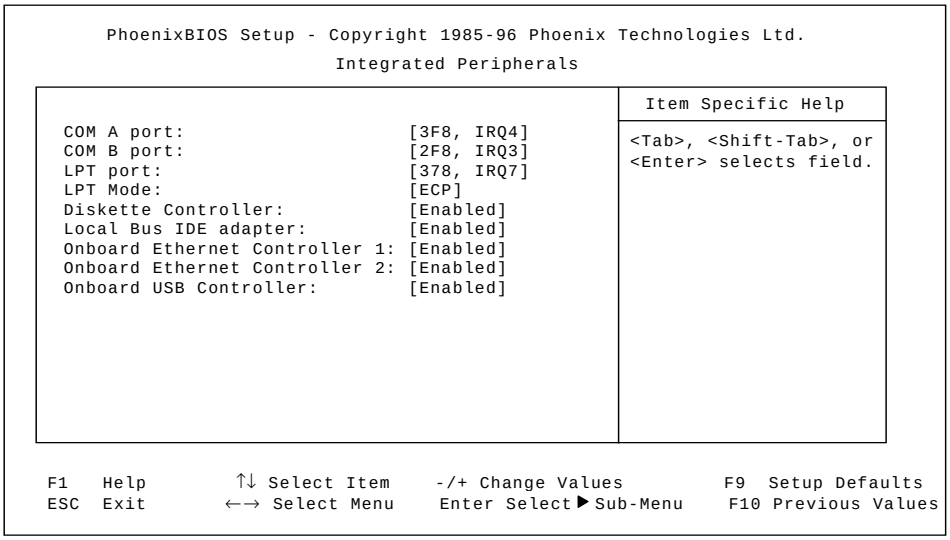


Figure 8. Integrated Peripherals Menu

COM 1 Port

This option configures the COM 1 serial port. The choices for I/O base addresses and IRQs are: "Disabled", "3F8, IRQ4", "2F8, IRQ3", "3E8, IRQ4", "2E8, IRQ3", and "Auto". "Auto" causes the System BIOS to choose a base address and IRQ setting that avoids conflicting with the other ports. The default I/O base and IRQ for this COM port are "3F8, IRQ4".

COM 2 Port

This option configures the COM 2 serial port. The choices for I/O base addresses and IRQs are: "Disabled", "3F8, IRQ4", "2F8, IRQ3", "3E8, IRQ4", "2E8, IRQ3", and "Auto". "Auto" causes the System BIOS to choose a base address and IRQ setting that avoids conflicting with the other ports. The default I/O base and IRQ for this COM port are "2F8, IRQ3".

LPT Port

This option configures the LPT1 parallel port. The choices for I/O base addresses and IRQs are: "Disabled", "378, IRQ7", "278, IRQ7", and "Auto". "Auto" causes the System BIOS to choose a base address and IRQ setting that avoids conflicting with the other ports. The default I/O base and IRQ for this LPT port are "378, IRQ7".

LPT Mode

This option sets the mode under which the LPT port operates. The selections are:

Output only
Bi-directional
ECP (the default)

Diskette Controller

This option enables or disables the onboard floppy disk controller. The default is "Enabled".

Local Bus IDE adapter

This option enables or disables the onboard PCIbus IDE hard disk controller. This option must be set to “Disabled” if a PCI add-in card hard disk controller is installed in the system. The default is “Enabled”.

Onboard Ethernet Controller 1

This option enables or disables the standard onboard PCIbus Ethernet controller. The default is “Enabled”.

Onboard Ethernet Controller 2

This option enables or disables the optional onboard PCIbus Ethernet controller. The default is “Enabled”.

Onboard USB controller

This option enables or disables the onboard PCIbus USB controller. The default is “Enabled”.

3.7 Advanced Chip-set Control Sub-menu

The options on this screen allow control over selected 82430HX chip-set settings that affect performance or function. The Advanced Chip-set Control Sub-menu is shown below.

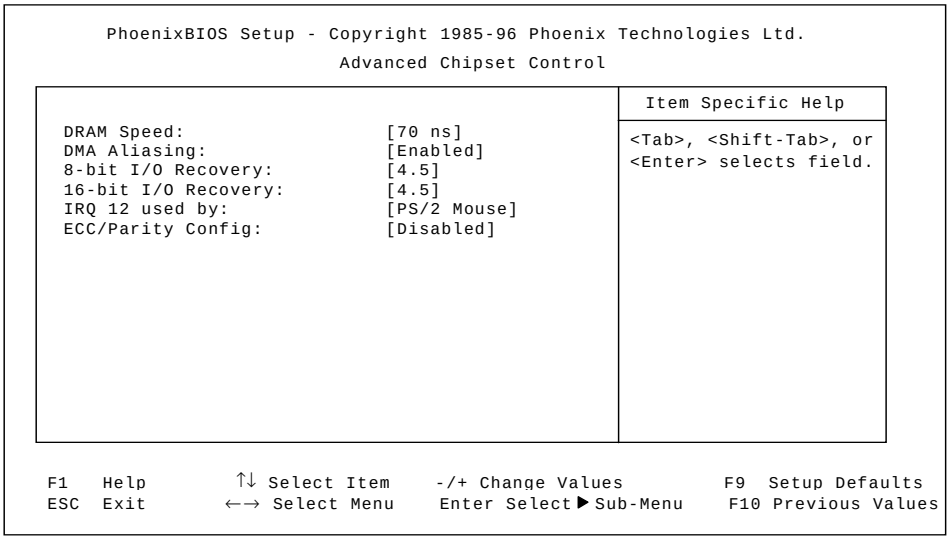


Figure 9. Advanced Chip-set Menu

DRAM Speed

This option selects the speed of the installed DRAM DIMMs. Selecting 70ns for 60ns DIMMs decreases performance. Selecting 60ns for 70ns DIMMs is invalid. The default is “70ns”.

DMA Aliasing

This option allows I/O accesses to the range 90-9Fh (except 92h) to alias to 80-8Fh. If an ISAbus device uses the address range 90-9Fh, then this option must be disabled to access the device. The default is “Enabled”.

8-bit I/O Recovery

This option selects the number of ISA bus SYSCLKs to be inserted between 8-bit back-to-back I/O accesses. Increasing the number of clocks decreases I/O performance but may allow slow devices to be accessed properly. This option can range from 3.5 through 11.5 SYSCLKs in 1 SYSCLK increments. The default is “4.5” SYSCLKs.

16-bit I/O Recovery

This option selects the number of ISA bus SYSCLKs to be inserted by the chip-set between 16-bit back-to-back I/O accesses. Increasing the number of clocks decreases I/O performance but may allow slow devices to be accessed properly. This option can range from 3.5 through 7.5 SYSCLKs in 1 SYSCLK increments. The default is “4.5” SYSCLKs.

IRQ 12 used by

This option selects the routing of IRQ12. For systems without a PS/2 mouse, this option may be set to “PCI bus” to allow an ISA bus peripheral to use this interrupt line. Systems using a PS/2 mouse must have this option set to “PS/2 Mouse” for the mouse to operate correctly. Since Grapevine supports the PS/2 mouse connector, the default is “PS/2 Mouse”.

ECC/Parity Config

This option configures the DRAM controller to use no parity (“Disabled”), parity (“Parity”), or Error Checking and Correction (“ECC”) when accessing DRAM. The default is “Disabled”.

3.8 Memory Cache Sub-menu

The options in this screen allows the control to cache certain memory regions plus control the settings of the Level 2 (L2) cache. The Memory Cache Sub-menu is shown below.

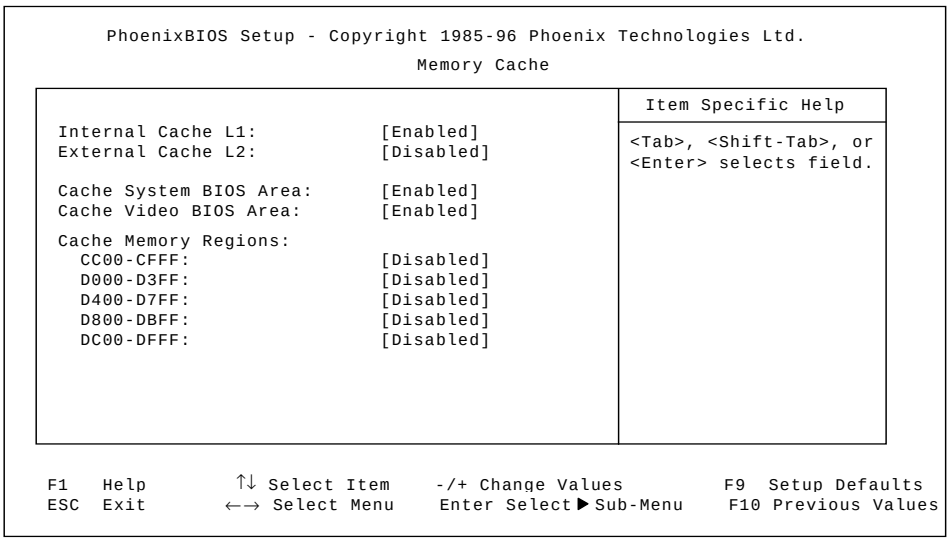


Figure 10. Memory Cache Menu

Internal Cache

This option enables or disables the Level 1 (L1) cache. The default is “Enabled”.

External Cache

This option enables or disables the Level 2 (L2) cache. The default is “Disabled”.

Cache System BIOS Area

This option enables or disables caching of the System BIOS area in the E0000h through FFFFFh DRAM area. The default is “Enabled”.

Cache Video BIOS Area

This option enables or disables caching of the VGA BIOS area in the C0000h through CBFFFh region. The default is “Enabled”.

Cache Memory Regions

These options enable or disable the caching of the associated memory regions. The default is “Disabled”.

3.9 Memory Shadow Sub-menu

The term “shadowing” refers to the technique of copying BIOS extensions from ROM into DRAM and executing them from DRAM. The Memory Shadow Sub-menu is shown below.

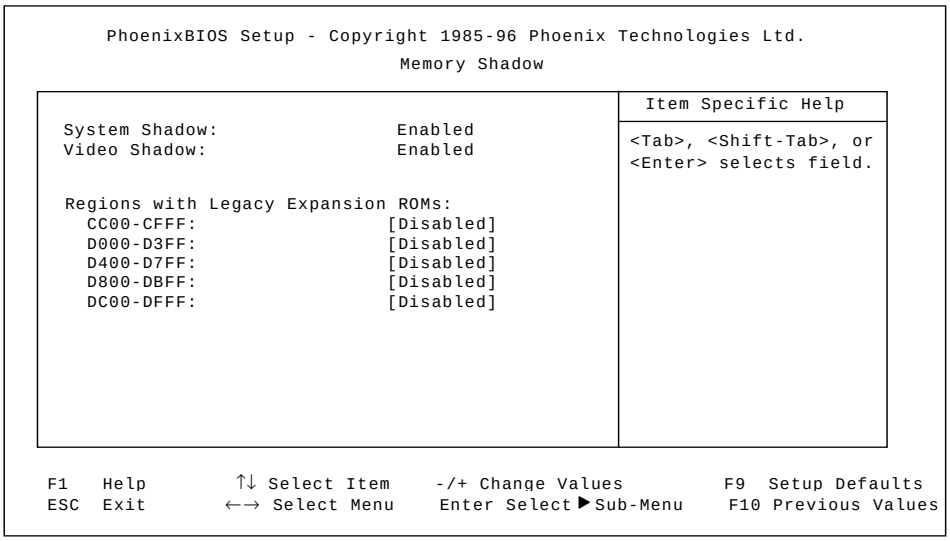


Figure 11. Memory Shadow Menu

System Shadow

This is not an option, the System BIOS is always shadowed.

Video Shadow

This is not an option, the VGA BIOS is always shadowed.

Shadow Memory Regions

This option enables or disables shadowing for the associated memory region. The default is “Disabled”.

3.10 Power Management Menu

The options in this menu provide control over the power management facilities. Only about one-half of the Power Management Menu Screen entries are visible at any one time. All of the Power Management Menu entries are listed and annotated.

System BIOS Power Management supported states are: Fully On, Standby Mode (partial power reduction), and Suspend Mode (maximum power reduction).

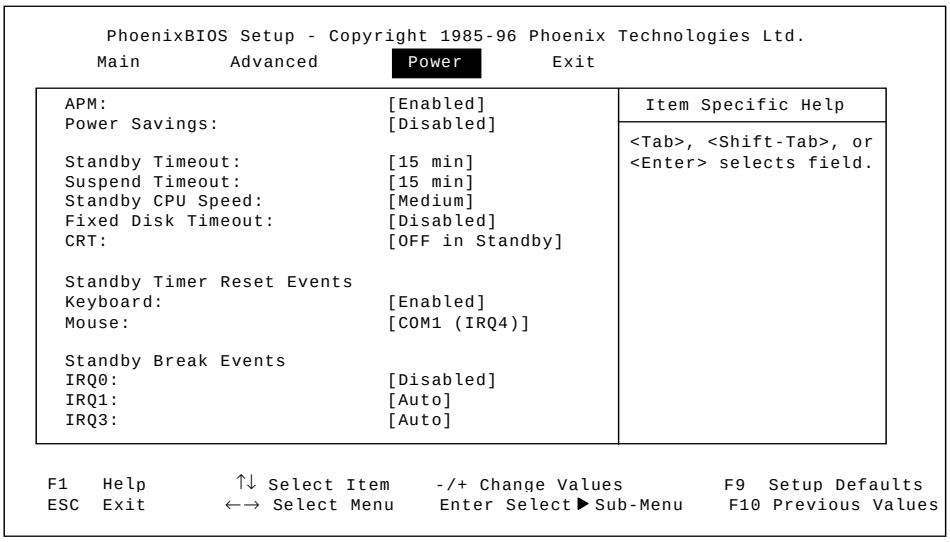


Figure 12. Power Management Menu

APM

This option enables or disables Advanced Power Management (APM). The default is "Enabled".

Power Savings

This option enables and selects the kind of power management, or disables power management. The options are: "Disabled", "Customize", "Maximum Power Savings", "Medium Power Savings", and "Minimum Power Savings". The default is "Disabled".

Standby Timeout

This option enables and sets the inactivity duration required to elapse before the system is placed into Standby Mode, or it disables the Standby Timeout. The options are: "Disabled", "2 min", "15 min", "30 min", "1 hour", "2 hours", "3 hours", and "4 hours". The default is "15 min".

Suspend Timeout

This option enables and sets the inactivity duration required to elapse before the system is placed into Suspend Mode from Standby Mode. This option can also be disabled. The options are: "Disabled", "2 min", "15 min", "30 min", "1 hour", "2 hours", "3 hours", and "4 hours". The default is "15 min".

Standby CPU Speed

This option enables or disables the changing of the CPU speed based upon the current power management state. The options are: "Disabled", "LOW", "MEDIUM", "HIGH", and "MAX". The default is "MEDIUM".

Fixed Disk Timeout

This option enables and sets the inactivity duration of fixed disk accesses required, before the system shuts off the disk drive. This option can also be disabled. The options are: "Disabled", "1 min", "2 min", "3 min", "4 min", "5 min", "10 min", and "16 min". The default is "Disabled".

CRT

This option enables or disables CRT power management during system entry/exit and into/from Standby Mode. The options are "OFF in Standby" and "ON". The default is "OFF in Standby".

Standby Timer Reset Events

These options enable or disable whether or not activity from the specified device causes the Standby Timer to be reset or not.

Keyboard

This option enables or disables keyboard activity to reset the Standby Timer or not. The default is "Disabled".

Mouse

This option enables or disables mouse activity to reset the Standby Timer or not. The options are disabled, "PS/2 (IRQ12)", "COM1 (IRQ4)", and "COM2 (IRQ3)". The default is "PS/2 (IRQ12)".

Standby Break Events

This option enables or disables a Standby Break Event for the specified IRQ. A Standby Break Event allows the system to run at full speed for the duration of the specified IRQ. There is no such event for IRQ2.

IRQ0

This option enables or disables the Standby Break Event for IRQ0. The options are: "Disabled" and "Auto". The default is "Disabled".

IRQ1

This option enables or disables the Standby Break Event for IRQ1. The options are: "Disabled" and "Auto". The default is "Auto".

IRQ3

This option enables or disables the Standby Break Event for IRQ3. The options are: "Disabled" and "Auto". The default is "Auto".

IRQ4

This option enables or disables the Standby Break Event for IRQ4. The options are: "Disabled" and "Auto". The default is "Auto".

IRQ5

This option enables or disables the Standby Break Event for IRQ5. The options are: "Disabled" and "Auto". The default is "Disabled".

IRQ6

This option enables or disables the Standby Break Event for IRQ6. The options are: "Disabled" and "Auto". The default is "Disabled".

IRQ7

This option enables or disables the Standby Break Event for IRQ7. The options are: "Disabled" and "Auto". The default is "Disabled".

IRQ8

This option enables or disables the Standby Break Event for IRQ8. The options are: "Disabled" and "Auto". The default is "Disabled".

IRQ9

This option enables or disables the Standby Break Event for IRQ9. The options are: "Disabled" and "Auto". The default is "Disabled".

IRQ10

This option enables or disables the Standby Break Event for IRQ10. The options are: "Disabled" and "Auto". The default is "Disabled".

IRQ11

This option enables or disables the Standby Break Event for IRQ11. The options are: "Disabled" and "Auto". The default is "Disabled".

IRQ13

This option enables or disables the Standby Break Event for IRQ13. The options are: "Disabled" and "Auto". The default is "Disabled".

IRQ14

This option enables or disables the Standby Break Event for IRQ14. The options are: "Disabled" and "Auto". The default is "Disabled".

IRQ15

This option enables or disables the Standby Break Event for IRQ15. The options are: "Disabled" and "Auto". The default is "Disabled".

Standby Wake-up Events

This option enables or disables the keyboard or mouse to cause a Standby Wakeup Event, allowing system activity to return to full speed.

Keyboard

This option enables or disables the Standby Wakeup Event for the keyboard. The default is "Enabled".

Mouse

This option enables and selects the IRQ that the mouse is bound to for the purposes of mouse activity detection for power management, or disables the Standby Wakeup Event for the mouse. The options are: "PS/2 (IRQ12)", "COM1 (IRQ4)", "COM2 (IRQ3)", and "Disabled". The default is "PS/2 (IRQ12)".

3.11 Exit Menu

The options in this menu allow saving settings and exiting, abandoning changes, then exiting to the system, or controlling the backup and restoration of CMOS RAM to Flash.

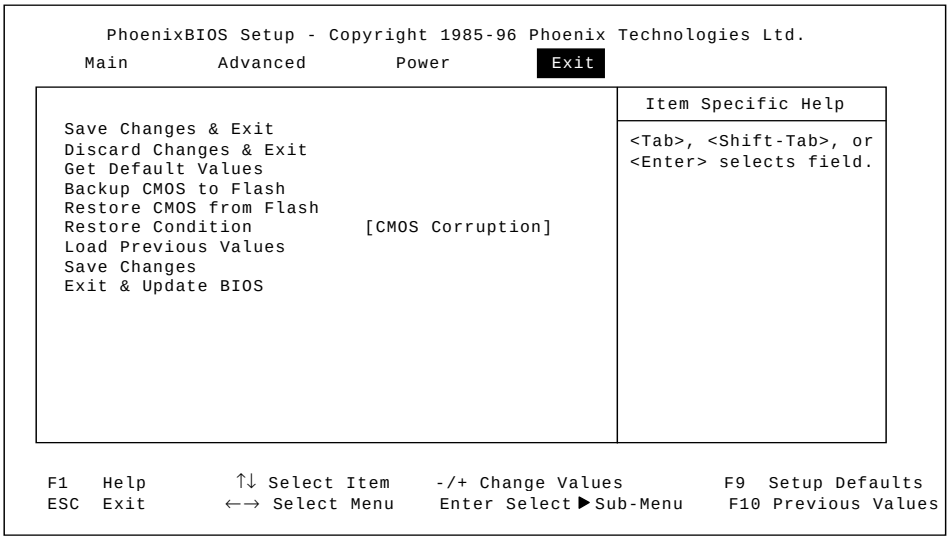


Figure 13. Exit Menu

Save Changes & Exit

This option saves into CMOS the values that have been entered and reboots the board.

Discard Changes & Exit

This option discards any changes made and reverts to the state when Setup was entered. The system reboots with the old values.

Get default values

This option is used to reset the Setup values to the original, default values that were set at the factory, before any suppliers or other end users made changes.

Backup CMOS to Flash

This option is used to immediately save current Setup settings to CMOS RAM and into Flash.

Restore CMOS from Flash

This option immediately restores CMOS RAM from flash, updating current Setup settings.

Restore Condition

This option determines what conditions the System BIOS restores CMOS RAM. The restore conditions are: “Always”, “Never”, and “CMOS Corruption”. The default is “CMOS Corruption”.

Load previous values

This option is used to load the system with the previous values before a Setup editing session started.

Save Changes

This option is used to save the edits made during a session.

Exit & Update BIOS

This option initiates a System BIOS update.

4.0 BIOS Recovery and BIOS Re-Flash

For a number of reasons, the flash device containing the BIOS may become corrupt or a new revision of the BIOS may need to be flashed into the Flash device. There are two methods to initiate a System BIOS update or recovery:

1. The "Force Recovery" jumper is installed to force a recovery sequence
2. The user selects "Exit and Update BIOS" from the Exit menu in Setup

Either method requires a floppy drive and a speaker be connected to the Base-G. Both methods have the Base-G boot from the boot block BIOS. There is no video during this process. A speaker is required to provide beep codes to indicate the progress/status of the process.

A floppy disk, called the Phlash diskette, containing files to update or recover the BIOS is also required. This Phlash diskette can be obtained from RadiSys.

4.1 Update or Re-flash the BIOS from the Setup "EXIT" Menu

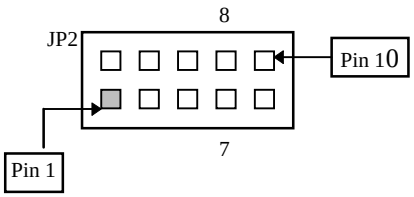
A BIOS update is performed from the Setup EXIT Menu.

1. Boot the Base-G and enter Setup by pressing the F2 key
2. Go to the EXIT menu
3. Make sure the floppy controller and floppy disk drive is properly configured in Setup.
4. Insert the Phlash diskette into the floppy drive
5. Select the option "Update BIOS and Exit"
6. The Base-G will reboot
7. After a few seconds the Base-G will emit a long beep followed by two short beeps
8. If the floppy diskette is not in the floppy drive or can not be accessed, the Base-G will emit three beeps
9. If the floppy is successfully being read by the boot block BIOS and the recovery process is successfully in progress, a steady single beep will continue the recovery is completed
10. If after two minutes a steady single beep has not materialized, there is something wrong with the floppy drive or the Phlash disk is bad
11. When one long beep is emitted, the recovery is completed
12. Remove the Phlash diskette and reboot the system/board

4.2 Re-flash the BIOS by Installing the "Force Recovery" Jumper

If the BIOS flash becomes corrupted, a recovery of the BIOS is performed by installing the "Force Recovery" jumper. This causes the Base-G to boot from the boot block BIOS.

1. Install the "Force Recovery" jumper on the Base-G



Pin	Description
7-8	Force Recovery

2. Make sure the floppy disk drive is properly installed
3. Insert the Phlash diskette into the floppy drive
4. Power up the Base-G NLX board/system
5. After a few seconds the Base-G will emit a long beep followed by two short beeps
6. If the floppy diskette is not in the floppy drive or can not be accessed, the Base-G will emit three beeps
7. If the floppy is successfully being read by the boot block BIOS and the recovery process is successfully in progress, a steady single beep will continue the recovery is completed
8. If after two minutes a steady single beep has not materialized, there is something wrong with the floppy drive or the Phlash disk is bad
9. When one long beep is emitted (if a speaker is attached), the recovery is completed
10. Power down the system/board
11. Remove the force jumper and the "Force Update" jumper
12. The baseboard/system can now be powered up

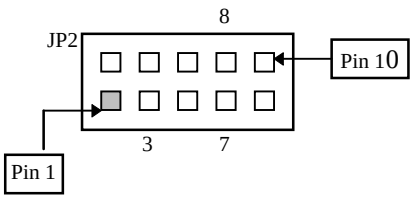
4.3 Boot Block Update Re-flash

The Base-G hardware and software is designed to protect the contents of the boot block. The boot block is the first code the processor executes at power-up or reset. If the boot block is corrupt and not executable, the Base-G must be returned to the factory for repair. Extreme caution must be taken when updating the boot block. A BIOS boot block rarely changes and should not require updating.

As with a BIOS recovery or BIOS update, the Phlash diskette is required, a floppy drive and a speaker must be connected to the Base-G. Updating the Boot Block Flash also updates the BIOS flash.. The baseboard still boots from the boot block BIOS. There is no video during this process. The speaker provides the beep codes to indicate the progress and status of the process.

To update the Boot Block BIOS the "force recovery" jumper and "boot block update" jumpers must be installed.

1. Install the "Force Recovery" and "Boot Block Update" jumpers on the Base-G



Pin	Description
7-8	Force Recovery
3-10	Boot Block Update

2. Make sure the floppy disk drive is properly installed
3. Insert the Phlash diskette into the floppy drive
4. Power up the Base-G NLX board/system
5. After a few seconds the Base-G will emit a long beep followed by two short beeps
6. If the floppy diskette is not in the floppy drive or can not be accessed, the Base-G will emit three beeps
7. If the floppy is successfully being read by the boot block BIOS and the recovery process is successfully in progress, a steady single beep will continue the recovery is completed
8. If after two minutes a steady single beep has not materialized, there is something wrong with the floppy drive or the Phlash disk is bad
9. When one long beep is emitted (if a speaker is attached), the recovery is completed
10. Power down the system/board
11. Remove the "Force Recovery" and "Boot Block Update" jumpers
12. The baseboard/system can now be powered up

5.0 Support and Service

5.1 Technical Support

RadiSys maintains a technical support phone that is staffed weekdays (except holidays) between 8:00 AM and 5:00PM pacific time. If assistance is required outside these hours, a voice-mail message can be left using the same phone number. Assistance can also be obtained via electronic mail or by a Fax addressed to RadiSys Technical Support Department. If you are sending email or a Fax, please include information on both the hardware and software being used, a detailed description of the problem, and specifically how the problem can be reproduced. RadiSys will respond by email, Fax or phone.

RadiSys Web Site home URL:	**www.RadiSys.com**
RadiSys support email address:	**support@RadiSys.com**
RadiSys support phone number:	**(800) 438-4769**
	(503) 615-1100

5.2 World Wide Web

RadiSys maintains an active site on the World Wide Web. The site contains current information about the company and locations of sales offices, new and existing products, contacts for sales, service and technical support information. You can also send email to RadiSys using the web site. Requests for sales, service, and technical support information receive a prompt response.

5.3 Repair Services

RadiSys provides Factory Repair Service for the entire RadiSys product line. Standard service for all RadiSys products covers factory repair with customers paying shipping to the factory and RadiSys paying for return shipment. Overnight return shipment is available at customer expense. Normal turn-around time for repair and re-certification is five working days.

Quick Exchange service (immediate shipment of loaner unit while the failed product is being repaired) are available. Negotiate these or other extra-cost services in advance to allow RadiSys to pool the correct product configurations. RadiSys does not maintain product “loaner” pool; units are available only for customers who have negotiated this service in advance.

RadiSys does not provide a fixed-price “swap-out” repair service. Many customers indicate the issues of serial number tracking and version control make it more convenient to receive their original products back after repair.

5.4 Warranty Repairs

RadiSys will repair at no charge, products having manufacturing defects during the warranty period. Products without fault sent in for warranty repair, are subject to a re-certification charge. Extended warranties are available for any product still under original warranty. RadiSys will gladly quote prices for extended warranties on products with lapsed original warranties.

Customer induced damage resulting from misuse, abuse, or exceeding a product’s specifications, is not covered by warranty.

5.5 Non-Warranty Services

There are several classes of non-warranty service. These include repair of customer induced problems, repairs of failures for products outside the warranty period, re-certification (function testing) of a product in or out of warranty, and the procurement of spare parts.
All non-warranty repairs are subject to service charges. RadiSys has determined the pricing of repairs based on time and materials is more cost-effective for the customer than a flat-rate repair charge. RadiSys analyzes the product after it is received. When instructed to do so, RadiSys informs the customer of repair costs for authorization. After the customer authorizes the repairs and makes the billing arrangements, RadiSys repairs the product and returns it to the customer.

5.6 Support and Service

RadiSys provides a re-certification service for products either in or out of warranty. This service verifies correct operation of a product by inspecting and testing the product using standard manufacturing tests. There is a product dependent charge for re-certification.

5.7 Arranging Service

To schedule service for a product, please call RadiSys' RMA Center. Have the product model and serial number available, along with a description of the problem. The RMA Dispatcher will issue a Returned Materials Authorization (RMA) number and a code number RadiSys uses to track the product while it is being processed. Follow the instructions of the RMA Dispatcher and return the product to RadiSys with the shipping prepaid. Mark the RMA number clearly on the exterior of the package. If possible, re-use the original shipping containers and packaging. Please follow good ESD control practices when handling the product.

Before you ship the product, include the following information:

- Return address
- Contact names and phone numbers
- A description of the problem

Ship the product to:

RadiSys Corporation
5445 N.E. Dawson Creek Dr.
Hillsboro, OR 97124

Attn: RadiSys RMA Center

Appendix A - User Installable Devices

A.1 Battery Replacement

The battery provides power backup for the real-time-clock and CMOS RAM. The lithium battery has a life expectancy of seven years. The batter is housed in a socket and can be replaced if it does fail.

Caution

There is a danger of explosion if the battery is incorrectly replaced. Replace with the same or equivalent type of battery.

To replace the battery, perform the following:

1. Turn off all peripheral devices connected to the system.
2. Turn off the system.
3. Remove any components blocking access to the battery.
4. Figure X shows the battery location on the baseboard.
5. Gently pry the battery free from the socket, noting the '+' and '-' orientation of the battery
6. Install the new battery
7. Replace any components previously removed.
8. Run set-up to reset the date and time.

A.2 DIMM Memory Installation

The Base-G has two 168-pin DIMM sockets with the option for an additional two more 168-pin DIMM sockets. The Base-G can be used with a single DIMM module, with a minimum memory size of 8Mbytes. A DIMM module can be place in any one of the DIMM socket sites.
The DIMM modules must be the following:

- 168-pin 3.3V with gold plated contacts
- 50ns - 60ns 3.3V non-buffered EDO memory
- 60ns-70ns FPM memory

Caution:
The memory DIMMs and other baseboard components can be damaged by electrostatic discharge (ESD) during installation. Please take the appropriate measures to prevent ESD damage.

1. Make sure the baseboard/system power is off.
2. Make sure the DIMM socket clip is 'open', pushed away from the DIMM socket
3. Orient the DIMM module to where the notch/key matches the notch/key of the socket (see figure X.)
4. Insert the DIMM module.
5. Flip the DIMM socket clip towards the DIMM module to secure the module

A.3 DIMM Memory Removal

Caution:
The memory DIMMs and other baseboard components can be damaged by electrostatic discharge (ESD) during installation. Please take the appropriate measures to prevent ESD damage.

1. Make sure baseboard/system power is off.
2. "Open" the DIMM socket by pushing the DIMM clip away from the DIMM socket (see figure X)
3. Remove the DIMM module

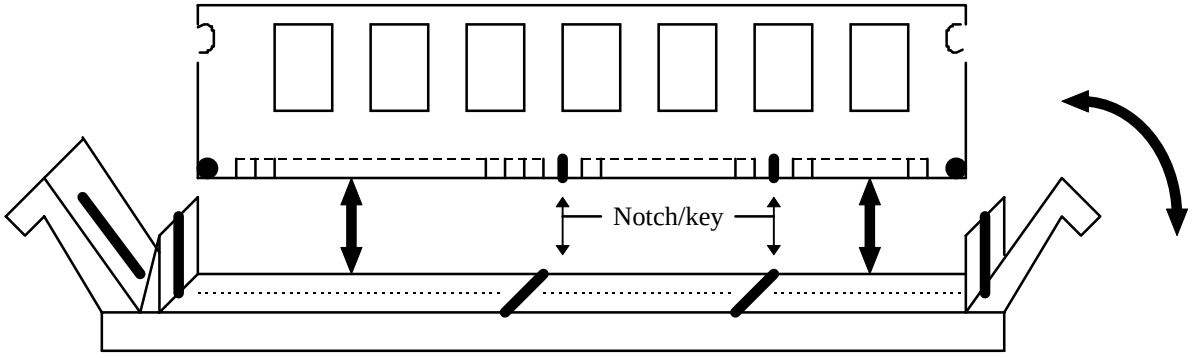


Figure 14. DIMM Memory Module Installation and Removal

Appendix B - Port 80 Post Codes

The Phoenix writes a number of checkpoints to I/O port 80h just before they are executed. The order of execution, for the most part, is the same as presented here. The beep codes require a speaker to be connected.

Beep Code	Post Code	Checkpoint Description
	02h	Verify Real Mode
	04h	Get CPU type
	06h	Initialize system hardware
	08h	Initialize chip-set registers with initial POST values
	09h	Set in POST flag
	0Ah	Initialize CPU registers
	0Bh	Enable CPU cache
	0Ch	Initialize cache to initial POST values
	0Eh	Initialize I/O
	0Fh	Initialize localbus IDE
	10h	Initialize Power Management
	11h	Load alternate registers with initial POST values
	12h	Jump to UserPatch0
	14h	Initialize keyboard controller
1-2-2-3	16h	BIOS ROM checksum
	18h	8254 timer initialization
	1Ah	8237 DMA controller initialization
	1Ch	Reset Programmable Interrupt Controller
1-3-1-1	20h	Test DRAM refresh
1-3-1-3	22h	Test 8742 Keyboard Controller
	24h	Set ES segment to register to 4GB
	28h	Autosize DRAM
	2Ah	Clear 512KB base RAM
1-3-4-1	2Ch	Test 512KB base address lines
1-3-4-3	2Eh	Test low byte of 512KB base memory
1-4-1-1	30h	Test high byte of 512KB base memory
	32h	Test CPU bus-clock frequency
	34h	Test CMOS RAM
	35h	Initialize alternate chip-set registers
	36h	Warmstart shutdown entry point
	37h	Reinitialize the chip-set
	38h	Shadow system BIOS ROM
	39h	Reinitialize the cache
	3Ah	Autosize cache
	3Ch	Configure advanced chip-set registers
	3Dh	Load alternate registers with CMOS values
	40h	Set Initial CPU speed
	42h	Initialize interrupt vectors
	44h	Initialize BIOS interrupts
2-1-2-3	46h	Check ROM copyright notice
	47h	Initialize manager for PCI Option ROMs

	48h	Check video configuration against CMOS
	49h	Initialize PCI bus and devices
	4Ah	Initialize all video adapters in system
	4Bh	Display QuietBoot™ screen
	4Ch	Shadow video BIOS ROM
	4Eh	Display copyright notice
	50h	Display CPU type and speed
	51h	Initialize EISA board
	52h	Test keyboard
	54h	Set key click if enabled
	56h	Enable keyboard
2-2-3-1	58h	Test for unexpected interrupts
	5Ah	Display prompt "Press F2 to enter SETUP"
	5Ch	Test RAM between 512KB and 640KB
	60h	Test extended memory
	62h	Test extended memory address lines
	64h	Jump to UserPatch1
	66h	Configure advanced cache registers
	68h	Enable external and CPU caches
	6Ah	Display external cache size
	6Ch	Display shadow message
	6Eh	Display non-disposable segments
	70h	Display error messages
	72h	Check for configuration errors
	74h	Test real-time clock
	76h	Check for keyboard errors
	7Ah	Test for key lock on
	7Ch	Set up hardware interrupts vectors
	7Eh	Test coprocessor if present
	80h	Disable onboard I/O ports
	82h	Detect and install external RS232 ports
	84h	Detect and install external parallel ports
	85h	Initialize PNP ISA devices
	86h	Re-initialize onboard I/O ports
	88h	Initialize BIOS Data Area
	8Ah	Initialize Extended BIOS Data Area
	8Ch	Initialize floppy controller
	90h	Initialize hard disk controller
	91h	Initialize localbus hard disk controller
	92h	Jump to UserPatch2
	93h	Build MPTABLE for multiprocessor boards
	94h	Disable A20 address line
	95h	Install CDROM for boot
	96h	Clear huge ES segment register
1-2	98h	Search for option ROMs (beep for bad checksum)
	9Ah	Shadow option ROMs
	9Ch	Set up Power Management
	9Eh	Enable hardware interrupts
	A0h	Set time of day
	A2h	Check keylock
	A4h	Initialize typematic rate

	A8h	Erase F2 prompt
	AAh	Scan for F2 keystroke
	ACh	Enter SETUP
	AEh	Clear in-POST flag
	B0h	Check for errors
	B2h	POST done--prepare to boot operating system
	B4h	One beep
	B5h	Display MultiBoot menu
	B6h	Check password (optional)
	B8h	Clear global descriptor table
	BCh	Clear parity checkers
	BEh	Clear screen (optional)
	BFh	Check virus and backup reminders
	C0h	Try to boot with INT19

Auxiliary Checkpoint Codes

Beep Code	Post Code	Checkpoint Description
	D0h	Interrupt handler error
	D2h	Unknown interrupt error
	D4h	Pending interrupt error
	D6h	Initialize option ROM error
	D8h	Shutdown error
	DAh	Extended Block Move
	DCh	Shutdown 10 error

Boot Block Checkpoint Codes

Beep Code	Post Code	Checkpoint Description
	E2h	Initialize the chip-set
	E3h	Initialize refresh counter
	E4h	Check for Forced Flash
	E5h	Check HW status of ROM
	E6h	BIOS ROM is OK
	E7h	Do a complete RAM test
	E8h	Do OEM initialization
	E9h	Initialize interrupt controller
	EAh	Read in bootstrap code
	EBh	Initialize all vectors
	ECh	Boot the Flash program
	EDh	Initialize the boot device
	EEh	Boot code was read OK

Appendix C - Power Supply Considerations

Power to the Base-G is drawn from the NLX riser board. The voltages provided by the NLX riser board include +12V, -12V, -5V, +5V, and 3.3V. The Base-G does not use -12V or -5V. The core voltage (Vcore) for the Pentium Processor is generated on the Base-G using the +5V supply using a LTC1430 switching power supply, capable of providing up to 6.5 amps of Vcore current.

Power monitoring circuitry on the Base-G board will reset the system if the required +3.3V or +5V supplies fall out of tolerance. This power monitoring circuit runs off the +12V supply and will not function correctly if the +12V falls lower than 3 volts. The power monitoring circuit on the board generates a reset to the system if:

- +5V on the board falls to less than 4.50 volts
- +3.3V on the board falls to less than 3.0 volts

The Base-G requires a NLX compliant power supply. When choosing a power supply for a Base-G NLX system, all system components requiring current from the power supply, PCI/ISA add-in cards, DIMM memory and peripherals need to be taken into consideration. The current for the 3.3V memory bus is drawn directly from the NLX power supply.

The following Base-G baseboard **worst-case** power specifications are supplied as a guide to help select the proper NLX compliant power supply (does not include the PMCM64A* option or DIMM memory) for a NLX compliant system.

Voltage Level	233MHz MMX
+5V	28.53
+3.3V	0.06W
+12.0V	8.52

* The PMCSVGA video option draws

Appendix D - Environmental Specifications

Temperature (Ambient)	operating	0^oC - 45^oC, derated 1^oC per 1000ft (300m) over 6600ft (2000m)
	storage	-40^oC - $+85^oC$
Humidity	operating / storage	5-95% RH non-condensing 25^oC - 60^oC
	condensation	15 minute max. recovery
Vibration	operating	$0.015g^2$/Hz from 5-500Hz, ~2.60g, 10 minutes each of 3 axes
	survival - random	$0.04g^2$/Hz from 5-500Hz, ~3.41g, 10 minutes each of 3 axes
	survival - sinusoid	5-500Hz resonance search, 1 oct./min. @ 1g (0-peak). 5 min. resonant dwell at up to 4 resonance, each of 3 axes.
Shock	operating	Delta v of ~90in/sec, 3ms half-sine impact, 150g, each of 6 product faces.
	survival	Delta v of ~292in/sec, 20-25ms trapezoidal impact, 45g, each of 6 product faces.
Altitude	operating	to 25,000ft (7700m)
	storage	to 50,000ft (15,300m)
Safety	ABSI/UL 1950 CSA22.2 No. 950-95 European CE Mark	
EMI/RFI	United States - FCC CISPR 22, Class A	