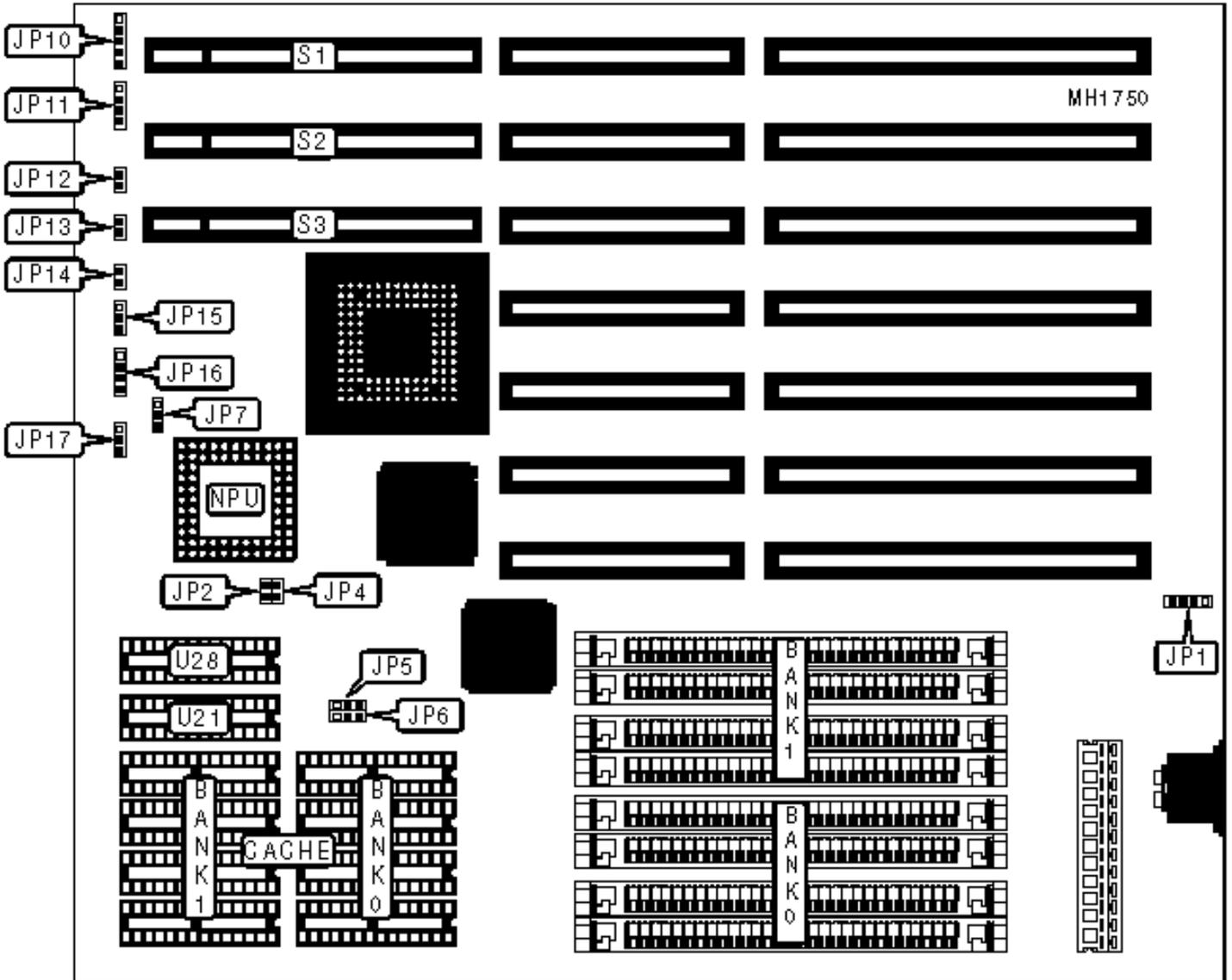


UNIDENTIFIED

M601 (VERSION 1.3)

Configuration



CONNECTIONS

Purpose	Location	Purpose	Location
External battery	JP1	Turbo switch	JP14
Power LED & keylock	JP10	32-bit VESA Local bus slot	S1
Speaker	JP11	32-bit VESA Local bus slot	S2
Turbo LED	JP12	32-bit VESA Local bus slot	S3
Reset switch	JP13		

USER CONFIGURABLE SETTINGS

Function	Jumper	Position
» CMOS normal operation (Internal)	JP1	pins 2 & 3 closed
CMOS normal operation (External)	JP1	pins 1 & 2 closed
CMOS memory clear	JP1	pins 3 & 4 closed

DRAM CONFIGURATION

Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
5MB	(4) 1M x 9	(4) 256K x 9
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
20MB	(4) 4M x 9	(4) 1M x 9
32MB	(4) 4M x 9	(4) 4M x 9
64MB	(4) 16M x 9	NONE

CACHE CONFIGURATION

Size	Bank 0	Bank 1	U21	U28
64KB	(4) 8K x 8	(4) 8K x 8	(1) 8K x 8	NONE
128KB	(4) 32K x 8	NONE	(1) 8K x 8	NONE
256KB	(4) 32K x 8	(4) 32K x 8	(1) 8K x 8	(1) 8K x 8
256KB	(4) 32K x 8	(4) 32K x 8	(1) 32K x 8	NONE

CACHE JUMPER CONFIGURATION

Size	JP2	JP4	JP5	JP6
64KB	Open	Open	pins 1 & 2 closed	Open
128KB	Open	Closed	pins 2 & 3 closed	pins 2 & 3 closed
256KB	Closed	Closed	pins 1 & 2 closed	pins 1 & 2 closed

CPU TYPE CONFIGURATION

CPU Type	JP16	JP17
CX486DLC	pins 2 & 3 closed	Open
80486SX	pins 2 & 3 closed	Open
80487SX	pins 1 & 2 and 3 & 4 closed	pins 2 & 3 closed
80486DX	pins 1 & 2 and 3 & 4 closed	pins 1 & 2 closed
80486DX2	pins 1 & 2 and 3 & 4 closed	pins 1 & 2 closed

CPU SPEED CONFIGURATION

Clock Generator	Speed	JP7	JP8
AV9107	40MHz	pins 1 & 2 closed	pins 1 & 2 closed
AV9107	50MHz	pins 2 & 3 closed	pins 1 & 2 closed
KTS0808C/0801C	40MHz	pins 1 & 2 closed	pins 1 & 2 closed

KTS0808C/0801C	50MHz	pins 2 & 3 closed	pins 1 & 2 closed
TK9207	33/66i MHz	pins 1 & 2 closed	pins 1 & 2 closed
TK9207	40MHz	pins 2 & 3 closed	pins 1 & 2 closed
TK9307	25/50i MHz	pins 1 & 2 closed	pins 1 & 2 closed
TK9307	33/66iMHz	pins 2 & 3 closed	pins 1 & 2 closed
TK9307	40MHz	pins 1 & 2 closed	pins 2 & 3 closed
TK9307	50MHz	pins 2 & 3 closed	pins 2 & 3 closed

Note:The exact location of JP8 is unknown.

VESA WAIT STATE/BUS SPEED CONFIGURATION

Speed	Wait states	JP15
25MHz	0 wait states	pins 1 & 2 closed
33MHz	1 wait state	pins 1 & 2 closed
50MHz	2 wait states	pins 1 & 2 closed