
# Neutron

## Single Board PC

## User Manual

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# COMPANY PROFILE

Blue Chip Technology is the leading specialist PC product manufacturer in UK/Europe.

Blue Chip Technology provides innovation with quality design and manufacturing from a single source.

Based in the Northwest, our purpose built complex contains one of the most advanced research and development facility, engineering workshop and production lines.

Specialising in the provision of industrial computing and electronic solutions for a wide range of UK and European organisations, Blue Chip Technology has one of the UK's largest portfolios of industrial PCs, peripherals and data acquisition cards. This extensive range of products, coupled with our experience and expertise, enables Blue Chip Technology to offer an industrial processing solution for any application. The PHOTON Single Board PC is one of the latest additions to our portfolio, providing a cost effective product development and volume production tool for OEMs.

A unique customisation and specialised system integration service is also available, delivering innovative solutions to customers problems. The company's success and reputation in this area has led to a number of large design and manufacturing projects for companies such as BNFL, Aston Martin, JaguarSport and British Gas.

British Standards Institute approval (BS EN ISO9001) means that all of Blue Chip Technology's design and manufacturing procedures are strictly controlled, ensuring the highest levels of quality, reliability and performance.

Blue Chip Technology are also committed to the single European market and continue to invest in the latest technology and skills to provide high performance computer and electronic solutions for a world-wide customer base.

# INTRODUCTION

## MANUAL OBJECTIVES

This manual describes in detail the Blue Chip Technology NEUTRON PC104 Single Board Processor Card (SBPC).

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard IBM Technical References, unless it proved to be necessary to aid in the understanding of the NEUTRON.

The manual is sectioned and includes a User Guide that will help the non-technical user to get the unit up and running. We strongly recommend that you study this manual carefully before attempting to interface with NEUTRON or change the standard configurations. Whilst all the necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier for guidance.

Please be aware that it is possible to create configurations within the CMOS RAM that make booting impossible. If this should happen, clear the CMOS settings by powering the system down and disconnecting the external lithium battery (if used).

If you have any suggestions or find any errors concerning this manual and want to inform us of these, please contact our Customer Support department with the relevant details.

## LIMITATIONS OF LIABILITY

In no event shall Blue Chip Technology be held liable for any loss, expenses or damages of any kind whatsoever, whether direct, indirect, incidental or consequential, arising from the design or use of this product or the support materials supplied with this product. If this product proves to be defective, Blue Chip Technology is only obliged to replace or refund the purchase price at Blue Chip Technology's discretion according to their Terms and Conditions of Sale.

## PRECAUTIONS

It is imperative that precautions are taken to avoid electro-static discharges, or any maltreatment of the off-board lithium battery.

### *ELECTRO-STATIC DISCHARGES*

The devices on this card can be totally destroyed by static electricity. Ensure that you take necessary static precautions, ideally wear an approved wrist strap or touch a suitable ground to discharge any static build up. This should be repeated if the handling is for any length of time.

When carrying the board around, please place it into the non-conductive bag in which it came. This will prevent any static electricity build up.

### *OFF-BOARD BATTERY*

This board supports an off board a Lithium battery. Great care should be taken with this type of battery. Under NO circumstances should:

- the outputs be shorted
- be exposed to temperatures in excess of 100°C
- be burnt
- be immersed in water
- be unsoldered
- be recharged
- be disassembled

***IF THE BATTERY IS MISTREATED IN ANY WAY THERE IS A VERY REAL POSSIBILITY OF FIRE, EXPLOSION AND HARM.***

## RELATED PUBLICATIONS

The following publications will provide useful information related to the Standard Personal Computer and can be used in conjunction with this manual.

- IBM Personal Computer AT Technical Reference, 1502494, IBM, 1984.
- IBM Personal System/2 & Personal Computer BIOS Interface Technical Reference, 15F0306, IBM, 1987.
- The Programmers PC Sourcebook, Microsoft
- The Winn L. Rosch Hardware Bible, Brady
- PC104 Consortium Technical Specification

## TRADEMARKS

# USER GUIDE

## OVERVIEW

The Blue Chip Technology NEUTRON single board PC sets new standards for integration of the latest advances in processor, memory, and I/O technologies. The NEUTRON complies with the PC104 interface requirements. NEUTRON is an ideal platform for the increasing requirements of today and tomorrow's embedded applications.

The design is based on the AMD Am5x86-P75 running at an internal clock rate of 133MHz providing an equivalent performance to a P75. The memory sub-system supports 16MB of on-board DRAM.

The NEUTRON single board PC utilises the ALI Finali PCI chipset to provide increased integration and performance over other single board PC designs. The Finali PCIset contains an integrated PCI Bus EIDE controller with a high performance IDE interface allowing up to two IDE devices (such as hard drives, CD-ROM readers, etc.). A Chips & Technologies 69000 video controller supports both CRT and LCD displays, simultaneously if required. The SMC 37C665 Super I/O controller integrates the standard PC I/O functions: floppy interface, two FIFO serial ports and one EPP/ECP capable parallel port.

In addition to superior hardware capabilities, a full set of software drivers and utilities are available to allow advanced operating systems such as Windows 95/98 to take full advantage of the hardware capabilities. Features such as Windows 95/98-ready Plug and Play (PnP), PCI EIDE and Advanced Power Management (APM) are available for NEUTRON.

A standard set of cables to cover most common applications is available separately.

## *BOARD LEVEL FEATURES*

- AMD 5x86-P75 133MHz CPU
- On-board 3.3 V CPU voltage regulator
- ALI Finali PCI chipset:
  M1489 Cache Memory PCI Controller (CMP)
  Also providing dual PCI IDE interface
  M1487 ISA bridge Controller (IBC)
- 16MByte of DRAM on-board
- Chips & Technologies 69000 video controller with 2MB of video DRAM
- PC104 (ISA) expansion bus
- SMC 37C665 I/O controller providing:
  Dual floppy interface
  EPP/ECP bi-directional parallel interface
  Dual RS232 serial ports.
- Real-time clock with support for off-board Lithium battery
- PS/2 keyboard support.
- 3 programmable digital input/output lines.
- 128 bytes user EEPROM.
- +5v only operation.
- Optional socketed Solid State Disk -
  2-288 MByte Flash expansion using Disk On Chip (DOC)

## *CPU*

The NEUTRON PC104 single board PC is designed to operate with AMD Am5x86-P75 CPU running at 3.3 Volts. An on-board voltage regulator circuit provides the required voltage for the processor from the 5V output of a standard PC power supply.

The Am5x86-P75 processor maintains full backward compatibility with the 8x86 architecture processors. It supports burst mode bus cycles, and includes an integrated unified 16KB on-chip cache which employs a write-back policy. Also integrated into the processor is an advanced numeric co-processor which significantly increases the speed of floating point operations, whilst maintaining backward compatibility with 8x87 math coprocessor and complying with ANSI/IEEE standard 754-1985.

## *BUS EXPANSION SLOTS*

NEUTRON is designed for use in an embedded application and provides ISA expansion via the standard PC/104 (ISA) connector. There may be up to four PC/104 bus expansion cards.

## *ELECTROMAGNETIC COMPATIBILITY*

This product meets the requirements of the European EMC Directive (89/336/EEC) and is eligible to bear the CE mark. However, because the board can be installed in a variety of computers and enclosures, certain conditions have to be applied to ensure that the compatibility is maintained. Subject to those conditions, it meets the requirements for an industrial environment (Class A product).

- The board must be installed in a computer system chassis that provides screening suitable for an industrial environment.
- Any recommendations made by the computer system manufacturer/supplier must be complied with regarding earthing and the installation of boards.
- The board must be installed with any bulkhead plates securely screwed to the chassis of the computer to ensure good metal-to-metal (i.e. earth) contact.
- Most EMC problems are caused by cabling external to the board. It is imperative that any external cabling to the board is totally screened, and that the screen of the cable connects to the metal enclosure and hence to earth. It is recommended that round screened cables with a braided wire screen are used in preference to those with a foil screen and drain wire. Use metal connector shells that connect around the full circumference of the screen: they are far superior to those that earth the screen by a simple “pig-tail”.
- The keyboard and mouse will play an important part in the compatibility of the processor card since it is a port into the board. Similarly, they will affect the compatibility of the complete system. A fully compatible keyboard and/or mouse must be used otherwise the complete system could be degraded. The keyboard/mouse themselves may radiate or behave as if keys are pressed when subject to interference. Under these circumstances it may be beneficial to add a ferrite clamp on the keyboard/mouse lead as close as possible to the connector. A suitable type is the Chomerics type H8FE-1004-AS.
- Ensure that the screens of any external cables are bonded to a good RF earth at the remote end of the cable.

Failure to observe these recommendations may invalidate the EMC compliance.

**Warning**
This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

## SPECIFICATION

| | | | |
|---|---|---|---|
| NEUTRON Power Requirement | | +5 V ± 5% | Required for processor operation. |
| | | +12 V ± 5%<br>-5 V ± 5%<br>-12 V ± 5% | ⎫ Not required for board operation.<br>⎬ The PC/104 voltage rails<br>⎭ are linked on board. |
| Typical System Consumption | | 8 Watts | Am5x86-P75 16 MB RAM |
| Temperature | Non-Operating | -40°C to +80°C | |
| | Operating | +0°C to +40°C (min. airflow of 15 $m^3$/hour)<br>+0°C to +50°C (min. airflow of 45 $m^3$/hour)<br>+0°C to +60°C (min. airflow of 66 $m^3$/hour) | |
| Humidity | Operating | 10 % to 90 % RH, non-condensing | |
| EMC | Emissions | EN55022 (A) | |
| | Immunity | EN50082-1 in a Blue Chip ICON Industrial PC Chassis | |
| MTBF | Estimated | 100,000 Hrs | |
| Dimensions | Board only | 108 x 96 mm | |

Power Consumption figures given are for a typical configuration. This information is provided only as a guide to calculating approximate total power usage for a system.

### *COOLING*

Efficient cooling is essential for long and reliable operation. The greater the volume of air, the greater the cooling effect and the lower the temperature rise above the ambient air temperature. However, the volume produced by any fan will vary with the pressure against which it has to work. The resistance to airflow (the back-pressure on the fan) will depend upon the enclosure, the mounting and restrictions. Therefore, when mounting and cabling the board, it is essential that the free circulation of the cooling airflow is not impeded.

The calculation of airflow through an enclosure is not straightforward, and depends on many factors. The method of meeting the cooling requirements will be specific for each system. Consequently, the system builder is responsible for ensuring adequate cooling. However, interpreting airflow volumes is not intuitive. As an aid to selecting suitable cooling, the following example is offered. A 60 mm axial fan (such as a Papst type 612NGH) blowing over the board can supply up to 46 $m^3$/hour when unrestricted. Restrictions to the airflow will reduce this volume.

# HARDWARE DESCRIPTION

## CHIPSET

The Ali Finali PCI Chipset consists of the M1489 Cache Memory PCI controller (CMP) and the M1487 ISA Bridge Controller (IBC).

## M1489 CACHE MEMORY PCI CONTROLLER (CMP)

The M1489 provides all control signals necessary to drive a second level cache (not implemented) and the DRAM array, including multiplexed address signals. The CMP provides access to memory and generates snoop controls to maintain cache coherency. The CMP also integrates an intelligent Host to PCI interface buffer to improve system performance. The high performance Local bus EIDE interface is also provided by the CMP. The CMP comes in a 208-pin PQFP package.

### *IDE SUPPORT*

The NEUTRON single board PC provides one high performance PCI IDE interfaces capable of supporting PIO Mode 3 and Mode 4 devices. The system BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes as well as ATAPI (e.g. CD-ROM) devices. Detection of IDE device transfer rate and translation mode capability is automatically determined by the system BIOS.

## M1487 ISA BRIDGE CONTROLLER (IBC)

The M1487 provides the bridge between the ISA bus, PCI bus and Host Bus. It integrates the standard PC peripherals such as DMA Interrupt controllers, keyboard, RTC and Timer functions. The IBC is packaged in a 160 pin PQFP

### *REAL TIME CLOCK, CMOS RAM AND BATTERY*

The integrated Real Time Clock (RTC) is both DS1287 and MC146818 compatible. It provides a time of day clock and a 100-year calendar with alarm features. The RTC can be set via the BIOS SETUP program. The RTC also supports128 bytes of battery-backed CMOS RAM which is reserved for BIOS use. The CMOS RAM can be set to specific values or cleared to the system default values using the BIOS SETUP program.

A battery is required to maintain the RTC and CMOS memory whilst the power is switched off. NEUTRON is fitted with a connector to allow the use of an off-board 3.7V Lithium battery. The CMOS RAM values can be cleared to the system defaults by disconnecting the external Lithium battery.

## VIDEO: CHIPS & TECHNOLOGIES 69000

The NEUTRON provides the latest technology integrated PCI video sub-system. The board is fitted with a 10-way header providing standard VGA signals, dual headers to interface to a wide range of LCD panels of up to 36 bits, and a dedicated connector for popular LCDs. The 69000 integrates 2MB of video memory and DAC into a single BGA device. All the necessary drivers for most popular operating systems are supplied on a utilities disk.

## SMC 37C665 SUPER I/O CONTROLLER

Control for the integrated serial ports, parallel port and floppy drive controller is incorporated into a single component, the SMC 37C665. This component provides:

- Two NS16C550-compatible UARTs with send/receive 16 byte FIFO
- Multi-mode bi-directional parallel port
  - Standard mode; IBM and Centronics compatible
  - Enhanced Parallel Port (EPP) with BIOS support
  - High Speed mode; Extended Capabilities Port (ECP) compatible
- Industry standard floppy controller with 16 byte data FIFO (2.88 MB floppy support)

The 37C665 is normally configured by the BIOS automatically, however configuration of these interfaces is possible via the CMOS Setup program that can be invoked during boot-up. The serial ports can be enabled as COM1, COM2, or disabled. The parallel port can be configured as normal, extended, EPP/ECP, or disabled. The floppy interface is configurable.

Header connectors allow cabling to use these interfaces.

### *FLOPPY CONTROLLER*

The 37C665 is software compatible with the DP8473 and 82077 floppy disk controllers.

The floppy interface can be configured for 360 KB or 1.2 MB 5¼" media or for 720 KB, 1.44 MB, or 2.88 MB 3½" media in the BIOS Setup. By default, the Floppy A interface is configured for 1.44 MB and Floppy B is disabled.

## WATCHDOG FUNCTION

NEUTRON provides both hardware and software watchdog functions.

The hardware watchdog will trigger a reset if the +5V supply drops below 4.6V.

When enabled the software watchdog will trigger a reset if there is a ½ second gap between reads from I/O port 101h. The software watchdog is enabled by writing 1 to bit 0 of I/O port101h.

## PROGRAMMABLE DIGITAL INPUT/OUTPUTS

NEUTRON provides for three programmable, TTL-compatible digital input/output lines. They are selected as a BIOS option to the User EEPROM. Digital I/O is not available if the user EEPROM option is selected.

See the section "Using the Additional IO Functions" on the use of the I/O lines.

## USER EEPROM

NEUTRON provides 128 bytes of user accessible non-volatile memory in the form of an EEPROM. This is selected as an option to the digital I/O function in the BIOS. The EEPROM is not available if the Digital I/O option is specified.

See the section "Using the Additional IO Functions" on the use of the EEPROM.

## SOLID STATE DISK SUPPORT

NEUTRON supports the use of Solid State Disks using a Disk-on-Chip module fitted into the 32-pin DIL socket. This permits Hard disk read/write emulation with disk capacities currently ranging from 2 M to 288 MBytes. See the section "*Disk-On-Chip Support*" under Software Description for installation details.

Please contact Blue Chip Technology's Sales Department for details.

# BIOS

The NEUTRON single board PC uses an AMI system BIOS, which is stored in EPROM. In addition to the System BIOS, the EPROM also contains the Setup utility, Power-On Self Test (POST), and the PCI auto-configuration utility. This single board PC supports system BIOS shadowing, allowing the BIOS to execute from 32-bit on-board write-protected DRAM.

The BIOS displays a sign-on message during POST identifying the type of BIOS and a revision code.

Note that the user-configurable parameters are stored in CMOS memory. In order to maintain the parameters whilst the power is switched off, a battery must be connected to the board.

## *SYSTEM SETUP UTILITY*

The EPROM-based Setup utility allows the configuration to be modified without opening the system for most basic changes. The Setup utility is accessible only during the Power-On Self Test (POST) by pressing the <DEL> key after the POST memory test has started and before boot begins. A prompt may be enabled that informs users to press the <DEL> key to access Setup.

## *PCI SUPPORT*

The Neutron board supports Version 2.0 of the PCI BIOS specification for the on-board PCI devices.

## *ISA PLUG AND PLAY*

The AMI BIOS incorporates ISA Plug and Play capabilities as defined by the Plug and Play Release 1.0A specification (Plug and Play BIOS Version 1.0A, ESCD Version 1.02). This allows auto-configuration of Plug and Play ISA cards, and resource management for non-Plug and Play (or legacy) ISA cards, when used in conjunction with Plug and Play aware operating systems (such as Windows 95/98).

## *AUTO-CONFIGURATION CAPABILITIES*

The auto-configuration utility operates in conjunction with the system Setup utility to allow the insertion and removal of ISA Plug and Play cards to the system without user intervention of the BIOS settings (Plug & Play). When the system is turned on after adding an ISA Plug and Play card, the BIOS automatically configures interrupts, DMA channels, I/O space, and memory space. The user does not have to configure jumpers or worry about potential resource conflicts. Because ISA Plug and Play cards use the same interrupt resources as ISA cards, the user can specify the interrupts used by ISA add-in cards in the Setup utility. If using Windows 95/98, the auto-configuration utility only initialises the devices required to boot up, Windows 95/98 initialises all the other devices since it is a Plug and Play aware operating system.

## ADVANCED POWER MANAGEMENT

The NEUTRON AMI BIOS supports power management through System Management Mode (SMM) interrupts to the CPU and Advanced Power Management (APM Version 1.1). In general, power management capabilities will allow the system to be put into a power managed, Stand-by mode either by entering a user configurable hot-key sequence on the keyboard, or by the expiration of a hardware timer which detects system inactivity for a user-configurable time. When in the Stand-by mode, the NEUTRON single board PC reduces power consumption by using the power saving capabilities of the Am5x86-P75 processor and also running down hard drives and turning off DPMS compliant monitors. Add-in cards supplied with APM-aware drivers can also be put into a power managed state for further energy savings. The ability to respond to external interrupts is fully maintained while in Stand-by mode, allowing the system to service requests (such as in-coming Fax's or network messages) while unattended, albeit slowly until the system wakes up.

## SLEEP MODE SUPPORT

When Advanced Power Management (APM) is activated in the System BIOS and the Operating System's APM driver is loaded, Sleep mode (Stand-By) can be entered in one of three ways.

Sleep/Resume may be activated by using either a momentary-action sleep switch in the UTILS header ('external SMI' input), a keyboard hot-key sequence, or by a time-out of the system inactivity timer. Both the keyboard hot-key and the inactivity timer are programmable in the BIOS setup (timer is set to 10 minutes by default). To re-activate the system, or "Resume", the user simply uses the keyboard or mouse, or presses the sleep switch. Note that mouse activity will only "wake up" the system if a mouse driver is loaded. While the system is in Stand-By or "Sleep" mode it is fully capable of responding to, and servicing external interrupts. Once in Sleep or Stand-By mode, the monitor will only turn on if a user interrupt occurs as defined above.

## SECURITY FEATURES

Note that the security features are only supported when an off-board battery supports the CMOS RAM.

### SUPERVISOR PASSWORD

If enabled, the supervisor password protects all sensitive Setup options from being changed by a user unless the password is entered (see appendix).

If the password is forgotten, it may be cleared by turning off the system and clearing the CMOS RAM by disconnecting the battery (if used).

### USER PASSWORD

The User Password feature provides access to all setup options that do not require the supervisor password. The User Password feature also provides security during the boot process. The User Password can be enabled using the Setup utility. (At boot-up, the system will complete the operating system boot up process, but keyboard and mouse operation will be locked until the User Password is entered.)

If the password is lost, it may be reset by clearing the CMOS RAM, (see below).

## CLEARING CMOS MEMORY

This should be required under exceptional circumstances such as losing the password, or setting incompatible parameters in the BIOS.

Switch off the system and disconnect the off-board battery from the NEUTRON. Wait for two minutes to allow the decoupling capacitor to discharge, and then reconnect the battery. Switch on the system, enter the BIOS setup and set as required.

## CONNECTORS

Various connectors are incorporated on the NEUTRON PC board. These provide connectivity to external peripherals (serial, parallel, keyboard, etc.), in-chassis peripherals (disk drives, etc.), and bus devices. A complete table of the available connectors and their pin-outs is given in the appendices.

An optional cable set is available to simplify setting up common applications. The cables included in the standard cable set are indicated against each connector. For the other connectors, suitable mating parts are given. The PC board layout at the end of the manual shows their positions.

ON-BOARD CONNECTORS

There are connectors on-board for Floppy Disk Drive, IDE, LCD, video, sound, serial and parallel ports, PC/104, digital inputs and utilities. There are also connectors for Power supply and external battery.

### *UTILITY CONNECTOR*

The NEUTRON PC board provides a connector to support functions such as reset switch, speaker, Turbo LED, Power LED, keyboard, and external SMI to invoke the power saving mode of the NEUTRON.

### *BUS CONNECTORS*

The board incorporates the PC/104 bus connector for expansion. See the appendices for the pin-out details.

## JUMPERS

Jumpers are used on the board to select options. Some of the jumpers are factory set to suit particular semiconductor options. These must not be disturbed, or damage to the board may ensue.

| JUMPER | AREA OF INFLUENCE | LINK | ACTION |
|---|---|---|---|
| **J1** | DRAM voltage | N/A | Hardwired in manufacture to suit DRAMs fitted. |
| **J2** | LCD Panel Power Supply<br>Note: your LCD may be damaged if set incorrectly | 1-2 | +3.3 volts selected |
| | | 2-3 | +5 volts selected |

# SOFTWARE DESCRIPTION

## BIOS SETUP

This section details the BIOS CMOS Setup Utility. The parameters described below are based on BIOS version 1.00; other BIOS versions may differ from the description below as new features are added. The BIOS Setup is entered by pressing the <DEL> key during the Power On Self Test (POST).

### OVERVIEW OF THE SETUP MENU SCREENS

The Setup program initially displays the Main menu screen. In each screen there are options for modifying the system configuration. Select a sub-menu screen by pressing the up <↑> or down <↓> arrow keys, followed by <Enter>. Within the menu use the up <↑> or down <↓> keys to select an item, then use <PgUp> or <PgDn> to modify it. Pressing <Enter> may bring up a sub-screen. After you have selected an item, use the <PgUp> or <PgDn> keys to modify the setting.

#### *MAIN SCREEN*

Shows the following menu:

Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Power Management Setup
PCI / Plug and Play Setup
Peripheral Setup
Auto Detect Hard Disk
Change User Password
Change Supervisor Password
Auto Configuration with Optimal Settings
Auto Configuration with Fail Safe Settings
Save Settings and Exit
Exit without Saving

Their operation is as follows:

*STANDARD CMOS SETUP*

For setting up and modifying basic items such as floppy disk drives, hard drives, and system time & date.

*ADVANCED CMOS SETUP*

Use to modify the more advanced features of the PC (e.g. system bootup options).

*ADVANCED CHIPSET SETUP*

Use to modify hardware level options.

### *POWER MANAGEMENT SETUP*

For specifying the "Green PC" features such as IDE and VGA timeouts.

### *PCI / PLUG AND PLAY SETUP*

For specifying Plug and Play options (e.g. IRQ assignments).

### *PERIPHERAL SETUP*

For specifying the system peripheral options such as serial and parallel port modes.

### *AUTO DETECT HARD DISK*

Automatically determines the parameters of any IDE devices connected, and sets up the parameters for "USER DEFINED" drives.

### *CHANGE USER PASSWORD*

Allows the password for the user level options to be set or changed. This option cannot be changed unless a supervisor password has been set.

### *CHANGE SUPERVISOR PASSWORD*

Allows the password for the supervisor level options to be changed.

### *AUTO CONFIGURATION WITH OPTIMAL SETTINGS*

Resets the CMOS setup options to a high performance configuration. The optimal default settings are best case values and should optimise the system performance. If CMOS RAM is corrupted, the optimal settings are loaded automatically.

### *AUTO CONFIGURATION WITH FAIL SAFE SETTINGS*

Resets the CMOS setup options to a lower performance but guaranteed working configuration. The fail safe settings provide far from optimal system performance, but are the most stable settings. Use these settings as a diagnostics aid if the system is performing erratically.

### *SAVE SETTINGS AND EXIT*

When selected, this allows you to save the change to CMOS and exit the Setup program. You can also press the <F10> key anywhere in the Setup program to do this. Note that unless an off-board battery is connected to the NEUTRON board, the CMOS settings will be lost when power is removed from the board.

### *EXIT WITHOUT SAVING*

When selected, this allows you to exit the Setup program without saving any changes. This means that any changes made while in the Setup program will be discarded and **NOT SAVED**. Pressing the <Esc> key in any of the four main screens will do this.

## *OVERVIEW OF THE SETUP KEYS*

| SETUP KEY | DESCRIPTION |
|---|---|
| <Esc> | Pressing the <Esc> key takes you back to the previous screen. Pressing it in the Main, Advanced, Security, or Exit screen allows you to Exit Discarding Changes (see later in this chapter). |
| <PgUp> <PgDn> | Pressing either key moves the selection of the current item up or down the available options. |
| < ↑ > | Pressing the up < ↑ > key changes the selection to the previous item or option. |
| < ↓ > | Pressing the down < ↓ > key changes the selection the to the next item or option. |
| < ← > < → > | Pressing the left < ← > or right < → > keys in the Main, Advanced, Security, or Exit menu screens changes the menu screen. Pressing either key in a subscreen does nothing. |
| <F10> | Pressing the <F10> key allows you to Exit Saving Changes (see later in this chapter). |

## *STANDARD SETUP*

This section describes the Setup options found on the standard setup screen.

### *SYSTEM DATE*

When selected, this allows you to set the current date by specifying a date, month and year.

### *SYSTEM TIME*

When selected, this allows you to set the current time by entering values for hours, minutes and seconds..

### *FLOPPY A: TYPE*

When selected, this allows you to cycle through the available options to specify the physical size and capacity of the diskette drive. The options are Not Installed; 360 KB, 5.25-inch; 1.2 MB, 5.25-inch; 720 KB, 3.5-inch; 1.44 MB, 3.5-inch; 2.88 MB, 3.5-inch. The default is 1.44 MB, 3.5-inch.

### *FLOPPY B: TYPE*

When selected, this allows you to cycle through the available options to specify the physical size and capacity of the diskette drive. The options are Not Installed, 360 KB, 5.25-inch; 1.2 MB, 5.25-inch; 720 KB, 3.5-inch; 1.44/1.25 MB, 3.5-inch; 2.88 MB, 3.5-inch. The default is Not Installed.

### *PRIMARY IDE MASTER*

This reports if a primary master IDE hard disk is connected to the system and allows for the configuration of drive parameters.

This allows for the manual configuration of the hard drive or, to have the system auto configure the drive. The options are Auto Configured, User Definable and Disabled. There are also options for IDE CD-ROM and 46 predefined hard drive types. If you select User Definable then the Number of Cylinders, Number of Heads, and Number of Sectors can each be modified. The default for this is Auto.

### *PRIMARY IDE SLAVE*

This reports if a primary slave IDE hard disk is connected to the system. It is configured exactly as described under Primary IDE Master above. The default is "Not Installed".

### *SECONDARY IDE MASTER*

This reports if a secondary master IDE hard disk is connected to the system. It is configured exactly as described under Primary IDE Master above. The default is "Not Installed". (Note: Neutron does not support an on board secondary IDE channel).

### *SECONDARY IDE SLAVE*

This reports if a secondary slave IDE hard disk is connected to the system. It is configured exactly as described under Primary IDE Master above. The default is "Not Installed". (Note: Neutron does not support an on board secondary IDE channel).

#### *NUMBER OF CYLINDERS*

If Hard Disk Type is set to User Definable, you must type the correct number of cylinders for your hard disk. If Hard Disk Type is set to Auto Configured, this reports the number of cylinders for your hard disk and cannot be modified.

#### *NUMBER OF HEADS*

If Hard Disk Type is set to User Definable, you must type the correct number of heads for your hard disk. If Hard Disk Type is set to Auto Configured, this reports the number of heads for your hard disk and cannot be modified.

#### *NUMBER OF SECTORS*

If Hard Disk Type is set to User Definable, you must type the correct number of sectors for your hard disk. If Hard Disk Type is set to Auto Configured, this reports the number of sectors for your hard disk and cannot be modified.

#### *LBA MODE*

Selects Logical Block Addressing mode for large capacity drives. Options are On or Off. The default is On.

#### *BLOCK MODE*

Permits multi-sector transfers. Options are On or Off. The default if On.

### *PIO MODE*

Selects an Advanced PIO mode of operation for faster transfers. Options are 0, 1, 2, 3, 4, 5, or Auto. The default is Auto.

### *32-BIT MODE*

Selects 32-bit transfer mode. The options are On or Off. The default is Off.

## *BOOT SECTOR VIRUS PROTECTION*

Detects if software tries to write to the boot sector. Options are Enabled or Disabled. The default is Disabled.

## *ADVANCED CMOS SETUP*

### *BOOTUP SEQUENCE*

This option specifies the sequence of the boot drives. The options are:

A:, C:, CDROM

C:, A:, CDROM ( Default)

CDROM, C:, A:

### *PARITY CHECK*

This option specifies the type of memory installed i.e. parity or non parity. When this option is set to Enabled a parity test is performed on all accesses to system DRAM. The Optimal and Fail-Safe default settings are Disabled.

### *OS/2 COMPATIBLE MODE*

Set this option to Yes to permit AMIBIOS to run with IBM OS/2. The settings are Enabled or Disabled. The default setting is Disabled.

### *WAIT FOR 'F1' IF ERROR*

AMIBIOS POST error messages are followed by:

Press <F1> to continue

If this option is set to Disabled, AMIBIOS does not wait for you to press the <F1> key after an error message. The settings are Disabled or Enabled. The Optimal and Fail-Safe default settings are Disabled.

### *HIT 'DEL' MESSAGE DISPLAY*

Set this option to Disabled to prevent the

Hit <DEL> if you want to run Setup

message from appearing on the first AMIBIOS screen when the computer boots. The settings are Disabled or Enabled. The Optimal and Fail-Safe default settings are Disabled.

### *INTERNAL CACHE*

This option specifies whether or not the L1 internal cache memory is enabled. The settings are Disabled or WriteBack. If WriteBack is selected, the write-back caching algorithm is used. The default is WriteBack.

### *SYSTEM BIOS SHADOW CACHEABLE*

When this option is set to Enabled, the contents of the F0000h system memory segment can be read from or written to L1 cache memory. The contents of the F0000h memory segment are always copied from the BIOS ROM to system RAM for faster execution.

The settings are Enabled or Disabled. The Optimal and Fail-Safe default settings are Enabled.

*C000, 16K Shadow*
*C400, 16K Shadow*
*C800, 16K Shadow*
*CC00, 16K Shadow*
*D000, 16K Shadow*
*D400, 16K Shadow*
*D800, 16K Shadow*
*DC00, 16K Shadow*

These options control the location of the contents of the 16KB blocks of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

| SETTING | DESCRIPTION |
|---|---|
| Enabled | The contents of the named ROM area (e.g. C0000h - C3FFFh) are written to the same address in system memory (RAM) for faster execution. |
| Cache | The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area.<br>In addition, the contents of the RAM area can be read from and written to cache memory. |
| Disabled | The ROM is not copied to RAM. The contents of the ROM cannot be read from or written to cache memory. |

The default settings are Cached for C000 and C400; Disabled for the remainder.

In the AMIBIOS for the ALI Finali chipset, the E000h page is used as ROM during POST and shadowing is enabled for this region. Thus the E000h page is not available on the local bus.

## *ADVANCED CHIPSET SETUP*

### *AUTO CONFIG FUNCTION*

When set to enabled, this option allows the BIOS to automatically determine the best system timing settings for the AT Bus and the DRAM and cache etc. The default settings are Enabled and it is strongly recommended that these values are not changed unless the user is fully aware of the system parameter timings. Changing these values to an incorrect setting can cause system instability or even prevent the Neutron board from booting. The options are Enabled or Disabled. The default setting is Enabled.

#### *AT BUS CLOCK*

This option is only available when the Auto Config Function is enabled. The options are 7.16 MHz, Clk/3, Clk/4, Clk/5, Clk/8.

#### *DRAM READ TIMING*

This option is only available when the Auto Config Function is enabled. The options are Slow, Normal, Faster, Fastest.

#### *DRAM WRITE TIMING*

Slow, Normal, Faster, Fastest.

#### *SRAM READ TIMING*

This option is only available when the Auto Config Function is enabled. The options are 2-1-1-1, 3-1-1-1, 3-2-2-2, 4-2-2-2.

#### *SRAM WRITE TIMING*

This option is only available when the Auto Config Function is enabled. The options are 0 wait states or 1 wait state.

### *HIDDEN REFRESH*

This option enables or disables ISA refresh cycles. The Optimal and Fail-Safe default settings are Disabled.

### *ISA I/O RECOVERY*

This option specifies whether or not an additional delay is inserted between consecutive I/O operations. The settings are Disabled or Enabled. The Optimal and Fail-Safe default settings are Disabled.

## *POWER MANAGEMENT SETUP*

### *POWER MANAGEMENT / APM*

Set this option to Enabled to enable the power management and APM (advanced Power Management) features.

The settings are Enabled, Disabled or Inst-On. The default settings are Disabled.

**Note:** The following options are only available if Power Management/APM is enabled.

### *INSTANT ON SUPPORT*

If this option is set in Power Management / APM it allows the computer to go to full power on mode when leaving a power-conserving state. AMIBIOS uses the RTC Alarm function to wake the computer at a pre-specified time. The settings are Enabled or Disabled. The default settings are Disabled.

### *GREEN PC MONITOR POWER STATE*

This option specifies the power management state that the Green PC-compliant video monitor enters after the specified period of display inactivity has expired. The settings are, Disabled, Standby, Suspend or Off. The default settings are Disabled.

### *VIDEO POWER DOWN MODE*

This option specifies the power management state that the video subsystem enters after the specified period of display inactivity has expired. The settings are Disabled, Standby or Suspend. The default settings are Disabled.

### *HARD DISK POWER DOWN MODE*

This option specifies the power management state that the hard disk drive enters after the specified period of display inactivity has expired. The settings are Disabled, Standby, or Suspend. The default settings are Disabled.

### *HARD DISK TIME OUT (MINUTE)*

This option specifies the duration of hard disk inactivity. When this period expires, the hard disk drive enters the power-conserving mode specified in the Hard Disk Power Down Mode option described above. The settings are Disabled, 1 (minutes), and all one minute intervals up to and including 14. The default settings are Disabled.

### *STANDBY TIME OUT (MINUTE)*

This option specifies the duration of system inactivity when the computer is in Full-On mode before the computer is placed in Standby mode. In Standby mode, the power use is reduced. The settings are Disabled, 1 (minutes), and all one minute intervals up to and including 14. The default settings are Disabled.

### *SUSPEND TIME OUT (MINUTE)*

This option specifies the duration of system inactivity when the computer is already in Standby mode before the computer is placed in Suspend mode. In Suspend mode, the power use is minimised. The settings are Disabled, 1 (minute), and all one minute intervals up to and including 14. The default settings are Disabled.

### *DISPLAY ACTIVITY*

This option specifies if AMIBIOS is to monitor activity on the display monitor for power conservation purposes. When this option is set to Monitor and there is no display activity for the length of time specified in the value in the (full on to) Standby Timeout (Minute) option, the computer enters a power saving state. The settings are Monitor or Ignore. The default settings are Ignore.

### *IRQ 3, 4, 5, 7, 9, 10, 11, 12, 13, 14, 15*

These options enable event monitoring. When the computer is in a power saving mode, activity on the named interrupt request line is monitored by AMIBIOS. When any activity occurs, the computer enters Full On mode.

Each of these options can be set to Monitor or Ignore. The default settings are Ignore.

## *PCI / PLUG AND PLAY SETUP*

### *PLUG AND PLAY AWARE O/S*

AMIBIOS only detects and enables PnP ISA adapter cards that are required for system boot. Set this option to Yes if the operating system installed in the computer is Plug and Play-aware. Windows 95/98 is PnP-aware. Windows 95/98 detects and enables all other PnP-aware adapter cards. Set this option to No if the operating system (such as DOS, OS/2, Windows 3.x) does not use PnP.

**Note:** You must set this option correctly or PnP-aware adapter cards installed in your computer will not be configured properly. The settings are No or Yes. The Optimal and Fail-Safe default settings are No.

### *PCI LATENCY TIMER (PCI CLOCKS)*

This option sets latency of all PCI devices on the PCI bus. The settings are in PCI clock units. The settings are 32, 64, 96, 128, 160, 192, 224, or 248. The Optimal and Fail-Safe default settings are 192.

### *CPU TO PCI WRITE BUFFER*

This option enables or disables a 4-layer double word buffer between the CPU and the PCI bus. When enabled it significantly improves the system performance. The settings are Disabled or Enabled. The Optimal and Fail-Safe default settings are Enabled.

#### *BYTE MERGE*

This option is only available when the CPU to PCI Write Buffer is enabled. It allows Neutron to use the 32-bit PCI bus more effectively. When enabled, this feature merges bytes or words to double words. When enabled it improves the system performance in non-32-bit applications or transfers. The Optimal and Fail-Safe default settings are Enabled.

#### *FAST BACK TO BACK*

This option is only available when the CPU to PCI Write Buffer is enabled. When enabled, it improves the CPU to Write Buffer performance. The options are Enabled or Disabled. The Optimal and Fail-Safe default settings are Enabled.

### *PCI TO DRAM BUFFER*

This option enables or disables a 2 line double word buffer to improve the transfer performance of a PCI master device. The options are Enabled or Disabled. The default settings are Enabled

### *DMA CHANNELS 0, 1, 3, 5, 6, 7*

These options specify the bus to which the DMA channel is allocated.

The options determine if AMIBIOS should remove a DMA channel from the available pool passed to BIOS configurable devices. The available pool is determined by reading the ESCD NVRAM. If more DMA channels must be removed from the pool, the end user can use these PCI/PnP Setup options to remove the channel by selecting the ISA/EISA setting. Onboard I/O is configured by AMIBIOS. The DMA channels used

by onboard I/O are configured as PnP. The options are PnP or ISA/EISA.

The default settings for all channels are PnP in both Optimal and Fail-Safe modes.

### *IRQ 3, 4, 5, 7, 9, 10, 11, 14, 15*

These options specify the bus on which the named interrupt request lines (IRQs) are used. These options allow you to specify IRQs for use by legacy ISA adapter cards.

The options determine if AMIBIOS should remove an IRQ from the pool of available IRQs passed to BIOS configurable devices. The available IRQ pool is determined by reading the ESCD NVRAM. If more IRQs must be removed from the pool, the user can remove the IRQ by selecting the ISA/EISA setting. Onboard I/O IRQs are configured by AMIBIOS as PCI/PnP.

The options are PCI/PnP or ISA/EISA. The optimal and fail-safe settings for all available IRQs are PCI/PnP.

### *RESERVED MEMORY SIZE*

This option specifies the size of the memory area reserved for legacy ISA adapter cards.

The settings are Disabled, 16K, 32K, or 64K. The Optimal and Fail-Safe default settings are Disabled.

### *RESERVED MEMORY ADDRESS*

This option specifies the starting address (in hex) of the reserved memory area. The specified ROM memory area is reserved for use by legacy ISA adapter cards.

The settings are C0000, C4000, C8000, CC000, D0000, D4000, D8000, DC000. The Optimal and Fail-Safe default settings are CC000.

## *PERIPHERAL SETUP*

### *ONBOARD FDC*

This option enables the floppy drive controller on the PC board. The settings are Auto, Enabled or Disabled. The default setting is Auto.

### *ONBOARD SERIAL PORT1*

This option enables serial port 1 on the board and specifies the base I/O port address for serial port 1.

The settings are Auto, 3F8h, 3E8h, 2F8h, 2E8h, or Disabled. The default is Auto.

### *ONBOARD SERIAL PORT2*

This option enables serial port 2 on the board and specifies the base I/O port address.

The settings are Auto, 3F8h, 3E8h, 2F8h, 2E8h, or Disabled. The default is Auto.

### *ONBOARD PARALLEL PORT*

This option enables the parallel port on the board and specifies the base I/O port address. The settings are Auto, 378h, 278h, 3BCh, or Disabled. The default setting is Auto.

### *PARALLEL PORT MODE*

This option specifies the parallel port mode. ECP and EPP are both bi-directional data transfer schemes that adhere to the IEEE P1284 specifications. The options are :

| SETTING | DESCRIPTION |
|---|---|
| Normal | The normal parallel port mode is used. This is the default setting. |
| EPP | The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bi-directional data transfer driven by the host device. |
| ECP | The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve transfer rates of approximately 2.5Mbs. ECP provides symmetric bi-directional communications. |

### *PARALLEL PORT DMA*

This option is only available if the setting for the Parallel Port Mode option is ECP.

The settings are 0, 1, or 3. The default setting is 3.

### *PARALLEL PORT IRQ*

Selects which IRQ is assigned to the parallel port. Options are 5 or 7. The default is 7.

### *ONBOARD IDE*

This option specifies the onboard IDE controller channels that will be used. The settings are Primary, Both or Disabled. The Optimal and Fail-Safe default settings are Primary.

### *HARDWARE IO PORT BASE ADDRESS*

The NEUTRON has additional IO functions (watchdog timer, three TTL-compatible, programmable digital input/output lines, and a user-accessible EEPROM). This menu option specifies the base address of the control registers for these options. The permissible values are:

100 hex (default) up to 300 hex, and 8000 hex up to 8300 hex, in increments of 100 hex.

### *EEPROM OR USER IO*

The user EEPROM and User IO are mutually exclusive. This option selects one or the other. The default setting is User IO.

### *IO LINE 0*

This option is only valid if User IO has been selected. It sets the IO line as either an input or an output. The default setting is as input.

Note that the setting may also be changed under program control (see the section "Using the Additional IO Functions".

### *IO LINE 1*

This option is only valid if User IO has been selected. It sets the IO line as either an input or an output. The default setting is as input.

Note that the setting may also be changed under program control (see the section "Using the Additional IO Functions".

### *IO LINE 2*

This option is only valid if User IO has been selected. It sets the IO line as either an input or an output. The default setting is as input.

Note that the setting may also be changed under program control (see the section "Using the Additional IO Functions".

# ADDRESS MAPS

## *MEMORY MAP*

| **ADDRESS RANGE** (DECIMAL) | **ADDRESS RANGE** (HEX**)** | **SIZE** | **DESCRIPTION** |
|---|---|---|---|
| 0K – 511K | 00000 - 7FFFF | 512K | Conventional |
| 512K – 638K | 80000 - 9FBFF | 127K | Extended conventional |
| 639K | 9FC00 - 9FFFF | 1K | Extended BIOS Data (moveable by QEMM, 386MAX) |
| 640K – 799K | A0000 – C7FFF | 160K | Video memory and BIOS ( if fitted) |
| 800K – 847K | C8000 – D3FFF | 48K | Available HI DOS memory (open to ISA and PCI bus) |
| 848K – 879K | D4000 – DBFFF | 32K | BIOS Extensions |
| 880K – 895K | DC000 – DFFFF | 16K | Solid State Disk Pages |
| 896K – 1023K | E0000 – FFFFF | 128K | AMI System BIOS (not available for UMB) |
| 1024K - 131072K | 100000 – 8000000 | 127M | Extended Memory |

## *I/O MAP*

The following table lists the I/O addresses used by single board PC devices. Some of these devices (e.g. graphics) may not be present in all configurations. Some devices (serial ports, parallel ports etc.) may be configured for various addresses or disabled. These I/O locations are listed in the Variable Resources column.

| ADDRESS (HEX) | SIZE Bytes | FIXED RESOURCES | VARIABLE RESOURCES |
|---|---|---|---|
| 0000 - 000F | 16 | DMA 1 | |
| 0020 - 0021 | 2 | Interrupt Controller 1 | |
| 002E - 002F | 2 | Ultra I/O configuration registers | |
| 0040 - 0043 | 4 | Timer 1 | |
| 0060 | 1 | Keyboard Controller Data Byte | |
| 0061 | 1 | NMI, speaker control | |
| 0064 | 1 | KBD Controller, CMD/STAT Byte | |
| 0070, bit 7 | 1 bit | Enable NMI | |
| 0070, bits 6:0 | 7 bits | RTC, Address | |
| 0071 | 1 | RTC, Data | |
| 0080 - 008F | 16 | DMA Page Register | |
| 00A0 - 00A1 | 2 | PIIIX - Interrupt Controller 2 | |
| 00B2 - 00B3 | 2 | APM Control / Status Interrupt Controller 2 | |
| 00C0 - 00DE | 31 | DMA 2 | |
| 00F0 | 1 | Reset Numeric Error | |
| 0100 # | 1 | EEPROM and Digital IO Register | |
| 0101 # | 1 | Watchdog | |
| 0102 – 0107 # | 6 | Reserved for Board Configuration | |
| 0170 - 0177 | 8 | | |
| 01F0 - 01F7 | 8 | | Primary IDE Channel |
| 0278 - 027B | 4 | | Parallel Port 2 |
| 02E8 - 02EF | 8 | | Serial Port 4 |
| 02F8 - 02FF | 8 | | Serial Port 2 |
| 0376 | 1 | | |
| 0377 | 1 | | |
| 0378 - 037F | 8 | | Parallel Port 1 |
| 03B0 - 03BB | 4 | | Video controller |
| 03BC - 03BF | 4 | | Parallel Port 3 |
| 03C0 - 03DF | 16 | | Video controller |
| 03E8 - 03EF | 8 | | Serial Port 3 |
| 03F0 - 03F5 | 6 | | Floppy Channel 1 |
| 03F6 | 1 | | Pri IDE Chan Cmnd Port |
| 03F7 (Write) | 1 | | Floppy Chan 1 Cmd |
| 03F7, bit 7 | 1 bit | | Floppy Disk Chg Chan 1 |
| 03F7, bits 6:0 | 7 bits | | Pri IDE Chan Status Port |
| 03F8 - 03FF | 8 | | Serial Port 1 |
| LPT + 400h | 3 | | ECP regs, LPT base + 400h |
| 04D0 - 04D1 | 2 | Edge/Level INTR Control Reg. | |
| 0CF8 - 0CFC* | 4 | PCI Config Address Reg. | |
| 0CF9 | 1 | Turbo & Reset control Reg. | |
| 0CFC - 0CFF | 4 | PCI Config Data Register | |
| FFA0 - FFA7 | 8 | | 1ary Bus Master IDE regs |
| FFA8 - FFAF | 8 | | 2ary Bus Master IDE regs |
| FF00-FF07 | 8 | | IDE Bus Master Reg. |

* only accessible by DWORD accesses.

# alternatively based at $100_h$ boundaries up to and including $300_h$, or $8000_h$ to $8300_h$.

## *INTERRUPTS & DMA CHANNELS*

The following tables list the Interrupt and DMA Channel configuration options for on-board devices. The serial ports, parallel ports, and IDE controller can be configured using SETUP, or any other Plug and Play resource manager (such as the Windows 95/98 Device Manager). The Graphics interrupt is assigned by the auto-configure utility during boot up.

| IRQ | RESERVED INTERRUPTS |
|---|---|
| NMI | I/O Channel Check |
| 0 | Interval Timer |
| 1 | Keyboard buffer full |
| 2 | Cascade interrupt from slave PIC |
| 3 | Serial 2 (COM2) |
| 4 | Serial 1 (COM1) |
| 5 | Parallel 2 (LPT2) |
| 6 | Floppy Controller |
| 7 | Parallel (LPT1) |
| 8 | Real time clock |
| 9 | |
| 10 | |
| 11 | |
| 12 | |
| 13 | Math co-processor |
| 14 | Primary E-IDE |
| 15 | |

| DMA | RESERVED |
|---|---|
| 0 | |
| 1 | |
| 2 | Floppy |
| 3 | |
| 4 | Cascade channel |
| 5 | |
| 6 | |
| 7 | |

## USING THE ADDITIONAL IO FUNCTIONS

NEUTRON provides as standard a watchdog timer, and depending upon the BIOS settings, either three programmable digital input/outputs or a user EEPROM. The board configuration registers for these functions are located at the IO base address set by the BIOS. (See "*Software Description - BIOS Setup – Peripheral Setup – Hardware IO Port Base Address*").

### *WATCHDOG TIMER OPERATION*

NEUTRON includes a watchdog timer circuit, which may be used to monitor software or processor hardware failure. The time-out period of the watchdog is fixed at 500 milliseconds. It may be enabled or disabled by using the software interrupt at INT 50h, or by writing individual bits to the Watchdog Timer Register directly.

The Watchdog Timer Register is located at the IO Base Address +01h. Setting bit 0 of the register enables the timer. When enabled, the watchdog will generate a hardware reset if it is not refreshed every 500 msecs or more frequently. Reading the register refreshes the timer. The data returned by the read operation is not meaningful.

Note that the watchdog is disabled following a power on or a reset sequence.

WATCHDOG TIMER – Base Address +01h

| BIT | FUNCTION |
|---|---|
| 0 | 0=Disabled(default), 1=Enabled<br>When enabled reading the port address refreshes the watchdog timer. |
| 1-7 | Reserved |

The following code demonstrates the control of the watchdog timer.

*ENABLE/DISABLE WATCHDOG*

EITHER use the software interrupt as follows:

Calling Registers: AH = 05
AL = 01 to enable, 00 to disable

Perform INT 50h.

Return Registers: AH = 00, and Carry flag is clear if successful
AH = 02, and Carry flag is set if function valid but disabled
AH = FF, and Carry flag set if function failed

OR execute the following code:

```
mov dx,101h      ;assumes base address is 100h (the default)
mov al,1h        ;enable watchdog
out dx,al

mov dx,101h      ;assumes base address is 100h (the default)
mov al,0h        ;disable watchdog
out dx,al
```

*REFRESH WATCHDOG*

EITHER use the software interrupt as follows at least once every 500 milliseconds:

Calling Registers: AH = 06

Perform INT 50h

Return Registers: Carry flag clear

OR execute the following code at least once every 500 milliseconds:

```
mov dx,101h      ;assumes base address is 100h (the default)
in al, dx        ;refresh timer
```

## *EEPROM ACCESS AND CONTROL*

The EEPROM on the NEUTRON unit is a NM93C46 serially programmed device that is accessed through a single register at IO Base Address +00h. It comprises 128 bytes of user programmable memory, organised as 64 x 16 bit words. The EEPROM does not have to be completely erased before writing to a single location.

Access to the EEPROM is by reading and writing individual bits in the control register. The bits are arranged thus:

EEPROM CONTROL – IO Base Address +00h

| BIT | FUNCTION |
|---|---|
| 0 | Write – Chip Select<br>Read – Data |
| 1 | Write – Clock<br>Read – N/A |
| 2 | Write – Data<br>Read – N/A |
| 3-7 | Reserved |

The EEPROM may be controlled directly by program, or through the BIOS. The BIOS provides two functions to simplify user access to the EEPROM memory, available through a software interrupt (INT 50h):

*WRITE TO SINGLE EEPROM LOCATION*

Calling Registers: AH = 03
BL = Location (0 – 63)
DX = Write data (16-bit value)

Perform INT 50h

Return Registers: AH = 00, and Carry flag is clear if successful
AH = 02, and Carry flag is set if function valid but disabled
AH = FF, and Carry flag set if function failed

*READ SINGLE EEPROM LOCATION*

Calling Registers: AH = 04
BL = Location (0 – 63)

Perform INT 50h

Return Registers: DX = EEPROM Data
AH = 00, and Carry flag is clear if successful
AH = 02, and Carry flag is set if function valid but disabled
AH = FF, and Carry flag set if function failed

## *PROGRAMMABLE DIGITAL INPUT/OUTPUTS*

NEUTRON provides three TTL-compatible programmable digital input/output lines as a BIOS-selected option. These lines occupy the lower 3 bits of the byte located at the IO Base Address +00h. They are individually selectable as input or output in the BIOS, or under program control by writing to the IO Base Address +05h.

IO DIRECTION CONTROL REGISTER - IO Base Address +05h

| BIT | FUNCTION |
|---|---|
| 0 | Write, 1=Output, 0=Input |
| 1 | Write, 1=Output, 0=Input |
| 2 | Write, 1=Output, 0=Input |
| 3-7 | Reserved |

The inputs are available by a simple read operation at IO Base Address +00h. As inputs, they are non-inverting, and are pulled high by on-board resistors. Bits 3 to 7 are undefined. Outputs are available by writing to the same address.

Alternatively the direction control and data may be handled using the software interrupt function (Int 50h):-

*SET USER IO LINE CONTROL*

Calling Registers: AH = 17 (hex)
DL (bits 2-0) = IO Line Mask (0=input, 1=output)

Perform INT 50h

Return Registers: Carry Flag is clear, and AH=00 if successful
Carry flag is set, and AH=02 if not enabled in BIOS setup.

*WRITE USER IO LINES*

Calling Registers: AH = 16 (hex)
DL (bits 2-0) = IO Line data

Perform INT 50h

Return Registers: Carry Flag is clear, and AH=00 if successful
Carry flag is set, and AH=02 if not enabled in BIOS setup.

*READ USER IO LINES*

| | |
|---|---|
| Calling Registers: | AH = 15 (hex) |
| Perform INT 50h | |
| Return Registers: | DL (bits 2-0) = IO Line data (bits 7-3 = 0)<br>Carry Flag is clear, and AH=00 if successful<br>Carry flag is set, and AH=02 if not enabled in BIOS setup. |

## *ACCESSING INT 50H FUNCTIONS*

Most high level languages allow access to software interrupts through a particular function call. The user loads a particular function code into the AH register followed by a specific set of parameters in the other registers before executing the interrupt.

For example, in C :-

```
#include <stdio.h>
#include <dos.h>

#define PHOTON 0x50

void main(void)
{
    union REGS regs;
    regs.x.ax = 0x0400;                    /* read eeprom data */
    regs.x.bx = 0x31;                      /* from address 0x31 */
    int86(PHOTON, &regs, &regs);
    printf("EEPROM Address 0x31 contains %x\n",regs.x.dx);
}
```

and similarly in Quick Basic

```
'Read EEPROM Data via interrupt 50 call
$include:'QB.BI'

DIM INARY%(7), OUTARY%(7)
CONST AX=0,BX=1,CX=2,DX=3,BP=4,SI=5,DI=6,FL=7

INARY%(AX) = &H0400                        ' Read e2 data
INARY%(BX) = &H31                          ' address &H31
CALL INT86OLD(&H50,INARY%(),OUTARY%())   ' Call the Int50h service
PRINT "EEPROM ADDRESS &H31 CONTAINS: ";OUTARY%(DX)
```

Note that only the functions listed in the sections above are valid. On return, the contents of register AH may contain a value indicating the status:

| | | |
|---|---|---|
| AH = 00h | - | Function successful, Carry flag cleared |
| AH = 01h | - | Function invalid, Carry flag set |
| AH = 02h | - | Function valid but disabled, Carry flag set |
| AH = 03h | - | Function failed, Carry flag set |

## DISK-ON-CHIP SUPPORT

The NEUTRON supports the use of M-Systems' DiskOnChip 2000 or DiskOnChip Millennium Flash Modules as solid-state disks. The notes below detail the use of the device with MS-DOS. If support is required for other operating systems, please consult Blue Chip Technology Technical Services, or M-Systems web-site at www.m-sys.com, for drivers and application notes.

The DiskOnChip 2000 and Millennium contain a built-in copy of the M-Systems industry-standard TrueFFS software, which allows the DiskOnChip to operate as a standard disk drive. The DiskOnChip may also contain the operating system thereby permitting systems to boot without a hard disk. The DiskOnChip may also be configured as the boot device in systems with a hard disk (see the section "Configuring the DiskOnChip as the First Drive").

The DiskOnChip is a self-contained device, the installation of which does not necessarily require any software installation. The basic design of the DiskOnChip allows for full upward and downward compatibility by supporting an unlimited capacity. Future DiskOnChip devices with higher densities will be fully compatible with today's capacities of 2 to 288 MBytes, and the standard DiskOnChip socket.

### *INSTALLING THE DISK-ON-CHIP*

Before installing or removing the DiskOnChip, please read the section on Electro-Static Discharges at the beginning of this manual. It is essential that you discharge any static electricity from your body before touching the board or DiskOnChip module. Use the following procedure to install the DiskOnChip:

- Align pin 1 on the DiskOnChip with pin 1 of the socket (adjacent to the battery).
- Push the DiskOnChip into the socket carefully until it is fully seated.
- Check that the DiskOnChip is installed securely, and that there are no bent pins.

**Caution: The DiskOnChip may be permanently damaged if installed incorrectly!**

To install the DiskOnChip as drive C on a system without a hard disk, set the CMOS setup of drive C to "not installed" (indicating that no physical magnetic disk is installed), and reboot the computer. The DiskOnChip will install as drive C. The DiskOnChip should then be formatted with the System files in order for it to be a bootable drive. See *"Configuring the DiskOnChip as the BOOT device"* below.

To install the DiskOnChip as drive D on a system with a hard disk, reboot the system, and the DiskOnChip will automatically install as drive D.

To install the DiskOnChip as Drive C on a system with a hard disk, see below *"Configuring the DiskOnChip as the First Drive"*.

### *CONFIGURING THE DISK-ON-CHIP AS THE BOOT DEVICE*

To configure the DiskOnChip as the boot device, the operating system files have to be copied to it. Copying the operating system files into DiskOnChip is done in exactly the same way as any other hard disk. The following is an example of a typical initialisation process:

- Set the DiskOnChip as a regular drive in your system (not a boot drive).
- Install a bootable floppy diskette in drive A and boot the system.
- At the DOS prompt, type `SYS C:` to transfer the DOS system files to the DiskOnChip (assuming the DiskOnChip is installed as drive C).
- Copy any files needed into the DiskOnChip.
- Remove the floppy diskette and reboot the system.

The system will boot from the DiskOnChip, and will allow you to run and access any files that have been copied into the DiskOnChip.

### *CONFIGURING THE DISK-ON-CHIP AS THE FIRST DRIVE*

The DiskOnChip can be configured to be installed as the last drive (default), or as the first drive in the system. When configured as the last drive, the DiskOnChip is installed as disk D if there is one other hard drive installed, and as drive C if no other hard disk is installed. When configured as the first drive, the DiskOnChip is always installed as drive C. The DiskOnChip is shipped from the factory, configured to install as the last drive. To configure the DiskOnChip to be installed as the first drive, proceed as follows:

- Boot the system and make sure the DiskOnChip is installed correctly as drive D
- At the DOS prompt type: `DUPDATE D: /FIRST /S:DOC123.EXB`

After re-booting the system, the DiskOnChip will appear as drive C:

# CONNECTORS

*E-IDE CONNECTOR **P1***

*40-way 2 mm pin header. Mating connector: 40-way 2 mm (IDC) socket.*

| PIN NO | SIGNAL | PIN NO | SIGNAL |
|---|---|---|---|
| 1 | -Reset | 2 | Ground |
| 3 | Data bit 7 (HD) | 4 | Data bit 8 (HD) |
| 5 | Data bit 6 (HD) | 6 | Data bit 9 (HD) |
| 7 | Data bit 5 (HD) | 8 | Data bit 10 (HD) |
| 9 | Data bit 4 (HD) | 10 | Data bit 11 (HD) |
| 11 | Data bit 3 (HD) | 12 | Data bit 12 (HD) |
| 13 | Data bit 2 (HD) | 14 | Data bit 13 (HD) |
| 15 | Data bit 1 (HD) | 16 | Data bit 14 (HD) |
| 17 | Data bit 0 (HD) | 18 | Data bit 15 (HD) |
| 19 | Ground | 20 | Not used |
| 21 | Drive Request | 22 | Ground |
| 23 | -IO Write (HD) | 24 | Ground |
| 25 | -IO Read (HD) | 26 | Ground |
| 27 | Drive Ready | 28 | Not Used |
| 29 | Drive Acknowledge | 30 | Ground |
| 31 | IRQ14 | 32 | HDIOCS16 |
| 33 | Address 1 (HD) | 34 | Not Used |
| 35 | Address 0 (HD) | 36 | Address 2 (HD) |
| 37 | -Chip Select 0 (HD) | 38 | -Chip Select 1 (HD) |
| 39 | Not Used | 40 | Ground |

*VGA CONNECTOR **P2***

*10-way pin header. Mating connector: 10-way 0.1” (IDC) socket.*

| PIN NO | SIGNAL | PIN NO | SIGNAL |
|---|---|---|---|
| 1 | Red | 2 | Ground |
| 3 | Green | 4 | Ground |
| 5 | Blue | 6 | Ground |
| 7 | Hsync | 8 | Ground |
| 9 | Vsync | 10 | Ground |

### *RS-232 SERIAL PORT 1 **P4** AND PORT 2 **P3***

*10-way pin headers. Mating connector: 10-way 0.1" (IDC) socket.*

| PIN NO | SIGNAL | PIN NO | SIGNAL |
|---|---|---|---|
| 1 | -Data Carrier Detect | 2 | -Data Set Ready |
| 3 | Receive Data | 4 | -Ready To Send |
| 5 | Transmit Data | 6 | -Clear To Send |
| 7 | -Data Terminal Ready | 8 | -Ring Indicator |
| 9 | Ground | 10 | NC |

### *PROPRIETARY LCD CONNECTOR **P5***

*20-way 2 mm pin header. Mating connector: 20-way 2 mm (IDC) socket.*

| PIN NO | SIGNAL | PIN NO | SIGNAL |
|---|---|---|---|
| 1 | Panel Data 0 | 2 | Switched +5 volts |
| 3 | Panel Data 1 | 4 | Switched +5 volts |
| 5 | Panel Data 2 | 6 | FLM<br>(LCD equivalent of VSYNC) |
| 7 | Ground | 8 | Line Clock |
| 9 | Panel Data 3 | 10 | MOD |
| 11 | Panel Data 4 | 12 | Ground |
| 13 | Panel Data 5 | 14 | Switched VEE |
| 15 | Panel Data 6 | 16 | Ground |
| 17 | Ground | 18 | Shift Clock |
| 19 | Panel Data 7 | 20 | Ground |

### *ECP/EPP PARALLEL PORT **P6***

*26-way pin header. Mating connector: 26-way 0.1" (IDC) socket*

| PIN NO | SIGNAL | PIN NO | SIGNAL |
|---|---|---|---|
| 1 | -Strobe | 2 | -Auto Feed XT |
| 3 | Data bit 0 | 4 | -Error |
| 5 | Data bit 1 | 6 | -Initialise |
| 7 | Data bit 2 | 8 | -Select (input) |
| 9 | Data bit 3 | 10 | Ground |
| 11 | Data bit 4 | 12 | Ground |
| 13 | Data bit 5 | 14 | Ground |
| 15 | Data bit 6 | 16 | Ground |
| 17 | Data bit 7 | 18 | Ground |
| 19 | -Acknowledge | 20 | Ground |
| 21 | Busy | 22 | Ground |
| 23 | Paper Empty | 24 | Ground |
| 25 | Select (Output) | 26 | NC |

### *FLOPPY DISK DRIVE CONNECTOR **P7***

*34-way pin header. Mating connector: 34-way 0.1" IDC socket.*

| PIN NO | SIGNAL | PIN NO | SIGNAL |
|---|---|---|---|
| 1 | Ground | 2 | +RPM/Low Current |
| 3 | Ground | 4 | Not used |
| 5 | Ground | 6 | Not used |
| 7 | Ground | 8 | -Index |
| 9 | Ground | 10 | -Motor 0 |
| 11 | Ground | 12 | -Drive select 1 |
| 13 | Ground | 14 | -Drive select 0 |
| 15 | Ground | 16 | -Motor 1 |
| 17 | Ground | 18 | +Direction |
| 19 | Ground | 20 | -Step |
| 21 | Ground | 22 | -Write Data |
| 23 | Ground | 24 | -Write Gate |
| 25 | Ground | 26 | -Track 0 |
| 27 | Ground | 28 | -Write Protect |
| 29 | Ground | 30 | -Read Data |
| 31 | Ground | 32 | +Head Select |
| 33 | Ground | 34 | +Disk Change |

### *LCD SECONDARY CONNECTOR FOR 36 BIT PANELS **P8***

*20-way 2mm header. Mating connector: 20-way 2 mm (IDC) socket.*

| PIN NO | SIGNAL | PIN NO | SIGNAL |
|---|---|---|---|
| 1 | Ground | 2 | Panel Data 35 |
| 3 | Panel Data 24 | 4 | Ground |
| 5 | Panel Data 25 | 6 | Panel Data 34 |
| 7 | Ground | 8 | Panel Data 33 |
| 9 | Panel Data 26 | 10 | Ground |
| 11 | Panel Data 27 | 12 | Panel Data 32 |
| 13 | Ground | 14 | Panel Data 31 |
| 15 | Panel Data 28 | 16 | Ground |
| 17 | Panel Data 29 | 18 | Panel Data 30 |
| 19 | Ground | 20 | Ground |

### *LCD CONNECTOR **P9***

*50-way 2mm header. Mating connector: 50-way 2 mm (IDC) socket*

| PIN NO | SIGNAL | PIN NO | SIGNAL |
|---|---|---|---|
| 1 | 5V/3V3 Link (J15) | 2 | Vertical Sync |
| 3 | Switched +12 volts | 4 | Ground |
| 5 | Switched VEE | 6 | Horizontal Sync |
| 7 | Switched +5 volts | 8 | Ground |
| 9 | Switched +5 volts | 10 | General Purpose 1 |
| 11 | Shift Clock | 12 | Ground |
| 13 | Line Clock | 14 | General Purpose 0 |
| 15 | MOD | 16 | Ground |
| 17 | FLM<br>(LCD equivalent of SYNC) | 18 | Ground |
| 19 | Panel Data 0 | 20 | Ground |
| 21 | Panel Data 1 | 22 | Panel Data 23 |
| 23 | Panel Data 2 | 24 | Ground |
| 25 | Panel Data 3 | 26 | Panel Data 22 |
| 27 | Panel Data 4 | 28 | Ground |
| 29 | Panel Data 5 | 30 | Panel Data 21 |
| 31 | Panel Data 6 | 32 | Ground |
| 33 | Panel Data 7 | 34 | Panel Data 20 |
| 35 | Panel Data 8 | 36 | Ground |
| 37 | Panel Data 9 | 38 | Panel Data 19 |
| 39 | Panel Data 10 | 40 | Ground |
| 41 | Panel Data 11 | 42 | Panel Data 18 |
| 43 | Panel Data 12 | 44 | Ground |
| 45 | Panel Data 13 | 46 | Panel Data 17 |
| 47 | Panel Data 14 | 48 | Ground |
| 49 | Panel Data 15 | 50 | Panel Data 16 |

### *BATTERY CONNECTOR **P10***

*4-way 0.1” pin header. Mating connector: 4-way Molex KK-type socket (housing 22-01-3047, crimp 97-00-0445).*

| PIN NO | SIGNAL |
|---|---|
| 1 | +3.7 Volts DC |
| 2 | Not used (key) |
| 3 | Ground |
| 4 | Ground |

### *DIGITAL INPUT/OUTPUTS **P11***

*5-way 0.1" pin header. Mating connector: 5-way JST connector (housing EHR-5, crimp BEH-001T-PP0.6).*

| PIN NO | SIGNAL |
|---|---|
| 1 | Input/Output Line bit 0 |
| 2 | Input/Output Line bit 1 |
| 3 | Input/Output Line bit 2 |
| 4 | Reserved |
| 5 | Ground |

These three IO lines are connected to bits 0-2 of port 100h (default address). Bits 0-2 are normally high, and can be pulled low by connecting them to ground.

### *AUXILIARY POWER CONNECTOR **P12***

*3-way 0.1" pin header. Mating connector: 3-way Molex KK-type socket (housing 22-01-3037, crimp 97-00-0445)*

| PIN NO | SIGNAL |
|---|---|
| 1 | -12 Volts DC |
| 2 | Ground |
| 3 | -5 Volts DC |

### *UTILITY CONNECTOR **P13***

*20-way 0.1" pin header. Mating connector: 20-way 0.1" (IDC) connector.*

| PIN NO | SIGNAL | PIN NO | SIGNAL |
|---|---|---|---|
| 1 | Speaker +ve | 2 | Speaker –ve |
| 3 | Reset +ve | 4 | Reset -ve (Ground) |
| 5 | Turbo LED +ve | 6 | Turbo LED –ve |
| 7 | Turbo switch +ve | 8 | Turbo switch -ve (Ground) |
| 9 | Power LED +ve | 10 | Power Led -ve ( Ground) |
| 11 | Reserved | 12 | Reserved |
| 13 | External SMI +ve | 14 | External SMI -ve (Ground) |
| 15 | +5V (fused) | 16 | 0 Volts (Ground) |
| 17 | External +3.6 Volt Battery | 18 | 0 Volts Battery (Ground) |
| 19 | Keyboard Data | 20 | Keyboard Clock |

## *PC104 PC/XT CONNECTOR **P14***

*64-way socket mates to PC104 add-in boards.*

| SIDE A | SIGNAL | SIDE B | SIGNAL |
|---|---|---|---|
| 1 | -IOCHCK | 1 | Ground |
| 2 | SD7 | 2 | Resetdrv |
| 3 | SD6 | 3 | +5 Volts |
| 4 | SD5 | 4 | IRQ9 |
| 5 | SD4 | 5 | -5 Volts |
| 6 | SD3 | 6 | DREQ2 |
| 7 | SD2 | 7 | -12 Volts |
| 8 | SD1 | 8 | -0WS |
| 9 | SD0 | 9 | +12 Volts |
| 10 | IOCHRDY | 10 | Ground |
| 11 | AEN | 11 | -SMEMW |
| 12 | SA19 | 12 | -SMEMR |
| 13 | SA18 | 13 | -IOW |
| 14 | SA17 | 14 | -IOR |
| 15 | SA16 | 15 | -DACK3 |
| 16 | SA15 | 16 | DREQ3 |
| 17 | SA14 | 17 | -DACK1 |
| 18 | SA13 | 18 | DREQ1 |
| 19 | SA12 | 19 | -REF |
| 20 | SA11 | 20 | CLK |
| 21 | SA10 | 21 | IRQ7 |
| 22 | SA9 | 22 | IRQ6 |
| 23 | SA8 | 23 | IRQ5 |
| 24 | SA7 | 24 | IRQ4 |
| 25 | SA6 | 25 | IRQ3 |
| 26 | SA5 | 26 | -DACK2 |
| 27 | SA4 | 27 | T/C |
| 28 | SA3 | 28 | BALE |
| 29 | SA2 | 29 | +5 Volts |
| 30 | SA1 | 30 | OSC |
| 31 | SA0 | 31 | Ground |
| 32 | Ground | 32 | Ground |

### *PC104 PC/AT CONNECTOR **P15***

*40-way socket mates to PC104 add-in boards.*

| SIDE C | SIGNAL | SIDE D | SIGNAL |
|---|---|---|---|
| 1 | Ground | 1 | Ground |
| 2 | -SBHE | 2 | -MEMCS16 |
| 3 | LA23 | 3 | -IOCS16 |
| 4 | LA22 | 4 | IRQ10 |
| 5 | LA21 | 5 | IRQ11 |
| 6 | LA20 | 6 | IRQ12 |
| 7 | LA19 | 7 | IRQ15 |
| 8 | LA18 | 8 | IRQ14 |
| 9 | LA17 | 9 | -DACK0 |
| 10 | -MEMR | 10 | DREQ0 |
| 11 | -MEMW | 11 | -DACK5 |
| 12 | SD8 | 12 | DREQ5 |
| 13 | SD9 | 13 | -DACK6 |
| 14 | SD10 | 14 | DREQ6 |
| 15 | SD11 | 15 | -DACK7 |
| 16 | SD12 | 16 | DREQ7 |
| 17 | SD13 | 17 | +5 Volts |
| 18 | SD14 | 18 | -Master |
| 19 | SD15 | 19 | Ground |
| 20 | No Connection | 20 | Ground |

### *POWER CONNECTOR **P16***

*3-way screw terminal block.*

| TERMINAL | SIGNAL |
|---|---|
| 1 | +5v |
| 2 | Ground |
| 3 | +12V |

# ERROR MESSAGES

## *AMIBIOS ERROR BEEP CODES*

The BIOS performs a **P**ower **O**n **S**elf **T**est (POST) after a reset or reboot. If errors occur during the POST, the microprocessor indicates the status of the test by writing codes to the I/O port at address 80 Hex. If the BIOS cannot find and configure the display controller then the errors are communicated through a series of audible beeps (by the speaker drive circuit). Fatal errors, which prevent the system from continuing the boot process, will produce beep codes.

Other errors are displayed textually. For these see AMIBIOS Error Messages, in the following subsection.

| BEEPS | ERROR MESSAGE | DESCRIPTION |
|---|---|---|
| 1long, 3 short | Video failure | A connection to a monitor was not detected. |
| 1 | Refresh Failure | The memory refresh circuitry on the single board PC is faulty. |
| 2 | Parity Error | Parity is not supported on this product, will not occur. |
| 3 | Base 64 KB Memory Failure | Memory failure in the first 64 KB. |
| 4 | Timer Not Operational | Memory failure in the first 64 KB of memory, or Timer 1 on the single board PC is not functioning. |
| 5 | Processor Error | The CPU on the single board PC generated an error. |
| 6 | 8042 - Gate A20 Failure | The keyboard controller (8042) may be bad. The BIOS cannot switch to protected mode. |
| 7 | Processor Exception Interrupt Error | The CPU generated an exception interrupt. |
| 8 | Display Memory Read/Write Error | System video adapter is either missing or its memory is faulty. This is not a fatal error. |
| 9 | ROM Checksum Error | ROM checksum value does not match the value encoded in BIOS. |
| 10 | CMOS Shutdown Register Rd/Wrt Error | The shutdown register for CMOS RAM failed. |
| 11 | Cache Error / External Cache Bad | The external cache is faulty. |

## *AMIBIOS ERROR CODES ON THE POST DISPLAY*

As the BIOS performs the POST after a reset or reboot, the microprocessor indicates the status of the test by writing codes to the I/O port at address 80 Hex. The following codes indicate the progress of the microprocessor during the power on test.

### *UNCOMPRESSED INIT CODE CHECKPOINTS*

| CODE (HEX) | DESCRIPTION |
|---|---|
| D0 | NMI is Disabled. CPU ID saved. Init code Checksum verification starting. |
| D1 | To do DMA init, Keyboard controller BAT test, start memory refresh and going to 4GB flat mode. |
| D3 | To start Memory sizing. |
| D4 | To come back to real mode. Execute OEM patch. Set stack. |
| D5 | E000 ROM enabled. Init code is copied to segment 0 and control to be transferred to segment 0. |
| D6 | Control is in segment 0. To check <CTRL><HOME> key and verify main BIOS checksum. If either <CTRL><HOME> is pressed or main BIOS checksum is bad, go to check point E0 else go to check point D7. |
| D7 | Main BIOS runtime code is to be decompressed and control to be passed to main BIOS in shadow RAM. |

### *BOOT BLOCK RECOVERY CODE CHECKPOINTS*

| CODE (HEX) | DESCRIPTION |
|---|---|
| E0 | On-Board Floppy Controller (if any) is initialised. To start base 512K memory test. |
| E1 | To initialise interrupt vector table. |
| E2 | To initialise DMA and interrupt controllers. |
| E6 | To enable floppy and timer IRQ, enable internal cache. |
| ED | Initialise floppy drive. |
| EE | Start looking for a diskette in drive A: and read 1st sector of the diskette. |
| EF | Floppy read error. |
| F0 | Start searching 'AMIBOOT.ROM' file in root directory. |
| F1 | 'AMIBOOT.ROM' file not present in root directory. |
| F2 | Start reading FAT table and analyse FAT to find the clusters occupied by 'AMIBOOT.ROM' file.. |
| F3 | Start reading 'AMIBOOT.ROM' file cluster by cluster. |
| F4 | 'AMIBOOT.ROM' file not of proper size. |
| F5 | Disable internal cache. |
| FB | Detect Flash type present. |
| FC | Erase Flash. |
| FD | Program Flash. |
| FF | Flash program successful. BIOS is going to restart. |

These Checkpoints are only utilised when the NEUTRON is fitted with a Flash BIOS

*RUNTIME CODE*

*(Uncompressed in F000 shadow RAM)*

| CODE (HEX) | DESCRIPTION |
|---|---|
| 03 | NMI is Disabled. To check soft reset/power-on. |
| 05 | BIOS stack set. Going to disable Cache if any. |
| 06 | POST code to be uncompressed. |
| 07 | CPU init and CPU data area init to be done. |
| 08 | CMOS checksum calculation to be done next. |
| 0B | Any initialisation before keyboard BAT to be done next. |
| 0C | KB controller I/B free. To issue the BAT command to keyboard controller. |
| 0E | Any initialisation after KB controller BAT to be done next. |
| 0F | Keyboard command byte to be written. |
| 10 | Going to issue Pin-23,24 blocking/unblocking command. |
| 11 | Going to check pressing of <INS> , <END> key during power-on. |
| 12 | To init CMOS if “Init CMOS in every boot” is set or <END> key is pressed. Going to disable DMA and Interrupt controllers. |
| 13 | Video display is disabled and port-B is initialised. Chipset init about to begin. |
| 14 | 8254 timer test about to start. |
| 19 | About to start memory refresh test. |
| 1A | Memory Refresh line is toggling. Going to check 15us ON/OFF time. |
| 23 | To read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable. |
| 24 | To do any setup before Int vector init. |
| 25 | Interrupt vector initialisation about to begin. To clear password if necessary. |
| 27 | Any initialisation before setting video mode to be done. |
| 28 | Going for monochrome mode and colour mode setting. |
| 2A | Different BUSes init (system, static, output devices) to start if present. |
| 2B | To give control for any setup required before optional video ROM check. |
| 2C | To look for optional video ROM and give control. |
| 2D | To give control to do any processing after video ROM returns control. |
| 2E | If EGA/VGA not found then do display memory R/W test. |
| 2F | EGA/VGA not found. Display memory R/W test about to begin. |
| 30 | Display memory R/W test passed. About to look for the retrace checking. |
| 31 | Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test. |
| 32 | Alternate Display memory R/W test passed. To look for the alternate display retrace checking. |
| 34 | Video display checking over. Display mode to be set next. |
| 37 | Display mode set. Going to display the power on message. |
| 38 | Different BUSes init (input, IPL, general devices) to start if present. |
| 39 | Display different BUSes initialisation error messages. |
| 3A | New cursor position read and saved. To display the Hit <DEL> message. |
| 40 | To prepare the descriptor tables. |

| | |
|---|---|
| 42 | To enter in virtual mode for memory test. |
| 43 | To enable interrupts for diagnostics mode. |
| 44 | To Initialise data to check memory wrap around at 0:0. |

| | |
|---|---|
| 45 | Data initialised. Going to check for memory wrap around at 0:0 and finding the total system memory size. |
| 46 | Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory. |
| 47 | Pattern to be tested written in extended memory. Going to write patterns in base 640k memory. |
| 48 | Patterns written in base memory. Going to find out amount of memory below 1M memory. |
| 49 | Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory. |
| 4B | Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point# 4Eh). |
| 4C | Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M. |
| 4D | Memory above 1M cleared. (SOFT RESET) Going to save the memory size. (Go to check point# 52h). |
| 4E | Memory test started. (NOT SOFT RESET) About to display the first 64k memory size. |
| 4F | Memory size display started. This will be updated during memory test. Going for sequential and random memory test. |
| 50 | Memory testing/initialisation below 1M complete. Going to adjust displayed memory size for relocation/ shadow. |
| 51 | Memory size display adjusted due to relocation/ shadow. Memory test above 1M to follow. |
| 52 | Memory testing/initialisation above 1M complete. Going to save memory size information. |
| 53 | Memory size information is saved. CPU registers are saved. Going to enter in real mode. |
| 54 | Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI. |
| 57 | A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow. |
| 58 | Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message. |
| 59 | Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test. |
| 60 | DMA page register test passed. To do DMA#1 base register test. |
| 62 | DMA#1 base register test passed. To do DMA#2 base register test. |
| 65 | DMA#2 base register test passed. To program DMA unit 1 and 2. |
| 66 | DMA unit 1 and 2 programming over. To Initialise 8259 interrupt controller. |
| 7F | Extended NMI sources enabling is in progress. |
| 80 | Keyboard test started. clearing output buffer, checking for stuck key, to issue keyboard reset command. |
| 81 | Kb reset error/stuck key found. To issue kb controller test command. |
| 82 | Keyboard controller interface test over. To write command byte and init circular buffer. |
| 83 | Command byte written, Global data init done. To check for lock-key. |
| 84 | Lock-key checking over. To check for memory size mismatch with CMOS. |

| | |
|---|---|
| 85 | Memory size check done. To display soft error and check for password or bypass setup. |
| 86 | Password checked. About to do programming before setup. |
| 87 | Programming before setup complete. To uncompress SETUP code and execute CMOS setup. |
| 88 | Returned from CMOS setup program and screen is cleared. About to do programming after setup. |
| 89 | Programming after setup complete. Going to display power on screen message. |
| 8B | First screen message displayed. <WAIT...> message displayed. PS/2 Mouse check and extended BIOS data area allocation to be done. |
| 8C | Setup options programming after CMOS setup about to start. |
| 8D | Going for hard disk controller reset. |
| 8F | Hard disk controller reset done. Floppy setup to be done next. |
| 91 | Floppy setup complete. Hard disk setup to be done next. |
| 95 | Init of different BUSes optional ROMs from C800 to start. |
| 96 | Going to do any init before C800 optional ROM control. |
| 97 | Any init before C800 optional ROM control is over. Optional ROM check and control will be done next. |
| 98 | Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache. |
| 99 | Any initialisation required after optional ROM test over. Going to setup timer data area and printer base address. |
| 9A | Return after setting timer and printer base address. Going to set the RS-232 base address. |
| 9B | Returned after RS-232 base address. Going to do any initialisation before Coprocessor test |
| 9C | Required initialisation before Coprocessor is over. Going to Initialise the Coprocessor next. |
| 9D | Coprocessor initialised. Going to do any initialisation after Coprocessor test. |
| 9E | Initialisation after Coprocessor test is complete. Going to check extd keyboard, keyboard ID and num-lock. Keyboard ID command to be |
| A2 | Going to display any soft errors. |
| A3 | Soft error display complete. Going to set keyboard typematic rate. |
| A4 | Keyboard typematic rate set. To program memory wait states. |
| A5 | Going to enable parity/NMI. |
| A7 | NMI and parity enabled. Going to do any initialisation required before giving control to optional ROM at E000. |
| A8 | Initialisation before E000 ROM control over. E000 ROM to get control next. |
| A9 | Returned from E000 ROM control. Going to do any initialisation required after E000 optional ROM control. |
| AA | Initialisation after E000 optional ROM control is over. Going to display the system configuration. |
| AB | To uncompress DMI data and execute DMI POST init. |
| B0 | System configuration is displayed. |
| B1 | Going to copy any code to specific area. |
| 00 | Copying of code to specific area done. Going to give control to INT-19 boot loader. |

### *AMIBIOS ERROR MESSAGES*

Textual error messages are displayed in the following format:

*ERROR Message Line 1*
*ERROR Message Line 2*

For most displayed error messages, there is only one message. If a second message appears, it is "RUN SETUP". If this message occurs, press <F1> to run Setup Utility.

| ERROR MESSAGE | EXPLANATION |
|---|---|
| 8042 Gate - A20 Error | Gate A20 on the keyboard controller (8042) is not working. Replace the 8042. |
| Address Line Short! | Error in the address decoding circuitry on the single board PC. |
| Cache Memory Bad, Do Not Enable Cache! | Cache memory is defective. Replace it. |
| CH-2 Timer Error | Most AT systems include two timers. There is an error in timer 2. |
| CMOS Battery State Low | CMOS RAM is powered by a battery. The battery power is low. Replace the battery. |
| CMOS Checksum Failure | After CMOS RAM values are saved, a checksum value is generated for error checking. The previous value is different from the current value. Run AMIBIOS Setup. |
| CMOS System Options Not Set | The values stored in CMOS RAM are either corrupt or non-existent. Run Setup. |
| CMOS Display Type Mismatch | The video type in CMOS RAM does not match the type detected by the BIOS. Run AMIBIOS Setup. |
| CMOS Memory Size Mismatch | The amount of memory on the single board PC is different than the amount in CMOS RAM. Run AMIBIOS Setup. |
| CMOS Time and Date Not Set | Run Standard CMOS Setup to set the date and time in CMOS RAM. |
| Diskette Boot Failure | The boot disk in floppy drive A: is corrupt. It cannot be used to boot the system. Use another boot disk and follow the screen instructions. |
| Display Switch Not Proper | The display jumper is not implemented on this product, this error will not occur. |
| DMA Error | Error in the DMA controller. |
| DMA #1 Error | Error in the first DMA channel. |
| DMA #2 Error | Error in the second DMA channel. |
| FDD Controller Failure | The BIOS cannot communicate with the floppy disk drive controller. Check all appropriate connections after the system is powered down. |
| HDD Controller Failure | The BIOS cannot communicate with the hard disk drive controller. Check all appropriate connections after the system is powered down. |
| INTR #1 Error | Interrupt channel 1 failed POST. |
| INTR #2 Error | Interrupt channel 2 failed POST. |
| Invalid Boot Diskette | The BIOS can read the disk in floppy drive A:, but cannot boot the system. Use another boot disk. |
| Keyboard Is Locked...Unlock It | The keyboard lock on the system is engaged. The system must be unlocked to continue. |
| Keyboard Error | There is a timing problem with the keyboard. Set the Keyboard option in Standard CMOS Setup to Not Installed to skip the keyboard POST routines. |
| KB/Interface Error | There is an error in the keyboard connector. |
| Off Board Parity Error | Parity error in memory installed in an expansion slot. The format is: OFF BOARD PARITY ERROR ADDR (HEX) = (XXXX) Where “XXXX” is the hex address where the error occurred. |
| On Board Parity Error | Parity is not supported on this product, this error will not occur. |
| Parity Error ???? | Parity error in system memory at an unknown address. |

## *ISA NMI MESSAGES*

| ISA NMI MESSAGE | EXPLANATION |
|---|---|
| Memory Parity Error at XXXXX | Memory failed.<br>If the memory location can be determined, it is displayed as XXXXX. If not, the message is Memory Parity Error ????. |
| I/O Card Parity Error at XXXXX | An expansion card failed.<br>If the address can be determined, it is displayed as XXXXX.<br>If not, the message is I/O Card Parity Error ????. |
| DMA Bus Time-out | A device has driven the bus signal for more than 7.8 microseconds. |

## *PCI CONFIGURATION ERROR MESSAGES*

The following PCI messages are displayed as a group with bus, device and function information.

<'NVRAM Checksum Error, NVRAM Cleared'>, \ ; String
<'System Board Device Resource Conflict'>, \ ; String
<'Primary Output Device Not Found'>, \ ; String
<'Primary Input Device Not Found'>, \ ; String
<'Primary Boot Device Not Found'>, \ ; String
<'NVRAM Cleared By Jumper'>, \ ; String
<'NVRAM Data Invalid, NVRAM Cleared'>, \ ; String
<'Static Device Resource Conflict'>, \ ; String

The following messages chain together to give a message such as:
"PCI I/O Port Conflict: Bus: 00, Device 0D, Function: 01".

<'PCI I/O Port Conflict:'>, \ ; String
<'PCI Memory Conflict: '>, \ ; String
<'PCI IRQ Conflict: '>, \ ; String
<' Bus '>, \ ; String
<', Device '>, \ ; String
<', Function '>, \ ; String
<'PCI Error Log is Full.'>, \ ; String
<'Floppy Disk Controller Resource Conflict '>, \ ; Text
<'Primary IDE Controller Resource Conflict '>, \ ; Text
<'Secondary IDE Controller Resource Conflict '>, \ ; Text
<'Parallel Port Resource Conflict '>, \ ; Text
<'Serial Port 1 Resource Conflict '>, \ ; Text
<'Serial Port 2 Resource Conflict '>, \ ; Text

If more than 15 PCI conflict errors are detected, the “log full” message is displayed.

# BOARD LAYOUT